

TP70H135G4PJSGB

700V SuperGaN® GaN FET in PQFN 5 × 6 mm Industry Standard Package (source tab)

Description

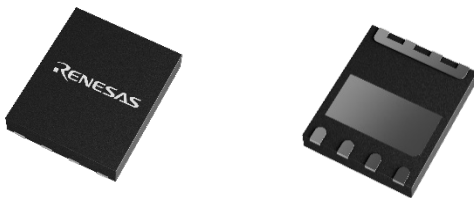
The TP70H135G4PJSGB 700V, 135mΩ Gallium Nitride (GaN) FET is a normally-off switch that uses Renesas' Gen IV plus platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior performance, standard drive, ease of adoption and reliability.

The Gen IV plus SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

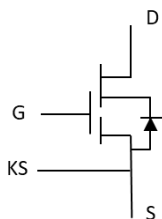
Benefits

- Superior normally off architecture with D-mode GaN HEMT
- Compatible with standard silicon drivers
- Enhanced noise immunity with high threshold voltage and no negative gate drive requirement
- Enables high-efficiency, high power density, and reliable power conversion in hard- and soft-switched circuits
- Facilitates cost-effective GaN adoption, reducing system size, weight, and costs

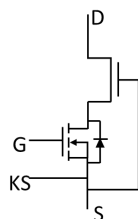
Product Diagrams



TP70H135G4PJSGB PQFN 5 × 6 mm



Symbol



Cascode Device Structure

Features

- Ultra-fast switching Gen IV plus GaN
- JEDEC-qualified GaN technology
- Robust design, defined by:
  - Transient over-voltage capability
  - Operation with E-mode gate drivers without need for Zener protection
- Extremely low crossover loss
- Negligible Qrr
- RoHS compliant and Halogen-free packaging
- Low reverse conduction drop  $V_{SD}$

Applications

- Consumer
- Power adapters
- Low power SMPS
- Lighting



Specifications

$V_{DS}$ (V)	700
$V_{DSS(TR)}$ (V) maximum	800
$R_{DS(on)}$ (mΩ) maximum	169
$Q_{OSS}$ (nC) typical	29.4
$Q_G$ (nC) typical	5.9

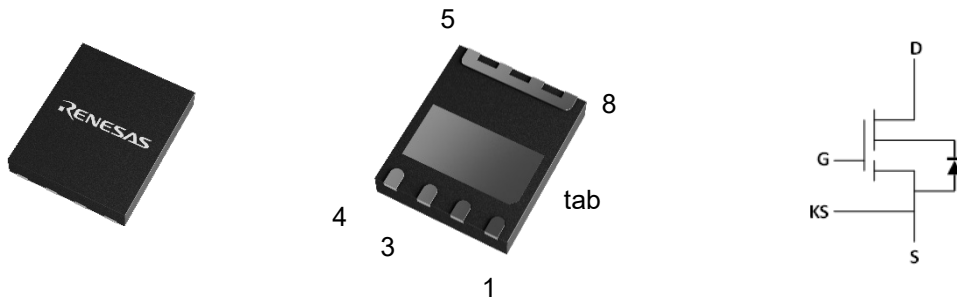
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# 1. Pin Information



## 1.1 Pin Assignments

Figure 1. Pin Assignments – Bottom View

## 1.2 Pin Descriptions

Pin Number	Pin Name	Description
1, 2	NC	No connection.
3	KS	Kelvin Source.
4	G	Gate.
5, 6, 7, 8	G	Drain.
tab	S	Source.

## 2. Specifications

### 2.1 Absolute Maximum Ratings

$T_c = 25^\circ\text{C}$  unless otherwise stated.

**Caution:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Symbol	Parameter	Minimum	Maximum	Test Condition	Unit
$V_{DSS}$	Drain to source voltage	-	700	$V_{GS} = 0V$ , Test as per JEDEC	V
$V_{DSS(TR)}, \text{non-repetitive}$	Transient drain to source voltage, non-repetitive	-	800	$V_{GS} = 0V$ , spike duration < 30 $\mu\text{s}$	
$V_{DSS(TR)}, \text{pulsed}$	Drain to source voltage, pulsed	-	750	$V_{GS} = 0V$ , spike duration < 5 $\mu\text{s}$	
$V_{GSS}$	Gate to source voltage	-20	+20	-	
$P_D$	Maximum power dissipation	-	69.4	$T_c = 25^\circ\text{C}$	W
$I_D$	Continuous drain current at $T_c = 25^\circ\text{C}$	-	15.8	$V_{GS} = 6V$ , $V_{DS}$ can be positive and negative	
	Continuous drain current at $T_c = 100^\circ\text{C}$	-	10		
$I_{D(PULSE)}$	Pulsed drain current at $T_c = 25^\circ\text{C}$	-	54	$V_{GS} = 6V$ , pulse width = 10 $\mu\text{s}$ $V_{DS}$ can be positive and negative	A
	Pulsed drain current at $T_c = 100^\circ\text{C}$	-	47		
$I_{SD(PULSE)}$	Pulsed reverse drain current at $T_c = 25^\circ\text{C}$	-	54	$V_{GS} = 0V$ , pulse width = 10 $\mu\text{s}$ , $V_{DS} < 0$	
	Pulsed reverse drain current at $T_c = 100^\circ\text{C}$	-	47		
$T_J$	Operating temperature junction	-55	+150	-	$^\circ\text{C}$
$T_S$	Storage temperature	-55	+150	Max shelf life depends on storage conditions	$^\circ\text{C}$
$T_{SOLD}$	Reflow soldering temperature <sup>[1]</sup>	-	260	-	$^\circ\text{C}$

1. Reflow MSL3.

### 2.2 Thermal Specifications

Symbol	Parameter	Typical Value	Unit	Test Condition
$R_{\theta JC}$	Junction-to-case	1.8	$^\circ\text{C}/\text{W}$	-
$R_{\theta JA}$	Junction-to-ambient	53		Device on 40 × 40 mm × 1.5mm epoxy PCB FR4 with 6cm <sup>2</sup> (one layer, 70 $\mu\text{m}$ thickness) copper area for tab (source) connection and cooling. PCB is vertical without air stream cooling.

## 2.3 Electrical Specifications – Forward Device

T<sub>J</sub> = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V <sub>DSS(BL)</sub>	Maximum drain-source voltage	V <sub>GS</sub> = 0V	700	-	-	V
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 0.5mA	1.5	2	2.5	V
ΔV <sub>GS(th)/T<sub>J</sub></sub>	Gate threshold voltage temperature coefficient		-	-7.6	-	mV/°C
R <sub>DS(on)eff</sub>	Drain-source on-resistance	V <sub>GS</sub> = 6V, I <sub>D</sub> = 4A, T <sub>J</sub> = 25°C	-	135	169	mΩ
		V <sub>GS</sub> = 6V, I <sub>D</sub> = 4A, T <sub>J</sub> = 150°C	-	276	-	
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>DS</sub> = 700V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 25°C	-	0.7	10	μA
		V <sub>DS</sub> = 700V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C	-	5	-	
I <sub>GSS</sub>	Gate-to-source forward leakage current <sup>[1]</sup>	V <sub>GS</sub> = 20V	-	-	10	μA
	Gate-to-source reverse leakage current <sup>[1]</sup>	V <sub>GS</sub> = -20V	-	-	-10	
C <sub>ISS</sub>	Input capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 400V, f = 1MHz	-	485	-	pF
C <sub>OSS</sub>	Output capacitance		-	29.5	-	
C <sub>RSS</sub>	Reverse transfer capacitance		-	2.7	-	
C <sub>O(er)</sub>	Output capacitance, energy related <sup>[2]</sup>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 400V	-	41.5	-	pF
C <sub>O(tr)</sub>	Output capacitance, time related <sup>[3]</sup>		-	73.5	-	
Q <sub>G</sub>	Total gate charge	V <sub>DS</sub> = 400V, V <sub>GS</sub> = 0V to 6V, I <sub>D</sub> = 4A	-	5.9	-	nC
Q <sub>GS</sub>	Gate-source charge		-	1.3	-	
Q <sub>GD</sub>	Gate-drain charge		-	2.4	-	
Q <sub>OSS</sub>	Output charge	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 400V	-	29.4	-	nC
t <sub>D(on)</sub>	Turn-on delay	V <sub>DS</sub> = 400V, V <sub>GS</sub> = 0 to 6V, R <sub>G</sub> = 30Ω, I <sub>D</sub> = 4A, (see Figure 15)	-	22.2	-	ns
t <sub>R</sub>	Rise time		-	3.6	-	
t <sub>D(off)</sub>	Turn-off delay		-	44.6	-	
t <sub>F</sub>	Fall time		-	11	-	

1. MOSFET has integrated ESD Protection Circuit
2. Equivalent capacitance to give same stored energy from 0V to 400V.
3. Equivalent capacitance to give same charging time from 0V to 400V.

## 2.4 Electrical Specifications – Reverse Device

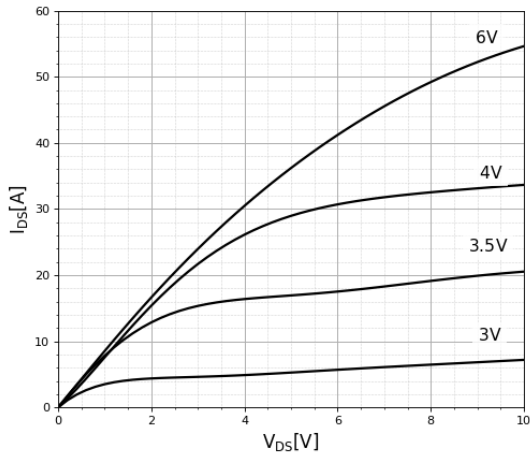
T<sub>J</sub> = 25°C unless otherwise stated.

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
V <sub>SD</sub>	Reverse voltage <sup>[1]</sup>	V <sub>GS</sub> = 0V, I <sub>S</sub> = 4A	-	1.3	-	V
		V <sub>GS</sub> = 0V, I <sub>S</sub> = 2A	-	1.1	-	

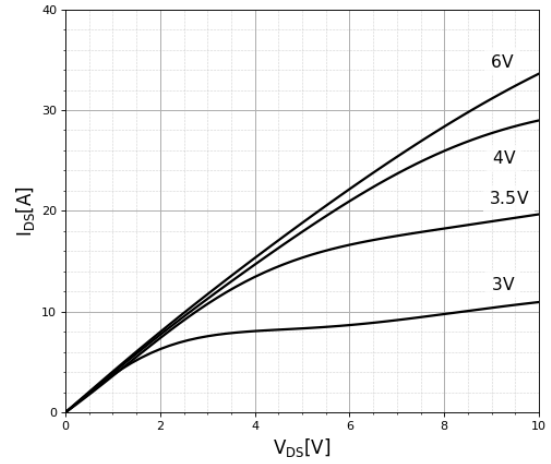
1. Reverse recovery charge is negligible enabled by the LV Si FET technology.

### 3. Typical Performance Graphs

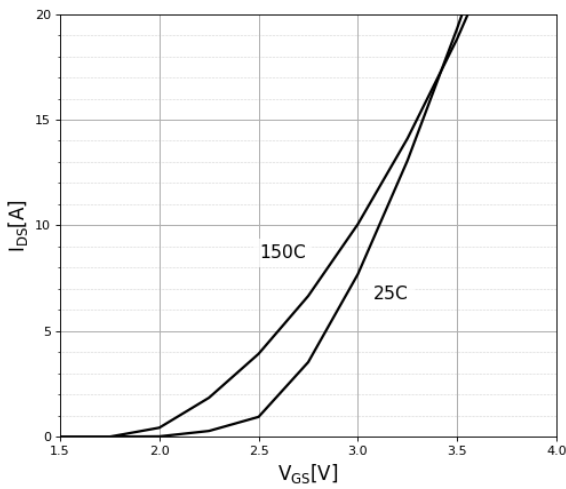
$T_c = 25^\circ\text{C}$  unless otherwise stated.



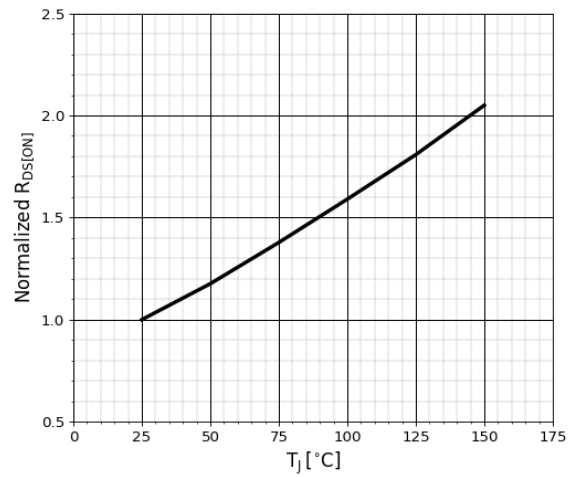
**Figure 2. Typical Output Characteristics,  $T_J = 25^\circ\text{C}$**   
Parameter:  $V_{GS}$



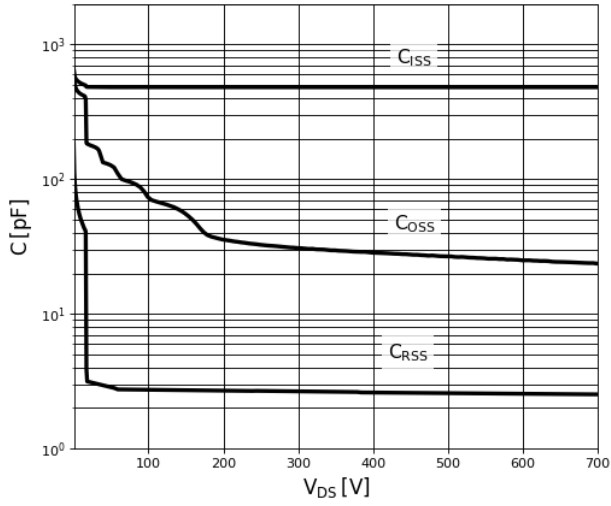
**Figure 3. Typical Output Characteristics,  $T_J = 150^\circ\text{C}$**   
Parameter:  $V_{GS}$



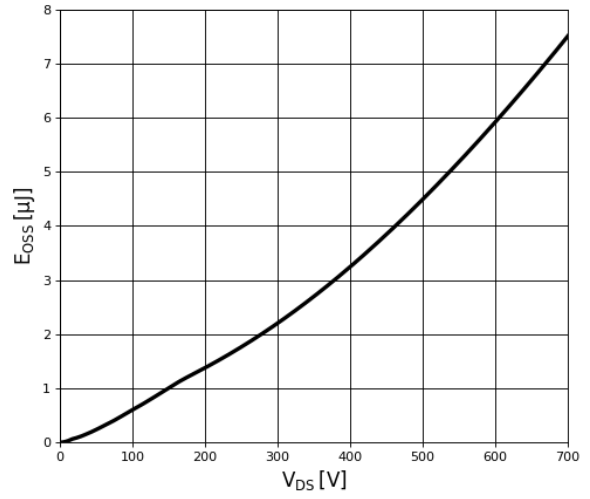
**Figure 4. Typical Transfer Characteristics,**  
 $V_{DS} = 10\text{V}$ , Parameter:  $T_J$



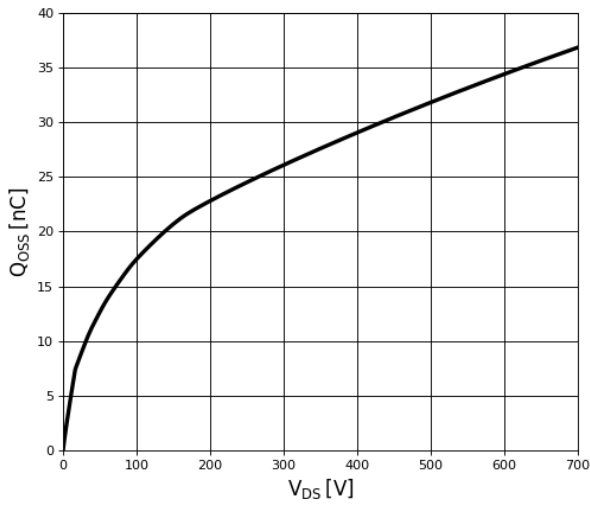
**Figure 5. Normalized On-resistance,**  
 $I_D = 4\text{A}$ ,  $V_{GS} = 6\text{V}$



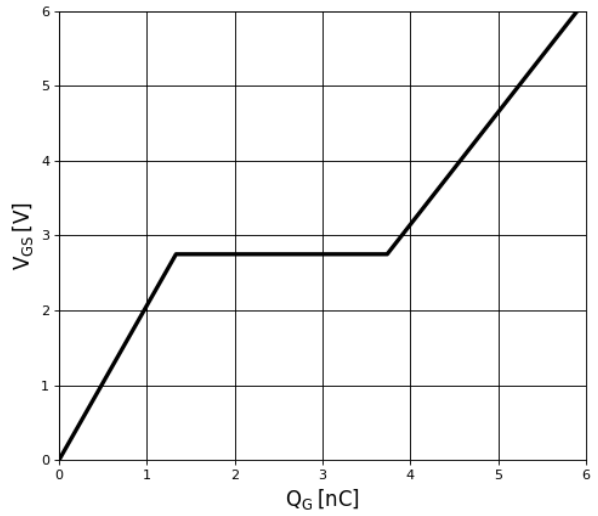
**Figure 6. Typical Capacitance,**  
V<sub>GS</sub> = 0V, f = 1MHz



**Figure 7. Typical Coss Stored Energy**



**Figure 8. Typical Q<sub>oss</sub>**



**Figure 9. Typical Gate Charge,**  
I<sub>DS</sub> = 4A, V<sub>DS</sub> = 400V

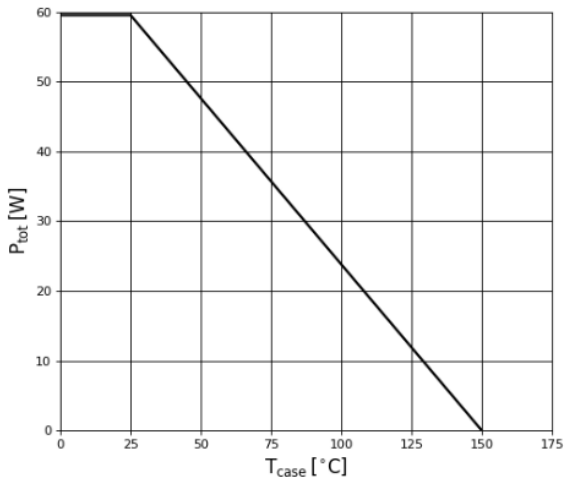


Figure 10. Power Dissipation

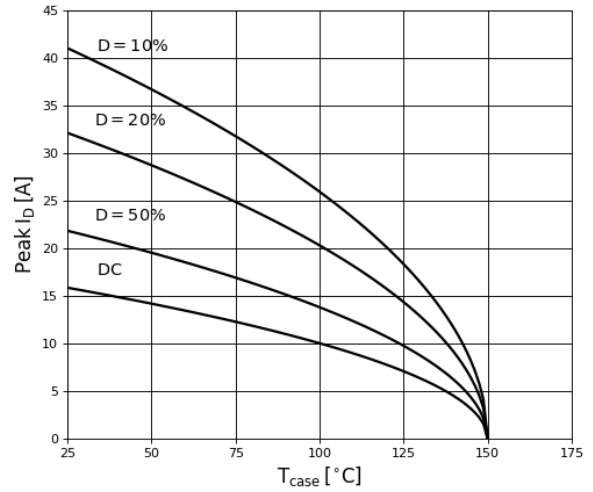


Figure 11. Current Derating,  
Pulse width ≤ 10μs, V<sub>GS</sub> ≥ 6V

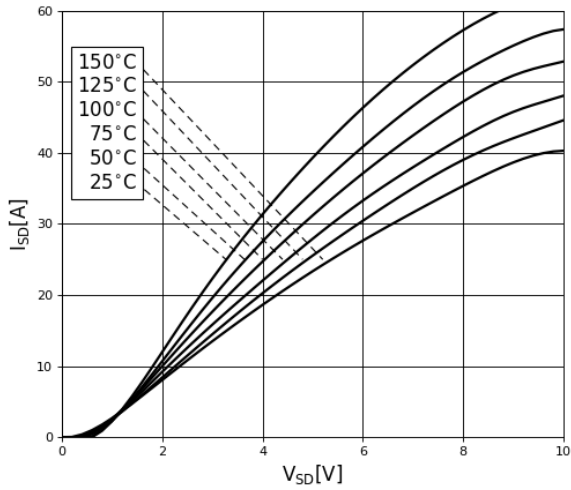


Figure 12. Forward Characteristics of Rev. Diode,  
I<sub>S</sub> = f(V<sub>SD</sub>), Parameter: T<sub>J</sub>

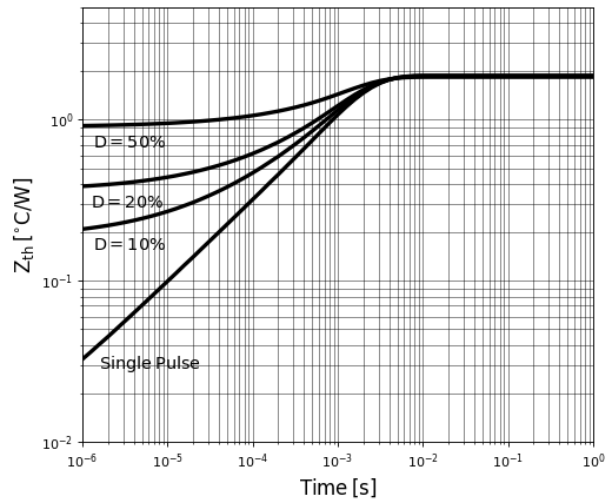


Figure 13. Transient Thermal Resistance

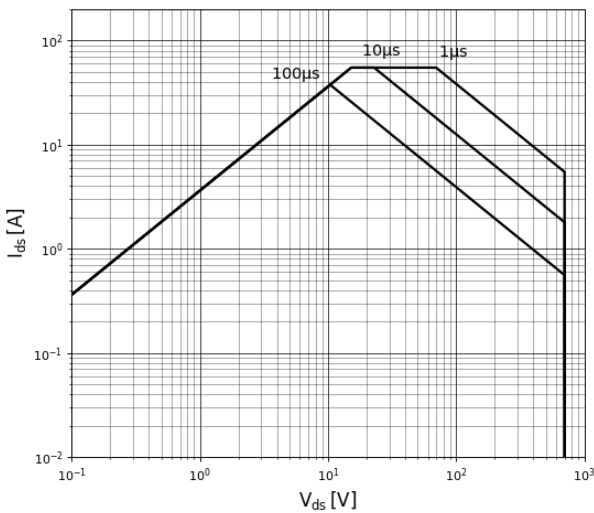


Figure 14. Safe Operating Area T<sub>C</sub> = 25°C

## 4. Test Circuits and Waveforms

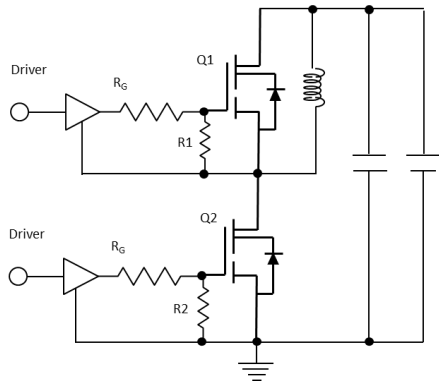


Figure 15. Switching Time Test Circuit

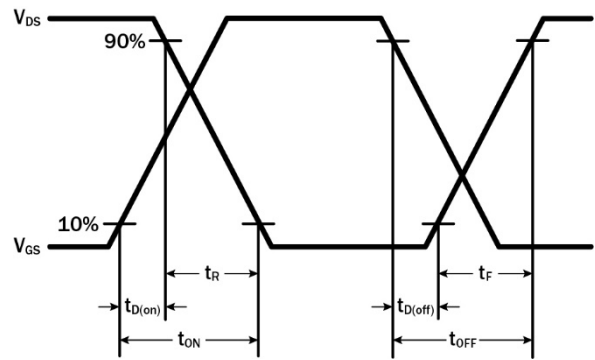


Figure 16. Switching Time Waveform

## 5. Package Outline Drawings

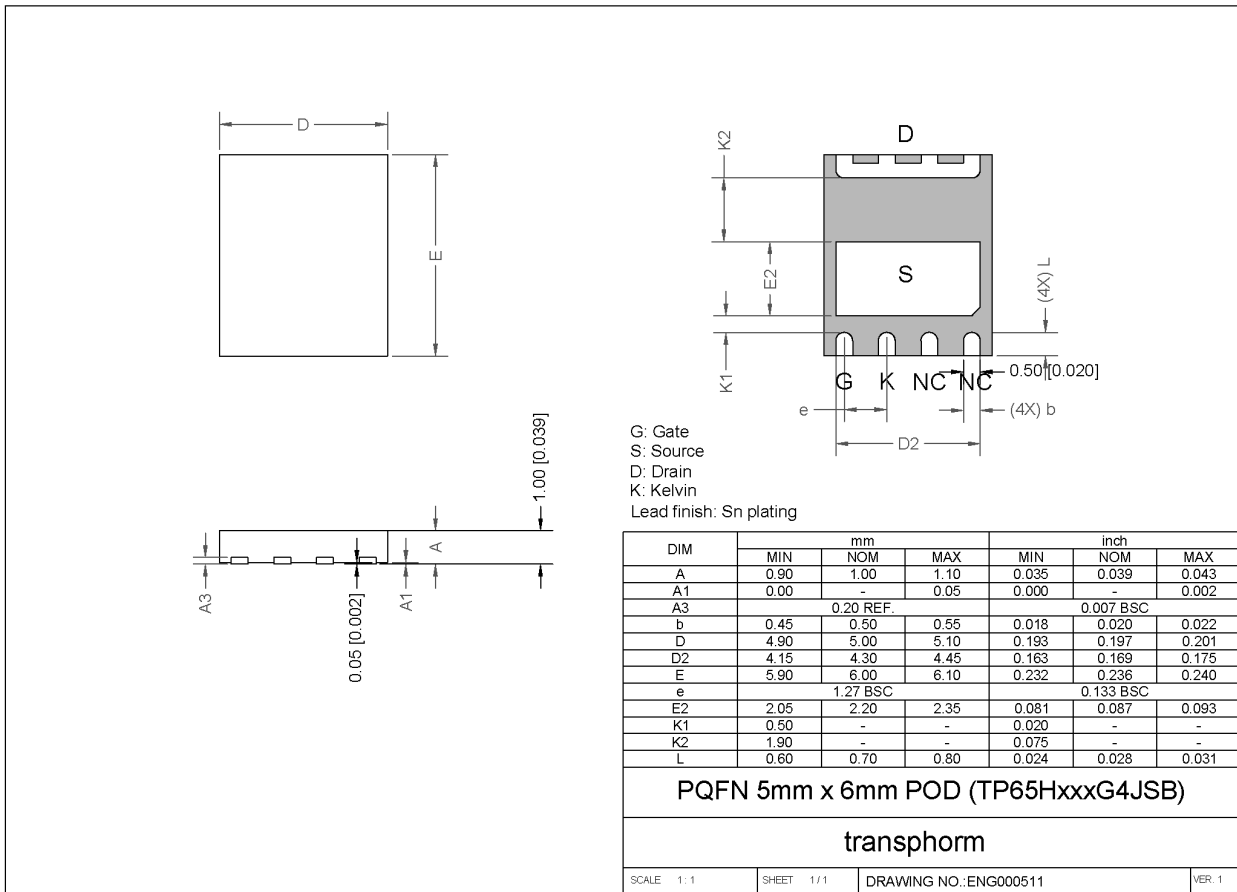


Figure 17. Package Outline Drawing – 5 × 6 mm PQFN

## 6. Related Information

All technical documents for Renesas GaN Power devices are accessible from the [GaN Power Solutions](#) page.

- Reference designs
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

## 7. Ordering Information

Part Number	Package Description	Package Configuration
TP70H135G4PJSGB-TR	PQFN 5 × 6 mm Industry Standard Package	Source tab

1. "-TR" suffix refers to tape and reel.

## 8. Revision History

Revision	Date	Description
1.00	Feb 20, 2026	Initial release.

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