

TW2866

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4-Channel Video Decoders and Audio Codecs and Video Encoder for Security Applications

The TW2866 includes four high quality NTSC/PAL/SECAM video decoders that convert analog composite video signal to digital component YCbCr data for security applications. Each channel contains 10-bit ADCs and proprietary clamp and gain controllers and utilizes 4H comb filter for separating luminance and chrominance to reduce cross noise artifacts. The TW2866 adopts the image enhancement techniques such as IF compensation filter, CTI and programmable peaking. TW2866 also includes one NTSC/PAL video encoder with two 10-bit DACs to support CVBS and YC output. The TW2866 also includes audio CODEC which has five audio analog-to-digital converters and one digital-to-analog converter. A built-in audio controller can generate digital outputs for recording/mixing and accepts digital input for playback.

- Provides multichannel audio mixed analog output
- Supports I2S/DSP master/slave interface for record output and playback input
- PCM 8-/16-bit and u-Law/A-Law 8-bit for audio word length
- Programmable audio sample rate that covers popular frequencies of 8/16/32/44.1/48kHz
- Supports a two-wire serial host interface
- Integrated one video encoder and two 10-bit video CMOS DACs
- Integrated clock PLL for 108MHz clock output
- Ultra low power consumption (typical 666.84mW)
- 128 pin LQFP package

Features

- Accepts all NTSC(M/4.43) / PAL(B/D/G/H/I/K/L/M/N/60)/SECAM standards with auto detection
- Integrated four video analog anti-aliasing filters and 10-bit CMOS ADCs
- High performance adaptive 4H comb filters for all NTSC/PAL standards
- IF compensation filter for improvement of color demodulation
- Color Transient Improvement (CTI)
- Automatic white peak control
- Programmable hue, saturation, contrast, brightness and sharpness
- Proprietary fast video locking system for non-realtime application
- Supports the standard ITU-R BT.656 format or time multiplexed output with 54/108MHz
- Provides simultaneous four channel full D1 and CIF time-multiplexed outputs with 54MHz
- Integrated five audio ADCs and one audio DAC

Block Diagram

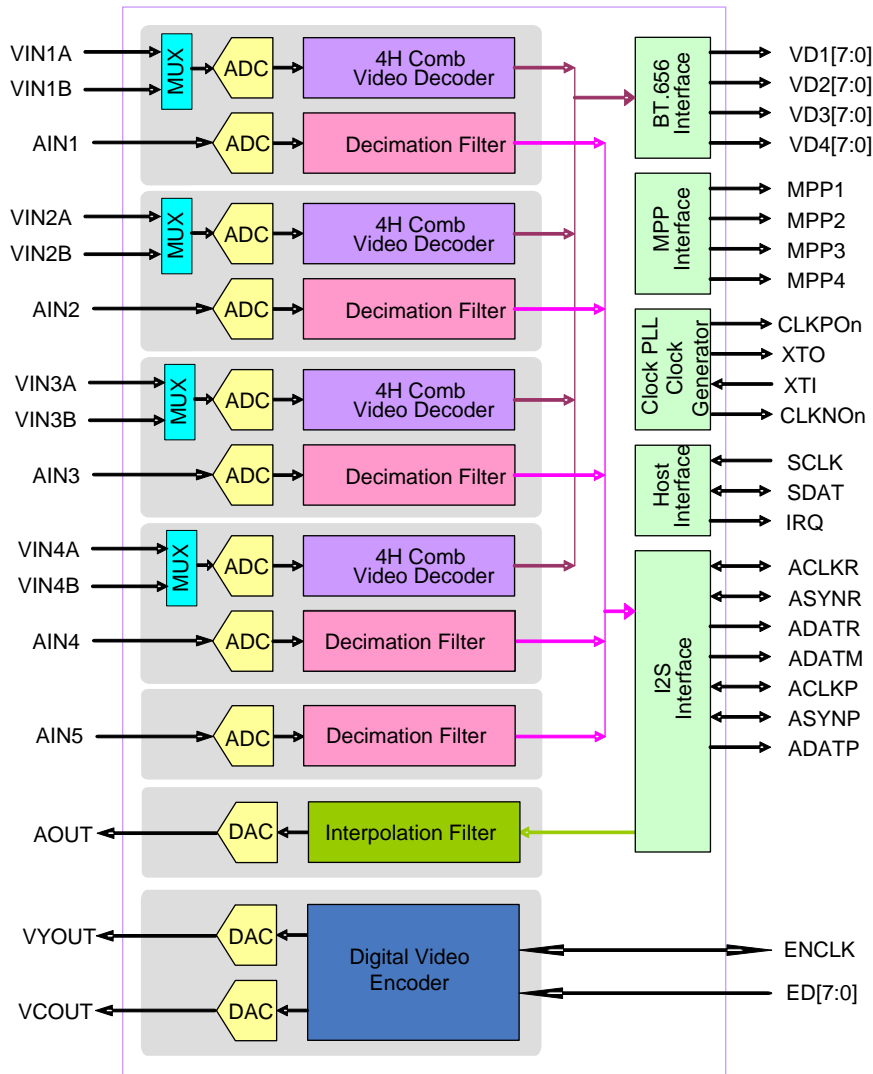


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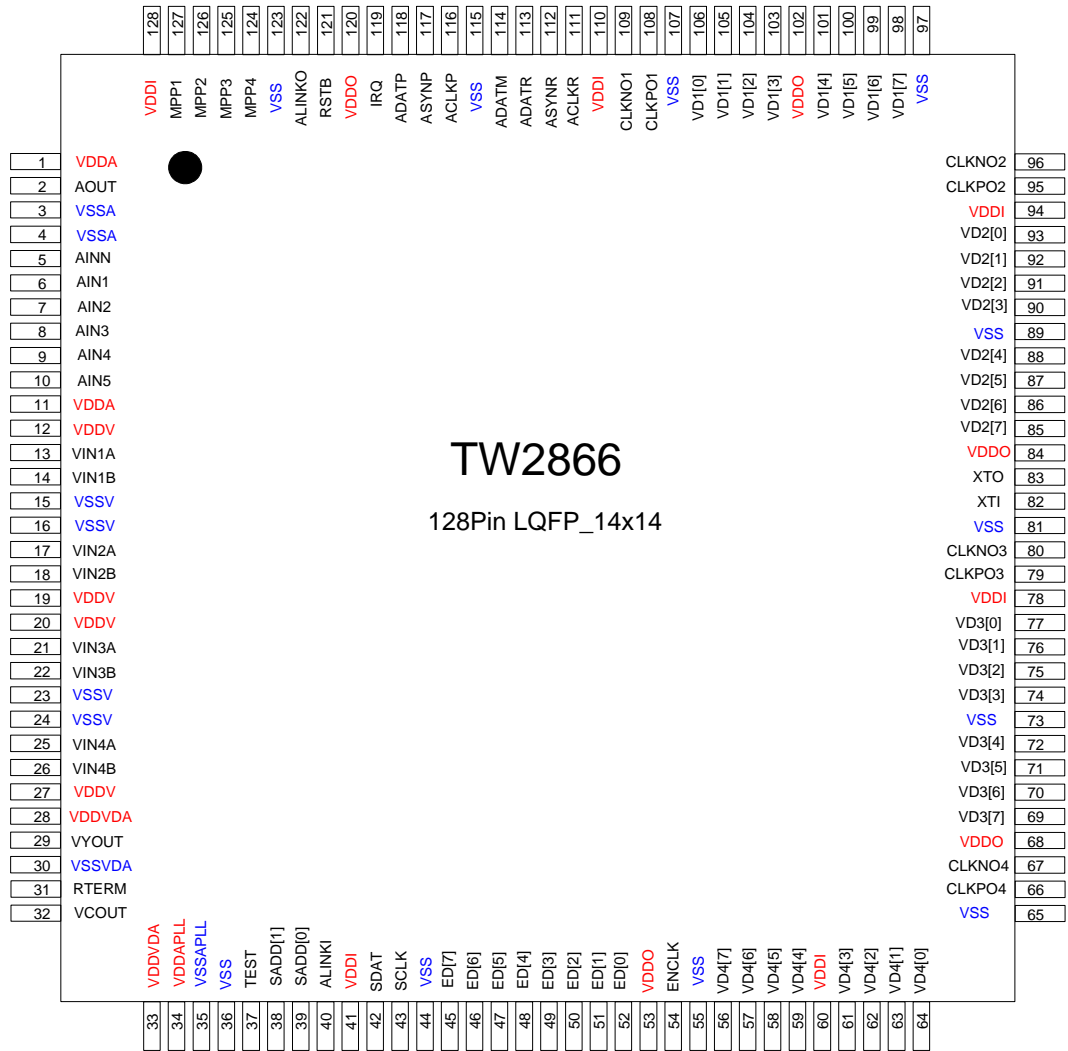
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Pin Diagram



Pin Description

Analog Video/Audio Interface Pins

| Name | Number | Type | Description |
|-------|--------|------|---------------------------------------|
| VIN1A | 13 | A | Composite video input A of channel 1. |
| VIN1B | 14 | A | Composite video input B of channel 1. |
| VIN2A | 17 | A | Composite video input A of channel 2. |
| VIN2B | 18 | A | Composite video input B of channel 2. |
| VIN3A | 21 | A | Composite video input A of channel 3. |
| VIN3B | 22 | A | Composite video input B of channel 3. |
| VIN4A | 25 | A | Composite video input A of channel 4. |
| VIN4B | 26 | A | Composite video input B of channel 4. |
| VYOUT | 29 | A | Analog video output. |
| VCOUT | 32 | A | Analog video output. |
| RTERM | 31 | A | Analog video resistance term. |
| AIN1 | 6 | A | Audio input of channel 1. |
| AIN2 | 7 | A | Audio input of channel 2. |
| AIN3 | 8 | A | Audio input of channel 3. |
| AIN4 | 9 | A | Audio input of channel 4. |
| AIN5 | 10 | A | Audio input of channel 5. |
| AINN | 5 | A | Audio input negative control. |
| AOUT | 2 | A | Audio mixing output. |

Digital Video/Audio Interface Pins

| Name | Number | Type | Description |
|----------|-----------------------------------|------|--|
| VD1[7:0] | 98,99,100,101, 103,104,105,106 | O | Video data output of channel 1. |
| VD2[7:0] | 85,86,87,88, 90,91,92,93 | O | Video data output of channel 2. |
| VD3[7:0] | 69,70,71,72, 74,75,76,77 | O | Video data output of channel 3. |
| VD4[7:0] | 56,57,58,59, 61,62,63,64 | O | Video data output of channel 4. |
| MPP1 | 127 | O | HS/VS/FLD/ACTIVE/NOVID of channel 1. |
| MPP2 | 126 | O | HS/VS/FLD/ACTIVE/NOVID of channel 2. |
| MPP3 | 125 | O | HS/VS/FLD/ACTIVE/NOVID of channel 3. |
| MPP4 | 124 | O | HS/VS/FLD/ACTIVE/NOVID of channel 4. |
| ED[7:0] | 45,46,47,48, 49,50,51,52 | I | ITU-R656 Video data input. |
| ACLKR | 111 | IO | Audio serial clock input/output of record. |
| ASYNR | 112 | IO | Audio serial sync input/output of record. |
| ADATR | 113 | O | Audio serial data output of record. |
| ADATM | 114 | O | Audio serial data output of mixing. |
| ACLKP | 116 | IO | Audio serial clock input/output of playback. |
| ASYNP | 117 | IO | Audio serial sync input/output of playback. |
| ADATP | 118 | I | Audio serial data input of playback. |
| ALINKI | 40 | I | Audio Multi-chip operation serial input. |
| ALINKO | 122 | O | Audio Multi-chip operation serial output. |

System Control Pins

| Name | Number | Type | Description |
|-----------|--------|------|--|
| RSTB | 121 | I | System reset. |
| XTI | 82 | I | Crystal 54MHz(27MHz) connection or Oscillator clock input. |
| XTO | 83 | O | For crystal 54MHz(27MHz) connection. |
| CLKPO1 | 108 | O | 27/54/108MHz clock output. |
| CLKNO1 | 109 | O | 27/54/108MHz clock output. |
| CLKPO2 | 95 | O | 27/54/108MHz clock output. |
| CLKNO2 | 96 | O | 27/54/108MHz clock output. |
| CLKPO3 | 79 | O | 27/54/108MHz clock output. |
| CLKNO3 | 80 | O | 27/54/108MHz clock output. |
| CLKPO4 | 66 | O | 27/54/108MHz clock output. |
| CLKNO4 | 67 | O | 27/54/108MHz clock output. |
| ENCLK | 54 | I/O | Input/output clock for ED[7:0] video data input. |
| TEST | 37 | I | Test pin. Connect to ground. |
| SCLK | 43 | I | Serial control clock line. |
| SDAT | 42 | IO | Serial control data line. |
| SADD[1:0] | 38,39 | I | Serial control address. |
| IRQ | 119 | O | Interrupt request output. |

Power and Ground Pins

| Name | Number | Type | Description |
|---------|---|------|--|
| VDDI | 41,60,78,94 110,128 | P | 1.2V Power for internal logic. |
| VDDO | 53,68,84, 102,120 | P | 3.3V Power for output driver. |
| VSS | 36,44,55,65, 73,81,89,97, 107,115,123 | G | Ground for internal logic and output driver. |
| VDDV | 12,19,20,27 | P | 3.3V Power for analog video ADC. |
| VSSV | 15,16,23,24 | G | Ground for analog video ADC. |
| VDDVDA | 28,33 | P | 3.3V Power for analog video DAC. |
| VSSVDA | 30 | G | Ground for analog video DAC. |
| VDDA | 1,11 | P | 3.3V Power for analog audio. |
| VSSA | 3,4 | G | Ground for analog audio. |
| VDDAPLL | 34 | P | 3.3V Power for analog clock PLL. |
| VSSAPLL | 35 | G | Ground for analog clock PLL. |

Functional Description

Video Input Formats

The TW2866 has build-in automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Each standard can be included or excluded in the standard recognition process by software control. The exceptions are the base standard NTSC and PAL, which are always enabled. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

TW2866 supports all common video formats as shown in Table1.

Table1. Video Input Formats Supported by the TW2866

| Format | Lines | Fields | Fsc | Country |
|---------------------------|-------|--------|----------------------|--|
| NTSC-M | 525 | 60 | 3.579545 MHz | U.S., many others |
| NTSC-Japan ⁽¹⁾ | 525 | 60 | 3.579545 MHz | Japan |
| PAL-B, G, N | 625 | 50 | 4.433619 MHz | Many |
| PAL-D | 625 | 50 | 4.433619 MHz | China |
| PAL-H | 625 | 50 | 4.433619 MHz | Belgium |
| PAL-I | 625 | 50 | 4.433619 MHz | Great Britain, others |
| PAL-M | 525 | 60 | 3.575612 MHz | Brazil |
| PAL-CN | 625 | 50 | 3.582056 MHz | Argentina |
| SECAM | 625 | 50 | 4.406MHz 4.250MHz | France, Eastern Europe, Middle East, Russia |
| PAL-60 | 525 | 60 | 4.433619 MHz | China |
| NTSC (4.43) | 525 | 60 | 4.433619 MHz | Transcoding |

Notes: (1). NTSC-Japan has 0 IRE setup.

Analog Frontend

The TW2866 contains four 10-bit ADC (Analog to Digital Converters) to digitize the analog video inputs. The ADC can be put into power-down mode by the V_ADC_PWDN register. The TW2866 also contains an anti-aliasing filter to prevent out-of-band frequency in analog video input signal. So there is no need of external components in analog input pin except ac coupling capacitor and termination resistor. The following Fig1 shows the frequency response of the anti-aliasing filter.

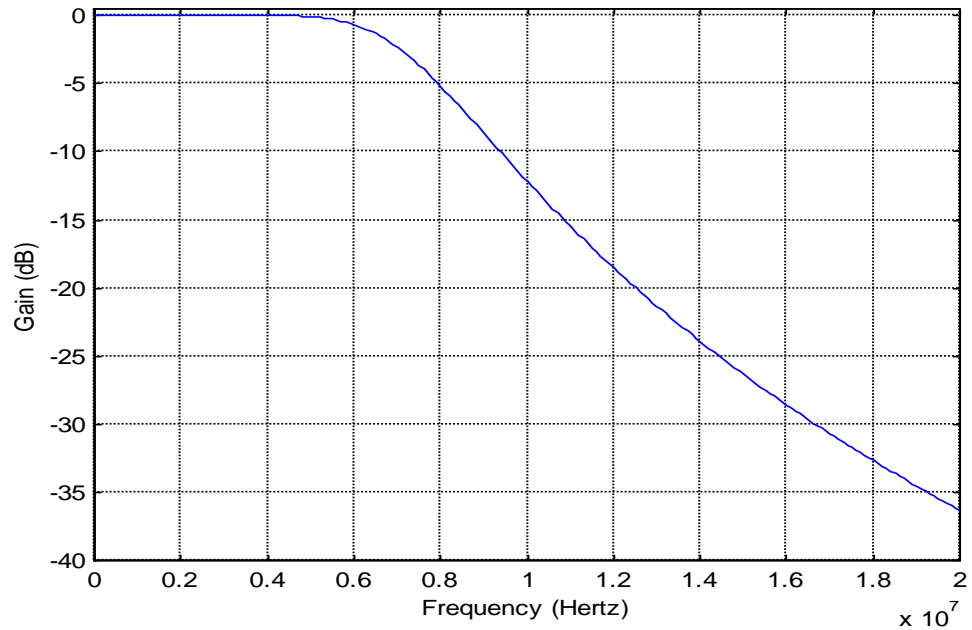


Fig1 The frequency response of anti-aliasing filter

Decimation Filter

The digitized composite video data are over-sampled to simplify the design of analog filter. The decimation filter is required to achieve optimum performance and prevent high frequency components from being aliased back into the video image when down-sampled. Fig2 shows the characteristic of the decimation filter.

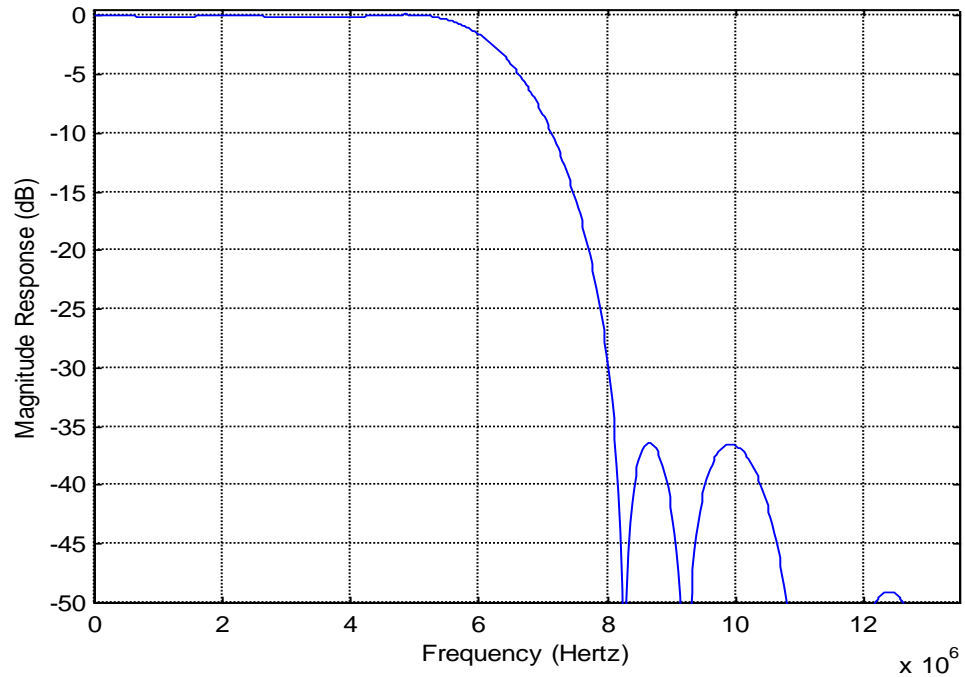


Fig2 The Characteristic of the Decimation Filter

Automatic Gain Control and Clamping

All four analog channels have built-in clamping circuit that restores the signal DC level. The Y channel restores the back porch of the digitized video to a level of 60. This operation is automatic through internal feedback loop. The Automatic Gain Control (AGC) of the Y channel adjusts input gain so that the sync tip is at a desired level. Programmable white peak protection logic is included to prevent saturation in the case of abnormal signal proportion between sync and white peak level.

Sync Processing

The sync processor of TW2866 detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-video or component signal. The processor contains a digital phase-locked-loop and decision logic to achieve reliable sync detection in stable signal as well as in unstable signals such as those from VCR fast forward or backward.

The vertical sync separator detects the vertical synchronization pattern in the input video signals. In addition, the actual sync determination is controlled by a detection window to provide more reliable synchronization. An option is available to provide faster responses for certain applications. The field status is determined at vertical synchronization time. The field logic can also be controlled to toggle automatically while tracking the input

Y/C Separation

The color-decoding block contains the luma/chroma separation for the composite video signal and multi-standard color demodulation. For NTSC and PAL standard signals, the luma/chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, adaptive notch/band-pass filter is used. The default selection for NTSC/PAL is comb filter.

In the case of comb filter, the TW2866 separates luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary 4H adaptive comb filter. The filter uses a four-line buffer. Adaptive logic combines the upper-comb and the lower-comb results based on the signal changes among the previous, current and next lines. This technique leads to excellent Y/C separation with small cross luma and cross color at both horizontal and vertical edges

Due to the line buffer used in the comb filter, there is always two lines processing delay at the output except for the component input mode which has only one line delay.

If notch/band-pass filter is selected, the characteristics of the filters are shown in the filter curve section.

The Fig3 show the frequency response of notch filter for each system NTSC and PAL. The Fig4 shows the frequency response of Chroma Band Pass Filter Curves.

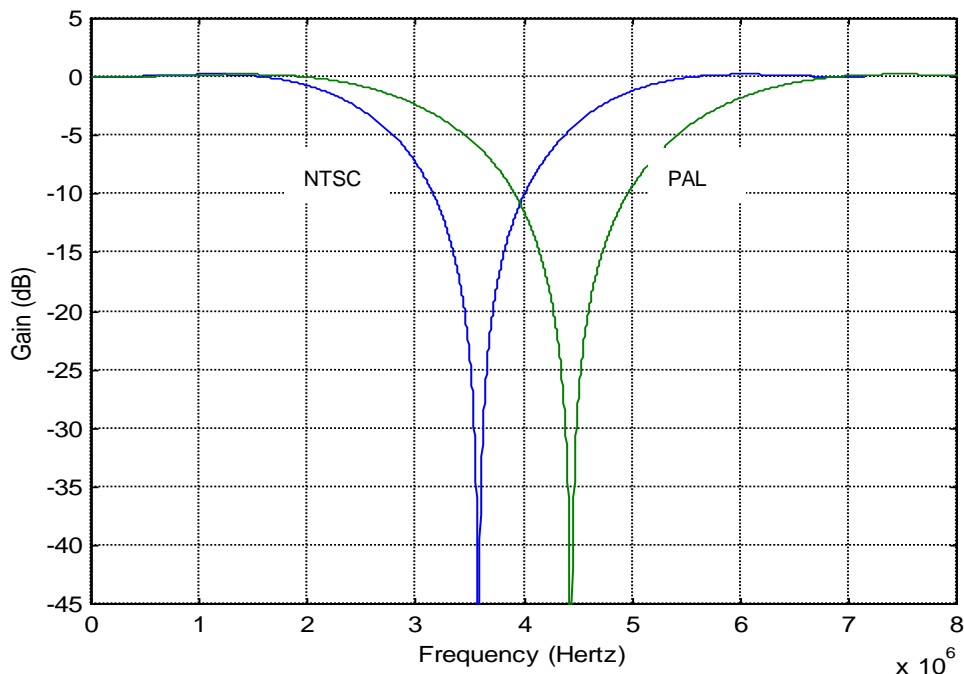


Fig3 The Characteristics of Luminance Notch Filter for PAL

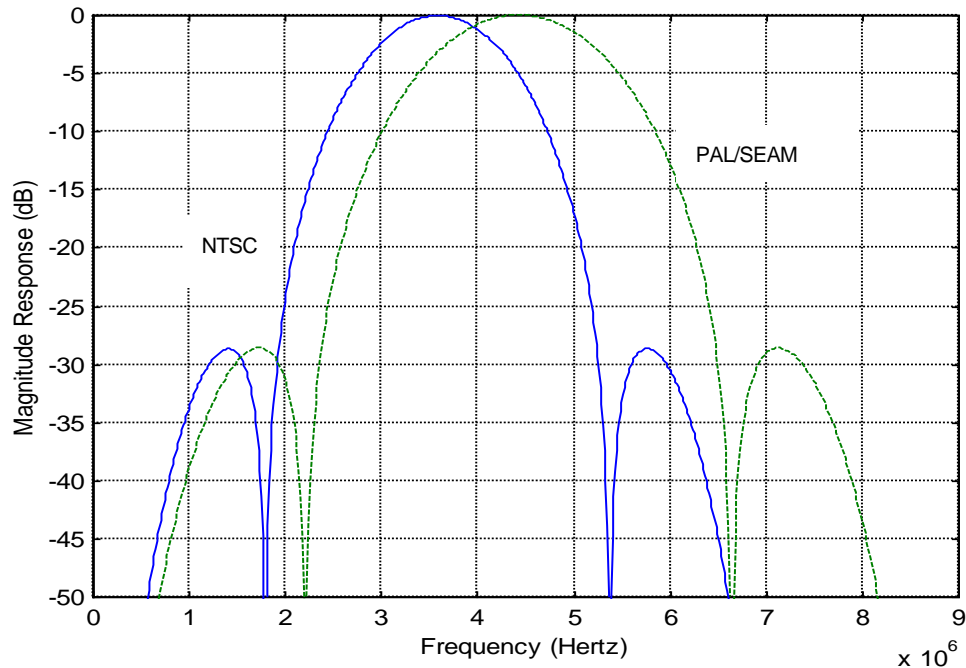


Fig4 Chroma Band Pass Filter Curves

Color Decoding

Chrominance Demodulation

The color demodulation for NTSC and PAL standard is done by first quadrature mixing the chroma signal to the base band. A low-pass filter is then used to remove carrier signal and yield chroma components. The low-pass filter characteristic can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

For SECAM, the color information is FM modulated onto different carrier. The demodulation process therefore consists of FM demodulator and de-emphasis filter. During the FM demodulation, the chroma carrier frequency is identified and used to control the SECAM color demodulation.

The sub-carrier signal for use in the color demodulator is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard of NTSC and PAL to be demodulated easily with single crystal frequency.

The Fig5 shows the frequency response of Chrominance Low-Pass Filter Curves.

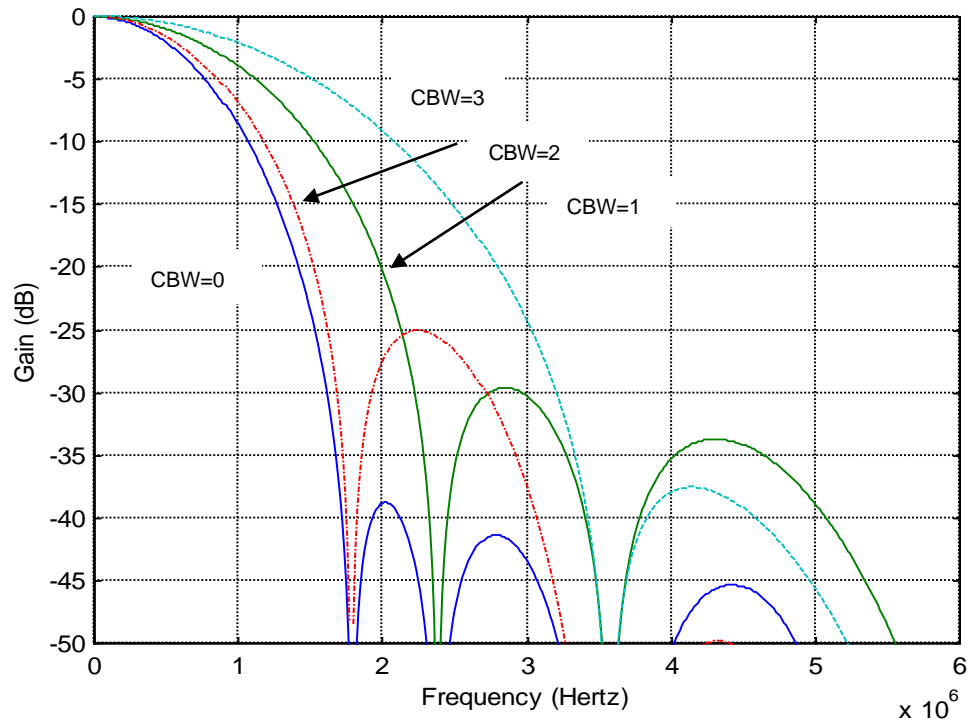


Fig5 Chrominance Low-Pass Filter Curves

ACC (Automatic Color gain control)

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. In the NTSC/PAL standard, the color reference signal is the burst on the back porch. It is measured to control the chroma output gain. The range of ACC control is -6db to $+24\text{db}$.

Chrominance Processing

Chrominance Gain, Offset and Hue Adjustment

When decoding NTSC signals, TW2866 can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift of NTSC decoding can be programmed through a control register. For the PAL standard, the PAL delay line is provided to compensate any hue error; therefore, there is no hue adjustment available. The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

CTI (Color Transient Improvement)

The TW2866 provides the Color Transient Improvement function to further enhance the image quality. The CTI enhance the color edge transient without any overshoot or under-shoot.

Luminance Processing

The TW2866 adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The TW2866 also provide programmable peaking function to further enhance the video sharpness. The peaking control has built-in coring function to prevent enhancement of noise.

The Fig6 shows the characteristics of the peaking filter for four different gain modes and different center frequencies.

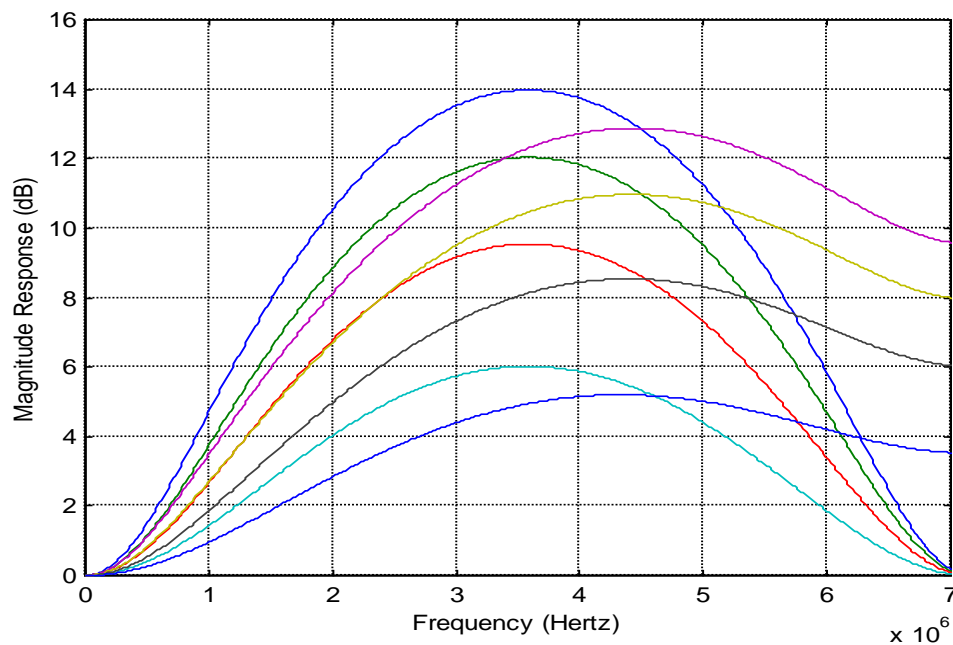


Fig6 The Characteristic of Luminance Peaking filter

Video Cropping

Cropping allows only subsection of a video image to be output. The active video region is determined by HDELAY, HACTIVE, VDELAY and VACTIVE register as illustrated in Fig7. The VACTIVE signal can be programmed to indicate the number of active lines to be displayed in a video field, and the HACTIVE signal can be programmed to indicate the number of active pixels to be displayed in a video line. The start of the field or frame in the vertical direction is indicated by the leading edge of VSYNC. The start of the line in the horizontal direction is indicated by the leading edge of the HSYNC. The start of the active lines from vertical sync edge is indicated by the VDELAY register. The start of the active pixels from the horizontal edge is indicated by the HDELAY register. The sizes and location of the active video are determined by HDELAY, HACTIVE, VDELAY, and VACTIVE registers. These registers are 8-bit wide, the lower 8-bits is, respectively, in HDELAY_LO, HACTIVE_LO, VDELAY_LO, and VACTIVE_LO. Their upper 2-bit shares the same register CROP_HI.

The Horizontal delay register (HDELAY) determines the number of pixels delay between the leading edge of HSYNC and the leading edge of the HACTIVE. Note that this value is referenced to the un-scaled pixel number. The Horizontal active register (HACTIVE) determines the number of active pixels to be output or scaled after the delay from the sync edge is met. This value is also referenced to the un-scaled pixel number. Therefore, if the scaling ratio is changed, the active video region used for scaling remain unchanged as set by the HACTIVE register, but the valid pixels output are equal or reduced due to down scaling. In order for the cropping to work properly, the following equation should be satisfied.

$$\text{HDELAY} + \text{HACTIVE} < \text{Total number of pixels per line.}$$

For NTSC output at 13.5 MHz pixel rate, the total number of pixels is 858. For PAL output at 13.5 MHz rate, the total number of pixels is 864. HACTIVE should be set to 720.

The Vertical delay register (VDELAY) determines the number of lines delay between the leading edge of the VSYNC and the start of the active video lines. It indicates number of lines to skip at the start of a frame before asserting the VACTIVE signal. This value is referenced to the incoming scan lines before the vertical scaling. The number of scan lines is 525 for the 60Hz systems and 625 for the 50Hz systems. The Vertical active register (VACTIVE) determines the number of lines to be used in the vertical scaling. Therefore, the number of scan lines output is equal or less than the value set in this register depending on the vertical scaling ratio. In order for the vertical cropping to work properly, the following equation should be observed.

$$\text{VDELAY} + \text{VACTIVE} < \text{Total number of lines per field}$$

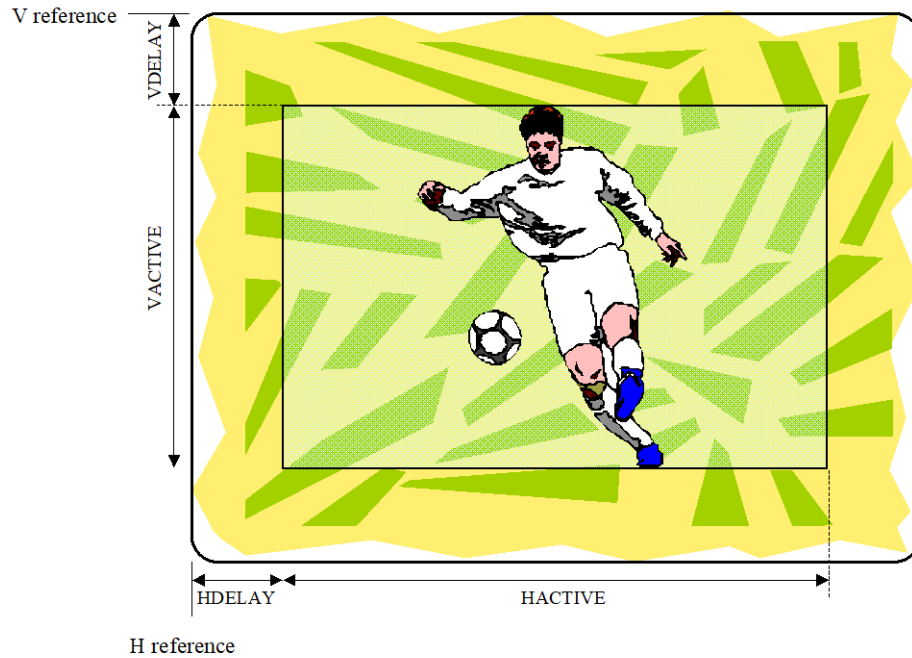


Fig7 The Effect of Cropping Registers

Video Scaler

The TW2866 can independently reduce the output video image size in both horizontal and vertical directions using arbitrary scaling ratios up to 1/16 in each direction. The horizontal scaling employs a dynamic 6-tap 32-phase interpolation filter for luma and a 2-tap 8-phase interpolation filter for chroma because of the limited bandwidth of the chroma data. The vertical scaling uses simple line dropping algorithm. Therefore, the use of non-integer vertical scaling ratio is not recommended.

Downscaling is achieved by programming the horizontal scaling ratio register (HSCALE) and vertical scaling ratio register (VSCALE). When outputting unscaled video, the TW2866 will output CCIR601 compatible 720 pixels per line or any number of pixels per line as specified by the HACTIVE register. The standard output for Square Pixel mode is 640 pixels for 60 Hz system and 768 pixels for 50 Hz systems. If the number of output pixels required is smaller than 720 in CCIR601 compatible mode or the number specified by the HACTIVE register, the 12-bit HSCALE register, which is the concatenation of two 8-bit registers SCALE_HI and HSCALE_LO, is used to reduce the output pixels to the desired number.

Following is an example using pixel ratio to determine the horizontal scaling ratio. These equations should be used to determine the scaling ratio to be written into the 12-bit HSCALE register assuming HACTIVE is programmed with 720 active pixels per line:

$$\text{NTSC:} \quad \text{HSCALE} = \lceil 720 / N_{\text{pixel_desired}} \rceil * 256$$

$$\text{PAL: HSCALE} = [(720/N_{\text{pixel_desired}})] * 256$$

Where: $N_{\text{pixel_desired}}$ is the nominal number of pixel per line.

For example, to output a CCIR601 compatible NTSC stream at SIF resolution, the HSCALE value can be found as:

$$\text{HSCALE} = [(720/320)] * 256 = 576 = 0x0240$$

However, to output a SQ compatible NTSC stream at SIF resolution, the HSCALE value should be found as:

$$\text{HSCALE} = [(640/320)] * 256 = 512 = 0x200$$

In this case, with total resolution of 768 per line, the HACTIVE should have a value of 640.

The vertical scaling determines the number of vertical lines output by the TW2866. The vertical scaling register (VSCALE) is a 12-bit register, which is the concatenation of a 4-bit register SCALE_HI and an 8-bit register VSCALE_LO. The maximum scaling ratio is 16:1. Following equations should be used to determine the scaling ratio to be written into the 12-bit VSCALE register assuming VACTIVE is programmed with 240 or 288 active lines per field.

$$60\text{Hz system: VSCALE} = [240/ N_{\text{line_desired}}] * 256$$

$$50\text{Hz system: VSCALE} = [288/ N_{\text{line_desired}}] * 256$$

Where: $N_{\text{line_desired}}$ is the number of active lines output per field.

The scaling ratios for some popular formats are listed in Table2. Fig8 shows Horizontal Scaler Pre-Filter Curves.

Table2. HSCALE and VSCALE value for some popular video formats.

| Scaling Ratio | Format | Total Resolution | Output Resolution | HSCALE values | VSCALE (frame) |
|---------------|--------------|------------------|-------------------|---------------|----------------|
| 1:1 | NTSC SQ | 780x525 | 640x480 | 0x0100 | 0x0100 |
| | NTSC CCIR601 | 858x525 | 720x480 | 0x0100 | 0x0100 |
| | PAL SQ | 944x625 | 768x576 | 0x0100 | 0x0100 |
| | PAL CCIR601 | 864x625 | 720x576 | 0x0100 | 0x0100 |
| 2:1 (CIF) | NTSC SQ | 390x262 | 320x240 | 0x0200 | 0x0200 |
| | NTSC CCIR601 | 429x262 | 360x240 | 0x0200 | 0x0200 |
| | PAL SQ | 472x312 | 384x288 | 0x0200 | 0x0200 |
| | PAL CCIR601 | 432x312 | 360x288 | 0x0200 | 0x0200 |
| 4:1 (QCIF) | NTSC SQ | 195x131 | 160x120 | 0x0400 | 0x0400 |
| | NTSC CCIR601 | 214x131 | 180x120 | 0x0400 | 0x0400 |
| | PAL SQ | 236x156 | 192x144 | 0x0400 | 0x0400 |
| | PAL CCIR601 | 216x156 | 180x144 | 0x0400 | 0x0400 |

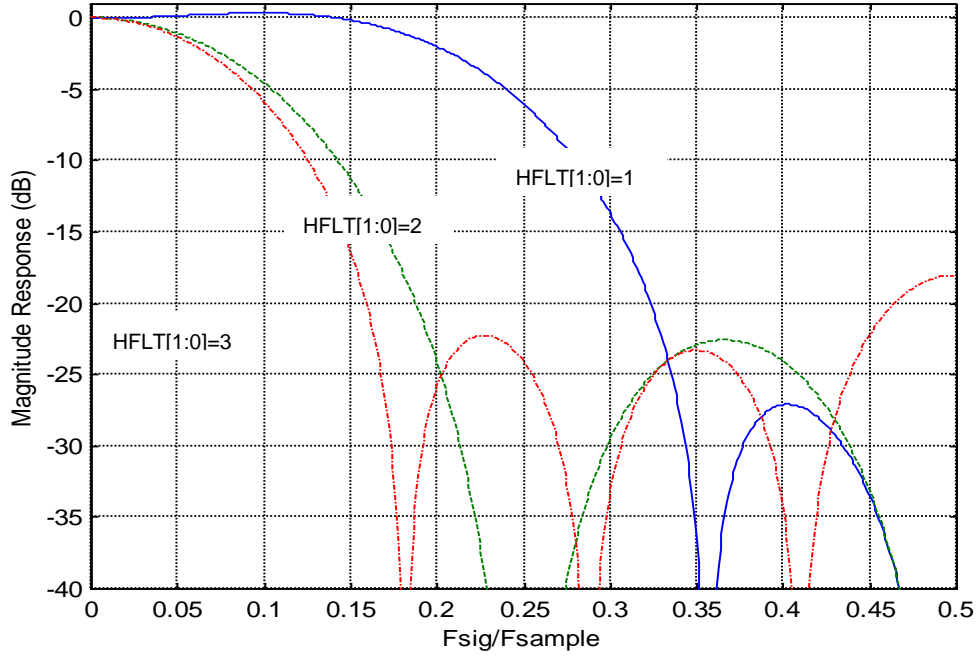


Fig8 Horizontal Scaler Pre-Filter Curves

Output Format

The TW2866 supports a standard ITU-R BT.656 format. All video data and timing signal of four channels are synchronous with the pins CLKPO_n or CLKNO_n output. Therefore, CLKPO_n or CLKNO_n can be connected to four channel interfaces for synchronizing data. And, the phase of CLKPO_n or CLKNO_n can be controlled by delay unit via the CLKPO_n_DEL or CLKNO_n_DEL registers and polarity inverse cell via the CLKPO_n_POL or CLKNO_n_POL registers independently.

ITU-R BT.656 Format

In ITU-R BT.656 format, SAV and EAV sequences are inserted into the data stream to indicate the active video time. It is noted that the number of active pixels per line is constant in this mode regardless of the actual incoming line length. The output timing is illustrated in Fig9. The SAV and EAV sequences are shown in Table3. An optional set of 656 SAV/EAV code sequence can be enabled to identify no-video status using the NOVID_656 bit.

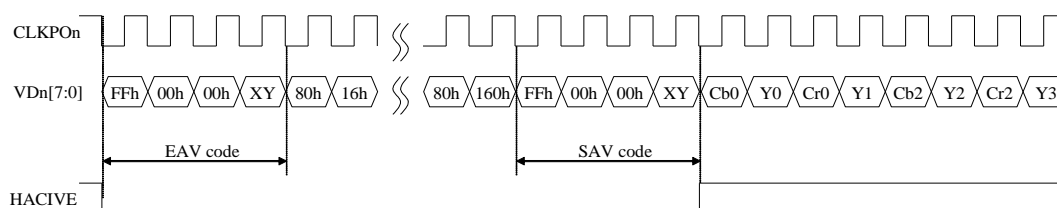


Fig9 Timing Diagram of ITU-R BT.656 format

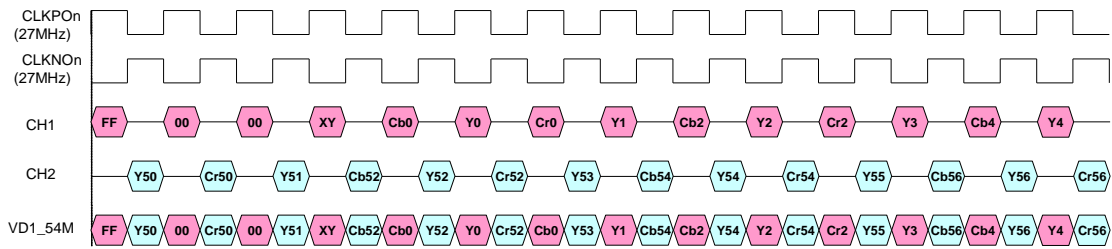
Table3 ITU-R BT.656 SAV and EAV Code Sequence

| Condition | | | 656 FVH Value | | | SAV/EAV Code Sequence | | | | |
|-----------|--------|--------|---------------|---|---|-----------------------|--------|-------|--------|---------|
| Field | V time | H time | F | V | H | First | Second | Third | Fourth | |
| | | | | | | | | | Normal | Option* |
| EVEN | Blank | EAV | 1 | 1 | 1 | 0xFF | 0x00 | 0x00 | 0xF1 | 0x71 |
| EVEN | Blank | SAV | 1 | 1 | 0 | 0xFF | 0x00 | 0x00 | 0xEC | 0x6C |
| EVEN | Active | EAV | 1 | 0 | 1 | 0xFF | 0x00 | 0x00 | 0xDA | 0x5A |
| EVEN | Active | SAV | 1 | 0 | 0 | 0xFF | 0x00 | 0x00 | 0xC7 | 0x47 |
| ODD | Blank | EAV | 0 | 1 | 1 | 0xFF | 0x00 | 0x00 | 0xB6 | 0x36 |
| ODD | Blank | SAV | 0 | 1 | 0 | 0xFF | 0x00 | 0x00 | 0xAB | 0x2B |
| ODD | Active | EAV | 0 | 0 | 1 | 0xFF | 0x00 | 0x00 | 0x9D | 0x1D |
| ODD | Active | SAV | 0 | 0 | 0 | 0xFF | 0x00 | 0x00 | 0x80 | 0x00 |

Note : * Option includes video loss information in ITU-R BT.656

Two Channel ITU-R BT.656 Time-multiplexed Format with 54MHz

The TW2866 supports two channels ITU-R BT.656 time-multiplexed format with 54MHz that is useful to security application requiring two channel outputs through one channel video port. The CHMDn register enables the dual ITU-R BT.656 time-multiplexed format and the MAINCHn/SELCHn register selects channel output to be multiplexed with its own channel on each VD pins. To de-multiplex the time-multiplexed data in the back end chip, the channel ID can be inserted in the data stream using the CHID_MD register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. The following Fig10-1 illustrates the logical timing diagram in the case of CH1 and CH2 time-multiplexed output through CH1 video output port. Fig10-2/10-3 illustrate VDn[7:0]/CLKPOn/CLKNOn pin default timing with 54MHz/27MHz clock output mode.



g10-1 Timing Diagram of Two Channel Time-multiplexed Format

Fi

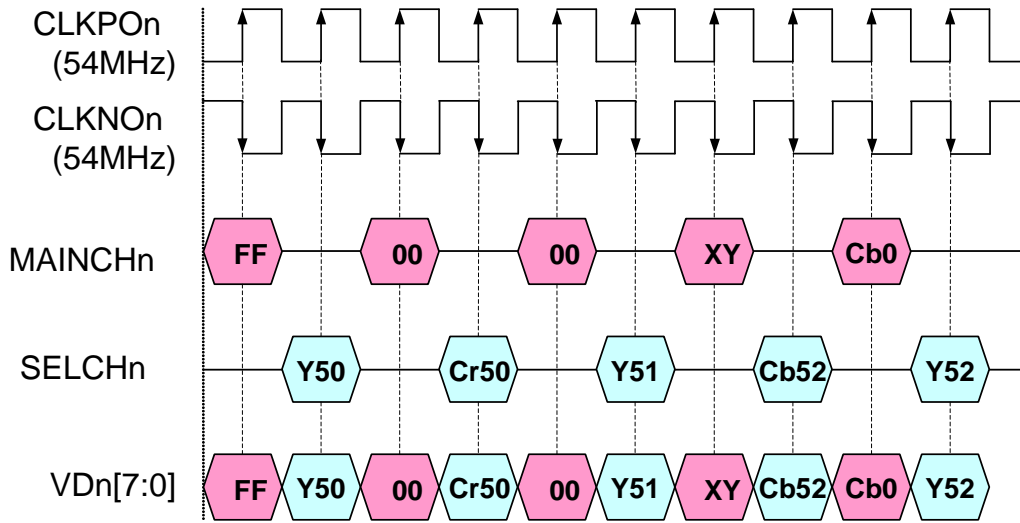


Fig10-2 Pin output timing of Two Channel Time-multiplexed Format with 54MHz clock.

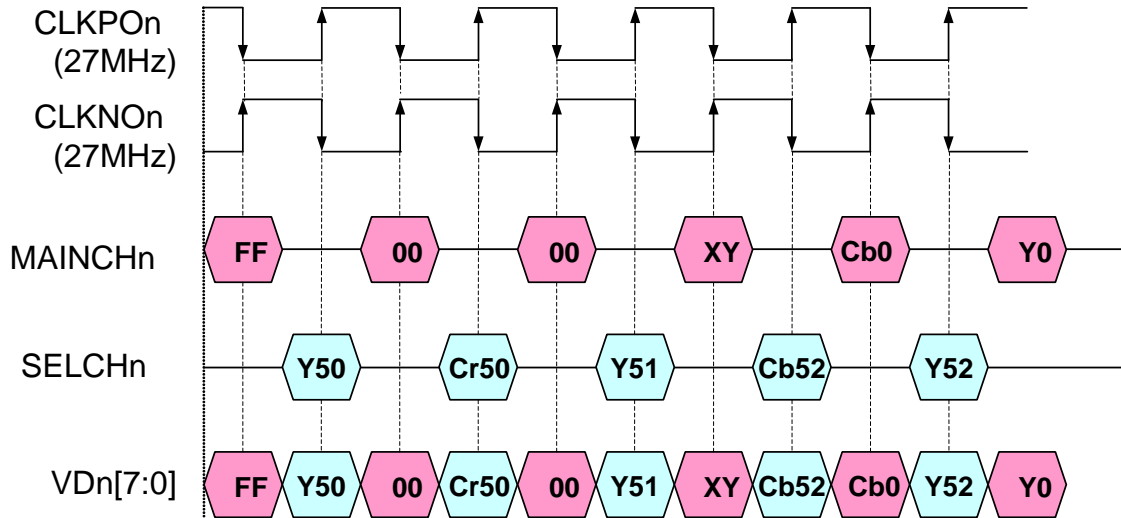
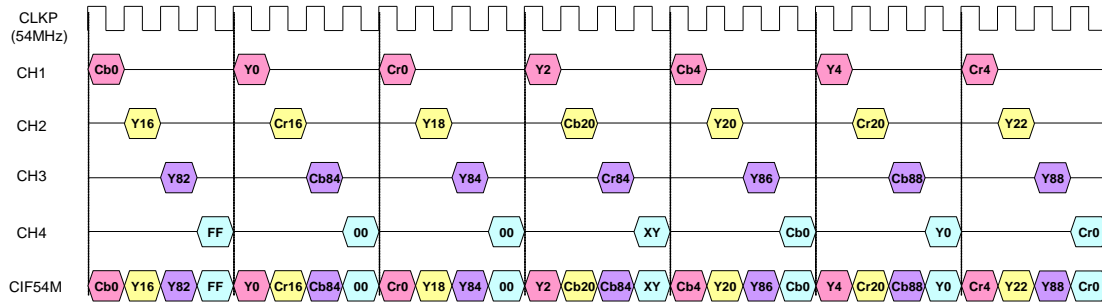


Fig10-3 Pin output timing of Two Channel Time-multiplexed Format with 27MHz clock.

Four Channel CIF Time-multiplexed Format with 54MHz

Four channel CIF (360x480) time-multiplexed format is also provided for specific security application using the CIF_54M register. For this format, each channel ITU-R BT.656 data stream is down-sampled into 13.5MHz ITU-R BT.656 data stream except the sync code. Optionally, the vertical scaling can also be enabled to support Quad (360x240) format using the VSCL_ENA register. Then, these four 13.5MHz ITU-R BT.656 data stream are time-multiplexed into 54MHz data stream. This format requires only one channel video port to transfer whole four channel CIF data independently. When CIF_54M register is set to 1, TW2866 can support one channel video port to transfer whole four channel CIF data independently and the other video port to transfer two channel Full D1 ITU-R BT.656 time-multiplexed format simultaneously. To de-multiplex the time-multiplexed data in the back end chip, the channel ID can be inserted in the data stream using the CHID_MD register. Two kinds of channel ID format can be supported. One is horizontal blanking code with channel ID and the other is ITU-R BT.656 sync code with channel ID. Optionally, when the vertical scaling is enabled, the ITU-R BT.656 sync code will be skipped in the invalid line through the VSCL_SYNC register. The following Fig11-1/11-2 and Table4 illustrate the timing diagram and detailed channel ID format for four channel CIF time-multiplexed format with 54MHz.



Fi

g11-1 Logical Timing Diagram of 4 Ch CIF Time-multiplexed Format

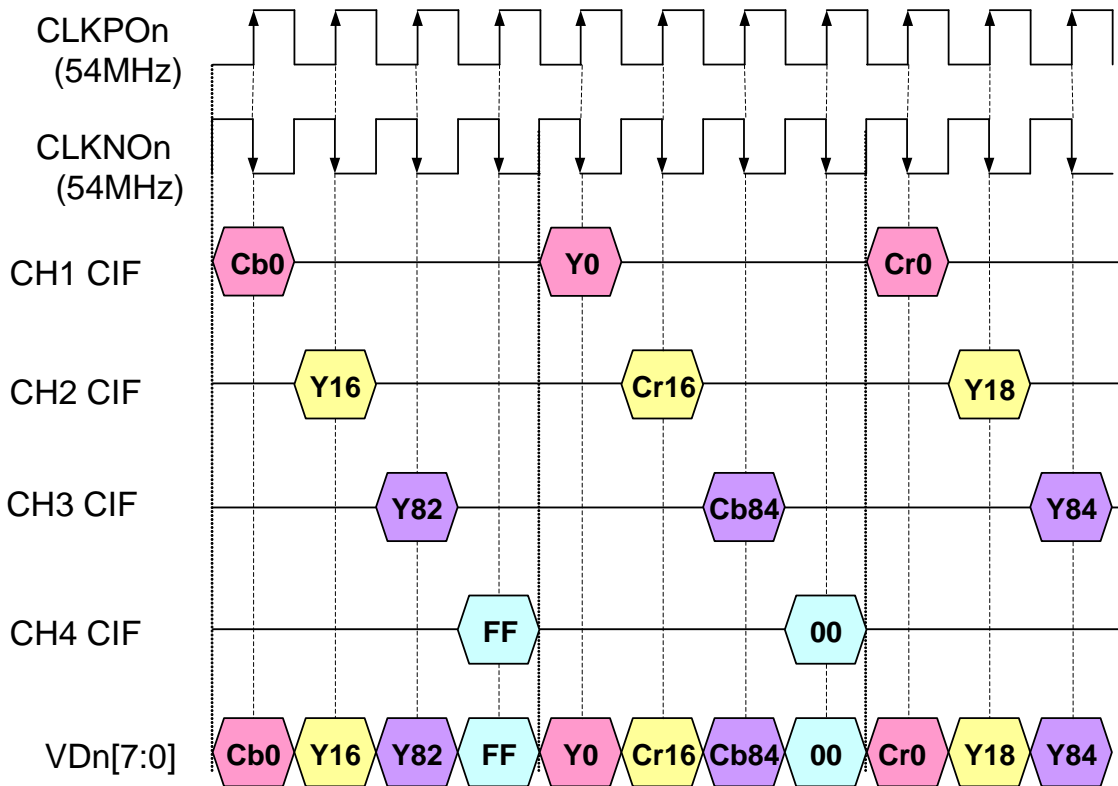


Fig11-2 Pin output timing of 4 Ch CIF Time-multiplexed Format with 54MHz clock

Table4 The Channel ID Format for 4 Ch CIF Time-multiplexed Format with 54MHz

| Condition | | | 656 FVH Value | | | SAV/EAV Code Sequence | | | | | | |
|-----------|--------|-------|---------------|---|---|-----------------------|--------|-------|--------|------|------|------|
| Field | Vtime | Htime | F | V | H | First | Second | Third | Fourth | | | |
| | | | | | | | | | Ch1 | Ch2 | Ch3 | Ch4 |
| EVEN | Blank | EAV | 1 | 1 | 1 | 0xFF | 0x00 | 0x00 | 0xF0 | 0xF1 | 0xF2 | 0xF3 |
| EVEN | Blank | SAV | 1 | 1 | 0 | 0xFF | 0x00 | 0x00 | 0xE0 | 0xE1 | 0xE2 | 0xE3 |
| EVEN | Active | EAV | 1 | 0 | 1 | 0xFF | 0x00 | 0x00 | 0xD0 | 0xD1 | 0xD2 | 0xD3 |
| EVEN | Active | SAV | 1 | 0 | 0 | 0xFF | 0x00 | 0x00 | 0xC0 | 0xC1 | 0xC2 | 0xC3 |
| ODD | Blank | EAV | 0 | 1 | 1 | 0xFF | 0x00 | 0x00 | 0xB0 | 0xB1 | 0xB2 | 0xB3 |
| ODD | Blank | SAV | 0 | 1 | 0 | 0xFF | 0x00 | 0x00 | 0xA0 | 0xA1 | 0xA2 | 0xA3 |
| ODD | Active | EAV | 0 | 0 | 1 | 0xFF | 0x00 | 0x00 | 0x90 | 0x91 | 0x92 | 0x93 |
| ODD | Active | SAV | 0 | 0 | 0 | 0xFF | 0x00 | 0x00 | 0x80 | 0x81 | 0x82 | 0x83 |

(a) ITU-R BT.656 Sync Code with Channel ID

| Channel | H Blanking Code with Channel ID | | |
|---------|---------------------------------|-------|-------|
| | Y | Cb | Cr |
| Ch1 | 8'h10 | 8'h80 | 8'h80 |
| Ch2 | 8'h11 | 8'h81 | 8'h81 |
| Ch3 | 8'h12 | 8'h82 | 8'h82 |
| Ch4 | 8'h13 | 8'h83 | 8'h83 |

(b) Horizontal Blanking Code with Channel ID

Four Channel D1 Time-division-multiplexed Format with 108MHz

Four channel of D1 (720x480) at 27MHz video stream that are time-division-multiplexed at 108MHz data rate format is implemented in TW2866 for security surveillance application. In order to reduce pin counts (thus shrink chip size) on both decoder's digital output port and the input port of the back end compression Codec devices, TW2866 implements single 8 bit bus at 4 times the base band pixel clock rate of 27MHz. While quadrupling the data rate on a single bus to meet the new requirement, individually, each channel data arrangement still retains the base band 27MHz ITU-R BT.656 specification. For interface that can accept the new 108MHz clock bus, only one single clock at 108MHz is required. Embedded timing (SAV-EAV) code and Channel ID are inserted into each channel for de-multiplexing and separation of channel data.

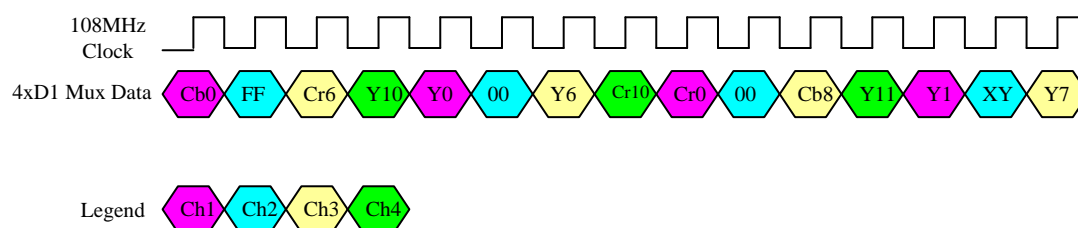


Fig12 -1 Timing Diagram of 108MHz 4 Ch D1 Time-Division-Multiplexed Video data

Fig12-1 depicts the temporal arrangement of the video data in 108MHz data rate. Each channel is byte level time-division multiplexed (TDM). Main clock is 108MHz clock

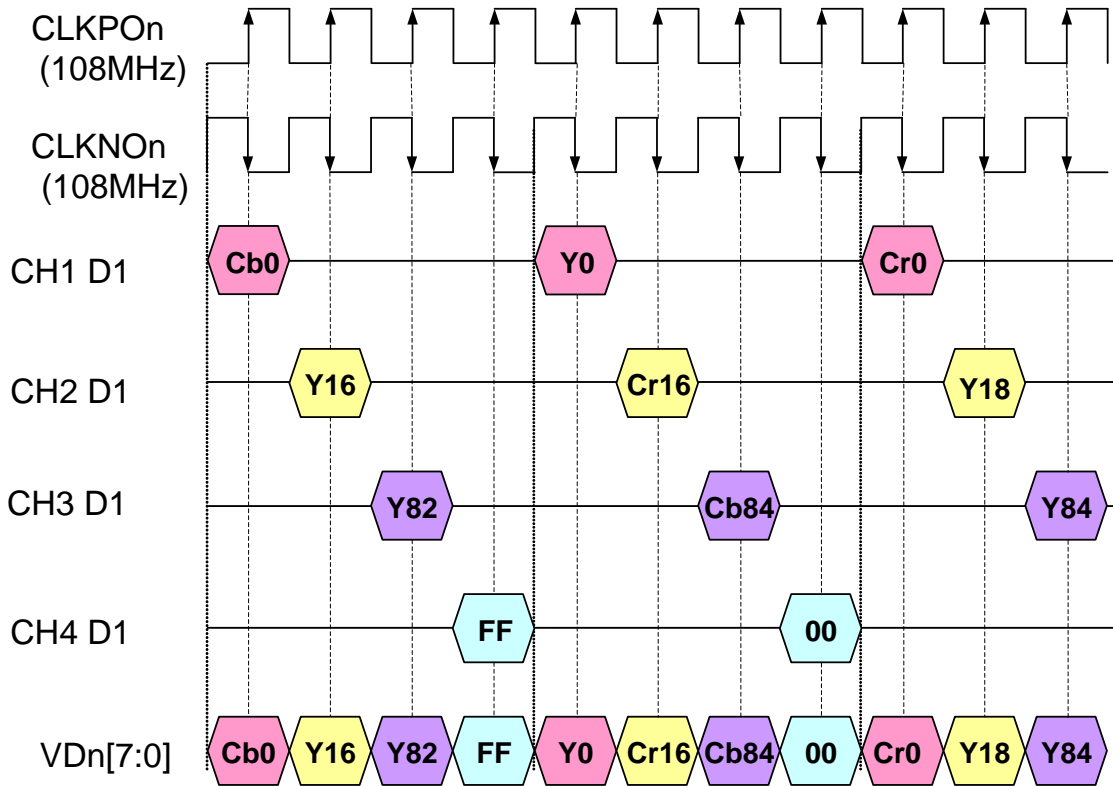


Fig12-2 Pin output Timing of 108MHz 4 Ch D1 Time-Division-Multiplexed Video data with 108MHz clock.

Table5. Shows the Special format of ITU-R BT. 656 Embedded timing code and Channel ID code

| Condition | | | 656 FVH Value | | | SAV-EAV Code | | | | | | |
|-----------|--------|--------|---------------|---|---|--------------|--------|-------|--------|------|------|------|
| Field | V-time | H-time | F | V | H | First | Second | Third | Fourth | | | |
| | | | | | | | | | Ch1 | Ch2 | Ch3 | Ch4 |
| EVEN | BLANK | EAV | 1 | 1 | 1 | 0xFF | 0x00 | 0x00 | 0xF0 | 0xF1 | 0xF2 | 0xF3 |
| EVEN | BLANK | SAV | 1 | 1 | 0 | 0xFF | 0x00 | 0x00 | 0xE0 | 0xE1 | 0xE2 | 0xE3 |
| EVEN | ACTIVE | EAV | 1 | 0 | 1 | 0xFF | 0x00 | 0x00 | 0xD0 | 0xD1 | 0xD2 | 0xD3 |
| EVEN | ACTIVE | SAV | 1 | 0 | 0 | 0xFF | 0x00 | 0x00 | 0xC0 | 0xC1 | 0xC2 | 0xC3 |
| ODD | BLANK | EAV | 0 | 1 | 1 | 0xFF | 0x00 | 0x00 | 0xB0 | 0xB1 | 0xB2 | 0xB3 |
| ODD | BLANK | SAV | 0 | 1 | 0 | 0xFF | 0x00 | 0x00 | 0xA0 | 0xA1 | 0xA2 | 0xA3 |
| ODD | ACTIVE | EAV | 0 | 0 | 1 | 0xFF | 0x00 | 0x00 | 0x90 | 0x91 | 0x92 | 0x93 |
| ODD | ACTIVE | SAV | 0 | 0 | 0 | 0xFF | 0x00 | 0x00 | 0x80 | 0x81 | 0x82 | 0x83 |

Output Enabling Act

After power-up, the TW2866 registers have unknown values. The RSTB pin must be asserted and released to bring all registers to its default values. After reset, the TW2866 data outputs are tri-stated. The OE register should be written after reset to enable outputs desired.

Video Output Channel Selection

If CHMDn[1:0] in Reg0xCA is set to 0hex, MAINCHn[1:0] in Reg0xCD selects one number of Video Channels to be output on VDn[7:0] pin as Single Channel ITU-R BT.656(D1) Format output. If CHMDn[1:0] in Reg0xCA is set to 1hex, MAINCHn[1:0] in Reg0xCD and SELCHn[1:0] in Reg0xCC select two numbers of Video Channels to be output on VDn[7:0] pin as Two Channel ITU-R BT.656(D1) Time-multiplexed Format output. If CHMDn[1:0] in Reg0xCA is set to 2hex, Four Channel ITU-R BT.656(D1) Time-multiplexed Format is output on VDn[7:0] pin.

Extra Sync Output

The additional timing information such as syncs and field flag are also supported through the MPP pins. The video output timing is illustrated in Fig13 and Fig14 TW2866 HS/VS/FLD output function is compatible to TW9907 Video decoder HSYNC/VS/FLD output function. Start of VS timing is controlled by VSHT register(V timing) and OVSDLY register(H timing). End of VS timing is controlled by OVSEND register(V Timing). Start of FLD timing is controlled by OFDLY register(V timing). Start of HS timing is controlled by HSBEGIN register and End of HS timing is controlled by HSEND register.

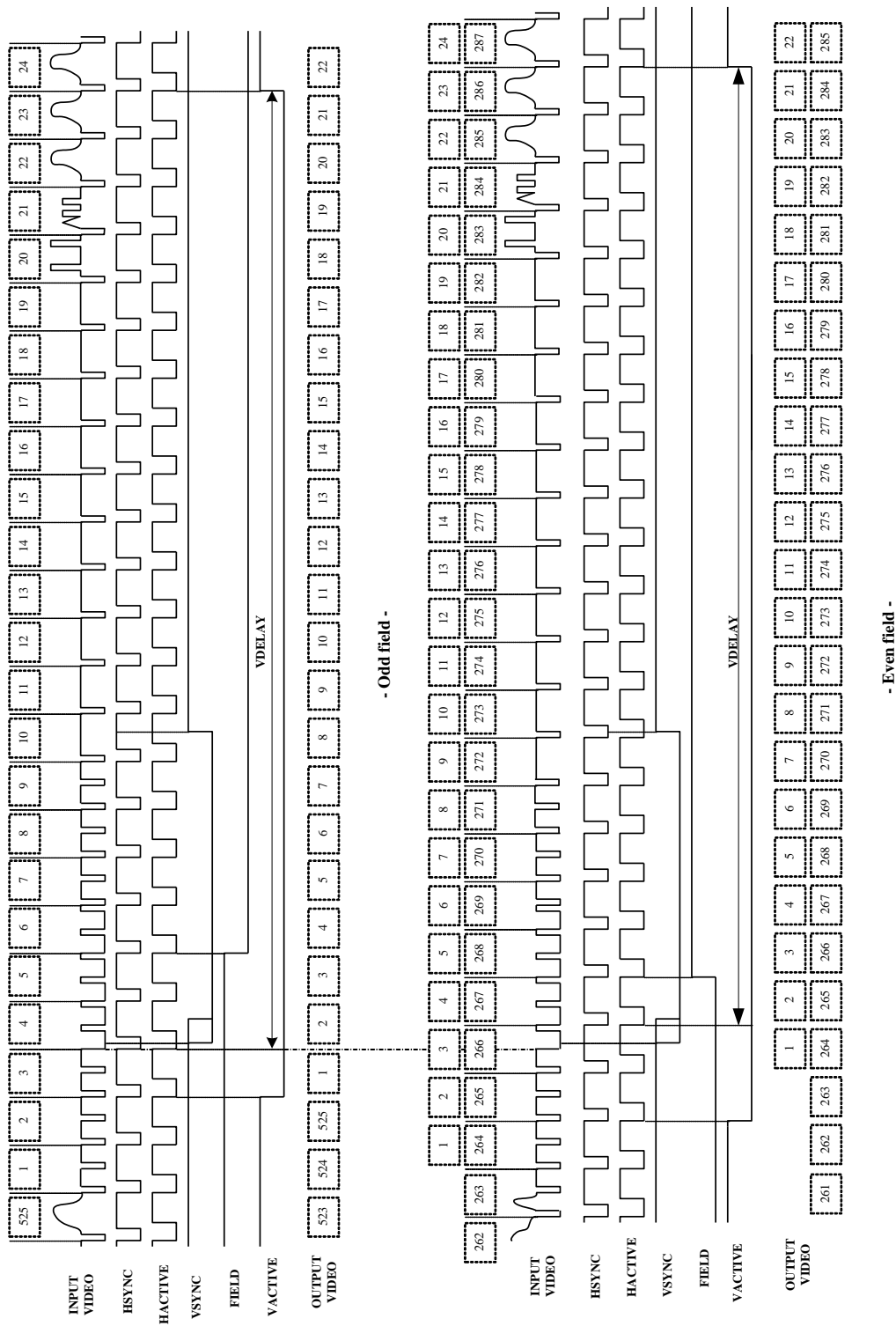


Fig13 Vertical timing diagram for 60Hz/525 line system

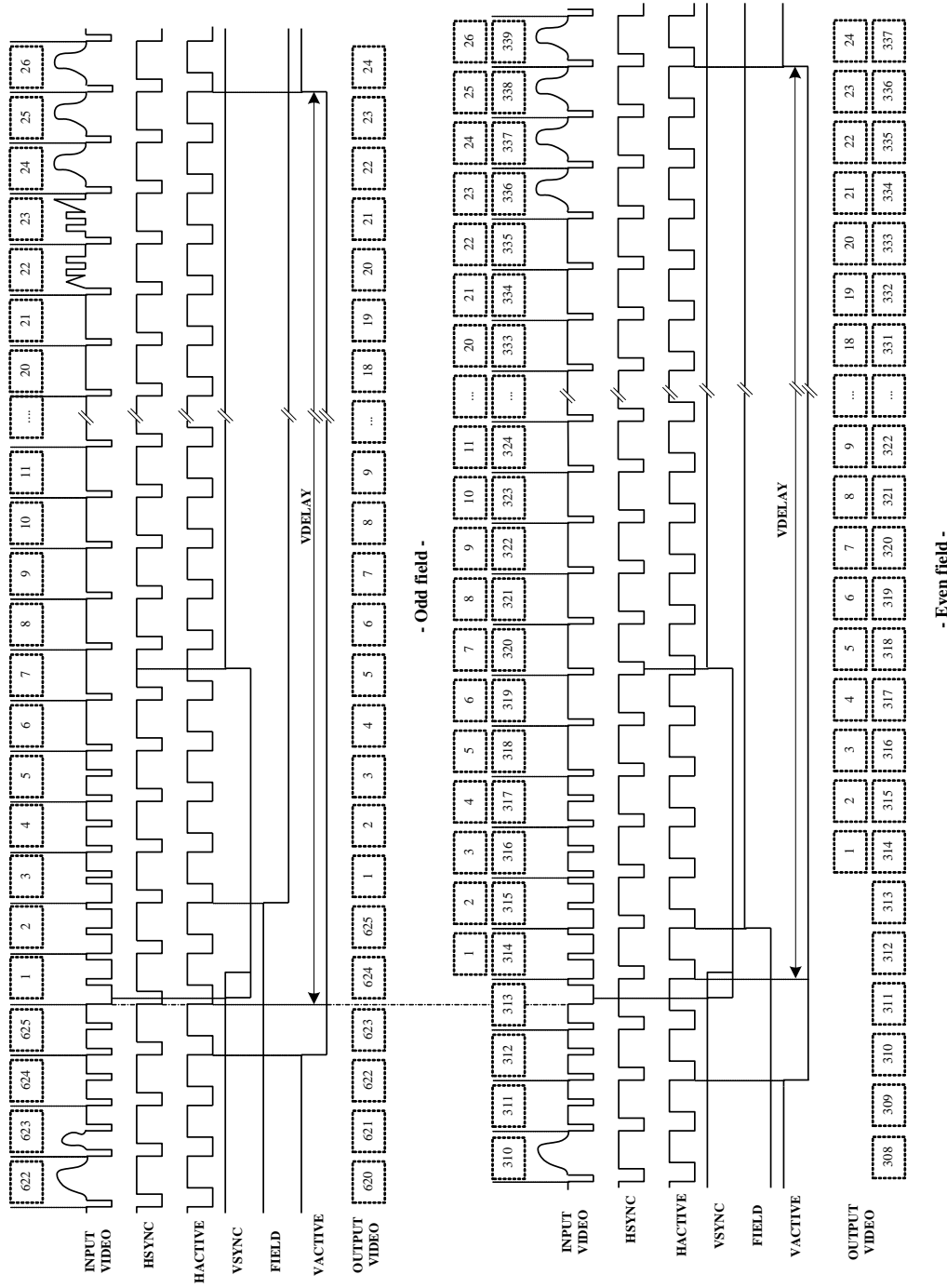


Fig14 Vertical timing diagram for 50Hz/625 line system

Video Encoder

The TW2866 has built-in NTSC/PAL video encoder to support the analog video output. It converts the standard digital ITU-R BT.656 data stream into analog composite or Y/C video output through two 10 bit video DACs. The digital video data is first gain adjusted according the format selected. The luminance signal is band-limited to 6MHz before interpolated to 27MHz sampling rate. The chrominance is also band-limited to selected bandwidth before modulated with the internal generated sub-carrier and interpolated to 27MHz sampling rate. These signals are finally combined with sync information before sending out to DAC. The encoder can operate in either master or slave clock mode. In the master mode, the clock comes from the internal generated 27MHz clock. The NTSC output can be selected to include a 7.5 IRE pedestal. The luminance, chrominance, sync and burst amplitude can be adjusted independently. It also has built-in color bar pattern generator for video adjustment. The block diagram is shown in following figure.

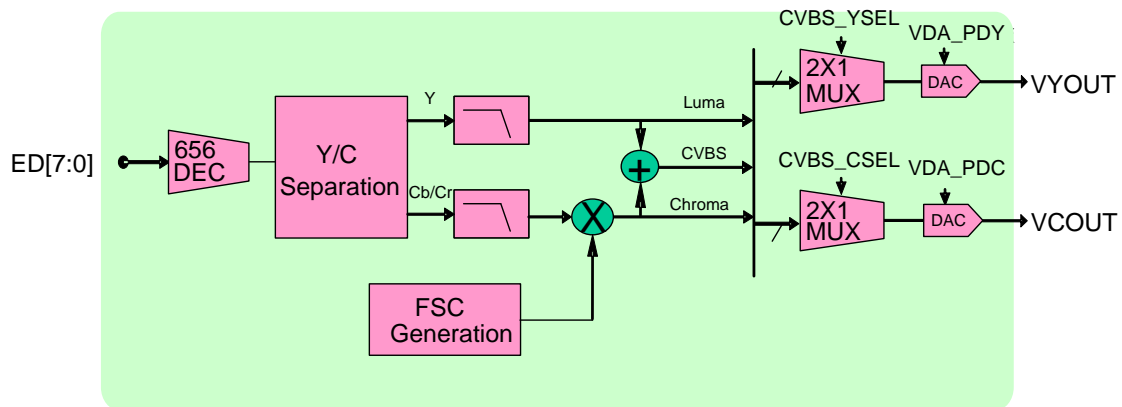


Fig15 Encoder block diagram

Output Standard Selection

The TW2866 supports various video standard outputs via the HZ50 and FSCSEL, PHALT, PED registers as described in the following Table 6.

Table 6 Analog output video standards

| Format | Specification | | | Register | | | |
|-----------|---------------|----------|------------|----------|--------|-------|-----|
| | Line/Fv (Hz) | Fh (KHz) | Fsc (MHz) | HZ50 | FSCSEL | PHALT | PED |
| NTSC-M | 525/59.94 | 15.734 | 3.579545 | 0 | 0 | 0 | 1 |
| NTSC-J | | | | | | | 0 |
| NTSC-4.43 | 525/59.94 | 15.734 | 4.43361875 | 0 | 1 | 0 | 1 |
| NTSC-N | 625/50 | 15.625 | 3.579545 | 1 | 0 | 0 | 0 |
| PAL-BDGI | 625/50 | 15.625 | 4.43361875 | 1 | 1 | 1 | 0 |
| PAL-N | | | | | | | 1 |
| PAL-M | 525/59.94 | 15.734 | 3.57561149 | 0 | 2 | 1 | 0 |
| PAL-NC | 625/50 | 15.625 | 3.58205625 | 1 | 3 | 1 | 0 |
| PAL-60 | 525/59.94 | 15.734 | 4.43361875 | 0 | 1 | 1 | 0 |

If the PHALT register is set to “1”, phase alternation can be reset every 8 field so that phase alternation keeps same phase every 8 field.

Chrominance Filter

The bandwidth of chrominance signal can be selected via the CBW register as shown in the following Fig16.

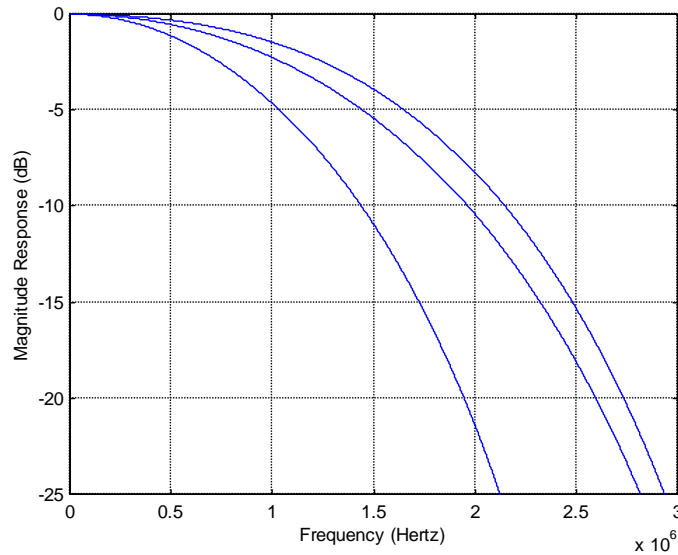


Fig16 Characteristics of chrominance Filter

Digital-to-Analog Converter

The digital video data from video encoder is converted to analog video signal by DAC (Digital to Analog Converter). The analog video signal format can be selected for each DAC independently via the CVBS_YSEL and CVBS_CSEL register. Each DAC can be disabled independently to save power by the VDA_PDY and VDA_PDC register. The full scale current can be controlled by the external RSET resistor.

A simple reconstruction filter is required externally to reject noise as shown in the Fig17.

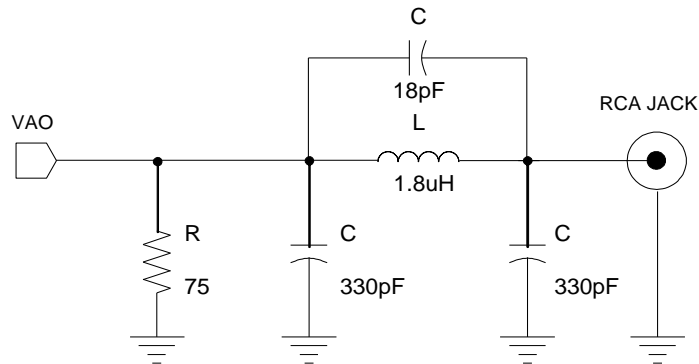


Fig17 Example of reconstruction filter

Audio Codec

The audio codec in the TW2866 is composed of five audio Analog-to-Digital converters, one Digital-to-Analog converter, audio mixer, digital serial audio interface and audio detector shown as the Fig18. The TW2866 can accept 5 analog audio signals and 1 digital serial audio data and produce 1 mixing analog audio signal and 2 digital serial audio data.

The level of analog audio input signal AIN1 ~ AIN5 can be adjusted respectively by internal programmable gain amplifiers that are defined via the AIGAIN1,AIGAIN2,AIGAIN3,AIGAIN4 and AIGAIN5 registers and then sampled by each Analog-to-Digital converters. The digital serial audio input data through the ACLKP, ASYNP and ADATP pin are used for playback function. To record audio data, the TW2866 provides the digital serial audio output via the ACLKR, ASYNR and ADATR pin.

The TW2866 can mix all of audio inputs including analog audio signal and digital audio data according to the predefined mixing ratio for each audio via the MIX_RATIO1 ~ MIX_RATIO5 and MIX_RATIOP registers. This mixing audio output can be provided through the analog and digital interfaces. The embedded audio Digital-to-Analog converter supports the analog mixing audio output whose level can be controlled by programmable gain amplifier via the AOGAIN register. The ADATM pin supports the digital mixing audio output and its digital serial audio timings are provided through the ACLKR and ASYNR pins that are shared with the digital serial audio record timing pins.

The main purpose of AIN5 is to make the standard I2S/DSP digital audio output on ADATM pin for special application.Usually,4 AIN1/AIN2/AIN3/AIN4 audio data are only used on ADATR pin output.

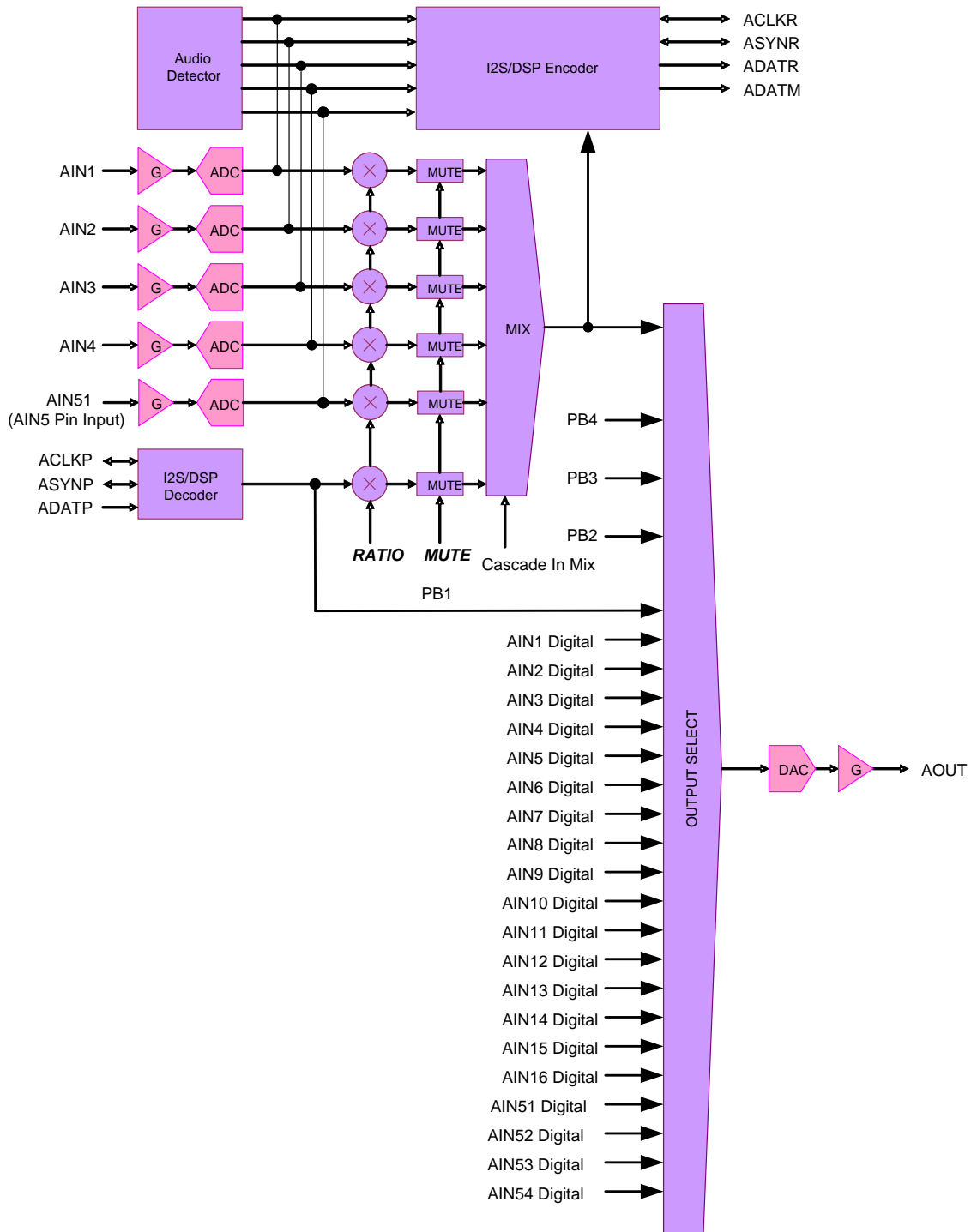


Fig18 Block Diagram of Audio Codec

Audio Clock Master/Slave mode

The TW2866 has two types of Audio Clock modes. If **ACLKRM** register is set to 1, fs audio sample date is processed from audio clock internal **ACKG** (Audio Clock Generator) generates. In this master mode, **ACLKR/ASYNR** pins are output mode. **ASYNROEN** register for **ASYNR** pin

should be set to 0(output enable mode).If ACLKRMAS^{TER} register is set to 0,fs audio sample rate is processed from audio clock on ACLKR pin input.256xfs,320xfs or 384xfs audio clock should be connected to ACLKR pin from external master clock source in this slave mode. ASYNR pin can be input or output by external Audio clock master in slave mode. ASYNR signal should change per fs audio sample rate in both master and slave mode.AIN5MD and AFS384 register set up Audio fs mode by following table.

| Register | | fs mode |
|----------|--------|---------|
| AIN5MD | AFS384 | |
| 0 | 0 | 256xfs |
| 1 | 0 | 320xfs |
| 0 | 1 | 384xfs |

Audio Detection

The TW2866 has an audio detector for individual 5 channels. There are 2 kinds of audio detection method defined by the ADET_MTH. One is the detection of absolute amplitude and the other is of differential amplitude. For both detection methods, the accumulating period is defined by the ADET_FILT register and the detecting threshold value is defined by the ADET_TH1 ~ ADET_TH5 registers. The status for audio detection is read by the STATE_AVDET register and it also makes the interrupt request through the IRQ pin with the combination of the status for video loss detection.

Multi-Chip Operation

TW2866 can output 16 channel audio data on ACLKR/ASYNR/ADATR output simultaneously. Therefore, up to 4 chips should be connected on most Multi-Chip application cases. SMD register selects Audio cascade serial interface mode. If SMD register is set to 2, ALINKI pin is audio cascade serial input and ALINKO pin is audio cascade serial output mode.

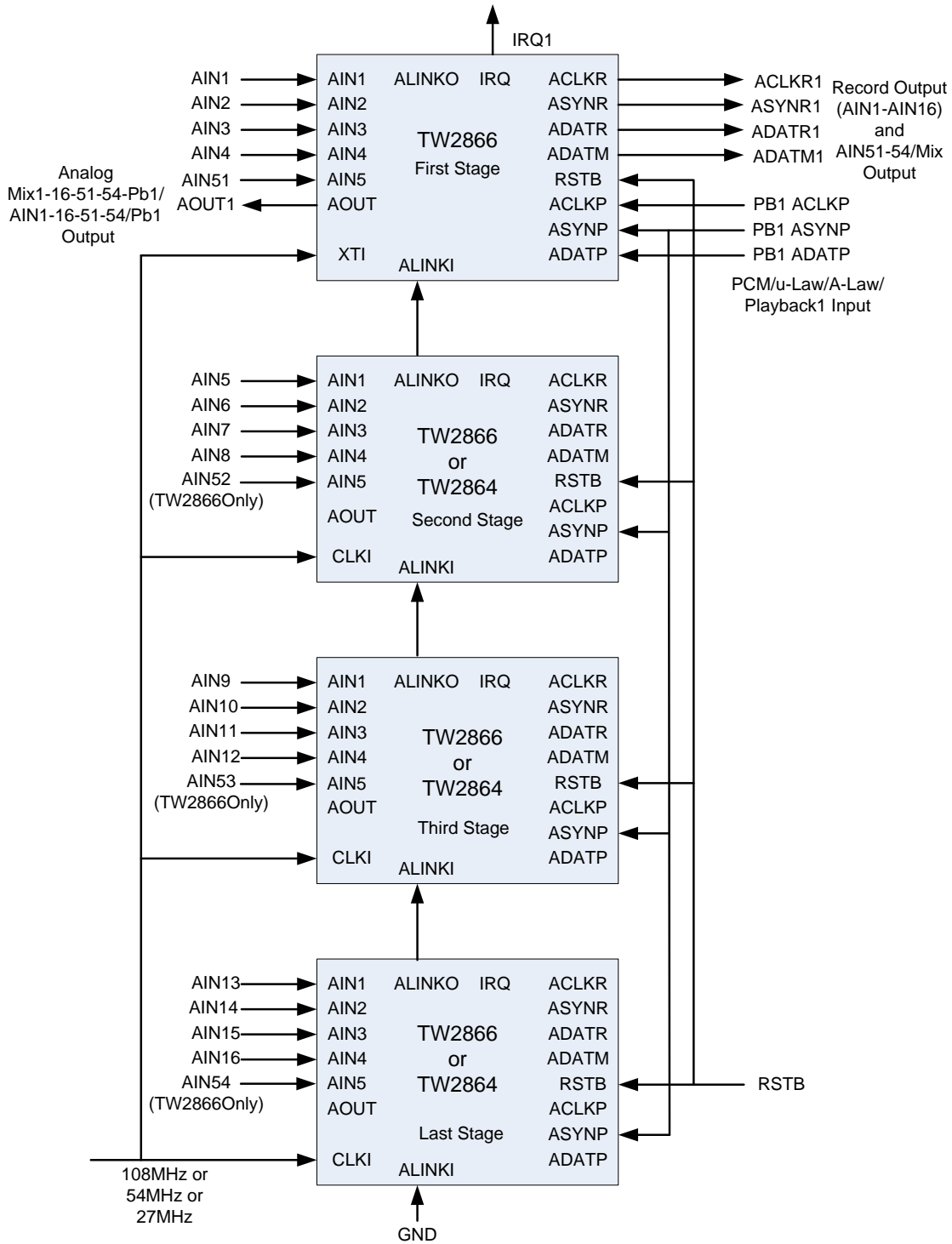
Each stage chip can accept 5 analog audio signals so that four cascaded chips will be 16-channel audio controller as default AIN5MD=0. The first stage chip provides 16ch digital serial audio data for record. Even though the first stage chip has only 1 digital serial audio data pin ADATR for record, the TW2866 can generate 16 channel data simultaneously using multi-channel method. Also, each stage chip can support 4 channel record outputs that are corresponding with analog audio inputs. This first stage chip can also output 16 channel mixing audio data by the digital serial audio data and analog audio signal. The first stage chip accepts the digital serial audio data for playback. The digital playback data can be converted to analog signal by Digital-to-Analog Converter in the first stage chip.

In Multi-Chip Audio operation mode, one same Oscillator clock source (108MHz or 54MHz) need to be connected to all TW2866 XTI or TW2864 CLKI pins or TW2865 pins. One 27MHz clock source can be connected if needed, too.

Several Master/Slave mode configurations are available. Fig19-1 is the most recommended and demanded system with Clock Master mode (ACLKRMAS_{TER}=1). Fig19-2 is the most recommended system with Clock Slave Sync Slave mode (ACLKRMAS_{TER}=0, ASYNROEN=1). Another system combinations are also available if application need different type specific system. Fig19-1 and Fig19-2 show most typical system.

In following each Fig, Mix1-16-51-54/Pb1 means Mix output of AIN1-16, AIN51-54 and Playback1. AIN1-16-51-54/Pb1 means one selected Audio output in AIN1-16-51-54/Pb1.

If one TW2866 uses AIN5MD=1, all other cascaded TW2866 chips must set up AIN5MD=1 together. Generally, 4 Audio input mode (AIN5MD=0) are most used in this cascade system.



F19-1 Recommended Clock Master cascade mode system
 All chips have SMD=2; ACLKRMAS=1; SYNROEN=0; PB_MASTER=0

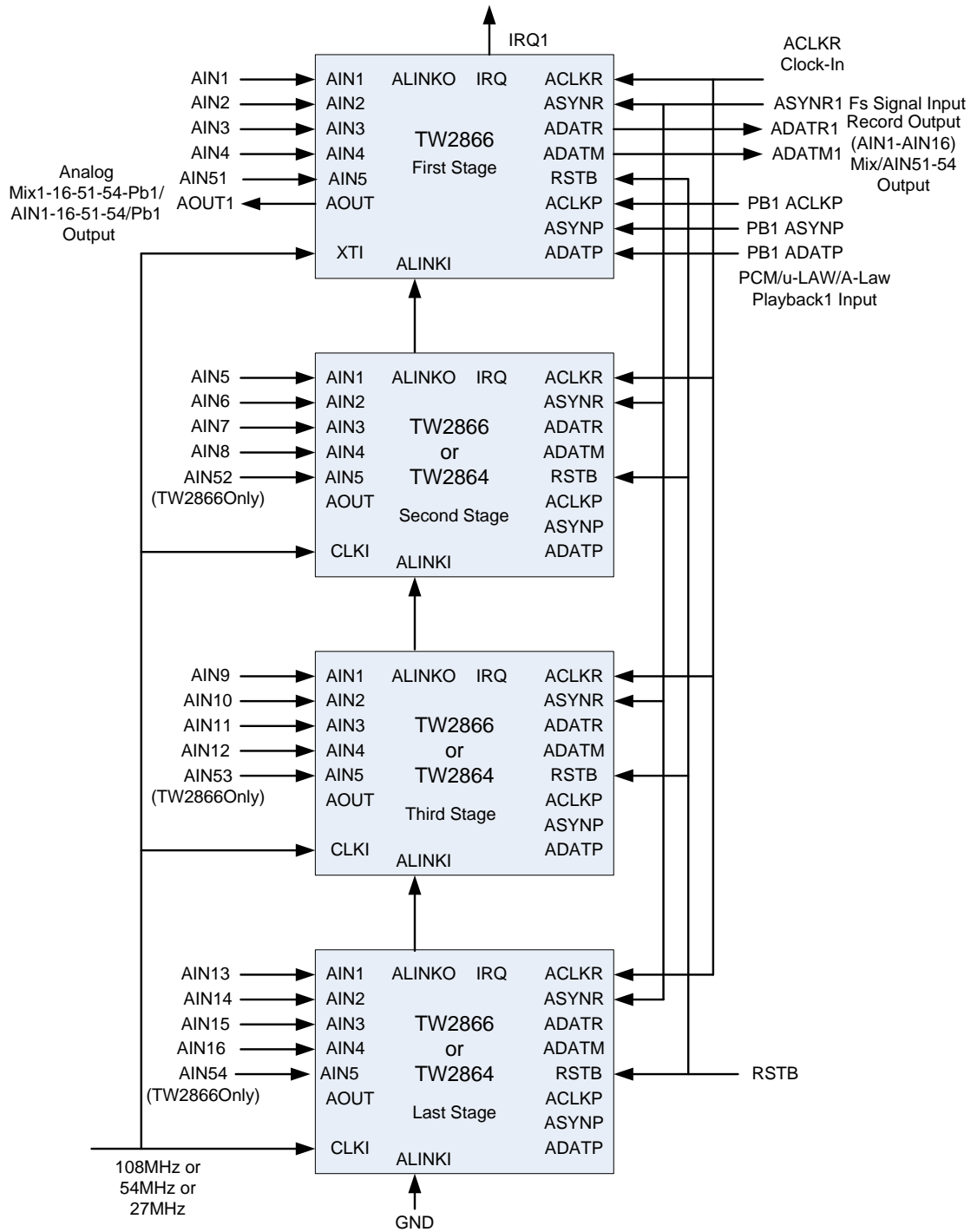


Fig19-2 Recommended Clock Slave Sync Slave cascade mode system
 All chips have SMD = 2;ACLKRMASER=0;ASYNROEN=1;PB_MASTER=0

Serial Audio Interface

There are 3 kinds of digital serial audio interfaces in the TW2866, the first is a recording output, the second is a mixing output and the third is a playback input. These 3 digital serial audio interfaces follow a standard I2S or DSP interface as shown in the Fig20

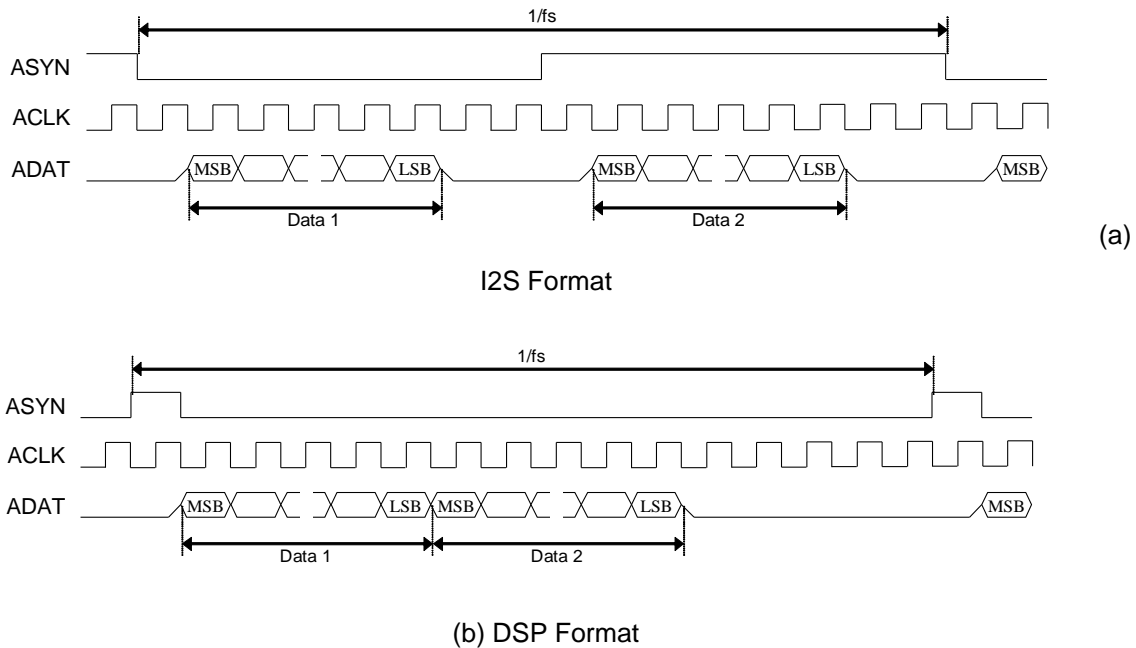


Fig20 Timing Chart of Serial Audio Interface

Playback Input

The serial interface using the ACLKP, ASYNP and ADATP pins accepts the digital serial audio data for the playback purpose. The ACLKP and ASYNP pins can be operated as master or slave mode. For master mode, these pins work as output pin and generate the standard audio clock and synchronizing signal. For slave mode, these pins are input mode and accept the standard audio clock and synchronizing signal. The ADATP pin is always input mode regardless of operating mode. One of audio data in left or right channel should be selected for playback audio by the PB_LRSEL.

Record Output

To record audio data, the TW2866 provides the digital serial audio data through the ACLKR, ASYNR and ADATR pins. Sampling frequency comes from 256xfs, 320xfs or 384xfs audio system clock setting. Even though the standard I2S and DSP format can have only 2 audio data on left and right channel, the TW2866 can provide an extended I2S and DSP format which can have 16 channel audio data through ADATR pin. The R_MULTCH defines the number of audio data to be recorded by the ADATR pin. ASYNR signal is always fs frequency rate. One ASYNR period is always equal to 256xACLKR clock length with AIN5MD=0. The Fig21 shows the digital serial audio data organization for multi-channel audio.

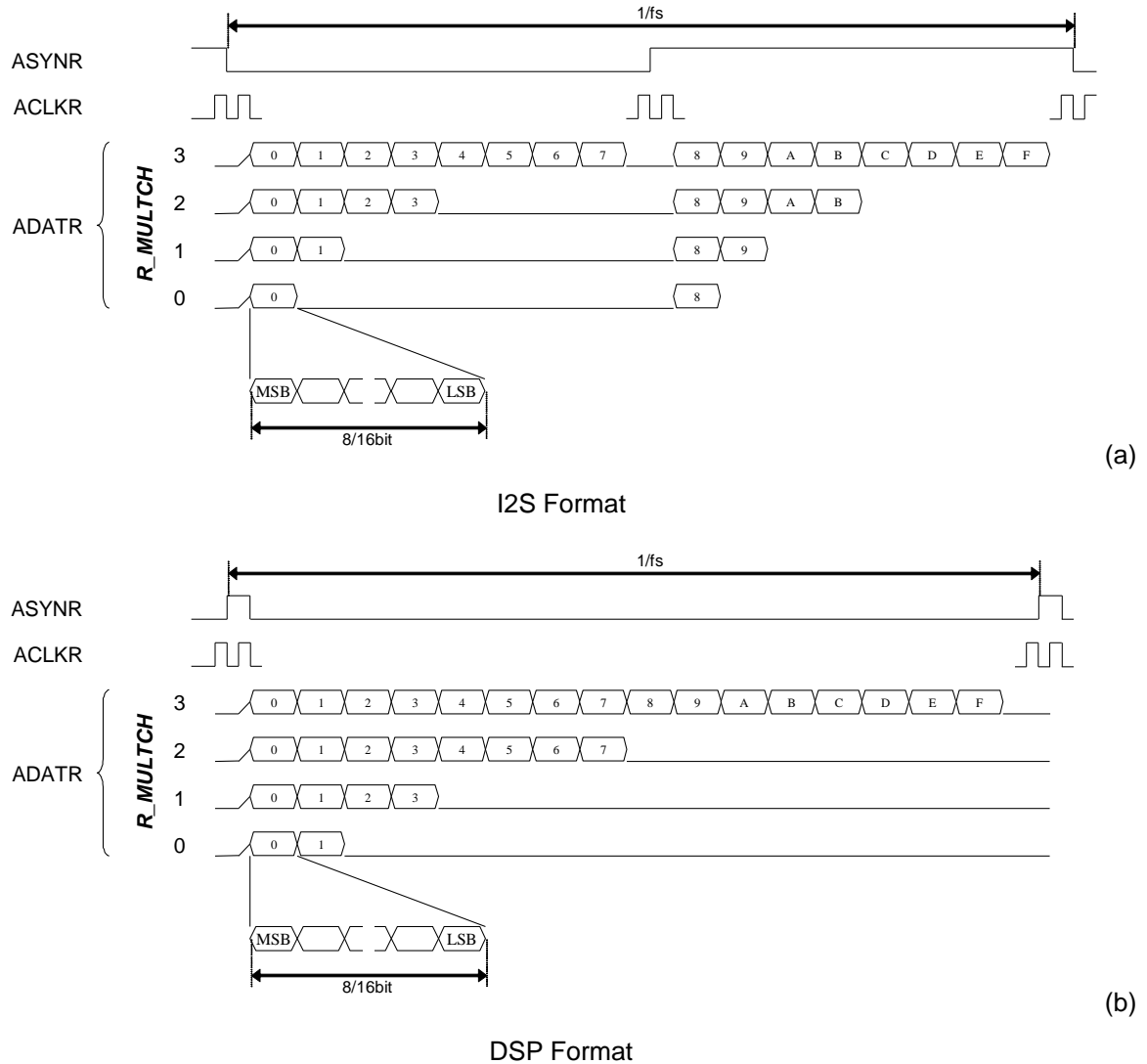


Fig21 Timing Chart of Multi-channel Audio Record

The following Table5 shows the sequence of audio data to be recorded for each mode of the R_MULTCH register. The sequences of 0 ~ F do not mean actual audio channel number but represent sequence only. The actual audio channel should be assigned to sequence 0 ~ F by the

R_SEQ_0 ~ R_SEQ_F register. When the ADATM pin is used for record via the R_ADATM register, the audio sequence of ADATM is showed also in Table7.

Table7 Sequence of Multi-channel Audio Record
(a) I2S Format

| R_MULTCH | Pin | Left Channel | | | | | | | | Right Channel | | | | | | | |
|----------|-------|--------------|---|---|---|---|---|---|---|---------------|---|---|---|---|---|---|---|
| 0 | ADATR | 0 | | | | | | | | 8 | | | | | | | |
| | ADATM | F | | | | | | | | 7 | | | | | | | |
| 1 | ADATR | 0 | 1 | | | | | | | 8 | 9 | | | | | | |
| | ADATM | F | E | | | | | | | 7 | 6 | | | | | | |
| 2 | ADATR | 0 | 1 | 2 | 3 | | | | | 8 | 9 | A | B | | | | |
| | ADATM | F | E | D | C | | | | | 7 | 6 | 5 | 4 | | | | |
| 3 | ADATR | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| | ADATM | F | E | D | C | B | A | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

(b) DSP Format

| R_MULTCH | Pin | Left/Right Channel | | | | | | | | | | | | | | | |
|----------|-------|--------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | ADATR | 0 | 1 | | | | | | | | | | | | | | |
| | ADATM | F | E | | | | | | | | | | | | | | |
| 1 | ADATR | 0 | 1 | 2 | 3 | | | | | | | | | | | | |
| | ADATM | F | E | D | C | | | | | | | | | | | | |
| 2 | ADATR | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | | | | | | | | |
| | ADATM | F | E | D | C | B | A | 9 | 8 | | | | | | | | |
| 3 | ADATR | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| | ADATM | F | E | D | C | B | A | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Mix Output

The digital serial audio data on the ADATM pin has 2 different audio data which are mixing audio and playback audio. The mixing digital serial audio data is the same as analog mixing output. The sampling frequency, bit width and number of audio for the ADATM pin are same as the ADATR pin because the ACLKR and ASYNR pins are shared with the ADATR and ADATM pins.

Audio Clock Slave Mode Data Output Timing

TW2866 always output ASYNR/ADATR/ADATM by ACLKR falling edge triggered timing.

ADATR/ADATM output data are always changing at next ACLKR falling edge triggered timing after ASYNR signal changes. If ASYNR is output, ADATR/ADATM output are always fixed to one ACLKR falling edge timing. But if ASYNR is input, ADATR/ADATM output timing changes by ASYNR input timing.

ASYNR is ACLKR falling edge triggered input/output

If ASYNR is input and ASYNR input is ACLKR falling edge triggered input as ASYNR input signal is changing after ACLKR falling edge, or if ASYNR is output, TW2866 output ADATR/ADATM by ACLKR falling edge triggered timing as shown on following figures. ASYNR signal is changing during $ACLKR = 0$. TW2866 output ADATR/ADATM data after next ACLKR falling edge triggered timing with more than half ACLKR clock delay.

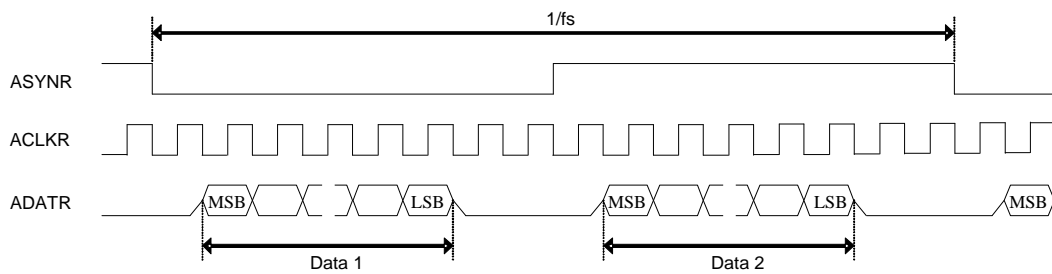


Fig22-1 ACLKMASTER=0, RM_SYNC=0

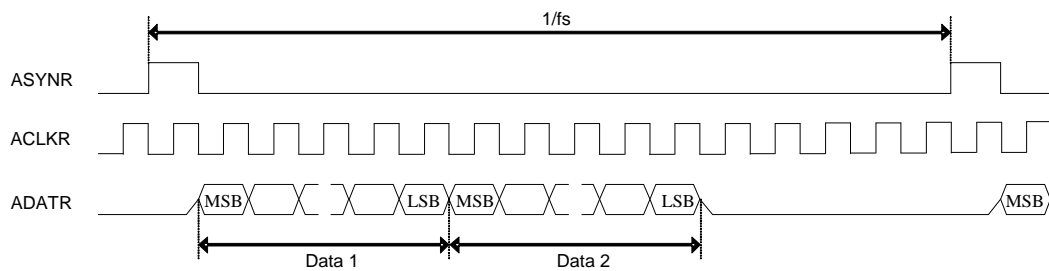


Fig22-2 ACLKMASTER=0, RM_SYNC=1

ASYNR is ACLKR rising edge triggered input

If ASYNR is input and ASYNR input is ACLKR rising edge triggered input as ASYNR input signal is changing after ACLKR rising edge, TW2866 output ADATR/ADATM by ACLKR falling edge triggered timing as shown on following figures. ASYNR signal is changing during ACLKR = 1. TW2866 output ADATR/ADATM data after next ACLKR falling edge triggered timing with less than half ACLKR clock delay.

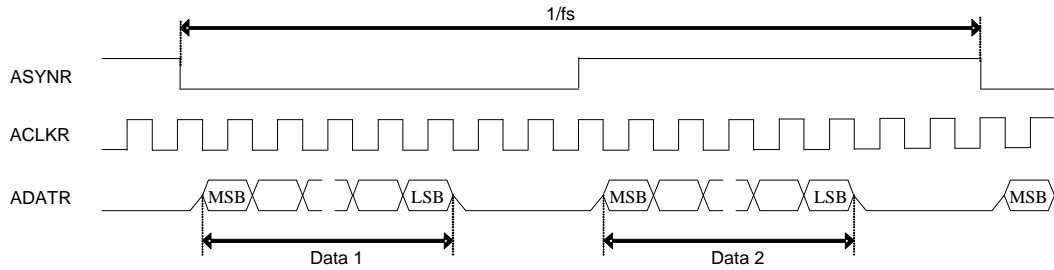


Fig22-3 ACLKMASTER=0, RM_SYNC=0, ASYNROEN=1

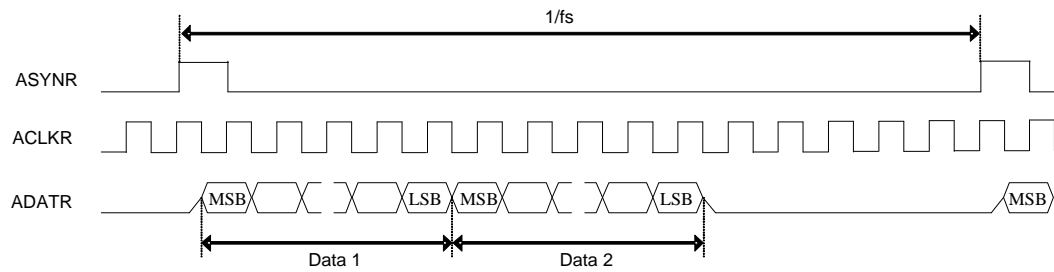


Fig22-4 ACLKMASTER=0, RM_SYNC=1, ASYNROEN=1

ACLKP/ASYNP Slave Mode Data Input Timing

Following 8 data input timings are supported. ADATPDLY register need to be set up according to the difference of ADATP data input timings. Data1 is only used as default. MSB bit is the first input bit as default PBINSWAP=0. If PBINSWAP=1, LSB bit is the first input bit.

ASYNP is ACLKP falling edge triggered input

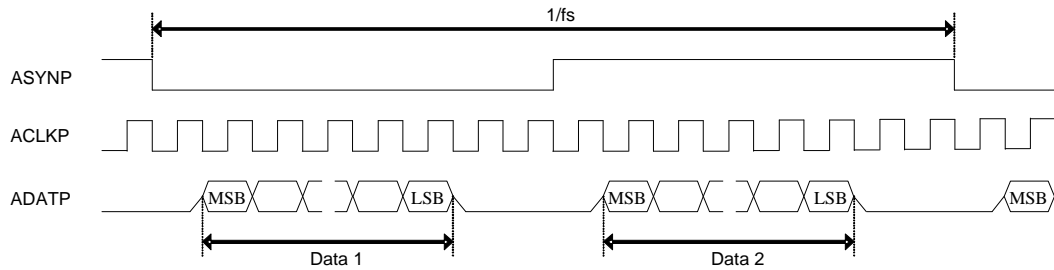


Fig23-1 RM_SYNC=0, PB_MASTER=0, ADATPDLY=0

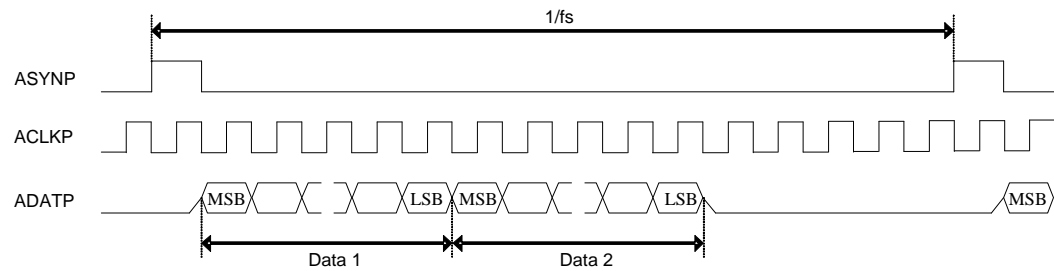


Fig23-2 RM_SYNC=1, PB_MASTER=0, ADATPDLY=0

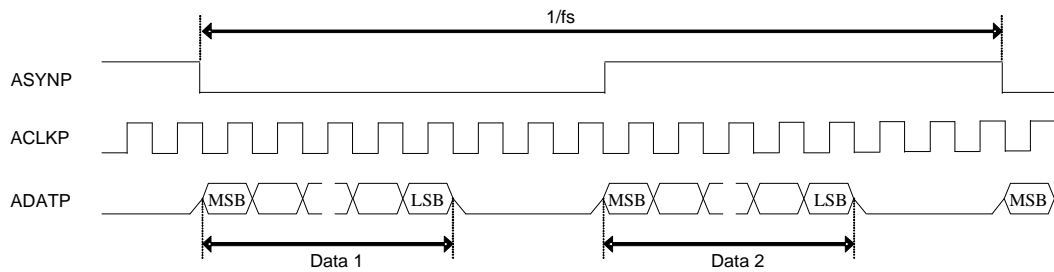


Fig23-3 RM_SYNC=0, PB_MASTER=0, ADATPDLY=1

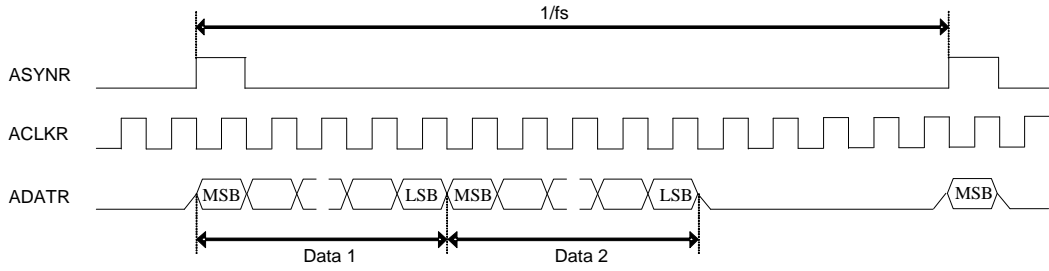


Fig23-4 RM_SYNC=1,PB_MASTER=0,ADATPDLY=1

ASYNP is ACLKP rising edge triggered input.

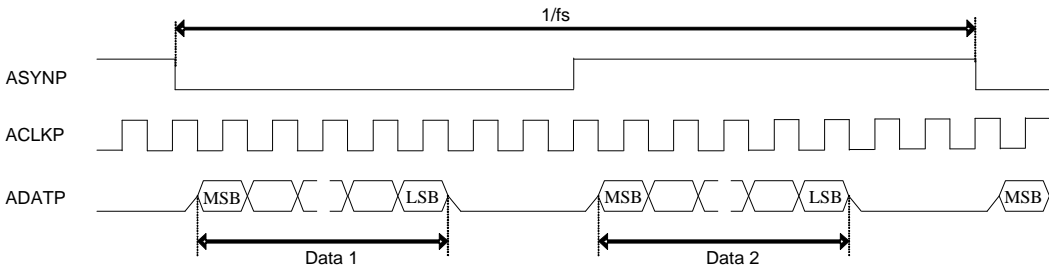


Fig23-5 RM_SYNC=0,PB_MASTER=0,ADATPDLY=1

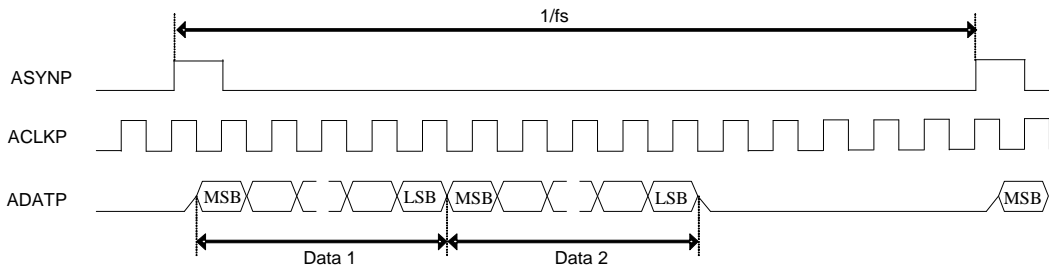
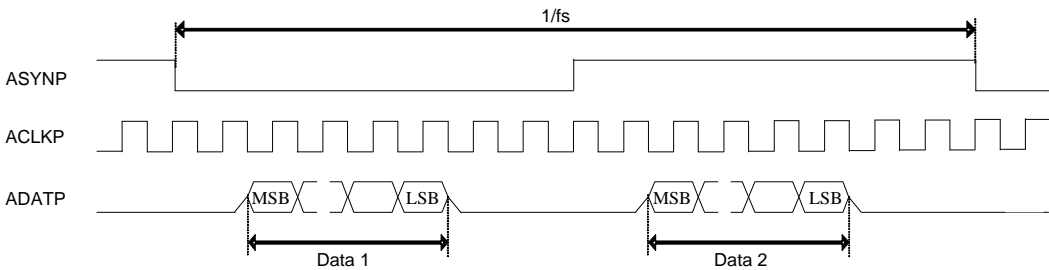


Fig23-6 RM_SYNC=1,PB_MASTER=0,ADATPDLY=1



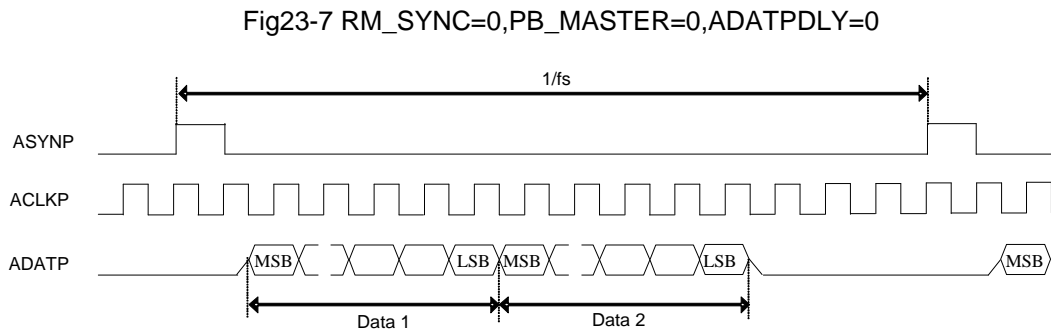


Fig23-8 RM_SYNC=1,PB_MASTER=0,ADATPDLY=0

Audio Clock Generation

TW2866 has built-in field locked audio clock generator for use in video capture applications. The circuitry will generate the same predefined number of audio sample clocks per field to ensure synchronous playback of video and audio after digital recording or compression. The audio clock is digitally synthesized from the crystal clock input. The master audio clock frequency is programmable through ACKN and ACKI register based following two equations.

$ACKN = \text{round}(F_{AMCLK} / F_{field})$, it gives the Audio master Clock Per Field.

$ACKI = \text{round}(F_{AMCLK} / F_{27MHz} * 2^{23})$, it gives the Audio master Clock Nominal increment.

Following table provides setting example of some common used audio frequency assuming Video Decoder system clock frequency of 27MHz. If ACLKRMASER register bit is set to 1, following AMCLK is used as audio system clock inside TW2866.

If Slave Playback-in lock mode is required, ACKN=00100hex and PBREFEN=1 needs to be set up. The number of AMCLK clock per one ASYNP input cycle is locked (fixed) to 256 in this mode.

Frequency equation is "AMCLK(Freq) = 256 x ASYNP(Freq)".

256xfs mode: AIN5MD=0,AFS384=0.

| AMCLK(MHz) | FIELD[Hz] | ACKN [dec] | ACKN [hex] | ACKI [dec] | ACKI [hex] |
|----------------------|-----------|------------|------------|------------|------------|
| 256 x 48 KHz | | | | | |
| 12.288 | 50 | 245760 | 3-C0-00 | 3817749 | 3A-41-15 |
| 12.288 | 59.94 | 205005 | 3-20-CD | 3817749 | 3A-41-15 |
| 256 x 44.1KHz | | | | | |
| 11.2896 | 50 | 225792 | 3-72-00 | 3507556 | 35-85-65 |
| 11.2896 | 59.94 | 188348 | 2-DF-BC | 3507556 | 35-85-65 |
| 256 x 32 KHz | | | | | |
| 8.192 | 50 | 163840 | 2-80-00 | 2545166 | 26-D6-0E |
| 8.192 | 59.94 | 136670 | 2-15-DE | 2545166 | 26-D6-0E |
| 256 x 16 KHz | | | | | |
| 4.096 | 50 | 81920 | 1-40-00 | 1272583 | 13-6B-07 |
| 4.096 | 59.94 | 68335 | 1-0A-EF | 1272583 | 13-6B-07 |
| 256 x 8 KHz | | | | | |
| 2.048 | 50 | 40960 | A0-00 | 636291 | 9-B5-83 |
| 2.048 | 59.94 | 34168 | 85-78 | 636291 | 9-B5-83 |

320xfs mode: AIN5MD=1,AFS384=0. 44.1kHz/48kHz are not supported.

| AMCLK(MHz) | FIELD[Hz] | ACKN [dec] | ACKN [hex] | ACKI [dec] | ACKI [hex] |
|---------------------|-----------|------------|------------|------------|------------|
| 320 x 32 KHz | | | | | |
| 10.24 | 50 | 204800 | 3-20-00 | 3181457 | 30-8B-91 |
| 10.24 | 59.94 | 170838 | 2-9B-56 | 3181457 | 30-8B-91 |
| 320 x 16 KHz | | | | | |
| 5.12 | 50 | 102400 | 1-90-00 | 1590729 | 18-45-C9 |
| 5.12 | 59.94 | 85419 | 1-4D-AB | 1590729 | 18-45-C9 |
| 320 x 8 KHz | | | | | |
| 2.56 | 50 | 51200 | C8-00 | 795364 | C-22-E4 |
| 2.56 | 59.94 | 42709 | A6-D5 | 795364 | C-22-E4 |

384xfs mode: AIN5MD=0,AFS384=1. 44.1kHz/48kHz are not supported.

| AMCLK(MHz) | FIELD[Hz] | ACKN [dec] | ACKN [hex] | ACKI [dec] | ACKI [hex] |
|---------------------|-----------|------------|------------|------------|------------|
| 384 x 32 KHz | | | | | |
| 12.288 | 50 | 245760 | 3-C0-00 | 3817749 | 3A-41-15 |
| 12.288 | 59.94 | 205005 | 3-20-CD | 381749 | 3A-41-15 |
| 384 x 16 KHz | | | | | |
| 6.144 | 50 | 122880 | 1-E0-00 | 1908874 | 1D-20-8A |
| 6.144 | 59.94 | 102503 | 1-90-67 | 1908874 | 1D-20-8A |
| 384 x 8 KHz | | | | | |
| 3.072 | 50 | 61440 | F0-00 | 954437 | E-90-45 |
| 3.072 | 59.94 | 51251 | C8-33 | 954437 | E-90-45 |

Audio Clock Auto Setup

If ACLKRMAS_{TER}=1 audio clock master mode is selected, and AFAUTO register is set to "1", TW2866 set up ACKI register by AFMD register value automatically. ACKI control input in ACKG module block is automatically set up to the required value by the condition of AIN5MD and AFS384 register value.

| AFAUTO | AFMD | ACKG module ACKI control input value |
|--------|------|--|
| 1 | 0 | 8kHz mode value by each AIN5MD/AFS384 case. |
| 1 | 1 | 16kHz mode value by each AIN5MD/AFS384 case. |
| 1 | 2 | 32kHz mode value by each AIN5MD/AFS384 case. |
| 1 | 3 | 44.1kHz mode value by each AIN5MD/AFS384 case. |
| 1 | 4 | 48kHz mode value by each AIN5MD/AFS384 case. |
| 0 | X | ACKI register set up ACKI control input value. |

Host Interface

Serial Interface

The two wire serial bus interface is used to allow an external micro-controller to write to or read from the data through the TW2866 register. The SCLK is the serial clock and SDAT is the data line. Both lines are pulled high by the resistors connected to VDD. The SADD[1:0] defines two LSB of the slave device address by tying the SADD pins either to VDD or GND.

| Slave Address | | | | | | | R/W |
|---------------|---|---|---|---|---------|---------|-----------------------|
| 0 | 1 | 0 | 1 | 0 | SADD[1] | SADD[0] | 1 = Read 0 = Write |

The TW2866 supports auto index increments in write/read mode if the data are in sequential order. Data transfer rate on the bus is up to 400 Kbits/s.

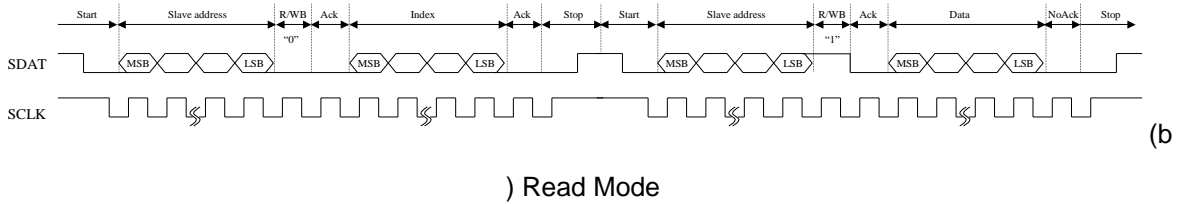
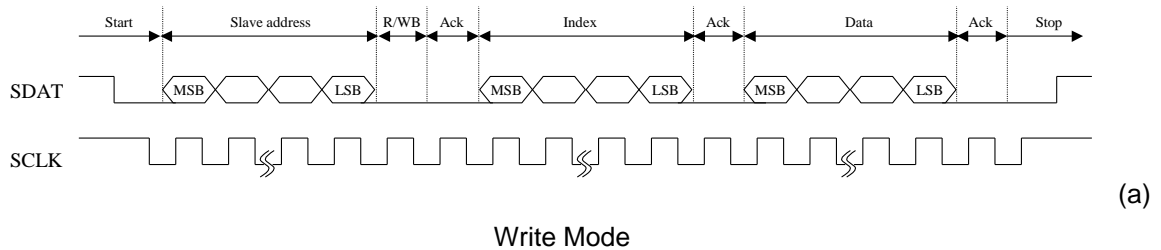
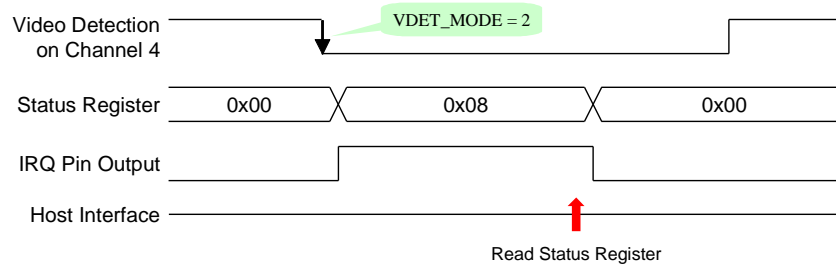


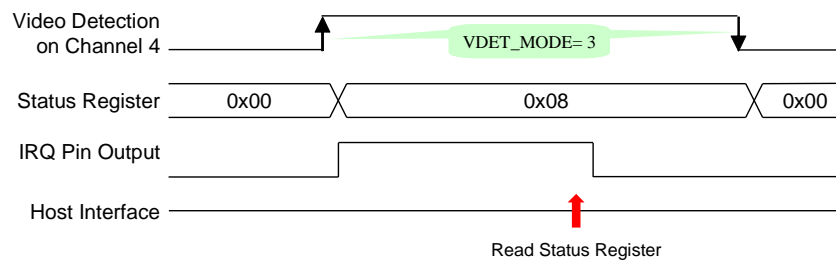
Fig24 Timing Chart of Serial Interface

Interrupt Interface

The TW2866 provides the interrupt request function using an IRQ pin so that the host does not need to waste much resource to detect video or audio signal from TW2866. To use interrupt request function, the interrupt request should be enabled by the IRQENA and polarity of the IRQ pin should be selected by the IRQPOL. Also, each channel of video and audio detection should be enabled by the AVDET_ENA. Then, the interrupt mode should be defined by the VDET_MODE and ADET_MODE that control the time to request interrupt and set the status register AVDET_STATE. The Fig25 shows operation of interrupt when the VDET_MODE and/or ADET_MODE are 2 and 3. The IRQ pin is cleared automatically by reading the AVDET_STATE. When the VDET_MODE and/or ADET_MODE is 1 or 2, the status register AVDET_STATE will also be cleared automatically by reading AVDET_STATE. However, when the VDET_MODE and/or ADET_MODE are 3, the status register AVDET_STATE will not be cleared automatically, but has the same value as actual status of video and audio detection flag.



(a) Status Register of Automatic Cleared Mode



(b) Status Register same as Video and Audio Detection Flag Mode

Fig25 Timing Diagram of Interrupt Interface

Squared Pixel mode operation

If FC27 register bit is set to 0, TW2866 works under Squared Pixel mode operation. XTI pin input on PAL-SQ mode should have either 59MHz(=29.5MHzx2) or 29.5MHz. Also, XTI pin input on NTSC-SQ mode should have either 49.086MHz(=24.543MHzx2) or 24.543MHz. HACTIVE register value should be 0x300(768dec) for PAL-SQ and 0x280(640dec) for NTSC-SQ. If Audio function is used with this Squared Pixel mode, ACKI register equation are as follows.

$ACKI = \text{round} (F_{AMCLK} / 29.5\text{MHz} * 2^{23})$for PAL-SQ

$ACKI = \text{round} (F_{AMCLK} / 24.543\text{MHz} * 2^{23})$for NTSC-SQ

Clock PLL

The TW2866 has built-in 2x/4x clock PLL to generate 2xXTI clock or 4xXTI clock. If 54MHz is connected to XTI pin, SEL_X24 register need to be 0(2x,default). If 27MHz is connected to XTI pin, SEL_X24 register need to be 1(4x). XTIMD register selects which clock source is used in the system. If analog clock PLL is not used, XTIMD register selects XTI input clock frequency mode.

Control Register

Register Map

| Address | | | | Mnemonic | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---------|------|------|------|------------|--------------|---------|---------------------|--------|--------------|-----------|--------------|--------|
| CH1 | CH2 | CH3 | CH4 | | | | | | | | | |
| 0x00 | 0x10 | 0x20 | 0x30 | VIDSTAT * | VDLOSS* | HLOCK* | SLOCK* | FLD* | VLOCK* | Reserved* | MONO* | DET50* |
| 0x01 | 0x11 | 0x21 | 0x31 | BRIGHT | BRIGHTNESS | | | | | | | |
| 0x02 | 0x12 | 0x22 | 0x32 | CONTRAST | CONTRAST | | | | | | | |
| 0x03 | 0x13 | 0x23 | 0x33 | SHARPNESS | SCURVE | VSF | CTI | | SHARPNESS | | | |
| 0x04 | 0x14 | 0x24 | 0x34 | SAT_U | SAT_U | | | | | | | |
| 0x05 | 0x15 | 0x25 | 0x35 | SAT_V | SAT_V | | | | | | | |
| 0x06 | 0x16 | 0x26 | 0x36 | HUE | HUE | | | | | | | |
| 0x07 | 0x17 | 0x27 | 0x37 | CROP_HI | VDELAY[9:8] | | VACTIVE[9:8] | | HDELAY[9:8] | | HACTIVE[9:8] | |
| 0x08 | 0x18 | 0x28 | 0x38 | VDELAY_LO | VDELAY[7:0] | | | | | | | |
| 0x09 | 0x19 | 0x29 | 0x39 | VACTIVE_LO | VACTIVE[7:0] | | | | | | | |
| 0x0A | 0x1A | 0x2A | 0x3A | HDELAY_LO | HDELAY[7:0] | | | | | | | |
| 0x0B | 0x1B | 0x2B | 0x3B | HACTIVE_LO | HACTIVE[7:0] | | | | | | | |
| 0x0C | 0x1C | 0x2C | 0x3C | MVSN* | SF* | PF* | FF* | KF* | CSBAD* | MCVSN* | CSTRIPE* | CTYPE* |
| 0x0D | 0x1D | 0x2D | 0x3D | STATUS2* | VCR* | WKAIR* | WKAIR1* | VSTD* | NINTL* | 0 | 0 | 0 |
| 0x0E | 0x1E | 0x2E | 0x3E | SDT | DETSTUS* | STDNOW* | | | ATREG | STANDARD | | |
| 0x0F | 0x1F | 0x2F | 0x3F | SDTR | ATSTART | PAL60EN | PALCNEN | PALMEN | NTSC44EN | SECAMEN | PALBEN | NTSCEN |
| 0xE4 | 0xE7 | 0xEA | 0xED | VSCALE_LO | VSCALE[7:0] | | | | | | | |
| 0xE5 | 0xE8 | 0xEB | 0xEE | SCALE_HI | VSCALE[11:8] | | | | HSACLE[11:8] | | | |
| 0xE6 | 0xE9 | 0xEC | 0xEF | HSCALE_LO | HSCALE[7:0] | | | | | | | |
| 0xA4 | 0xA5 | 0xA6 | 0xA7 | IDCNTL | IDX | | NSEN/SSEN/PSEN/WKTH | | | | | |
| 0xC4 | 0xC5 | 0xC6 | 0xC7 | HREF* | HREF | | | | | | | |

Note : * Read only registers

| Address | | | | Mnemonic | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---------|-----|-----|-----|-------------|-------------|--------------|-----------|-----------|------------|------------|-----------|-----------|
| CH1 | CH2 | CH3 | CH4 | | | | | | | | | |
| 0x41 | | | | ENCCTL | HZ50 | INTERLACE | FSCSEL | | COFF | PHALT | PDRST | PED |
| 0x42 | | | | ENCTEST1 | YBW | | CBW | | CBGEN | TCSEL | | |
| 0x43 | | | | ENCCLK | CKMST | ENCKPOL | NONSTA | FRUN | YDEL | | | |
| 0x44 | | | | ENCOUT | CVBS_YSEL | CVBS_CSEL | ENCTMODE | | | | | |
| 0x45 | | | | SCH | SCH | | | | | | | |
| 0x46 | | | | ENCYGAIN | ENCYGAIN | | | | | | | |
| 0x47 | | | | ENCCGAIN | ENCCGAIN | | | | | | | |
| 0x48 | | | | ENCSGAIN | ENCSGAIN | | | | | | | |
| 0x49 | | | | ENCBGAIN | ENCBGAIN | | | | | | | |
| 0x4A | | | | ENCIREF | VDA_IREFC | | | | VDA_IREFY | | | |
| 0x4B | | | | ENCTEST2 | ENCVDOUT | TEST_DAC | VDA_PDC | VDA_PDY | VDAC_CKPOL | ENC_LOOP | LOOP_CH | |
| 0x4C | | | | EVDELAY | 0 | 0 | 0 | EVDELAY | | | | |
| 0x4D | | | | EHDELAY | 0 | 0 | EHDELAY | | | | | |
| 0x50 | | | | ADACCT1 | ADACLK_INV | DAC_IB_DAC | | | 0 | DAC_IB_ADC | | |
| 0x51 | | | | DAC_LPFBIAS | DAC_LPFBIAS | | | | | | | |
| 0x52 | | | | ADACLPF | 0 | LPF_SEL | | | BIAS_SEL | DAC_IB_OTA | | |
| 0x53 | | | | ANADACTEST | 0 | TAADCO | | | TVSENSE | ANADACTEST | | |
| 0x54 | | | | ASAVE | 0 | 0 | DOUT_RST | DIV_RST | ACALEN | ASAVE | | |
| 0x58 | | | | VSENSE* | VSENSE4B* | VSENSE3B* | VSENSE2B* | VSENSE1B* | VSENSE4A* | VSENSE3A* | VSENSE2A* | VSENSE1A* |
| 0x59 | | | | PDBV | PDBV4B | PDBV3B | PDBV2B | PDBV1B | PDBV4A | PDBV3A | PDBV2A | PDBV1A |
| 0x5A | | | | VSAVE | AVDSMD | VREF50M_AVDS | BIAS_AVDS | | PD_BIAS | VSAVE | | |
| 0x5B | | | | DS | VD4_DS | VD3_DS | VD2_DS | VD1_DS | CK4_DS | CK3_DS | CK2_DS | CK1_DS |
| 0x5C | | | | BGCTL | 0 | 0 | BGCTL | VSWEN | VSWNUM | | | |
| 0x5D | | | | CH2MISC2 | NKILL_2 | PKILL_2 | SKILL_2 | CBAL_2 | FCS_2 | LCS_2 | CCS_2 | BST_2 |
| 0x5E | | | | CH3MISC2 | NKILL_3 | PKILL_3 | SKILL_3 | CBAL_3 | FCS_3 | LCS_3 | CCS_3 | BST_3 |
| 0x5F | | | | CH4MISC2 | NKILL_4 | PKILL_4 | SKILL_4 | CBAL_4 | FCS_4 | LCS_4 | ICCS_4 | BST_4 |

| Address | | | | Mnemonic | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---------|-----|-----|-----|------------|---------------|-----------|-----------|------------|-----------|-----------|---------------|--------------|
| CH1 | CH2 | CH3 | CH4 | | | | | | | | | |
| 0x60 | | | | PLL1 | 0 | PLL_PD | PLLIREF | SEL_X24 | LP_X4 | | CP_X4 | |
| 0x61 | | | | PLL2 | 0 | 0 | 0 | DECOSC | CKOUTSEL | | XTIMD | |
| 0x65 | | | | VDOEB | P0 | 0 | 0 | D4ORD | VD4OEB | VD3OEB | VD2OEB | VD1OEB |
| 0x66 | | | | CK13 | VD4_27C | VD3_27C | VD2_27C | VD1_27C | CK4_13 | CK3_13 | CK2_13 | CK1_13 |
| 0x67 | | | | CK2DEL | CLKNO2_DEL | | | CLKPO2_DEL | | | | |
| 0x68 | | | | CK3DEL | CLKNO3_DEL | | | CLKPO3_DEL | | | | |
| 0x69 | | | | CLK4DEL | CLKNO4_DEL | | | CLKPO4_DEL | | | | |
| 0x6A | | | | CLK2MD | 0 | 0 | CLKNO2OEB | CLKPO2OEB | CLKNO2MD | | CLKPO2MD | |
| 0x6B | | | | CLK3MD | 0 | 0 | CLKNO3OEB | CLKPO3OEB | CLKNO3MD | | CLKPO3MD | |
| 0x6C | | | | CLK4MD | 0 | 0 | CLKNO4OEB | CLKPO4OEB | CLKNO4MD | | CLKPO4MD | |
| 0x6D | | | | CLKPNPOL | CLKNO4POL | CLKPO4POL | CLKNO3POL | CLKPO3POL | CLKNO2POL | CLKPO2POL | 0 | 0 |
| 0x6E | | | | A12NUM | 0 | A2NUM | | | 0 | A1NUM | | |
| 0x6F | | | | A34NUM | 0 | A4NUM | | | 0 | A3NUM | | |
| 0x70 | | | | ACLKPOL | 0 | S2I_8BIT | ACLKRPOL | ACLKPPOL | AFAUTO | AFMD | | |
| 0x71 | | | | AINCTL | I2S8MODE | MASCKMD | PBINSWAP | ASYNRDLY | ASYNPDLY | ADATPDLY | INLAWMD | |
| 0x72 | | | | MRATIOMD | MRATIOMD | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x73 | | | | A5NUM | AIMANU | A5NUM | | 0 | 0 | 0 | A5DET_ENA | |
| 0x74 | | | | A5DETST | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A5DET_STATE* |
| 0x75 | | | | AADC5OFS_H | 0 | 0 | 0 | 0 | 0 | 0 | AADC5OFS[9:8] | |
| 0x76 | | | | AADC5OFS_L | AADC5OFS[7:0] | | | | | | | |
| 0x77 | | | | AUD5ADC_H | 0 | 0 | 0 | 0 | 0 | 0 | AUD5ADC[9:8] | |
| 0x78 | | | | AUD5ADC_L | AUD5ADC[7:0] | | | | | | | |
| 0x79 | | | | ADJAADC5_H | 0 | 0 | 0 | 0 | 0 | 0 | ADJAADC5[9:8] | |
| 0x7A | | | | ADJAADC5_L | ADJAADC5[7:0] | | | | | | | |

| Address | | | | Mnemonic | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---------|-----|-----|-----|-----------|---------------|--------------|----------|---------------|------------|------------|----------|----------|
| CH1 | CH2 | CH3 | CH4 | | | | | | | | | |
| 0x7B | | | | I2SO_RSEL | 0 | 0 | 0 | I2SO_RSEL | | | | |
| 0x7C | | | | I2SO_LSEL | 0 | 0 | 0 | I2SO_LSEL | | | | |
| 0x7D | | | | RECSEL5 | RECSEL54 | | RECSEL53 | | RECSEL52 | | RECSEL51 | |
| 0x7E | | | | ADATMI2S | A5OUTOFF | ADATMI2SOEN | MUTEA5 | ADET_TH5[4:0] | | | | |
| 0x7F | | | | AIGAIN5 | AIGAIN5 | | | | MIX_RATIO5 | | | |
| 0x80 | | | | SRST | 0 | 0 | AUDIORST | VOUTrST | VDEC4RST | VDEC3RST | VDEC2RST | VDEC1RST |
| 0x81 | | | | ACNTL | 0 | IREF | VREF | 0 | CLKPDN | 0 | YFLEN | YSV |
| 0x82 | | | | ACNTL2 | CTEST | YCLEN | 0 | AFLTEN | GTEST | VLPF | CKLY | CKLC |
| 0x83 | | | | CNTRL1 | PBW | DEM | PALSW | SET7 | COMB | HCOMP | YCOMB | PDLY |
| 0x84 | | | | CKHY | GMEN | CKHY | | HSDLY | | | | |
| 0x85 | | | | SHCOR | SHCOR | | | VIN4 | VIN3 | VIN2 | VIN1 | |
| 0x86 | | | | CORING | CTCOR | | CCOR | VCOR | | CIF | | |
| 0x87 | | | | CLMPG | CLPEND | | | CLPST | | | | |
| 0x88 | | | | IAGC | NMGAIN | | | WPGAIN | | | 0 | |
| 0x89 | | | | AIN5MD | 0 | 0 | ACLKR128 | ACLKR64 | AFS384 | AIN5MD | 0 | 1 |
| 0x8A | | | | PEAKWT | PEAKWT | | | | | | | |
| 0x8B | | | | CLMPL | CLMPLD | CLMPL | | | | | | |
| 0x8C | | | | SYNCT | SYNCTD | SYNCT | | | | | | |
| 0x8D | | | | MISSCNT | MISSCNT | | | | HSWIN | | | |
| 0x8E | | | | PCLAMP | PCLAMP | | | | | | | |
| 0x8F | | | | VCNTL1 | VLCKI | | VLCKO | | VMODE | DETV | AFLD | VINT |
| 0x90 | | | | VCNTL2 | BSHT | | | VSHT | | | | |
| 0x91 | | | | CKILL | CKILMAX | | | CKILMIN | | | | |
| 0x92 | | | | COMB | COMBMD | HTL | | | VTL | | | |
| 0x93 | | | | LDLY | CKLM | YDLY | | | HPF_RES | | | |
| 0x94 | | | | MISC1 | HPLC | ENCNT | PALC | SDET | TBCEN | BYPASS | SYOUT | 0 |
| 0x95 | | | | LOOP | HPM | | ACCT | | SPM | | CBW | |
| 0x96 | | | | MISC2 | NKILL | PKILL | SKILL | CBAL | FCS | LCS | CCS | BST |
| 0x97 | | | | CLMD | FRM | | YNR | | CLMD | | PSP | |
| 0x98 | | | | HSLOWCTL | 0 | HSBEGIN[2:0] | | | 0 | HSEND[2:0] | | |
| 0x99 | | | | HSBEGIN | HSBEGIN[10:3] | | | | | | | |

| Address | | | | Mnemonic | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---------|-----|-----|-----|-------------|---------------|--------|---------------|--------|---------------|-------------|---------------|-------------|
| CH1 | CH2 | CH3 | CH4 | | | | | | | | | |
| 0x9A | | | | HSEND | HSEND[10:3] | | | | | | | |
| 0x9B | | | | OVSDLY | OVSDLY | | | | | | | |
| 0x9C | | | | OVSEND | HASYNC | OFDLY | | | VSMODE | OVSEND | | |
| 0x9D | | | | HBLN | HBLN | | | | | | | |
| 0x9E | | | | NOVID | 0 | FC27 | CHID_MD | | NOVID_656 | EAVSWAP | VIPCFCG | NTSC656 |
| 0x9F | | | | CLK1MD | CLKNO1_DEL | | | | CLKPO1_DEL | | | |
| 0xA8 | | | | HFLT21 | HFLT2 | | | | HFLT1 | | | |
| 0xA9 | | | | HFLT43 | HFLT4 | | | | HFLT3 | | | |
| 0xAA | | | | AGCEN | AGCEN4 | AGCEN3 | AGCEN2 | AGCEN1 | AGCGAIN4[8] | AGCGAIN3[8] | AGCGAIN2[8] | AGCGAIN1[8] |
| 0xAB | | | | AGCGAIN1 | AGCGAIN1[7:0] | | | | | | | |
| 0xAC | | | | AGCGAIN2 | AGCGAIN2[7:0] | | | | | | | |
| 0xAD | | | | AGCGAIN3 | AGCGAIN3[7:0] | | | | | | | |
| 0xAE | | | | AGCGAIN4 | AGCGAIN4[7:0] | | | | | | | |
| 0xAF | | | | VSH21 | 0 | VSH2 | | | 0 | VSH1 | | |
| 0xB0 | | | | VSH43 | 0 | VSH4 | | | 0 | VSH3 | | |
| 0xB1 | | | | NOVIDMODE | CH8IDEN | 0 | NOVIDMODE | | 0 | 0 | 0 | 0 |
| 0xB2 | | | | VDLOSSOE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | VDLOSSOE |
| 0xB3 | | | | AADC0FS_H | AADC4OFS[9:8] | | AADC3OFS[9:8] | | AADC2OFS[9:8] | | AADC1OFS[9:8] | |
| 0xB4 | | | | AADC1OFS_L | AADC1OFS[7:0] | | | | | | | |
| 0xB5 | | | | AADC2OFS_L | AADC2OFS[7:0] | | | | | | | |
| 0xB6 | | | | AADC3OFS_L | AADC3OFS[7:0] | | | | | | | |
| 0xB7 | | | | AADC4OFS_L | AADC4OFS[7:0] | | | | | | | |
| 0xB8 | | | | AUDADC_H* | AUD4ADC[9:8] | | AUD3ADC[9:8] | | AUD2ADC[9:8] | | AUD1ADC[9:8] | |
| 0xB9 | | | | AUD1ADC_L* | AUD1ADC[7:0] | | | | | | | |
| 0xBA | | | | AUD2ADC_L* | AUD2ADC[7:0] | | | | | | | |
| 0xBB | | | | AUD3ADC_L* | AUD3ADC[7:0] | | | | | | | |
| 0xBC | | | | AUD4ADC_L* | AUD4ADC[7:0] | | | | | | | |
| 0xBD | | | | ADJAADC_H* | ADJAADC4[9:8] | | ADJAADC3[9:8] | | ADJAADC2[9:8] | | ADJAADC1[9:8] | |
| 0xBE | | | | ADJAADC1_L* | ADJAADC1[7:0] | | | | | | | |
| 0xBF | | | | ADJAADC2_L* | ADJAADC2[7:0] | | | | | | | |
| 0xC0 | | | | ADJAADC3_L* | ADJAADC3[7:0] | | | | | | | |
| 0xC1 | | | | ADJAADC4_L* | ADJAADC4[7:0] | | | | | | | |

| Address | | | | Mnemonic | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---------|-----|-----|-----|----------|-----------|-----------|------------|------------|-------------|-------------|-------------|-------------|
| CH1 | CH2 | CH3 | CH4 | | | | | | | | | |
| 0xC8 | | | | CLK_DEL1 | GPP_VAL2 | MPP_MODE2 | | GPP_VAL1 | MPP_MODE1 | | | |
| 0xC9 | | | | CLK_DEL2 | GPP_VAL4 | MPP_MODE4 | | GPP_VAL3 | MPP_MODE3 | | | |
| 0xCA | | | | CHMD | CHMD4 | | CHMD3 | | CHMD2 | | CHMD1 | |
| 0xCB | | | | CIF54M | POLMPP4 | POLMPP3 | POLMPP2 | POLMPP1 | CIF54M4 | CIF54M3 | CIF54M2 | CIF54M1 |
| 0xCC | | | | SELCH | SELCH4 | | SELCH3 | | SELCH2 | | SELCH1 | |
| 0xCD | | | | MAINCH | MAINCH4 | | MAINCH3 | | MAINCH2 | | MAINCH1 | |
| 0xCE | | | | ANAPWDN | AAUTOMUTE | HPF_RES | A_DAC_PWDN | A_ADC_PWDN | V4_ADC_PWDN | V3_ADC_PWDN | V2_ADC_PWDN | V1_ADC_PWDN |
| 0xCF | | | | SMD | SMD | | VRSTSEL | | 0 | 0 | 0 | 0 |
| 0xD0 | | | | AIGAIN21 | AIGAIN2 | | | | AIGAIN1 | | | |
| 0xD1 | | | | AIGAIN43 | AIGAIN4 | | | | AIGAIN3 | | | |
| 0xD2 | | | | R_MULTCH | M_RLSWAP | RM_SYNC | RM_PBSEL | | R_ADATM | | R_MULTCH | |
| 0xD3 | | | | R_SEQ10 | R_SEQ_1 | | | | R_SEQ_0 | | | |
| 0xD4 | | | | R_SEQ32 | R_SEQ_3 | | | | R_SEQ_2 | | | |
| 0xD5 | | | | R_SEQ54 | R_SEQ_5 | | | | R_SEQ_4 | | | |
| 0xD6 | | | | R_SEQ76 | R_SEQ_7 | | | | R_SEQ_6 | | | |
| 0xD7 | | | | R_SEQ98 | R_SEQ_9 | | | | R_SEQ_8 | | | |
| 0xD8 | | | | R_SEQBA | R_SEQ_B | | | | R_SEQ_A | | | |
| 0xD9 | | | | R_SEQDC | R_SEQ_D | | | | R_SEQ_C | | | |
| 0xDA | | | | R_SEQFE | R_SEQ_F | | | | R_SEQ_E | | | |

| Address | | | | Mnemonic | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | |
|---------|-----|-----|-----|--------------|---------------|-------------|-------------|---------------|-------------|-------------|---------------|--------------|--|
| CH1 | CH2 | CH3 | CH4 | | | | | | | | | | |
| 0xDB | | | | AMASTER | ADACEN | AADCEN | PB_MASTER | PB_LRSEL | PB_SYNC | RM_8BIT | ASYNROEN | ACLKRMMASTER | |
| 0xDC | | | | MIX_MUTE | LAWMD | | MIX_DERATIO | MIX_MUTE | | | | | |
| 0xDD | | | | MIX_RATIO21 | MIX_RATIO2 | | | MIX_RATIO1 | | | | | |
| 0xDE | | | | MIX_RATIO43 | MIX_RATIO4 | | | | | | MIX_RATIO3 | | |
| 0xDF | | | | MIX_RATIO1P | 1 | 0 | 0 | 0 | MIX_RATIO1P | | | | |
| 0xE0 | | | | MIX_OUTSEL | VADCCKPOL | AADCCKPOL | ADACCKPOL | MIX_OUTSEL | | | | | |
| 0xE1 | | | | ADET | AAMPMD | ADET_FILTER | | ADET_TH4[4] | ADET_TH3[4] | ADET_TH2[4] | ADET_TH1[4] | | |
| 0xE2 | | | | ADET_TH21 | ADET_TH2[3:0] | | | ADET_TH1[3:0] | | | | | |
| 0xE3 | | | | ADET_TH43 | ADET_TH4[3:0] | | | | | | ADET_TH3[3:0] | | |
| 0xF0 | | | | ACKI_L | ACKI[7:0] | | | | | | | | |
| 0xF1 | | | | ACKI_M | ACKI[15:8] | | | | | | | | |
| 0xF2 | | | | ACKI_H | 0 | 0 | ACKI[21:16] | | | | | | |
| 0xF3 | | | | ACKN_L | ACKN[7:0] | | | | | | | | |
| 0xF4 | | | | ACKN_M | ACKN[15:8] | | | | | | | | |
| 0xF5 | | | | ACKN_H | 0 | 0 | 0 | 0 | 0 | 0 | ACKN[17:16] | | |
| 0xF6 | | | | SDIV | 0 | 0 | SDIV | | | | | | |
| 0xF7 | | | | LRDIV | 0 | 0 | LRDIV | | | | | | |
| 0xF8 | | | | ACCNTL | APZ | APG | | 0 | ACPL | SRPH | LRPH | | |
| 0xF9 | | | | VMISC | LIM16 | PBREFEN | YCBCR422 | HA656MD | VBI_FRAM | CNTL656 | VSCL_SYNC | HA_EN | |
| 0xFA | | | | CLKOCTL | VSCL_ENA | OE | CLKNO1_OEB | CLKPO1_OEB | CLKNO1_MD | | CLKPO1_MD | | |
| 0xFB | | | | AVDET_MODE | CLKNO1_POL | CLKPO1_POL | IRQENA | IRQPOL | ADET_MODE | | VDET_MODE | | |
| 0xFC | | | | AVDET_ENA | AVDET_ENA | | | | | | | | |
| 0xFD | | | | AVDET_STATE* | AVDET_STATE | | | | | | | | |
| 0xFE | | | | TEST | DEV_ID[6:5]* | | 0 | 0 | 0 | TEST | | | |
| 0xFF | | | | DEV_ID* | DEV_ID[4:0]* | | | | REV_ID | | | | |

Note : * Read only registers

Register Description**0x00(CH1)/0x10(CH2)/0x20(CH3)/0x30(CH4) – Video Status Register**

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | VDLOSS | R | 1 = Video not present. (sync is not detected in number of consecutive line periods specified by MISSCNT register) 0 = Video detected. | 0 |
| 6 | HLOCK | R | 1 = Horizontal sync PLL is locked to the incoming video source. 0 = Horizontal sync PLL is not locked. | 0 |
| 5 | SLOCK | R | 1 = Sub-carrier PLL is locked to the incoming video source. 0 = Sub-carrier PLL is not locked. | 0 |
| 4 | FIELD | R | 0 = Odd field is being decoded. 1 = Even field is being decoded. | 0 |
| 3 | VLOCK | R | 1 = Vertical logic is locked to the incoming video source. 0 = Vertical logic is not locked. | 0 |
| 2 | Reserved | R | Reserved | 0 |
| 1 | MONO | R | 1 = No color burst signal detected. 0 = Color burst signal detected. | 0 |
| 0 | DET50 | R | 0 = 60Hz source detected 1 = 50Hz source detected The actual vertical scanning frequency depends on the current standard invoked. | 0 |

0x01(CH1)/0x11(CH2)/0x21(CH3)/0x31(CH4) – BRIGHTNESS Control Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-0 | BRIGHT | R/W | These bits control the brightness. They have value of –128 to 127 in 2's complement form. Positive value increases brightness. A value 0 has no effect on the data. | 00 |

0x02(CH1)/0x12(CH2)/0x22(CH3)/0x32(CH4) – CONTRAST Control Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-0 | CNTRST | R/W | These bits control the luminance contrast gain. A value of 100 (64h) has a gain of 1. The range of adjustment is from 0% to 255% at 1% per step. | 64h |

0x03(CH1)/0x13(CH2)/0x23(CH3)/0x33(CH4) – SHARPNESS Control Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | SCURVE | R/W | This bit controls the center frequency of the peaking filter. The corresponding gain adjustment is HFLT. 0 = low 1 = center | 0 |
| 6 | VSF | R/W | This bit is for internal used. | 0 |
| 5-4 | CTI | R/W | CTI level selection. 0 = None. 3 = highest. | 1 |
| 3-0 | SHARP | R/W | These bits control the amount of sharpness enhancement on the luminance signals. There are 16 levels of control with '0' having no effect on the output image. 1 through 15 provides sharpness enhancement with 'F' being the strongest. | 1 |

0x04(CH1)/0x14(CH2)/0x24(CH3)/0x34(CH4) – Chroma (U) Gain Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-0 | SAT_U | R/W | These bits control the digital gain adjustment to the U (or Cb) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. | 80 |

0x05(CH1)/0x15(CH2)/0x25(CH3)/0x35(CH4) – Chroma (V) Gain Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-0 | SAT_V | R/W | These bits control the digital gain adjustment to the V (or Cr) component of the digital video signal. The color saturation can be adjusted by adjusting the U and V color gain components by the same amount in the normal situation. The U and V can also be adjusted independently to provide greater flexibility. The range of adjustment is 0 to 200%. A value of 128 (80h) has gain of 100%. | 80 |

0x06(CH1)/0x16(CH2)/0x26(CH3)/0x36(CH4) – Hue Control Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-0 | HUE | R/W | These bits control the color hue as 2's complement number. They have value from +90° (7Fh) to -90° (80h) with an increment of 2.8°. The 2 LSB has no effect. The positive value gives greenish tone and negative value gives purplish tone. The default value is 0° (00h). This is effective only on NTSC and PAL system. | 00 |

0x07(CH1)/0x17(CH2)/0x27(CH3)/0x37(CH4) – Cropping Register, High

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|--|-------|
| 7-6 | VDELAY_HI | R/W | These bits are bit 9 to 8 of the 10-bit Vertical Delay register. | 0 |
| 5-4 | VACTIVE_HI | R/W | These bits are bit 9 to 8 of the 10-bit VACTIVE register. Refer to description on Reg09 for its shadow register. | 1 |
| 3-2 | HDELAY_HI | R/W | These bits are bit 9 to 8 of the 10-bit Horizontal Delay register. | 0 |
| 1-0 | HACTIVE_HI | R/W | These bits are bit 9 to 8 of the 10-bit HACTIVE register. | 2 |

0x08(CH1)/0x18(CH2)/0x28(CH3)/0x38(CH4) – Vertical Delay Register, Low

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|--|-------|
| 7-0 | VDELAY_LO | R/W | These bits are bit 7 to 0 of the 10-bit Vertical Delay register. The two MSBs are in the CROP_HI register. It defines the number of lines between the leading edge of VSYNC and the start of the active video. | 12 |

0x09(CH1)/0x19(CH2)/0x29(CH3)/0x39(CH4) – Vertical Active Register, Low

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|--|-------|
| 7-0 | VACTIVE_LO | R/W | <p>These bits are bit 7 to 0 of the 10-bit Vertical Active register. The two MSBs are in the CROP_HI register. It defines the number of active video lines per frame output.</p> <p>The VACTIVE register has a shadow register for use with 50Hz source when ATREG of Reg0x1C is not set. This register can be accessed through the same index address by first changing the format standard to any 50Hz standard.</p> | 20 |

0x0A(CH1)/0x1A(CH2)/0x2A(CH3)/0x3A(CH4) – Horizontal Delay Register, Low

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|--|-------|
| 7-0 | HDELAY_LO | R/W | <p>These bits are bit 7 to 0 of the 10-bit Horizontal Delay register. The two MSBs are in the CROP_HI register. It defines the number of pixels between the leading edge of the HSYNC and the start of the image cropping for active video.</p> <p>The HDELAY_LO register has two shadow registers for use with PAL and SECAM sources respectively. These register can be accessed using the same index address by first changing the decoding format to the corresponding standard.</p> | 0A |

0x0B(CH1)/0x1B(CH2)/0x2B(CH3)/0x3B(CH4) – Horizontal Active Register, Low

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|--|-------|
| 7-0 | HACTIVE_LO | R/W | <p>These bits are bit 7 to 0 of the 10-bit Horizontal Active register. The two MSBs are in the CROP_HI register. It defines the number of active pixels per line output.</p> | D0 |

0x0C(CH1)/0x1C(CH2)/0x2C(CH3)/0x3C(CH4) – Macrovision Detection

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | SF | R | This bit is for internal use. | 0 |
| 6 | PF | R | This bit is for internal use. | 0 |
| 5 | FF | R | This bit is for internal use. | 0 |
| 4 | KF | R | This bit is for internal use. | 0 |
| 3 | CSBAD | R | 1 = Macrovision color stripe detection may be un-reliable | 0 |
| 2 | MVCSN | R | 1 = Macrovision AGC pulse detected. 0 = Not detected. | 0 |
| 1 | CSTRIPE | R | 1 = Macrovision color stripe protection burst detected. 0 = Not detected. | 0 |
| 0 | CTYPE | R | This bit is valid only when color stripe protection is detected, i.e. CSTRIPE=1. 1 = Type 2 color stripe protection 0 = Type 3 color stripe protection | 0 |

0x0D(CH1)/0x1D(CH2)/0x2D(CH3)/0x3D(CH4) – Chip STATUS II

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | VCR | R | VCR signal indicator. | 0 |
| 6 | WKAIR | R | Weak signal indicator 2. | 0 |
| 5 | WKAIR1 | R | Weak signal indicator controlled by WKTH. | 0 |
| 4 | VSTD | R | 1 = Standard signal 0 = Non-standard signal | 0 |
| 3 | NINTL | R | 1 = Non-interlaced signal 0 = interlaced signal | 0 |
| 2-0 | Reserved | R | Reserved | 0h |

0x0E(CH1)/0x1E(CH2)/0x2E(CH3)/0x3E(CH4) – Standard Selection

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|---|-------|
| 7 | DETSTATUS | R | 0 = Idle 1 = detection in progress | 0 |
| 6-4 | STDNOW | R | Current standard invoked 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Not valid | 0 |
| 3 | ATREG | R/W | 1 = Disable the shadow registers. 0 = Enable VACTIVE and HDELAY shadow registers value depending on standard | 0 |
| 2-0 | STD | R/W | Standard selection 0 = NTSC(M) 1 = PAL (B,D,G,H,I) 2 = SECAM 3 = NTSC4.43 4 = PAL (M) 5 = PAL (CN) 6 = PAL 60 7 = Auto detection | 7 |

0x0F(CH1)/0x1F(CH2)/0x2F(CH3)/0x3F(CH4) – Standard Recognition

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7 | ATSTART | R/W | Writing 1 to this bit will manually initiate the auto format detection process. This bit is a self-resetting bit. | 0 |
| 6 | PAL6_EN | R/W | 1 = enable recognition of PAL60. 0 = disable recognition. | 1 |
| 5 | PALN_EN | R/W | 1 = enable recognition of PAL (CN). 0 = disable recognition. | 1 |
| 4 | PALM_EN | R/W | 1 = enable recognition of PAL (M). 0 = disable recognition. | 1 |
| 3 | NT44_EN | R/W | 1 = enable recognition of NTSC 4.43. 0 = disable recognition. | 1 |
| 2 | SEC_EN | R/W | 1 = enable recognition of SECAM. 0 = disable recognition. | 1 |
| 1 | PALB_EN | R/W | 1 = enable recognition of PAL (B,D,G,H,I). 0 = disable recognition. | 1 |
| 0 | NTSC_EN | R/W | 1 = enable recognition of NTSC (M). 0 = disable recognition. | 1 |

0xE4(CH1)/0xE7(CH2)/0xEA(CH3)/0xED(CH4) – Vertical Scaling Register, Low

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|---|-------|
| 7-0 | VSCALE_LO | R/W | These bits are bit 7 to 0 of the 12-bit vertical scaling ratio register | 00 |

0xE5(CH1)/0xE8(CH2)/0xEB(CH3)/0xEE(CH4) – Scaling Register, High

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|---|-------|
| 7-4 | VSCALE_HI | R/W | These bits are bit 11 to 8 of the 12-bit vertical scaling ratio register. | 1 |
| 3-0 | HSCALE_HI | R/W | These bits are bit 11 to 8 of the 12-bit horizontal scaling ratio register. | 1 |

0xE6(CH1)/0xE9(CH2)/0xEC(CH3)/0xEF(CH4) – Horizontal Scaling Register, Low

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|--|-------|
| 7-0 | HSCALE_LO | R/W | These bits are bit 7 to 0 of the 12-bit horizontal scaling ratio register. | 00 |

0xA4(CH1)/0xA5(CH2)/0xA6(CH3)/0xA7(CH4) – ID Detection Control

| Bit | Function | R/W | Description | Reset |
|-----|------------------------------------|-----|---|----------------------------|
| 7-6 | IDX | R/W | These two bits indicate which of the four lower 6-bit registers is currently being controlled. The write sequence is a two steps process unless the same register is written. A write of {ID,000000} selects one of the four registers to be written. A subsequent write will actually write into the register. | 0 |
| 5-0 | NSEN / SSEN / PSEN / WKTH | R/W | IDX = 0 controls the NTSC color carrier detection sensitivity (NSEN). IDX = 1 controls the SECAM ID detection sensitivity (SSEN). IDX = 2 controls the PAL ID detection sensitivity (PSEN). IDX = 3 controls the weak signal detection sensitivity (WKTH). | 1A / 20 / 1C / 2A |

0xC4(CH1)/0xC5(CH2)/0xC6(CH3)/0xC7(CH4) – H monitor

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-0 | HFREF | R | Horizontal line frequency indicator(Test purpose only) | X |

0x80 – Software Reset Control Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-6 | Reserved | R | Reserved | 00b |
| 5 | AUDIORST | W | An 1 written to this bit resets the Audio portion to its default state but all register content remain unchanged. This bit is self-resetting. | 0 |
| 4 | VOUTrST | W | An 1 written to this bit resets Video data mux output logic to its default state but all register content remain unchanged. This bit is self-resetting. | 0 |
| 3 | VDEC4RST | W | An 1 written to this bit resets the Video4 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting. | 0 |
| 2 | VDEC3RST | W | An 1 written to this bit resets the Video3 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting. | 0 |
| 1 | VDEC2RST | W | An 1 written to this bit resets the Video2 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting. | 0 |
| 0 | VDEC1RST | W | An 1 written to this bit resets the Video1 Decoder portion to its default state but all register content remain unchanged. This bit is self-resetting. | 0 |

0x81 – Analog Control Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | Reserved | R | Reserved | 0 |
| 6 | IREF | R/W | 0 = Internal current reference 1. 1 = Internal current reference increase 30%. | 0 |
| 5 | VREF | R/W | 0 = Internal voltage reference. 1 = Internal voltage reference shut down. | 0 |
| 4 | Reserved | R/W | 0 = Normal operation(must be 0), 1 = AIGAINTEST | 0 |
| 3 | CLKPDN | R/W | 0 = Normal clock operation. 1 = All 4Ch Video Decoder System clock in power down mode, but the MPU INTERFACE module and output clocks (CLKP and CLKN) are still active. | 0 |
| 2 | Reserved | R/W | 0 = Normal operation(must be 0), 1 = AINSWTEST | 0 |
| 1 | YFLEN | R/W | Analog Video CH1/CH2/CH3/CH4 anti-alias filter control 1 = enable 0 = disable | 1 |
| | YSV | R/W | Analog Video CH1/CH2/CH3/CH4 Reduced power mode 1 = enable 0 = disable | 0 |

0x82 – Analog Control Register2

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | CTEST | R/W | Clamping control for debugging use.(Test purpose only) | 0 |
| 6 | YCLEN | R/W | 1 = Y channel clamp disabled(Test purpose only) 0 = Enabled. | 0 |
| 5 | CKIPOL | R/W | 27MHz clock output signal rise/fall timing. 0: change by 54MHz clock output falling edge. 1: change by 54MHz clock output rising edge. | 0 |
| 4 | Reserved | R | | 0 |
| 3 | GTEST | R/W | 1 = Test.(Test purpose only) 0 = Normal operation. | 0 |
| 2 | VLPF | R/W | Clamping filter control. | 0 |
| 1 | CKLY | R/W | Clamping current control 1. | 0 |
| 0 | CKLC | R/W | Clamping current control 2. | 0 |

0x83 – Control Register I

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | PBW | R/W | 1 = Wide Chroma BPF BW 0 = Normal Chroma BPF BW | 1 |
| 6 | DEM | R/W | Reserved | 1 |
| 5 | PALSW | R/W | 1 = PAL switch sensitivity low. 0 = PAL switch sensitivity normal. | 0 |
| 4 | SET7 | R/W | 1 = The black level is 7.5 IRE above the blank level. 0 = The black level is the same as the blank level. | 0 |
| 3 | COMB | R/W | 1 = Adaptive comb filter for NTSC and PAL(recommended). Not for SECAM. 0 = Notch filter. For SECAM. | 1 |
| 2 | HCOMP | R/W | 1 = operation mode 1. (recommended) 0 = mode 0. | 1 |
| 1 | YCOMB | R/W | 1 = Bypass Comb filter when no burst presence 0 = No bypass | 0 |
| 0 | PDLY | R/W | PAL delay line. 0 = enabled. 1 = disabled. | 0 |

0x84 – Color Killer Hysteresis Control Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7 | GMEN | R/W | Reserved. | 0 |
| 6-5 | CKHY | R/W | Color killer hysteresis. 0 – fastest 1 – fast 2 – medium 3 - slow | 00b |
| 4-0 | HSDLY | RW | Reserved for test. | 00h |

0x85 – Vertical Sharpness

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-4 | SHCOR | R/W | These bits provide coring function for the sharpness control. | 8 |
| 3 | VIN4 | R/W | Ch4 Video ADC input signal select. 0:VIN4A, 1:VIN4B | 0 |
| 2 | VIN3 | R/W | Ch3 Video ADC input signal select. 0:VIN3A, 1:VIN3B | 0 |
| 1 | VIN2 | R/W | Ch2 Video ADC input signal select. 0:VIN2A, 1:VIN2B | 0 |
| 0 | VIN1 | R/W | Ch1 Video ADC input signal select. 0:VIN1A, 1:VIN1B | 0 |

0x86 – Coring Control Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-6 | CTCOR | R/W | These bits control the coring for CTI. | 1 |
| 5-4 | CCOR | R/W | These bits control the low level coring function for the Cb/Cr output. | 0 |
| 3-2 | VCOR | R/W | These bits control the coring function of vertical peaking. | 1 |
| 1-0 | CIF | R/W | These bits control the IF compensation level. 0 = None 1 = 1.5dB 2 = 3dB 3 = 6dB | 0 |

0x87 – Clamping Gain

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-4 | CLPEND | R/W | These 4 bits set the end time of the clamping pulse. Its value should be larger than the value of CLPST. | 5 |
| 3-0 | CLPST | R/W | These 4 bits set the start time of the clamping. It is referenced to PCLAMP position. | 0 |

0x88 – Individual AGC Gain

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-4 | NMGAIN | R/W | These bits control the normal AGC loop maximum correction value. | 2 |
| 3-1 | WPGAIN | R/W | Peak AGC loop gain control. | 1 |
| 0 | Reserved | R | Reserved | 0 |

0x8A – White Peak Threshold

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-0 | PEAKWT | R/W | These bits control the white peak detection threshold. Setting 'FF' can disable this function. | D8 |

0x8B – Clamp level

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | CLMPLD | R/W | 0 = Clamping level is set by CLMPL. 1 = Clamping level preset at 60d. | 1 |
| 6-0 | CLMPL | R/W | These bits determine the clamping level of the Y channel. | 3C |

0x8C – Sync Amplitude

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7 | SYNCTD | R/W | 0 = Reference sync amplitude is set by SYNCT. 1 = Reference sync amplitude is preset to 38h. | 1 |
| 6-0 | SYNCT | R/W | These bits determine the standard sync pulse amplitude for AGC reference. | 38 |

0x8D – Sync Miss Count Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-4 | MISSCNT | R/W | These bits set the threshold for horizontal sync miss count threshold. | 4 |
| 3-0 | HSWIN | R/W | These bits determine the VCR mode detection threshold. | 4 |

0x8E – Clamp Position Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-0 | PCLAMP | R/W | These bits set the clamping position from the PLL sync edge | 38 |

0x8F – Vertical Control I

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-6 | VLCKI | R/W | Vertical lock in time. 0 = fastest 3 = slowest. | 0 |
| 5-4 | VLCKO | R/W | Vertical lock out time. 0 = fastest 3 = slowest. | 0 |
| 3 | VMODE | R/W | This bit controls the vertical detection window. 1 = search mode. 0 = vertical count down mode. | 0 |
| 2 | DETV | R/W | 1 = recommended for special application only. 0 = Normal Vsync logic | 0 |
| 1 | AFLD | R/W | Auto field generation control 0 = Off 1 = On | 0 |
| 0 | VINT | R/W | Vertical integration time control. 1 = short 0 = normal | 0 |

0x90 – Vertical Control II

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-5 | BSHT | R/W | Burst PLL center frequency control. | 0 |
| 5-0 | VSHT | R/W | Vsync output delay control in the increment of half line length. | 00 |

0x91 – Color Killer Level Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-6 | CKILMAX | R/W | These bits control the amount of color killer hysteresis. The hysteresis amount is proportional to the value. | 1 |
| 5-0 | CKILMIN | R/W | These bits control the color killer threshold. Larger value gives lower killer level. | 38 |

0x92 – Comb Filter Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7 | HTL | R/W | 0 = adaptive mode 1 = fixed comb | 0 |
| 6-4 | HTL | R/W | Adaptive Comb filter threshold control 1. | 4 |
| 3-0 | VTL | R/W | Adaptive Comb filter threshold control 2. | 4 |

0x93 – Luma Delay and H Filter Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | CKLM | R/W | Color Killer mode. 0 = normal 1 = fast (for special application) | 0 |
| 6-4 | YDLY | R/W | Luma delay fine adjustment. This 2's complement number provides -4 to +3 unit delay control. | 3 |
| 3-0 | Reserved | RW | | 0h |

0x94 – Miscellaneous Control I

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | HPLC | R/W | Reserved for internal use. | 0 |
| 6 | EVCNT | R/W | 1 = Even field counter in special mode. 0 = Normal operation | 0 |
| 5 | PALC | R/W | Reserved for future use. | 0 |
| 4 | SDET | R/W | ID detection sensitivity. A '1' is recommended. | 1 |
| 3 | TBC_EN | R/W | 1 = Internal TBC enable. Total pixel per line on Video active line is always 858x2 for NTSC/PAL-M(60Hz) and 864x2 for PAL/SECAM(50Hz). 0 = TBC off. | 0 |
| 2 | BYPASS | R/W | It controls the standard detection and should be set to '1' in normal use. | 1 |
| 1 | SYOUT | R/W | 1 = Hsync output is disabled when video loss is detected 0 = Hsync output is always enabled | 0 |
| 0 | Reserved | R | Reserved | 0 |

0x95 – LOOP Control Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-6 | HPM | R/W | Horizontal PLL acquisition time. 3 = Fast 2 = Auto1 1 = Auto2 0 = Normal | 2 |
| 5-4 | ACCT | R/W | ACC time constant 0 = No ACC 1 = slow 2 = medium 3 = fast | 2 |
| 3-2 | SPM | R/W | Burst PLL control. 0 = Slowest 1 = Slow 2 = Fast 3 = Fastest | 1 |
| 1-0 | CBW | R/W | Chroma low pass filter bandwidth control. Refer to filter curves. | 1 |

0x96 – Miscellaneous Control II

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | NKILL | R/W | 1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled. | 1 |
| 6 | PKILL | R/W | 1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled. | 1 |
| 5 | SKILL | R/W | 1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled. | 1 |
| 4 | CBAL | R/W | 0 = Normal output 1 = special output mode. | 0 |
| 3 | FCS | R/W | 1 = Force decoder output value determined by CCS. 0 = Disabled. | 0 |
| 2 | LCS | R/W | 1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled. | 0 |
| 1 | CCS | R/W | When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black. | 0 |
| 0 | BST | R/W | 1 = Enable blue stretch. 0 = Disabled. | 0 |

0x97 – CLAMP MODE

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-6 | FRM | R/W | Free run mode control 0 = Auto, 2 = default to 60Hz, 3 = default to 50Hz | 0 |
| 5-4 | YNR | R/W | Y HF noise reduction 0 = None, 1 = smallest, 2 = small, 3 = medium | 0 |
| 3-2 | CLMD | R/W | Clamping mode control. 0 = Sync top, 1 = Auto, 2 = Pedestal, 3 = N/A | 1 |
| 1-0 | PSP | R/W | Slice level control 0 = low 1 = medium 2 = high | 1 |

0x98 – HSLWCTL

| Bit | Function | R/W | Description | Reset |
|-----|--------------|-----|--------------------------------------|-------|
| 7 | Reserved | R/W | | 0 |
| 6-4 | HSBEGIN[2:0] | R/W | HSYNC Start position Control Bit2-0. | 00 |
| 3 | Reserved | R/W | | 0 |
| 2-0 | HSEND[2:0] | R/W | HSYNC End position Control Bit2-0. | 00 |

0x99 – HSBEGIN

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|---------------------------------------|-------|
| 7-0 | HSBEGIN[10:3] | R/W | HSYNC Start position Control Bit10-3. | 28 |

0x9A – HSEND

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|-------------------------------------|-------|
| 7-0 | HSEND[10:3] | R/W | HSYNC End position Control Bit10-3. | 44 |

0x9B – OVSDLY

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-0 | OVSDLY | R/W | VSYNC Start position. Control H position on VSYNC start. | 44 |

0x9C – OVSEND

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | HASYNC | R/W | 1:the length of EAV to SAV is set up and fixed by HBLEN registers. 0:the length of SAV to EAV is set up and fixed by HACTIVE registers. | 0 |
| 6-4 | OFDLY | R/W | FIELD output delay. 0h:0H line delay FIELD output.(601 mode only) 1h-6h: 1H-6H line delay FIELD output. 7h:Reserved. | 2 |
| 3 | VSMODE | R/W | 1:VSYNC output is HACTIVE-VSYNC mode. 0:VSYNC output is HSYNC-VSYNC mode. | 0 |
| 2-0 | OVSEND | R/W | Line delay for VSYNC end position. | 0 |

0x9D – HBLEN

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-0 | HBLEN | R/W | These bits are effective when HASYNC bit is set to 1.These bits set up the length of EAV to SAV code when HASYNC bit is 1.Normal value is (Total pixel per line – HACTIVE) value. NTSC/PAL-M(60Hz): 8Ah(138dec)=858-720 PAL/SECAM(50Hz): 90h(144dec)=864-720 If Reg0x0E[3](ATRIG for CH1) is set to 0,this value changes into 8Ah or 90h at auto video format detection initial time automatically according to CH1 video detection status. | 90h |

0x9E – NOVID

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|---|-------|
| 7 | Reserved | R | Reserved | 0 |
| 6 | FC27 | R/W | 1:normal ITU-R656 operation 0:Squared Pixel mode. | 1 |
| 5-4 | CHID_MD | R/W | Select the Channel ID format for time-multiplexed output 0 No channel ID (default) 1 CHID with the specific ITU-R BT.656 sync Code 2 CHID with the specific horizontal blanking code 3 CHID with the specific ITU-R BT.656 sync and horizontal blanking code | 0 |
| 3 | NOVID_656 | R/W | 0:Normal ITU-R BT.656 SA/EAV(default) 1:AN optional set of ITU-R BT.656 SAV/EAV code for No-video status | 0 |
| 2 | EAVSWAP | R/W | 1:EAV-SAV code is swapped. 0:EAV-SAV code is not swapped(standard 656 output mode) | 0 |
| 1 | VIPCFG | R/W | Set up Bit7 in 4th byte of EAV/SAV code. 1:Standard ITU-R656 code format.(It's also VIP task-A code format.) 0:Old VIP task-B code format. | 1 |
| 0 | NTSC656 | R/W | 1:Number of Even Field Video output line is (the number of Odd field Video output line – 1).This bit is required for ITU-R BT.656 output for 525 line system standard. 0: Number of Even Field Video output line is same as the number of Odd field Video output line. | 0 |

0x41 – Video Encoder Standard Control

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|---|-------|
| 7 | HZ50 | R/W | 1 = 50Hz field rate 0 = 60Hz field rate | 0 |
| 6 | INTERLACE | R/W | 1 = Interlaced output 0 = Non-interlaced output | 1 |
| 5-4 | FSCSEL | R/W | FSCSEL frequency selection 00= NTSC-M, 01= PAL-B, 10= PAL-M, 11= PAL-N | 0 |
| 3 | COFF | R/W | 1 = Turn off chroma output 0 = chroma output on | 0 |
| 2 | PHALT | R/W | 1 = Alternating burst for PAL 0 = NTSC | 0 |
| 1 | PDRST | R/W | 1 = PAL phase reset every 8 fields 0 = No phase reset | 0 |
| 0 | PED | R/W | 1 = Pedestal enabled (NTSC-M) 0 = disabled | 0 |

0x42 – Video Encoder Test Generation

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-6 | YBW | R/W | Luminance bandwidth control. 2,3 = Normal BW 1,0 = not available | 2 |
| 5-4 | CBW | R/W | Chrominance bandwidth control. Refer to filter diagram. | 1 |
| 3 | CBGEN | R/W | 1 = Enable internal test pattern generation 0 = Disabled | 0 |
| 2-0 | TCSEL | R/W | Test pattern selection. 0 = 75% color bar 1 = White 2 = Yellow 3 = Cyan 4 = Green 5 = Magenta 6 = Red 7 = Blue | 0 |

0x43 – Video Encoder Clock and Delay control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | CKMST | R/W | 1 = Use internal 27MHz clock as encoder clock.ENCLK pin is clock output. 0 = Use input clock as encoder clock.ENCLK pin is clock input. | 0 |
| 6 | CKPOL | R/W | It controls the clock polarity for latching input data | 0 |
| 5 | NONSTA | R/W | 1 = Non-standard 656 input (Internal use only) 0 = Normal 656 input | 0 |
| 4 | FRUN | R/W | 0 = Encoder timing generation bases on input 1 = Internal generated timing for built-in test pattern | 0 |
| 3-0 | YDEL | R/W | Y delay adjustment relative to Cb/Cr. The center value is 8.8h should be set up normally. | 8 |

0x44 – Video Encoder Output Control

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|---|-------|
| 7 | CVBS_YSEL | R/W | DAC1 output control 1 = Luma output 0 = CVBS output | 0 |
| 6 | CVBS_CSEL | R/W | DAC2 output control 1 = Chroma output 0 = CVBS output | 0 |
| 5-0 | TMODE | R/W | Encoder test mode. For internal use only. | 0 |

0x45 – Video Encoder SCH

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 6-0 | SCH | R/W | Sub-carrier phase control. For internal use only. | 38h |

0x46 – Video Encoder YGAIN

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-0 | YGAIN | R/W | Luminance amplitude gain control. The 0dB gain is 0x80. | 80h |

0x47 – Video Encoder CGAIN

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-0 | CGAIN | R/W | Chrominance amplitude gain control, The 0dB gain is 0x80. | 80h |

0x48 – Video Encoder SGAIN

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-0 | SGAIN | R/W | Sync pulse amplitude gain control. The 0dB gain is 0x80 | 80h |

0x49 – Video Encoder BGAIN

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-0 | BGAIN | R/W | Burst amplitude gain control. The 0dB gain is 0x80 | 80h |

0x4A – Video DAC control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--------------------------|-------|
| 7-4 | VDAIREFC | R/W | C Video DAC IREF control | F |
| 3-0 | VDAIREFY | R/W | Y Video DAC IREF control | F |

0x4B – Video DAC control

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|---|-------|
| 7 | ENCVDOUT | R/W | Test purpose only. | 0 |
| 6 | TESTDAC | R/W | Test purpose only. | 0 |
| 5 | VDA_PDC | R/W | 1:C Video DAC power down mode,0:normal mode | 1 |
| 4 | VDA_PDY | R/W | 1:Y Video DAC power down mode,0:normal mode. | 1 |
| 3 | VDACCKPOL | R/W | 1:Analog Video DAC input clock polarity inverse: 0:not inverse. | 0 |
| 2 | ENC_LOOP | R/W | Video Decoder to Video Encoder loop test mode. 1:Video Decoder output direct connect to Video Encoder input for Test purpose only.LOOP_CH register select Video Ch number to be connected to Video Encoder in this mode.This function is internal test use only. 0:Normal Video Decoder and Video Encoder operation. Video Decoder and Video Encoder are working independently. | 0 |
| 1-0 | LOOP_CH | R/W | Select Video Ch number to be connected to Video Encoder directly when ENC_LOOP register is set to 1. 0: Ch1 Video Data. 1: Ch2 Video Data 2: Ch3 Video Data. 3. Ch4 Video Data. | 0 |

0x4C – Video Encoder Vdelay

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-5 | Reserved | R | | 0 |
| 4-0 | EVDELAY | R/W | Video Encoder output Vertical position control. | 0 |

0x4D – Video Encoder Hdelay

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-5 | Reserved | R | | 0 |
| 4-0 | EHDELAY | R/W | Video Encoder output Horizontal position control. | 0 |

0x9F(CH1)/0x67(CH2)/0x68(CH3)/0x69(CH4) – Clock Output Delay Control Register

| Index | Bit | Function | R/W | Description | Reset |
|---|-----|------------|-----|---|-------|
| 0x9F | 7-4 | CLKNO1_DEL | R/W | Control the clock delay of CLKNO _n pin. 0h/1h/3h/7h/Fh values are effective. 1h: about 2ns more delay, 3h: about 4ns more delay, 7h: about 6ns more delay, Fh: about 7ns more delay | 0h |
| 0x67 | | CLKNO2_DEL | RW | | |
| 0x68 | | CLKNO3_DEL | R/W | | |
| 0x69 | | CLKNO4_DEL | RW | | |
| 0x9F | 3-0 | CLKPO1_DEL | R/W | Control the clock delay of CLKPO _n pin. 0h/1h/3h/7h/Fh values are effective. 1h: about 2ns more delay, 3h: about 4ns more delay, 7h: about 6ns more delay, Fh: about 7ns more delay | 0h |
| 0x67 | | CLKPO2_DEL | R/W | | |
| 0x68 | | CLKPO3_DEL | R/W | | |
| 0x69 | | CLKPO4_DEL | R/W | | |
| <p>*) CLKNO_n_POL/CLKPO_n_POL controls have more better and easy clock margin adjustment. Use CLKNO_n_POL/CLKPO_n_POL at first normally, especially for 27MHz/54MHz data output application. CLKNO_n_DEL/CLKPO_n_DEL are sometimes required for 108MHz data output interface. CLKNO_n_DEL/CLKPO_n_DEL are not required for 27MHz/54MHz data output in most cases.</p> | | | | | |

0xA8 ~0xA9 – Horizontal Scaler Pre-filter Control Register**0xA8 – Horizontal Scaler Pre-filter Control Register**

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-4 | HFLT2 | R/W | Pre-filter selection for Video CH1/CH2 horizontal scaler. If HSCALE[11:8]=1,HFLT [3:0] controls the peaking function. If HSCALE[11:8]>1,HFLT [2:0] function is bellow. 1** = Bypass | 0h |
| 3-0 | HFLT1 | R/W | 000 = Auto selection based on Horizontal scaling ratio. 001 = Recommended for CIF size image. 010 = Recommended for QCIF size image. 011 = Recommended for ICON size image. | 0h |

0xA9 – Horizontal Scaler Pre-filter Control Register

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-4 | HFLT4 | R/W | Pre-filter selection for Video CH3/CH4 horizontal scaler. If HSCALE[11:8]=1,HFLT [3:0] controls the peaking function. If HSCALE[11:8]>1,HFLT [2:0] function is bellow. 1** = Bypass | 0h |
| 3-0 | HFLT3 | R/W | 000 = Auto selection based on Horizontal scaling ratio. 001 = Recommended for CIF size image. 010 = Recommended for QCIF size image. 011 = Recommended for ICON size image. | 0h |

Video AGC Control**0xAA – Video AGC Control**

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|---|-------|
| 7 | AGCEN4 | R/W | Select Video AGC loop function on VIN4 0: AGC loop function enabled.(recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN4 | 0 |
| 6 | AGCEN3 | R/W | Select Video AGC loop function on VIN3 0: AGC loop function enabled.(recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN3 | 0 |
| 5 | AGCEN2 | R/W | Select Video AGC loop function on VIN2 0: AGC loop function enabled.(recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN2 | 0 |
| 4 | AGCEN1 | R/W | Select Video AGC loop function on VIN1 0: AGC loop function enabled.(recommended for most application cases) 1: AGC loop function disabled. Gain is set by AGCGAIN1 | 0 |
| 3 | AGCGAIN4[8] | R/W | AGCGAIN4 MSB bit | 0 |
| 2 | AGCGAIN3[8] | R/W | AGCGAIN3 MSB bit | 0 |
| 1 | AGCGAIN2[8] | R/W | AGCGAIN2 MSB bit | 0 |
| 0 | AGCGAIN1[8] | R/W | AGCGAIN1 MSB bit | 0 |

0xAB – Video AGC Control

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|--|-------|
| 7-0 | AGCGAIN1[7:0] | R/W | To control the AGC Gain when AGC loop is disabled. AGCGAIN1 bit7-0. | F0h |

0xAC – Video AGC Control

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|--|-------|
| 7-0 | AGCGAIN2[7:0] | R/W | To control the AGC Gain when AGC loop is disabled. AGCGAIN2 bit7-0. | F0h |

0xAD – Video AGC Control

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|--|-------|
| 7-0 | AGCGAIN3[7:0] | R/W | To control the AGC Gain when AGC loop is disabled. AGCGAIN3 bit7-0. | F0h |

0xAE – Video AGC Control

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|---|-------|
| 7-0 | AGCGAIN4[7:0] | R/W | To control the AGC Gain when AGC loop is disabled. AGC GAIN4 bit7-0. | F0h |

0xAF – Vertical Peaking Level Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7 | Reserved | R | | 0 |
| 6-4 | VSHP2 | R/W | Select CH2 Video Vertical peaking level. (*) 0 : none. 7 : highest | 0 |
| 3 | Reserved | R | | 0 |
| 2-0 | VSHP1 | R/W | Select CH1 Video Vertical peaking level. (*) 0 : none. 7 : highest | 0 |

*Note: VSHP must be set to '0' if Reg0x83 COMB = 0.

0xB0 – Vertical Peaking Level Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7 | Reserved | R | | 0 |
| 6-4 | VSHP4 | R/W | Select CH4 Video Vertical peaking level. (*) 0 : none. 7 : highest | 0 |
| 3 | Reserved | R | | 0 |
| 2-0 | VSHP3 | R/W | Select CH3 Video Vertical peaking level. (*) 0 : none. 7 : highest | 0 |

*Note: VSHP must be set to '0' if Reg0x83 COMB = 0.

0xB1 – NOVIDMODE

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|---|-------|
| 7 | CH8IDEN | R/W | Video Channel ID number have following value in Sync Code and Horizontal Blanking Code. 0: 4 channel ID Only output VIN1A/VIN1B : 0h VIN2A/VIN2B : 1h VIN3A/VIN3B : 2h VIN4A/VIN4B: 3h 1: 8 channel ID output VIN1A : 0h VIN2A : 1h VIN3A : 2h VIN4A : 3h VIN1B : 4h VIN2B : 5h VIN3B : 6h VIN4B : 7h | 0 |
| 6 | Reserved | R | | 1 |
| 5-4 | NOVIDMODE | R/W | Select NOVID_656 output mode status.When NOVID_656 is set to 1, NOVID_656 code is being output when following status is active in Video Decoding logic. 0 : Video lost (vdloss). 1 : No Video (novideo). 2 : Video lost or No video(vdloss or novideo) 3 : NOVID_656 code is not being output at anytime. | 0h |
| 3-0 | Reserved | R | | Ah |

Audio ADC Digital Input Offset Control**0xB3 – Audio ADC Digital Input Offset Control**

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|---|-------|
| 7-6 | AADC4OFS[9:8] | R/W | Ch4 Digital ADC input data offset control bit9-8. | 0h |
| 5-4 | AADC3OFS[9:8] | R/W | Ch3 Digital ADC input data offset control bit9-8. | 0h |
| 3-2 | AADC2OFS[9:8] | R/W | Ch2 Digital ADC input data offset control bit9-8. | 0h |
| 1-0 | AADC1OFS[9:8] | R/W | Ch1 Digital ADC input data offset control bit9-8. | 0h |

Digital ADC input data offset control. Digital ADC input data is adjusted by

$$ADJAADCn = AUDnADC + AADCnOFS.$$

AUDnADC is 2's formatted Analog Audio ADC output.
AADCnOFS is adjusted offset value by 2's format.

0xB4 – Audio ADC Digital Input Offset Control

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|---|-------|
| 7-0 | AADC1OFS[7:0] | R/W | Ch1 Digital ADC input data offset control bit7-0. | 0h |

0xB5 – Audio ADC Digital Input Offset Control

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|---|-------|
| 7-0 | AADC2OFS[7:0] | R/W | Ch2 Digital ADC input data offset control bit7-0. | 0h |

0xB6 – Audio ADC Digital Input Offset Control

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|---|-------|
| 7-0 | AADC3OFS[7:0] | R/W | Ch3 Digital ADC input data offset control bit7-0. | 0h |

0xB7 – Audio ADC Digital Input Offset Control

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|---|-------|
| 7-0 | AADC4OFS[7:0] | R/W | Ch4 Digital ADC input data offset control bit7-0. | 0h |

0x75 – Audio ADC Digital Input Offset Control

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|---|-------|
| 7-2 | Reserved | R | | 0h |
| 1-0 | AADC5OFS[9:8] | R/W | Ch5 Digital ADC input data offset control bit9-8. | 0h |

Digital ADC input data offset control. Digital ADC input data is adjusted by

$$ADJAADCn = AUDnADC + AADCnOFS.$$

AUDnADC is 2's formatted Analog Audio ADC output.

AADCnOFS is adjusted offset value by 2's format.

0x76 – Audio ADC Digital Input Offset Control

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|---|-------|
| 7-0 | AADC5OFS[7:0] | R/W | Ch5 Digital ADC input data offset control bit7-0. | 0h |

Analog Audio ADC Digital Output Value**0xB8 – Analog Audio ADC Digital Output Value**

| Bit | Function | R/W | Description | Reset |
|-----|--------------|-----|--|-------|
| 7-6 | AUD4ADC[9:8] | R | Bit9-8 of Ch4 Analog Audio ADC Digital Output Value by 2's format. | X |
| 5-4 | AUD3ADC[9:8] | R | Bit9-8 of Ch3 Analog Audio ADC Digital Output Value by 2's format. | X |
| 3-2 | AUD2ADC[9:8] | R | Bit9-8 of Ch2 Analog Audio ADC Digital Output Value by 2's format. | X |
| 1-0 | AUD1ADC[9:8] | R | Bit9-8 of Ch1 Analog Audio ADC Digital Output Value by 2's format. | X |

0xB9 – Analog Audio ADC Digital Output Value

| Bit | Function | R/W | Description | Reset |
|-----|--------------|-----|--|-------|
| 7-0 | AUD1ADC[7:0] | R | Bit7-0 of Ch1 Analog Audio ADC Digital Output Value by 2's format. | X |

0xBA – Analog Audio ADC Digital Output Value

| Bit | Function | R/W | Description | Reset |
|-----|--------------|-----|--|-------|
| 7-0 | AUD2ADC[7:0] | R | Bit7-0 of Ch2 Analog Audio ADC Digital Output Value by 2's format. | X |

0xBB – Analog Audio ADC Digital Output Value

| Bit | Function | R/W | Description | Reset |
|-----|--------------|-----|---|-------|
| 7-0 | AUD3ADC[7:0] | R | Bit7-0 of Ch3 Analog Audio ADC Digital Output Value by 2's format.. | X |

0xBC – Analog Audio ADC Digital Output Value

| Bit | Function | R/W | Description | Reset |
|-----|--------------|-----|--|-------|
| 7-0 | AUD4ADC[7:0] | R | Bit7-0 of Ch4 Analog Audio ADC Digital Output Value by 2's format. | X |

0x77 – Analog Audio ADC Digital Output Value

| Bit | Function | R/W | Description | Reset |
|-----|--------------|-----|--|-------|
| 7-2 | Reserved | | Reserved | 00h |
| 1-0 | AUD5ADC[9:8] | R | Bit9-8 of Ch5 Analog Audio ADC Digital Output Value by 2's format. | X |

0x78 – Analog Audio ADC Digital Output Value

| Bit | Function | R/W | Description | Reset |
|-----|--------------|-----|--|-------|
| 7-0 | AUD5ADC[7:0] | R | Bit7-0 of Ch5 Analog Audio ADC Digital Output Value by 2's format. | X |

Adjusted Analog Audio ADC Digital Input Value**0xBD – Adjusted Analog Audio ADC Digital Input Value**

| Bit | Function | R/W | Description | Reset |
|--|---------------|-----|--|-------|
| 7-6 | ADJAADC4[9:8] | R | Bit9-8 of Ch4 adjusted Audio ADC Digital Input Data Value by 2's format. | X |
| 5-4 | ADJAADC3[9:8] | R | Bit9-8 of Ch3 adjusted Audio ADC Digital Input Data Value by 2's format. | X |
| 3-2 | ADJAADC2[9:8] | R | Bit9-8 of Ch2 adjusted Audio ADC Digital Input Data Value by 2's format. | X |
| 1-0 | ADJAADC1[9:8] | R | Bit9-8 of Ch1 adjusted Audio ADC Digital Input Data Value by 2's format. | X |
| The value shows the first input data in front of Digital Audio Decimation Filtering process. | | | | |

0xBE – Adjusted Analog Audio ADC Digital Input Value

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|--|-------|
| 7-0 | ADJAADC1[7:0] | R | Bit7-0 of Ch1 adjusted Audio ADC Digital Input Data Value by 2's format. | X |

0xBF – Adjusted Analog Audio ADC Digital Input Value

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|--|-------|
| 7-0 | ADJAADC2[7:0] | R | Bit7-0 of Ch2 adjusted Audio ADC Digital Input Data Value by 2's format. | X |

0xC0 – Adjusted Analog Audio ADC Digital Input Value

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|--|-------|
| 7-0 | ADJAADC3[7:0] | R | Bit7-0 of Ch3 adjusted Audio ADC Digital Input Data Value by 2's format. | X |

0xC1 – Adjusted Analog Audio ADC Digital Input Value

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|--|-------|
| 7-0 | ADJAADC4[7:0] | R | Bit7-0 of Ch4 adjusted Audio ADC Digital Input Data Value by 2's format. | X |

0x79 – Adjusted Analog Audio ADC Digital Input Value

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|--|-------|
| 7-2 | | | Reserved | 00h |
| 1-0 | ADJAADC5[9:8] | R | Bit9-8 of Ch5 adjusted Audio ADC Digital Input Data Value by 2's format. | X |

0x7A – Adjusted Analog Audio ADC Digital Input Value

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|--|-------|
| 7-0 | ADJAADC5[7:0] | R | Bit7-0 of Ch5 adjusted Audio ADC Digital Input Data Value by 2's format. | X |

MPP Pin Output Mode Control**0xC8 – MPP Pin Output Mode Control**

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|---|-------|
| 7 | GPP_VAL2 | R/W | Select the general purpose value through the MPP2 pin for Ch2. 0 : "0" vaule, 1: "1" value | 0h |
| 6-4 | MPP_MODE2 | R/W | Select the output mode for MPP2 pin. Followings show the status when POLMPP2 register is set to 0. If POLMPP2 register is set to 1, following values have inversed status. 0:Horizontal sync output.Low is H-sync active. 1:Vertical sync output.Low is V-sync active. 2:Field flag output.Low is field1(Odd),High is field2 (Even). 3:Horizontal active signal output.High is H-active. 4:Vertical active and horizontal active signal output.High is VH-active. 5:No video flag.High is No-video,Low is Video. 6:Digital serial audio mixing data same as ADATM pin 7:GPP_VAL.Same as GPP_VAL2 register value. If VDLOSSOE register is set to "1", vdloss2 signal is output to MPP2 pin and these MPP_MODE2 function is not effective. | 0h |
| 3 | GPP_VAL1 | R/W | Select the general purpose value through the MPP1 pin for Ch1. 0 : "0" vaule, 1: "1" value | 0h |
| 2-0 | MPP_MODE1 | R/W | Select the output mode for MPP1 pin. Followings show the status when POLMPP1 register is set to 0. If POLMPP1 register is set to 1, following values have inversed status. 0:Horizontal sync output.Low is H-sync active. 1:Vertical sync output.Low is V-sync active. 2:Field flag output.Low is field1(Odd),High is field2(Even). 3:Horizontal active signal output.High is H-active. 4:Vertical active and horizontal active signal output.High is VH-active. 5:No video flag.High is No-video,Low is Video. 6:Digital serial audio mixing data same as ADATM pin 7:GPP_VAL.Same as GPP_VAL1 register value. If VDLOSSOE register is set to "1", vdloss1 signal is output to MPP1 pin and these MPP_MODE1 function is not effective. | 0h |

0xC9 – MPP Pin Output Mode Control

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|--|-------|
| 7 | GPP_VAL4 | R/W | Select the general purpose value through the MPP4 pin for Ch4. 0 : "0" vaule, 1: "1" value | 0h |
| 6-4 | MPP_MODE4 | R/W | Select the output mode for MPP4 pin. Followings show the status when POLMPP4 register is set to 0. If POLMPP4 register is set to 1, following values have inversed status. 0:Horizontal sync output.Low is H-sync active. 1:Vertical sync output.Low is V-sync active. 2:Field flag output.Low is field1(Odd),High is field2(Even). 3:Horizontal active signal output.High is H-active. 4:Vertical active and horizontal active signal output.High is VH-active. 5:No video flag.High is No-video,Low is Video. 6:Digital serial audio mixing data same as ADATM pin 7:GPP_VAL.Same as GPP_VAL4 register value. If VDLOSSOE register is set to "1", vdloss4 signal is output to MPP4 pin and these MPP_MODE4 function is not effective. | 0h |
| 3 | GPP_VAL3 | R/W | Select the general purpose value through the MPP3 pin for Ch3. 0 : "0" vaule, 1: "1" value | 0h |
| 2-0 | MPP_MODE3 | R/W | Select the output mode for MPP3 pin. Followings show the status when POLMPP3 register is set to 0. If each POLMPP3 register is set to 1, following values have inversed status. 0:Horizontal sync output.Low is H-sync active. 1:Vertical sync output.Low is V-sync active. 2:Field flag output.Low is field1(Odd),High is field2(Even). 3:Horizontal active signal output.High is H-active. 4:Vertical active and horizontal active signal output.High is VH-active. 5:No video flag.High is No-video,Low is Video. 6:Digital serial audio mixing data same as ADATM pin 7:GPP_VAL.Same as GPP_VAL3 register value. If VDLOSSOE register is set to "1", vdloss3 signal is output to MPP3 pin and these MPP_MODE3 function is not effective. | 0h |

0xCA – Video Channel Output Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-6 | CHMD4 | R/W | Select video bus output mode on 8bit VD4[7:0] pin. 0: Single Channel ITU-R BT.656 format output. 1: Two Channel ITU-R BT.656 Time-multiplexed format output. 2: Four Channel ITU-R BT.656 Time-multiplexed format output. | 0h |
| 5-4 | CHMD3 | R/W | Select video bus output mode on 8bit VD3[7:0] pin. 0: Single Channel ITU-R BT.656 format output. 1: Two Channel ITU-R BT.656 Time-multiplexed format output. 2: Four Channel ITU-R BT.656 Time-multiplexed format output. | 0h |
| 3-2 | CHMD2 | R/W | Select video bus output mode on 8bit VD2[7:0] pin. 0: Single Channel ITU-R BT.656 format output. 1: Two Channel ITU-R BT.656 Time-multiplexed format output. 2: Four Channel ITU-R BT.656 Time-multiplexed format output. | 0h |
| 1-0 | CHMD1 | R/W | Select video bus output mode on 8bit VD1[7:0] pin. 0: Single Channel ITU-R BT.656 format output. 1: Two Channel ITU-R BT.656 Time-multiplexed format output. 2: Four Channel ITU-R BT.656 Time-multiplexed format output. | 0h |

0xCB – Four Channel CIF Time-multiplexed Format

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | POLMPP4 | R/W | Select MPP4 pin output polarity. 0: normal, 1: inverse polarity. | 0 |
| 6 | POLMPP3 | R/W | Select MPP3 pin output polarity. 0: normal, 1: inverse polarity. | 0 |
| 5 | POLMPP2 | R/W | Select MPP2 pin output polarity. 0: normal, 1: inverse polarity. | 0 |
| 4 | POLMPP1 | R/W | Select MPP1 pin output polarity. 0: normal, 1: inverse polarity. | 0 |
| 3 | CIF_54M4 | R/W | Enable four channel CIF time-multiplexed format with 54MHz for CH4. * 1: Output this Four channel CIF time-multiplexed format on VD4[7:0] with 54MHz. | 0 |
| 2 | CIF_54M3 | R/W | Enable four channel CIF time-multiplexed format with 54MHz for CH3.* 1: Output this Four channel CIF time-multiplexed format on VD3[7:0] with 54MHz. | 0 |
| 1 | CIF_54M2 | R/W | Enable four channel CIF time-multiplexed format with 54MHz for CH2. * 1: Output this Four channel CIF time-multiplexed format on VD2[7:0] with 54MHz. | 0 |
| 0 | CIF_54M1 | R/W | Enable four channel CIF time-multiplexed format with 54MHz for CH1. * 1: Output this Four channel CIF time-multiplexed format on VD1[7:0] with 54MHz. | 0 |

*** Note :**

Enable four channel CIF time-multiplexed format with 54MHz

CIF_54M1~4 stands for CH1 to CH4.

When CHMD4/CHMD3/CHMD2/CHMD1 registers have 0h or 1h, this function is effective on all Video ports.

When CHMD4/CHMD3/CHMD2/CHMD1 registers have 2h value, all video ports are always four channel D1 Time-division-multiplexed Format with 108MHz.

0 : output format is controlled by CHMD4/CHMD3/CHMD2/CHMD1 registers and it's not four channel CIF time-multiplexed format with 54MHz.(default)

1 : Four channel CIF time-multiplexed format with 54MHz

0xCC – 2nd Channel Selection

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-6 | SELCH4 | R/W | Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD4 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output | 0h |
| 5-4 | SELCH3 | R/W | Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD3 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output | 3h |
| 3-2 | SELCH2 | R/W | Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD2 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output | 2h |
| 1-0 | SELCH1 | R/W | Select 2nd video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD1 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output | 1h |

0xCD – 1st Channel Selection

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-6 | MAINCH4 | R/W | Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD4 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output | 3h |
| 5-4 | MAINCH3 | R/W | Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD3 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output | 2h |
| 3-2 | MAINCH2 | R/W | Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD2 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output | 1h |
| 1-0 | MAINCH1 | R/W | Select 1st video output channel on Two Channel ITU-R BT.656 Time-multiplexed Format on VD1 pin 0: CH1 video output 1: CH2 video output 2: CH3 video output 3: CH4 video output | 0h |

0xCE – Analog Power Down Control

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|--|-------|
| 7 | AAUTOMUTE | R/W | 1: When input Analog data is less than ADET_TH level, output PCM data will be 0x0000(0x00). Audio DAC data input is 0x200. 0: No effect | 0 |
| 6 | Reserved | R | Reserved | 0 |
| 5 | A_DAC_PWDN | R/W | Power down the audio DAC. 0: Normal operation 1: Power down | 0 |
| 4 | A_ADC_PWDN | R/W | Power down the audio ADC. 0: Normal operation 1: Power down | 0 |
| 3-0 | V_ADC_PWDN | R/W | Power down the video ADC. V_ADC_PWDN[3:0] stands for CH4 to CH1. 0: Normal operation 1: Power down | 0h |

0xCF – Serial Mode Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-6 | SMD | R/W | Set up cascade Audio Serial mode. When SMD=2hex or 3hex, ALINKO pin output cascaded audio serial data. When SMD=0hex, ALINKO pin output is tri-state. 00: No Serial mode. ALINKO pin is tri-state output. 10: ALINKO pin is Serial out pin. ALINKI pin is Serial input pin. | 0h |
| 5-4 | VRSTEL | R/W | Select VRST(V reset) signal on ACKG (Audio Clock Generator) refin input . 0 Ch1 VRST 1 Ch2 VRST 2 Ch3 VRST 3 Ch4 VRST | 0h |
| 3-0 | Reserved | R | | 0 |

0xD0, 0xD1, 0x7F - Analog Audio Input Gain

| Index | Bit | Function | R/W | Description | Reset | | | | | |
|-------|-----|-----------|-----|---|---|---------|-----|---------|-----|-----|
| 0xD0 | 7-4 | AIGAIN2 | R/W | Select the amplifier's gain for each analog audio input AIN1 ~ AIN5. 0 0.25 1 0.31 2 0.38 3 0.44 4 0.50 5 0.63 6 0.75 7 0.88 8 1.00 (default) 9 1.25 10 1.50 11 1.75 12 2.00 13 2.25 14 2.50 15 2.75 TW2866 : Typical recommended value is AIGAIN=8. | 8h | | | | | |
| 0xD1 | | | | | | AIGAIN4 | R/W | | | |
| 0x7F | | | | | | | | AIGAIN5 | R/W | |
| | | 0xD0 | 3-0 | | AIGAIN1 | | | | | R/W |
| | | 0xD1 | | | | | | | | |
| 0x7F | | MIXRATIO5 | R/W | | Audio input AIN5 ratio value for audio mixing | 0h | | | | |

0xD2 – Number of Audio to be Recorded

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7 | M_RLSWAP | R/W | Define the sequence of mixing and playback audio data on the ADATM pin. If RM_SYNC=0 : I2S format, 0:Mixing audio on position 0 and playback audio on position 8 1:Playback audio on position 0 and mixing audio on position 8 If RM_SYNC=1 : DSP format, 0:Mixing audio on position 0 and playback audio on position 1 1:Playback audio on position 0 and mixing audio on position 1 | 0 |
| 6 | RM_SYNC | R/W | Define the digital serial audio data format for record and mixing audio on the ACLKR, ASYNR, ADATR and ADATM pin. 0 I2S format 1 DSP format | 0 |
| 5-4 | RM_PBSEL | R/W | Select the output PlayBackIn data for the ADATM pin. 0 First Stage PalyBackIn audio 1 Second Stage PalyBackIn audio 2 Third Stage PalyBackIn audio 3 Last Stage PalyBackIn audio | 0h |
| 3-2 | R_ADATM | R/W | Select the output mode for the ADATM pin. 0:Digital serial data of mixing audio 1:Digital serial data of ADATR format record audio 2:Digital serial data of ADATM format record audio | 0h |
| 1-0 | R_MULTCH | R/W | Define the number of audio for record on the ADATR pin. 0 2 audios 1 4 audios 2 8 audios 3 16 audios Number of output data is limited as shown on Sequence of Multi-channel Audio Record table. Also, each output position data are selected by R_SEQ_0/R_SEQ_1/.../R_SEQ_F registers. | 0h |

0xD3, 0xD4, 0xD5, 0xD6, 0xD7, 0xD8, 0xD9, 0xDA – Sequence of Audio to be Recorded

| Index | Bit | Function | R/W | Description | Reset |
|-------|-----|----------|-----|---|-------|
| 0xD3 | 7-4 | R_SEQ1 | R/W | Define the sequence of record audio on the ADATR pin. Refer to the Fig21 and Table7 for the detail of the R_SEQ_0 ~ R_SEQ_F. The default value of R_SEQ_0 is "0", R_SEQ_1 is "1", and R_SEQ_F is "F". | 1h |
| | 3-0 | R_SEQ0 | R/W | | 0h |
| 0xD4 | 7-4 | R_SEQ3 | R/W | | 3h |
| | 3-0 | R_SEQ2 | R/W | | 2h |
| 0xD5 | 7-4 | R_SEQ5 | R/W | 0 AIN1 1 AIN2 2 AIN3 : : : : 14 AIN15 15 AIN16 | 5h |
| | 3-0 | R_SEQ4 | R/W | | 4h |
| 0xD6 | 7-4 | R_SEQ7 | R/W | | 7h |
| | 3-0 | R_SEQ6 | R/W | | 6h |
| 0xD7 | 7-4 | R_SEQ9 | R/W | | 9h |
| | 3-0 | R_SEQ8 | R/W | | 8h |
| 0xD8 | 7-4 | R_SEQB | R/W | | Bh |
| | 3-0 | R_SEQA | R/W | | Ah |
| 0xD9 | 7-4 | R_SEQD | R/W | | Dh |
| | 3-0 | R_SEQC | R/W | | Ch |
| 0xDA | 7-4 | R_SEQF | R/W | | Fh |
| | 3-0 | R_SEQE | R/W | | Eh |

0xDB –Master Control

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|---|-------|
| 7 | ADACEN | R/W | Audio DAC Function mode 0:Audio DAC function disable(test purpose only) 1:Audio DAC function enable | 1 |
| 6 | AADCEN | R/W | Audio ADC Function mode 0:Audio ADC function disable(test purpose only) 1:Audio ADC function enable | 1 |
| 5 | PB_MASTER | R/W | Define the operation mode of the ACLKP and ASYNP pin for playback. 0:All type I2S/DSP Slave mode(ACLKP and ASYNP is input) 1:TW2866 type I2S/DSP Master mode (ACLKP and ASYNP is output) | 0 |
| 4 | PB_LRSEL | R/W | Select audio data to be used for playback input. If PB_SYNC=0 I2S format, 0: 1st Left channel audio data(default), 1: 1st Right channel audio data. If PB_SYNC=1 DSP format, 0: 1st input audio data. 1: 2nd input audio data | 0 |
| 3 | PB_SYNC | R/W | Define the digital serial audio data format for playback audio on the ACLKP, ASYNP and ADATP pin. 0:I2S format 1:DSP format | 0 |
| 2 | RM_8BIT | R/W | Define output data format per one word unit on ADATR pin. 0:16bit one word unit output 1:8bit one word unit packed output | 0 |
| 1 | ASYNROEN | R/W | Define input/output mode on the ASYNR pin. 1:ASYNR pin is input 0:ASYNR pin is output | 1 |
| 0 | ACLKRMASER | R/W | Define input/output mode on the ACLKR pin and set up audio system processing. 0:ACLKR pin is input.External 256xfs or 320fs or 384xfs clock should be connected to ACLKR pin by AIN5MD/AFS384 setting. 1:ACLKR pin is output. Internal ACKG generates audio system clock. | 0 |

u-Law/A-Law Output and Mix Mute Control**0xDC –u-Law/A-Law Output and Mix Mute Control**

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|---|-------|
| 7-6 | LAWMD | R/W | Select u-Law/A-Law/PCM/SB data output format on ADATR and ADATM pin. 0:PCM output 1:SB(Signed MSB bit in PCM data is inverted) output 2:u-Law output 3:A-Law output | 0 |
| 5 | MIX_DERATIO | R/W | Disable the mixing ratio value for all audio. 0:Apply individual mixing ratio value for each audio 1:Apply nominal value for all audio commonly | 0 |
| 4-0 | MIX_MUTE | R/W | Enable the mute function for each audio. It effects only for mixing. MIX_MUTE[0] : Audio input AIN1. MIX_MUTE[1] : Audio input AIN2. MIX_MUTE[2] : Audio input AIN3. MIX_MUTE[3] : Audio input AIN4. MIX_MUTE[4] : Playback audio input. 0:Normal 1:Muted. | 00h |

0x7E – MIX_MUTE_A5

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|---|-------|
| 7 | A5OUTOFF | R/W | AIN5 data output control on ADATR record signal. 0: output AIN51/AIN52/AIN53/AIN54 record data on ADATR. 1: not output AIN51/AIN52/AIN53/AIN54 record data on ADATR. | 1 |
| 6 | ADATM_I2SOEN | R/W | Define ADATM pin output 2 word data to make standard I2S output. 0:Mixing Data or Playback Input data are only output on ADATM pin by M_RLSWAP register.(default) 1:L/R data on ADATM pin is selected by I2SO_RSEL / I2SO_LSEL registers. | 0 |
| 5 | MIX_MUTE_A5 | R/W | MIX_MUTE_A5: Audio input AIN5 mute function control. 0:Normal 1:Muted | 1 |
| 4-0 | ADET_TH5[4:0] | R/W | AIN5 threshold value for audio detection | 03h |

Mix Ratio Value**0x72 – Mix Ratio Value**

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|---|-------|
| 7 | MRATIOMD* | R/W | Audio Mixing ratio value divider control 0: MIX_RATIO default value 1: MIX_RATIO / 64 | 0 |
| 6-0 | Reserved | R | | 00h |

If MRATIOMD=0(default) :

Mix Ratio Value

| | |
|----|--|
| 0 | 0.25 (default) Recommended for most cases. |
| 1 | 0.31 |
| 2 | 0.38 |
| 3 | 0.44 |
| 4 | 0.50 |
| 5 | 0.63 |
| 6 | 0.75 |
| 7 | 0.88 |
| 8 | 1.00 |
| 9 | 1.25 |
| 10 | 1.50 |
| 11 | 1.75 |
| 12 | 2.00 |
| 13 | 2.25 |
| 14 | 2.50 |
| 15 | 2.75 |

If MRATIOMD=1, Mixing ratio is MIX_RATIO_n / 64.

0xDD – Mix Ratio Value

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|---|-------|
| 7-4 | MIX_RATIO2 | R/W | Audio input AIN2 ratio value for audio mixing | 0 |
| 3-0 | MIX_RATIO1 | R/W | Audio input AIN1 ratio value for audio mixing | 0 |

0xDE – Mix Ratio Value

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|---|-------|
| 7-4 | MIX_RATIO4 | R/W | Audio input AIN4 ratio value for audio mixing | 0 |

| | | | | |
|-----|------------|-----|---|---|
| 3-0 | MIX_RATIO3 | R/W | Audio input AIN3 ratio value for audio mixing | 0 |
|-----|------------|-----|---|---|

0xDF – Analog Audio Output Gain

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|--|-------|
| 7-4 | Reserved | R | | 8h |
| 3-0 | MIX_RATIO3 | R/W | Playback audio input ratio value for audio mixing. | 0 |

0xE0 – Mix Output Selection

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|---|-------|
| 7 | VADCCCKPOL | R/W | Test purpose only. | 0 |
| 6 | AADCCCKPOL | R/W | 1:Analog Audio ADC input clock polarity inverse 0:not inverse. | 0 |
| 5 | ADACCKPOL | R/W | Test purpose only. | 0 |

| | | | | |
|-----|------------|-----|---|-----|
| 4-0 | MIX_OUTSEL | R/W | Define the final audio output for analog and digital mixing out. 0 Select record audio of channel 1 1 Select record audio of channel 2 2 Select record audio of channel 3 3 Select record audio of channel 4 4 Select record audio of channel 5 5 Select record audio of channel 6 6 Select record audio of channel 7 7 Select record audio of channel 8 8 Select record audio of channel 9 9 Select record audio of channel 10 10(Ah) Select record audio of channel 11 11(Bh) Select record audio of channel 12 12(Ch) Select record audio of channel 13 13(Dh) Select record audio of channel 14 14(Eh) Select record audio of channel 15 15(Fh) Select record audio of channel 16 16(10h) Select playback audio of the first stage chip 17(11h) Select playback audio of the second stage chip 18(12h) Select playback audio of the third stage chip 19(13h) Select playback audio of the last stage chip 20(14h) Select mixed audio (default) 21(15h) Select record audio of channel AIN51 22(16h) Select record audio of channel AIN52 23(17h) Select record audio of channel AIN53 24(18h) Select record audio of channel AIN54 Others no sound. | 1Fh |
|-----|------------|-----|---|-----|

Audio Detection Period and Audio Detection Threshold**0xE1 – Audio Detection Period and Audio Detection Threshold**

| Bit | Function | R/W | Description | Reset |
|-----|--------------|-----|--|-------|
| 7 | AAMPMD | R/W | Define the audio detection method. 0: Detect audio if absolute amplitude is greater than threshold 1: Detect audio if differential amplitude is greater than threshold | 1 |
| 6-4 | ADET_FILT | R/W | Select the filter for audio detection 0: Wide LPF 7: Narrow LPF | 7 |
| 3 | ADET_TH4[4]* | R/W | MSB bit of AIN4 threshold value for audio detection. | 0 |
| 2 | ADET_TH3[4]* | R/W | MSB bit of AIN3 threshold value for audio detection. | 0 |
| 1 | ADET_TH2[4]* | R/W | MSB bit of AIN2 threshold value for audio detection. | 0 |
| 0 | ADET_TH1[4]* | R/W | MSB bit of AIN1 threshold value for audio detection. | 0 |

* Note :

ADET_TH :Define the threshold value for audio detection.

ADET_TH1: Audio input AIN1.

ADET_TH2: Audio input AIN2.

ADET_TH3: Audio input AIN3.

ADET_TH4: Audio input AIN4.

ADET_TH5: Audio input AIN5.

0:Low value (default)

.

31:High value

0xE2 – Audio Detection Threshold

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|---|-------|
| 7-4 | ADET_TH2[3:0] | R/W | Bit3-0 of AIN2 threshold value for audio detection. | 3h |
| 3-0 | ADET_TH1[3:0] | R/W | Bit3-0 of AIN1 threshold value for audio detection. | 3h |

0xE3 – Audio Detection Threshold

| Bit | Function | R/W | Description | Reset |
|-----|---------------|-----|---|-------|
| 7-4 | ADET_TH4[3:0] | R/W | Bit3-0 of AIN4 threshold value for audio detection. | 3h |
| 3-0 | ADET_TH3[3:0] | R/W | Bit3-0 of AIN3 threshold value for audio detection. | 3h |

Audio Clock Increment**0xF0 – Audio Clock Increment**

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|--|-------|
| 7-0 | ACKI[7:0] | R/W | ACKI[7:0], these bits control ACKI Clock Increment in ACKG block. ACKI[21:0]: 09B583h for fs = 8kHz is default. | 83h |

0xF1 – Audio Clock Increment

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|--|-------|
| 7-0 | ACKI[15:8] | R/W | ACKI[15:8], these bits control ACKI Clock Increment in ACKG block. | B5h |

0xF2 – Audio Clock Increment

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|---|-------|
| 7-6 | Reserved | R | | 0h |
| 5-0 | ACKI[21:16] | R/W | ACKI[21:16], these bits control ACKI Clock Increment in ACKG block. | 09h |

Audio Clock Number**0xF3 – Audio Clock Number**

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|--|-------|
| 7-0 | ACKN[7:0] | R/W | ACKN[7:0], these bits control ACKN Clock Number in ACKG block. ACKN[17:0]: 000100h for Playback Slave-in lock is default. | 00h |

0xF4 – Audio Clock Number

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|---|-------|
| 7-0 | ACKN[15:8] | R/W | ACKN[15:8], these bits control ACKN Clock Number in ACKG block. | 01h |

0xF5 – Audio Clock Number

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|--|-------|
| 7-2 | Reserved | R | | 00h |
| 1-0 | ACKN[17:16] | R/W | ACKN[17:16], these bits control ACKN Clock Number in ACKG block. | 0h |

0xF6 – Serial Clock Divider

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-6 | Reserved | R | | 0 |
| 5-0 | SDIV | R/W | These bits control SDIV Serial Clock Divider in ACKG block. | 00h |

0xF7 – Left/Right Clock Divider

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|-------------|-------|
| 7-6 | Reserved | R | | 0 |
| 5-0 | LRDIV | R/W | Reserved. | 20h |

0xF8 – Audio Clock Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7 | APZ | R/W | These bits control Loop in ACKG block. | 1 |
| 6-4 | APG | R/W | These bits control Loop in ACKG block. | 4h |
| 3 | Reserved | R | | 0 |
| 2 | ACPL | R/W | These bits control Loop closed/open in ACKG block. 0: Loop closed 1 :Loop open(recommended on most application case) | 1 |
| 1 | SRPH | R/W | Reserved.This function is not used in TW2866 chip. | 0 |
| 0 | LRPH | R/W | Reserved.This function is not used in T2866 chip. | 0 |

0xF9 – Video Miscellaneous Function Control

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|---|-------|
| 7 | LIM16 | R/W | 0: Output ranges are limited to 2~254 1: Output ranges are limited to 16~235 for Y and 16~239 for CbCr | 0 |
| 6 | PBREFEN | R/W | Audio ACKG Reference(refin) input select 0: ACKG has video VRST refin input selected by VRSTSEL register 1: ACKG has audio ASYNP refin input | 1 |
| 5 | YCBCR422 | R/W | Control YCbCr 4:2:2 output mode 0: Normal 4:2:2 output mode 1: Averaging 4:2:2 output mode | 0 |
| 4 | HA656MD | R/W | Control HACTIVE signal output on H-Down Scaling output mode. 0: HACTIVE signal is always HACTIVE register's length. 1: HACTIVE signal is same as DVALID signal in H-Down Scaled video output. | 1 |
| 3 | VBI_FRAM | R/W | Test purpose only. | 0 |
| 2 | CNTL656 | R/W | Select invalid data value. 0: 0x80 and 0x10 code will be output as invalid data during active video line. 1: 0x00 code will be output as invalid data during active video line. | 0 |
| 1 | VSCL_SYNC | R/W | Enable the optional ITU-R.656 sync code format. 0: Skip ITU-R BT.656 sync code for non-valid vertical line. 1: Standard ITU-R BT.656 sync code on any vertical line. | 0 |
| 0 | HA_EN | R/W | Control HACTIVE output during vertical blanking period. 0: HACTIVE output is disabled during vertical blanking period. 1: HACTIVE output is enabled during vertical blanking period. | 1 |

Output Enable Control and Clock Output Control**0xFA – Output Enable Control and Clock Output Control**

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|---|-------|
| 7 | VSCL_ENA | R/W | Enable the vertical scaler for 4x CIF time-multiplexed format with 54MHz. 0: Full size for vertical direction 1: Half size for vertical direction | 0 |
| 6 | OE | R/W | Control the tri-state of output pin 0: Outputs are Tri-state except clock output (CLKPOn, CLKNO1) pin 1: Outputs are enabled | 0 |
| 5 | CLKNO1_OEB | R/W | Control the tri-state of CLKNO1 pin 0: Output is enabled (default) 1: Output is Tri-state | 0 |
| 4 | CLKPO1_OEB | R/W | Control the tri-state of CLKPO1 pin 0: Output is enabled 1: Output is Tri-state | 0 |
| 3-2 | CLKNO1_MD | R/W | Control the clock frequency of CLKNO1 pin 0: 27MHz clock output 1: 54MHz clock output 2: 108MHz clock output 3: always 0 value | 0h |
| 1-0 | CLKPO1_MD | R/W | Control the clock frequency of CLKPO1 pin 0: 27MHz clock output 1: 54MHz clock output 2: 108MHz clock output 3: always 0 value | 0h |

0x6A – Clock Output Control

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|--|-------|
| 7-6 | Reserved | R | | 0h |
| 5 | CLKNO2_OEB | R/W | Control the tri-state of CLKNO2 pin 0: Output is enabled 1: Output is Tri-state | 0 |
| 4 | CLKPO2_OEB | R/W | Control the tri-state of CLKPO2 pin 0: Output is enabled 1: Output is Tri-state | 0 |
| 3-2 | CLKNO2_MD | R/W | Control the clock frequency of CLKNO2 pin 0: 27MHz clock output 1: 54MHz clock output 2: 108MHz clock output 3: always 0 value | 0 |
| 1-0 | CLKPO2_MD | R/W | Control the clock frequency of CLKPO2 pin 0: 27MHz clock output 1: 54MHz clock output 2: 108MHz clock output 3: always 0 value | 0 |

0x6B – Clock Output Control

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|--|-------|
| 7-6 | Reserved | R | | 0h |
| 5 | CLKNO3_OEB | R/W | Control the tri-state of CLKNO3 pin 0: Output is enabled 1: Output is Tri-state | 0 |
| 4 | CLKPO3_OEB | R/W | Control the tri-state of CLKPO3 pin 0: Output is enabled 1: Output is Tri-state | 0 |
| 3-2 | CLKNO3_MD | R/W | Control the clock frequency of CLKNO3 pin 0: 27MHz clock output 1: 54MHz clock output 2: 108MHz clock output 3: always 0 value | 0 |
| 1-0 | CLKPO3_MD | R/W | Control the clock frequency of CLKPO3 pin 0: 27MHz clock output 1: 54MHz clock output 2: 108MHz clock output 3: always 0 value | 0 |

0x6C – Output Enable Control and Clock Output Control

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|--|-------|
| 7-6 | Reserved | R | | 0h |
| 5 | CLKNO4_OEB | R/W | Control the tri-state of CLKNO4 pin 0: Output is enabled 1: Output is Tri-state | 0 |
| 4 | CLKPO4_OEB | R/W | Control the tri-state of CLKPO4 pin 0: Output is enabled 1: Output is Tri-state | 0 |
| 3-2 | CLKNO4_MD | R/W | Control the clock frequency of CLKNO4 pin 0: 27MHz clock output 1: 54MHz clock output 2: 108MHz clock output 3: always 0 value | 0 |
| 1-0 | CLKPO4_MD | R/W | Control the clock frequency of CLKPO4 pin 0: 27MHz clock output 1: 54MHz clock output 2: 108MHz clock output 3: always 0 value | 0 |

Clock Polarity Control**0xFB – Clock Polarity Control**

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|--|-------|
| 7 | CLKNO1_POL | R/W | Polarity inverse control on output CLKNO1 signal just before CLKNO1 pin. 0: Not inverted. 1: Polarity inverse. Good for 27MHz/54MHz clock output. | 0 |
| 6 | CLKPO1_POL | R/W | Polarity inverse control on output CLKPO1 signal just before CLKPO1 pin. 0: Not inverted. Good for 27MHz/54MHz clock output. 1: Polarity inverse. | 0 |
| 5 | IRQENA | R/W | Enable/Disable the interrupt request through the IRQ pin. 0: Disable 1: Enable | 0 |
| 4 | IRQPOL | R/W | Select the polarity of interrupt request through the IRQ pin. 0: Falling edge requests the interrupt and keeps its state until cleared 1: Rising edge requests the interrupt and keeps its state until cleared | 0 |
| 3-2 | ADET_MODE | R/W | Define the polarity of state register and interrupt request for audio detection. 0: No interrupt request by the audio detection 1: Make the interrupt request rising only when the audio signal comes in 2: Make the interrupt request falling only when the audio signal goes out 3: Make the interrupt request rising and falling when the audio comes in and goes out | 3 |
| 1-0 | VDET_MODE | R/W | Define the polarity of state register and interrupt request for video detection. 0: No interrupt request by the video detection 1: Make the interrupt request rising only when the video signal comes in 2: Make the interrupt request falling only when the video signal goes out 3: Make the interrupt request rising and falling when the video comes in and goes out | 3 |

0x6D – Clock Polarity Control

| Bit | Function | R/W | Description | Reset |
|-----|------------|-----|---|-------|
| 7 | CLKNO4_POL | R/W | Polarity inverse control on output CLKNO1 signal just before CLKNO1 pin. 0: Not inverted. 1: Polarity inverse. Good for 27MHz/54MHz clock output. | 0 |
| 6 | CLKPO4_POL | R/W | Polarity inverse control on output CLKPO1 signal just before CLKPO1 pin. 0: Not inverted. Good for 27MHz/54MHz clock output. 1: Polarity inverse. | 0 |
| 5 | CLKNO3_POL | R/W | Polarity inverse control on output CLKNO3 signal just before CLKNO3 pin. 0: Not inverted. 1: Polarity inverse. Good for 27MHz/54MHz clock output. | 0 |
| 4 | CLKPO3_POL | R/W | Polarity inverse control on output CLKPO3 signal just before CLKPO3 pin. 0: Not inverted. Good for 27MHz/54MHz clock output. 1: Polarity inverse. | 0 |
| 3 | CLKNO2_POL | R/W | Polarity inverse control on output CLKNO2 signal just before CLKNO2 pin. 0: Not inverted. 1: Polarity inverse. Good for 27MHz/54MHz clock output. | 0 |
| 2 | CLKPO2_POL | R/W | Polarity inverse control on output CLKPO2 signal just before CLKPO2 pin. 0: Not inverted. Good for 27MHz/54MHz clock output. 1: Polarity inverse. | 0 |
| 1-0 | Reserved | R | | 0h |

Enable Video and Audio Detection**0xFC – Enable Video and Audio Detection**

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|--|-------|
| 7-0 | AVDET_ENA | R/W | Enable state register updating and interrupt request of video and audio detection for each input. [0] : Video input VIN1. [1] : Video input VIN2. [2] : Video input VIN3. [3] : Video input VIN4. [4] : Audio input AIN1. [5] : Audio input AIN2. [6] : Audio input AIN3. [7] : Audio input AIN4. 0: Disable state register updating and interrupt request 1: Enable state register updating and interrupt request | FFh |

0x73 – Enable Video and Audio Detection

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|---|-------|
| 7 | Reserved | R | Reserved | 0 |
| 6-4 | Reserved | R | Reserved | 0 |
| 3-1 | Reserved | R | Reserved | 0h |
| 0 | A5DET_ENA | R/W | Enable state register updating and interrupt request of audio AIN5 detection for each input. 0: Disable state register updating and interrupt request 1: Enable state register updating and interrupt request | 1 |

Status of Video and Audio Detection**0xFD – Status of Video and Audio Detection**

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|--|-------|
| 7-0 | AVDET_STATE | R/W | <p>State of Video and Audio detection. These bits are activated according VDET_MODE and ADET_MODE.</p> <p>[0] : Video input VIN1. [1] : Video input VIN2. [2] : Video input VIN3. [3] : Video input VIN4. [4] : Audio input AIN1. [5] : Audio input AIN2. [6] : Audio input AIN3. [7] : Audio input AIN4.</p> <p>0 Inactivated 1 Activated</p> | 00h |

0x74 – Status of Video and Audio Detection

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|---|-------|
| 7-1 | Reserved | R | | 00h |
| 0 | A5DET_STATE | R/W | <p>State of Audio AIN5 detection. This bit is activated according ADET_MODE.</p> <p>0 Inactivated 1 Activated</p> | 0 |

Device ID and Revision ID Flag**0xFE – Device ID and Revision ID Flag**

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|---|-------|
| 7-6 | DEV_ID[6:5] | R | Bit6-5 of Device ID. Together with 0xFF[7:3] indicate TW2866 product ID code. DEV_ID=7'h19 | 0 |
| 5-3 | Reserved | R | | 0 |
| 2-0 | TEST | R/W | Test purpose only. This must be 0 in normal mode. | 0 |

0xFF – Device ID and Revision ID Flag

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|--|-------|
| 7-3 | DEV_ID[4:0] | R | Bit4-0 of Device ID. | 19h |
| 2:0 | REV_ID | R | The revision number. REV_ID=3'h0 1st TW2866 chip. | 0h |

0x60 – Clock PLL Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7 | Reserved | R | | 0 |
| 6 | PLL_PD | R/W | Clock PLL Power down control. 0: Clock PLL normal mode. 1: Clock PLL power down mode. | 0 |
| 5 | PLL_IREF | R/W | Clock PLL Current bias reference. 0: reference 0. 1: reference 1. | 0 |
| 4 | SEL_X24 | R/W | Clock PLL output mode 0: 2x XTI input frequency.54MHz clock input mode. 1: 4x XTI input frequency.27MHz clock input mode. | 0 |
| 3-2 | LP_X4 | R/W | Loop resistor for PLL. 0: 80.5kOhm. 1: 35.5kOhm. 2: 25.5kOhm. 3: 20.5kOhm. | 1h |
| 1-0 | CP_X4 | R/W | Charge-pump current for PLL. 0: 1uA. 1: 5uA. 2: 10uA. 3: 15uA. | 1h |

0x61 – 108MHz Clock Select

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-5 | Reserved | R | Reserved | 0h |
| 4 | DECOSC | R/W | Video Decoder system clock select. 0: Analog Clock PLL output 108MHz/4 clock is selected. 1: system clock generated by XTI input crystal clock. If 108MHz is connected, system clock is XTI / 4 If 54MHz is connected, system clock is XTI / 2. If 27MHz is connected, system clock is XTI. | 0 |
| 3-2 | CKOUTSEL | R/W | Analog Clock PLL output 108MHz select. 0: 108MHz Clock output - in phase. 1: 108MHz Clock output - 90 degree phase shift. 2: 108MHz Clock output - 180 degree phase shift. 3: 108MHz Clock output – 270 degree phase shift. | 0h |
| 1-0 | XTIMD | R/W | XTI pin input clock process control. If XTIMD=0/1/2, Analog Clock PLL Output clock is not used for internal logic process. 0: 27MHz XTI input clock is used for all clock source. 1: 54MHz XTI input clock is used for all clock source. 2: 108MHz XTI input clock is used for all clock source. 3: Analog Clock PLL 108MHz output is used for all system clock source. | 3h |

0x65 – VIDEO Bus Tri-state Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-5 | Reserved | R | | 0h |
| 4 | VD4ORD | R/W | Select the video channel output order on 4xD1 output mode. 0:Ch1->Ch2->Ch3->Ch4->Ch1->Ch2->Ch3->....(increase). 1:Ch4->Ch3->Ch2->Ch1->Ch4->Ch3->Ch2->....(decrease) | 0 |
| 3 | VD4OEB | R/W | VD4[7:0] output tri-state control. 1: tri-state output VD4[7:0]. 0: normal output VD4[7:0]. | 0 |
| 2 | VD3OEB | R/W | VD3[7:0] output tri-state control. 1: tri-state output VD3[7:0]. 0: normal output VD3[7:0]. | 0 |
| 1 | VD2OEB | R/W | VD2[7:0] output tri-state control. 1: tri-state output VD2[7:0]. 0: normal output VD2[7:0]. | 0 |
| 0 | VD1OEB | R/W | VD1[7:0] output tri-state control. 1: tri-state output VD1[7:0]. 0: normal output VD1[7:0]. | 0 |

0x66 – Optional Clock Output

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | VD4_27C | R/W | 0: normal 27MHz output if CLKPO4_MD/CLKNO4_MD select 27MHz output. 1: Optional type 27MHz clock output on CLKPO4/CLKNO4 pins. | 0 |
| 6 | VD3_27C | R/W | 0: normal 27MHz output if CLKPO3_MD/CLKNO3_MD select 27MHz output. 1: Optional type 27MHz clock output on CLKPO3/CLKNO3 pins. | 0 |
| 5 | VD2_27C | R/W | 0: normal 27MHz output if CLKPO2_MD/CLKNO2_MD select 27MHz output. 1: Optional type 27MHz clock output on CLKPO2/CLKNO2 pins. | 0 |
| 4 | VD1_27C | R/W | 0: normal 27MHz output if CLKPO1_MD/CLKNO1_MD select 27MHz output. 1: Optional type 27MHz clock output on CLKPO1/CLKNO1 pins. | 0 |
| 3 | CK4_13 | R/W | 0: normal clock output on CLKPO4/CLKNO4 pins by CLKPO4_MD/CLKNO4_MD. 1: Optional 13.5MHz clock output on CLKPO4/CLKNO4 pins. | 0 |
| 2 | CK3_13 | R/W | 0: normal clock output on CLKPO3/CLKNO3 pins by CLKPO3_MD/CLKNO3_MD. 1: Optional 13.5MHz clock output on CLKPO3/CLKNO3 pins. | 0 |
| 1 | CK2_13 | R/W | 0: normal clock output on CLKPO2/CLKNO2 pins by CLKPO2_MD/CLKNO2_MD. 1: Optional 13.5MHz clock output on CLKPO2/CLKNO2 pins. | 0 |
| 0 | CK1_13 | R/W | 0: normal clock output on CLKPO1/CLKNO1 pins by CLKPO1_MD/CLKNO1_MD. 1: Optional 13.5MHz clock output on CLKPO1/CLKNO1 pins. | 0 |

0x6E – Reserved

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|-------------|-------|
| 7 | Reserved | R | | 0 |
| 6-4 | Reserved | R | | 2h |
| 3 | Reserved | R | | 0 |
| 2-0 | Reserved | R | | 1h |

0x6F – Reserved

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|-------------|-------|
| 7 | Reserved | R | | 0 |
| 6-4 | Reserved | R | | 4h |
| 3 | Reserved | R | | 0 |
| 2-0 | Reserved | R | | 3h |

0x70 – Audio Clock Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | Reserved | R | | 0 |
| 6 | S2I_8BIT | R/W | 0: ACLKP/ASYNP/ADATP pin input is 16bit control. 1: ACLKP/ASYNP/ADATP pin input is 8bit control. | 0 |
| 5 | ACLKRPOL | R/W | ACLKR input signal polarity inverse. 0: not inverse. 1: inverse. | 0 |
| 4 | ACLKPPOL | R/W | ACLKP input signal polarity inverse. 0: not inverse. 1: inverse. | 0 |
| 3 | AFAUTO | R/W | ACKI[21:0] control automatic set up with AFMD registers. This mode is only effective when ACLKRMAS=1. 0: ACKI[21:0] registers set up ACKI control. 1: ACKI control is automatically set up by AFMD register values. | 0 |
| 2-0 | AFMD | R/W | AFAUTO control mode. 0: 8kHz setting(default). 1: 16kHz setting. 2: 32kHz setting. 3: 44.1kHz setting. 4: 48kHz setting. | 0h |

0x71 – Digital Audio Input Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7 | I2S8MODE | R/W | 8bit I2S Record output mode. 0: L/R half length separated output. 1: One continuous packed output equal to DSP output format. | 0 |
| 6 | MASCKMD | R/W | Audio Clock Master ACLKR output wave format. 0: High period is one 27MHz clock period. 1: Almost duty 50-50% clock output on ACLKR pin.If this mode is selected, two times bigger number value need to be set up ACKI registers. If AFAUTO=1, ACKI control is automatically set up even if MASCKMD=1. SDIV=00h is used with this function normally. | 0 |
| 5 | PBINSWAP | R/W | Playback ACLKP/ASYNP/ADATP input data MSB-LSB swapping. 0: Not swapping. 1: Swapping. | 0 |
| 4 | ASYNRDLY | R/W | ASYNR input signal delay. 0: No delay. 1: Add one 27MHz period delay in ASYNR signal input. | 0 |
| 3 | ASYNPDLY | R/W | ASYNP input signal delay. 0: No delay. 1: Add one 27MHz period delay in ASYNP signal input. | 0 |
| 2 | ADATPDLY | R/W | ADATP input data delay by one ACLKP clock. 0: No delay. This is for I2S type 1T delay input interface. 1: Add 1 ACLKP clock delay in ADATP input data. This is for left-justified type 0T delay input interface. | 0 |
| 1-0 | INLAWMD | R/W | Select u-Law/A-Law/PCM/SB data input format on ADATP pin. 0:PCM input 1:SB(Signed MSB bit in PCM data is inverted) input 2:u-Law input 3:A-Law input | 0h |

ADATM I2S Output Select**0x7B – ADATM I2S Output Select**

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|--|-------|
| 7-5 | Reserved | R | | 0h |
| 4-0 | I2SO_RSEL | R/W | Select R-channel output data on ADATM pin when ADATM_I2SOEN=1. * | 15h |

***Note :**

Both I2SO_RSEL and I2SO_LSEL select output data by following order.

| | |
|---------|---|
| 0 | Select record audio of channel 1(AIN1) |
| 1 | Select record audio of channel 2(AIN2) |
| 2 | Select record audio of channel 3(AIN3) |
| 3 | Select record audio of channel 4(AIN4) |
| 4 | Select record audio of channel 5(AIN5) |
| 5 | Select record audio of channel 6(AIN6) |
| 6 | Select record audio of channel 7(AIN7) |
| 7 | Select record audio of channel 8(AIN8) |
| 8 | Select record audio of channel 9(AIN9) |
| 9 | Select record audio of channel 10(AIN10) |
| 10(Ah) | Select record audio of channel 11(AIN11) |
| 11(Bh) | Select record audio of channel 12(AIN12) |
| 12(Ch) | Select record audio of channel 13(AIN13) |
| 13(Dh) | Select record audio of channel 14(AIN14) |
| 14(Eh) | Select record audio of channel 15(AIN15) |
| 15(Fh) | Select record audio of channel 16(AIN16) |
| 16(10h) | Select playback audio of the first stage chip(PB1) |
| 17(11h) | Select playback audio of the second stage chip(PB2) |
| 18(12h) | Select playback audio of the third stage chip(PB3) |
| 19(13h) | Select playback audio of the last stage chip(PB4) |
| 20(14h) | Select mixed audio. |
| 21(15h) | Select record audio of channel 51(AIN51)(default) |
| 22(16h) | Select record audio of channel 52(AIN52) |
| 23(17h) | Select record audio of channel 53(AIN53) |
| 24(18h) | Select record audio of channel 54(AIN54) |
| Others | no audio output. |

0x7C – ADATM I2S Output Select

| Bit | Function | R/W | Description | Reset |
|-----|-----------|-----|--|-------|
| 7-5 | Reserved | R | | 0h |
| 4-0 | I2SO_LSEL | R/W | Select L-channel output data on ADATM pin when ADATM_I2SOEN=1. * | 15h |

* Note : Please read 0x7B Note for detail description.

AIN5 Record Output**0x7D – AIN5 Record Output**

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|--|-------|
| 7-6 | I2SRECSEL54 | R/W | Select output data in bellow dat54 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54. | 3h |
| 5-4 | I2SRECSEL53 | R/W | Select output data in bellow dat53 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54. | 2h |
| 3-2 | I2SRECSEL52 | R/W | Select output data in bellow dat52 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54. | 1h |
| 1-0 | I2SRECSEL51 | R/W | Select output data in bellow dat51 position. 0: AIN51, 1:AIN52, 2:AIN53, 3:AIN54. | 0 |

If I2S mode(RM_SYNC=0),
 L data : <dat0><dat1><dat2><dat3><dat4><dat5><dat6><dat7><dat51><dat52>
 R data : <dat8><dat9><datA><datB><datC><datD><datE><datF><dat53><dat54>

If DSP mode(RM_SYNC=1),all data are continuous.
 <dat0><dat1><dat2><dat3><dat4><dat5><dat6><dat7><dat8><dat9><datA><datB><datC>
 <datD><datE><datF><dat51><dat52><dat53><dat54>

All other datN(N=0,1,2,,,,F) are selected by R_SEQ_N registers

0x89 – Audio Fs Mode Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-6 | Reserved | R | | 0 |
| 5 | ACLKR128 | R/W | ACLKR clock output mode for special 16x8bit(total 128bit) data interface. 0: ACLKR output is normal. 1: the number of ACLKR clock per fs is 128.This function is effective with RM_8BIT=1 8bit mode(special purpose). | 0 |
| 4 | ACLKR64 | R/W | ACLKR clock output mode for special 4 word output interface.ACLKRMASMASTER=1 mode only. 0: ACLKR output is normal 1: the number of ACLKR clock per fs is 64. | 0 |
| 3 | AFS384 | R/W | Special Audio fs Sampling mode. 0: Audio fs Sampling mode is normal 256xfS if AIN5=0. 1: Audio fs Sampling mode is 384xfS mode. In this mode,AIMANU=1,A1NUM=0,A2NUM=1, A3NUM=2,A4NUM=3,A5NUM=4 are needed to be set up. | 0 |
| 2 | AIN5MD | R/W | Audio Input process mode. 0: AIN1/AIN2/AIN3/AIN4 4 Audio input only process. This mode is 256xfS if AFS384=0.In this mode,AIN5 input is not processed. 1: AIN1/AIN2/AIN3/AIN4/AIN5 5 Audio input process. This mode is 320xfS Mode if AFS384=0. | 0 |
| 1-0 | Reserved | R | | 1h |

0xB2 – VDLOSS Output

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7-1 | Reserved | R | | 00h |
| 0 | VDLOSSOE | R/W | Video Decoder VDLOSS1/VDLOSS2/VDLOSS3/VDLOSS4 signals output MPP1/ MPP2/ MPP3/ MPP4 pins. 0: not output VDLOSS1/VDLOSS2/VDLOSS3/VDLOSS4 on MPP1/MPP2/MPP3/MPP4 pins(default). 1: Ch1 Video Decoder VDLOSS1 output on MPP1 pin. Ch2 Video Decoder VDLOSS2 output on MPP2 pin. Ch3 Video Decoder VDLOSS3 output on MPP3 pin. Ch4 Video Decoder VDLOSS4 output on MPP4 pin. | 0 |

0x50 – Audio DAC Gain Control

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|---|-------|
| 7 | ADACCLK_INV | R/W | Clock inversion control in Audio DAC module. 0: not inverted. 1: inverted. | 0 |
| 6-4 | DAC_IB_DAC | R/W | Audio DAC bias fine control 000->10uA 001->12uA 010->6uA 011->8uA 100->18uA 101->20uA 110->14uA 111->16uA Note: Idac=10uA + Idac_ib_dac + i_dac_ib_adc Default: Idac=60uA. 80uA to get full scale | 0 |
| 3 | Reserved | R | | 0 |
| 2-0 | DAC_IB_ADC | R/W | Audio DAC bias coarse control 000->40uA 001->48uA 010->24uA 011->32uA 100->72uA 101->80uA 110->56uA 111->64uA Note: Idac=10uA + Idac_ib_dac + i_dac_ib_adc Default: Idac=60uA. 80uA to get full scale | 0 |

0x51 – Audio DAC Low Pass Bias Control

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|--|-------|
| 7-0 | DAC_LPFBIAS | R/W | Audio DAC Reference LPF control DAC_LPFBIAS<7:5>=000 -> 2uA DAC_LPFBIAS<7:5>=001 -> 4uA DAC_LPFBIAS<7:5>=010 -> 6uA DAC_LPFBIAS<7:5>=011 -> 8uA DAC_LPFBIAS<7:5>=100 -> 10uA DAC_LPFBIAS<7:5>=101 -> 12uA DAC_LPFBIAS<7:5>=110 -> 14uA DAC_LPFBIAS<7:5>=111 -> 16uA DAC_LPFBIAS<4>=0 -> disable the onchip reference bias DAC_LPFBIAS<4>=1 -> enable the onchip reference bias DAC_LPFBIAS<3:0>=0000 -> 31.25nA DAC_LPFBIAS<3:0>=0001 -> 62.5nA DAC_LPFBIAS<3:0>=1000 -> 125nA (default) DAC_LPFBIAS<3:0>=1111 -> 343.75nA | 00 |

0x52 – Audio DAC LPF and Bias Control

| Bit | Function | R/W | Description | Reset |
|-----|-------------|-----|---|-------|
| 7 | Reserved | R | | 0 |
| 6-4 | LPFSEL | R/W | Audio DAC LPF corner frequency selection 000->15.6kHz 001->7.8kHz 010->Don't use 011->3.9kHz 100->Don't use 101->Don't use 110->Don't use 111->2.6Khz | 0 |
| 3 | BIAS_SEL | RW | Audio DAC Bias selection. 0-> AVDD33 as the reference voltage. 1-> select bandgap voltage as the reference | 0 |
| 2-0 | DAC_IB_OTAs | R/W | Audio DAC OTA bias control. 000->10uA 001->12uA 010->6uA 011->8uA 100->18uA 101->20uA 110->14uA 111->16uA | 0 |

0x53 – Audio DAC Test Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7 | Reserved | R | | 0 |
| 6-4 | TAADCO | R/W | <p>Audio ADC Test Purpose only. When TEST(regFE[2:0]) register is set to 7h, ADATM.MPP4,VD4[7:0]} pins have audio ADC data output by following selection.</p> <p>0 : AIN1 Audio ADC data output 1 : AIN2 Audio ADC data output 2 : AIN3 Audio ADC data output 3 : AIN4 Audio ADC data output 4 : AIN5 Audio ADC data output</p> | 0 |
| 3 | TVSENSE | RW | <p>AVDS Test purpose only.0 should be set up. 0:VD4[7:0] pin are normal function output. 1:VD4[7:0] pin output have followings.</p> <p>VD4[7] : VSENSE4B VD4[6] : VSENSE3B VD4[5] : VSENSE2B VD4[4] : VSENSE1B VD4[3] : VSENSE4A VD4[2] : VSENSE3A VD4[1] : VSENSE2A VD4[0] : VSENSE1A</p> | 0 |
| 2-0 | ADACTEST | R/W | <p>Audio DAC test control</p> <p>000->normal operation 001->ibias places to the dac_out (Don't use) 010->din_0 is places to the dac_out (Don't use) 011->both ibais and din_o are placed at the dac_out (Don't use) 100->disable output driver. Dac_out floating 101-> disable output driver, ibais places to dac_out 110-> disable output driver, din_0 places to dac_out 111->don't use</p> | 0 |

0x54 – Audio ADC Control

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7-6 | Reserved | R | | 0 |
| 5 | DOUT_RST | R/W | Audio ADC digital output reset for all channel. This bit must be set up to 0 again after 1 value is set up. | 0 |
| 4 | DIV_RST | R/W | Audio ADC divider reset. This bit must be set up to 0 again after 1 value is set up. | 0 |
| 3 | ACALEN | RW | Audio ADC Calibration control. This bit must be set up to 0 again after 1 value is set up. | 0 |
| 2-0 | ASAVE | R/W | Audio ADC power save | 7 |

0x58 – AVDS Status(Test Purpose only)

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---------------------------|-------|
| 7 | VSENSE4B | R | VIN4B AVDS VSENSE signal. | X |
| 6 | VSENSE3B | R | VIN3B AVDS VSENSE signal. | X |
| 5 | VSENSE2B | R | VIN2B AVDS VSENSE signal. | X |
| 4 | VSENSE1B | R | VIN1B AVDS VSENSE signal. | X |
| 3 | VSENSE4A | R | VIN4A AVDS VSENSE signal. | X |
| 2 | VSENSE3B | R | VIN3A AVDS VSENSE signal. | X |
| 1 | VSENSE2B | R | VIN2A AVDS VSENSE signal. | X |
| 0 | VSENSE1B | R | VIN1A AVDS VSENSE signal. | X |

0x59 – AVDS Power Control(Test Purpose only)

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | PDBV4B | R/W | 0: VIN4B AVDS power down. 1: VIN4B AVDS normal operation. | 0 |
| 6 | PDBV3B | R/W | 0: VIN3B AVDS power down. 1: VIN3B AVDS normal operation. | 0 |
| 5 | PDBV2B | R/W | 0: VIN2B AVDS power down. 1: VIN2B AVDS normal operation. | 0 |
| 4 | PDBV1B | R/W | 0: VIN1B AVDS power down. 1: VIN1B AVDS normal operation. | 0 |
| 3 | PDBV4A | R/W | 0: VIN4A AVDS power down. 1: VIN4A AVDS normal operation. | 0 |
| 2 | PDBV3B | R/W | 0: VIN3A AVDS power down. 1: VIN3A AVDS normal operation. | 0 |
| 1 | PDBV2B | R/W | 0: VIN2A AVDS power down. 1: VIN2A AVDS normal operation. | 0 |
| 0 | PDBV1B | R/W | 0: VIN1A AVDS power down. 1: VIN1A AVDS normal operation. | 0 |

0x5A – VSAVE

| Bit | Function | R/W | Description | Reset |
|-----|--------------|-----|---|-------|
| 7 | AVDSMD | R/W | AVDS module PDB input select. (Test purpose only). 0: PDBV4B input = PDBV4B register. PDBV3B input = PDBV3B register. PDBV2B input = PDBV2B register. PDBV1B input = PDBV1B register. PDBV4A input = PDBV4A register. PDBV3A input = PDBV3A register. PDBV2A input = PDBV2A register. PDBV1A input = PDBV1A register. 1: PDBV4B input = inversed VIN4 register. PDBV3B input = inversed VIN3 register. PDBV2B input = inversed VIN2 register. PDBV1B input = inversed VIN1 register. PDBV4A input = VIN4 register. PDBV3A input = VIN3 register. PDBV2A input = VIN2 register. PDBV1A input = VIN1 register. | 0 |
| 6 | VREF50M_AVDS | R/W | AVDS Vref selection(Test purpose only). 0->100mV, 1->50mV | 0 |
| 5-4 | BIAS_AVDS | R/W | AVDS BIAS selection(Test purpose only). 00->1.0uA 01->2.0uA 10->8.0uA 11->8.0uA | 0 |
| 3 | PD_BIAS | R/W | Video ADC PD_BIAS. | 0 |
| 2-0 | VSAVE | R/W | Video ADC power save. | 7 |

0x5B– Video Output Pin Drive

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | VD4_DS | R/W | VD4[7:0] pin drive. 0: Low-drive, 1: High-drive | 0 |
| 6 | VD3_DS | R/W | VD3[7:0] pin drive. 0: Low-drive, 1: High-drive | 0 |
| 5 | VD2_DS | R/W | VD2[7:0] pin drive. 0: Low-drive, 1: High-drive | 0 |
| 4 | VD1_DS | R/W | VD1[7:0] pin drive. 0: Low-drive, 1: High-drive | 0 |
| 3 | CK4_DS | R/W | CLKPO4/CLKNO4 pin drive. 0: Low-drive, 1: High-drive | 0 |
| 2 | CK3_DS | R/W | CLKPO3/CLKNO3 pin drive. 0: Low-drive, 1: High-drive | 0 |
| 1 | CK2_DS | R/W | CLKPO2/CLKNO2 pin drive. 0: Low-drive, 1: High-drive | 0 |
| 0 | CK1_DS | R/W | CLKPO1/CLKNO1 pin drive. 0: Low-drive, 1: High-drive | 0 |

0x5C– Video Output Pin Drive

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|---|-------|
| 7 | Reserved | R | | 0 |
| 5 | BGCTL | R/W | 0: Reg96[7:0] control all CH1/CH2/CH3/CH4 video. 1: Reg96[7:0] control only CH1 video. Reg5D[7:0] control only CH2 video. Reg5E[7:0] control only CH3 video. Reg5F[7:0] control only CH4 video. | 0 |
| 4 | VSWEN | R/W | 0: Video Input VIN1A/VIN1B, VIN2A/VIN2B, VIN3A/VIN3B, VIN4A/VIN4B are selected by register VIN1/VIN2/VIN3/VIN4. 1: One Video input time of either VINnA or VINnB changes automatically by VSWNUM setting. | 0 |
| 3-0 | VSWNUM | R/W | One Video input time is (VSWNUM+1) frame time in VIN1A/VIN1B video when VSWEN=1. 0: 1 frame time in VIN1A/VIN1B video. 1: 2 frame time in VIN1A/VIN1B video. 2: 3 frame time in VIN1A/VIN1B video. . . . F: 16 frame time in VIN1A/VIN1B video. | 1 |

0x5D – CH2 Miscellaneous Control II on BGCTL=1

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | NKILL_2 | R/W | 1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled. | 1 |
| 6 | PKILL_2 | R/W | 1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled. | 1 |
| 5 | SKILL_2 | R/W | 1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled. | 1 |
| 4 | CBAL_2 | R/W | 0 = Normal output 1 = special output mode. | 0 |
| 3 | FCS_2 | R/W | 1 = Force decoder output value determined by CCS. 0 = Disabled. | 0 |
| 2 | LCS_2 | R/W | 1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled. | 0 |
| 1 | CCS_2 | R/W | When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black. | 0 |
| 0 | BST_2 | R/W | 1 = Enable blue stretch. 0 = Disabled. | 0 |

0x5E – CH3 Miscellaneous Control II on BGCTL=1

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | NKILL_3 | R/W | 1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled. | 1 |
| 6 | PKILL_3 | R/W | 1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled. | 1 |
| 5 | SKILL_3 | R/W | 1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled. | 1 |
| 4 | CBAL_3 | R/W | 0 = Normal output 1 = special output mode. | 0 |
| 3 | FCS_3 | R/W | 1 = Force decoder output value determined by CCS. 0 = Disabled. | 0 |
| 2 | LCS_3 | R/W | 1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled. | 0 |
| 1 | CCS_3 | R/W | When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black. | 0 |
| 0 | BST_3 | R/W | 1 = Enable blue stretch. 0 = Disabled. | 0 |

0x5F – CH4 Miscellaneous Control II on BGCTL=1

| Bit | Function | R/W | Description | Reset |
|-----|----------|-----|--|-------|
| 7 | NKILL_4 | R/W | 1 = Enable noisy signal color killer function in NTSC mode. 0 = Disabled. | 1 |
| 6 | PKILL_4 | R/W | 1 = Enable automatic noisy color killer function in PAL mode. 0 = Disabled. | 1 |
| 5 | SKILL_4 | R/W | 1 = Enable automatic noisy color killer function in SECAM mode. 0 = Disabled. | 1 |
| 4 | CBAL_4 | R/W | 0 = Normal output 1 = special output mode. | 0 |
| 3 | FCS_4 | R/W | 1 = Force decoder output value determined by CCS. 0 = Disabled. | 0 |
| 2 | LCS_4 | R/W | 1 = Enable pre-determined output value indicated by CCS when video loss is detected. 0 = Disabled. | 0 |
| 1 | CCS_4 | R/W | When FCS is set high or video loss condition is detected when LCS is set high, one of two colors display can be selected. 1 = Blue color. 0 = Black. | 0 |
| 0 | BST_4 | R/W | 1 = Enable blue stretch. 0 = Disabled. | 0 |

Electrical Information

Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Units |
|----------------------------------|----------------------|------|-----|---------|-------|
| VDDV (measured to VSSV) | VDD _{VM} | -0.5 | | 4.5 | V |
| VDDVDA(measured to VSSVDA) | VDD _{VDAM} | -0.5 | | 4.5 | V |
| VDDAPLL(measured to VSSAPLL) | VDD _{APLLM} | -0.5 | | 4.5 | V |
| VDDA (measured to VSSA) | VDD _{AM} | -0.5 | | 4.5 | V |
| VDDI (measured to VSS) | VDD _{IM} | -0.5 | | 2.3 | V |
| VDDO (measured to VSS) | VDD _{OM} | -0.5 | | 4.5 | V |
| Digital Input/Output Voltage | - | -0.5 | | 4.5 | V |
| Analog Input Voltage | - | -0.5 | | 3.3 | V |
| Storage Temperature | T _S | -65 | | 150 | ° C |
| Junction Temperature | T _J | 0 | | 125 | ° C |
| Reflow Soldering (10-30 Seconds) | T _{PEAK} | | | 255-260 | ° C |

Note : Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if operate exceeding the rating. The device should be operated under recommended operating condition.

Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---------------------|------|-----|------|-------|
| VDDV (measured to VSSV) | VDD _V | 3.0 | 3.3 | 3.6 | V |
| VDDVDA(measured to VSSVDA) | VDD _{VDA} | 3.0 | 3.3 | 3.6 | V |
| VDDAPLL(measured to VSSAPLL) | VDD _{APLL} | 3.0 | 3.3 | 3.6 | V |
| VDDA (measured to VSSA) | VDD _A | 3.0 | 3.3 | 3.6 | V |
| VDDI (measured to VSS) | VDD _I | 1.08 | 1.2 | 1.32 | V |
| VDDO (measured to VSS) | VDD _O | 3.0 | 3.3 | 3.6 | V |
| Analog Input V _{pp} (AC coupling required) | V _{AIN} | 0 | 1.0 | 2.0 | V |
| Ambient Operating Temperature | T _A | -40 | | 85 | ° C |

DC Electrical Parameters

| Parameter | Symbol | Min | Typ | Max | Units |
|---|--------------|------|--------|----------|---------|
| Digital Inputs | | | | | |
| Input High Voltage | V_{IH} | 2.0 | | 3.6 | V |
| Input Low Voltage | V_{IL} | -0.3 | | 0.8 | V |
| Input Leakage Current (@ $V_I=3.3V$ or $0V$) | I_L | | | ± 10 | μA |
| Input Capacitance | C_{IN} | | 6 | | pF |
| Digital Outputs | | | | | |
| Output High Voltage | V_{OH} | 2.4 | | | V |
| Output Low Voltage | V_{OL} | | | 0.4 | V |
| High Level Output Current (@ $V_{OH}=2.4V$) | I_{OH} | 9.3 | 18.2 | 29.5 | mA |
| Low Level Output Current (@ $V_{OL}=0.4V$) | I_{OL} | 7.4 | 11.8 | 16.5 | mA |
| Tri-state Output Leakage Current (@ $V_O=3.3V$ or $0V$) | I_{OZ} | | | ± 10 | μA |
| Output Capacitance | C_O | | 6 | | pF |
| Analog Pin Input Capacitance | C_A | | 6 | | pF |
| Supply Current | | | | | |
| Analog Video ADC Supply Current (V_{DDV} , 3.3V) | I_{DDV} | | 66.0 | | mA |
| Analog Video DAC Supply Current (V_{DDVDA} , 3.3V) | I_{DDVDA} | | 71.6 | | mA |
| Analog Audio Supply Current (V_{DDA} , 3.3V) | I_{DDA} | | 21.5 | | mA |
| Clock PLL Supply Current (V_{DDAPLL} , 3.3V) | I_{DDAPLL} | | 2.2 | | mA |
| Digital Internal Supply Current (V_{DDI} , 1.2V) | I_{DDI} | | 36.5 | | mA |
| Digital I/O Supply Current (V_{DDO} , 3.3V) | I_{DDO} | | 27.5 | | mA |
| Total Power Dissipation | P | | 666.84 | | mW |

XTI and Video Data/Sync Timing

| Parameter | Symbol | Min | Typ | Max | Units |
|---|--------|-----|-----|-----|-------|
| Delay from XTI to CLKPOn(27MHz) | 1 | 1 | | 5 | Ns |
| Hold from CLKPOn to Video Data/Sync (27MHz) | 2a | 18 | | | Ns |
| Delay from CLKPOn to Video Data/Sync (27MHz) | 2b | | | 19 | Ns |
| Delay from XTI to CLKPO(54MHz) | 3 | 0.1 | | 5 | Ns |
| Hold from CLKPOn to Video Data/Sync (54MHz) | 4a | 9 | | | Ns |
| Delay from CLKPOn to Video Data/Sync (54MHz) | 4b | | | 10 | Ns |
| Delay from XTI to CLKPO(108MHz) | 5 | 3 | | | Ns |
| Hold from CLKPOn to Video Data/Sync (108MHz) | 6a | 5 | | | Ns |
| Delay from CLKPOn to Video Data/Sync (108MHz) | 6b | | | 6 | Ns |

Note : CLKPOn timing is related with CLKPOn_DEL register value. The following timing diagram is illustrated in the case that the CLKPOn_DEL is set to 0hex and CLKPOn_POL is set to 0. CLKNOn timing is almost inversed CLKPOn timing as default setting.

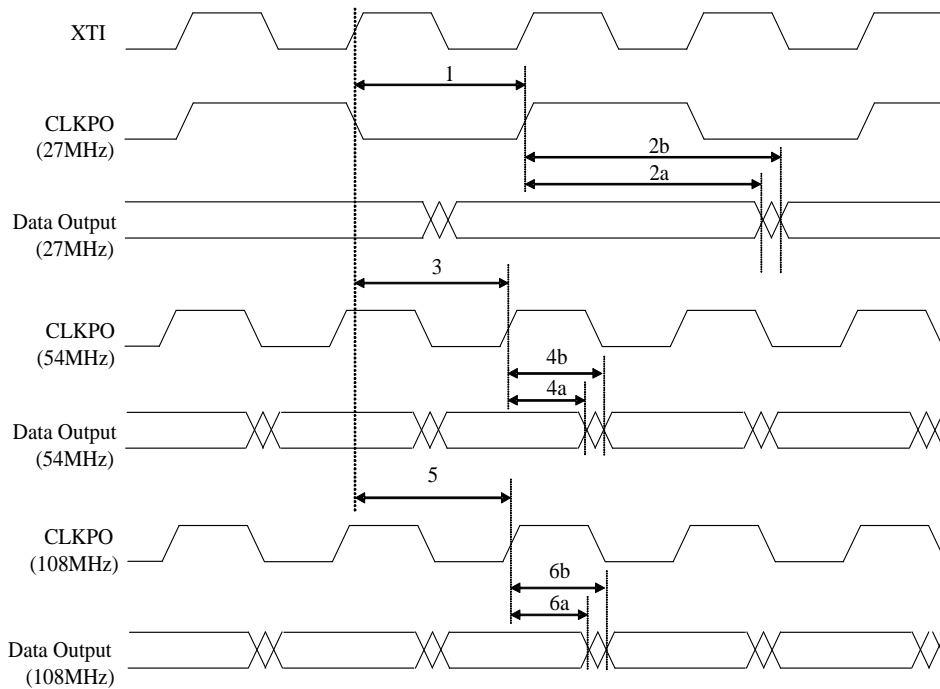
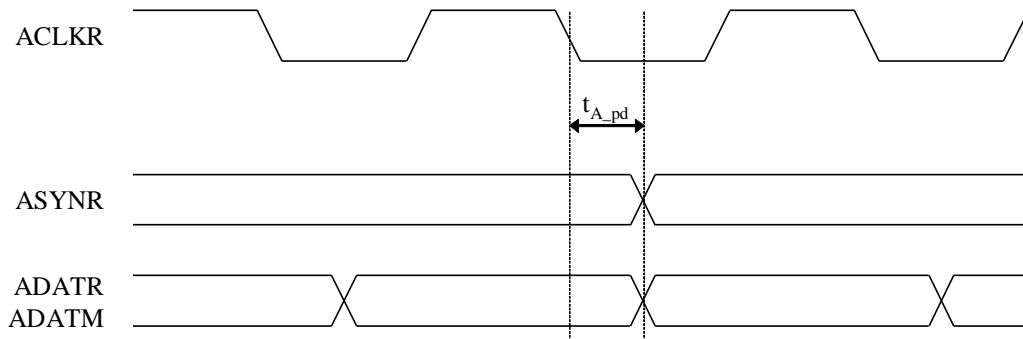


Fig26 XTI and Video Data Timing Diagram

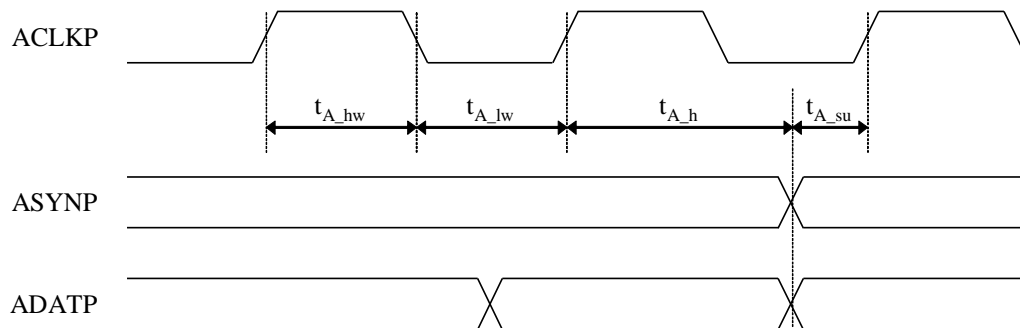
Digital Serial Audio Interface Timing

| Parameter | Symbol | Min | Typ | Max | Units |
|-------------------------------------|-------------|-----|-----|-----|-------|
| ASYNR,ADATR,ADATM propagation delay | T_{A_pd} | 0.6 | | 2 | ns |
| ACLKP High pulse duration | T_{A_hw} | 37 | | | ns |
| ACLKP Low pulse duration | T_{A_lw} | 74 | | | ns |
| ASYNP, ADATP setup time | T_{A_su} | 36 | | | ns |
| ASYNP, ADATP hold time | T_{A_h} | 35 | | | ns |

Note : T_{A_lw} Min value and T_{A_su} Min value are $F_s=48\text{KHz}$ mode only.If $F_s < 48\text{KHz}$,these Min values are more bigger.High period of ACLKR/ACLKP is 27MHz one clock period.



(a) Record and Mix Audio(Master mode)



(b) Playback Audio(Master mode)

Fig27 Timing Diagram of Digital Serial Audio Interface

Serial Host Interface Timing

| Parameter | Symbol | Min | Typ | Max | Units |
|--------------------------------------|-------------|-----|-----|-----|-------|
| Bus Free Time between STOP and START | t_{BF} | 740 | | | ns |
| SDAT setup time | t_{sSDAT} | 100 | | | ns |
| SDAT hold time(XTI 108MHz) | t_{hSDAT} | 50 | | | ns |
| SDAT hold time(XTI 54MHz) | | 100 | | | ns |
| Setup time for START condition | t_{sSTA} | 370 | | | ns |
| Setup time for STOP condition | t_{sSTOP} | 370 | | | ns |
| Hold time for START condition | t_{hSTA} | 74 | | | ns |
| Rise time for SCLK and SDAT | t_R | | | 300 | ns |
| Fall time for SCLK and SDAT | t_F | | | 300 | ns |
| Capacitive load for each bus line | C_{BUS} | | | 400 | pF |
| LOW period of SCLK | t_{LOW} | 0.5 | | | us |
| HIGH period of SCLK | t_{HIGH} | 0.5 | | | us |
| SCLK clock frequency(XTI 108MHz) | f_{SCLK} | | | 400 | KHz |
| SCLK clock frequency(XTI 54MHz) | | | | 350 | KHz |

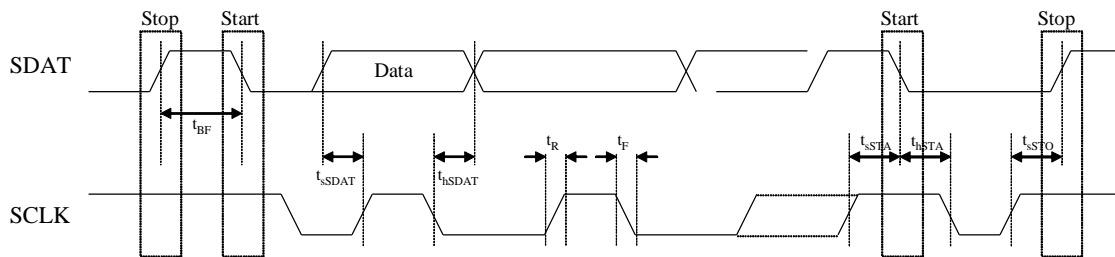


Fig28 Serial Host Interface Timing

Video Decoder Parameter 1

| Parameter | Symbol | Min | Typ | Max | Units |
|---------------------------------|--------------|------|---------|-----|-------|
| ADCs | | | | | |
| ADC resolution | ADCR | - | 10 | - | Bits |
| ADC integral Non-linearity | AINL | - | ±1 | - | LSB |
| ADC differential non-linearity | ADNL | - | ±1 | - | LSB |
| ADC clock rate | f_{ADC} | 24 | 27 | 30 | MHz |
| Horizontal PLL | | | | | |
| Line frequency (50Hz) | f_{LN} | - | 15.625 | - | KHz |
| Line frequency (60Hz) | f_{LN} | - | 15.734 | - | KHz |
| static deviation | Δf_H | - | - | 6.2 | % |
| Subcarrier PLL | | | | | |
| subcarrier frequency (NTSC-M) | f_{SC} | - | 3579545 | - | Hz |
| subcarrier frequency (PAL-BDGI) | f_{SC} | - | 4433619 | - | Hz |
| subcarrier frequency (PAL-M) | f_{SC} | - | 3575612 | - | Hz |
| subcarrier frequency (PAL-N) | f_{SC} | - | 3582056 | - | Hz |
| lock in range | Δf_H | ±450 | - | - | Hz |
| Oscillator Input | | | | | |
| nominal frequency | | - | 27 | - | MHz |
| deviation | | - | - | ±50 | ppm |
| duty cycle | | - | - | 55 | % |

Video Decoder Parameter 2

| Parameter | Symbol | Min | Typ | Max | Units |
|--------------------------------|--------|-----|------|-----|--------|
| Lock Specification | | | | | |
| Sync Amplitude Range | | 1 | | 200 | % |
| Color Burst Range | | 5 | | 200 | % |
| Horizontal Lock Range | | -5 | | 5 | % |
| Vertical Lock Range | | 45 | | 65 | Hz |
| Fsc Lock Range | | | ±450 | | Hz |
| Color Burst Position Range | | | ±2.2 | | μs |
| Color Burst Width Range | | | | | cycle |
| Video Bandwidth | | | | | |
| B/W | | | 6 | | MHz |
| Noise Specification | | | | | |
| SNR (Luma flat field) | | | 57 | | dB |
| Nonlinear Specification | | | | | |
| Y Nonlinearity | | | 0.5 | 0.7 | % |
| Differential Phase | DP | | 0.4 | 0.6 | Degree |
| Differential Gain | DG | | 0.6 | 0.8 | % |
| Chroma Specification | | | | | |
| Hue Accuracy | | | 1 | | Degree |
| Chroma ACC Range | | | | 400 | % |
| Chroma Amplitude Error | | | 1 | | % |
| Chroma Phase Error | | | 0.3 | | % |
| Chroma Luma Intermodulation | | | 0.2 | | % |
| K-Factor | | | | | |
| K2T | | | 0.5 | | % |
| Kpulse/bar | | | 0.5 | | % |

Analog Audio Parameters

1. Tested at input gain of 0 dB, $F_{in} = 1\text{KHz}$.
2. Tested at input gain of 0 dB, $F_s=8\text{ KHz}$ and 16KHz .

| Parameter | Symbol | Min | Typ | Max | Units |
|--|-------------|-----|-----|------|-------|
| Analog Audio Input Characteristics | | | | | |
| AIN1-5 Input Impedance | RINX | 10 | | | Kohm |
| Interchannel gain mismatch | | | 0.2 | | dB |
| Input voltage range | | | | 2 | Vpp |
| Full scale input voltage ¹ | V_{iFULL} | | 1 | | Vpp |
| Interchannel isolation ² | | | 90 | | dB |
| Analog Audio Output Characteristics | | | | | |
| AOUT Output Load Resistance | RLAO | 2K | 10K | | ohm |
| AOUT Load Capacitance | CLAO | | 20 | 1000 | pF |
| AOUT Offset Voltage | VOSAO | | | 100 | mV |
| Full scale output voltage ³ | V_{oFULL} | | 2.0 | 2.5 | Vpp |

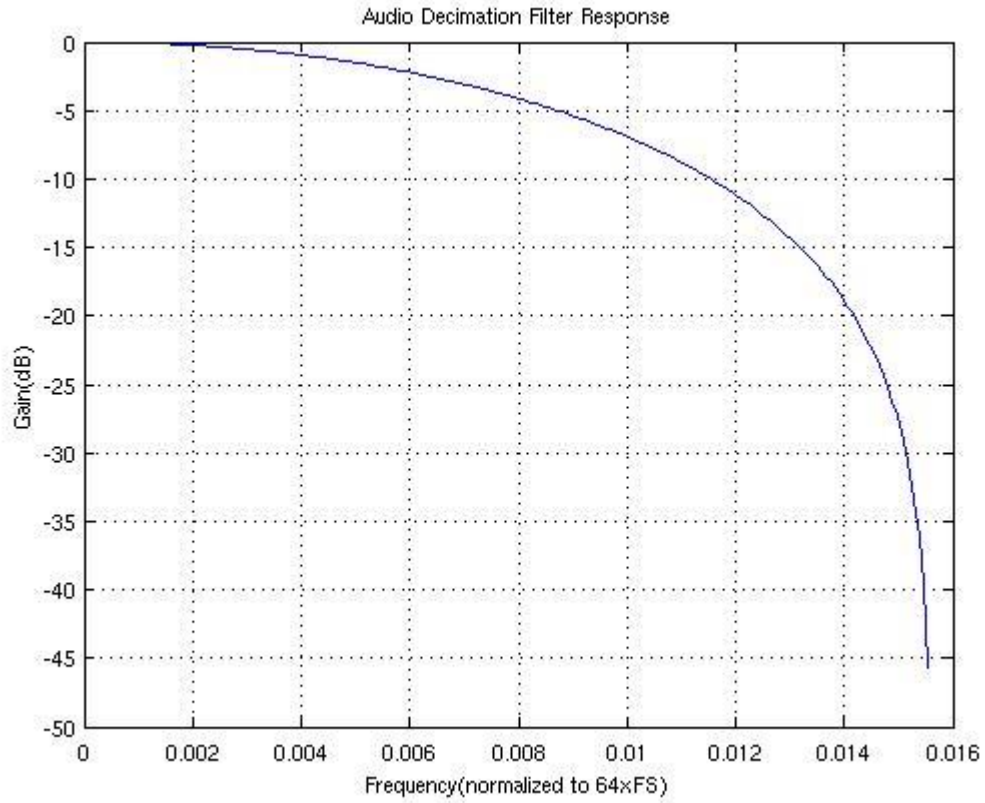
put gain of 0 dB, $F_{out} = 1\text{KHz}$.

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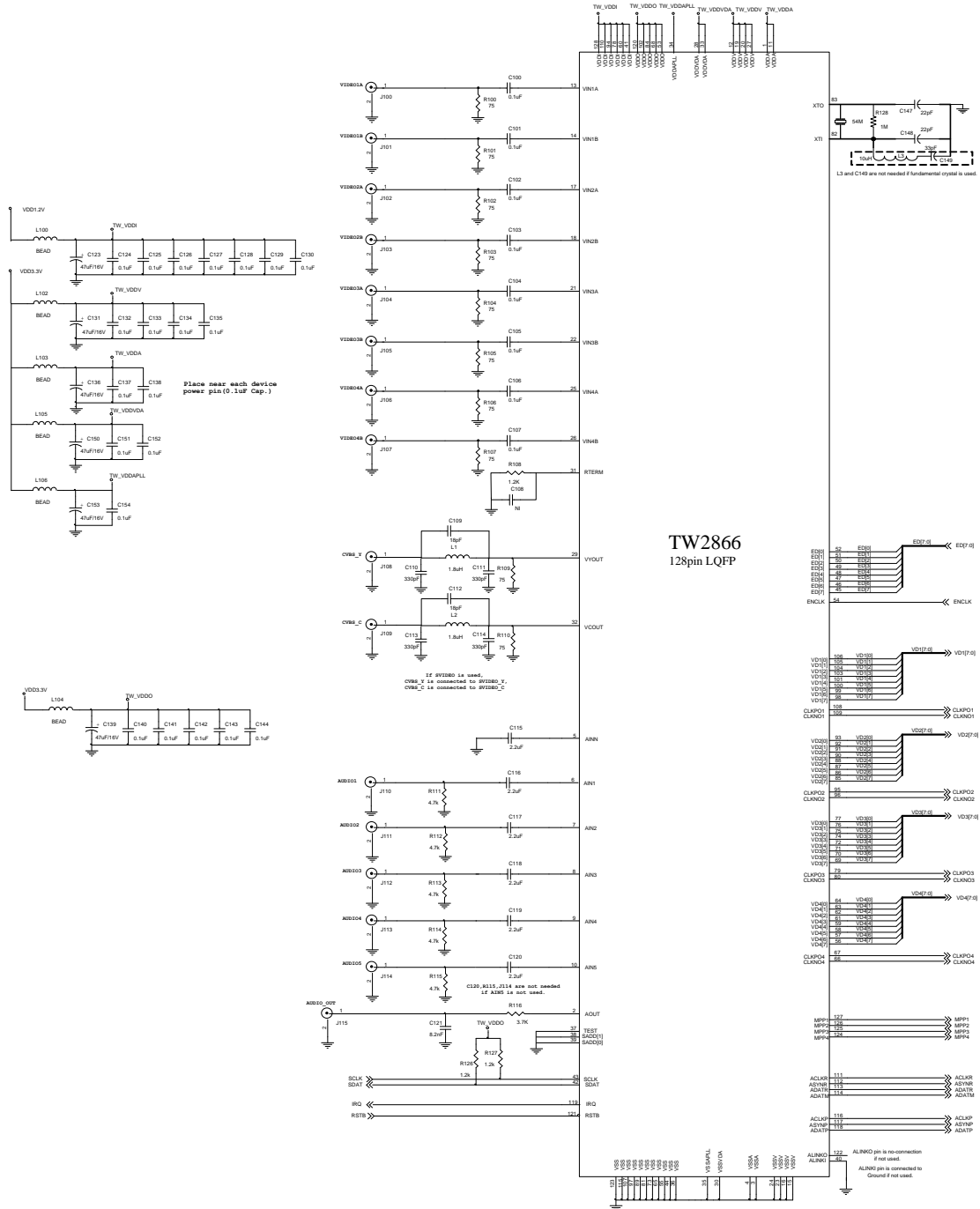
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Audio Decimation Filter Response



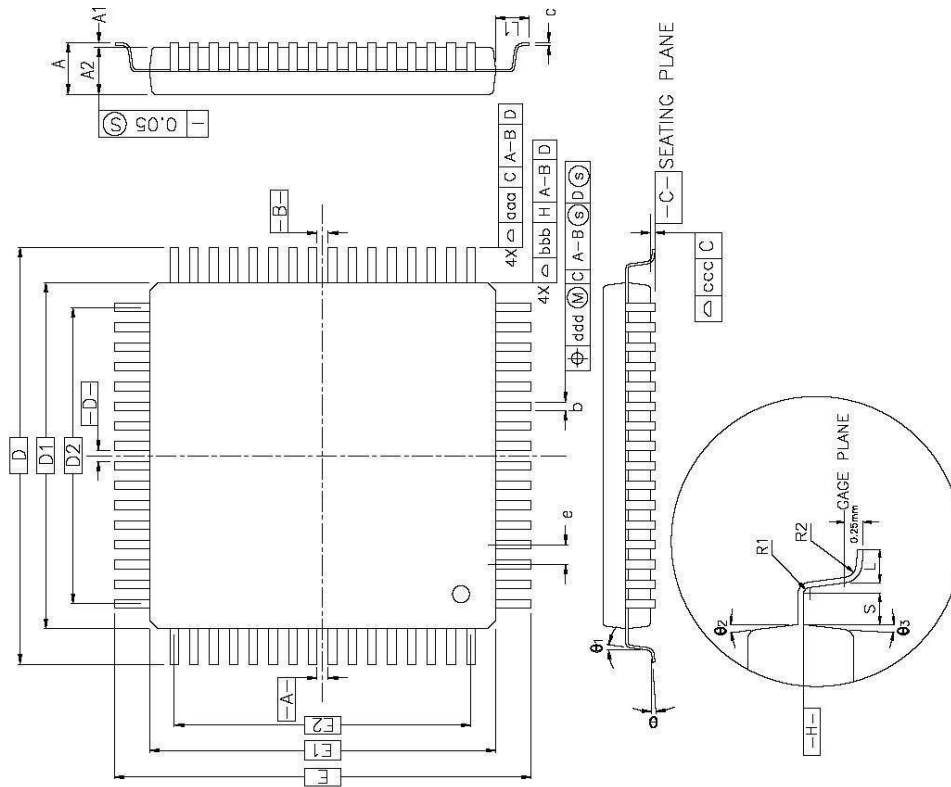
Application Schematic



Package Dimension

CONTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | INCH | |
|----------|-----------------------|-----------|-------|-----------|
| | MIN. | NOM. MAX. | MIN. | NOM. MAX. |
| A | — | 1.60 | — | 0.063 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 1.35 | 1.40 | 0.053 | 0.055 |
| D | 16.00 BSC. 0.630 BSC. | | | |
| D1 | 14.00 BSC. 0.551 BSC. | | | |
| E | 16.00 BSC. 0.630 BSC. | | | |
| E1 | 14.00 BSC. 0.551 BSC. | | | |
| R2 | 0.08 | — | 0.003 | 0.008 |
| R1 | 0.08 | — | 0.003 | — |
| ϕ | 0° | 3.5° | 0° | 3.5° |
| ϕ_1 | 0° | — | 0° | — |
| ϕ_2 | 11° | 12° | 11° | 12° |
| ϕ_3 | 11° | 12° | 11° | 12° |
| c | 0.09 | — | 0.20 | 0.004 |
| L | 0.45 | 0.60 | 0.75 | 0.018 |
| L1 | 1.00 REF. 0.039 REF. | | | |
| S | 0.20 | — | 0.008 | — |



| SYMBOL | 64L | | | 80L | | | 100L | | | 120L | | |
|---------------------------------|--------------------------------|--------------------------|-------|--------------------------------|--------------------------|-------|--------------------------------|--------------------------|-------|--------------------------------|--------------------------|-------|
| | MILLIMETER | INCH | | MILLIMETER | INCH | | MILLIMETER | INCH | | MILLIMETER | INCH | |
| b | MIN. 0.30 MAX. 0.35 0.45 | MIN. 0.012 MAX. 0.014 | 0.018 | MIN. 0.22 MAX. 0.30 0.38 | MIN. 0.009 MAX. 0.012 | 0.015 | MIN. 0.17 MAX. 0.20 0.27 | MIN. 0.007 MAX. 0.008 | 0.011 | MIN. 0.13 MAX. 0.16 0.23 | MIN. 0.005 MAX. 0.006 | 0.009 |
| e | 0.80 BSC. | 0.031 BSC. | | 0.65 BSC. | 0.026 BSC. | | 0.50 BSC. | 0.020 BSC. | | 0.40 BSC. | 0.016 BSC. | |
| D2 | 12.00 | 0.472 | | 12.35 | 0.486 | | 12.00 | 0.472 | | 11.60 | 0.457 | |
| E2 | 12.00 | 0.472 | | 12.35 | 0.486 | | 12.00 | 0.472 | | 11.60 | 0.457 | |
| TOLERANCES OF FORM AND POSITION | | | | | | | | | | | | |
| ccc | 0.20 | 0.008 | | 0.20 | 0.008 | | 0.20 | 0.008 | | 0.20 | 0.008 | |
| bbb | 0.20 | 0.008 | | 0.20 | 0.008 | | 0.20 | 0.008 | | 0.20 | 0.008 | |
| ccc | 0.10 | 0.004 | | 0.10 | 0.004 | | 0.08 | 0.003 | | 0.08 | 0.003 | |
| ddd | 0.20 | 0.008 | | 0.13 | 0.005 | | 0.08 | 0.003 | | 0.07 | 0.003 | |

| SYMBOL | 128L | | |
|--------|--------------------------------|--------------------------|-------|
| | MILLIMETER | INCH | |
| b | MIN. 0.13 MAX. 0.16 0.23 | MIN. 0.005 MAX. 0.006 | 0.009 |
| e | 0.40 BSC. | 0.016 BSC. | |
| D2 | 12.40 | 0.488 | |
| E2 | 12.40 | 0.488 | |
| ccc | 0.20 | 0.008 | |
| bbb | 0.20 | 0.008 | |
| ccc | 0.08 | 0.003 | |
| ddd | 0.07 | 0.003 | |

NOTES :

- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.
- ALL DIMENSION OF 128L WERE BASE ON THOSE OF 120L SINCE THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026.

Datasheet Revision History

| Revision | Date | Description |
|----------|------------|--|
| FN7747.0 | 12/07/2010 | Assigned file number FN7747.0 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. No changes to datasheet content. Removed Techwell disclaimer from page 1. |

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