To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

# MOS FIELD EFFECT POWER TRANSISTORS

Phase-out/Discontinued

# μPA1751

## SWITCHING
## DUAL N-CHANNEL POWER MOS FET
## INDUSTRIAL USE

### DESCRIPTION

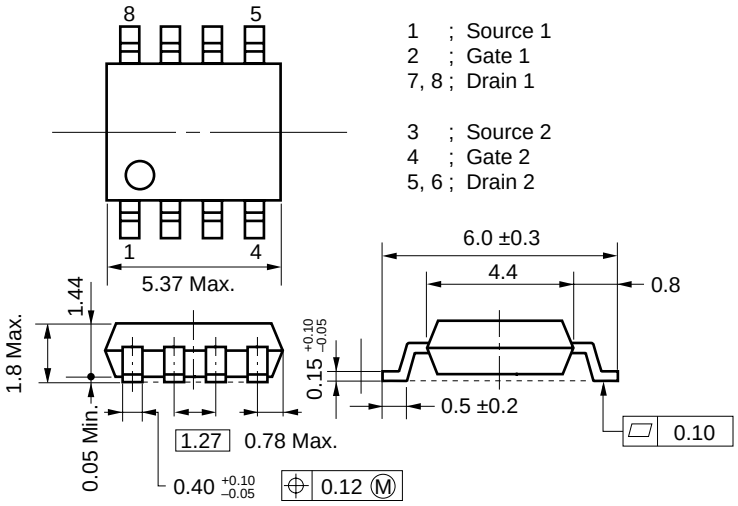
This product is Dual N-Channel MOS Field Effect Transistor designed for power management application of notebook computers, and Li-ion battery application.

### FEATURES

- Dual MOSFET chips in small package
- 4 V Gate Drive Type and Low On-Resistance
  $R_{DS(on)1}$ = 37 mΩ Max. ($V_{GS}$ = 10 V, $I_D$ = 2.5 A)
  $R_{DS(on)2}$ = 64 mΩ Max. ($V_{GS}$ = 4 V, $I_D$ = 2.5 A)
- Low $C_{iss}$ $C_{iss}$ = 510 pF Typ.
- Built-in G-S Protection Diode
- Small and Surface Mount Package
  (Power SOP8)

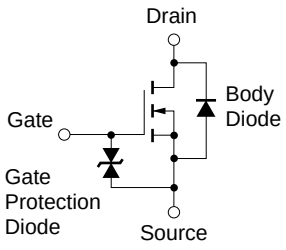
### PACKAGE DIMENSIONS

**(in: millimeter)**




### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, all terminals are connected)

| | | | |
|---|---|---|---|
| Drain to Source Voltage | $V_{DSS}$ | 30 | V |
| Gate to Source Voltage | $V_{GSS}$ | ±20 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ±5.0 | A |
| Drain Current (pulse)* | $I_{D(pulse)}$ | ±20 | A |
| Total Power Dissipation (1 unit)** | $P_T$ | 1.7 | W |
| Total Power Dissipation (2 unit)** | $P_T$ | 2.0 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +150 | °C |




* PW ≤ 10 μs, Duty Cycle ≤ 1 %

** Mounted on ceramic substrate of 2000 $mm^2 \times 1.1$ mm

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.



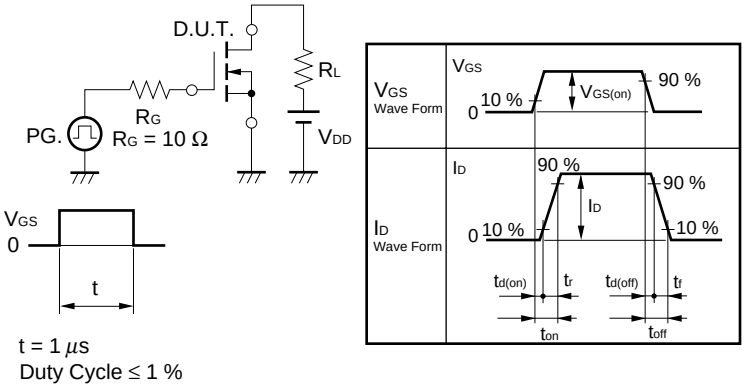
Document No. G10620EJ2V0DS00
Date Published April 1996 P
Printed in Japan

Phase-out/Discontinued

**ELECTRICAL CHARACTERISTICS ($T_A$ = 25 °C, all terminal are connected)**

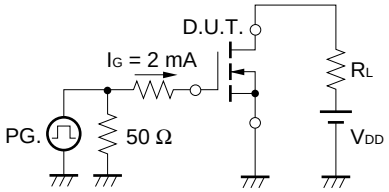
| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain to Source On-state Resistance | $R_{DS(on)1}$ | $V_{GS}$ = 10 V, $I_D$ = 2.5 A | | 27 | 37 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = 4 V, $I_D$ = 2.5 A | | 44 | 64 | mΩ |
| Gate to Source Cutoff Voltage | $V_{GS(off)}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 1.0 | 1.5 | 2.0 | V |
| Forward Transfer Admittance | $\|y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 2.5 A | 3.0 | 6.0 | | S |
| Drain Leakage Current | $I_{DSS}$ | $V_{DS}$ = 30 V, $V_{GS}$ = 0 | | | 10 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 | | | ±10 | μA |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V<br>$V_{GS}$ = 0<br>f = 1 MHz | | 510 | | pF |
| Output Capacitance | $C_{oss}$ | | | 350 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 150 | | pF |
| Turn-On Delay Time | $t_{d(on)}$ | $I_D$ = 2.5 A<br>$V_{GS(on)}$ = 10 V<br>$V_{DD}$ = 15 V<br>$R_G$ = 10 Ω | | 10 | | ns |
| Rise Time | $t_r$ | | | 95 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | | | 120 | | ns |
| Fall Time | $t_f$ | | | 100 | | ns |
| Total Gate Charge | $Q_G$ | $I_D$ = 5.0 A<br>$V_{DD}$ = 24 V<br>$V_{GS}$ = 10 V | | 19 | | nC |
| Gate to Source Charge | $Q_{GS}$ | | | 1.5 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | | | 6.6 | | nC |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | $I_F$ = 5.0 A, $V_{GS}$ = 0 | | 0.8 | | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 5.0 A, $V_{GS}$ = 0<br>di/dt = 100 A/μs | | 85 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | | | 90 | | nC |

**Test Circuit 1 Switching Time**

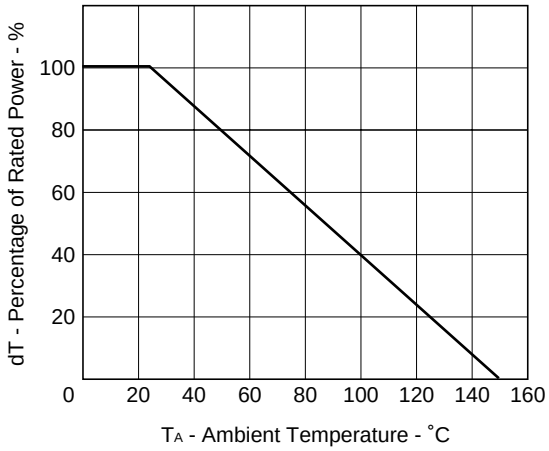



t = 1 μs
Duty Cycle ≤ 1 %

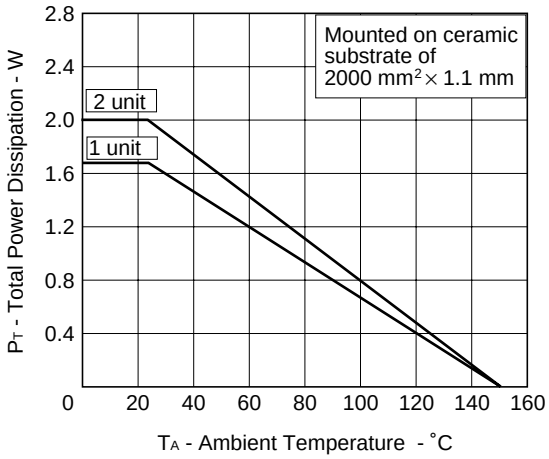
**Test Circuit 2 Gate Charge**



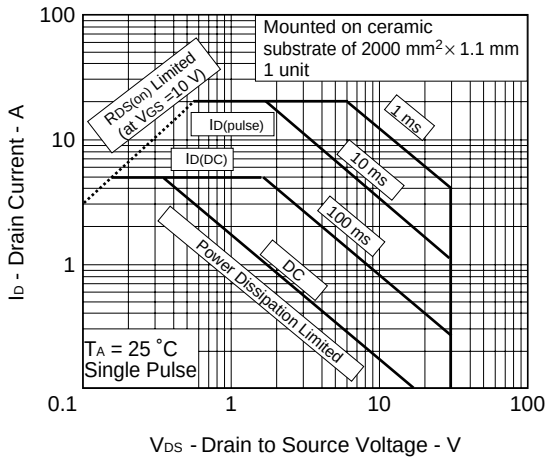
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



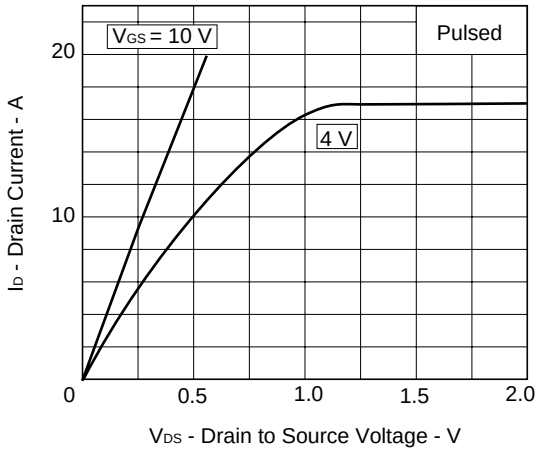

TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



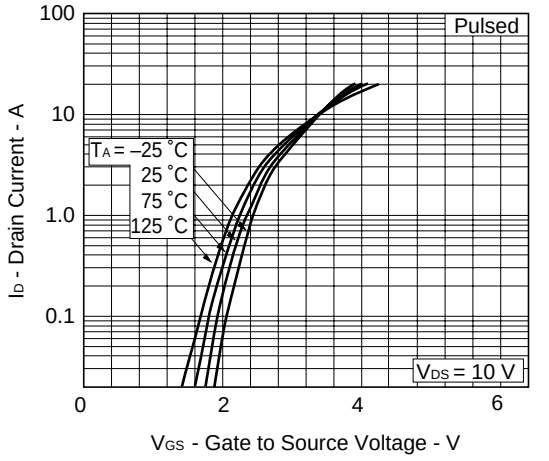

FORWARD BIAS SAFE OPERATING AREA



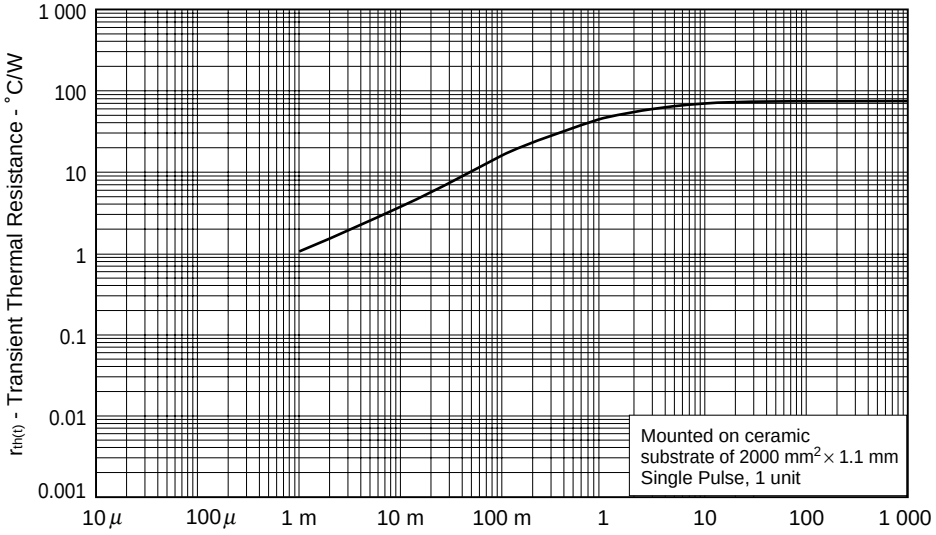

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



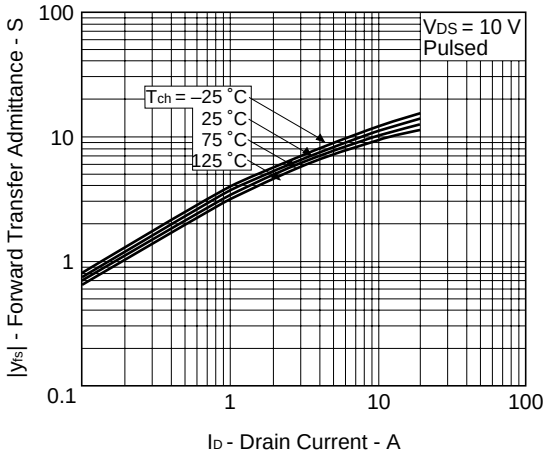

FORWARD TRANSFER CHARACTERISTICS



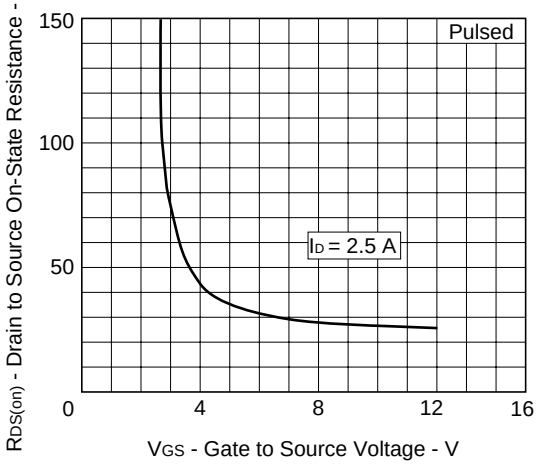
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



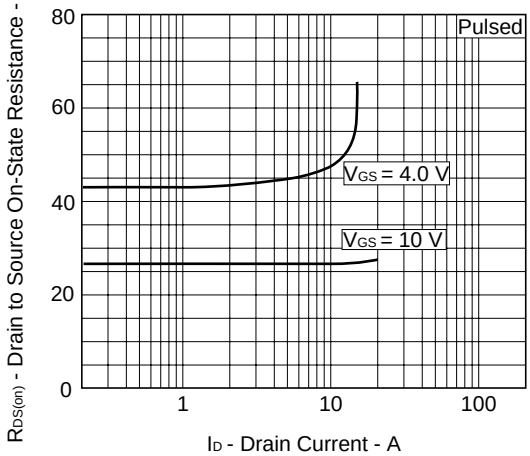

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



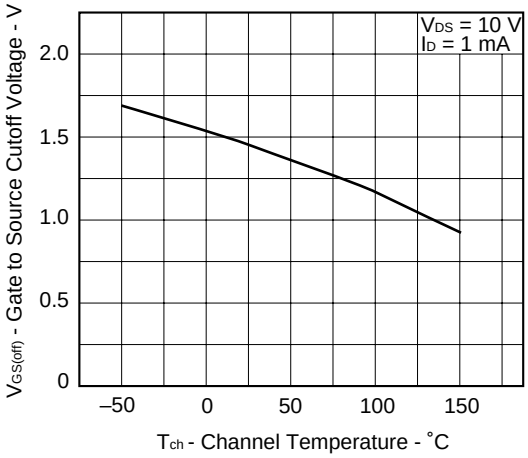

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



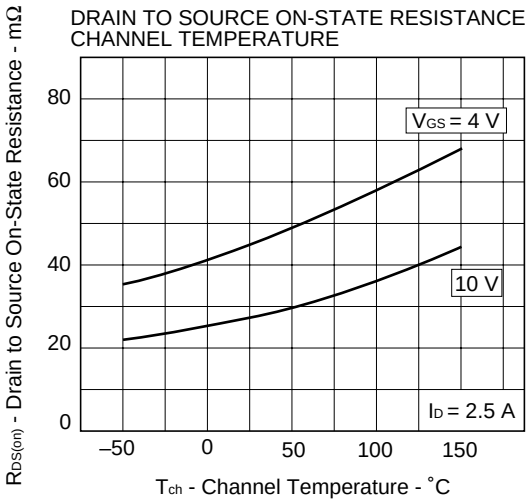

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



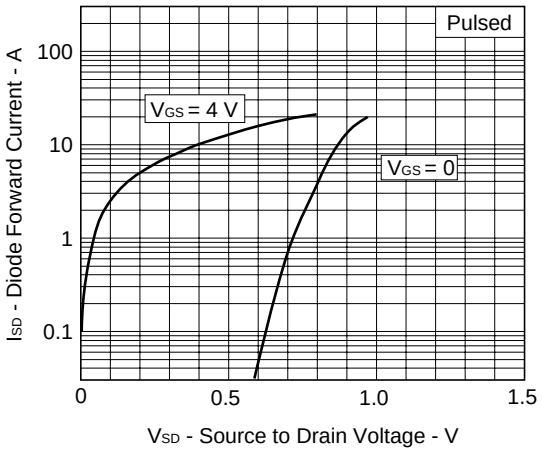

GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



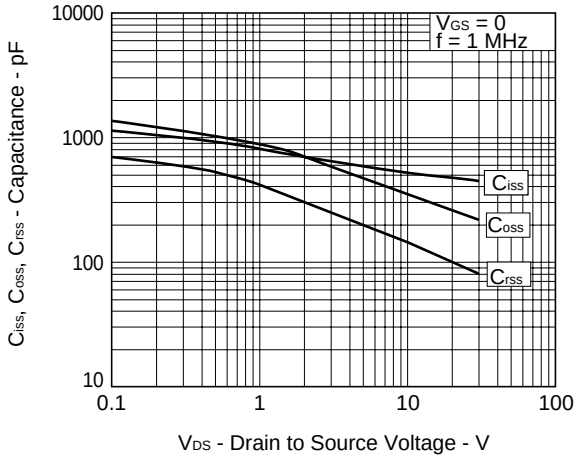
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



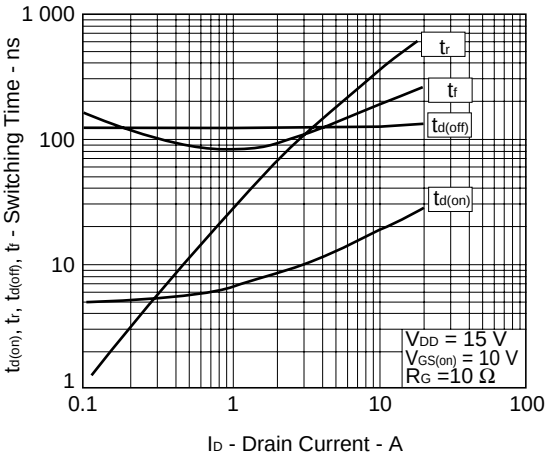

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



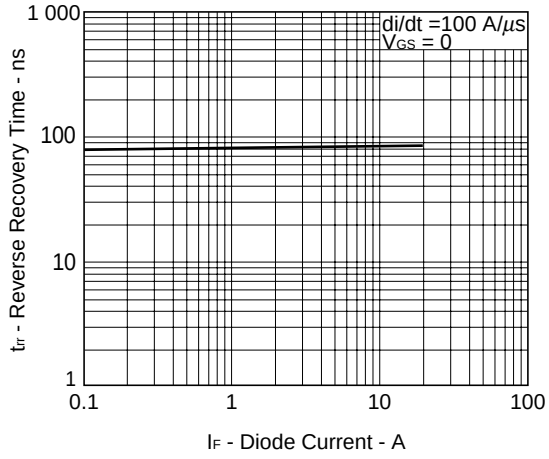

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



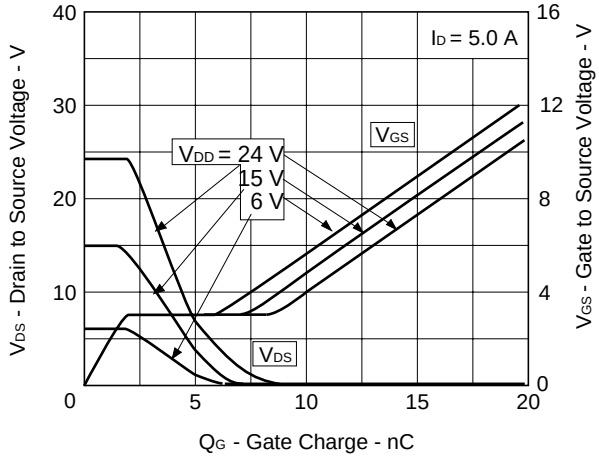

SWITCHING CHARACTERISTICS




REVERSE RECOVERY TIME vs. BODY DIODE CURRENT




DYNAMIC INPUT/OUTPUT CHARACTERISTICS



## REFERENCE

| Document Name | Document No. |
|---|---|
| NEC semiconductor device reliability/quality control system | TEI-1202 |
| Quality grade on NEC semiconductor devices | IEI-1209 |
| Semiconductor device mounting technology manual | C10535E |
| Semiconductor device package manual | C10943X |
| Guide to quality assurance for semiconductor devices | MEI-1202 |
| Semiconductor selection guide | X10679E |
| Power MOS FET features and application switching power supply | TEA-1034 |
| Application circuits using Power MOS FET | TEA-1035 |
| Safe operating area of Power MOS FET | TEA-1037 |

[MEMO]

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