To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR

μPA1774

SWITCHING
DUAL P-CHANNEL POWER MOS FET

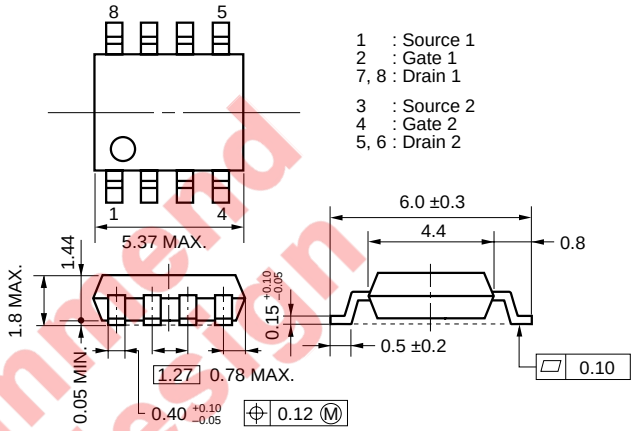
DESCRIPTION

The μPA1774 is Dual P-channel MOS Field Effect Transistor.

FEATURES

- Dual chip type
- Low on-state resistance
  $R_{DS(on)1}$ = 250 mΩ MAX. (V_{GS} = –10 V, I_D = –2.0 A)
  $R_{DS(on)2}$ = 300 mΩ MAX. (V_{GS} = –4.5 V, I_D = –2.0 A)
  $R_{DS(on)3}$ = 330 mΩ MAX. (V_{GS} = –4.0 V, I_D = –2.0 A)
- Low input capacitance
  C_{iss} = 420 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit: mm)



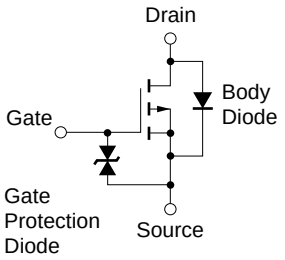
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1774G	Power SOP8

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	∓2.8	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	∓18	A
Total Power Dissipation (1 unit) Note2	P_T	0.6	W
Total Power Dissipation (2 unit) Note2	P_T	0.8	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to 150	°C
Single Avalanche Current Note3	I_{AS}	–2.8	A
Single Avalanche Energy Note3	E_{AS}	0.78	mJ

EQUIVALENT CIRCUIT (1/2 circuit)



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on Glass Epoxy Board of 1600 mm^2 x 1.6 mm. Drain pad size: 264 mm^2 x 35 μm, T_A = 25°C

3. Starting T_{ch} = 25°C, V_{DD} = –30 V, R_G = 25 Ω, V_{GS} = –20→0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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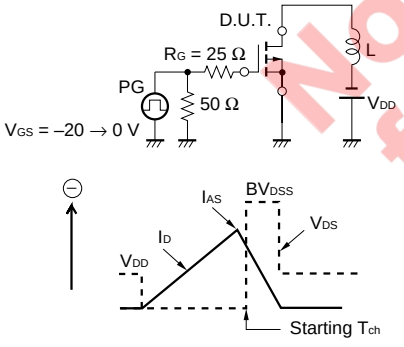
Date Published June 2002 NS CP(K)
Printed in Japan

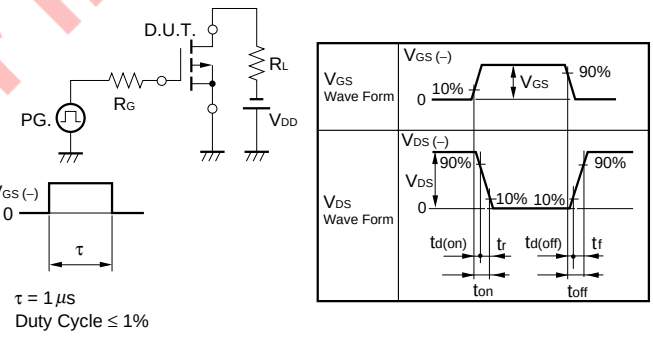
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –60 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓16 V, V_{DS} = 0 V			∓10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = 1 mA	–1.5	–2.0	–2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –2.0 A	2.5	4.3		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –2.0 A		200	250	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –2.0 A		230	300	mΩ
	$R_{DS(on)3}$	V_{GS} = –4.0 V, I_D = –2.0 A		240	330	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		420		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		80		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		30		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –30 V, I_D = –2.0 A		8		ns
Rise Time	t_r	V_{GS} = –10 V		5		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		35		ns
Fall Time	t_f			8		ns
Total Gate Charge	Q_G	V_{DD} = –48 V		10		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –10 V		1.7		nC
Gate to Drain Charge	Q_{GD}	I_D = –2.8 A		2.2		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 2.8 A, V_{GS} = 0 V		0.89		V
Reverse Recovery Time	t_{rr}	I_F = 2.8 A, V_{GS} = 0 V		45		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		65		μC

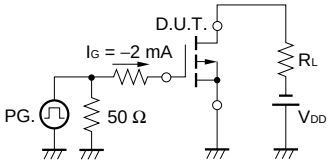
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

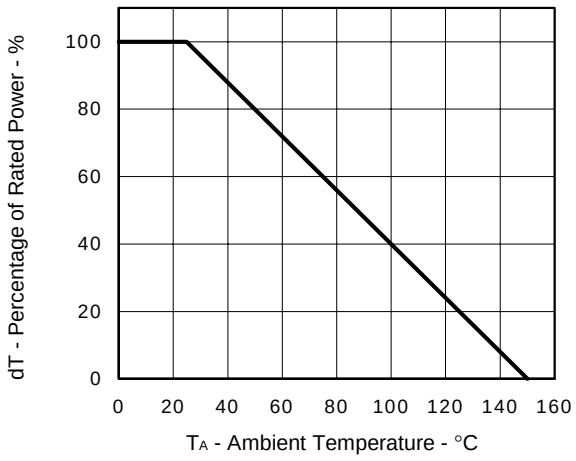


TEST CIRCUIT 3 GATE CHARGE

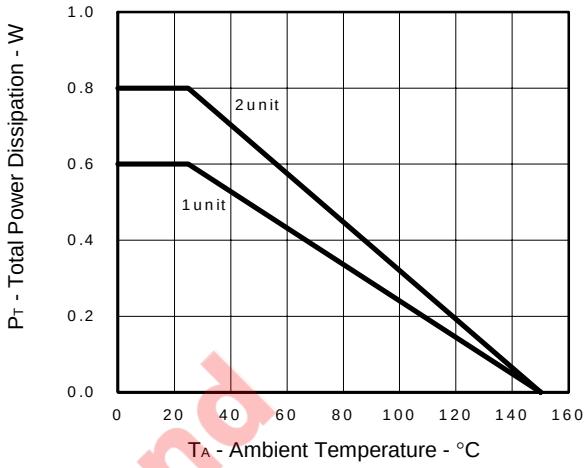


TYPICAL CHARACTERISTICS (T_A = 25°C)

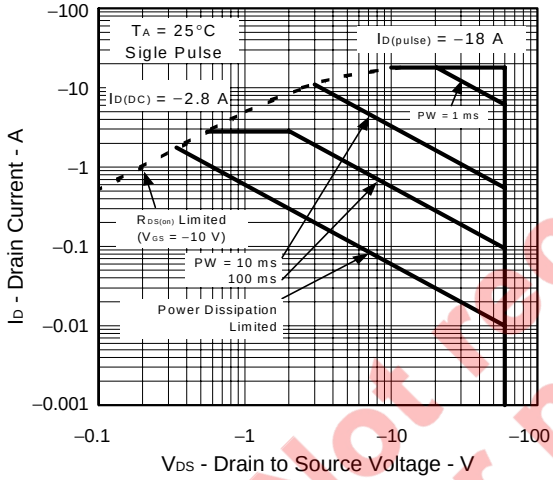
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



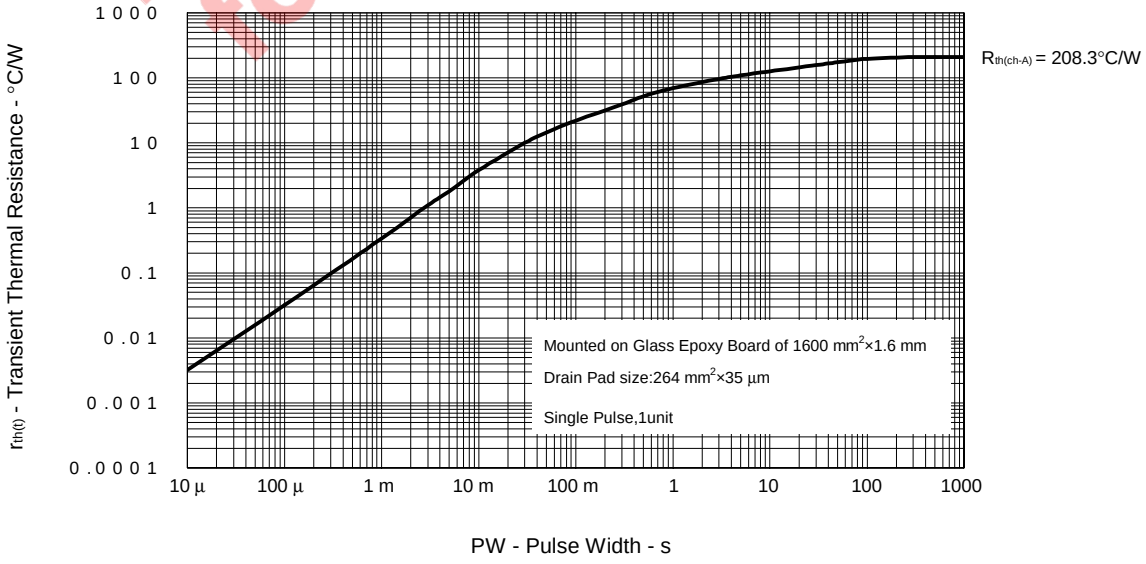
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



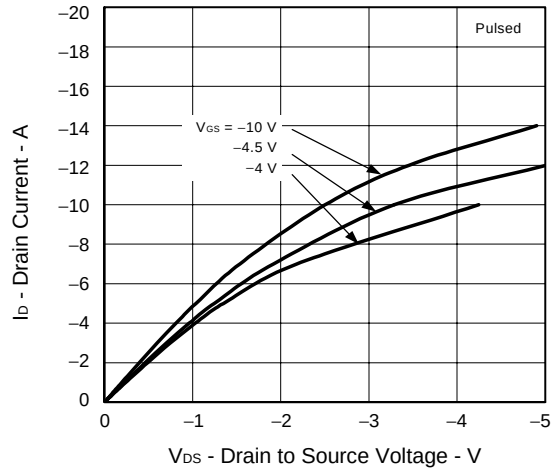
FORWARD BIAS SAFE OPERATING AREA



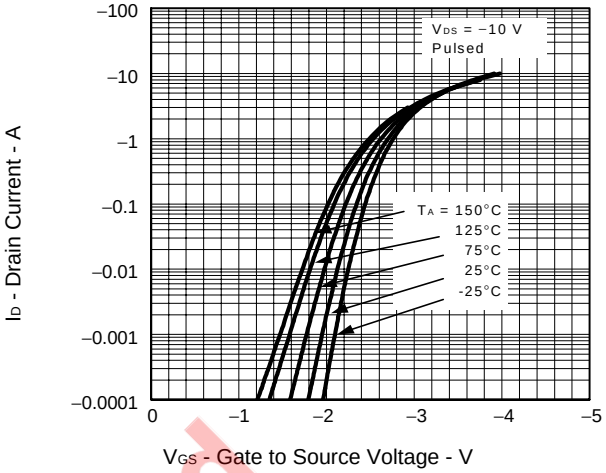
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



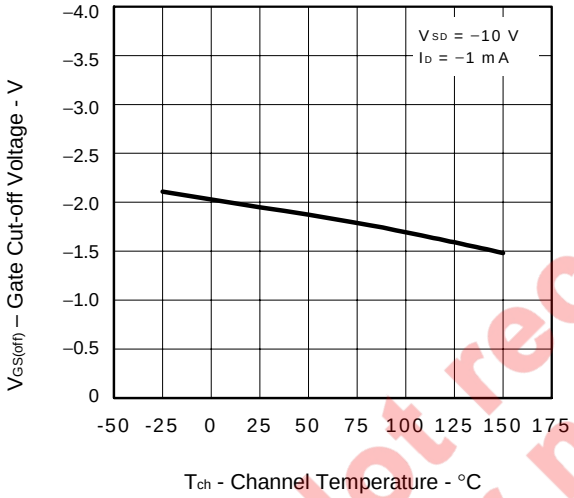
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



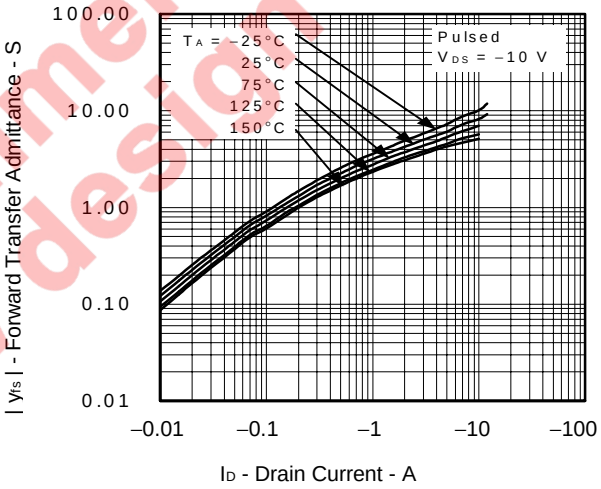
FORWARD TRANSFER CHARACTERISTICS



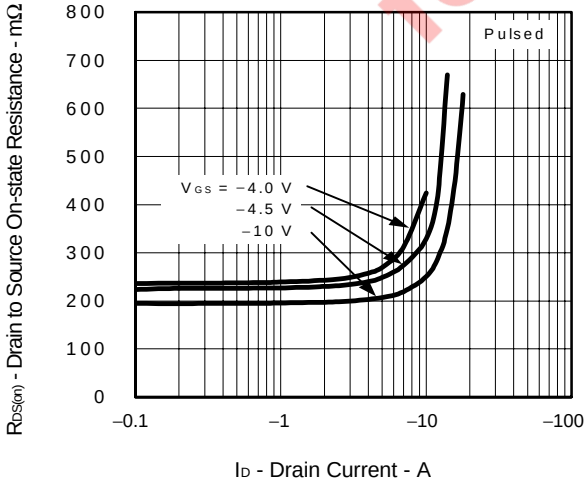
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



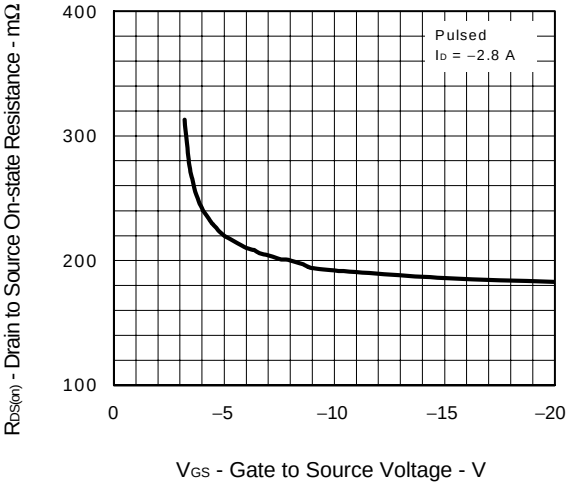
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



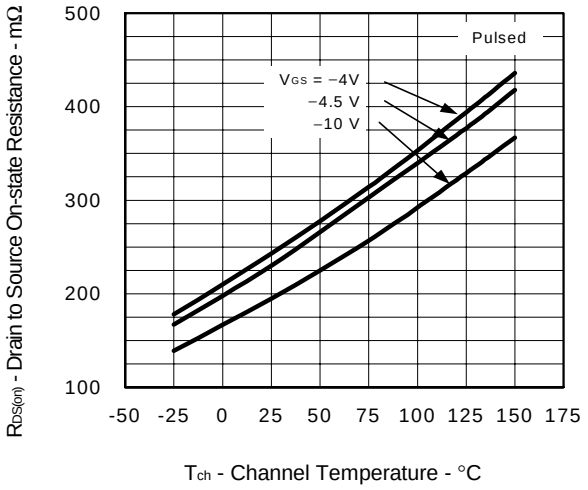
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



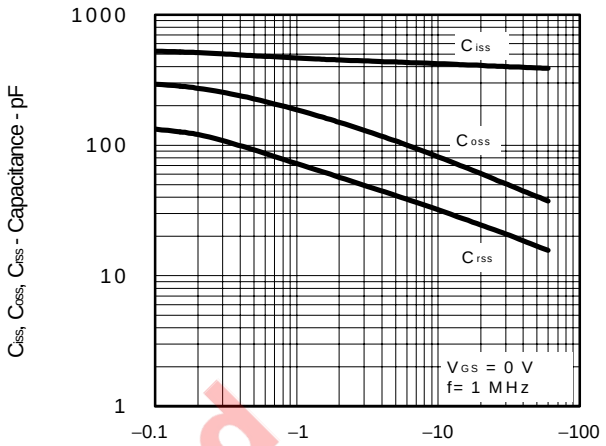
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



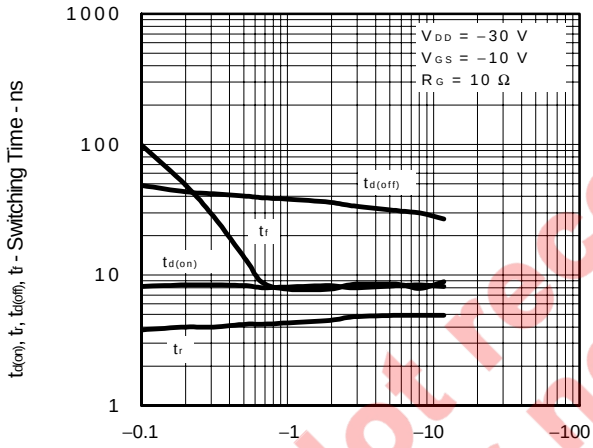
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



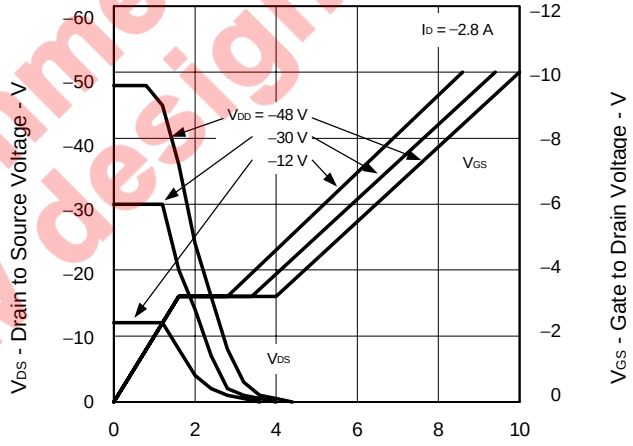
CAPACITANCE vs.
DRAIN TO SOURCE VOLTAGE



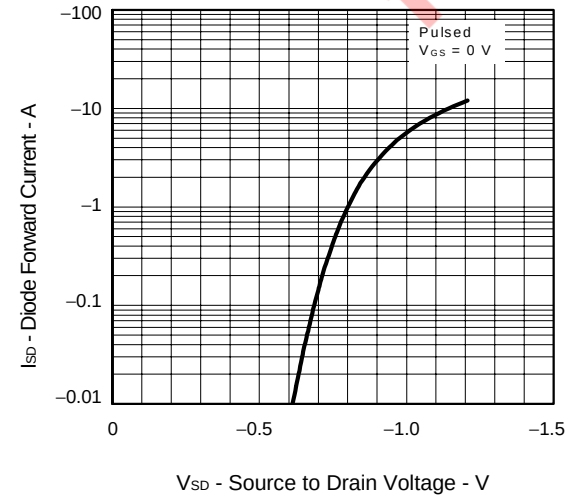
SWITCHING CHARACTERISTICS



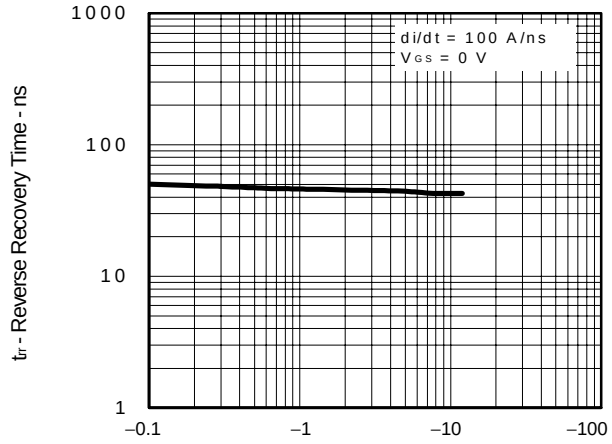
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



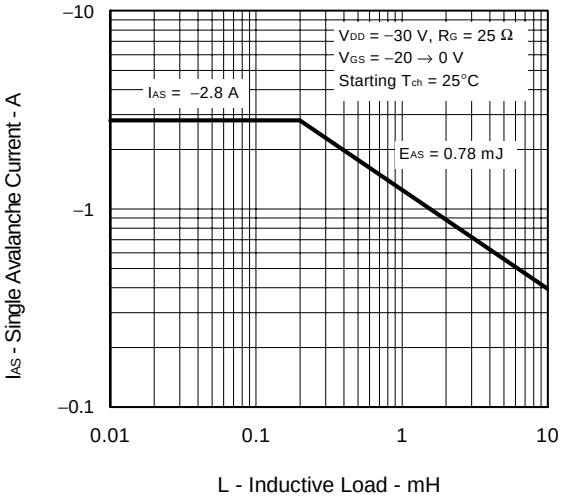
SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



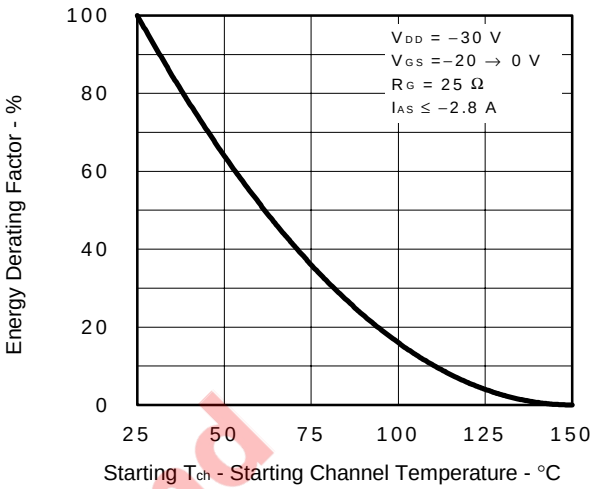
REVERSE RECOVERY TIME vs. DRAIN CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY
DERATING FACTOR



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