

UPC451A

Single Power Supply Quad Operational Amplifiers

DESCRIPTION

UPC451A is a quad operational amplifier designed for single power supply operation. Main features include low-voltage operation, a common-mode input voltage that range from V^- (GND) level, an output from a V^- (GND) level that is determined by the output stage utilizing class C push-pull circuit with 50 μ A(TYP.) constant current, and low current consumption.

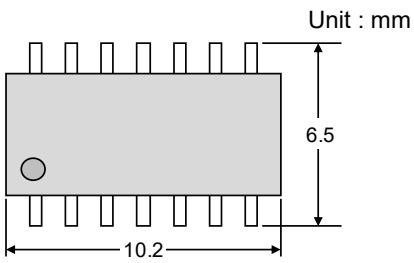
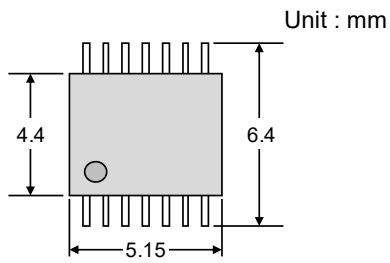
In addition, this amplifier supports both positive and negative power supply and can be used in various amplifier circuits.

UPC1251A which is a dual type with the same circuit configuration is also available under this series of operational amplifiers.

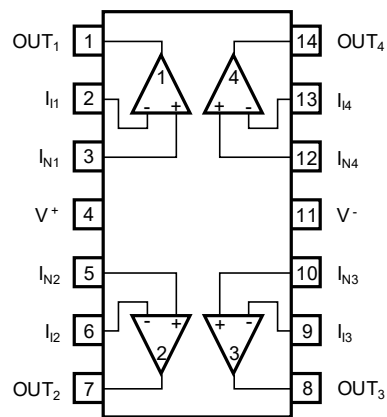
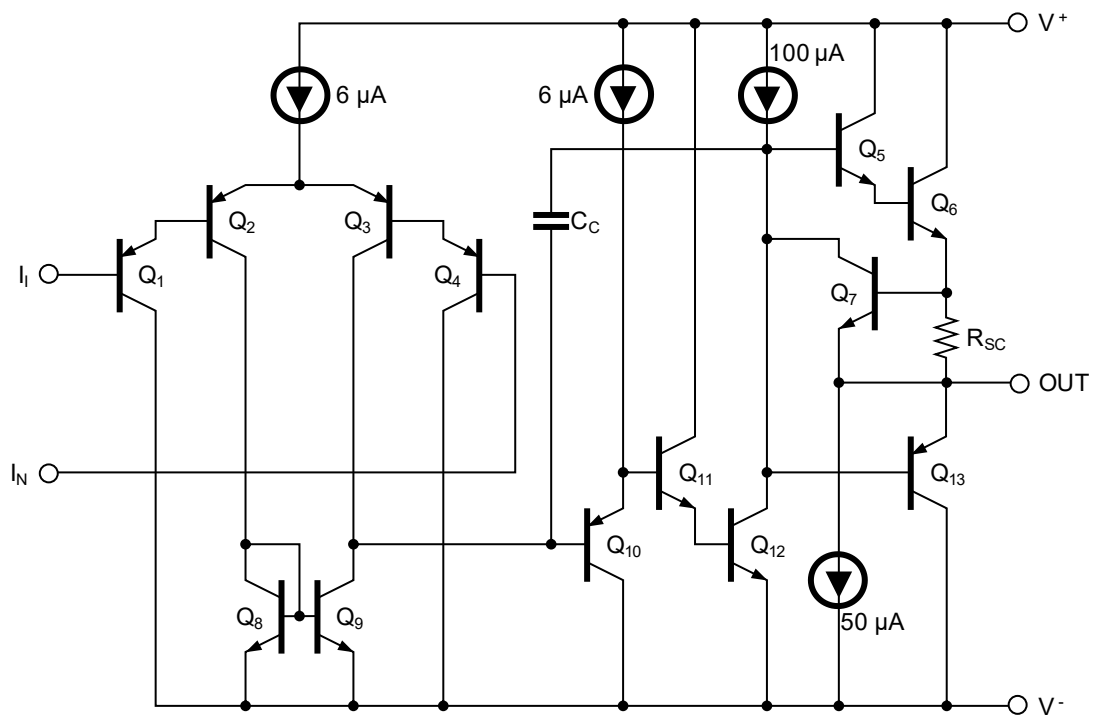
FEATURES

- AEC-Q100 Compliance
- Input Offset Voltage ± 2 mV (TYP.)
- Input Offset Current ± 5 nA (TYP.)
- Large Signal Voltage Gain 100000 (TYP.)
- Internal Frequency Compensation
- Output Short-Circuit Protection

PRODUCT LINEUP

Package	Standard SOP	TSSOP
Subject Part Number (1)	UPC451AG2(20)-AX	UPC451AGR(20)-9LG-A
Outline Comparison		

- (1) Subject Part Number containing E1 or E2 indicate that the packaging format is embossed tapping.
Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

PIN CONFIGURATION (Marking side)**EQUIVALENT CIRCUIT (1/4 Circuit)**

ABSOLUTE MAXIMUM RATINGS

(T_A = 25 °C)

Parameter	Symbol	Ratings	Unit
Voltage between V ⁺ and V ⁻ Note 1	V ⁺ - V ⁻	-0.3 ~ +32	V
Differential Input Voltage	V _{ID}	±32	V
Input Voltage Note 2	V _I	V ⁻ -0.3 ~ V ⁻ +32	V
Output applied Voltage Note 3	V _O	V ⁻ -0.3 ~ V ⁺ +0.3	V
Total Power Dissipation Note 4	P _T	550	mW
Output Short Circuit Duration Note 5	t _s	Indefinite	s
Operating Ambient Temperature	T _A	-40 ~ +125	°C
Storage Temperature	T _{stg}	-55 ~ +150	°C

- [Note]**
- Note that reverse connections of the power supply may damage the ICs.
 - The input voltage range that can be applied to the input terminal without deterioration or destruction of characteristics. It can be applied regardless of the power supply voltage as long as it is within the rating. Either input signal is not allowed to go negative by more than 0.3 V. In addition, the input voltage that operates normally as an operational amplifier is within the Common Mode Input Voltage range of an electrical characteristic.
 - A range where input voltage can be applied to an output pin externally with no deterioration or damage to the feature (characteristic). The input voltage can be applied regardless of the electric supply voltage. This specification which includes the transition state such as electric power ON/OFF must be kept.
 - This is the value when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted.
Note that restrictions will be made to the following conditions for each product, and the derating ratio depending on the operating ambient temperature.
UPC451AG2(20) : Derate at -5.5 mW/°C when T_A > 25 °C
UPC451AGR(20) : Derate at -7.0 mW/°C when T_A > 71 °C
 - Short circuits from the output to V⁺ can cause destruction. (V⁺ ≤ +15V, for any one channel only) Pay careful attention to the total power dissipation by not exceeding the absolute maximum ratings, **Note 4**.

RECOMMENDED OPERATING CONDITIONS

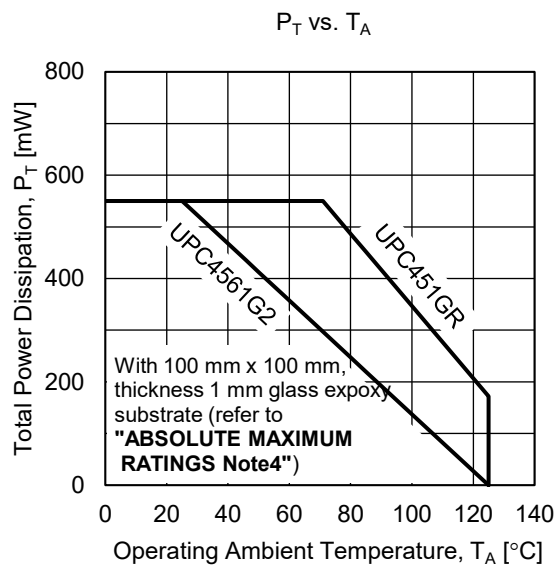
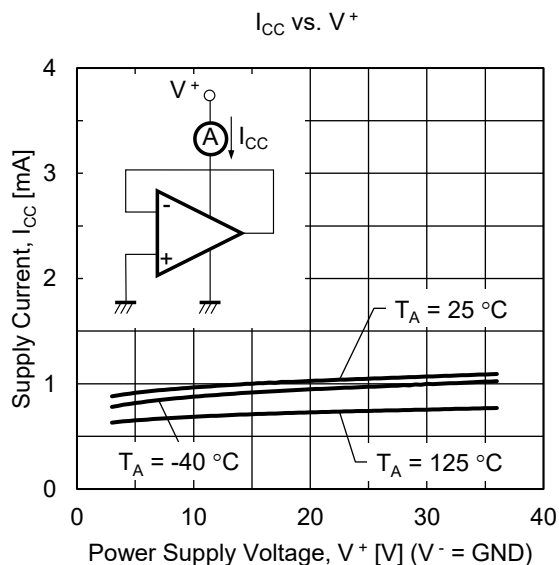
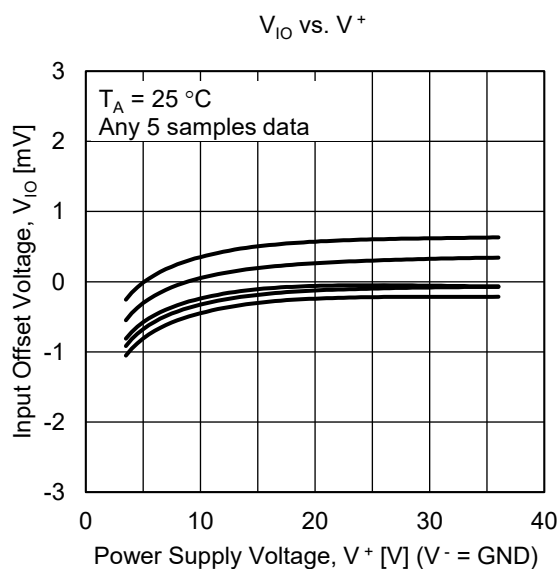
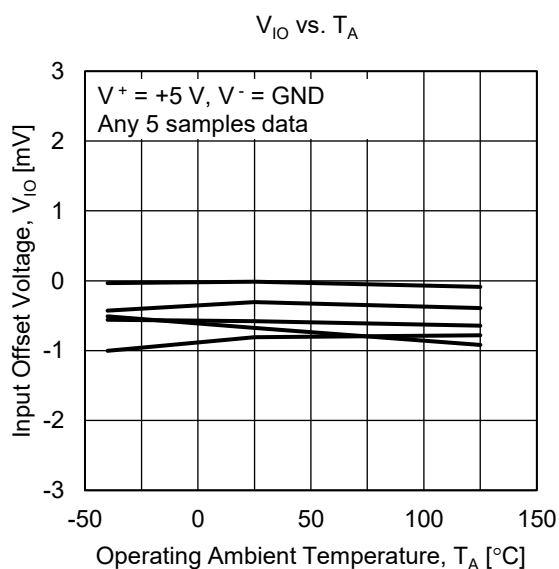
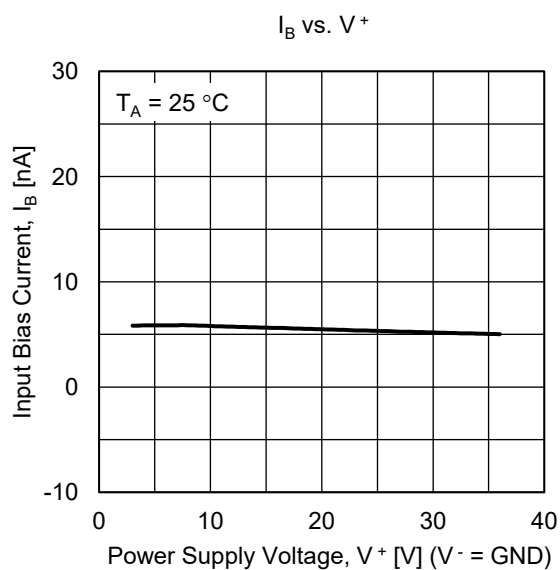
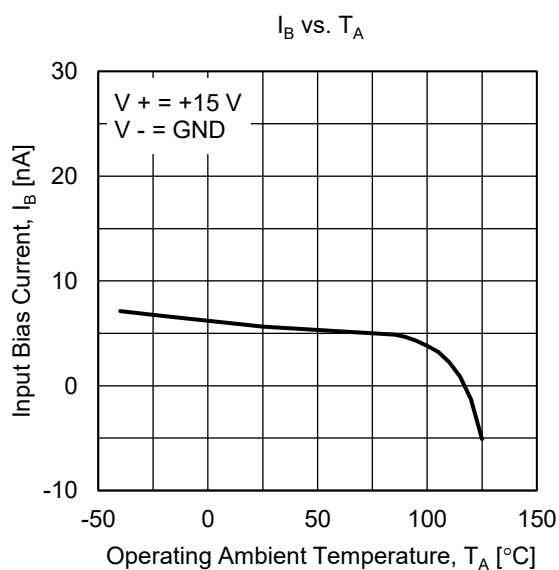
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (Dual)	$V^{\pm}$	± 1.5		± 15	V
Power Supply Voltage ($V^- = \text{GND}$)	V^+	+3		+30	V

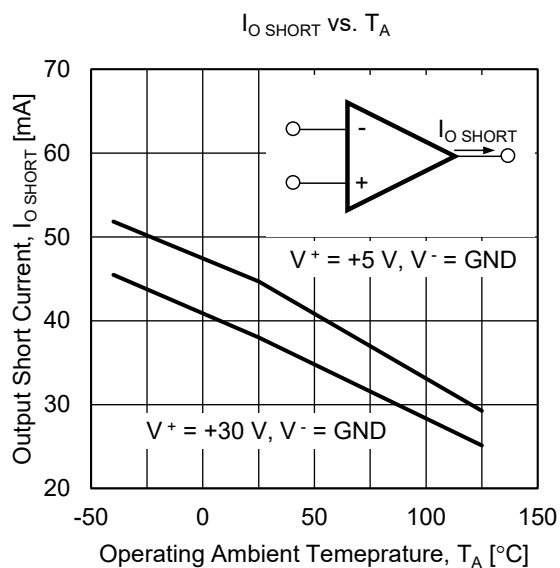
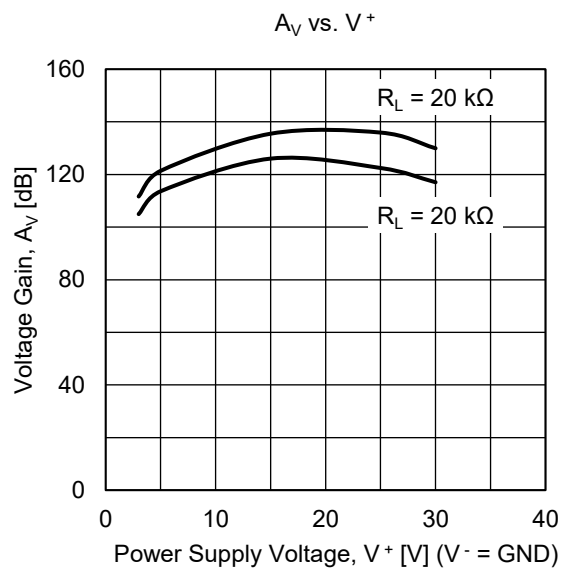
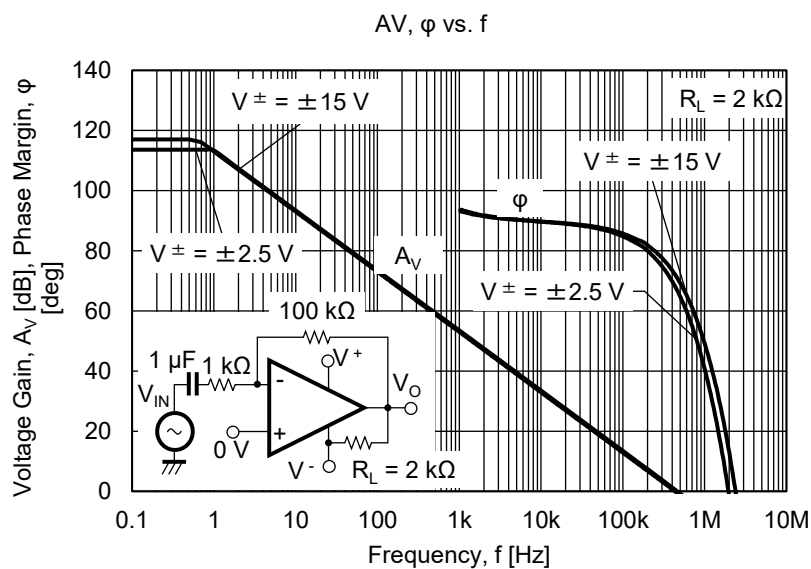
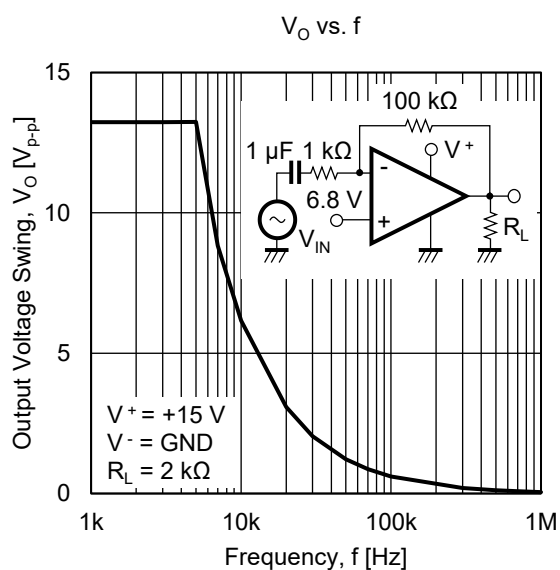
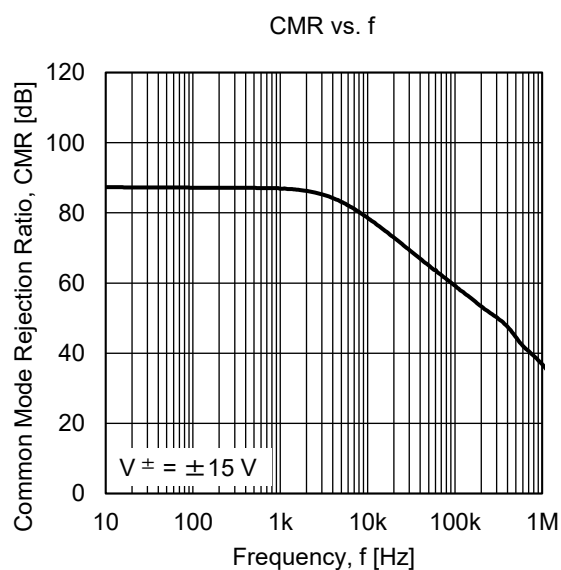
ELECTRICAL CHARACTERISTICS(T_A = 25 °C, V⁺ = +5 V, V⁻ = GND)

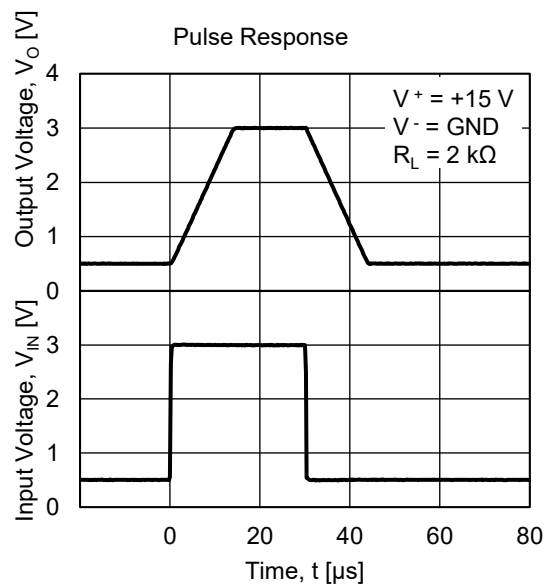
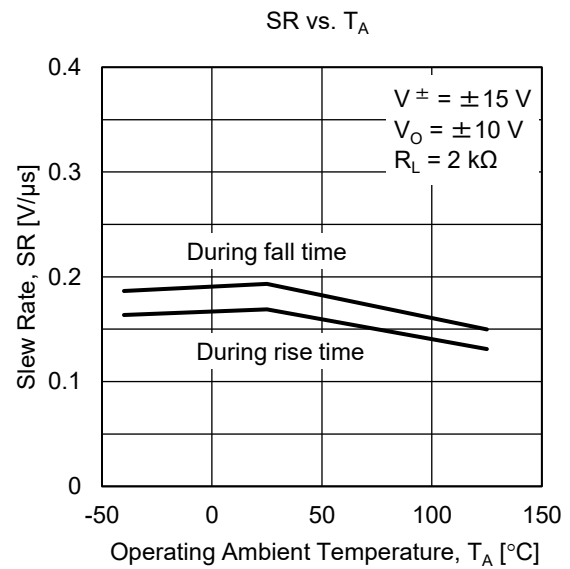
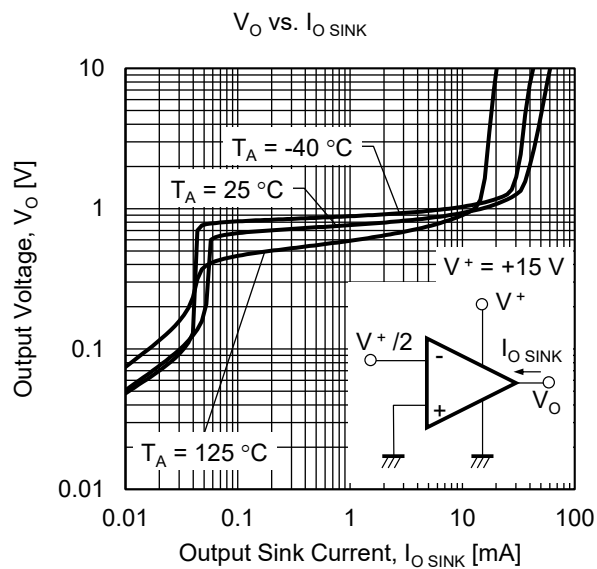
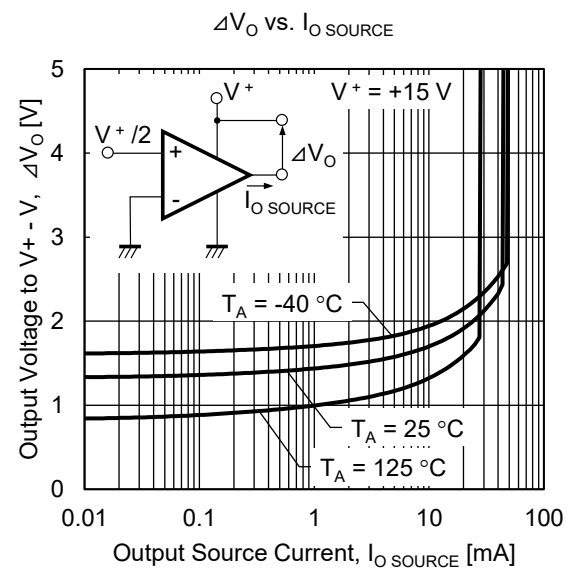
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V _{IO}		±2	±7	mV	R _S = 0 Ω
Input Offset Current	I _{IO}		±5	±50	nA	
Input Bias Current ^{Note 6}	I _B		26	250	nA	
Large Signal Voltage Gain	A _V	25000	100000			R _L ≥ 2 kΩ
Circuit Current ^{Note 7}	I _{CC}		1.0	2.0	mA	R _L = ∞, I _O = 0 A
Common Mode Rejection Ratio	CMR	65	85		dB	
Supply Voltage Rejection Ratio	SVR	65	100		dB	
Output Voltage Swing	V _O	0		V ⁺ -1.5	V	R _L = 2 kΩ (Connected to GND)
Common Mode Input Voltage Range	V _{ICM}	0		V ⁺ -1.5	V	
Output Source Current	I _{O SOURCE}	20	40		mA	V _{IN (+)} = +1 V, V _{IN (-)} = 0 V
Output Sink Current	I _{O SINK1}	10	20		mA	V _{IN (-)} = +1 V, V _{IN (+)} = 0 V
	I _{O SINK2}	12	50		μA	V _{IN (-)} = +1 V, V _{IN (+)} = 0 V, V _O = 200 mV
Channel Separation			120		dB	f = 1 ~ 20 kHz

【Note】 6. The absolute value of the input bias current is small, thus the direction of the current flowing from the inside of the IC may be reversed due to variations in the product during high temperature.

7. This is a current that flows in the internal circuit. This current will flow irrespective of the channel used.

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, TYP.) (Reference value)



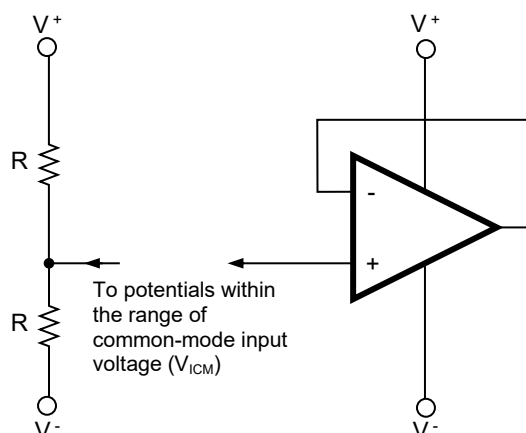


PRECAUTIONS

- **The process of unused circuits**

If there is an unused circuit, the following connection is recommended.

Process example of unused circuits



Remark A midpoint potential of V^+ and V^- is applied to this example.

- **Ratings of input/output pin voltage**

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than V^- , or the output pin exceeds the power supply voltage, it is recommended to make a clamp circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Range of common-mode input voltage**

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

$$V_{ICM} \text{ (TYP.): } V^- \text{ to } V^+ - 1.5 \text{ [V] (} T_A = 25^\circ\text{C).}$$

During designing, do include some tolerance by considering temperature characteristics and etc.

- **Maximum output voltage**

The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

$$V_{om}^+ \text{ (TYP.): } V^+ - 1.5 \text{ [V] (} T_A = 25^\circ\text{C), } V_{om}^- \text{ (TYP.): (} I_{o \text{ SINK}} \leq 50 \mu\text{A): Approx. } V^- \text{ [V] (} T_A = 25^\circ\text{C)}$$

During designing, include some tolerance such as characteristics variation and temperature characteristics consideration and so forth. In addition, also note that the output voltage range ($V_{om}^+ - V_{om}^-$) will become narrow when an output current increases.

- **Operation of output**

This IC output level consist of a class C push-pull. Therefore, when a load resistance is connected to the midpoint potential of V^+ , V^- , a crossover distortion occurs during the transition state of output current flow direction (source, sink).

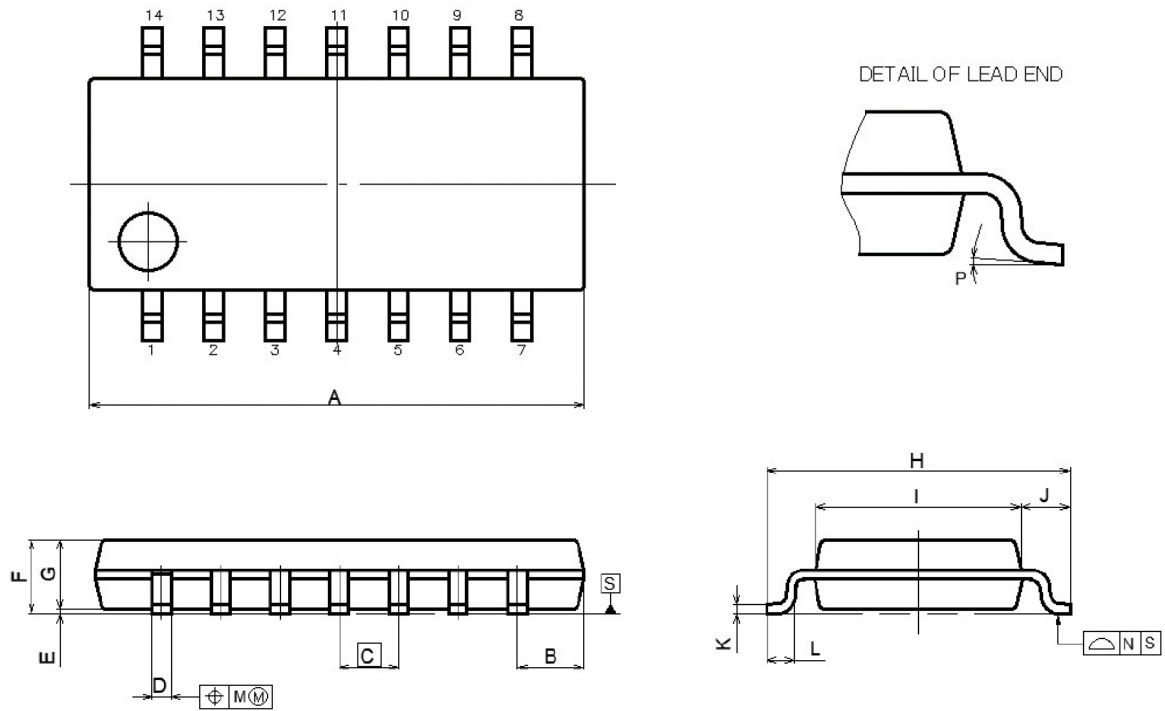
- **Handling of ICs**

Warpage or bending of a PCB board will apply stress to the ICs, the characteristic may change due to piezoelectric effect. Therefore, pay attention to warpage or bending of the board.

PACKAGE DRAWINGS

14-Pin PLASTIC SOP

JEITA Package code	RENESAS code	MASS (TYP.) [g]
P-LSOP14-4.4×10.2-1.27	PLSP0014DB-A	0.17[g]

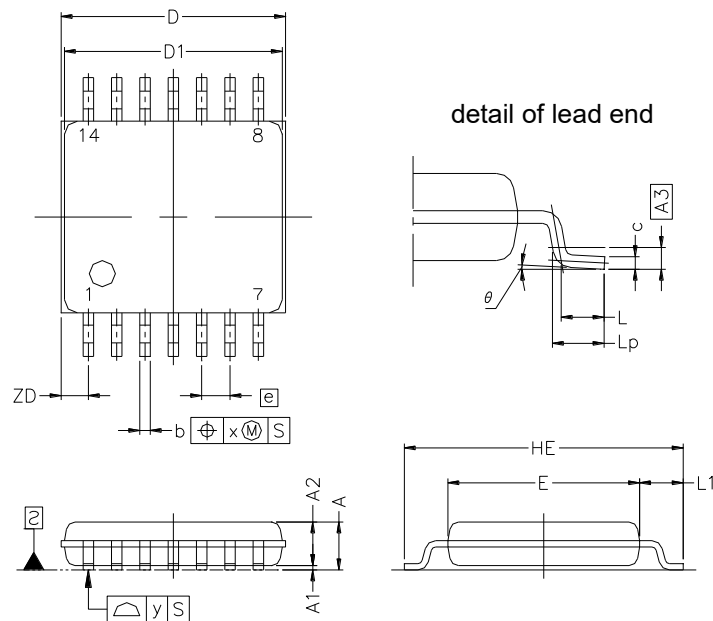


NOTE
EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)	
ITEM	DIMENSIONS
A	10.2±0.2
B	1.42MAX
C	1.27(T.P)
D	0.40±0.05
E	0.1±0.1
F	1.59±0.20
G	1.49±0.1
H	6.5±0.2
I	4.4±0.1
J	1.05±0.15
K	0.2±0.07
L	0.6±0.20
M	0.1MAX
N	0.1MAX
P	4°±4°

14-Pin PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.) [g]
P-TSSOP14-0225-0.65	PTSP0014JB-A	P14GR-65-9LG-1	—



Unit : mm

NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

ITEM	MILLIMETERS
D	5.15 ±0.15
D1	5.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 ^{+0.06} _{-0.05}
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° ^{+5°} _{-3°}
e	0.65
x	0.10
y	0.10
ZD	0.625

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改訂記録(社内用)

Rev.	発行日	改訂内容	
		ページ	ポイント
1.00	2019.01.17	All	Rev. 1. 00 発行 R03DS0142EJ0100
2.00	2026.9.2	All	後工程の移管に伴う変更（主に外形寸法図）, (20) 追記
2.00	2026.10.07	All	ページ設定、朱書き→黒字