UPC4572

Low Supply Voltage, Ultra Low-Noise, High Speed, Wide Band, Low I_B Dual Operational Amplifier

DESCRIPTION

UPC4572 is a dual wide band, ultra low noise operational amplifier designed for low supply voltage operation of +4 V to +14 V single supply and ±2 V to ±7 V dual supplies. Using high h_{FE} PNP transistors for the input circuit, Input bias current and input equivalent noise are better than conventional wide band operational amplifier.

UPC4572 is an excellent choice for preamplifiers and active filters in audio, instrumentation, and communication circuit.

In addition, special arrangement products with sorted DC items are available.

FEATURES

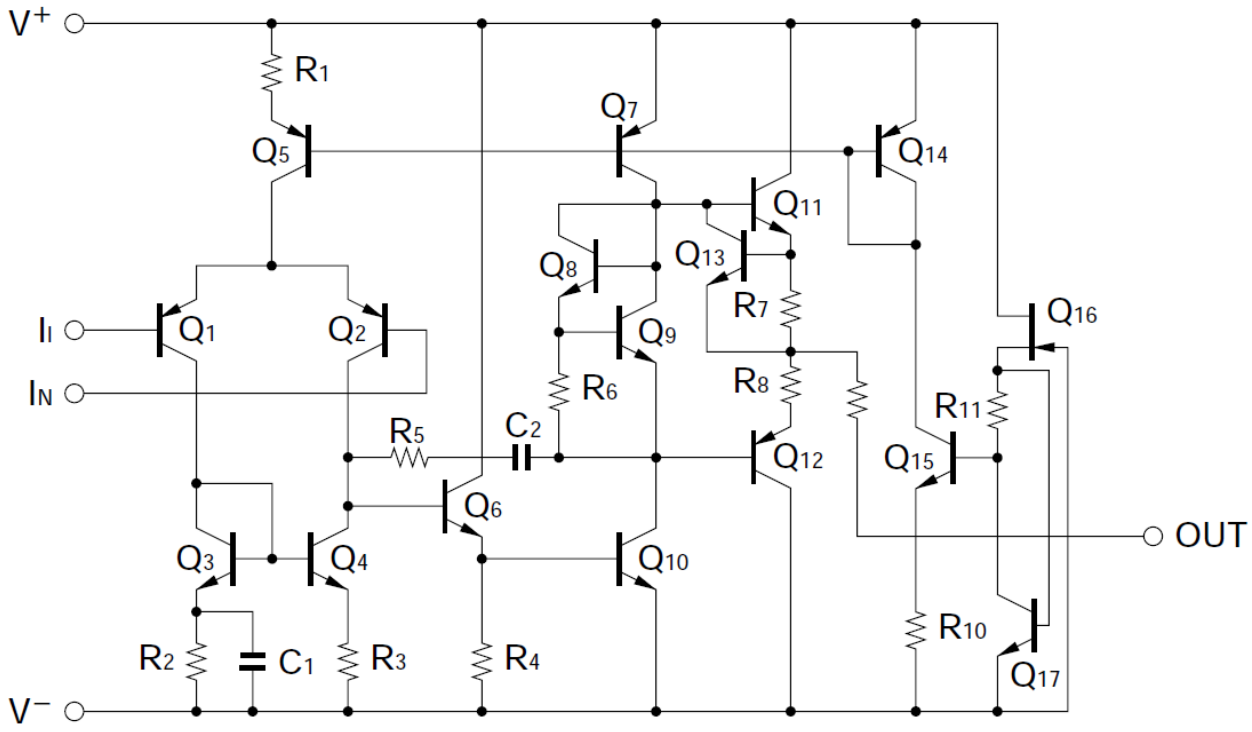
- Input Equivalent Noise Voltage Density (f = 1 kHz) 4 nV/$\sqrt{Hz}$ (TYP.)
- Input Equivalent Noise Voltage (RIAA features) 0.8 $\mu V_{r.m.s.}$ (TYP.)
- Total Harmonic Distortion 0.002 % (TYP.)
- Slew Rate 6 V/µs (TYP.)
- Gain Bandwidth Product GBW (f = 100 kHz) 16 MHz (TYP.)
- Low Input Bias Current 100 nA (TYP.)
- Input Offset Voltage ±0.3 mV (TYP.)
- Low Supply Voltage ±2 V ~ ±7 V (Dual)
  +4 V ~ +14 V (Single, V^- = GND)
- Internal Frequency Compensation
- Standard Dual Op-Amp terminal connection (pin compatible)

ORDERING INFORMATION

Order Name (1)	Selected Grade	Package
UPC4572G2-AP	Standard	8-pin plastic SOP (5.72 mm (225))
UPC4572G2(5)-AP	DC item sorted product	8-pin plastic SOP (5.72 mm (225))

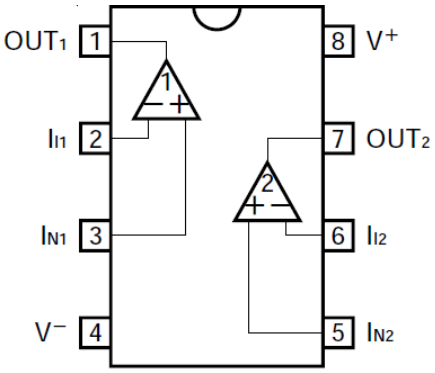
(1) Order names containing E1 or E2 indicate that the packaging format is embossed taping.
Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

EQUIVALENT CIRCUIT (1/2 Circuit)



PIN CONFIGURATION (Marking Side)

UPC4572G2, UPC4572G2(5)



ABSOLUTE MAXIMUM RATINGS(T_A = 25 °C)

Parameter	Symbol	UPC4572G2, UPC4572G2(5)	Unit
Power Supply Voltage Note 1	$V^+ - V^-$	-0.3 ~ +15	V
Differential Input Voltage	V_{ID}	±10	V
Input Voltage Note 2	V_I	V^- -0.3 ~ V^+ +0.3	V
Output Applied Voltage Note 3	V_O	V^- -0.3 ~ V^+ +0.3	V
Total Power Dissipation Note 4	P_T	440	mW
Output Short Circuit Duration Note 5	t_S	10	s
Operating Ambient Temperature	T_A	-20 ~ +80	°C
Storage Temperature	T_{stg}	-55 ~ +125	°C

【**Note**】**1.** Reverse connection of supply voltage can cause destruction.

2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

3. This specification is the voltage, which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics

4. Thermal derating factor is -4.4 mW/°C when ambient temperature is higher than 25 °C.

5. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings and Note 4.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (Dual)	$V^±$	±2	±5	±7	V
Power Supply Voltage (V^- = GND)	V^+	+4	+5 / +12	+14	V
Output Current	I_O			±10	mA
Capacitive Load (A_V = +1)	C_L			100	pF

ELECTRICAL CHARACTERISTICS

UPC4572G2 (T_A = 25 °C, $V^{\pm}$ = ±5 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		±0.3	±5	mV	R_S ≤ 50 Ω
Input Offset Current	I_{IO}		±10	±100	nA	
Input Bias Current Note 6	I_B		100	400	nA	
Large Signal Voltage Gain	A_V	10000	100000			R_L ≥ 2 kΩ, V_O = ±2 V
Circuit Current Note 7	I_{CC}		4.5	7	mA	I_O = 0 A
Common Mode Rejection Ratio	CMR	70	90		dB	
Supply Voltage Rejection Ratio	SVR	70	85		dB	
Output Voltage Swing	V_{om}	±3.3	±3.7		V	R_L ≥ 10 kΩ
Output Voltage Swing	V_{om}	±3.0	±3.5		V	R_L ≥ 2 kΩ
Common Mode Input Voltage Range	V_{ICM}	±3.5	±4		V	
Output Short Circuit Current	I_O	±15	±20		mA	R_L = 0 Ω
Slew Rate	SR	3.5	6		V/μs	R_L ≥ 2 kΩ
Gain Bandwidth Product	GBW	10	16		MHz	f_O = 100 kHz
Unity Gain Frequency	f_{unity}		9		MHz	open loop
Phase Margin	φ_{unity}		60		Deg	open loop
Total Harmonic Distortion	THD		0.002		%	V_O = 1 $V_{r.m.s.}$, f = 20 Hz ~ 20 kHz (Figure 1)
Equivalent Noise Input Voltage	V_n		0.8		$\mu V_{r.m.s}$	RIAA (Figure 2)
Equivalent Noise Input Voltage	V_n		0.5	0.65	$\mu V_{r.m.s}$	FLAT + JIS A, R_S = 100 Ω (Figure 3)
Equivalent Noise Input Voltage Density	e_n		4.5		nV/√Hz	f_O = 10 Hz
Equivalent Noise Input Voltage Density	e_n		4.0		nV/√Hz	f_O = 1 kHz
Equivalent Noise Input Current Density	i_n		0.7		pA/√Hz	f_O = 1 kHz
Channel Separation			120		dB	f = 20 Hz ~ 20 kHz
Average VIO Temperature Drift	$\Delta V_{IO}/\Delta T$		±2		μV/°C	

UPC4572G2 (T_A = 25 °C, V^+ = +5 V, V^- = GND)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		±0.3	±5	mV	R_S ≤ 50 Ω
Input Offset Current	I_{IO}		±10	±100	nA	
Input Bias Current Note 6	I_B		100	400	nA	
Large Signal Voltage Gain	A_V	8000	80000			R_L ≥ 2 kΩ
Supply Current Note 7	I_{CC}		4	6	mA	I_O = 0 A
Common Mode Rejection Ratio	CMR	60	75		dB	
Supply Voltage Rejection Ratio	SVR	60	70		dB	
Output Voltage (High)	V_{OH}	3.2	3.5		V	R_L ≥ 2 kΩ (R_L to 1/2 V^+)
Output Voltage (Low)	V_{OL}		1.3	1.6	V	R_L ≥ 2 kΩ (R_L to 1/2 V^+)
Common Mode Input Voltage Range	V_{ICM}	1.5		3.5	V	
Slew Rate	SR		4		V/μs	
Gain Band Width Product	GBW		12		MHz	

【**Note**】**6.** Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

7. This current flows irrespective of the existence of use.

ELECTRICAL CHARACTERISTICS

UPC4572G2(5) (T_A = 25 °C, $V^{\pm}$ = ±5 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		±0.3	±1.5	mV	R_S ≤ 50 Ω
Input Offset Current Note 6	I_{IO}		±10	±50	nA	
Input Bias Current Note 6	I_B		100	200	nA	
Large Signal Voltage Gain	A_V	30000	100000			R_L ≥ 2 kΩ, V_O = ±2 V
Circuit Current Note 7	I_{CC}		4.5	5.5	mA	I_O = 0 A
Common Mode Rejection Ratio	CMR	75	90		dB	
Supply Voltage Rejection Ratio	SVR	70	85		dB	
Output Voltage Swing	V_{om}	±3.45	±3.7		V	R_L ≥ 10 kΩ
Output Voltage Swing	V_{om}	±3.3	±3.5		V	R_L ≥ 2 kΩ
Common Mode Input Voltage Range	V_{ICM}	±3.8 -3.7	±4		V	
Output Short Circuit Current	I_O	±15	±20		mA	R_L = 0 Ω
Slew Rate	SR	3.5	6		V/μs	R_L ≥ 2 kΩ
Gain Bandwidth Product	GBW	10	16		MHz	f_O = 100 kHz
Unity Gain Frequency	f_{unity}		9		MHz	open loop
Phase Margin	φ unity		60		Deg	open loop
Total Harmonic Distortion	THD		0.002		%	V_O = 1 $V_{r.m.s.}$, f = 20 Hz ~ 20 kHz (Figure 1)
Equivalent Noise Input Voltage	V_n		0.8		$\mu V_{r.m.s}$	RIAA (Figure 2)
Equivalent Noise Input Voltage	V_n		0.5	0.65	$\mu V_{r.m.s}$	FLAT + JIS A, R_S = 100 Ω (Figure 3)
Equivalent Noise Input Voltage Density	e_n		4.5		$nV/\sqrt{Hz}$	f_O = 10 Hz
Equivalent Noise Input Voltage Density	e_n		4.0		$nV/\sqrt{Hz}$	f_O = 1 kHz
Equivalent Noise Input Current Density	i_n		0.7		$pA/\sqrt{Hz}$	f_O = 1 kHz
Channel Separation			120		dB	f = 20 Hz ~ 20 kHz
Average VIO Temperature Drift	$\Delta V_{IO}/\Delta T$		±2		μV/°C	

UPC4572G2(5) (T_A = 25 °C, V^+ = +5 V, V^- = GND)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		±0.3	±1.5	mV	R_S ≤ 50 Ω
Input Offset Current Note 6	I_{IO}		±10	±50	nA	
Input Bias Current Note 6	I_B		100	200	nA	
Large Signal Voltage Gain	A_V	40000	80000			R_L ≥ 2 kΩ
Supply Current Note 7	I_{CC}		4	5	mA	I_O = 0 A
Common Mode Rejection Ratio	CMR	65	75		dB	
Supply Voltage Rejection Ratio	SVR	60	70		dB	
Output Voltage (High)	V_{OH}	3.4	3.5		V	R_L ≥ 2 kΩ (R_L to 1/2 V^+)
Output Voltage (Low)	V_{OL}		1.3	1.45	V	R_L ≥ 2 kΩ (R_L to 1/2 V^+)
Common Mode Input Voltage Range	V_{ICM}	1.2		3.8	V	
Slew Rate	SR		4		V/μs	
Gain Band Width Product	GBW		12		MHz	

【**Note**】 **6.** Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

7. This current flows irrespective of the existence of use.

MEASUREMENT CIRCUIT

Figure 1: Total Harmonic Distortion Measurement Circuit

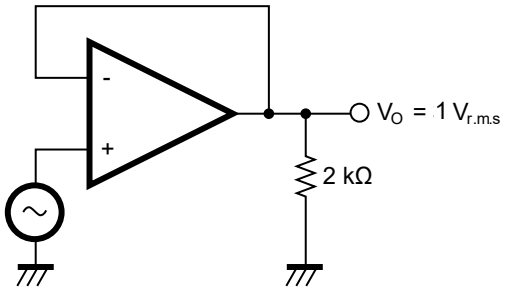


Figure 2: Noise Measurement Circuit (RIAA)

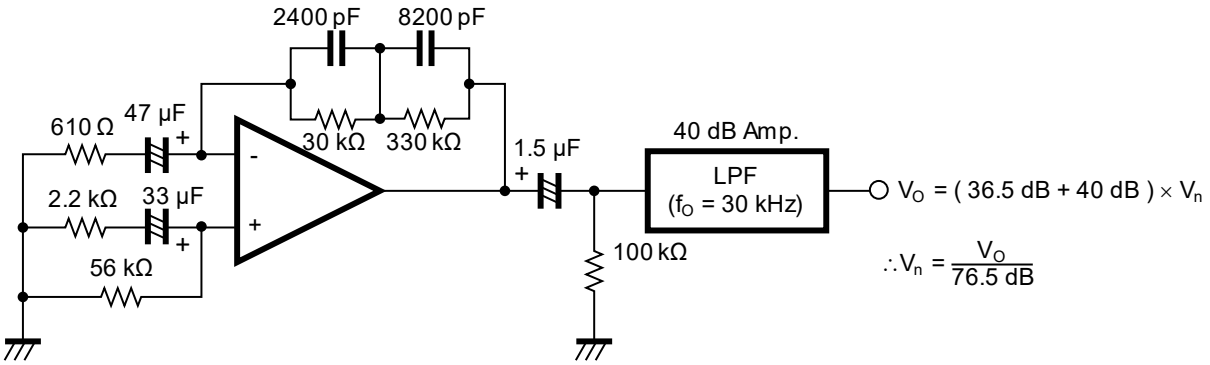
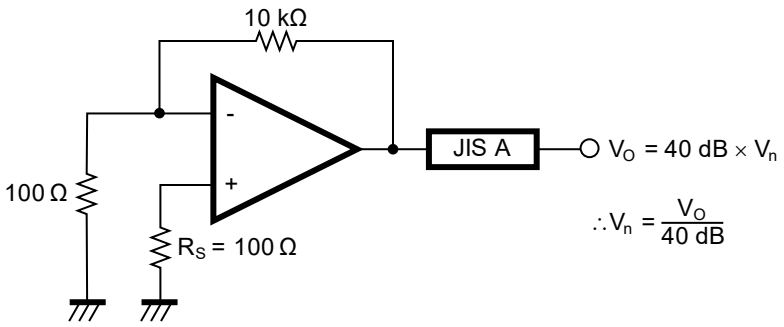
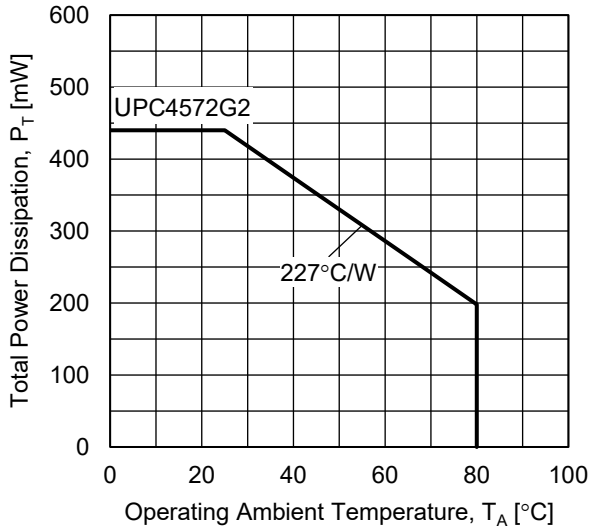


Figure 3: Noise Measurement Circuit (FLAT+JIS A)

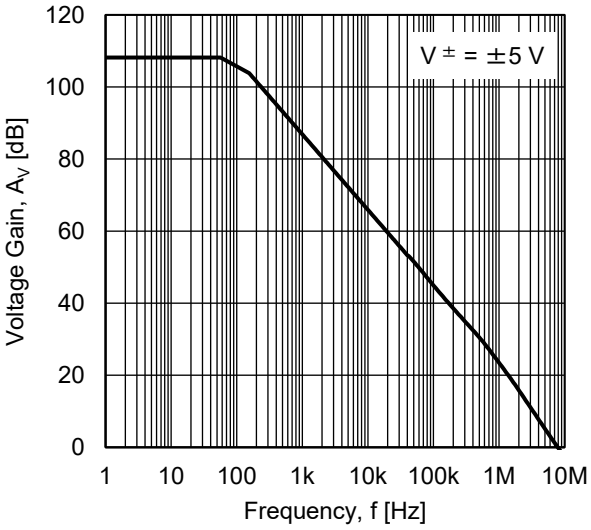


CHARACTERISTICS CURVE (T_A = 25 °C, TYP.) (REFERENCE VALUE)

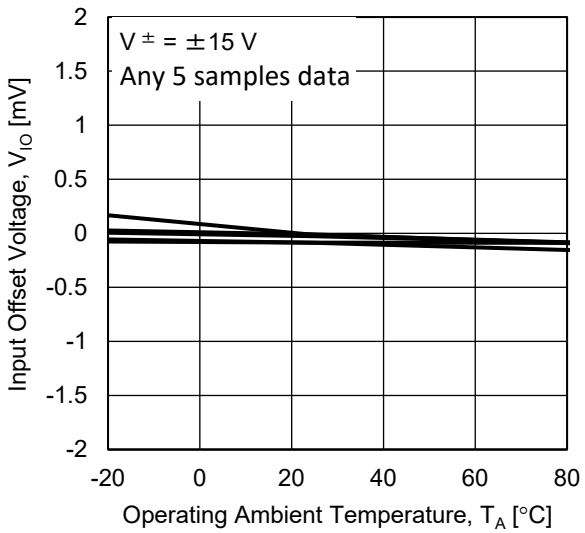
P_T vs. T_A (Absolute maximum rating)



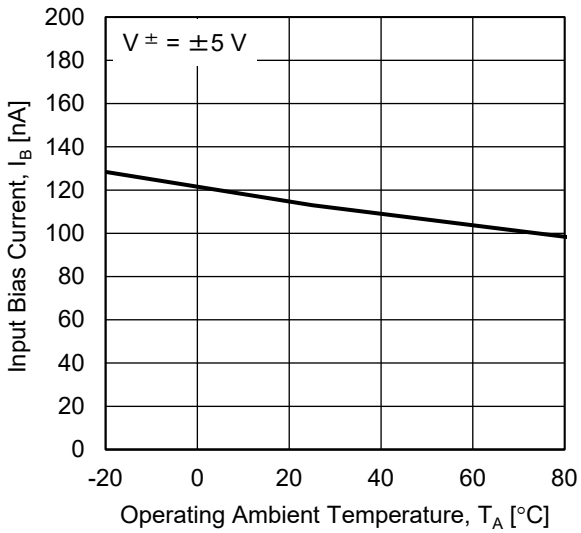
A_V vs. f



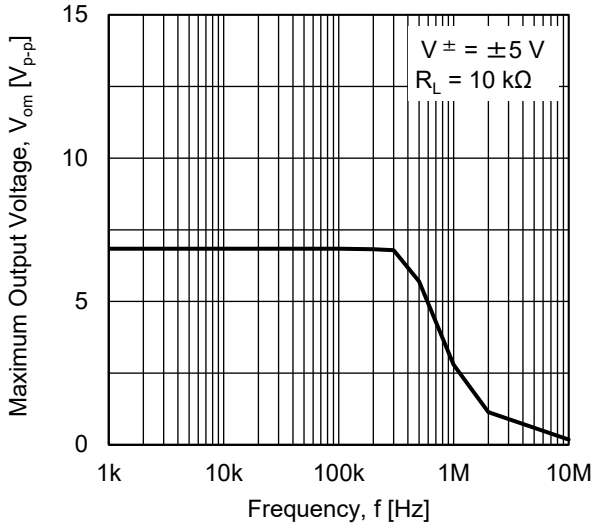
V_{IO} vs. T_A



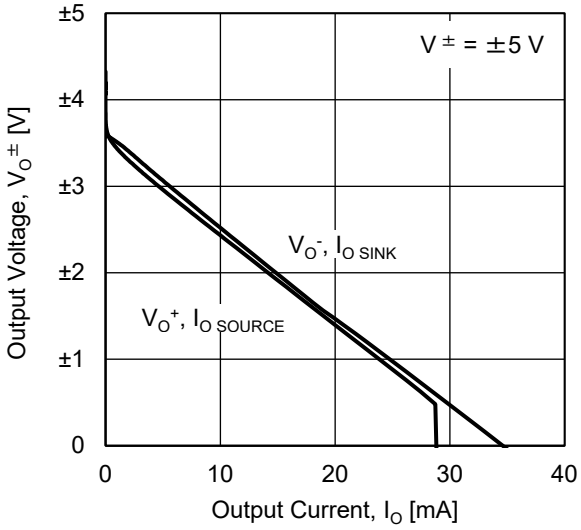
I_B vs. T_A



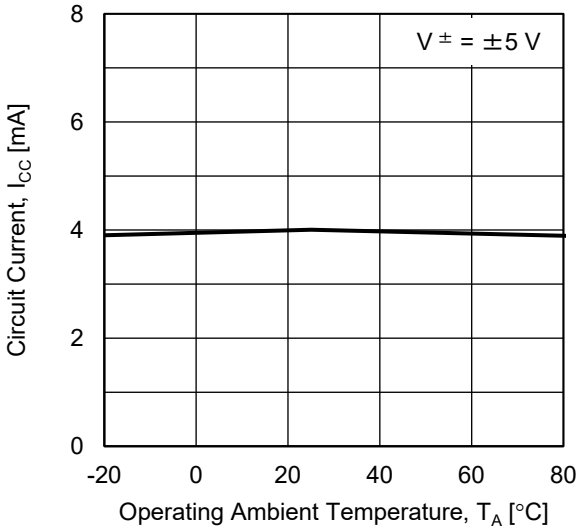
V_{Om} vs. f



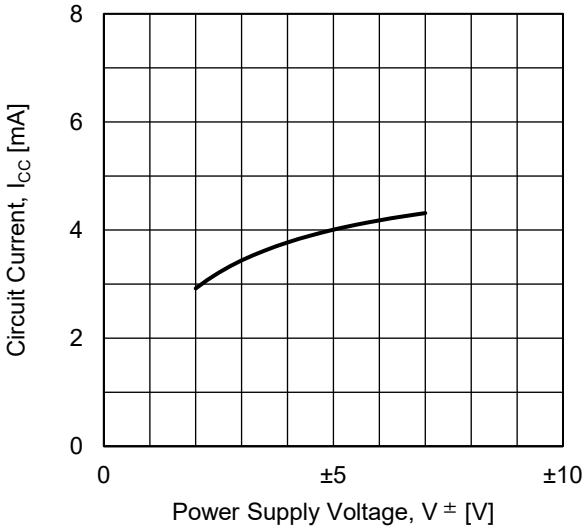
$V_O^{\pm}$ vs. I_O



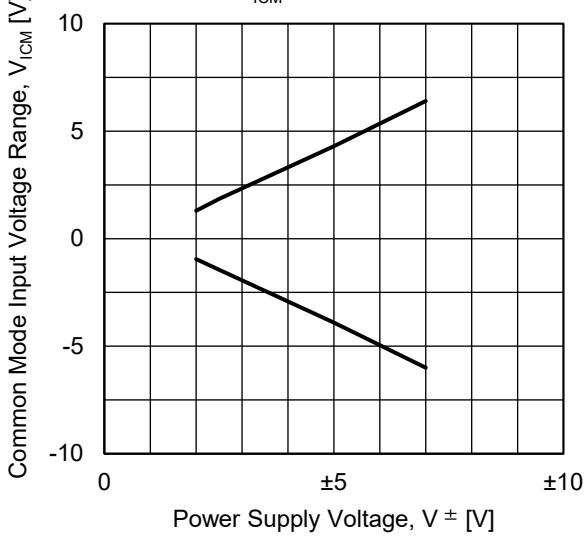
I_{CC} vs. T_A



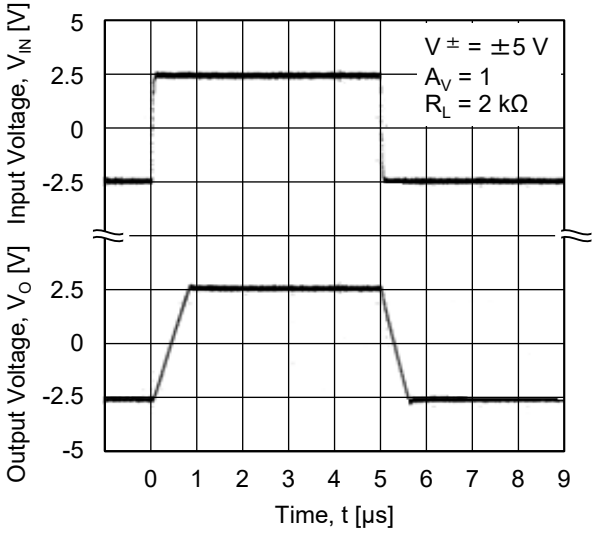
I_{CC} vs. $V^{\pm}$



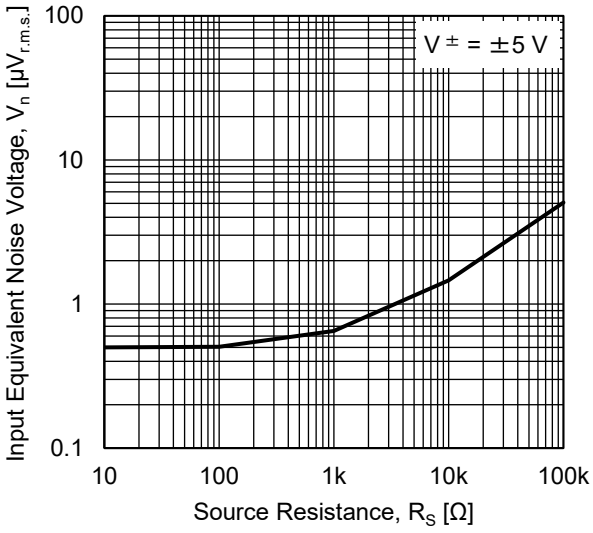
V_{ICM} vs. $V^{\pm}$



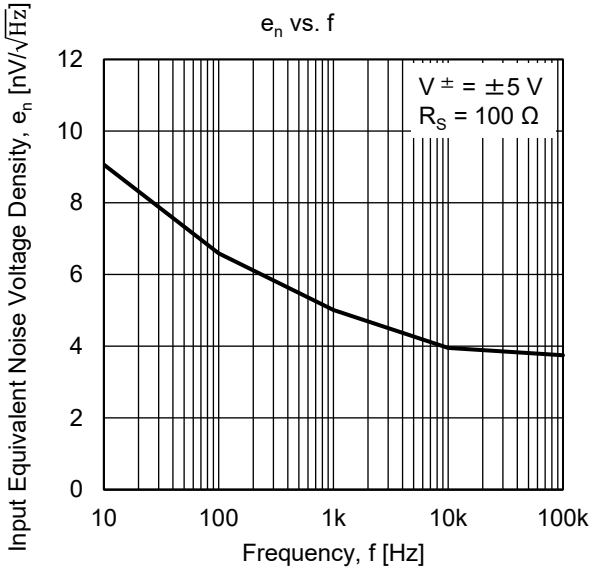
Pulse Response

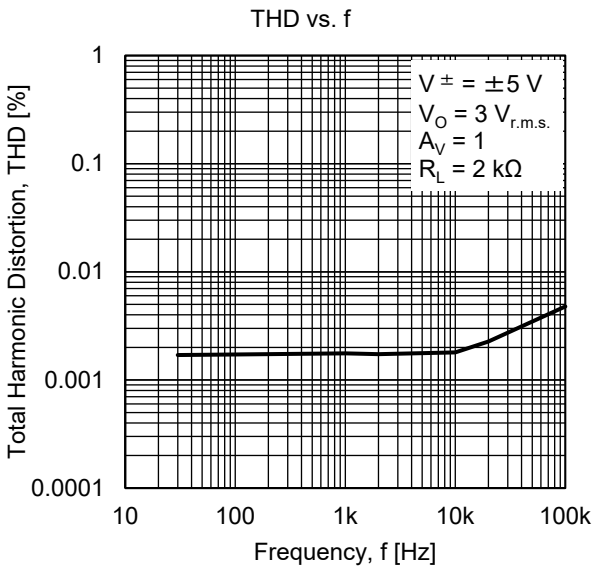


V_n vs. R_S (FLAT + JSI A)



e_n vs. f



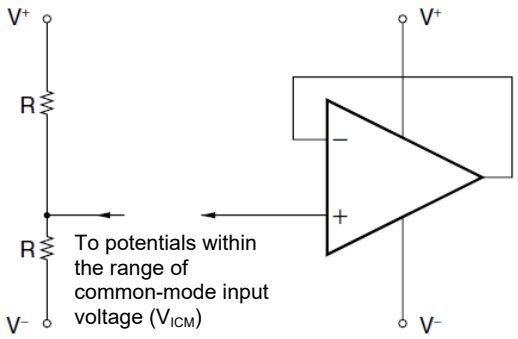

THD vs. f
Total Harmonic Distortion, THD [%]
1
0.1
0.01
0.001
0.0001
10
100
1k
10k
100k
Frequency, f [Hz]
V± = ±5 V
VO = 3 Vr.m.s.
AV = 1
RL = 2 kΩ

USE WITH PRECAUTIONS

- **Managing unused circuits**

  If there is an unused circuit, the following connection is recommended.

Example of unused circuit process



Remark: In this example, an intermediate potential between V^+ and V^- is applied.

- **Power Supply (Dual Power Supply / Single Power Supply)**

  The op-amp operates as long as a predetermined voltage is applied between V^+ and V^-. Therefore, it can operate with a single power supply (V^- = GND), but it cannot operate the input and output near GND. Common-mode input voltage Please pay attention to the range and maximum output voltage.

- **Ratings of input/output pin voltage**

  When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than V^-, or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Range of common-mode input voltage**

  When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

  V_{ICM} (TYP.) : V^- +1 ~ V^+ -1 [V] (T_A = 25°C).

  During designing, do include some tolerance by considering temperature characteristics etc.

- **Maximum output voltage**

  The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

  V_{om}^+ (TYP.): V^+ - 1.3 [V] (T_A = 25°C), V_{om}^- (TYP.): V^- + 1.3 [V] (T_A = 25°C)

  During designing, do include some tolerance by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range ($V_{om}^+ - V_{om}^-$) will become narrow when the output current increases.

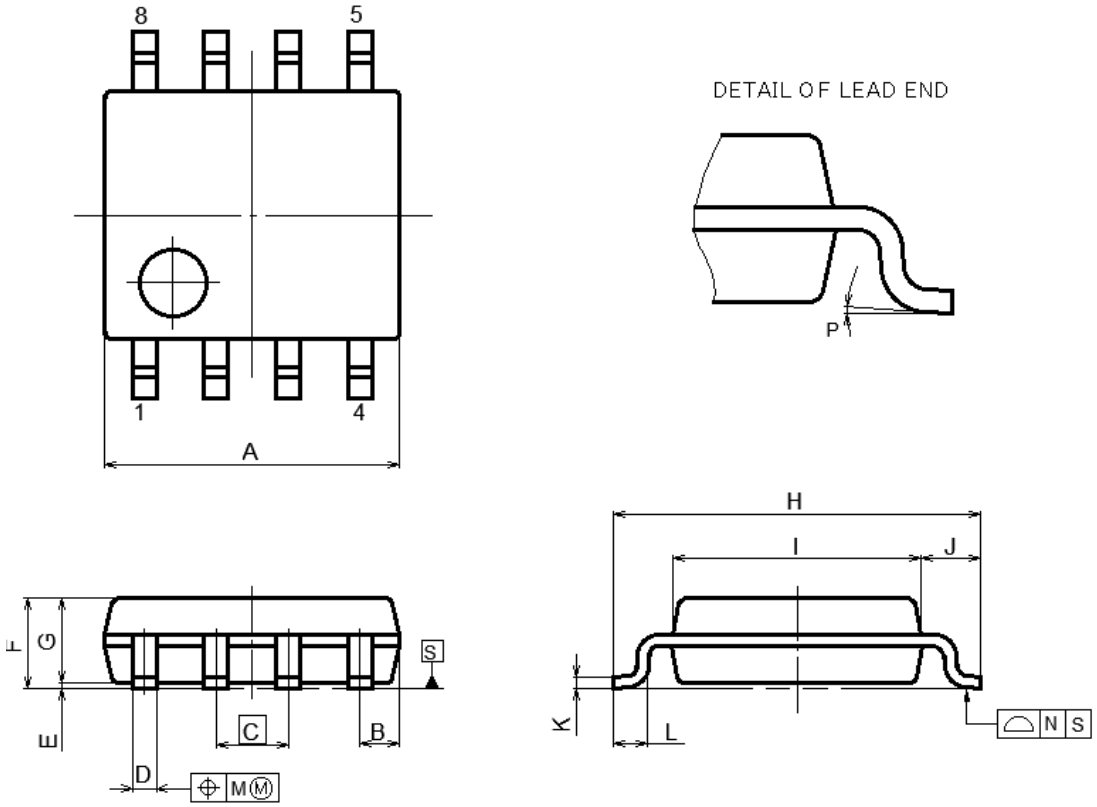
- **Handling of ICs**

  When stress is added to ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

PACKAGE DRAWINGS

8-PIN PLASTIC SOP

JEITA Package code	RENESAS code	MASS (TYP.) [g]
P-LSOP8-4.4×5.2-1.27	PLSP0008DE-A	0.09[g]



NOTE
EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF
ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

ITEM	DIMENSIONS
A	5.2±0.17
B	0.78MAX
C	1.27(T.P)
D	0.40±0.05
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.1
J	1.05±0.15
K	0.2±0.07
L	0.6±0.20
M	0.1MAX
N	0.1MAX
P	4°±4°

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