UPC813

High Slew Rate, Low Offset Voltage J-FET Input Operational Amplifier

DESCRIPTION

UPC813 is a high-speed version of UPC811. The J-FET input operational amplifier features a high-speed PNP transistor in the output stage for stable operation at a high slew rate of 25V/μs with a gain of 1 (full feedback).

The resistor-trimming method proven in other Renesas High-Precision Op-Amp and High-Precision reference voltage is incorporate in this Op-Amp input stage, thus producing an excellent low offset voltage characteristics that has surpassed conventional general purpose op-amp in spite of being J-FET input.

Under the same series, UPC814, 4094 with the same circuit configuration are also available.

FEATURES

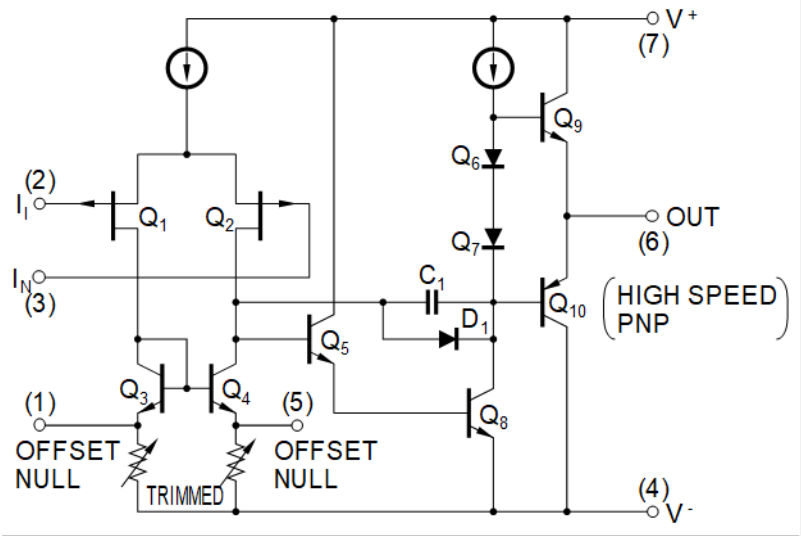
- Input Offset Voltage ±1 mV (TYP.) (±2.5 mV MAX.)
- V_{IO} Temperature Drift ±7 μV/°C (TYP.)
- Input Bias Current 50 pA (TYP.)
- Slew Rate 25 V/μs (TYP.)
- Unity Gain Frequency 6 MHz (TYP.))
- Input Equivalent Noise Voltage Density 19 nV/$\sqrt{Hz}$ (TYP.) (f = 1 kHz)
- Stable operation against capacitive load (Capacitive Load at 220 pF, AV = +1)
- Built-In Phase Compensation Circuit
- Built-In Output Short Circuit Protection
- Standard Single Op-Amp terminal connection (pin compatible)

ORDERING INFORMATION

Order Name (1)	Package
UPC813G2-AP	8-Pin plastic SOP (5.72 mm (225))

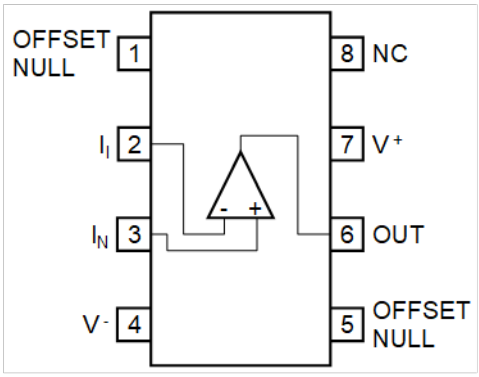
(1) Order names containing E1 or E2 indicate that the packaging format is embossed taping. Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

EQUIVALENT CIRCUIT



PIN CONFIGURATION (Top View)

UPC813G2



Note NC : No Connection

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	UPC813G2	Unit
Supply Voltage Note1	$V^+ - V^-$	-0.3 ~ +36	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Note 2	V_I	V^- -0.3 ~ V^+ +0.3	V
Output Applied Voltage Note3	V_O	V^- -0.3 ~ V^+ +0.3	V
Total Power Dissipation Note4	P_T	440	mW
Output Short Circuit Duration Note5		Indefinite	s
Operating Ambient Temperature	T_A	-40 ~ +85	°C
Storage Temperature	T_{stg}	-55 ~ +125	°C

【Note】 **1.** Note that reverse connections of the power supply may damage the ICs.

2. The input terminal must be applied within the input voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp input voltage must operates within the electrical characteristics range of input common-mode voltage.

3. The output terminal must be applied within the output voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp output voltage must operates within the electrical characteristics range of maximum output voltage.

4. This is the value at $T_A \leq +25$ °C. De-rate value at -4.4 mW/°C when $T_A > 25$ °C.

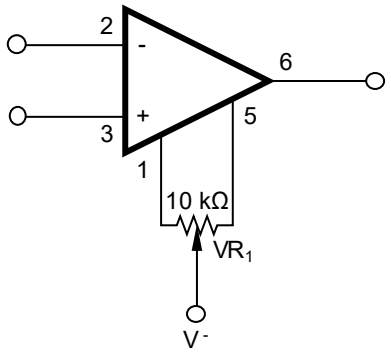
5. Please use the total loss and the de-rating value from Note 4.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	$V^{\pm}$	±5		±16	V
Load Current	I_O			±10	mA
Load Capacitance (When A_V = +1)	C_L			220 Note6	pF

【Note】 **6.** This is the value when the feedback resistor (R_f) = 0 Ω. The higher the R_f value, the more likely it is to oscillate due to the influence of the input capacitance. So connect a capacitor of about 100 pF in parallel with R_f.

OFFSET ADJUSTMENT METHOD



【Note】 OFFSET NULL pin should be open or connected to V⁻ via a resistor as shown above. Any connection other than V⁻ may cause malfunction, characteristics degradation or damage.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, $V^{\pm}$ = ±15 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		±1	±2.5	mV	R_S ≤ 50 Ω
Input Offset Current Note7	I_{IO}		±25	±100	pA	
Input Bias Current Note7	I_B		50	200	pA	
Large Signal Voltage Gain	A_V	25000	200000			R_L ≥ 2 kΩ, V_O = ±10 V
Circuit Current	I_{CC}		2.5	3.4	mA	I_O = 0 A
Common Mode Rejection Ratio	CMR	70	100		dB	
Supply Voltage Rejection Ratio	SVR	70	100		dB	
Output Voltage Swing	V_{om}	±12	+14.0 -13.3		V	R_L ≥ 10 kΩ
Output Voltage Swing	V_{om}	±10	+13.5 -12.8		V	R_L ≥ 2 kΩ
Common Model Input Voltage Range	V_{ICM}	±11	+14 -12		V	
Slew Rate	SR		25		V/μs	A_V = 1
Unity Gain Frequency	f_{unity}		6		MHz	
Input Equivalent Noise Voltage Density	e_n		19		nV/$\sqrt{Hz}$	R_S = 100 Ω, f = 1 kHz
Input Offset Voltage	V_{IO}			±5	mV	R_S ≤ 50 Ω, T_A = -20 ~ +70 °C
Average V_{IO} Temperature Drift	$\Delta V_{IO}/\Delta T$		±7		μV/°C	T_A = -20 ~ +70 °C
Input Offset Current Note7	I_{IO}			±2	nA	T_A = -20 ~ +70 °C
Input Bias Current Note7	I_B			7	nA	T_A = -20 ~ +70 °C

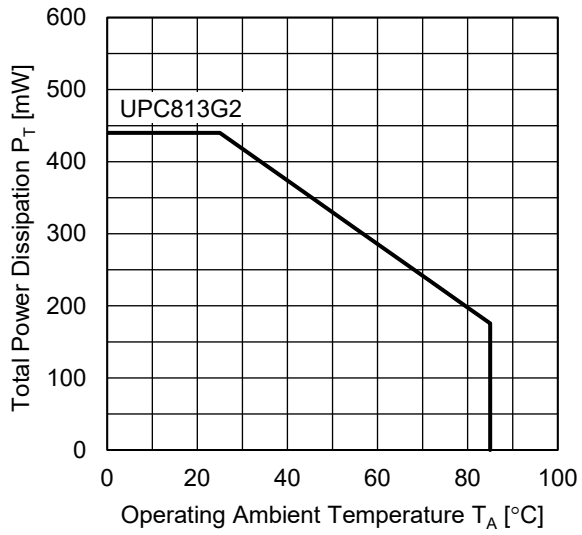
【Note】 **7.** The direction of the input bias current is the same direction that flows into the IC because the first stage is composed of Pch J-FET. When T_J = 25°C or higher, it increases exponentially with increase in temperature (please see I_B - T_A characteristics). During measurement, please kindly take care of $T_J \fallingdotseq T_A$.

Caution

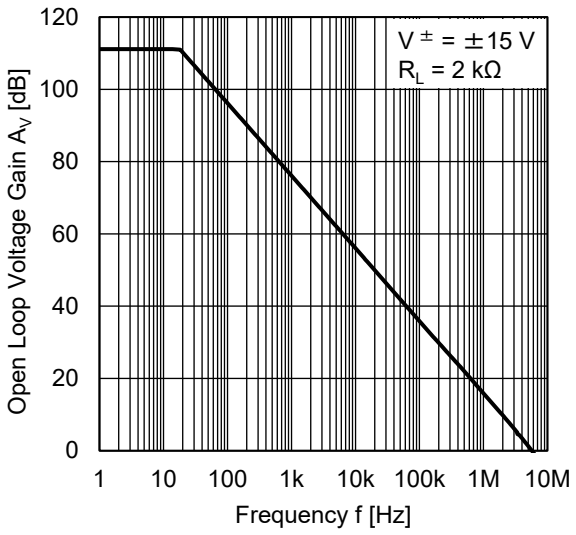
Since UPC813 has high input impedance characteristics, please be careful of insulation between the terminals on the board.

ELECTRICAL CHARACTERISTICS CURVE (T_A = 25 °C, TYP.)

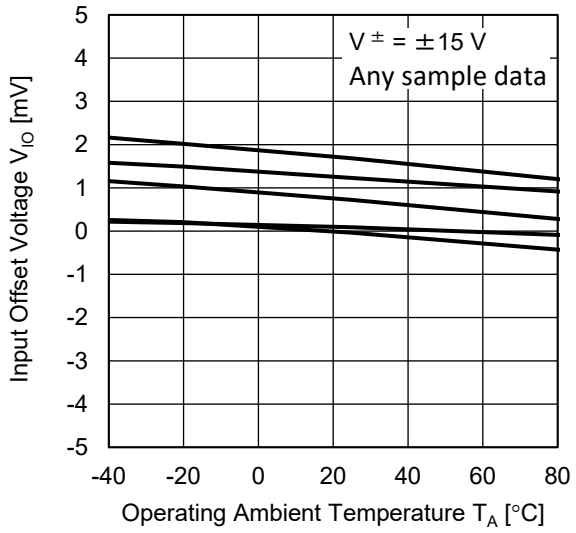
P_T vs. T_A (Absolute maximum rating)



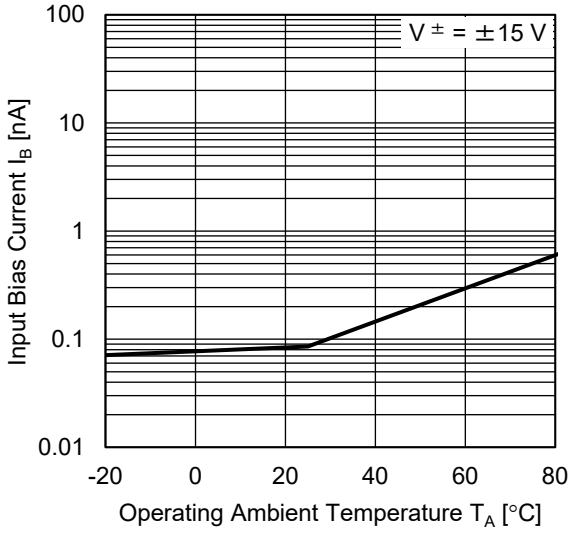
A_V vs. f



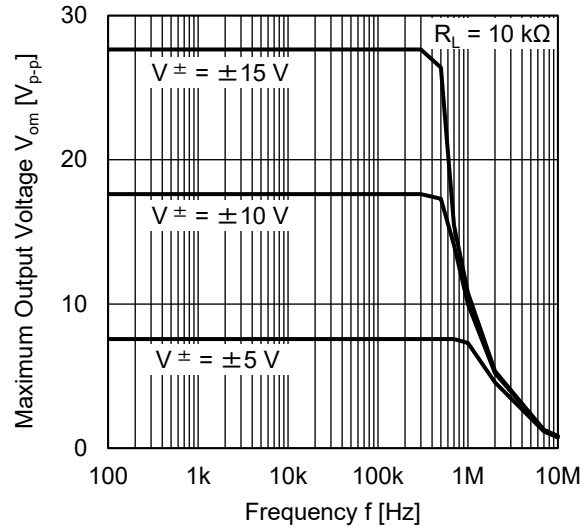
V_{IO} vs. T_A



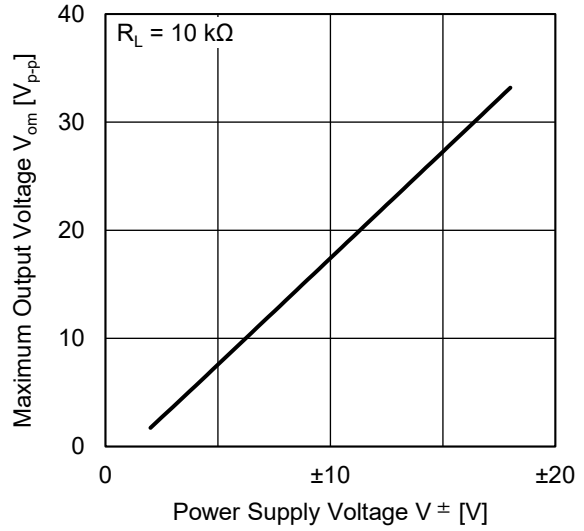
I_B vs. T_A



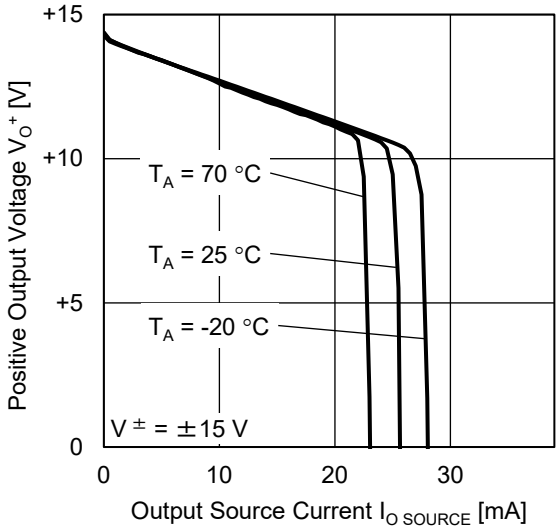
V_{om} vs. f



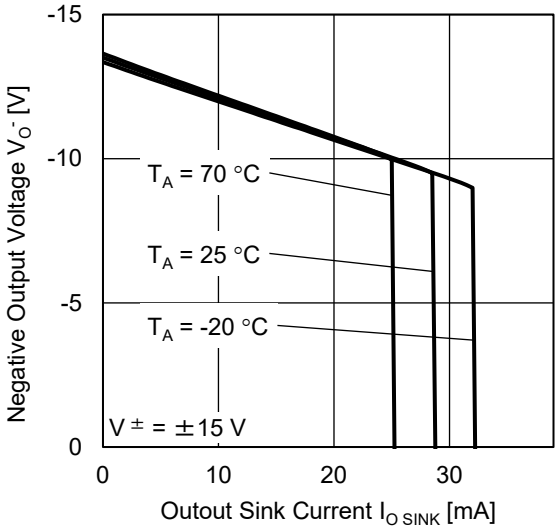
V_{om} vs. $V^{\pm}$



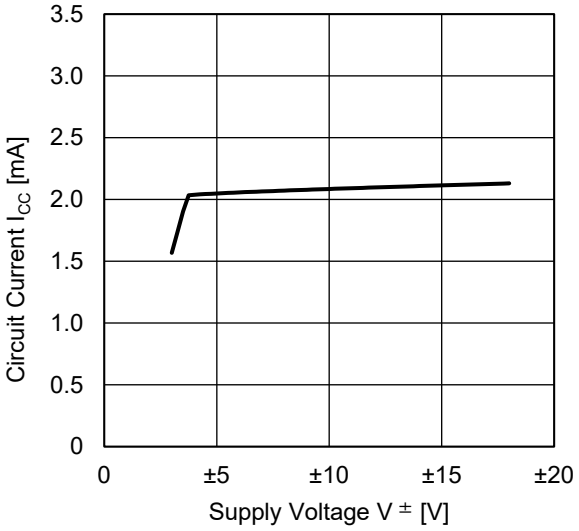
V_O^+ vs. $I_{O\ SOURCE}$



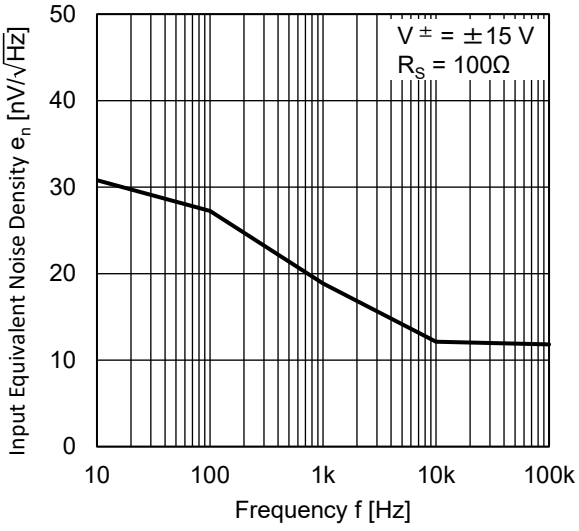
V_O^- vs. $I_{O\ SINK}$



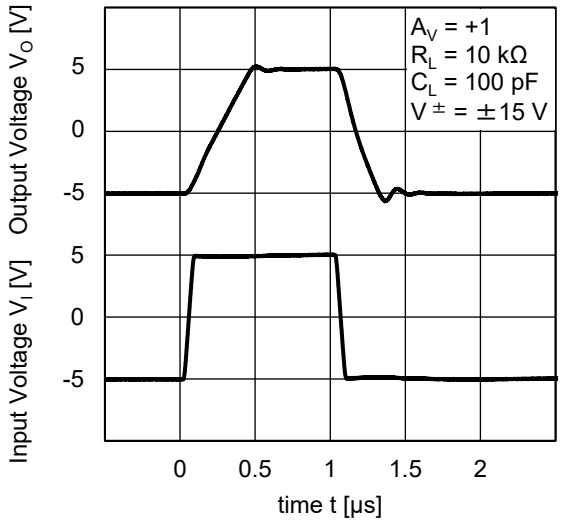
I_{CC} vs. $V^{\pm}$



e_n vs. f



Pulse Response Characteristics



USE WITH PRECAUTIONS

- **Power Supply (Dual Power Supply / Single Power Supply)**

  The op amp operates when a predetermine voltage is applied between V^+ - V^- . Therefore, while it operates from a single power supply (V^- = GND), it is not possible to operate the input and output near GND. So please be careful of the common-mode input voltage range and maximum output voltage.

- **Ratings of input/output pin voltage**

  When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than V^-, or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Range of common-mode input voltage**

  When the supply voltage does not meet the condition of electrical characteristics, the range of common−mode input voltage is as follows.

  V_{ICM} (TYP.) : V^- +3 ~ V^+ -1 [V] (T_A = 25 °C).

  During designing, do include some margin by considering characteristics variation, temperature characteristics etc.

- **Maximum Output voltage**

  The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

  V_{om}^+ (TYP.): V^+ - 1 [V] (T_A = 25°C), V_{om}^- (TYP.): V^- + 1.7 [V] (T_A = 25°C)

  During designing, do include some margin by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range (V_{om}^+ - V_{om}^-) will become narrow when the output current increases.

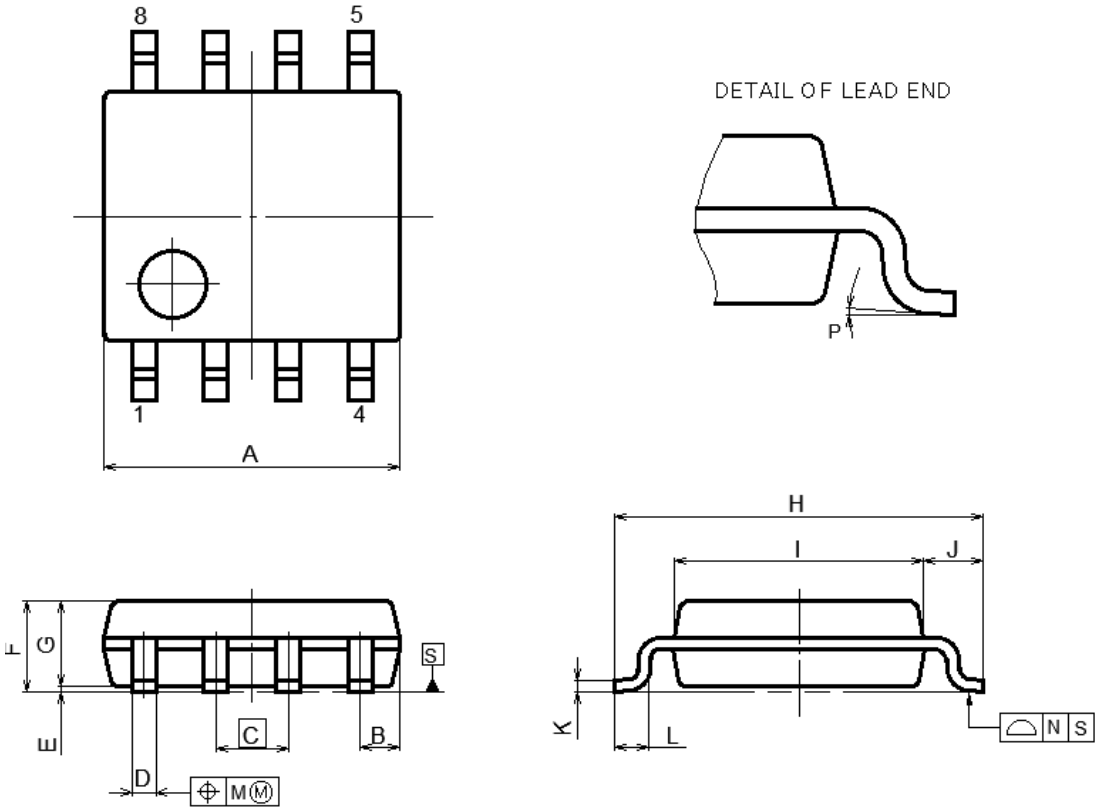
- **Handling of ICs**

  When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

PACKAGE DRAWINGS

8-PIN PLASTIC SOP

JEITA Package code	RENESAS code	MASS (TYP.) [g]
P-LSOP8-4.4×5.2-1.27	PLSP0008DE-A	0.09[g]



NOTE
EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF
ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

ITEM	DIMENSIONS
A	5.2±0.17
B	0.78MAX
C	1.27(T.P)
D	0.40±0.05
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.1
J	1.05±0.15
K	0.2±0.07
L	0.6±0.20
M	0.1MAX
N	0.1MAX
P	4°±4°

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