To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

BIPOLAR ANALOG INTEGRATED CIRCUIT

Phase-out/Discontinued

μPC8178TB

SILICON MMIC LOW CURRENT AMPLIFIER FOR MOBILE COMMUNICATIONS

DESCRIPTION

The μPC8178TB is a silicon monolithic integrated circuit designed as amplifier for mobile communications. This IC can realize low current consumption with external chip inductor which can not be realized on internal 50 Ω wideband matched IC. This low current amplifier operates on 3.0 V.

This IC is manufactured using NEC's 30 GHz f_{max} UHS0 (Ultra High Speed Process) silicon bipolar process. This process uses direct silicon nitride passivation film and gold electrodes. These materials can protect the chip surface from pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

FEATURES

- Low current consumption : I_{CC} = 1.9 mA TYP. @ V_{CC} = 3.0 V
- Supply voltage : V_{CC} = 2.4 to 3.3 V
- Excellent isolation : ISL = 39 dB TYP. @ f = 1.0 GHz
  ISL = 40 dB TYP. @ f = 1.9 GHz
  ISL = 38 dB TYP. @ f = 2.4 GHz
- Power gain : G_P = 11.0 dB TYP. @ f = 1.0 GHz
  G_P = 11.5 dB TYP. @ f = 1.9 GHz
  G_P = 11.5 dB TYP. @ f = 2.4 GHz
- Gain 1 dB compression output power : $P_{O (1 dB)}$ = –4.0 dBm TYP. @ f = 1.0 GHz
  $P_{O (1 dB)}$ = –7.0 dBm TYP. @ f = 1.9 GHz
  $P_{O (1 dB)}$ = –7.5 dBm TYP. @ f = 2.4 GHz
- Operating frequency : 0.1 to 2.4 GHz (Output port LC matching)
- High-density surface mounting : 6-pin super minimold package (2.0 × 1.25 × 0.9 mm)
- Low weight : 7 mg (Standard value)

APPLICATION

- Buffer amplifiers on 0.1 to 2.4 GHz mobile communications system

Caution Electro-static sensitive devices

Document No. P14895EJ2V0DS00 (2nd edition)
Date Published November 2000 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

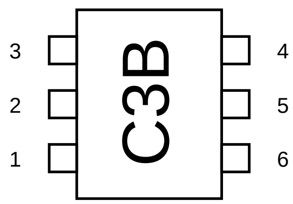
ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
μPC8178TB-E3	6-pin super minimold	C3B	Embossed tape 8 mm wide. 1, 2, 3 pins face the perforation side of the tape. Qty 3 kpcs/reel.

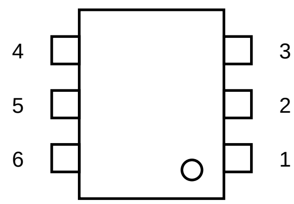
Remark To order evaluation samples, please contact your local NEC sales office.
(Part number for sample order: μPC8178TB)

PIN CONNECTIONS

(Top View)



(Bottom View)



Pin No.	Pin Name
1	INPUT
2	GND
3	GND
4	OUTPUT
5	GND
6	V_{CC}

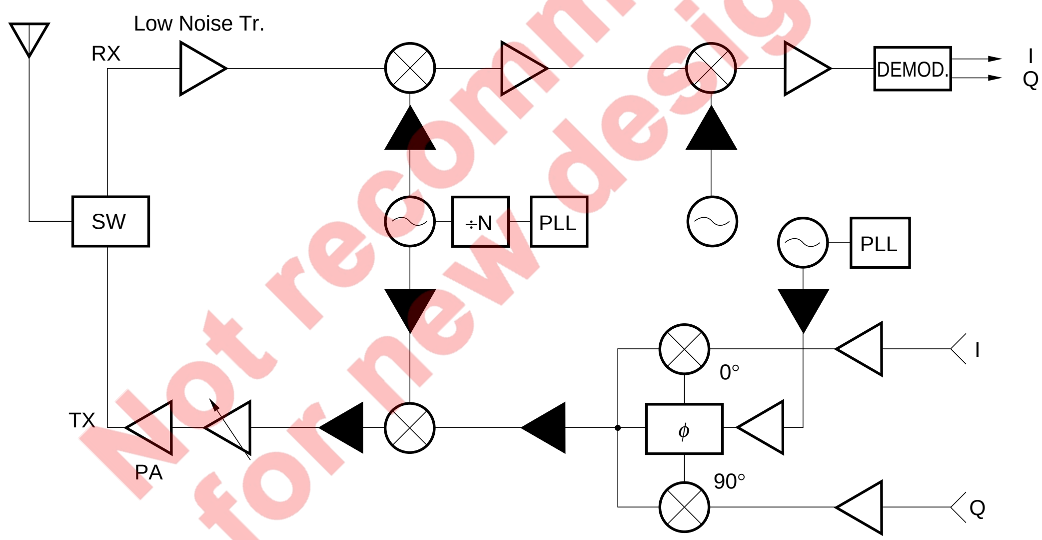
PRODUCT LINE-UP (T_A = +25°C, V_{CC} = V_{out} = 3.0 V, Z_S = Z_L = 50 Ω)

Parameter / Part No.	I_{CC} (mA)	1.0 GHz output port matching frequency			1.66 GHz output port matching frequency			1.9 GHz output port matching frequency			2.4 GHz output port matching frequency			Marking
		G_P (dB)	ISL (dB)	$P_{O(1dB)}$ (dBm)	G_P (dB)	ISL (dB)	$P_{O(1dB)}$ (dBm)	G_P (dB)	ISL (dB)	$P_{O(1dB)}$ (dBm)	G_P (dB)	ISL (dB)	$P_{O(1dB)}$ (dBm)	
μPC8178TB	1.9	11	39	–4.0	–	–	–	11.5	40	–7.0	11.5	38	–7.5	C3B
μPC8179TB	4.0	13.5	44	+3.0	–	–	–	15.5	42	+1.5	15.5	41	+1.0	C3C
μPC8128TB	2.8	12.5	39	–4.0	13	39	–4.0	13	37	–4.0	–	–	–	C2P
μPC8151TB	4.2	12.5	38	+2.5	15	36	+1.5	15	34	+0.5	–	–	–	C2U
μPC8152TB	5.6	23	40	–4.5	19.5	38	–8.5	17.5	35	–8.5	–	–	–	C2V

Remark Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.

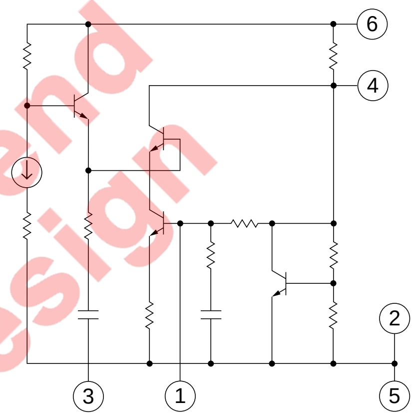
SYSTEM APPLICATION EXAMPLE

Location examples in digital cellular



These ICs can be added to your system around ▲ parts, when you need more isolation or gain. The application herein, however, shows only examples, therefore the application can depend on your kit evaluation.

PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage (V)	Pin Voltage (V)[Note]	Function and Applications	Internal Equivalent Circuit
1	INPUT	–	0.91	Signal input pin. A internal matching circuit, configured with resisters, enables 50 Ω connection over a wide band. This pin must be coupled to signal source with capacitor for DC cut.	
2 3 5	GND	0	–	Ground pin. This pin should be connected to system ground with minimum inductance. Ground pattern on the board should be formed as wide as possible. All the ground pins must be connected together with wide ground pattern to decrease impedance defference.	
4	OUTPUT	voltage as same as V_{CC} through external inductor	–	Signal output pin. This pin is designed as collector output. Due to the high impedance output, this pin should be externally equipped with LC matching circuit to next stage. For L, a size 1005 chip inductor can be chosen.	
6	V_{CC}	2.4 to 3.3	–	Power supply pin. This pin should be externally equipped with bypass capacitor to minimize its impedance.	

Note Pin voltage is measured at V_{CC} = 3.0 V.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	V_{CC}	T_A = +25°C, Pin 4, Pin 6	3.6	V
Circuit Current	I_{CC}	T_A = +25°C	15	mA
Power Dissipation	P_D	Mounted on double sided copper clad 50 × 50 × 1.6 mm epoxy glass PWB (T_A = +85°C)	270	mW
Operating Ambient Temperature	T_A		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +150	°C
Input Power	P_{in}	T_A = +25°C	+5	dBm

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remarks
Supply Voltage	V_{CC}	2.4	3.0	3.3	V	The same voltage should be applied to pin 4 and pin 6.
Operating Ambient Temperature	T_A	–40	+25	+85	°C	

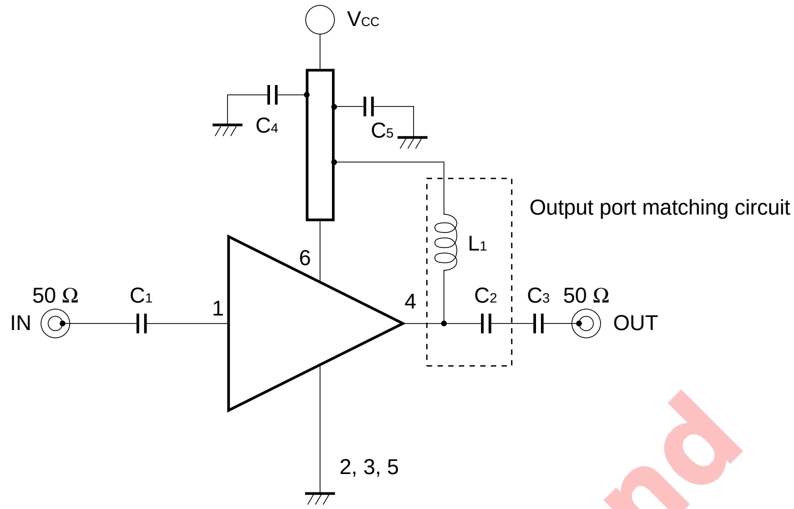
★ ## ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, T_A = +25°C, V_{CC} = V_{out} = 3.0 V, Z_S = Z_L = 50 Ω, at LC matched frequency)

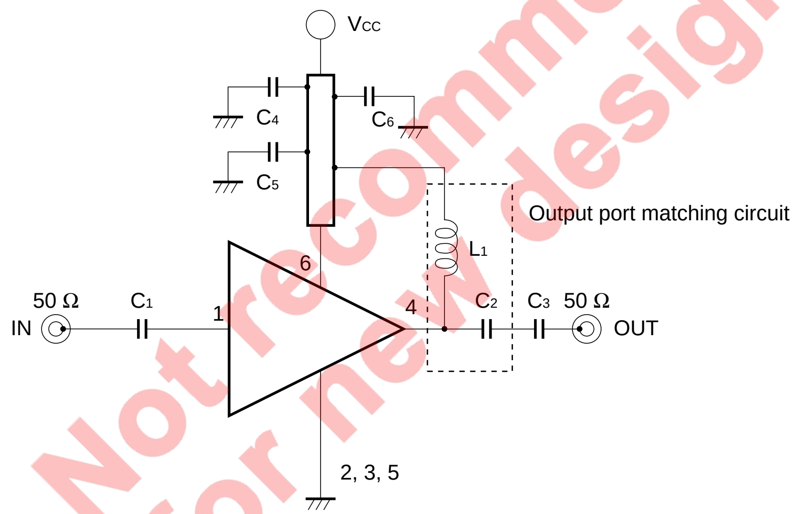
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	I_{CC}	No signal	1.4	1.9	2.4	mA
Power Gain	G_P	f = 1.0 GHz, P_{in} = –30 dBm f = 1.9 GHz, P_{in} = –30 dBm f = 2.4 GHz, P_{in} = –30 dBm	9.0 9.0 9.0	11.0 11.5 11.5	13.0 13.5 13.5	dB
Isolation	ISL	f = 1.0 GHz, P_{in} = –30 dBm f = 1.9 GHz, P_{in} = –30 dBm f = 2.4 GHz, P_{in} = –30 dBm	34 35 33	39 40 38	– – –	dB
Gain 1 dB Compression Output Power	$P_{O(1dB)}$	f = 1.0 GHz f = 1.9 GHz f = 2.4 GHz	–8.0 –11.0 –11.5	–4.0 –7.0 –7.5	– – –	dBm
Noise Figure	NF	f = 1.0 GHz f = 1.9 GHz f = 2.4 GHz	– – –	5.5 5.5 5.5	7.0 7.0 7.0	dB
Input Return Loss	RL_{in}	f = 1.0 GHz, P_{in} = –30 dBm f = 1.9 GHz, P_{in} = –30 dBm f = 2.4 GHz, P_{in} = –30 dBm	4 5 6.5	7 8 9.5	– – –	dB

TEST CIRCUITS

★ <1> f = 1.0 GHz



<2> f = 1.9 GHz



<3> f = 2.4 GHz

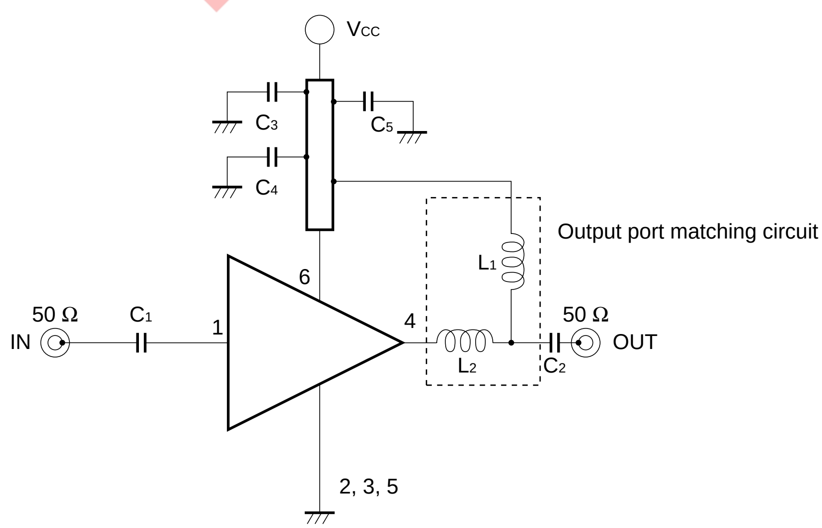
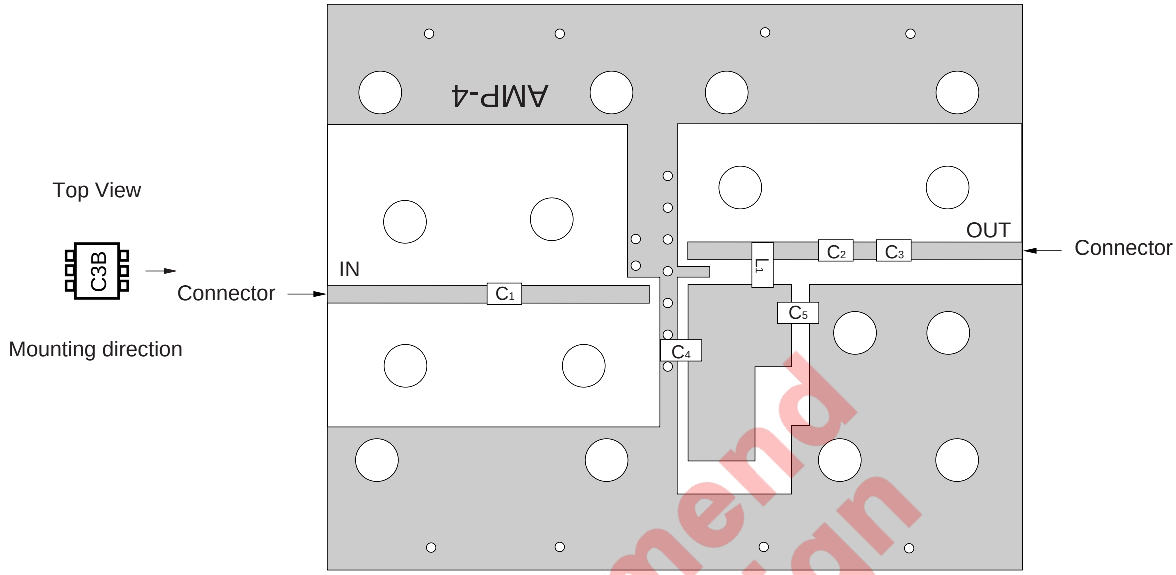


ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD

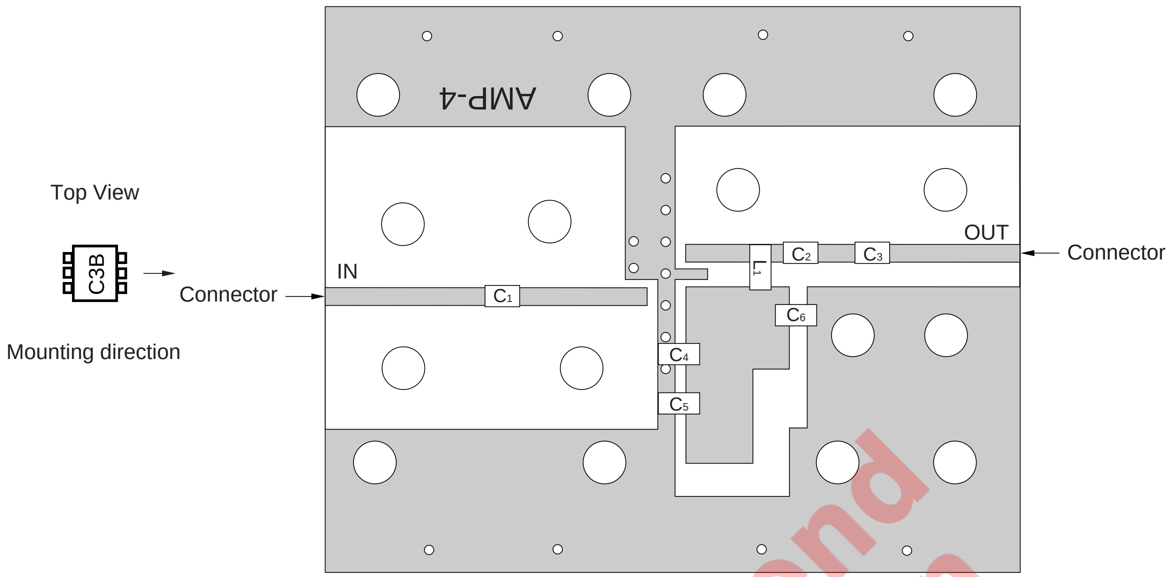
<1> f = 1.0 GHz



COMPONENT LIST

	1.0 GHz Output Port Matching
C_1, C_3, C_5	1 000 pF
C_2	0.75 pF
C_4	10 pF
L_1	12 nH

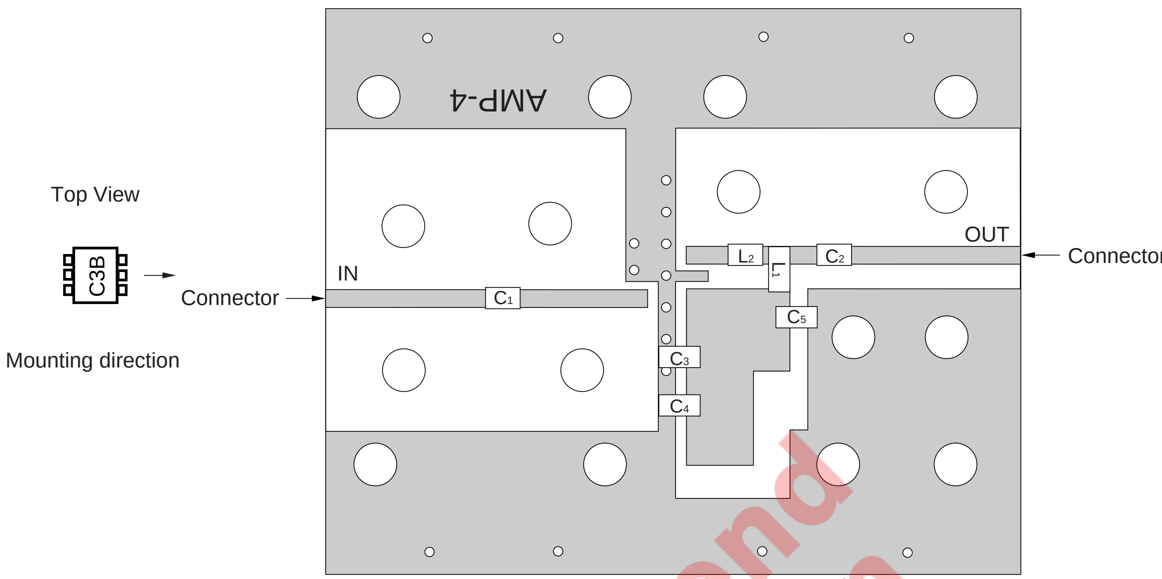
<2> f = 1.9 GHz



COMPONENT LIST

	1.9 GHz Output Port Matching
C_1, C_3, C_5, C_6	1 000 pF
C_2	0.5 pF
C_4	10 pF
L_1	3.9 nH

<3> f = 2.4 GHz



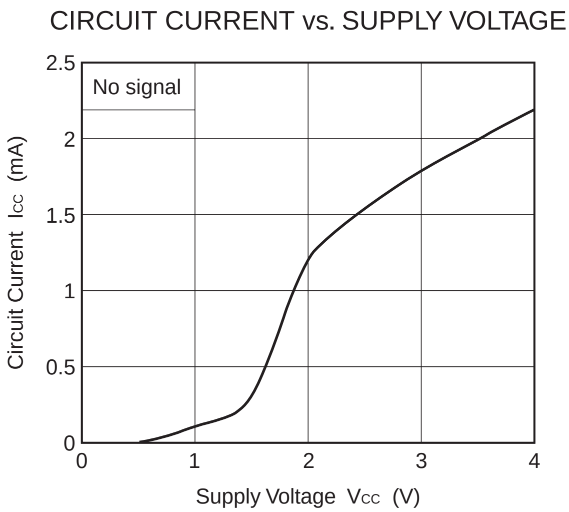
COMPONENT LIST

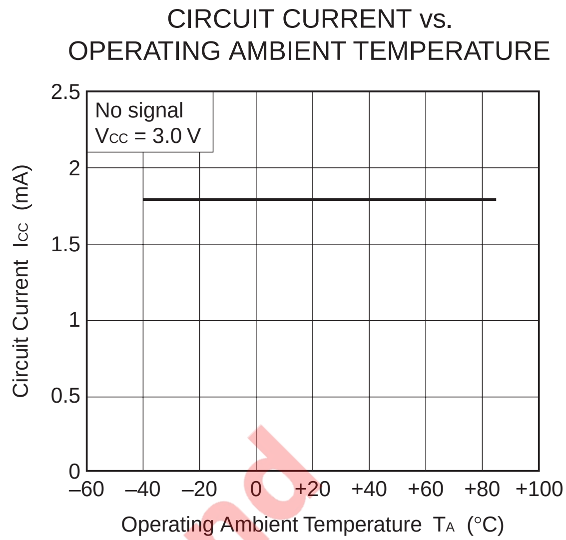
	2.4 GHz Output Port Matching
C_1, C_2, C_4, C_5	1 000 pF
C_3	10 pF
L_1	1.8 nH
L_2	2.7 nH

NOTES

(∗1) 42 × 35 × 0.4 mm double sided copper clad polyimide board
(∗2) Solder plated on pattern
(∗3) Back side: GND pattern
(∗4) ○ ◯ : Through holes

★ TYPICAL CHARACTERISTICS (Unless otherwise specified, T_A = +25°C)

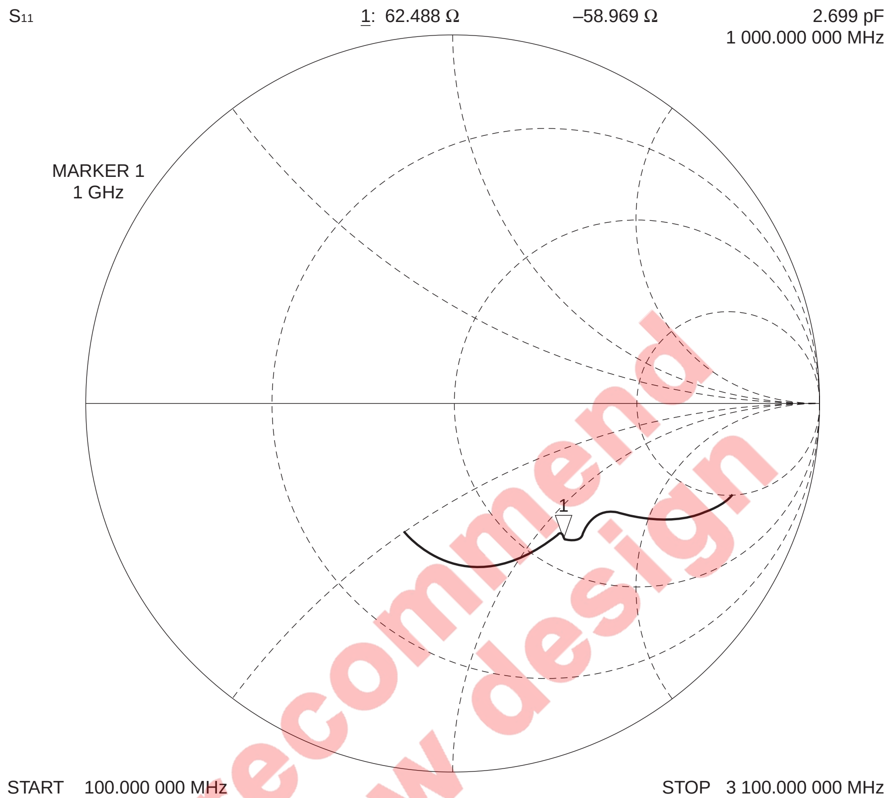


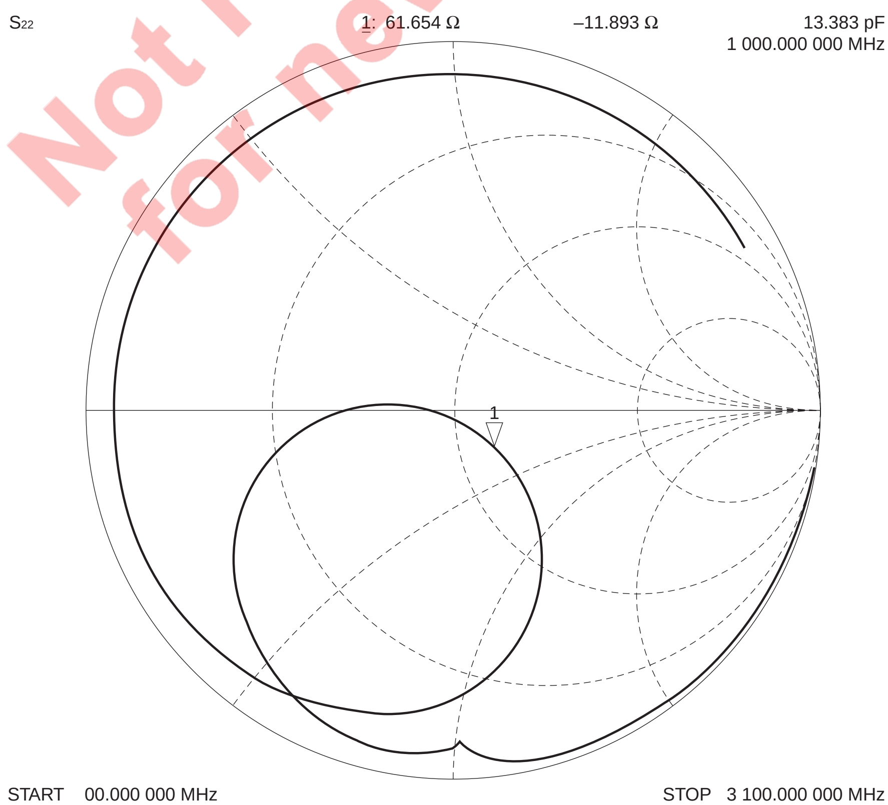


1.0 GHz OUTPUT PORT MATCHING

S-PARAMETERS (monitored at connector on board)

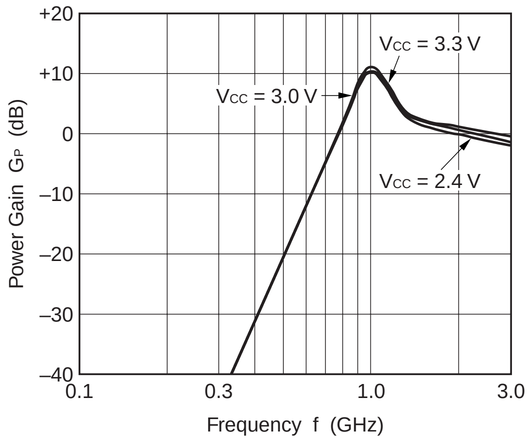
T_A = +25°C , V_{CC} = V_{out} = 3.0 V



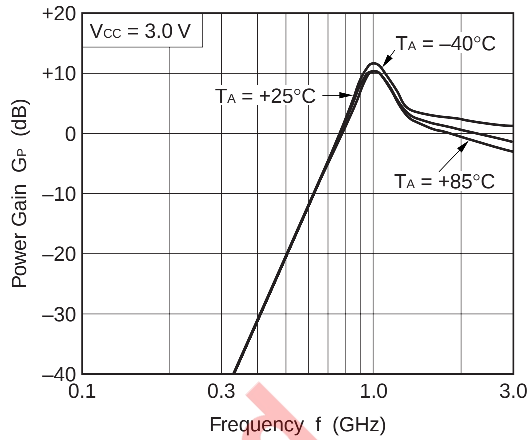


1.0 GHz OUTPUT PORT MATCHING

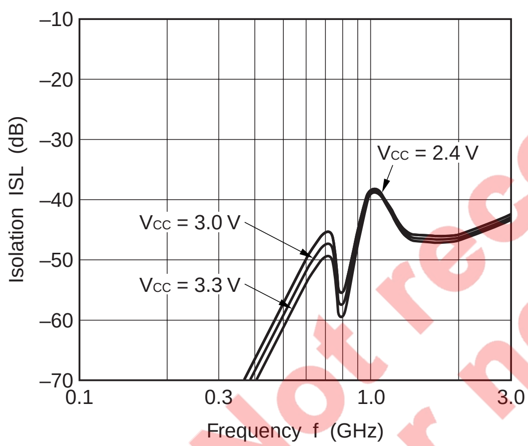
POWER GAIN vs. FREQUENCY



POWER GAIN vs. FREQUENCY



ISOLATION vs. FREQUENCY



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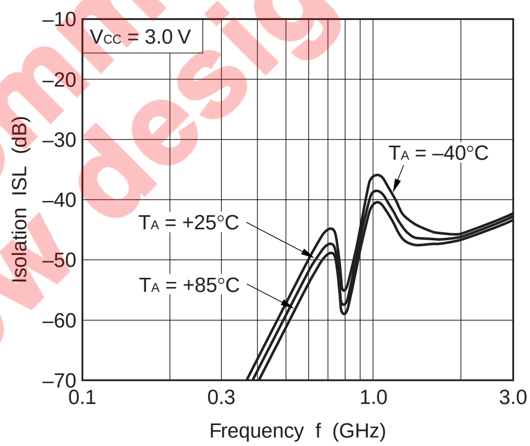
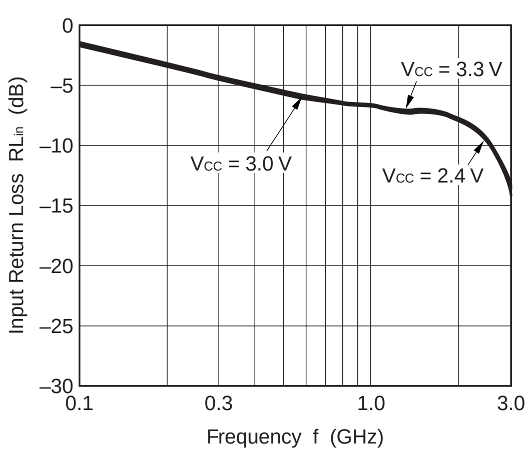
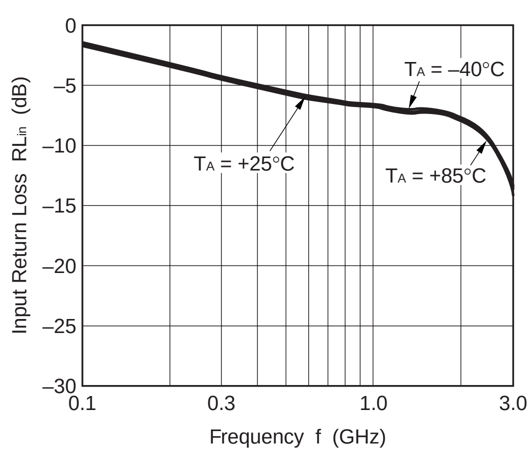


INPUT RETURN LOSS vs. FREQUENCY

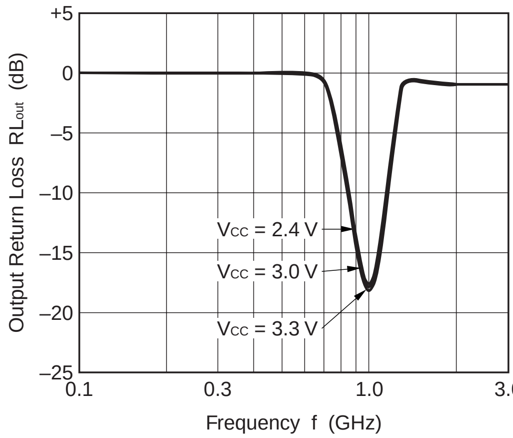


INPUT RETURN LOSS vs. FREQUENCY

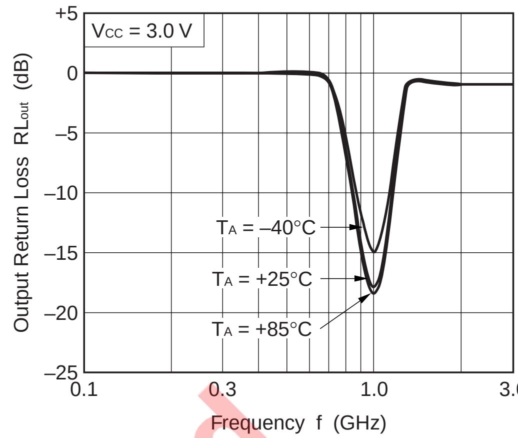


1.0 GHz OUTPUT PORT MATCHING

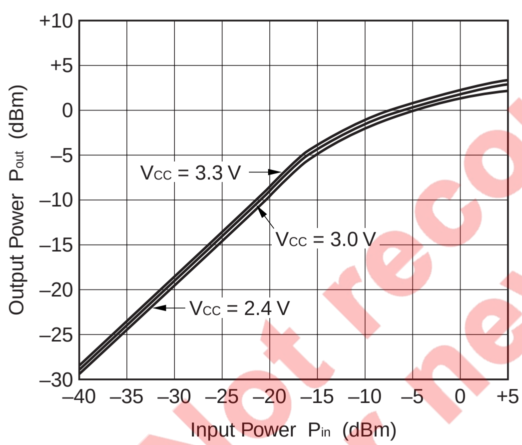
OUTPUT RETURN LOSS vs. FREQUENCY



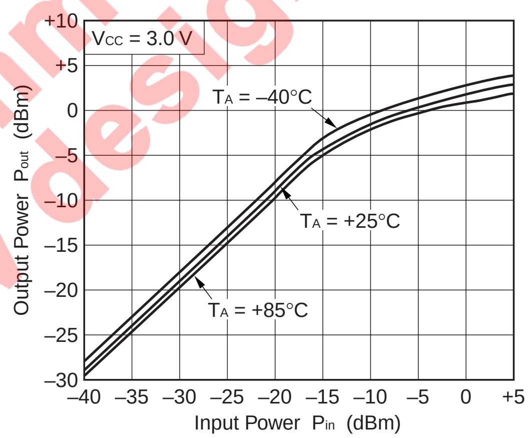
OUTPUT RETURN LOSS vs. FREQUENCY



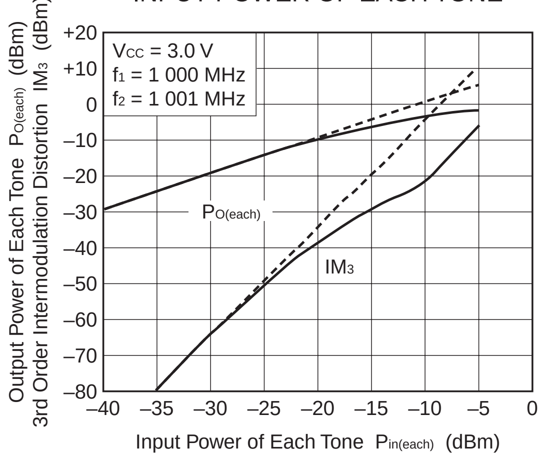
OUTPUT POWER vs. INPUT POWER



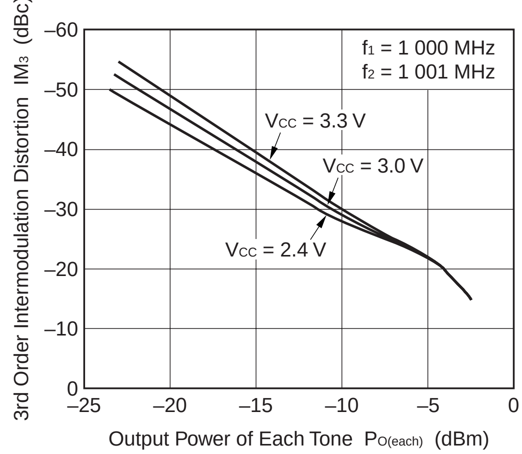
OUTPUT POWER vs. INPUT POWER



OUTPUT POWER OF EACH TONE, IM3 vs.
INPUT POWER OF EACH TONE

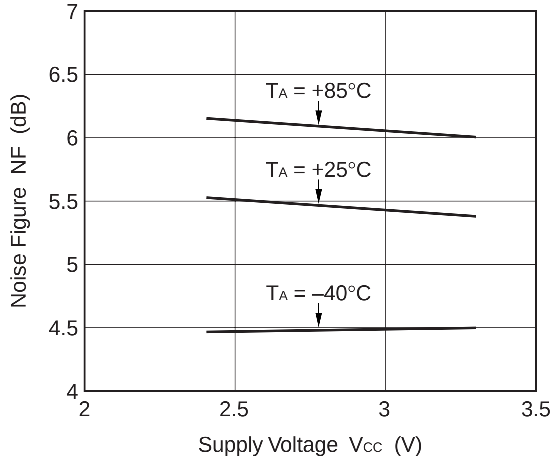


3RD ORDER INTERMODULATION DISTORTION vs.
OUTPUT POWER OF EACH TONE



1.0 GHz OUTPUT PORT MATCHING

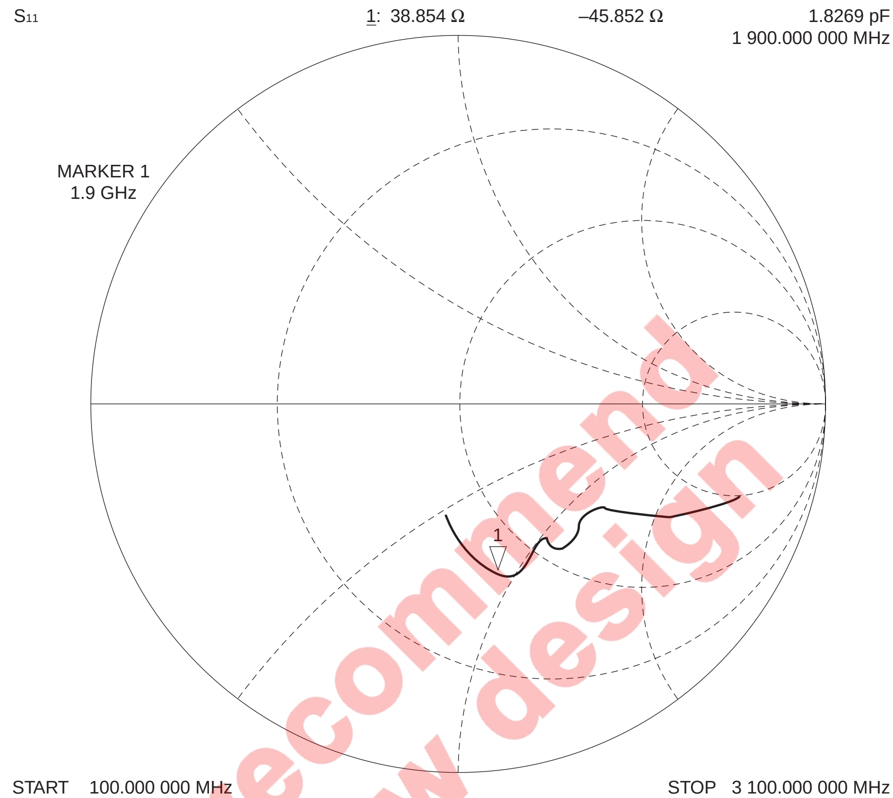
NOISE FIGURE vs. SUPPLY VOLTAGE

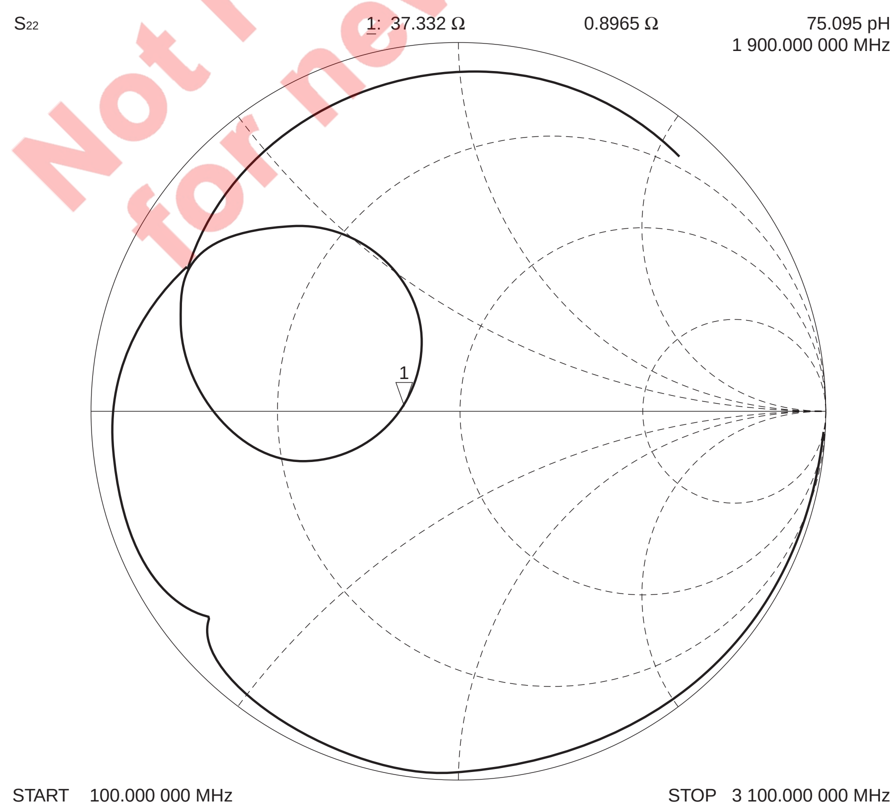


1.9 GHz OUTPUT PORT MATCHING

S-PARAMETERS (monitored at connector on board)

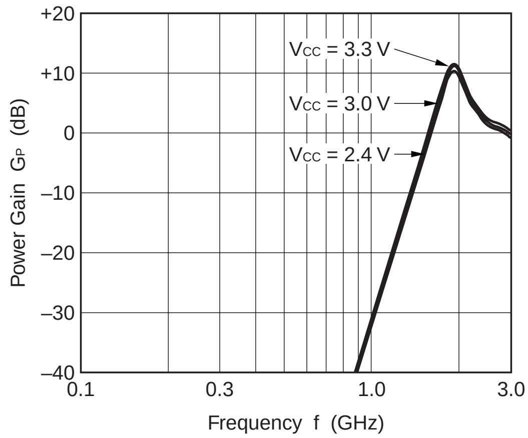
T_A = +25°C , V_{CC} = V_{out} = 3.0 V



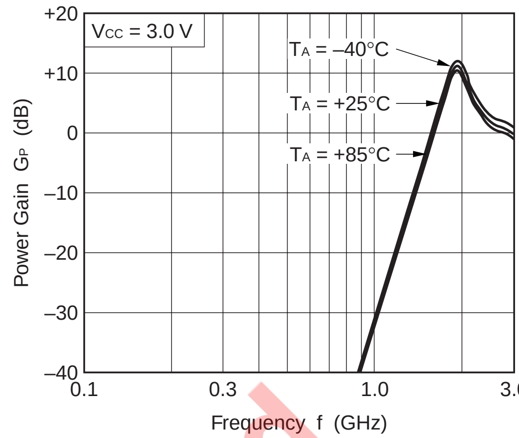


1.9 GHz OUTPUT PORT MATCHING

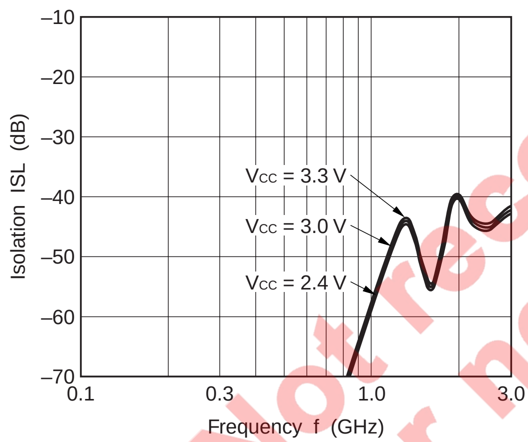
POWER GAIN vs. FREQUENCY



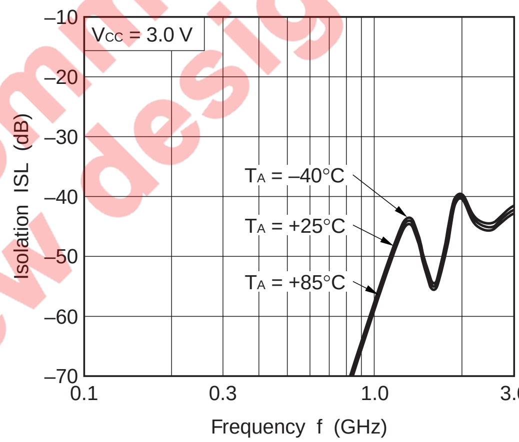
POWER GAIN vs. FREQUENCY



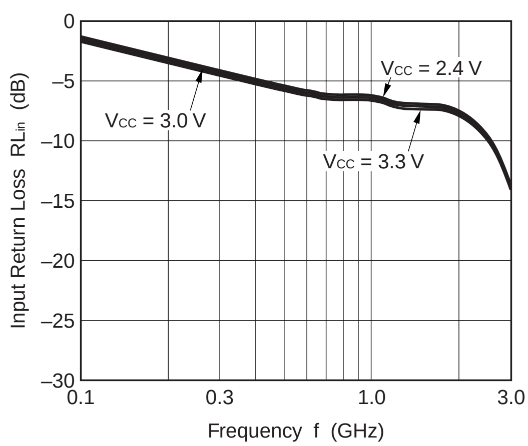
ISOLATION vs. FREQUENCY



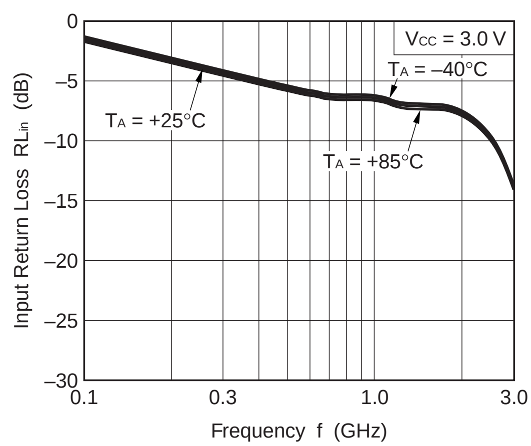
ISOLATION vs. FREQUENCY



INPUT RETURN LOSS vs. FREQUENCY

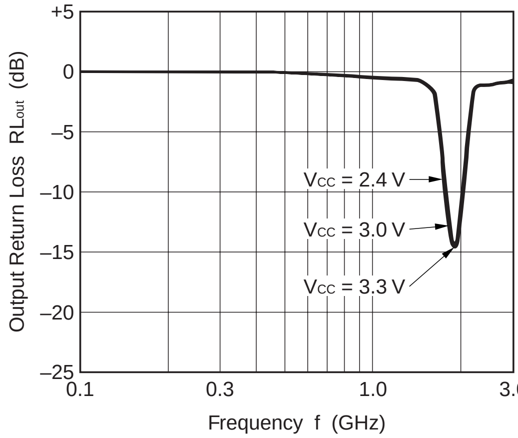


INPUT RETURN LOSS vs. FREQUENCY

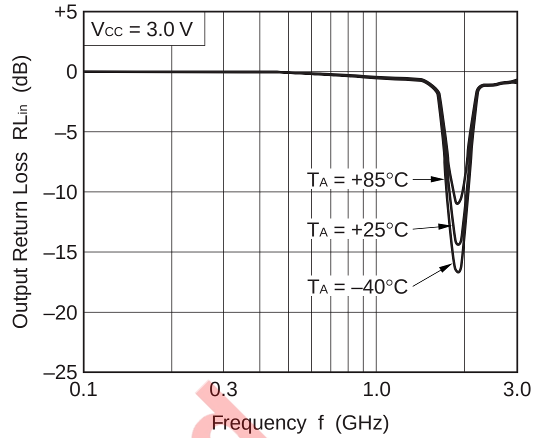


1.9 GHz OUTPUT PORT MATCHING

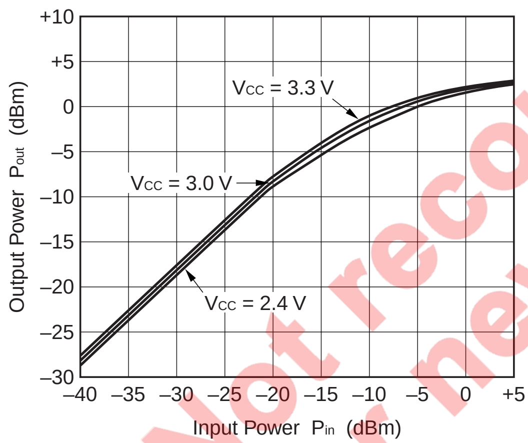
OUTPUT RETURN LOSS vs. FREQUENCY



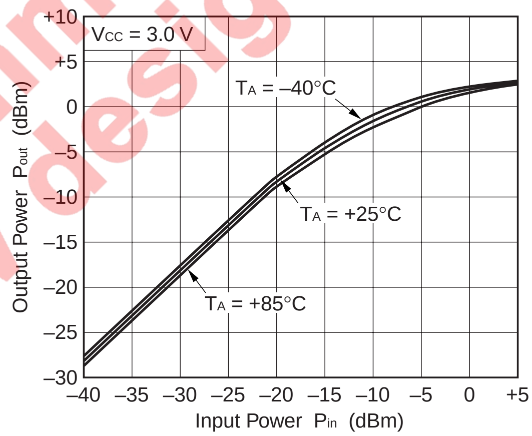
OUTPUT RETURN LOSS vs. FREQUENCY



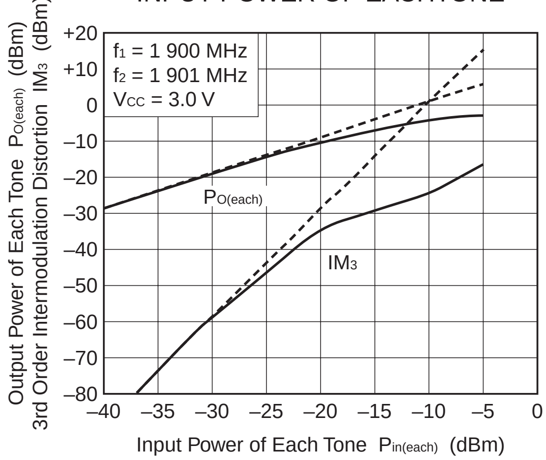
OUTPUT POWER vs. INPUT POWER



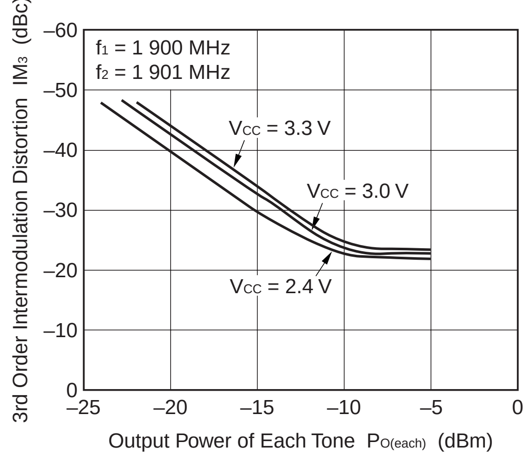
OUTPUT POWER vs. INPUT POWER



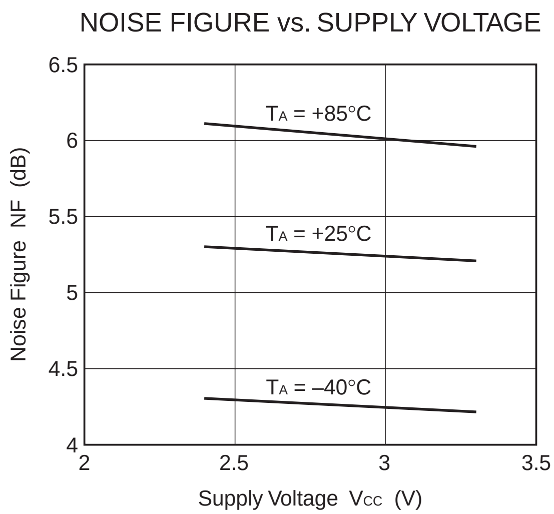
OUTPUT POWER OF EACH TONE, IM3 vs. INPUT POWER OF EACHTONE



3RD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE



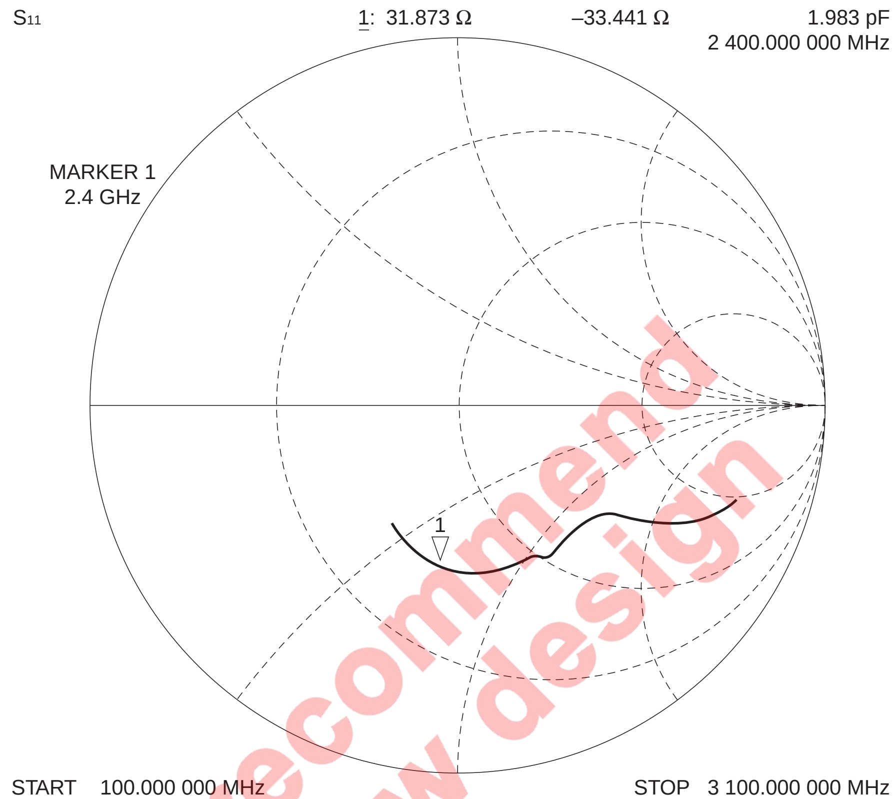
1.9 GHz OUTPUT PORT MATCHING

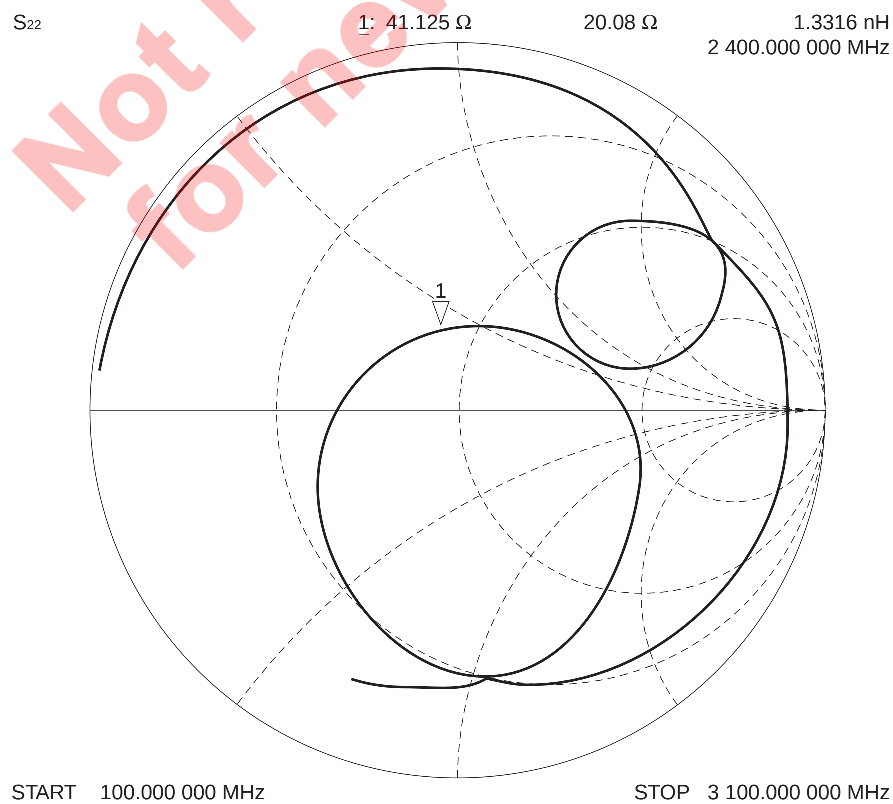


2.4 GHz OUTPUT PORT MATCHING

S-PARAMETERS (monitored at connector on board)

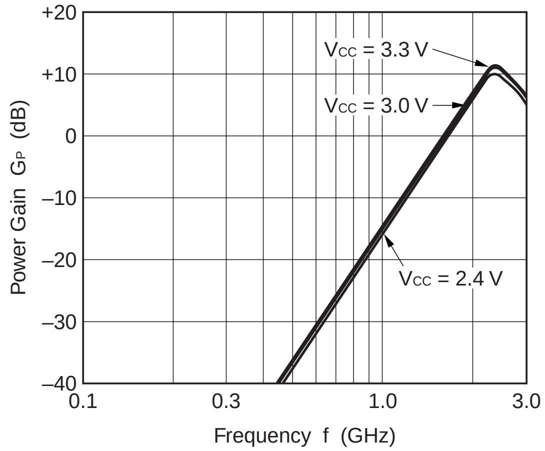
T_A = +25°C , V_{CC} = V_{out} = 3.0 V



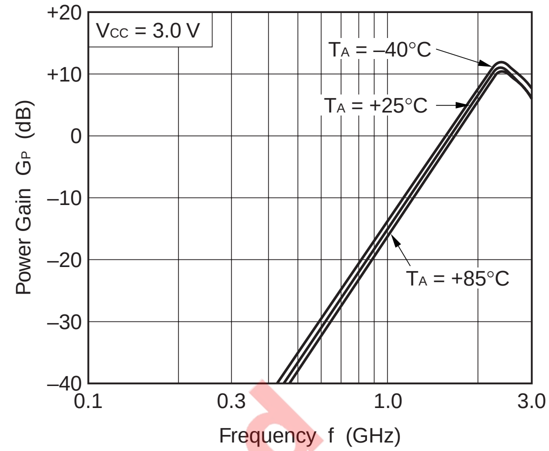


2.4 GHz OUTPUT PORT MATCHING

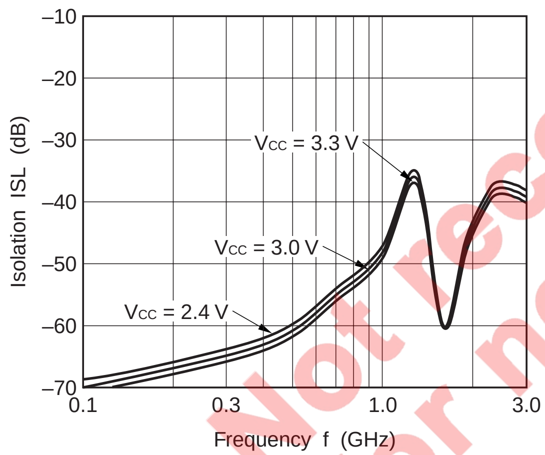
POWER GAIN vs. FREQUENCY



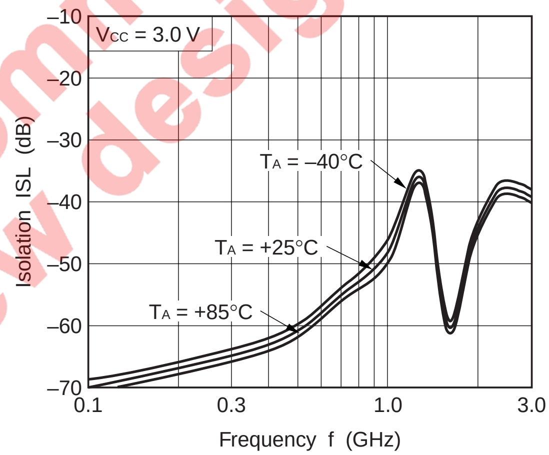
POWER GAIN vs. FREQUENCY



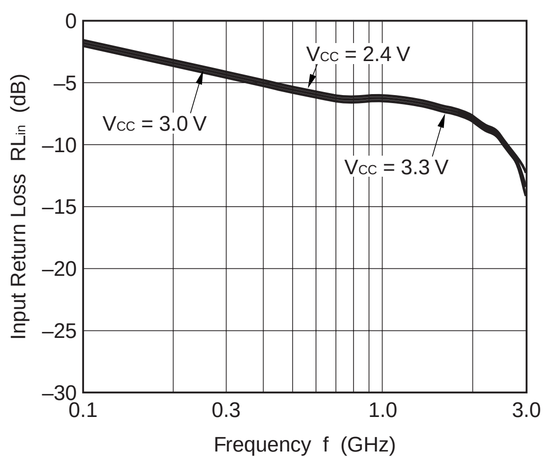
ISOLATION vs. FREQUENCY



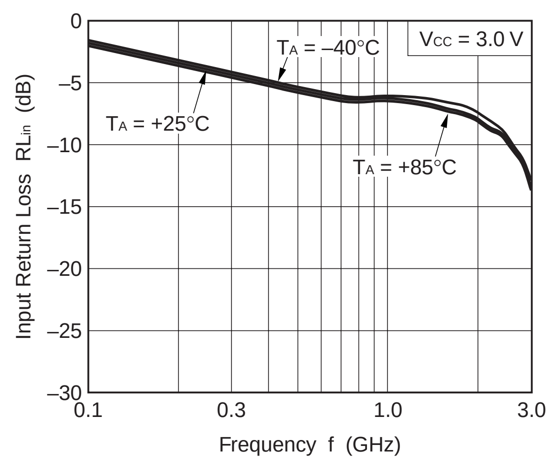
ISOLATION vs. FREQUENCY



INPUT RETURN LOSS vs. FREQUENCY

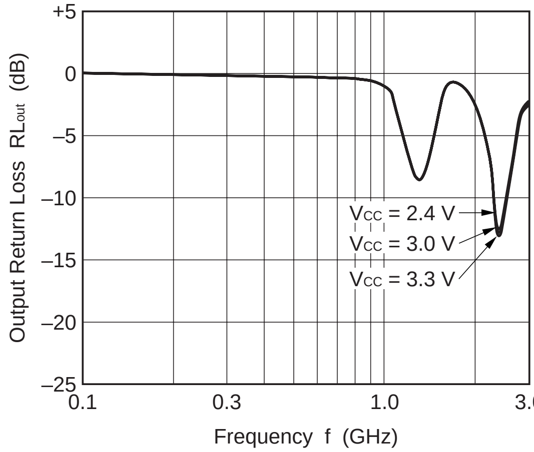


INPUT RETURN LOSS vs. FREQUENCY

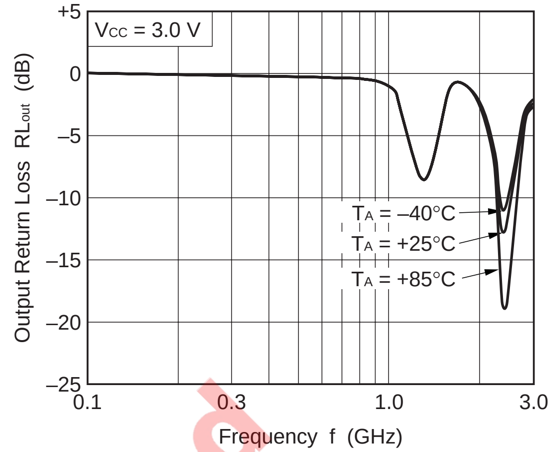


2.4 GHz OUTPUT PORT MATCHING

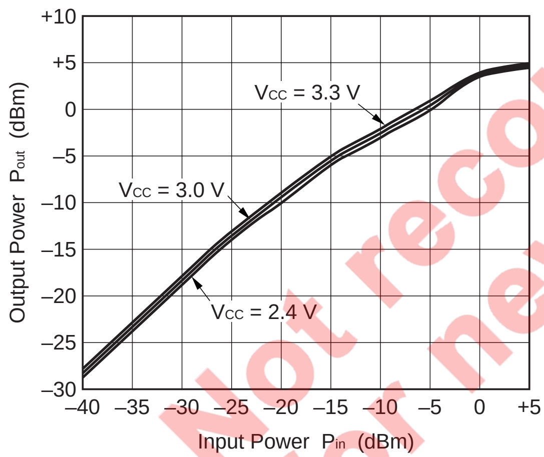
OUTPUT RETURN LOSS vs. FREQUENCY



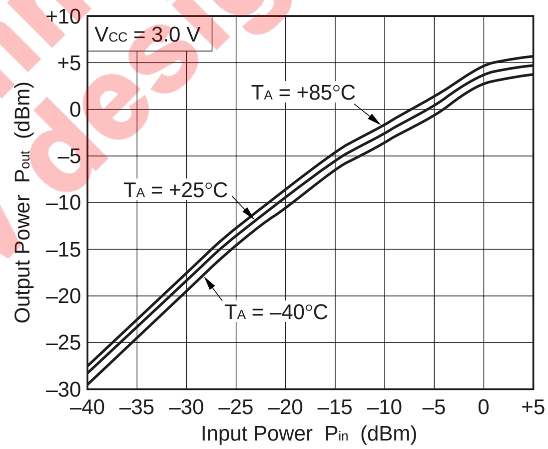
OUTPUT RETURN LOSS vs. FREQUENCY



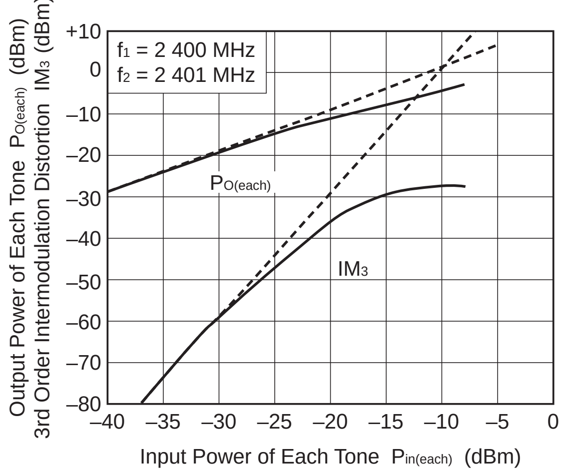
OUTPUT POWER vs. INPUT POWER



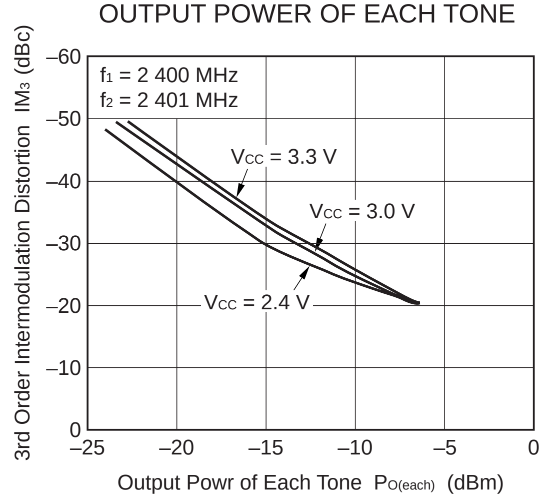
OUTPUT POWER vs. INPUT POWER



OUTPUT POWER OF EACH TONE, IM3 vs. INPUT POWER OF EACH TONE

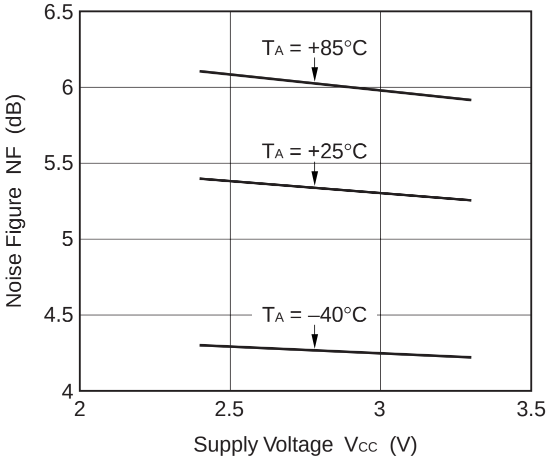


3RD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE



2.4 GHz OUTPUT PORT MATCHING

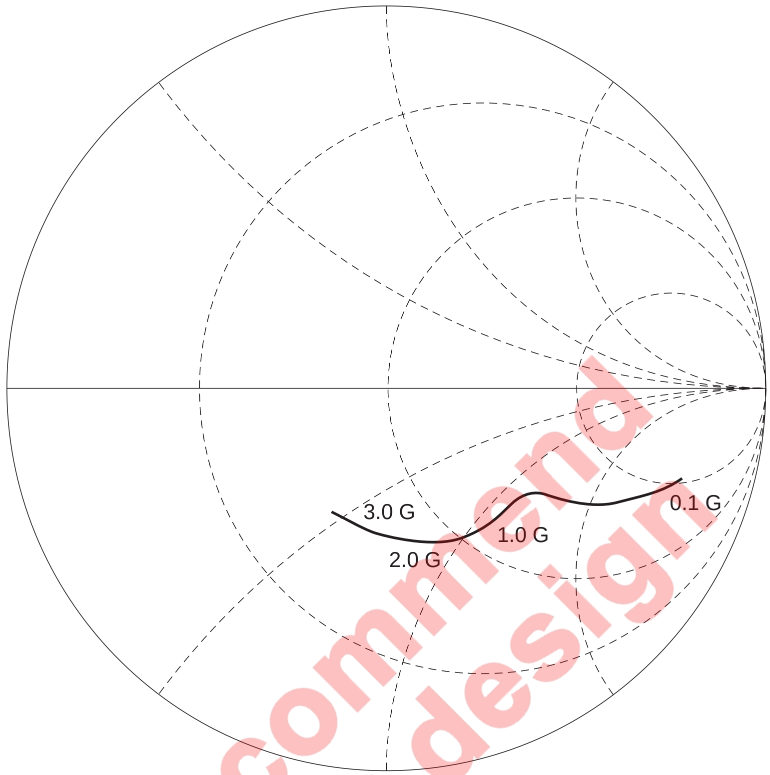
NOISE FIGURE vs. SUPPLY VOLTAGE



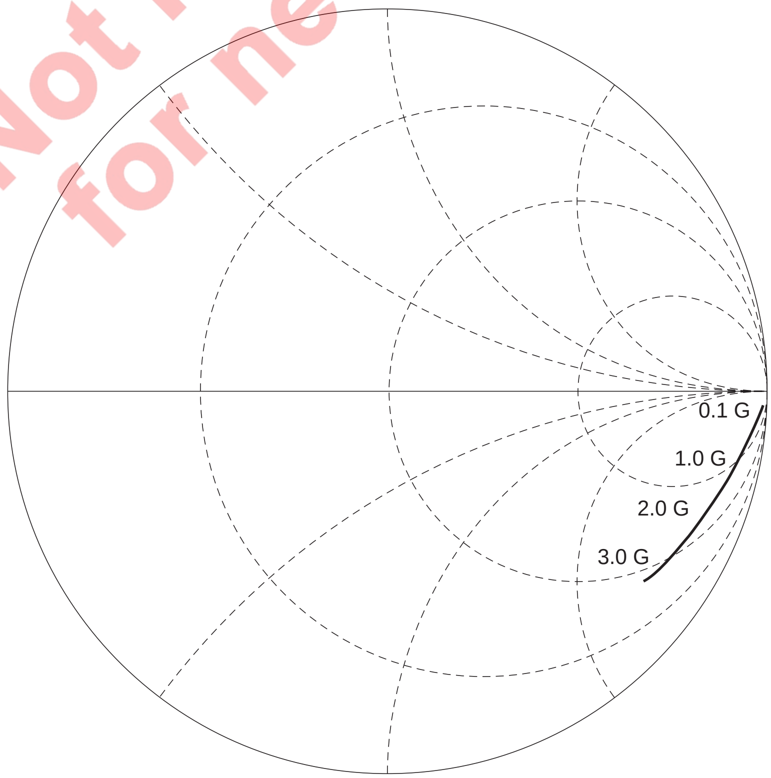
Remark The graphs indicate nominal characteristics.

S-PARAMETERS (V_{CC} = V_{out} = 3.0 V)

S_{11}-FREQUENCY



S_{22}-FREQUENCY



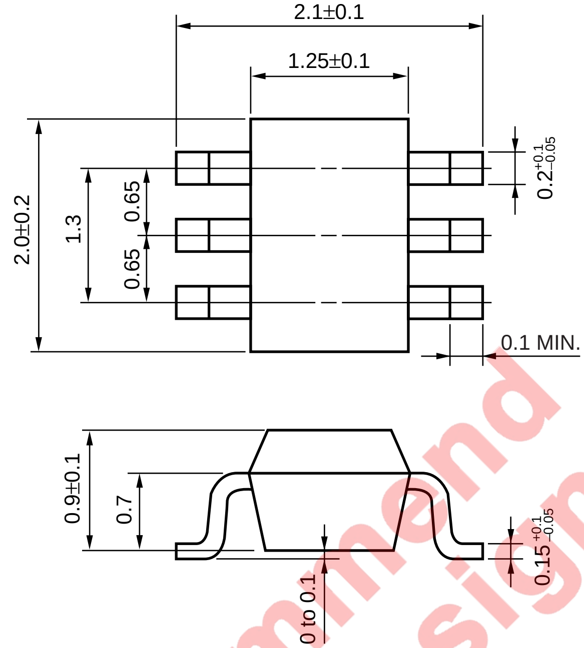
TYPICAL S-PARAMETER VALUES (T_A = +25°C)

$V_{CC} = V_{out}$ = 3.0 V, I_{CC} = 1.9 mA

FREQUENCY	S_{11}		S_{21}		S_{12}		S_{12}	
MHz	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.
100.0000	0.821	–16.9	1.060	180.0	0.002	83.1	0.996	–1.9
200.0000	0.692	–26.0	1.042	–177.2	0.004	57.2	0.994	–3.9
300.0000	0.598	–30.2	1.085	–174.3	0.004	56.5	0.985	–5.4
400.0000	0.540	–31.6	1.164	–172.7	0.004	40.1	0.973	–6.9
500.0000	0.501	–33.1	1.259	–172.3	0.006	36.8	0.958	–8.2
600.0000	0.484	–34.0	1.365	–173.8	0.004	27.3	0.952	–9.7
700.0000	0.477	–35.5	1.516	–176.1	0.005	41.3	0.948	–10.8
800.0000	0.474	–37.4	1.601	–179.4	0.006	47.2	0.946	–11.9
900.0000	0.469	–40.4	1.700	177.2	0.006	41.9	0.942	–13.0
1000.0000	0.466	–42.8	1.791	172.1	0.006	39.8	0.927	–14.4
1100.0000	0.453	–45.2	1.867	167.6	0.006	30.9	0.916	–15.5
1200.0000	0.447	–48.2	1.929	163.2	0.005	27.1	0.915	–16.8
1300.0000	0.442	–51.3	2.030	157.3	0.005	37.0	0.913	–17.8
1400.0000	0.439	–55.1	2.067	152.2	0.006	40.6	0.907	–19.0
1500.0000	0.439	–59.0	2.109	146.4	0.004	52.5	0.902	–19.8
1600.0000	0.439	–62.6	2.118	142.5	0.006	32.5	0.888	–21.1
1700.0000	0.433	–66.0	2.089	137.2	0.005	44.7	0.880	–22.0
1800.0000	0.427	–69.8	2.082	132.7	0.006	52.4	0.882	–23.0
1900.0000	0.416	–73.1	2.034	127.9	0.005	48.6	0.884	–24.1
2000.0000	0.405	–77.4	2.025	124.0	0.006	42.4	0.880	–25.0
2100.0000	0.399	–82.2	1.967	119.6	0.005	57.6	0.872	–26.1
2200.0000	0.395	–86.5	1.992	116.7	0.004	62.3	0.864	–27.2
2300.0000	0.398	–89.4	1.999	113.6	0.005	70.7	0.863	–28.1
2400.0000	0.396	–92.5	2.019	110.7	0.003	105.5	0.862	–29.2
2500.0000	0.394	–95.2	1.963	107.2	0.004	88.3	0.860	–30.4
2600.0000	0.382	–97.5	2.013	103.6	0.005	110.9	0.857	–31.2
2700.0000	0.368	–101.1	1.948	101.4	0.005	107.6	0.849	–32.1
2800.0000	0.360	–104.8	1.934	96.2	0.007	124.4	0.846	–33.2
2900.0000	0.359	–108.7	1.986	94.5	0.005	100.5	0.842	–34.7
3000.0000	0.357	–111.2	1.951	89.5	0.008	128.9	0.844	–35.4
3100.0000	0.355	–113.7	2.049	85.8	0.009	113.3	0.846	–36.7

PACKAGE DIMENSIONS

6-PIN SUPER MINIMOLD (UNIT: mm)



NOTES ON CORRECT USE

(1) Observe precautions for handling because of electro-static sensitive devices.
(2) Form a ground pattern as widely as possible to minimize ground impedance (to prevent undesired oscillation). All the ground pins must be connected together with wide ground pattern to decrease impedance difference.
(3) The bypass capacitor should be attached to V_{CC} line.
(4) The inductor (L) should be attached between output and V_{CC} pins. The L and series capacitor (C) values should be adjusted for applied frequency to match impedance to next stage.
(5) The DC capacitor must be attached to input pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

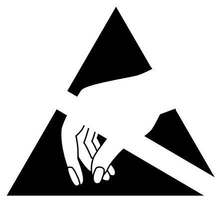
Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235°C or below Time: 30 seconds or less (at 210°C) Count: 3, Exposure limit: None[Note]	IR35-00-3
VPS	Package peak temperature: 215°C or below Time: 40 seconds or less (at 200°C) Count: 3, Exposure limit: None[Note]	VP15-00-3
Wave Soldering	Soldering bath temperature: 260°C or below Time: 10 seconds or less Count: 1, Exposure limit: None[Note]	WS60-00-1
Partial Heating	Pin temperature: 300°C Time: 3 seconds or less (per side of device) Exposure limit: None[Note]	–

Note After opening the dry pack, keep it in a place below 25°C and 65% RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document **SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E)**.

[MEMO]



ATTENTION

OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES