UPC844, UPC4744

Single Power Supply, High Speed, Wide Band, Quad Operational Amplifiers

DESCRIPTION

UPC844 and UPC4744 are high-speed version of the single-power general-purpose operational amplifier UPC451, UPC324, realizing high-speed response and high stability. By adopting a high speed PNP transistor circuit, various characteristics such as slew rate and gain bandwidth are improved, as compared to UPC451 and UPC324, the load capacity stability is also improved, with no crossover distortion.

It can be used widely for various application circuits such as single power supply AC amplifier, active filter, line driver, amplifier for light receiving element, etc.

Depending on the usage and operating ambient temperature range, the UPC844 is designed for extended temperature and suited for wide operating ambient temperature application, and UPC4744 is design for general purposes. Along with this series of lineup, the dual type operational amplifier, UPC842, UPC4742 with the same circuit configuration are also available.

FEATURES

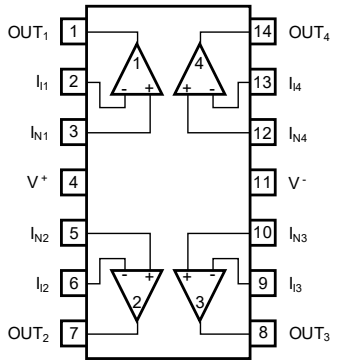
- Slew Rate (A_V = 1) 7 V/μs (TYP.) (V^+ = +5 V, V^- = GND)
- Gain Bandwidth Product (f = 100 kHz) 3.5 MHz (TYP.)
- Input Offset Voltage ±2 mV (TYP.)
- Input Offset Current ±6nA (TYP.)
- Operating Ambient Temperature
  UPC844G2 : T_A = -40 ~ +85 °C, UPC4744G2 : T_A = -20 ~ +80 °C
  UPC844GR-9LG : T_A = -40 ~ +125 °C, UPC4744GR-9LG : T_A = -40 ~ +85°C
- Stability to capacitive load (Capacitive load, 1000 pF)
- Build-in phase correction circuit.
- Built-in output short-circuit protection circuit.
- Standard pin (pin compatible) configuration of a quad operational amplifier.

ORDERING INFORMATION

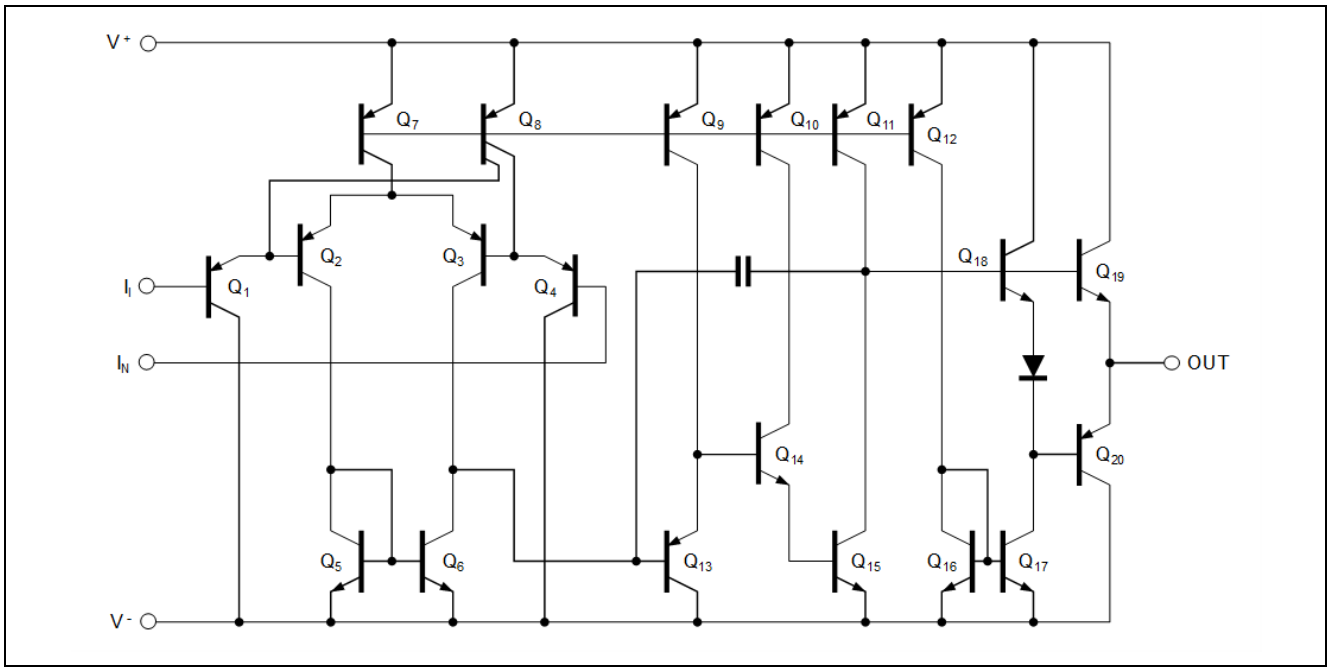
Order Name (1)	Selected Grade	Package
UPC844G2-AP	Standard	14-pin plastic SOP (5.72 mm (225))
UPC4744G2-AP	Standard	14-pin plastic SOP (5.72 mm (225))
UPC844GR-9LG-A	Standard	14-pin plastic TSSOP (5.72 mm (225))
UPC4744GR-9LG-A	Standard	14-pin plastic TSSOP (5.72 mm (225))

(1) Order names containing E1 or E2 indicate that the packaging format is embossed taping.
Pin 1 of E1 is on draw-out side, and pin 1 of E2 is at take-up side.

PIN CONFIGURATION (Top View)



EQUIVALENT CIRCUIT (1/4 Circuit)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	UPC844G2	UPC4744G2	UPC844GR-9LG	UPC4744GR-9LG	Unit
Power Supply Voltage Note 1	$V^+ - V^-$	-0.3 ~ +36				V
Differential Input Voltage	V_{ID}	±36				V
Input Voltage Note 2	V_I	V^- -0.3 ~ V^- +36				V
Output Applied Voltage Note 3	V_O	V^- -0.3 ~ V^+ +0.3				V
Total Power Dissipation Note 4	P_T	550				mW
Output Short Circuit Duration Note 5	t_S	Indefinite				s
Operating Ambient Temperature	T_A	-40 ~ +85	-20 ~ +80	-40 ~ +125	-40 ~ +85	°C
Storage Temperature	T_{stg}	-55 ~ +125		-55 ~ +150	-55 ~ +125	°C

【Note】 **1.** Note that reverse connections of the power supply may damage the ICs.

2. The allowable input voltage range without damaging or destructing the device. Independent to power supply voltage range.
Do not apply voltage equivalent to V^- (GND) - 0.3 V or less.
Note that the operational amplifier will operate normally when the input voltage applied is within the common mode input voltage range.

3. The input voltage range that can be applied to the output pin externally without deteriorating or damaging the device characteristic. The permitted input voltage that can be applied regardless of the power supply voltage. This specification also includes precaution during transition state such as ON/OFF, etc.

4. This is the value when the glass epoxy substrate (size: 100 mm x 100 mm, thickness: 1 mm, 15% of the substrate area where only one side is copper foiled is filling wired) is mounted.
Note that restrictions will be made to the following conditions for each product, and the de-rating ratio depending on the operating ambient temperature.

UPC844G2, 4744G2 : De-rate -5.5 mW/°C when T_A > 25 °C
(Junction − ambient thermal resistance $R_{th(J-A)}$ = 182°C/W)
UPC844GR-9LG : De-rate -7.0 mW/°C when T_A > 71 °C
(Junction − ambient thermal resistance $R_{th(J-A)}$ = 144°C/W)
UPC4744GR-9LG : De-rate -7.0 mW/°C when T_A > 46 °C
(Junction − ambient thermal resistance $R_{th(J-A)}$ = 144°C/W)

5. Please use the total loss and the de-rating factor of Note 4.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage (V^- = GND)	V^+	+3	+5 ~ +30	+32	V
Power Supply Voltage (Dual Supply)	$V^\pm$	±1.5		±16	V
Output Current	I_O			±10	mA
Capacitive Load (A_V = +1)	C_L			1000 Note 6	pF

【Note】 **6.** This is the value when feedback resistor (Rf) = 0 Ω.

ELECTRICAL CHARACTERISTICS

(T_A = 25 °C, $V^\pm$ = ±15 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		±2	±6	mV	
Input Offset Current	I_{IO}		±6	±75	nA	
Input Bias Current Note 7	I_B		130	500	nA	
Large Signal Voltage Gain	A_V	25000	300000			R_L ≥ 2 kΩ, V_O = ±10 V
Circuit Current Note 8	I_{CC}		7.5	11	mA	I_O = 0 A
Common Mode Rejection Ratio	CMR	70	86		dB	
Supply Voltage Rejection Ratio	SVR	70	93		dB	
Output Voltage Swing	V_{Om1}	±13.7	+14		V	R_L ≥ 10 kΩ
			-14.3			
	V_{Om2}	±13.5			V	R_L ≥ 2 kΩ
Common Mode Input Voltage Range	V_{ICM}	V^-		V^+ -1.8	V	
Slew Rate	SR		8.5		V/μs	A_V = 1 (Rise)
Gain Bandwidth Product	GBW		3.5		MHz	f = 100 kHz
Channel Separation			120		dB	f = 20 Hz ~ 20 kHz

(T_A = 25 °C, V^+ = +5 V, V^- = GND)

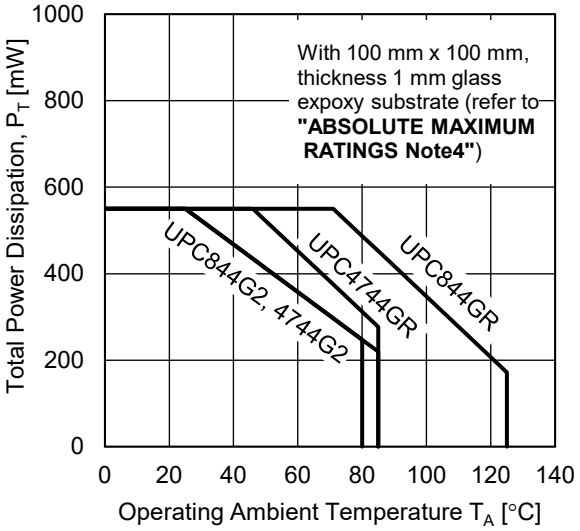
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Input Offset Voltage	V_{IO}		±2	±5	mV	
Input Offset Current	I_{IO}		±6	±75	nA	
Input Bias Current Note 7	I_B		150	500	nA	
Large Signal Voltage Gain	A_V	25000	300000			R_L ≥ 2 kΩ
Circuit Current Note 8	I_{CC}		6	9	mA	I_O = 0 A
Common Mode Rejection Ratio	CMR	70	80		dB	
Supply Voltage Rejection Ratio	SVR	70	95		dB	
Output Voltage Swing	V_{Om}	3.7	4.0		V	R_L ≥ 2 kΩ (Connected to GND)
		0	0			
Common Mode Input Voltage Range	V_{ICM}	0		V^+ -1.8	V	
Output Source Current	$I_{O\ SOURCE}$	10	30		mA	$V_{IN\ (+)}$ = +1 V, $V_{IN\ (-)}$ = 0 V
Output Sink Current	$I_{O\ SINK}$	10	30		mA	$V_{IN\ (+)}$ = 0 V, $V_{IN\ (-)}$ = +1 V
Slew Rate	SR		7		V/μs	A_V = 1 (Rise)

【Note】 **7.** The current flow direction of the input bias is out from the IC because the first stage of the IC composed of PNP transistor.

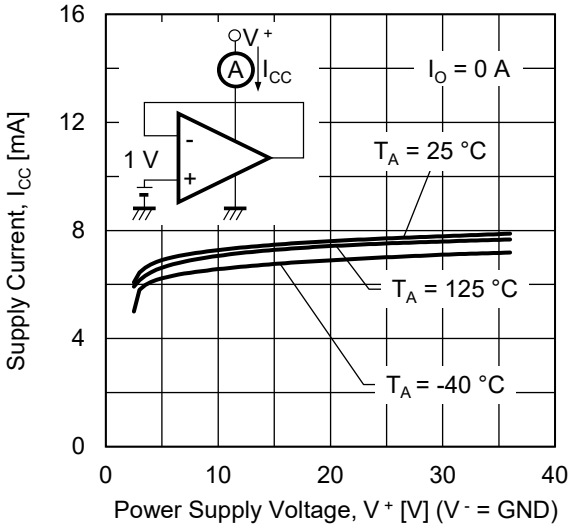
8. Current flowing through the internal circuit. This current flow regardless of the channel used.

CHARACTERISTICS CURVE (T_A = 25 °C, TYP.) (REFERENCE VALUE)

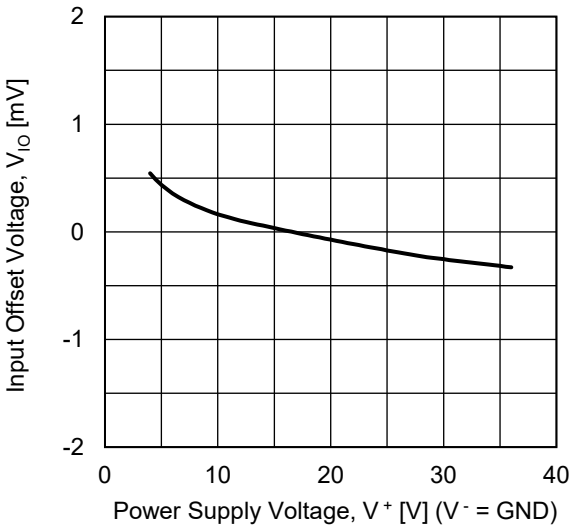
P_T vs. T_A



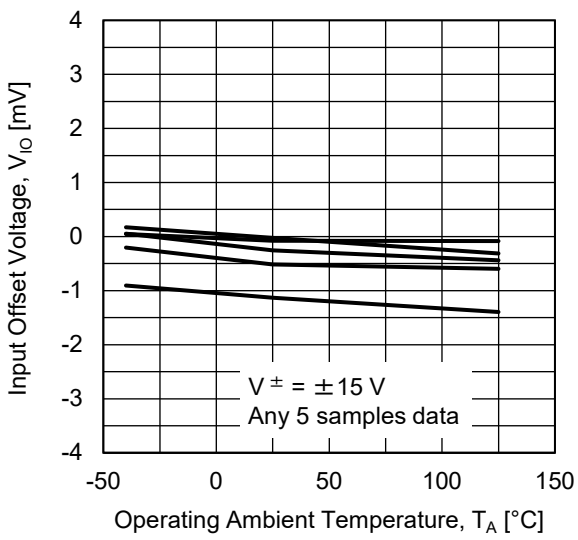
I_{CC} vs. V^+



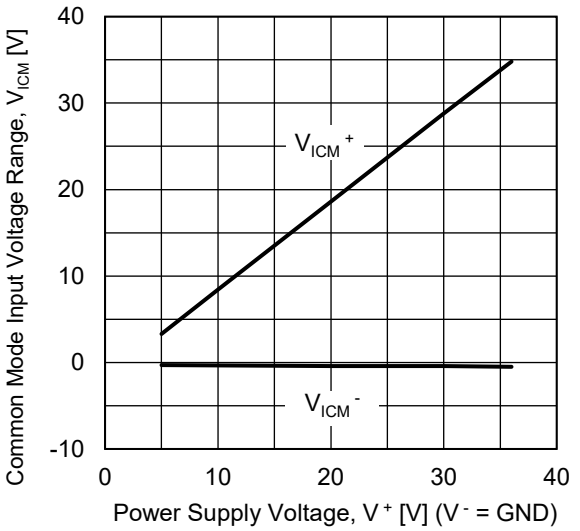
V_{IO} vs. V^+



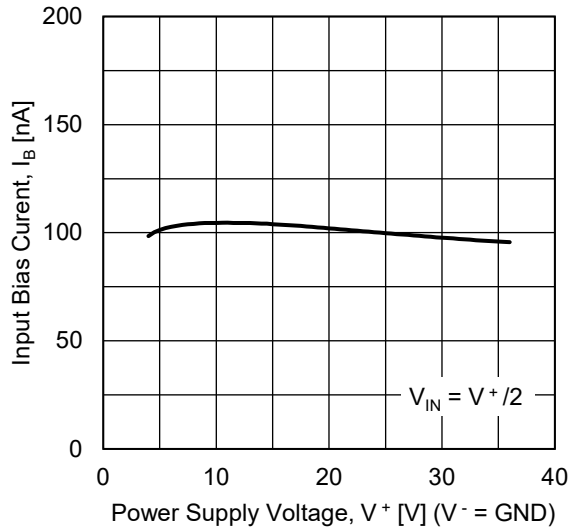
V_{IO} vs. T_A



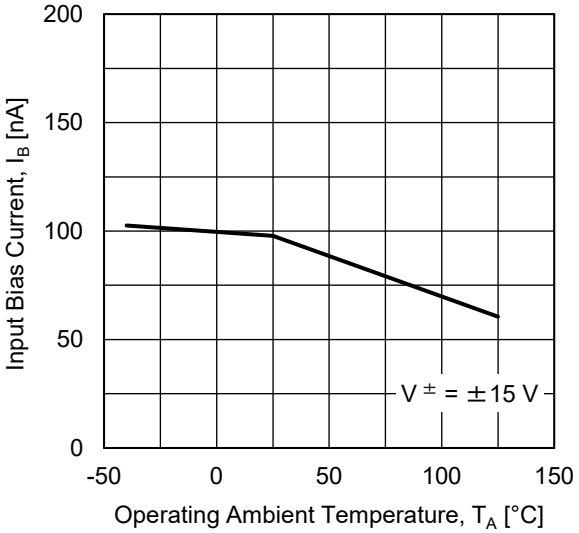
V_{ICM} vs. V^+



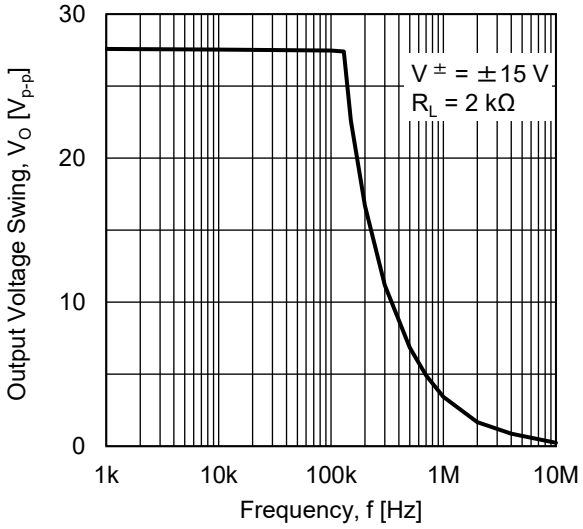
I_B vs. V^+



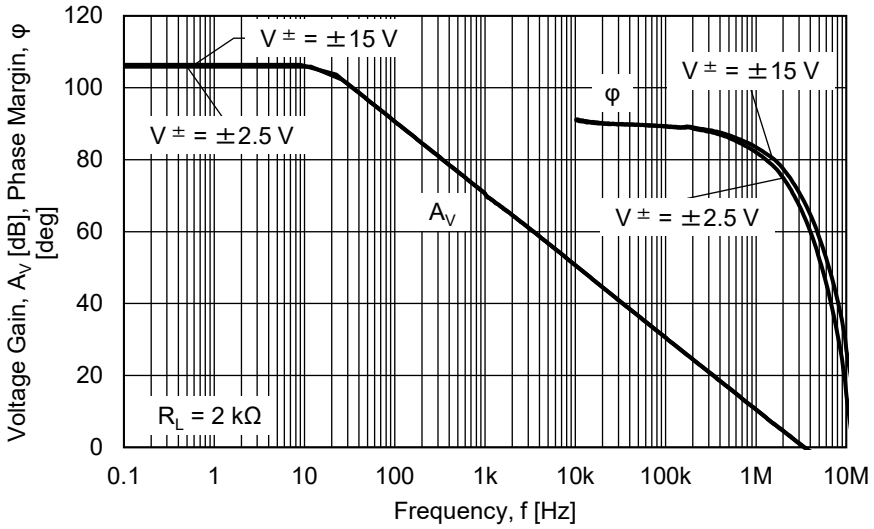
I_B vs. T_A



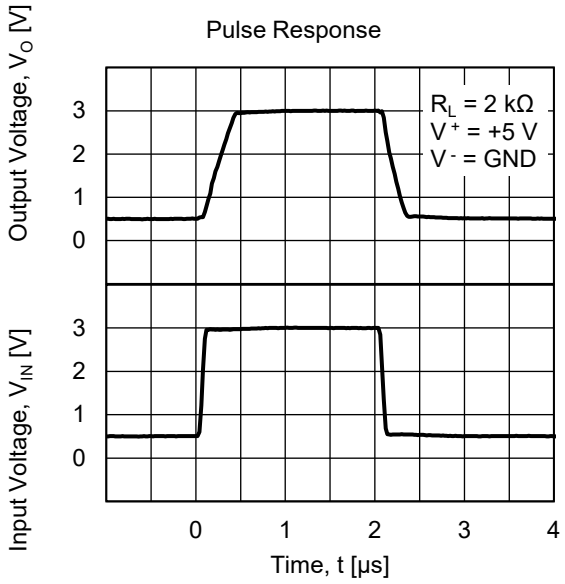
V_O vs. f



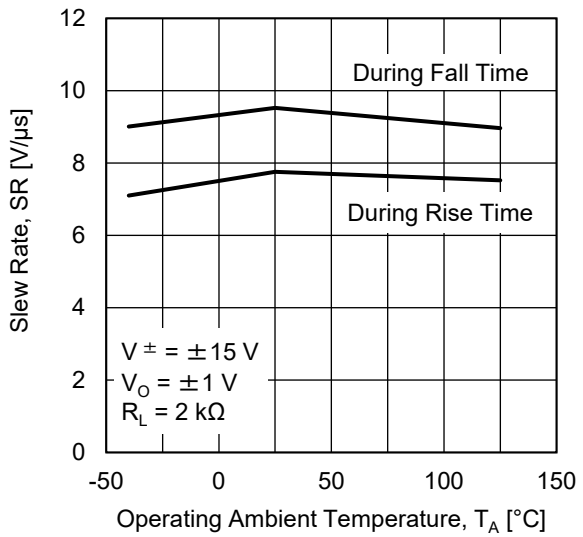
A_V, φ vs. f

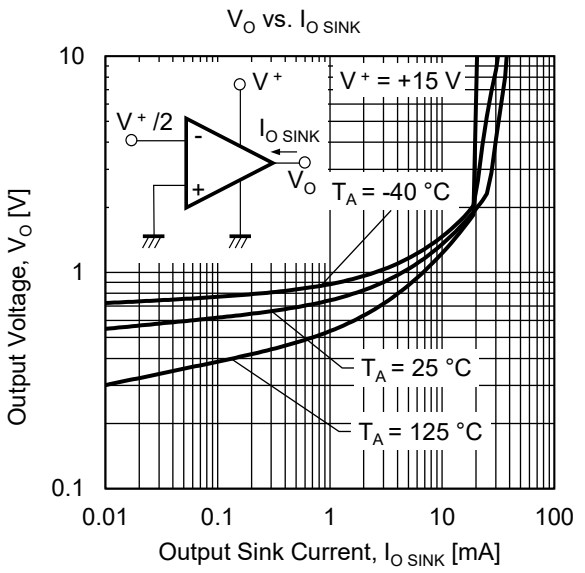


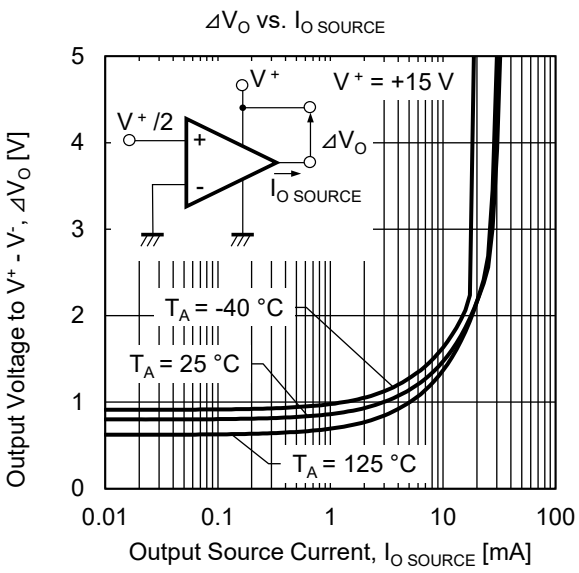
Pulse Response



SR vs. T_A




V_O vs. $I_{O\ SINK}$
10
1
0.1
0.01
0.1
1
10
100
Output Voltage, V_O [V]
Output Sink Current, $I_{O\ SINK}$ [mA]
V^+
V^+ = +15 V
V^+ /2
$I_{O\ SINK}$
V_O
T_A = -40 °C
T_A = 25 °C
T_A = 125 °C

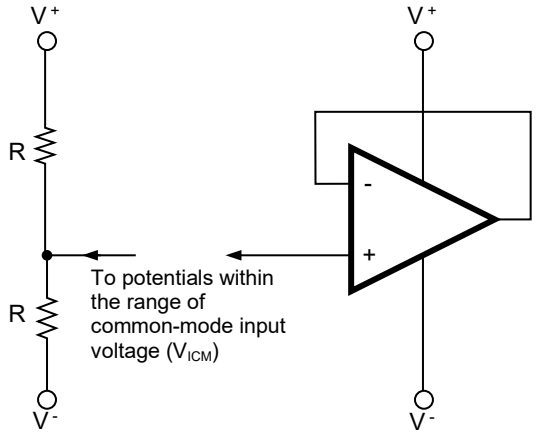

ΔV_O vs. $I_{O\ SOURCE}$
5
4
3
2
1
0
0.01
0.1
1
10
100
Output Voltage to V^+ - V^-, ΔV_O [V]
Output Source Current, $I_{O\ SOURCE}$ [mA]
V^+
V^+ = +15 V
V^+ /2
ΔV_O
$I_{O\ SOURCE}$
T_A = -40 °C
T_A = 25 °C
T_A = 125 °C

USE WITH PRECAUTIONS

- **Managing unused circuits**

If there is an unused circuit, the following connection is recommended.

Process example of unused circuits



Remark : In this example, an intermediate potential between V^+ and V^- is applied.

- **Ratings of input/output pin voltage**

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the input pin is lower than V^-, or the output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- **Range of common-mode input voltage**

When the supply voltage does not meet the condition of electrical characteristics, the range of common-mode input voltage is as follows.

V_{ICM} (TYP.): $V^- \sim V^+ - 1.8$ (V) (T_A = 25°C).

During designing, do include some tolerance by considering temperature characteristics etc.

- **Maximum output voltage**

The TYP. value range of the maximum output voltage when the supply voltage does not meet the condition of electrical characteristics is as follows:

$V_{om}{}^+$ (TYP.) : V^+ -1 [V] (T_A = 25 °C), $V_{om}{}^-$ (TYP.) : V^- +0.7 [V] (T_A = 25 °C)

During designing, do include some tolerance by considering characteristics variation, temperature characteristics and so on. In addition, also note that the output voltage range ($V_{om}{}^+ - V_{om}{}^-$) will become narrow when the output current increases.

- **Output Operation**

This IC will not be able to sink output current when the output voltage is V^- + 0.7 V and below. In this case, the output voltage level can be improved to the V^- side by connecting the load resistor between the output terminal and V^- to sink the current at the load resistor. (The effect will differ depending on the flow of current in the load resistance.)

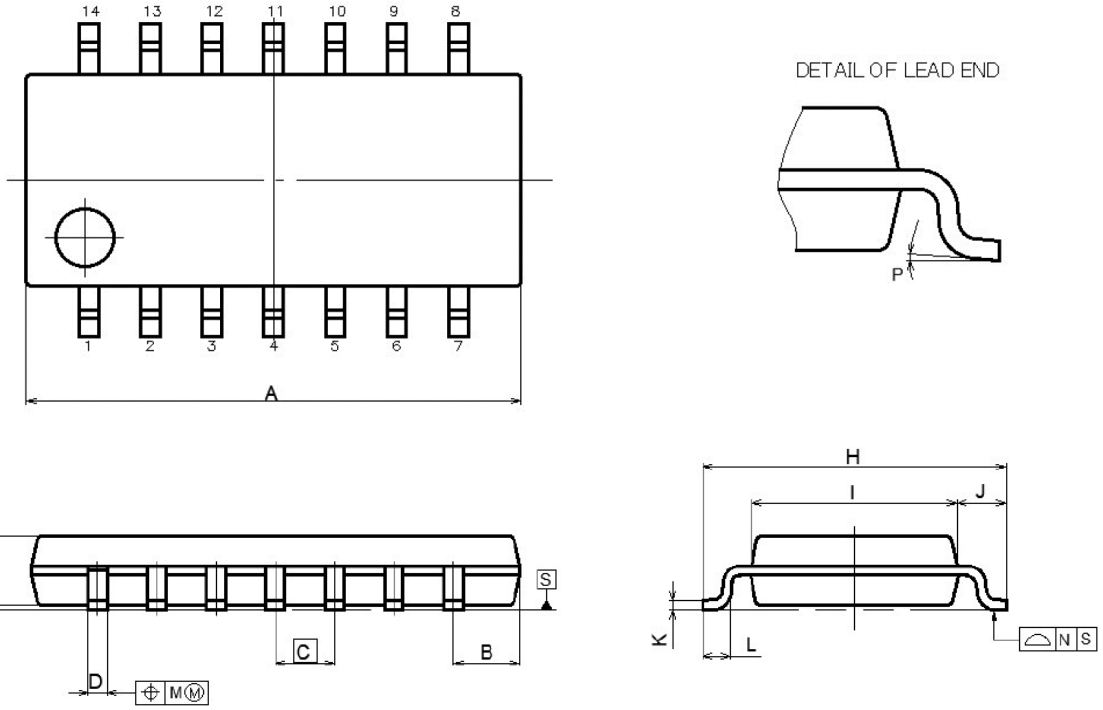
- **Handling of ICs**

When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuates due to piezoelectric effect. Therefore, pay attention to warpage or bending of a board.

PACKAGE DRAWINGS

14-PIN PLASTIC SOP

JEITA Package code	RENESAS code	MASS (TYP.) [g]
P-LSOP14-4.4×10.2-1.27	PLSP0014DB-A	0.17[g]



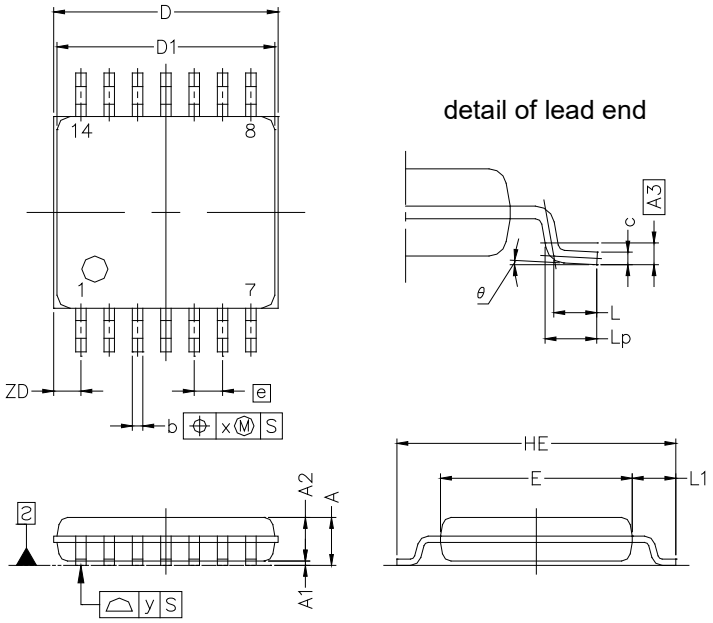
NOTE
EACH LEAD CENTERLINE IS LOCATED WITHIN 0.12 MM OF
ITS TRUE POSITION(T.P.) AT MAXIMUM MATERIAL CONDITION.

(UNIT:mm)

ITEM	DIMENSIONS
A	10.2±0.2
B	1.42MAX
C	1.27(T.P)
D	0.40±0.05
E	0.1±0.1
F	1.59±0.20
G	1.49±0.1
H	6.5±0.2
I	4.4±0.1
J	1.05±0.15
K	0.2±0.07
L	0.6±0.20
M	0.1MAX
N	0.1MAX
P	4°±4°

14-PIN PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.) [g]
P-TSSOP14-0225-0.65	PTSP0014JB-A	P14GR-65-9LG-1	—



Unit : mm

ITEM	MILLIMETERS
D	5.15 ±0.15
D1	5.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 +0.06 -0.05
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
θ	3° +5° -3°
e	0.65
x	0.10
y	0.10
ZD	0.625

NOTE

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

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