μPD166034T1U

R07DS1168EJ0200
Rev.2.00
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INTELLIGENT POWER DEVICE

1. Overview

1.1 Description

Family:

μPD166034T1U is part of 2nd Generation Intelligent Power Devices (IPD). They are N-channel high-side switches with charge pump, voltage controlled input, diagnostic feedback with proportional load current sense and embedded protection function. Family includes up to 14 devices depending on on-state resistance, package and channel number combination.

Scalability:

Variety of on-state resistance combined with standardized package on pin-out give user high flexibility for unit design depending on target load.

Robustness:

Because of advanced protection method, 2nd Generation Intelligent Power Devices achieve high robustness against long term and repetitive short circuit condition.

1.2 Features

- Built-in charge pump
- 3.3V compatible logic interface
- Low standby current
- Short circuit protection
  - Shutdown by over current detection
  - Power limitation protection by over load detection (Power limitation: current limitation with delta Tch control)
  - Absolute Tch over temperature protection
- Built-in diagnostic function
  - Proportional load current sensing
  - Defined fault signal in case of abnormal load condition
- Loss of ground protection
- Under voltage lock out
- Active clamp operation at inductive load switch off
- Cross current protection in case of H-bridge high side usage
- Reverse battery protection by turn on the output
- AEC Qualified
- RoHS compliant

1.3 Application

- Light bulb switching from 55W to 75W according to on-state resistance
- Switching of all types of 14V DC grounded loads, such as LED, inductor, resistor and capacitor
- Power supply switch, fail-safe switch of 14V DC grounded system

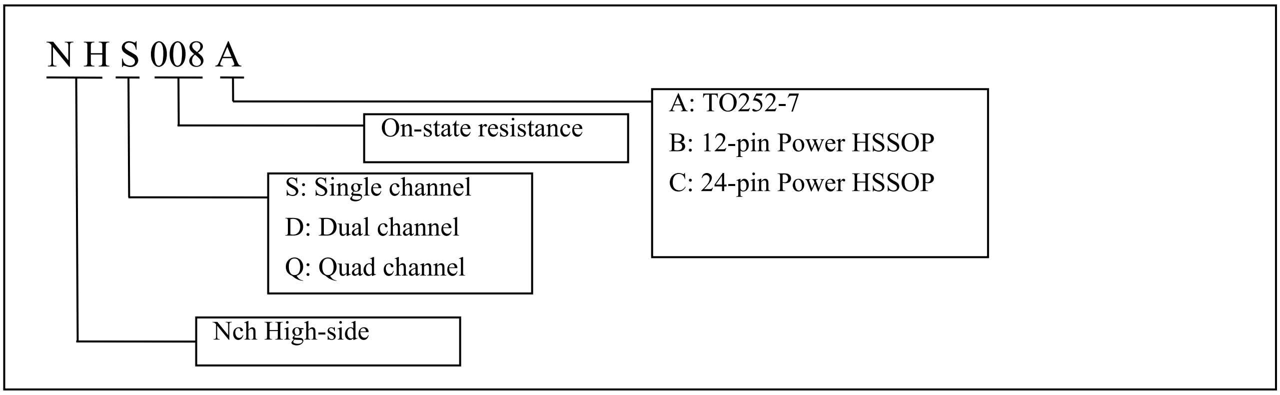
Note: The information contained in this document is the one that was obtained when the document was issued, and may be subject to change.

2. Ordering Information

Part No.	Nick name	Lead plating	Packing	Package
UPD166034T1U-E1-AY	NHS008A	Pure Matte Sn	Tape 2500 p/reel	TO252-7

Note: Part No. and Nick name are tentative and might change at anytime without notice.

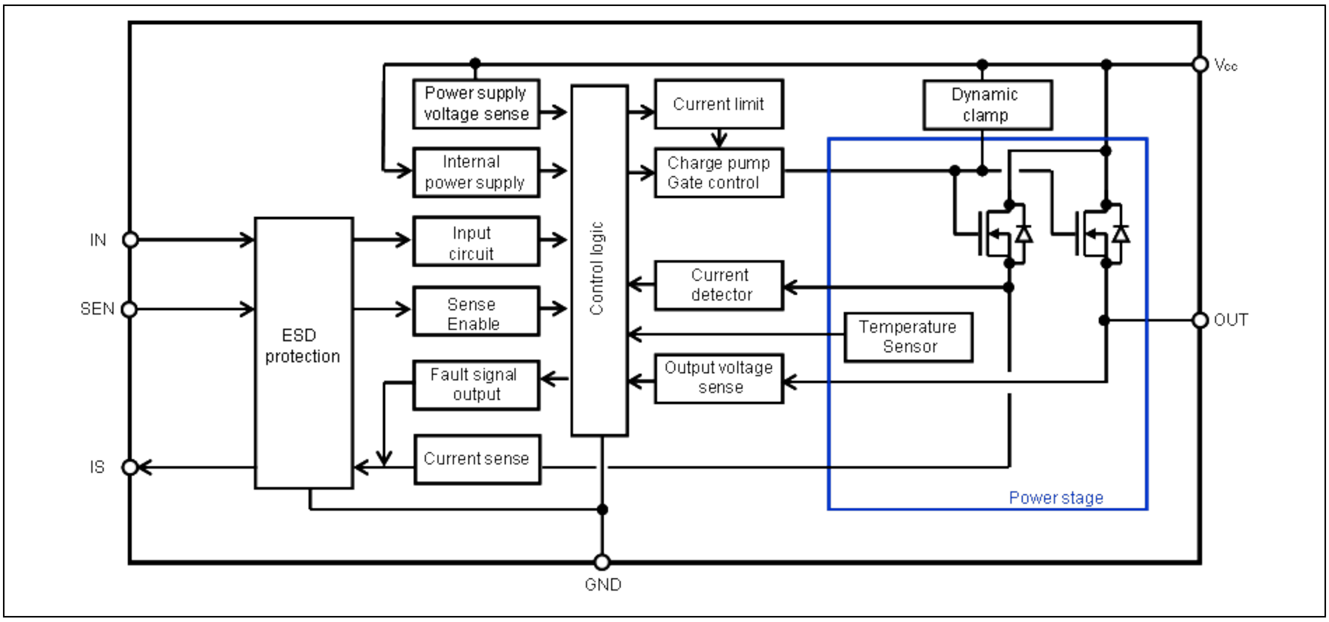
2.1 Nick name



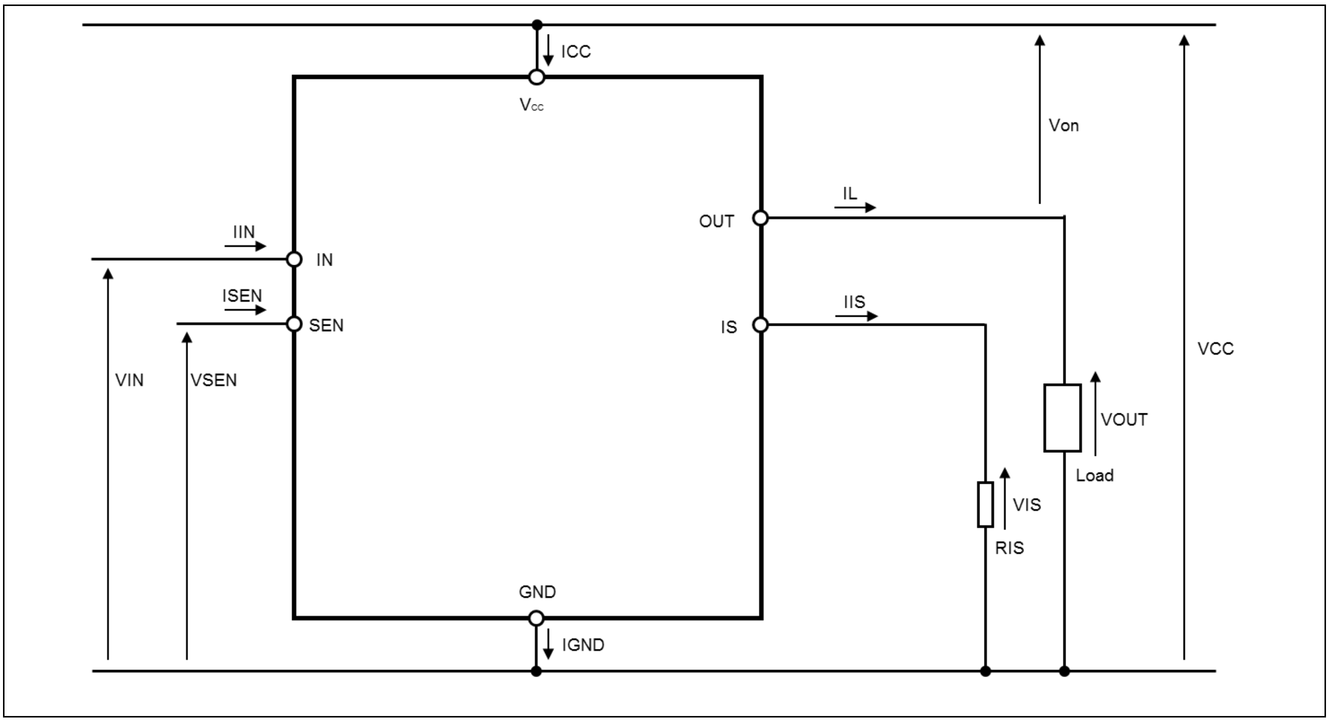
3. Specification

3.1 Block Diagram

3.1.1 Nch High-side Single Device



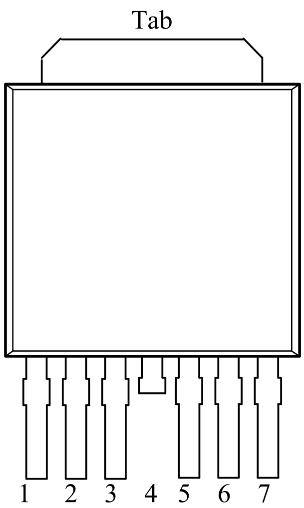
Voltage and Current Definition



3.2 Pin Configuration

3.2.1 TO252-7 Pin Configuration

Pin No.	Terminal Name
1	OUT
2	GND
3	IN
4, Tab	VCC
5	IS
6	SEN
7	OUT



Pin function

Terminal Name	Pin function	Recommended connection
GND	Ground connection	Connected to GND through a 100 Ω resistor Refer chapter 6.
IN	Input signal	Connected to MCU port through 2k-50K serial resistor.
IS	Current sense and Diagnosis output signal	Connected to GND through a 0.67K-5K resistor. Not connect if this pin is not used.
SEN	Sense enable input	Connected to MCU port through 2k-50K serial resistor. Not connect if this pin is not used.
OUT	Protected high-side power output	Connected to load with small 50-100nF capacitor in parallel.
VCC	Positive power supply for logic supply as well as output power supply	Connected to battery voltage with small 100nF capacitor in parallel.

3.3 Absolute Maximum Ratings

Ta=25°C, unless other specified

Parameter	Symbol	Rating	Unit	Test Condition
Vcc Voltage	V_{CC}	28	V	
Vcc Voltage at reverse battery condition	$-V_{CC}$	-16	V	RL=1.5Ω, t<2min, RIN=2kΩ, RSEN=2kΩ, RIS=1kΩ, RGND=100Ω
Vcc voltage under Load Dump condition	$V_{load\ dump}$	42	V	RI=1Ω, RL=1.5Ω, RIS=1kΩ, RIN=2kΩ, RSEN=2kΩ, RGND=100Ω, td=400ms
Load Current	I_L	Self limited	A	
Total power dissipation for whole device (DC)	P_D	1.85	W	Ta=85°C, Device on 50mm×50mm×1.5mm epoxy PCB FR4 with 6 cm^2 of 70 μm copper area
Voltage at IN pin	V_{IN}	-2 ~ 16	V	DC RIN=2kΩ
		-16		At reverse battery condition, t<2min, RIN=2kΩ, RSEN=2kΩ
IN pin current	I_{IN}	10	mA	DC
Voltage at IS pin	V_{IS}	VCC	V	DC RIS=1kΩ
		-16	V	At reverse battery condition, t<2min, RL=1.5Ω, RIS=1kΩ
IS Reverse current at reverse battery condition	$I_{IS(Rev)}$	-30	mA	At reverse battery condition, t<2min, RL=1.5Ω
Voltage at SEN pin	V_{SEN}	-2 ~ 16	V	DC RSEN=2kΩ
		-16		At reverse battery condition, t<2min RIN=2kΩ, RSEN=2kΩ
SEN pin current	I_{SEN}	10	mA	DC
Channel Temperature	Tch	-40 to +150	°C	
Storage Temperature	Tstg	-55 to +150	°C	
ESD susceptibility	V_{ESD}	2000	V	HBM: AEC-Q100-002 std. R=1.5kΩ, C=100pF — All pin
		4000		HBM: IEC61000-4-2 std. R=330Ω, C=150pF, 100nF at VCC and OUT — VCC, OUT
		200	V	MM: AEC-Q100-003 std. R=0Ω, C=200pF
Inductive load switch-off energy dissipation single pulse	EAS	210	mJ	VCC=13.5V, Tch,start<150°C, RL=1.5Ω
Inductive load switch-off energy dissipation repetitive pulse	EAR	150	mJ	VCC=13.5V, Tch,start=85°C, RL=1.5Ω

Remark) All voltages refer to ground pin of the device

3.4 Thermal Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Thermal characteristics	Rth(ch-a)		35		°C/W	According to JEDEC JESD51-2, -5, -7 on FR4 2s2p board
	Rth(ch-c)		0.8		°C/W	

3.5 Electrical Characteristics

Operation function

Tch=-40 to 150°C, Vcc=7 to 18V, unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition	
Operating Voltage	V_{CC}	4.5		28	V	VIN=4.5V, RL=1.5Ω	
Operating current	I_{GND}		2.2	4	mA	VIN=4.5V	
Output Leakage current	$I_{L(off)}$			0.5	μA	Tch=25°C	VCC=13.5V, VIN=0V, VSEN=0V, VIS=0V, VOUT=0V, VGND=0V
				5		Tch=-40~125°C	
Standby current	$I_{CC(off)}$			0.5	μA	Tch=25°C	VCC=13.5V, VIN=0V, VSEN=0V, VIS=0V, VOUT=0V, VGND=0V
				1.5		Tch=-40~85°C	
On-state resistance	Ron		8		mΩ	Tch=25°C	IL=9A
				16		Tch=150°C	
Low level IN pin voltage	V_{IL}			0.8	V		
High level IN pin voltage	V_{IH}	2.5			V		
Low level IN pin current	I_{IL}	2		25	μA	VIN=0.8V	
High level IN pin current	I_{IH}	2		25	μA	VIN=2.5V	
Clamping IN pin voltage [1)]	V_{ZIN}	5	6		V		
Low level SEN pin voltage	V_{SENL}			0.8	V		
High level SEN pin voltage	V_{SENH}	2.5			V		
Low level SEN pin current	I_{SENL}	2		25	μA	VSEN=0.8V	
High level SEN pin current	I_{SENH}	2		25	μA	VSEN=2.5V	
Clamping SEN pin voltage[1)]	V_{ZSEN}	5	6		V		
Under voltage shutdown	$V_{CC(Uv)}$			4.5	V		
Under voltage restart	$V_{CC(Cpr)}$			5.0	V		
Turn on time	ton			200	μs	VCC=13.5V, RL=1.5Ω	
Turn on delay time	td(on)			100	μs		
Turn off time	toff			200	μs		
Turn off delay time	td(off)			150	μs		
Slew rate on	dV/dton			1.0	V/μs		
Slew rate off	-dV/dtoff			1.0	V/μs		
Switching drift[1)]	ton-toff	-50		+50	μs	Vcc = 9 to 18V drift from Vcc=13.5V, Tch=-40 to 150°C drift from Tch=25°C ton; Vout=Vcc-1.5V after input signal active	
Turn on energy loss [1)]	Eon		1.2	2.4	mJ	VCC=13.5V,Tch=25°C, RL=1.5Ω	
Turn off energy loss [1)]	Eoff		1.2	2.4	mJ		
Driving capability [1)]	Dr(capa)	115			mΩ	Tch=25°C, VCC=8~16V	
		145				Tch=105°C, VCC=8~16V	

Remark) All voltages refer to ground pin of the device

1) not subjected production test, guaranteed by design

Protection function

Tch=-40 to 150°C, Vcc=7 to 18V, unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition	
Over current detection current	IL(SC)	80	130		A	VCC=13.5V, Von=5V, Tch=25°C	
Current limitation under power limitation toggling	IL(CL)		60		A	VCC=13.5V	
Current limitation under absolute thermal toggling	IL(TT)		25		A	VCC=13.5V	
Current limitation trigger threshold during turn-on	Von(CL1)		1.0		V	VCC=13.5V	
Current limitation trigger threshold during on-state	Von(CL2)		0.3		V	VCC=13.5V	
Current limitation trigger time after input signal positive slope	td(CL)		500		μs	VCC=13.5V	
Absolute thermal shutdown temperature	aTth	150			°C		
Thermal hysteresis for absolute thermal toggling	aTth,hys		20		°C		
Power limitation thermal shutdown temperature	dTth		40		°C		
Power limitation restart temperature	dTth,restart		20		°C		
Output clamp at inductive load switch off	Von,clamp	30		40	V	VCC=13.5V, IL=40mA, Tch=25°C	
Output current while GND disconnection	IL(GND)			1	mA	IIN=0A, ISEN=0A, IGND=0A, IIS=0A	
On-state resistance at reverse battery condition	Ron(rev)		9		mΩ	Tch=25°C	VCC=-13.5V, IL=9A
				18		Tch=150°C	
Gnd current at reverse battery condition	I_{GND}(rev)		-2		mA	VCC=-16V, Tch=25°C, IIN=0A, ISEN=0A, IIS=0A	

Remark) All voltages refer to ground pin of the device

Diagnosis function

Tch=-40 to 150°C, Vcc=7 to 18V, VIN=4.5V, VSEN=4.5V, unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Current sense ratio	KILIS	7520	9400	11280		IL=9.2A
		6580	9400	12220		IL=1.8A
Current sense drift depend on temperature	dKILIS	-15		15	%	VCC=13.5V, Tch,start=25°C, RL=1.5Ω
Sense current offset current	Iis,offset			2	μA	IL<10mA
Sense current leakage current	Iis,dis			1	μA	VIN=0V, VSEN=0V
Sense current under fault condition	Iis,fault	3		9.5	mA	VCC=13.5V, RIS=0.67kΩ
		3.5		9		VCC=13.5V, RIS=1kΩ
		3.5		5.5		VCC=13.5V, RIS=2kΩ
Minimum output current for current sense output	IL(CSE)	10		100	mA	IIS>5μA
Open load detection threshold at off-state	VOUT(OL)	2.0		5.0	V	VIN=0V, Tch = -40~105°C
OUT terminal current at Open load condition	IOUT(OL)	-1.0			μA	VIN =0V
Open load detection delay after input negative slope	tdop		300		μs	VIN=4.5V to 0V, VOUT>VOUT(OL)

Remark) All voltages refer to ground pin of the device

Diagnosis function

Tch=-40 to 150°C, Vcc=7 to 18V, VIN=4.5V, VSEN=4.5V, unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Sense current settling time after input signal positive slope	tsis(on)			250	μs	VCC=13.5V, VIN=0V to 4.5V, IL/IIS=KILIS, RL=1.5Ω
Sense current settling time after input signal negative slope [1)]	tsis(off)			10	μs	VIN=4.5V to 0V
Sense current settling time after sense enable during on-state [1)]	tssen(on)			20	μs	VSEN=0V to 4.5V, RL=1.5Ω
Sense current settling time after sense disable during on-state [1)]	tssen(off)			20	μs	VSEN=4.5V to 0V, RL=1.5Ω
Sense current settling time during on-state [1)]	tsis(LC)			20	μs	RL=1.5Ω to 0.75Ω
Fault signal delay after over current detection [1)]	tdsc(fault)			10	μs	VIN=0V to 4.5V, IL=IL(SC)
Fault signal delay after power limitation valid [1)]	tdpl(fault)			10	μs	Von>Von(CL1)
Fault signal delay after power limitation invalid [1)]	tdpl(off)			30	μs	Von<Von(CL1)
Fault signal delay after absolute thermal shutdown [1)]	tdot(fault)			10	μs	IIS→IIS,fault
Fault signal delay after open load detection at off-state [1)]	tdop(fault)			10	μs	VIN=0V, VOUT>VOUT(OL)
Fault signal delay after input negative slope [1)]	tdoff(fault)			10	μs	VIN=4.5V to 0V

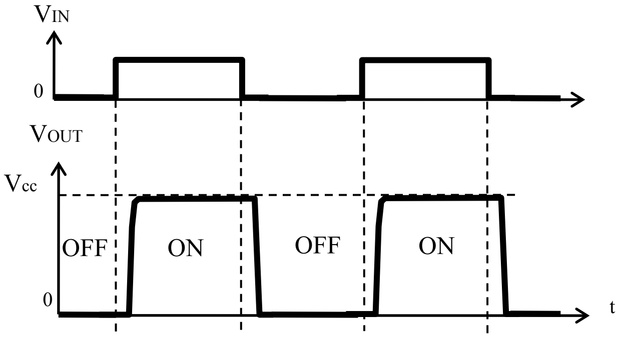
Remark) All voltages refer to ground pin of the device

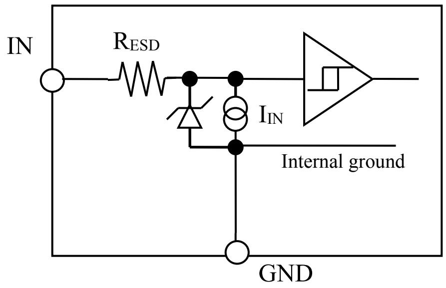
1) not subjected production test, guaranteed by design

3.6 Feature Description

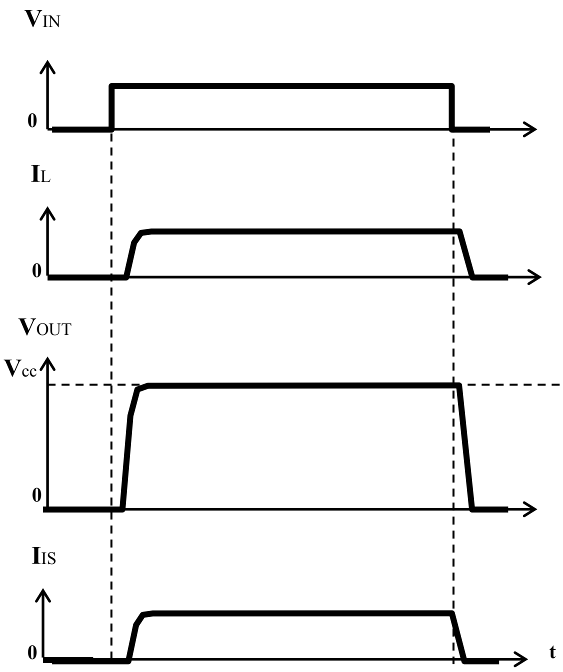
3.6.1 Driving Circuit

The high-side output is turned on, if the input pin is over VIH. The high-side output is turned off, if the input pin is open or the input pin is below VIL. Threshold is designed between VIH min and VIL max with hysteresis. IN terminal is pulled down with constant current source.

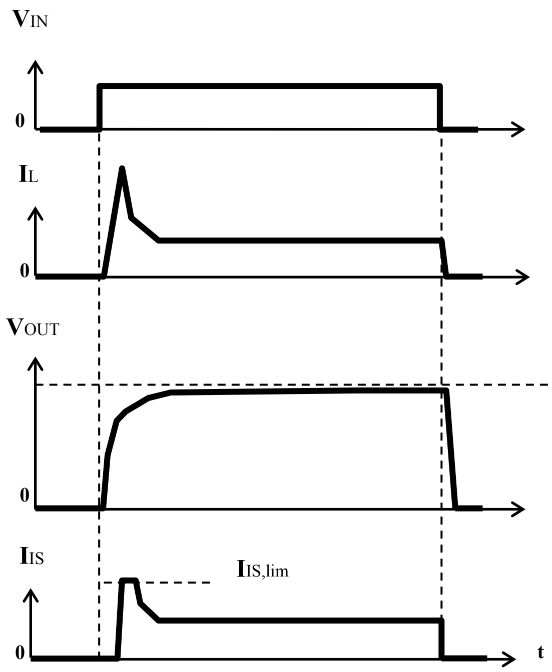




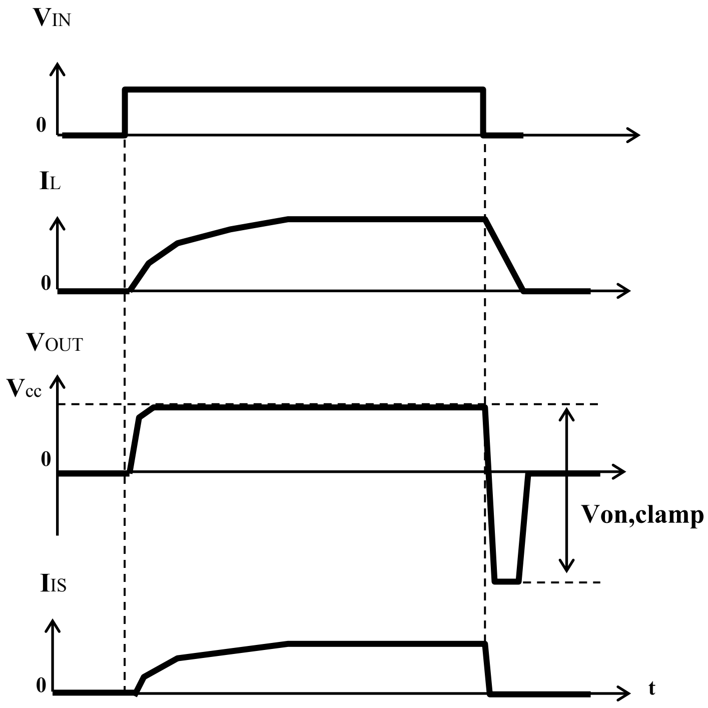
Switching a resistive load



Switching lamps



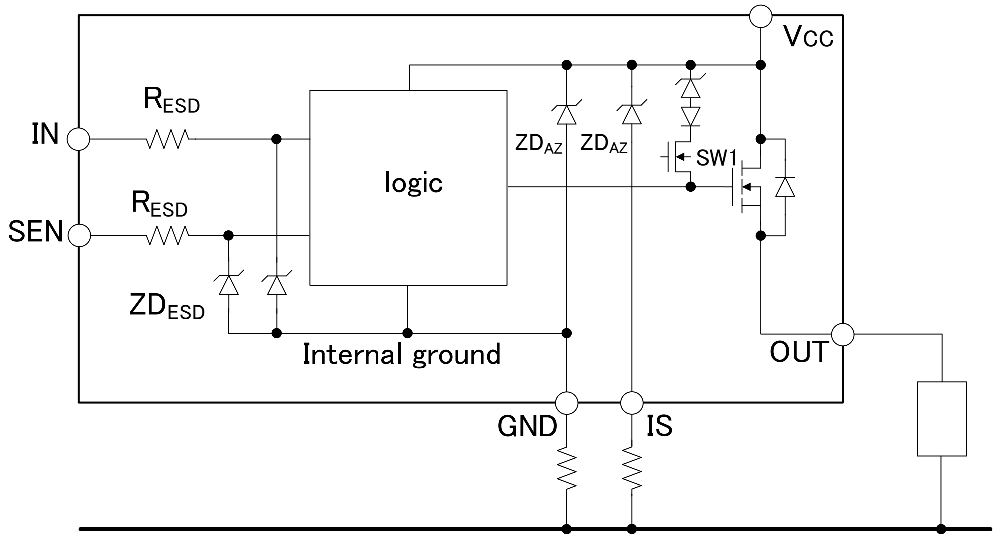
Switching an inductive load



The dynamic clamp circuit works only when the inductive load is switched off. When the inductive load is switched off, the voltage of OUT falls below 0V. The gate voltage of SW1 is then nearly equal to GND. Next, the voltage at the source of SW1 (= gate of output MOS) falls below the GND voltage.

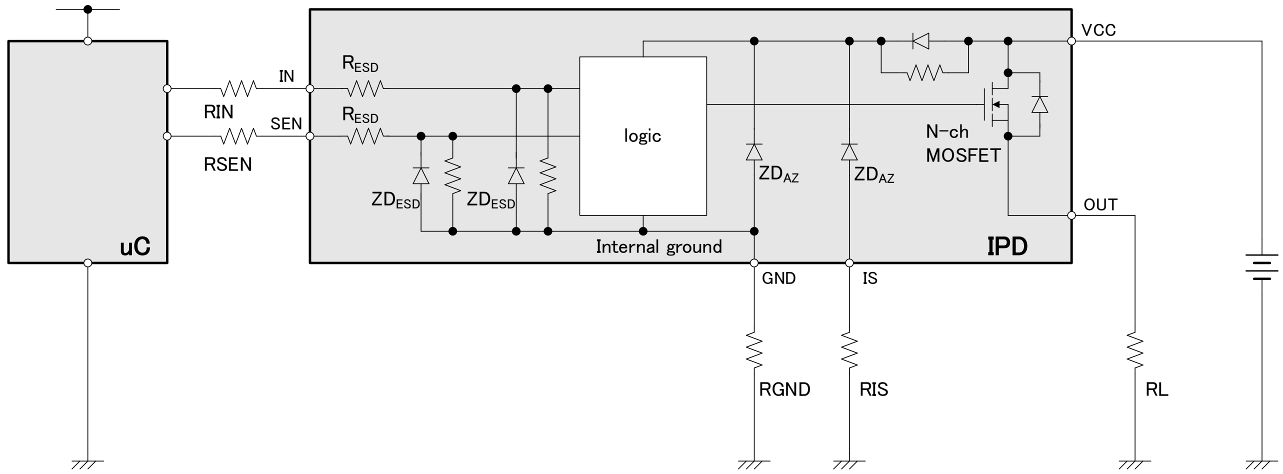
SW1 is turned on, and the clamp diode is connected to the gate of the output MOS, activating the dynamic clamp circuit.

When the over-voltage is applied to VCC, the gate voltage and source voltage of SW1 are both nearly equal to GND. SW1 is not turned on, the clamp diode is not connected to the gate of the output MOS, and the dynamic clamp circuit is not activated.



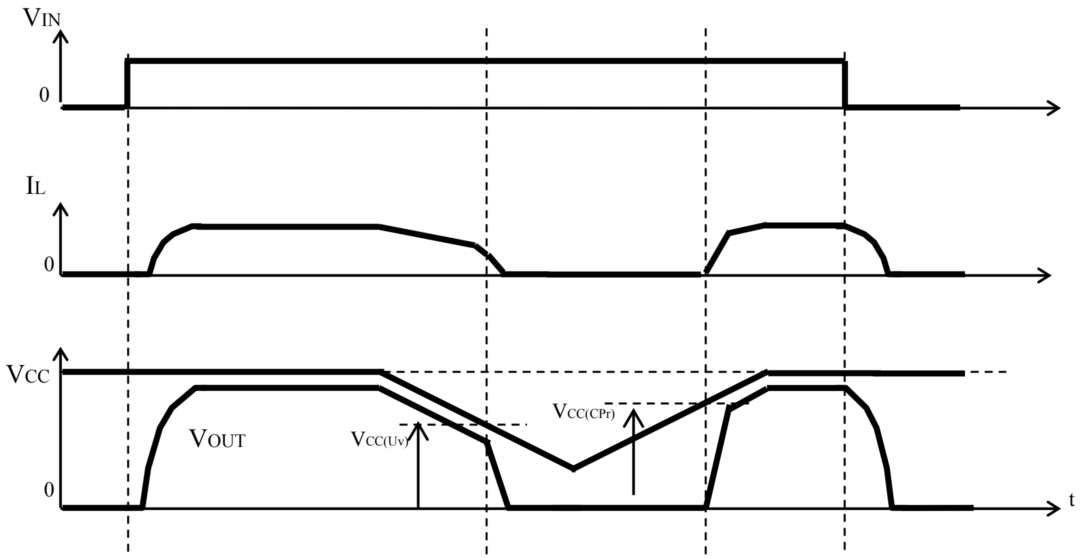
3.6.2 Device behavior at over voltage condition

In case of supply voltage greater than Vload dump, logic part is clamped by ZD_{AZ} (35V min). And current through of logic part is limited by external ground resistor. In addition, the power transistor switches off in order to protect the load from over voltage. Permanent supply voltage than V_{load} dump must not be applied to VCC.



3.6.3 Device behavior at low voltage condition

If the voltage supply (V_{CC}) goes down under V_{CC}(Uv), the device outputs shuts down. If voltage supply (V_{CC}) increase over V_{CC}(Cpr), the device outputs turns back on automatically. The device keeps off state after under voltage shutdown. The IS output is cleared during off-state.



3.6.4 Loss of Ground protection

In case of complete loss of the device ground connection, but connected load ground, the device securely changes to off if VIN was initially greater than VIH state or keeps off state if VIN was initially lower than VIL state.

In case of device loss of ground, IN and SEN terminal will/ could/ might be at VCC voltage.

3.6.5 Short circuit protection

Turn-on in an over load condition including short circuit condition

The device shuts down automatically when condition (a) is detected. The sense pin output Iis,fault. Shutdown is latched until the next reset via input pin. The device shuts down automatically when condition (b) is detected. The device restarts automatically in power limitation mode. The device shuts down automatically when condition (c) is detected and restarts automatically in absolute thermal toggling mode. The device starts current limitation when (d) is detected. The sense pin output Iis,fault during power limitation mode or thermal toggling mode.

(a) IL > IL(SC)

(b) deltaTch > dTth

(c) Tch > aTth

(d) Von > Von(CL1) after td(CL)

Over load condition including short circuit condition during on-state

The device runs automatically into power limitation mode when condition (a) is detected once after Von < Von(CL2). The device shuts down automatically when condition (b) is detected. The device restarts automatically in power limitation mode. The device shuts down automatically when condition (c) is detected and restarts automatically in absolute thermal toggling mode. The sense pin output Iis,fault during power limitation mode or thermal toggling mode.

(a) Von > Von(CL2)

(b) deltaTch > dTth

(c) Tch > aTth

Power limitation control

Current limitation control with IL(CL) when auto restart from deltaTch protection.

During the current limitation operation and Von>Von(CL1), the sense pin outputs Iis,fault. Even auto restart from delta Tch protection, if Von<Von(CL2) depends on short circuit impedance condition, the device does not operate as current limitation with IL(CL). In this case, the sense pin output sense current at on-state, Iis,fault at off-state during toggling operation with power limitation mode.

Absolute thermal toggling

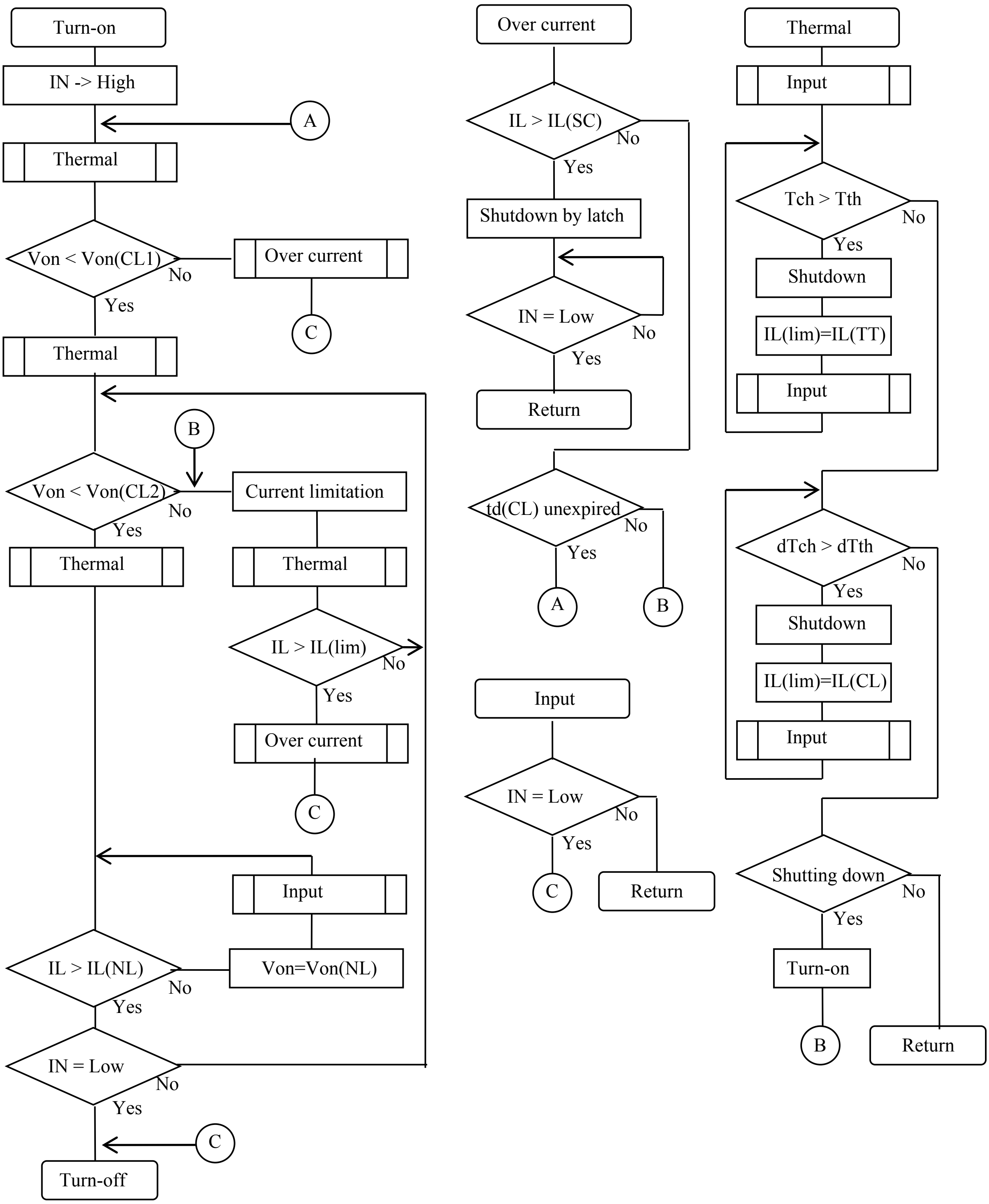
Current limitation control with IL(TT) when auto restart from absolute Tch protection.

During the current limitation operation and Von>Von(CL1), the sense pin outputs Iis,fault. Even auto restart from absolute Tch protection, if Von<Von(CL2) depends on short circuit impedance condition, the device does not operate as current limitation with IL(TT). In this case, the sense pin output sense current at on-state, Iis,fault at off-state during toggling operation with thermal toggling mode.

delta Tch

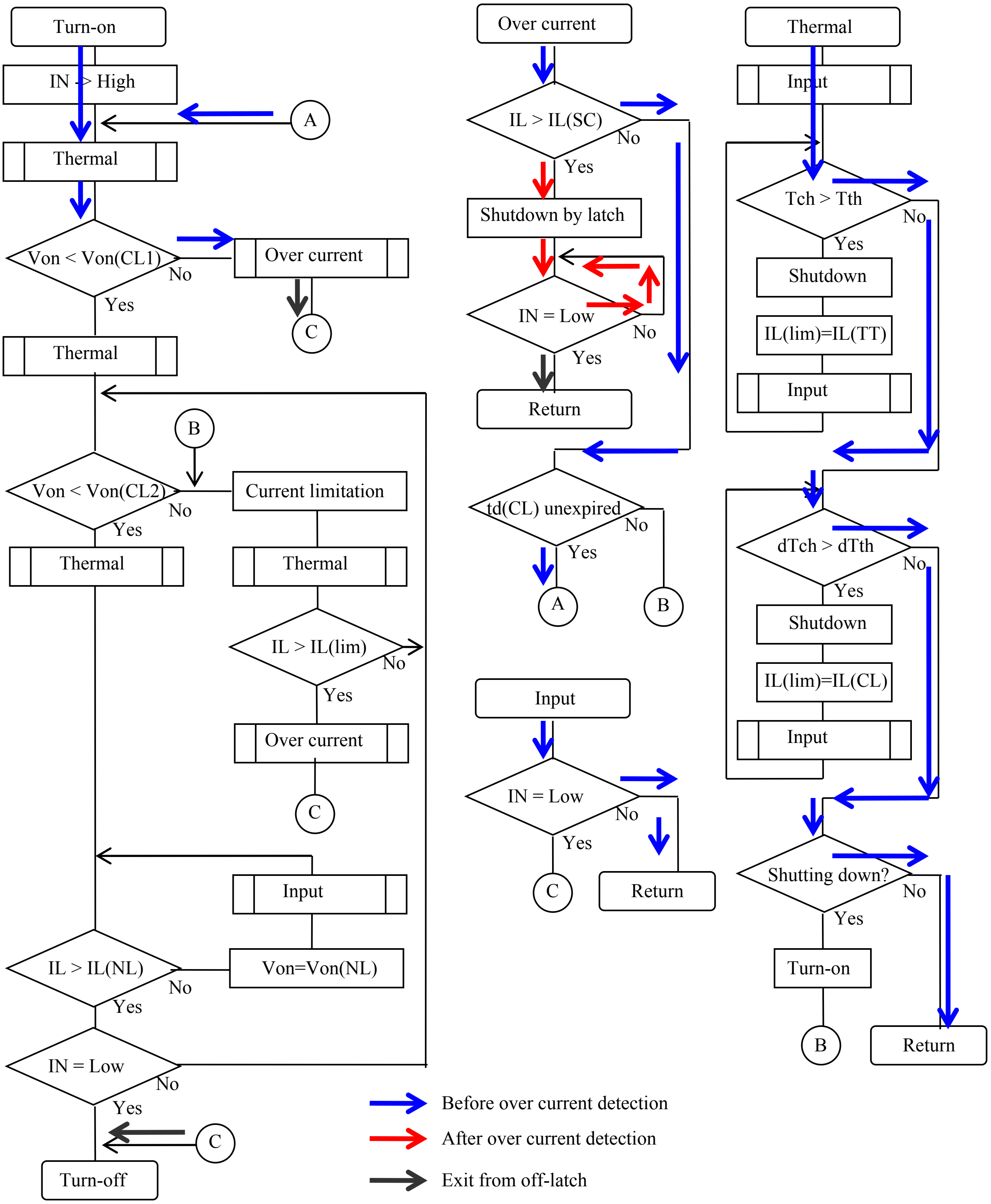
Junction temperature differences between thermal sensor of power area and thermal sensor of control area.

State transition diagram



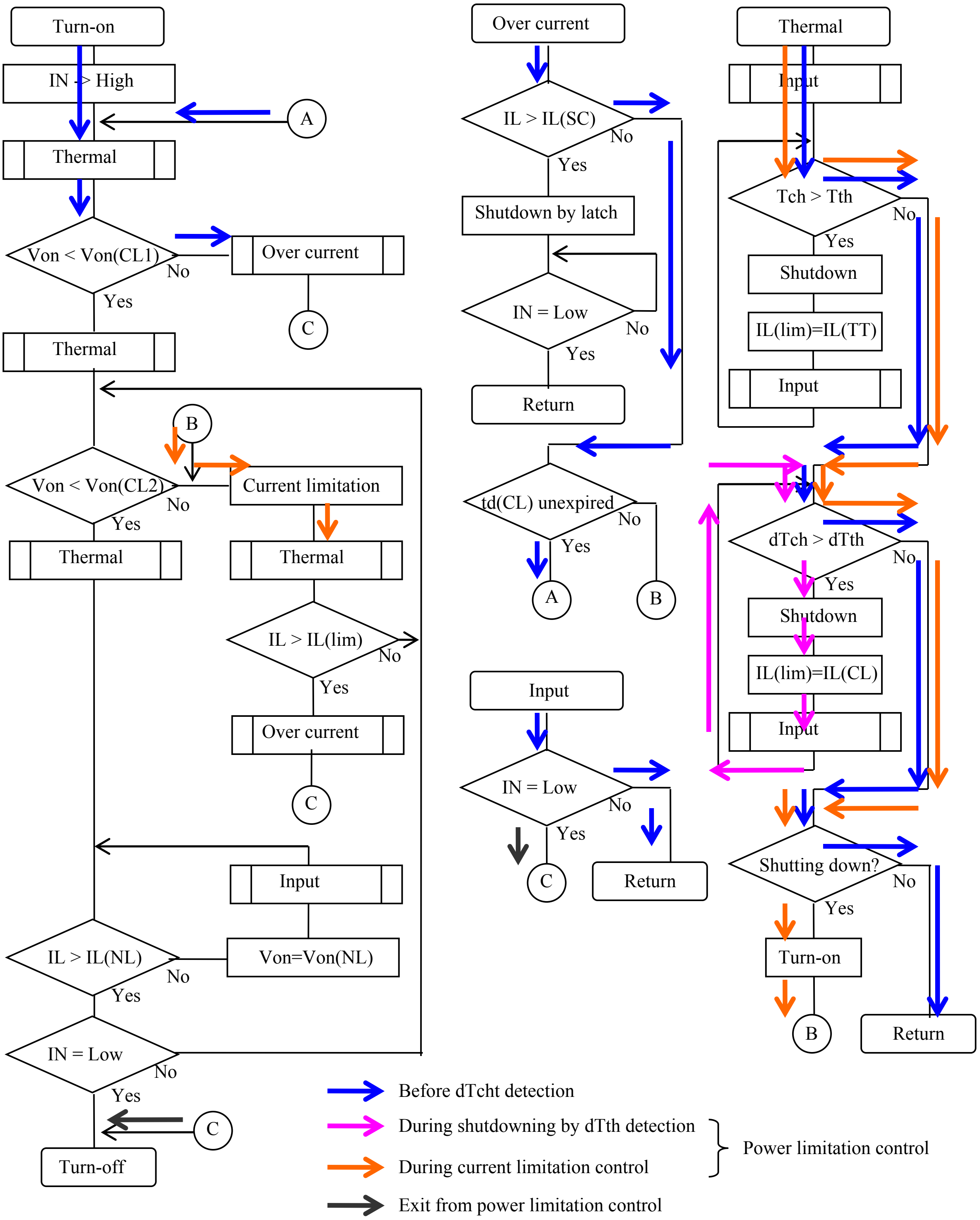
Turn-on in an over load condition including short circuit condition

(a) IL > IL(SC)



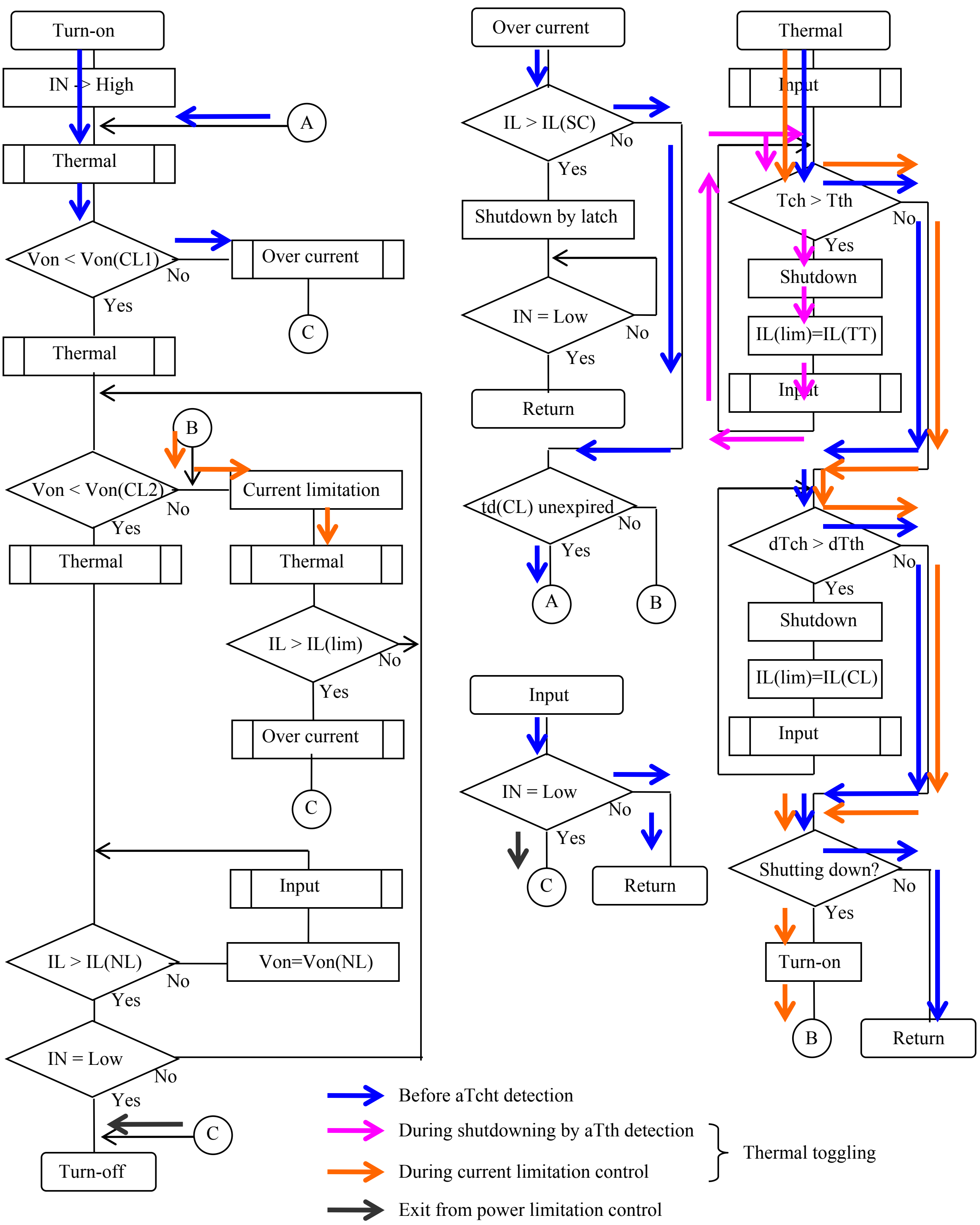
Turn-on in an over load condition including short circuit condition

(b) deltaTch > dTth



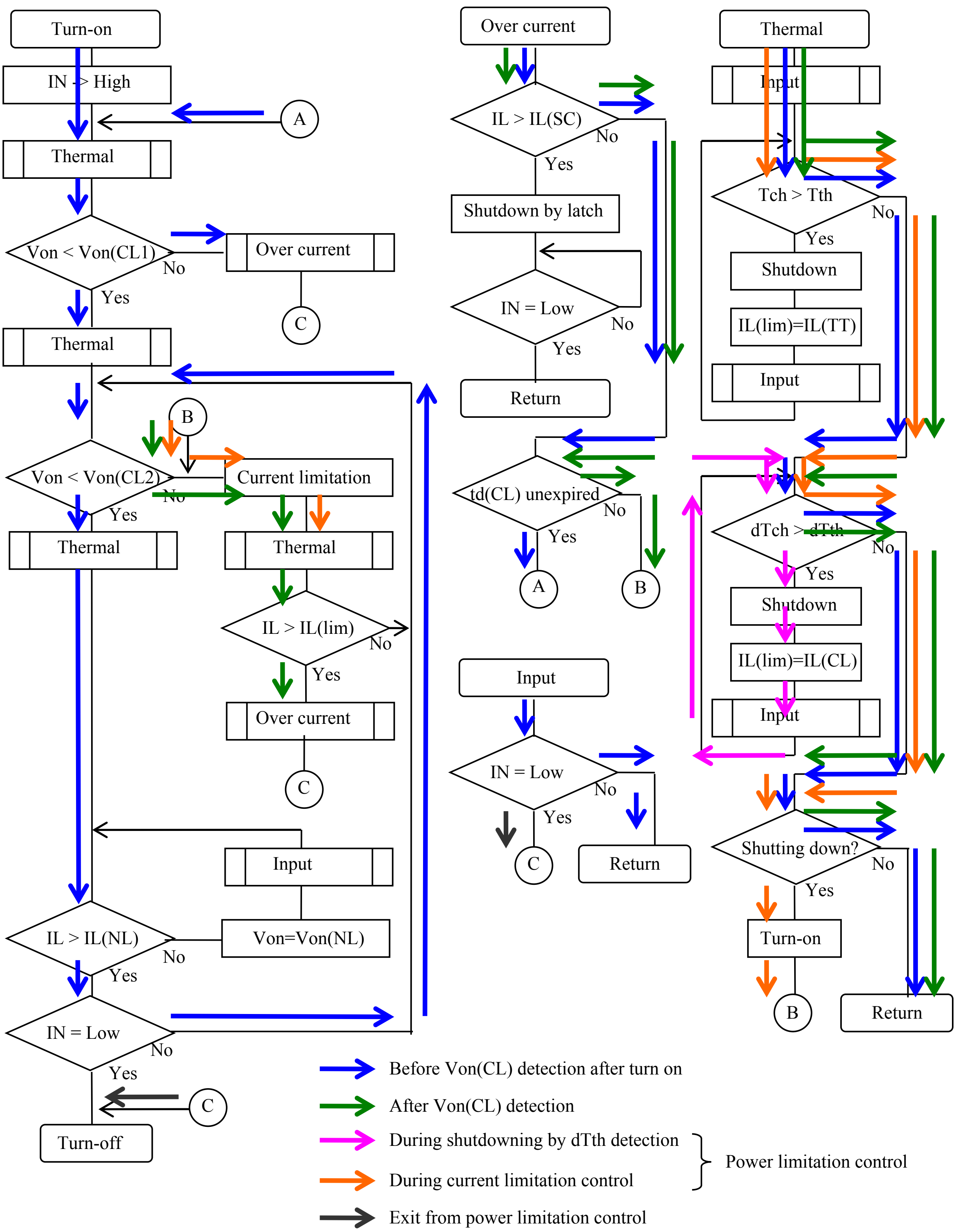
Turn-on in an over load condition including short circuit condition

(c) Tch > aTth



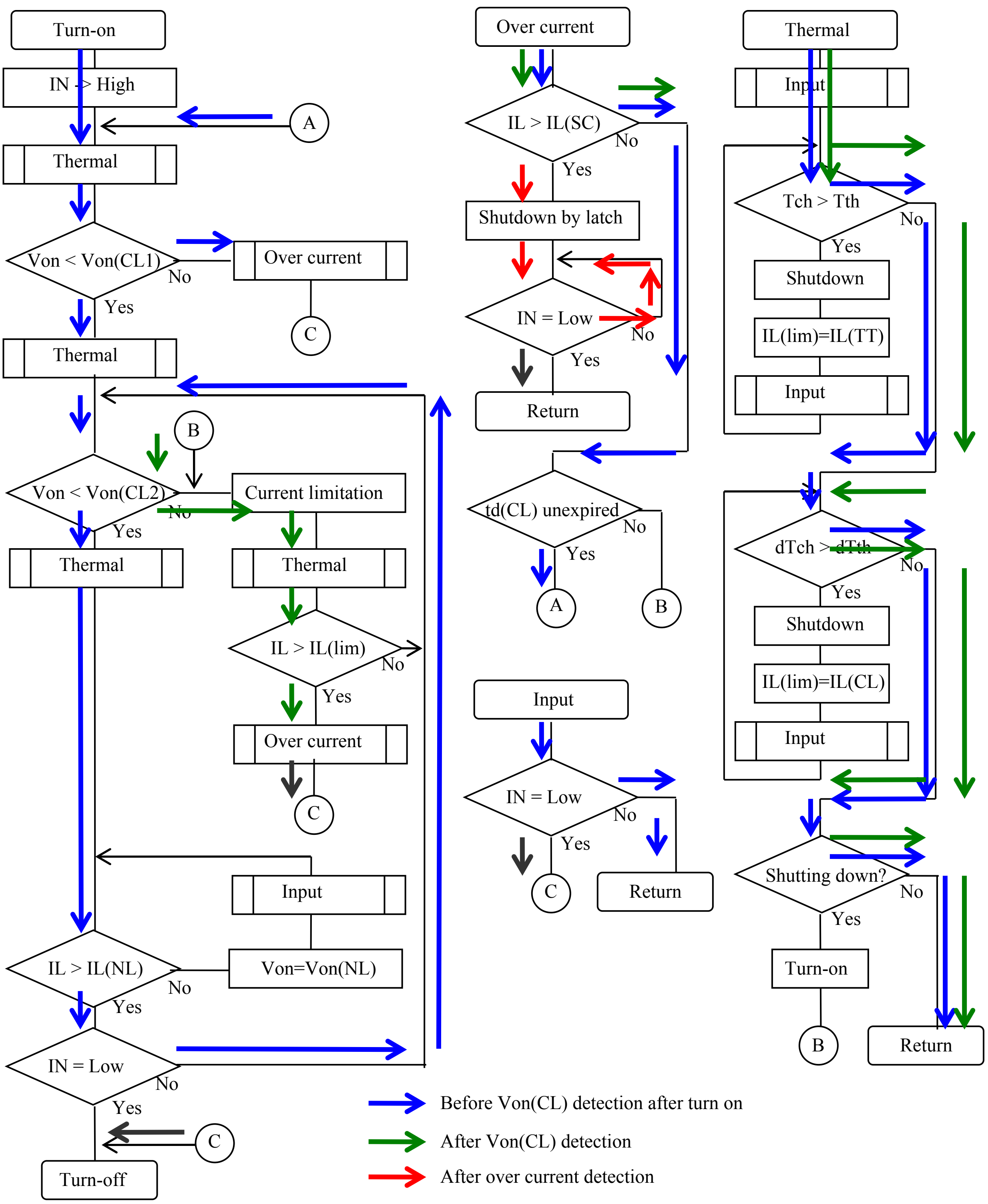
An over load condition which is include a short circuit condition during on-state

(a) Von > Von(CL) with weak short condition



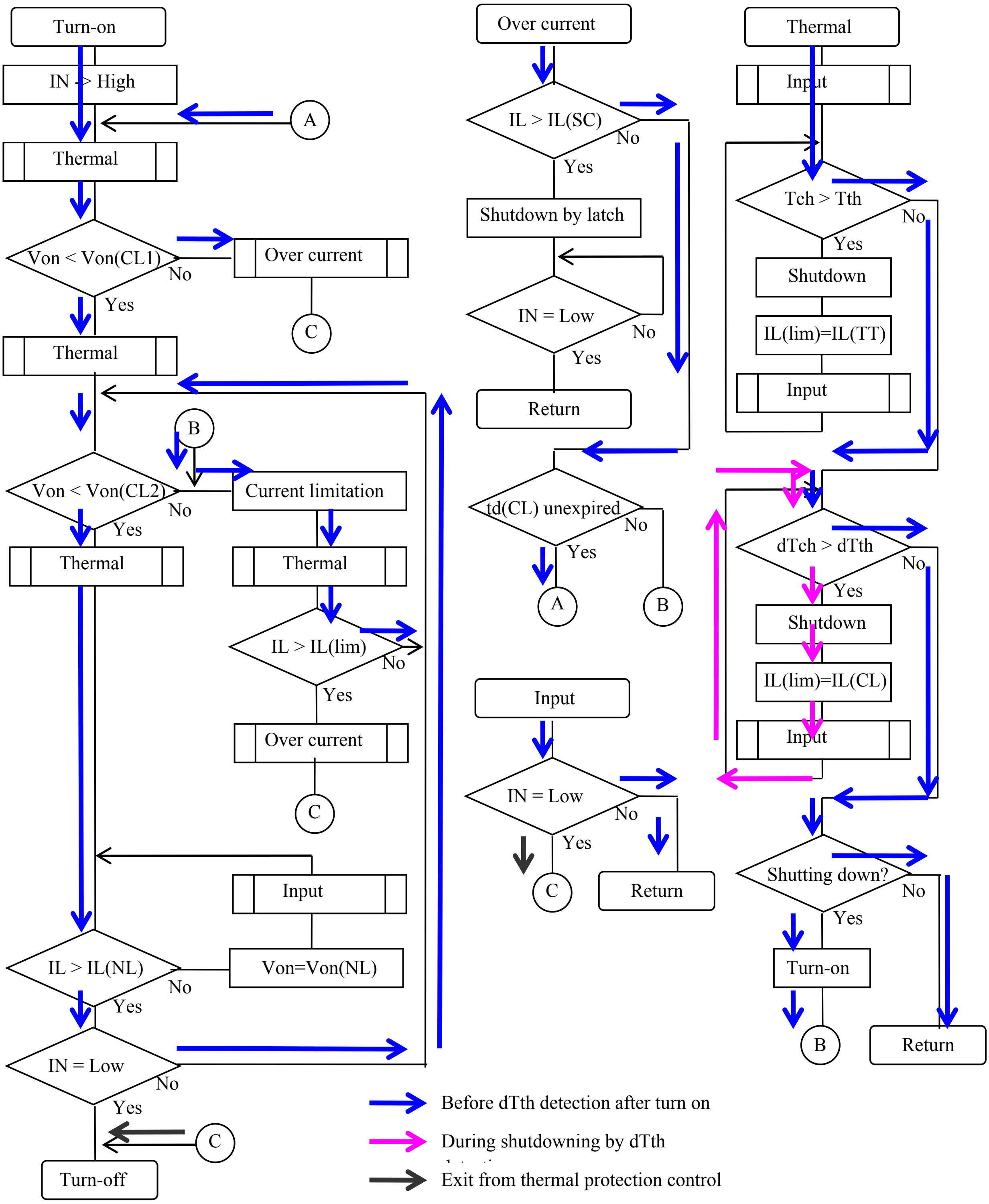
An over load condition including short circuit condition during on-state

(a) Von > Von(CL) with dead condition



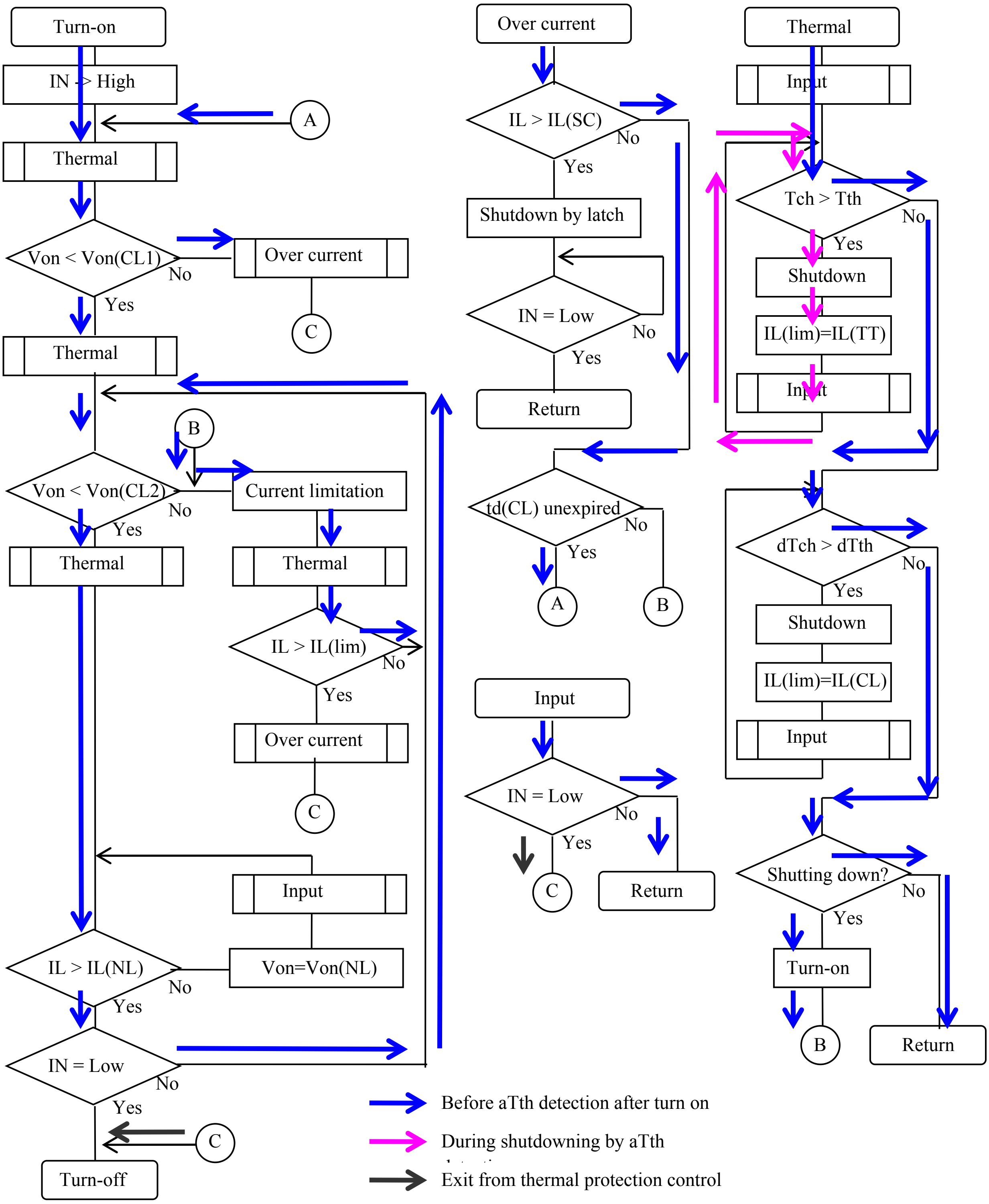
An over load condition including short circuit condition during on-state

(b) deltaTch > dTth



An over load condition including short circuit condition during on-state

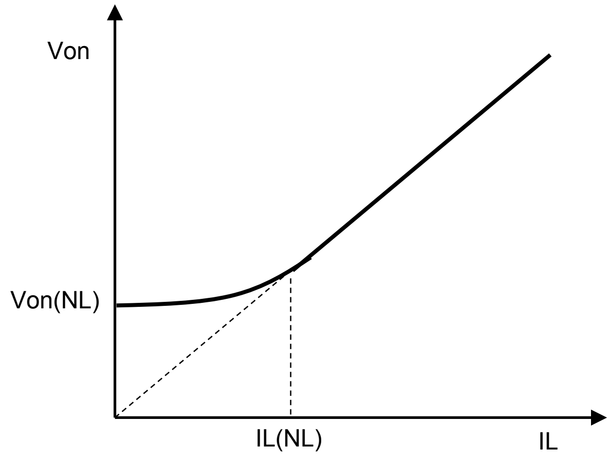
(c) Tch > aTth



3.6.6 Device behavior at small load current conduction

The device has a function which controls Ron in order to improve KILIS accuracy at small load current conduction.

Von (VCC-OUT) is proportionate to IL under normal conditions. Under IL<IL(NL) condition, Ron is controlled to increase to be Von=Von(NL)=30mV(typ).



3.6.7 Diagnostic signal

Truth table

	SEN	Input	Output	Diagnostic output [2]
Normal Operation	H	H	VCC	IIS = IL/KILIS
		L	L [1]	< 1μA (Iis,dis)
Shutdown by over current detection		H	L [1]	Iis,fault [3]
		L	L [1]	< 1μA (Iis,dis)
Power limitation		H	VOUT [6]	IIS = IL/KILIS in case of Von<Von(CL1)
				Iis,fault [4] in case of Von>Von(CL1)
			L [1]	Iis,fault [4]
		L	L [1]	< 1μA (Iis,dis)
Thermal toggling		H	VOUT [6]	IIS = IL/KILIS in case of Von<Von(CL1)
				Iis,fault [5] in case of Von>Von(CL1)
			L [1]	Iis, fault [5]
		L	L [1]	< 1μA (Iis,dis)
Short circuit to VCC		H	VCC	< 2μA (Iis,offset)
		L	VOUT [7]	Iis,fault in case of VOUT>VOUT(OL)
Open Load		H	VCC	< 2μA (Iis,offset)
		L	VOUT [7]	Iis,fault in case of VOUT>VOUT(OL)
X [8]	L	X [8]	X [8]	< 1μA (Iis,dis)

1) In case of OUT terminal is connected to GND via load.

2) In case of IS terminal is connected to GND via resister.

3) IS terminal keeps Iis,fault as long as input signal activate after the over current detection.

4) IS terminal keeps Iis,fault during power limitation if Von>Von(CL1).

5) IS terminal keeps Iis,fault during thermal toggling if Von>Von(CL1)..

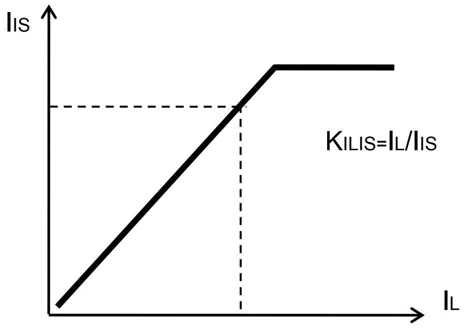
6) VOUT depends on the short circuit condition

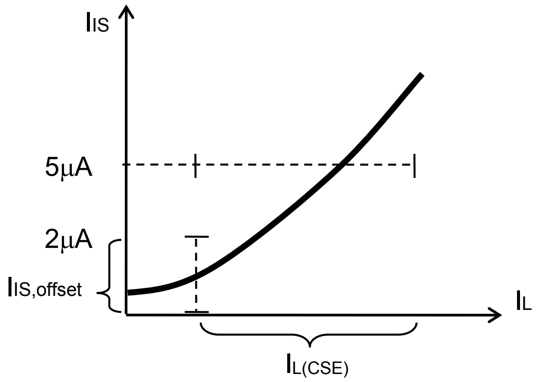
7) VOUT depends on the ratio of VCC-OUT-GND resistive component.

8) Don’t care

Current sense output

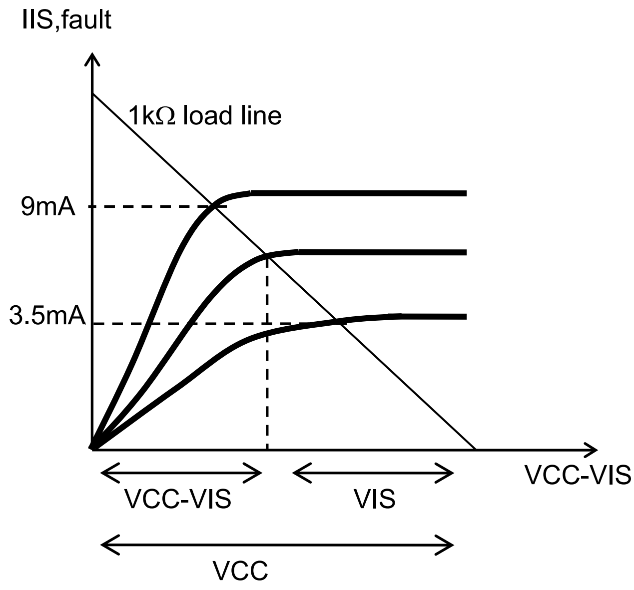
The device output analog feedback current proportional to output current from IS pin. In the case of much higher current than nominal load current, current sense output is saturated. In the case of much lower current than nominal load current, current sense output is above 5μA if output current is above IL(CSE) max, current sense output is below 2μA, IIS,offset max, if output current is below IL(CSE) min.

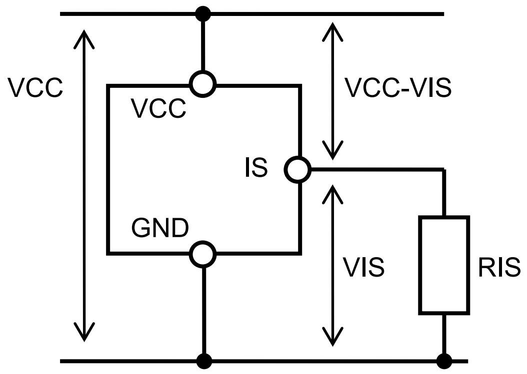




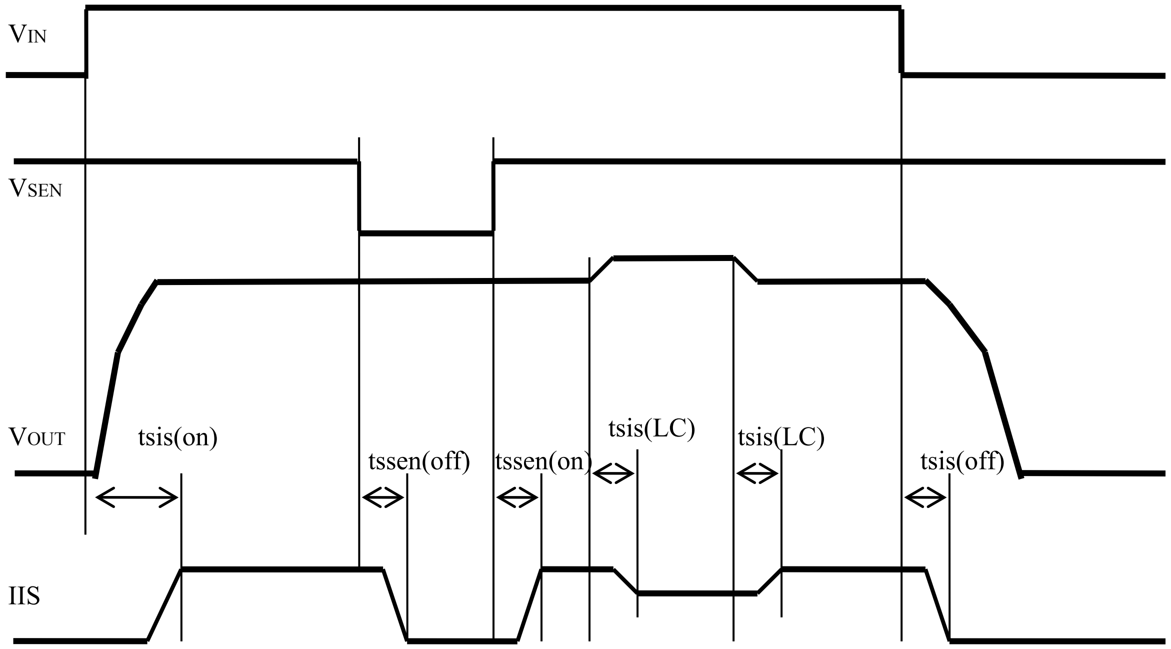
Sense current under fault condition

The device output IIS,fault, constant current, from IS pin under fault condition such as after over current detection, during power limitation and during thermal toggling. IIS,fault is specified with RIS=1kΩ condition. IIS,fault is attenuated depends on VCC-VIS voltage. Operation point as IIS,fault output is also depends on RIS condition. For example, In the case of RIS=1kΩ, IIS,fault could be 3.5mA to 9mA, VCC-VIS could be 4.5V to 10V, VIS could be 9V to 3.5V if VCC=13.5V. In the case of RIS is higher than 1kΩ, Operation point as IIS,fault is lower than specified value but VIS should be higher than RIS=1kΩ condition.

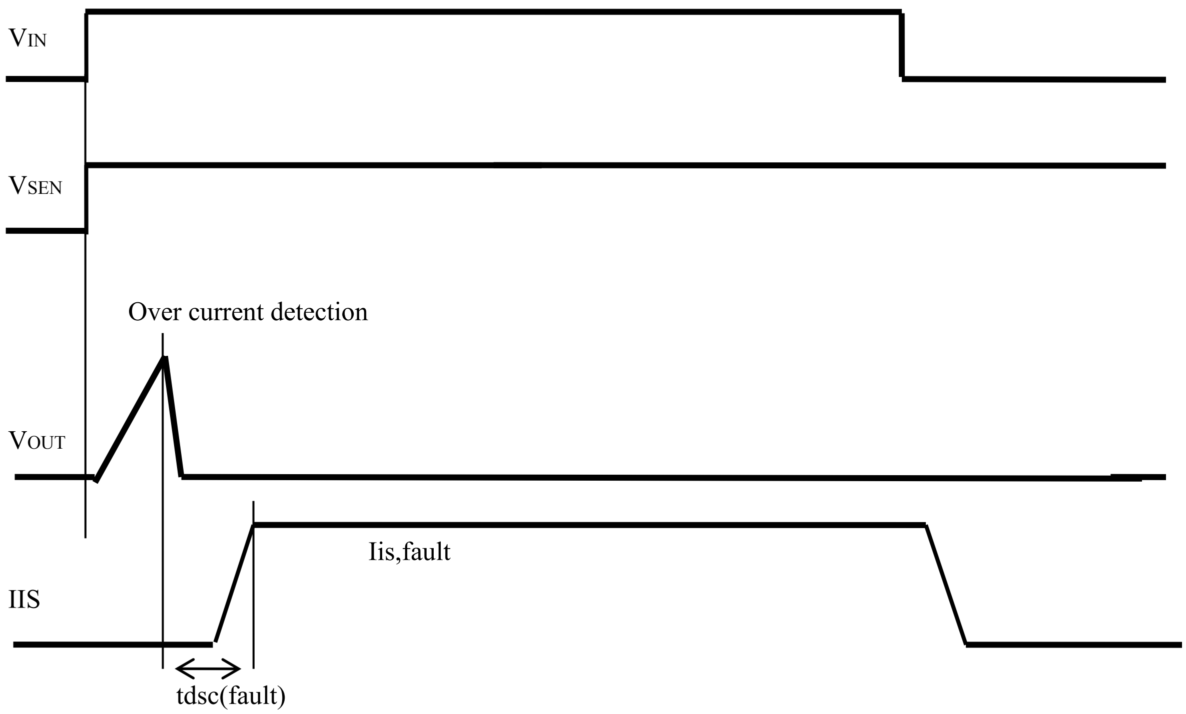




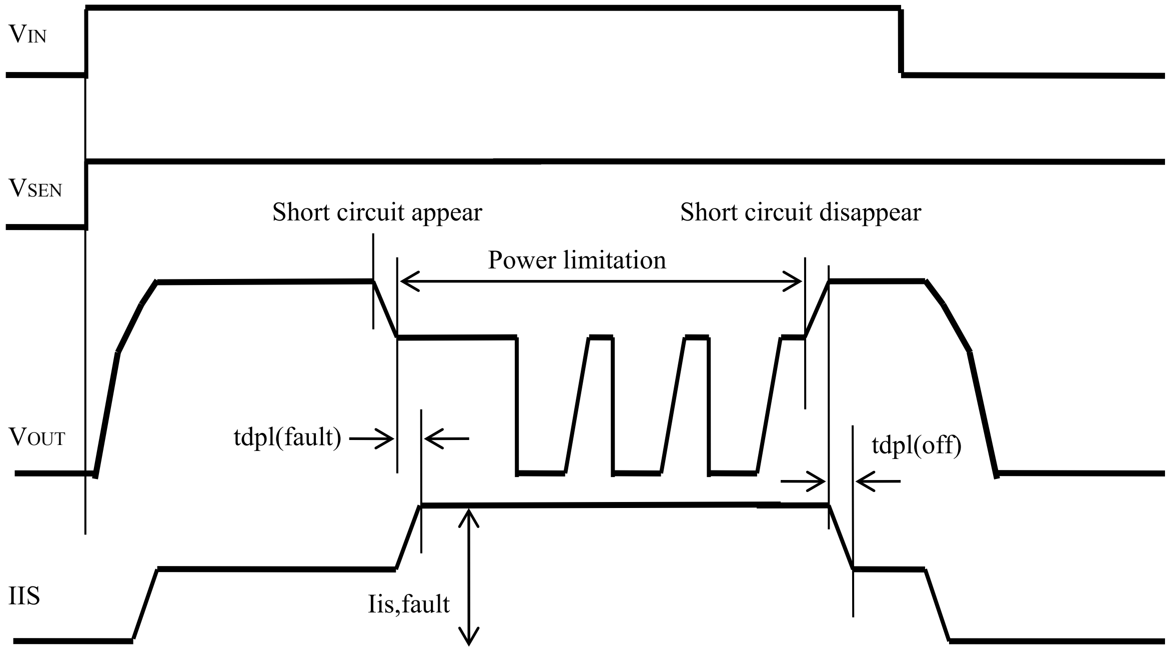
Sense current settling time



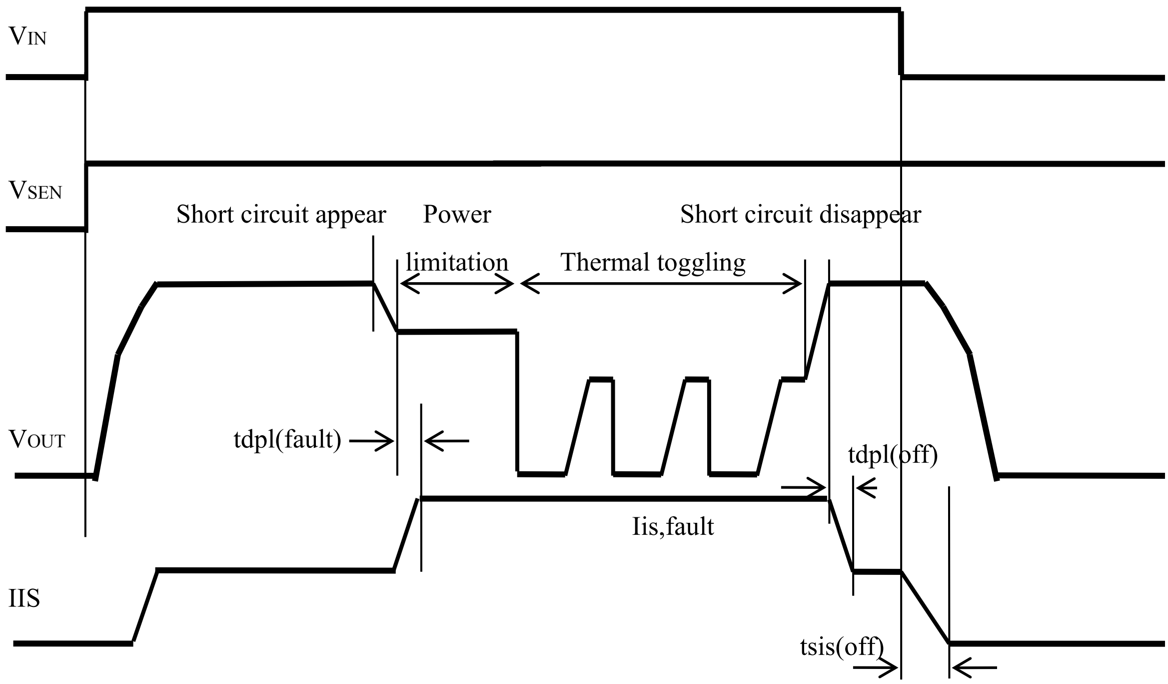
Fault signal delay time at over current detection



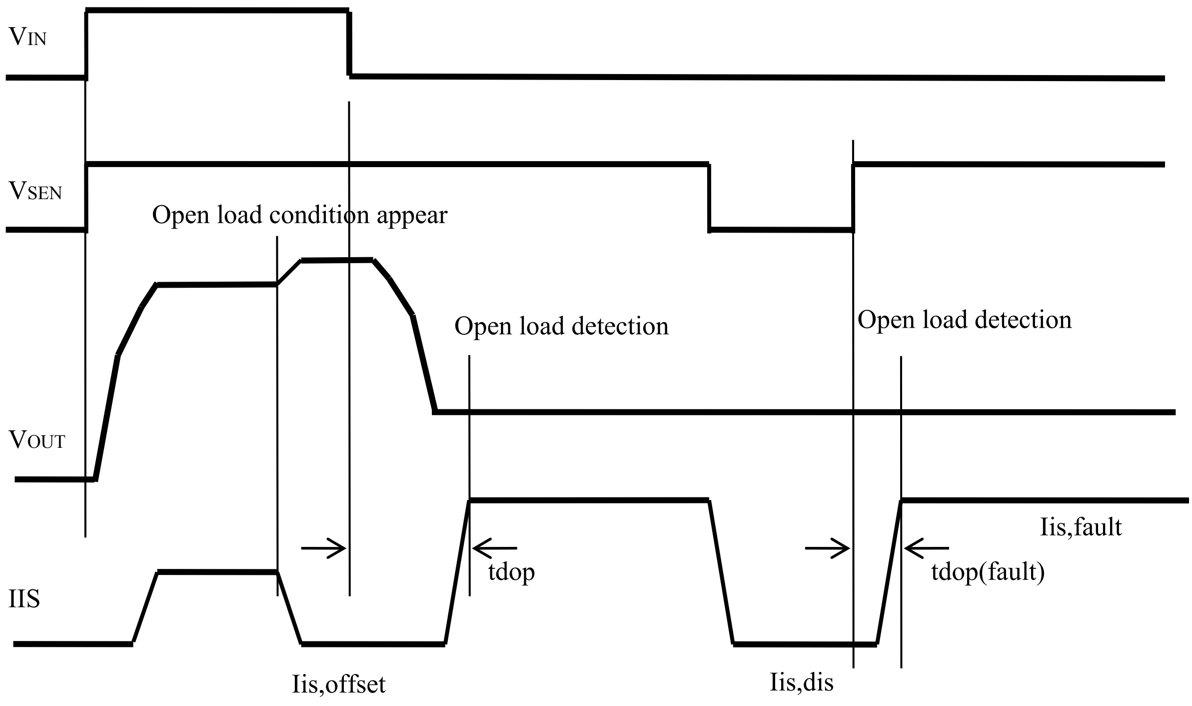
Fault signal delay time at power limitation



Fault signal delay time at Thermal toggling



Fault signal delay time at open load detection

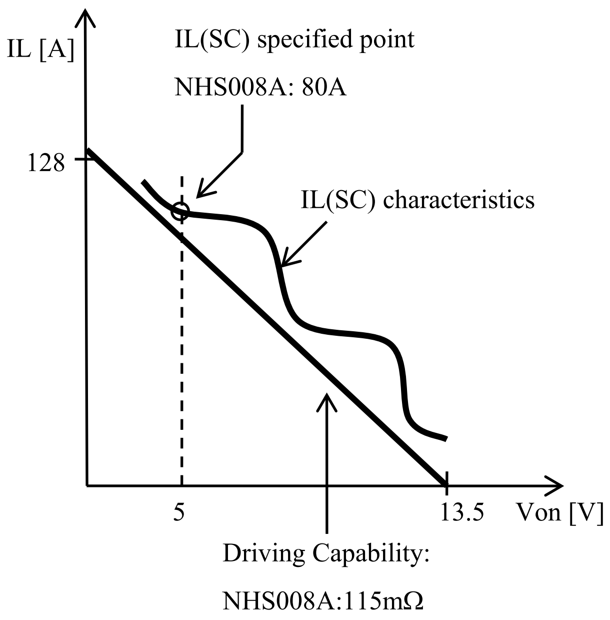


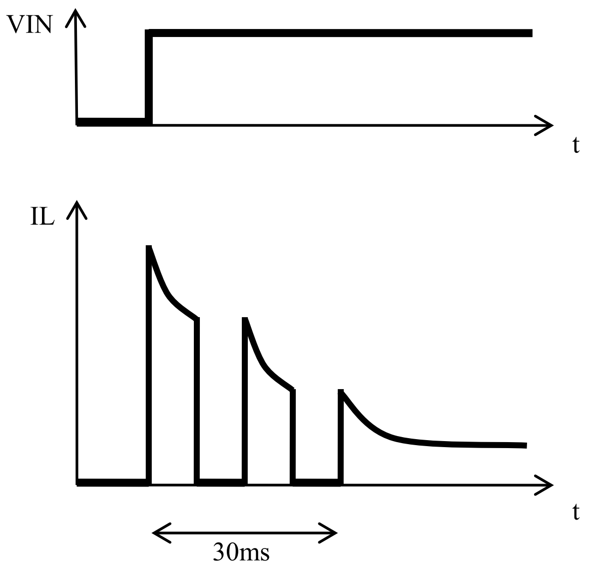
3.6.8 Nominal load

Product	Nominal load
NHS008A	1.5Ω

3.6.9 Driving Capability

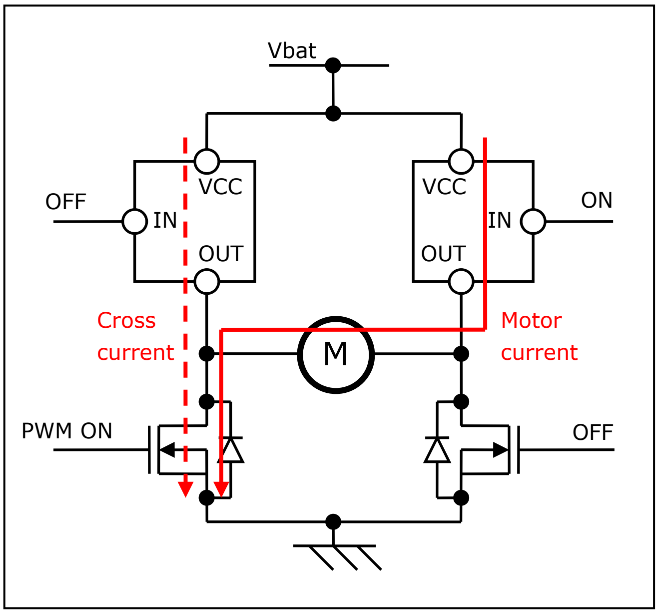
Driving Capability is specified as load impedance. Over current detection characteristics is designed above Driving Capability characteristics. If estimated load impedance which comes from peak inrush current is lower than Driving Capability characteristics, this means, the device does not detect inrush current as over current and does not shutdown the output. Depend on the conditions, Power Limitation function may work during inrush current. If estimated load impedance which comes from peak inrush current is lower than Driving Capability characteristics, Power limitation disappear within 30ms. This parameter does not mean that the device can drive the resistive load up to Driving Capability characteristics.





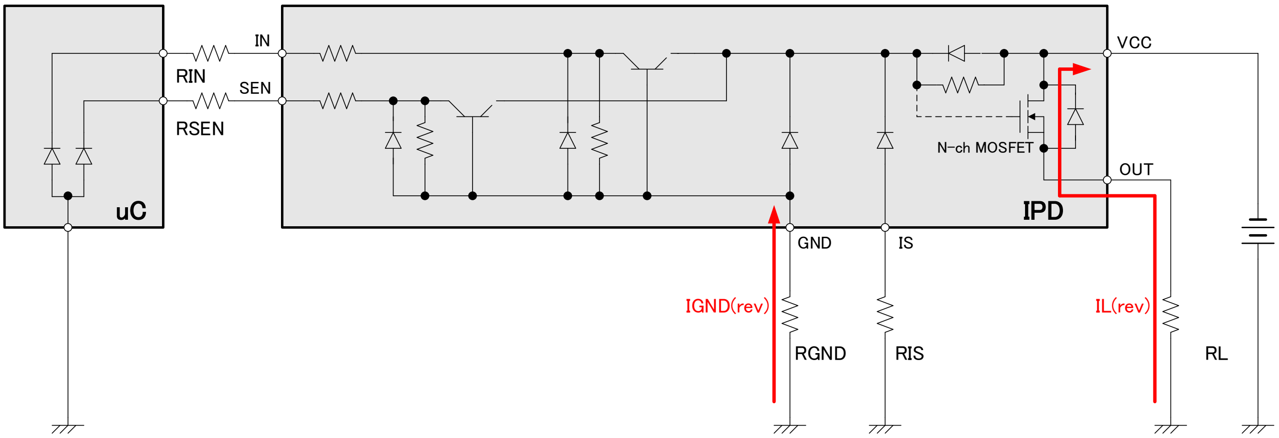
3.6.10 Cross current protection in case of H-bridge high side usage

In case of using High side driver in H-bridge circuit, High side driver protects High side driver itself and also low side driver from high power dissipation by cross current when low side driver switching on.



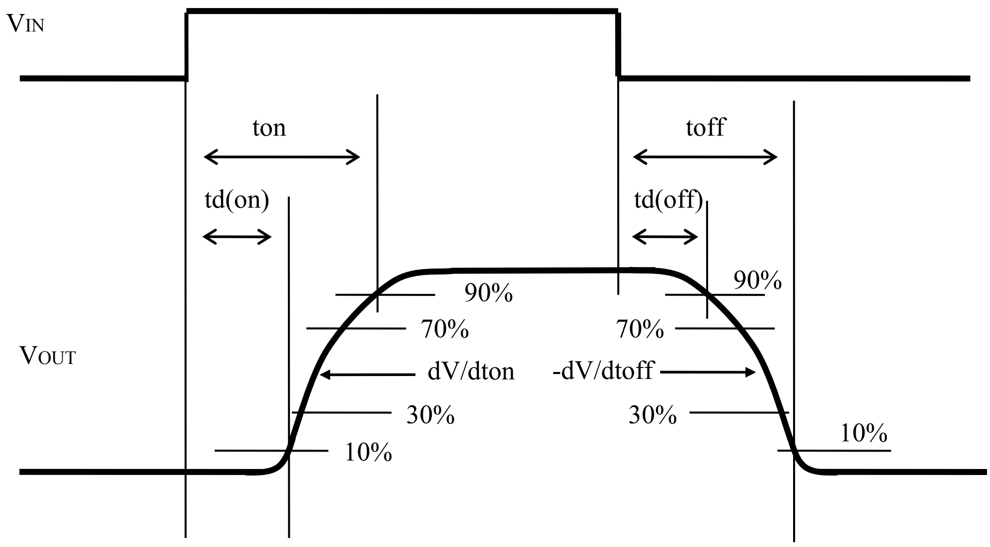
3.6.11 Reverse Battery Protection by turn on the output

In case of a reverse battery is applied to the device, the N-ch MOSFET will turn on only if reverse current flow from GND pin. The reverse current through the N-ch MOSFET has to be limited by the connected load. IGND(rev) is limited internally approx. 2mA even without external RGND. Reverse current flow from IN, SEN, IS should be limited by external component such as recommendation value in Pin function, refer 3.2 Pin configuration.



3.6.12 Measurement condition

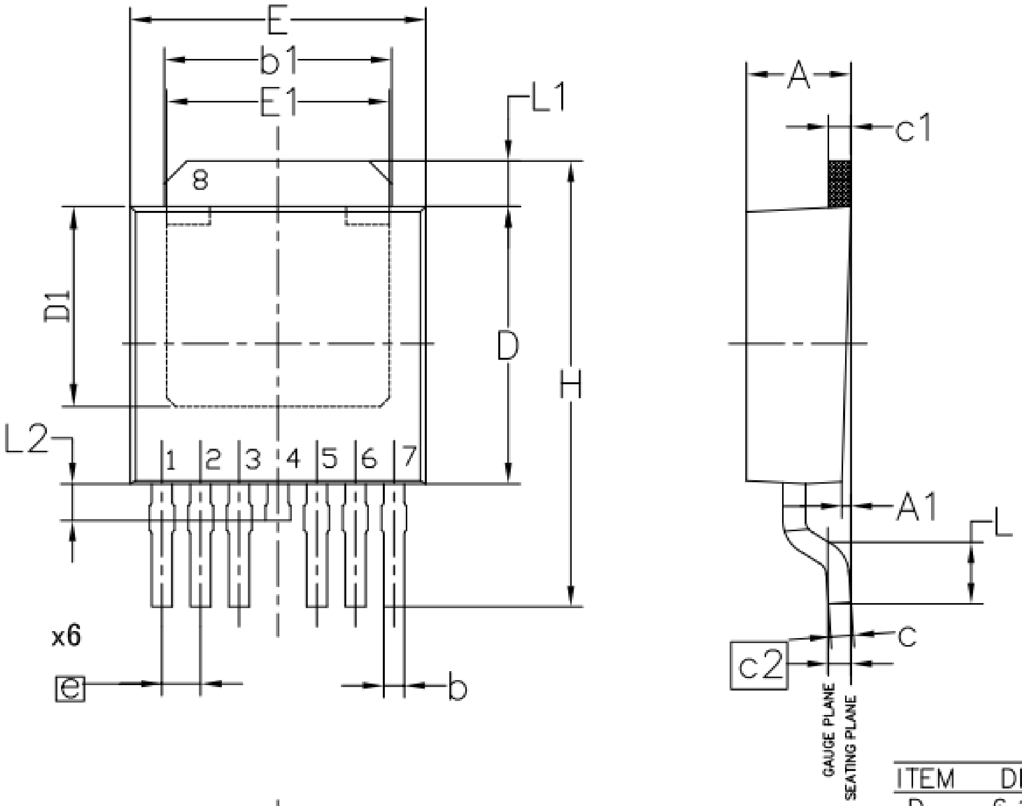
Switching waveform of OUT terminal

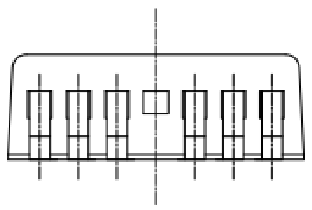


3.7 Package drawing

JEITA Package Code	Renesas Code	Previous Code	Mass(TYP.)[g]
–	PRSS0008ZA-A	P7J5-85-314	0.33

Unit : mm



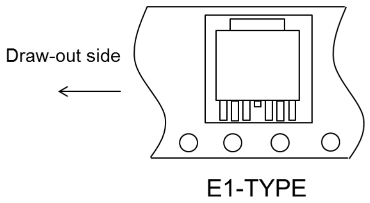


ITEM	DIMENSIONS
D	6.10±0.20
D1	4.4TYP(4.0MIN)
E	6.50±0.20
E1	4.9TYP(4.8MIN)
H	9.8TYP(10.3MAX)
A	2.30±0.10
A1	0.125MAX
b	0.45±0.10
b1	5.0
c	0.50±0.10
c1	0.50±0.10
c2	0.508
e	0.85
L	1.52±0.12
L1	1.0
L2	0.80

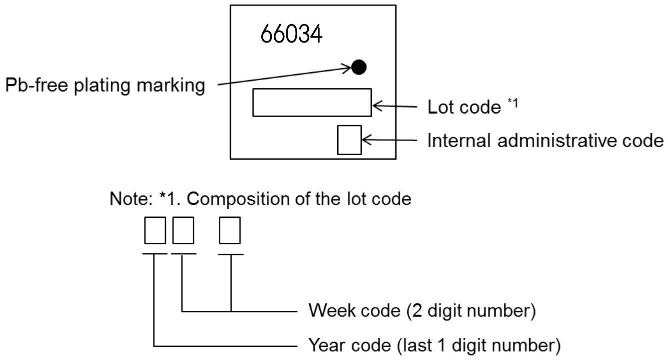
NOTE

1, ▒ No Plating area

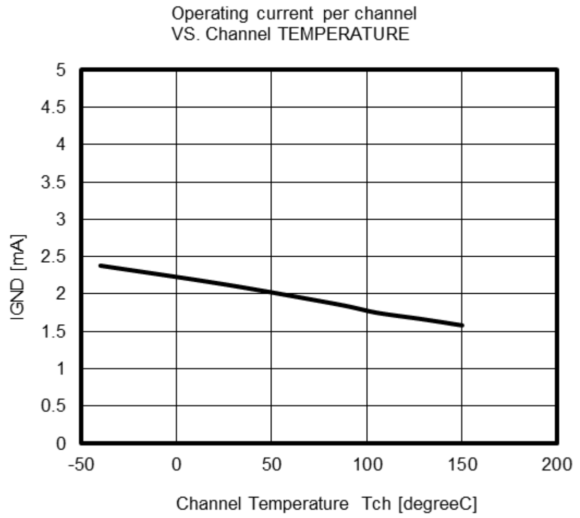
3.8 Taping information

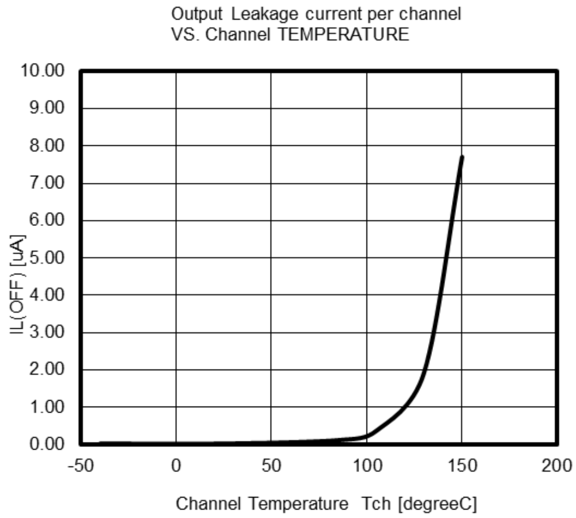


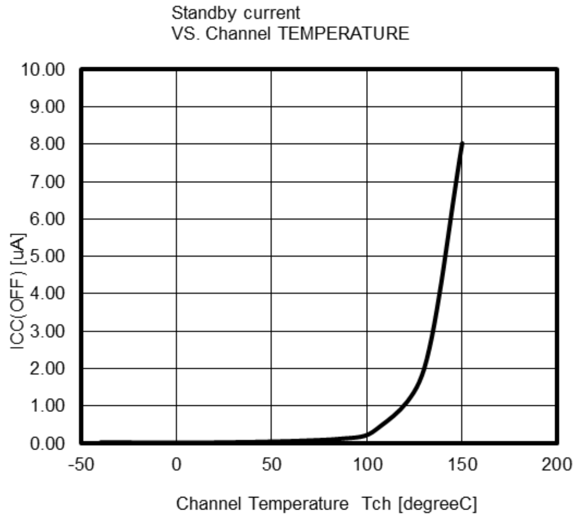
3.9 Marking information

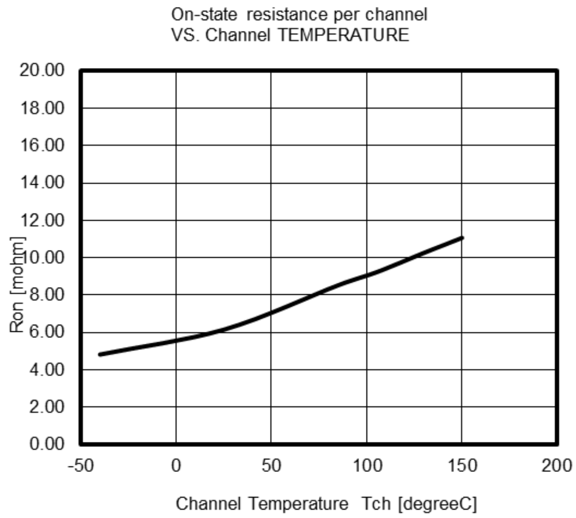


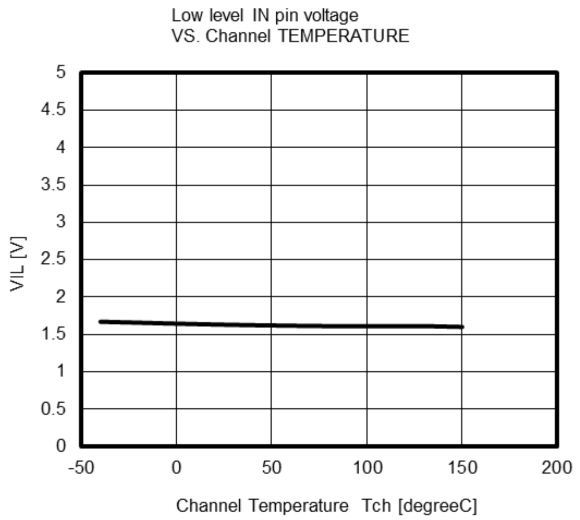
4. Typical characteristics

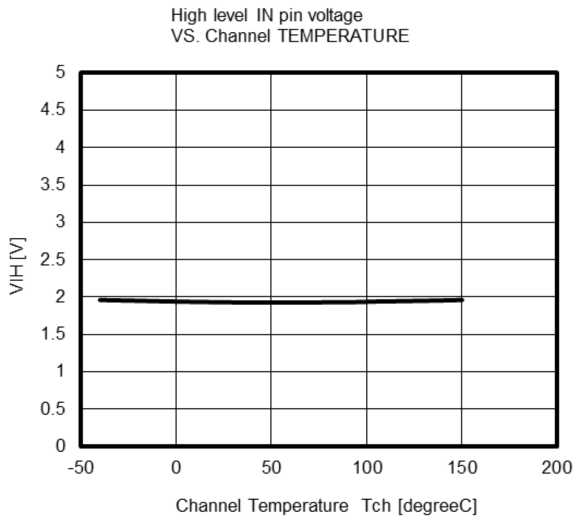


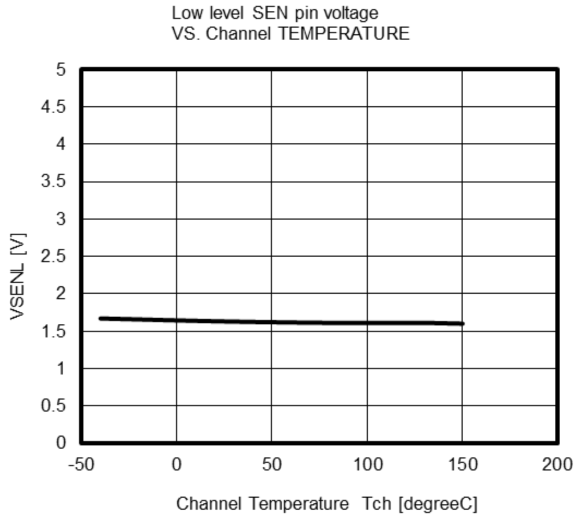


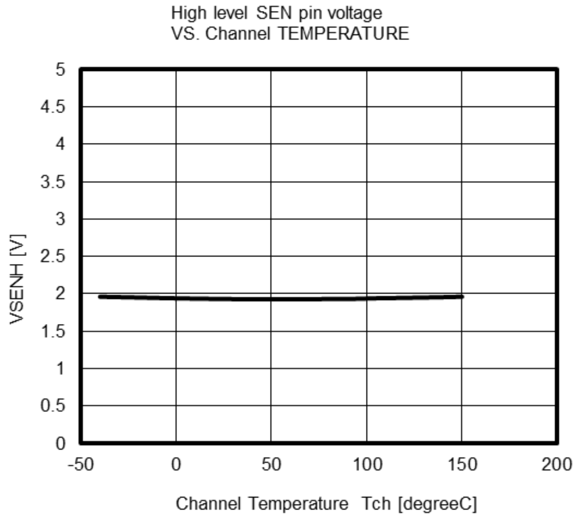


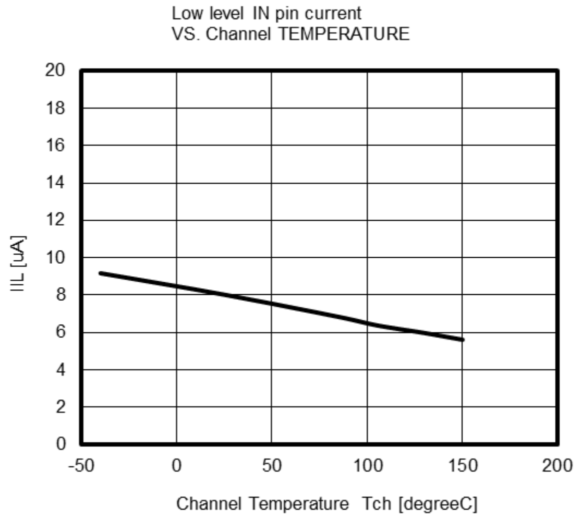


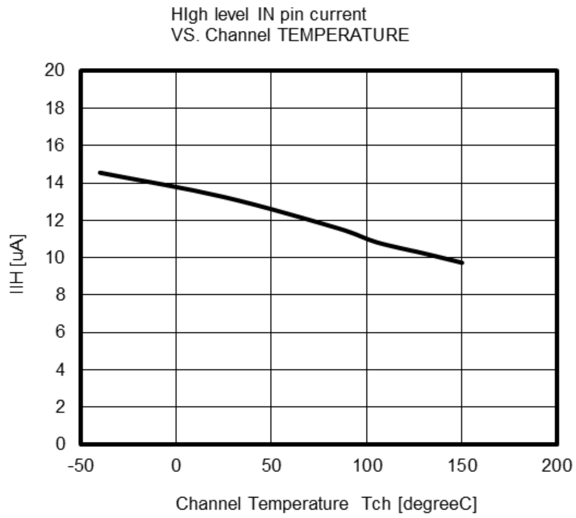


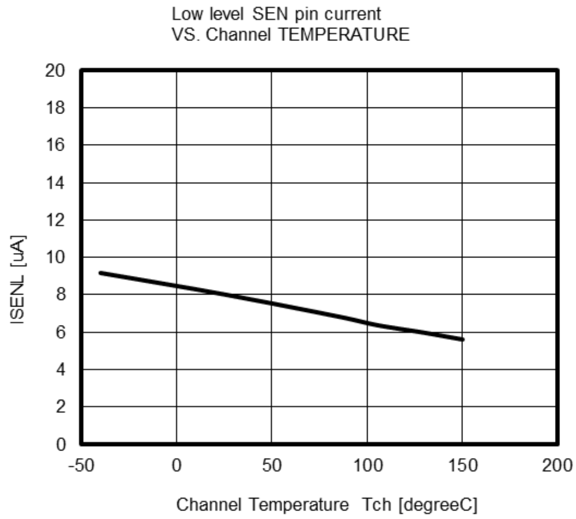


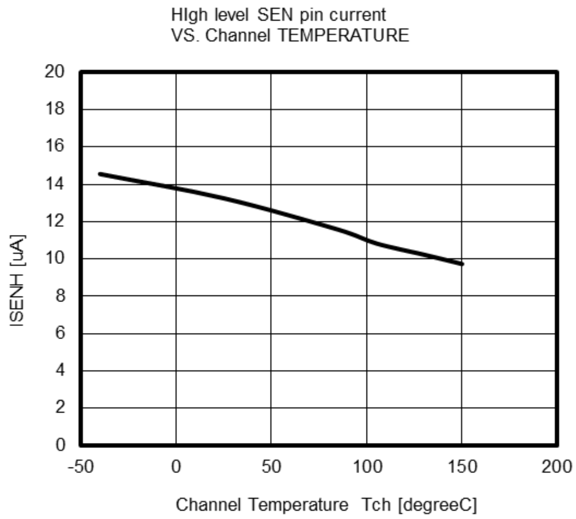

Low level SEN pin voltage
VS. Channel TEMPERATURE
VSENL [V]
Channel Temperature Tch [degreeC]


High level SEN pin voltage
VS. Channel TEMPERATURE
VSENH [V]
Channel Temperature Tch [degreeC]

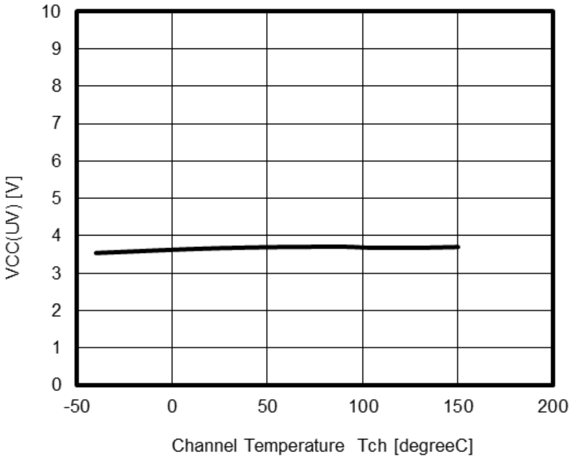

Low level IN pin current
VS. Channel TEMPERATURE
IIL [uA]
Channel Temperature Tch [degreeC]


HIgh level IN pin current
VS. Channel TEMPERATURE
IIH [uA]
Channel Temperature Tch [degreeC]

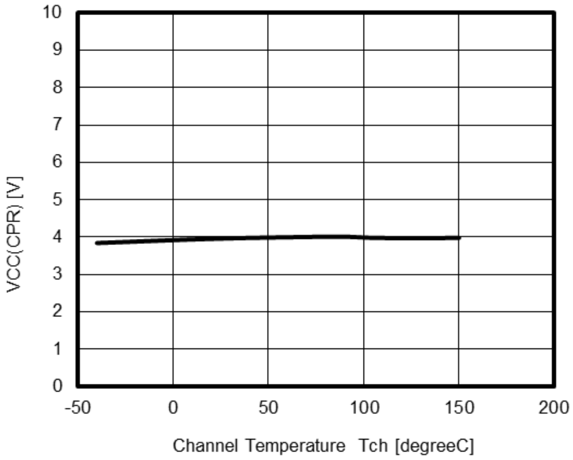

Low level SEN pin current
VS. Channel TEMPERATURE
ISENL [uA]
Channel Temperature Tch [degreeC]


HIgh level SEN pin current
VS. Channel TEMPERATURE
ISENH [uA]
Channel Temperature Tch [degreeC]

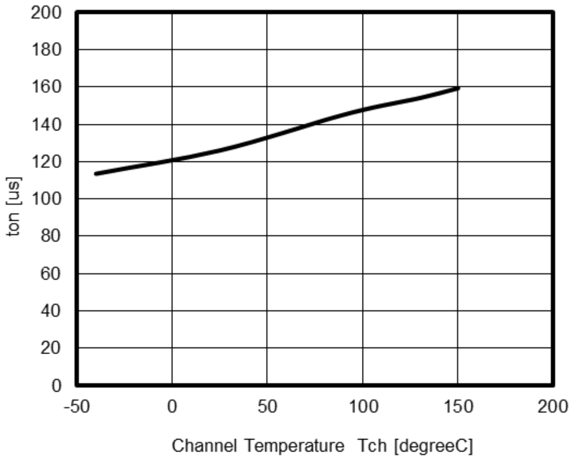
Under voltage shutdown
VS. Channel TEMPERATURE



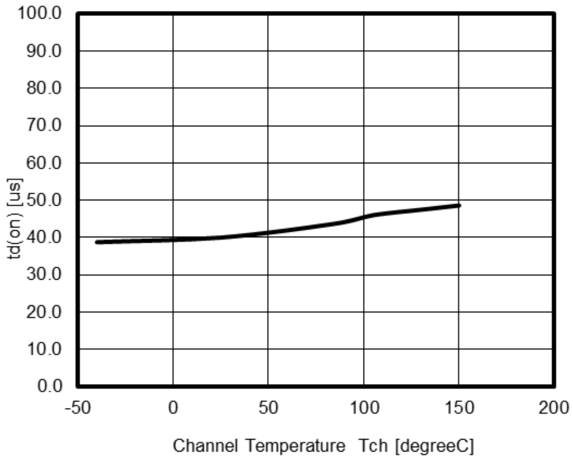
Under voltage shutdown
VS. Channel TEMPERATURE



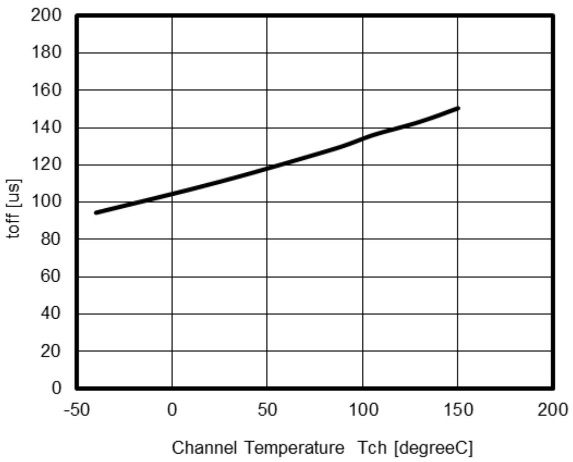
Turn on time
VS. Channel TEMPERATURE



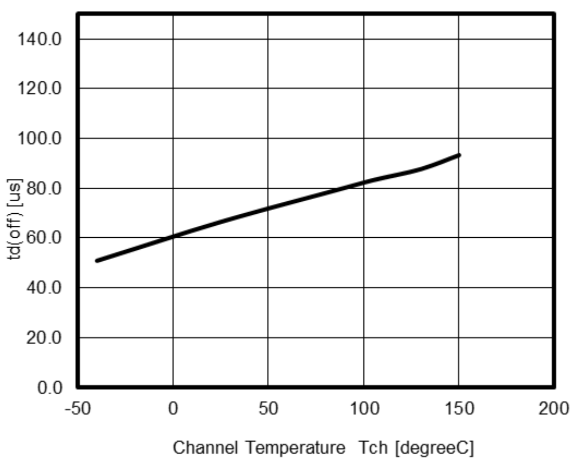
Turn on delay time
VS. Channel TEMPERATURE

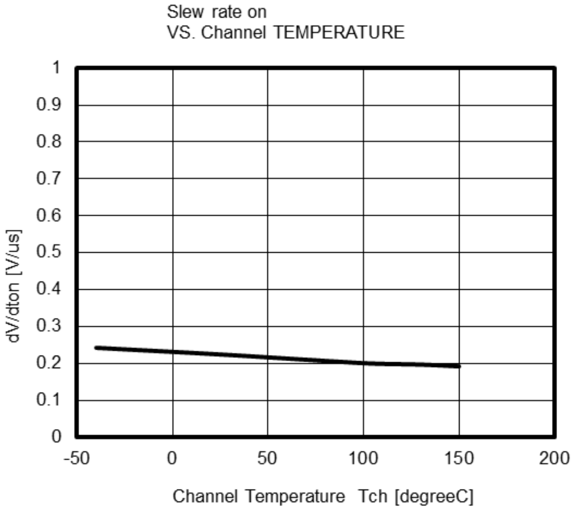


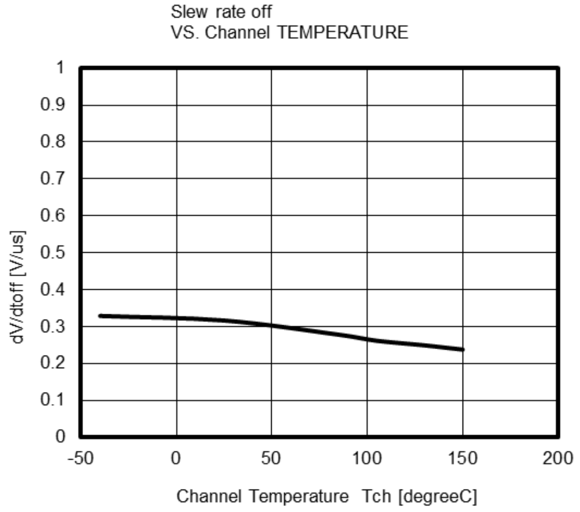
Turn off time
VS. Channel TEMPERATURE

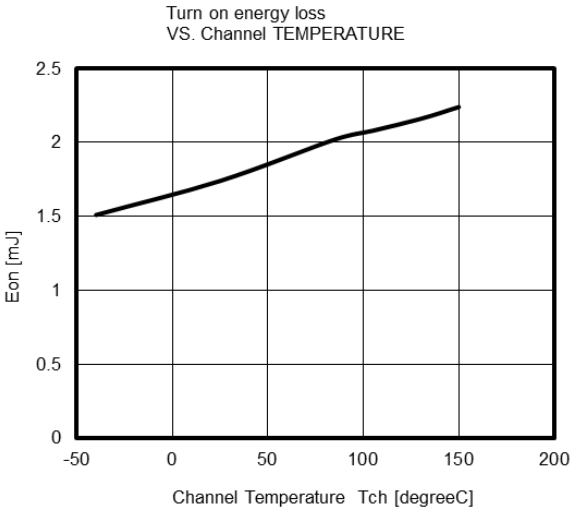


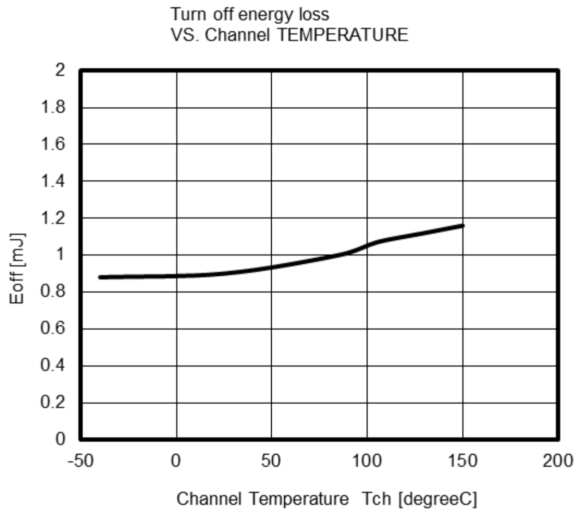
Turn off delay time
VS. Channel TEMPERATURE

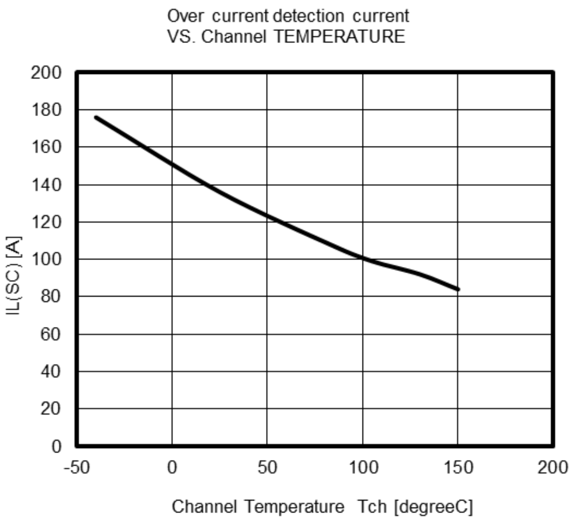


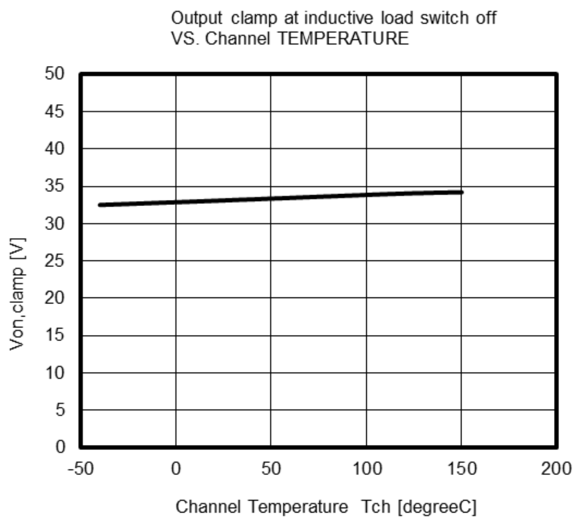

Slew rate on
VS. Channel TEMPERATURE
dV/dton [V/us]
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
-50
0
50
100
150
200
Channel Temperature Tch [degreeC]

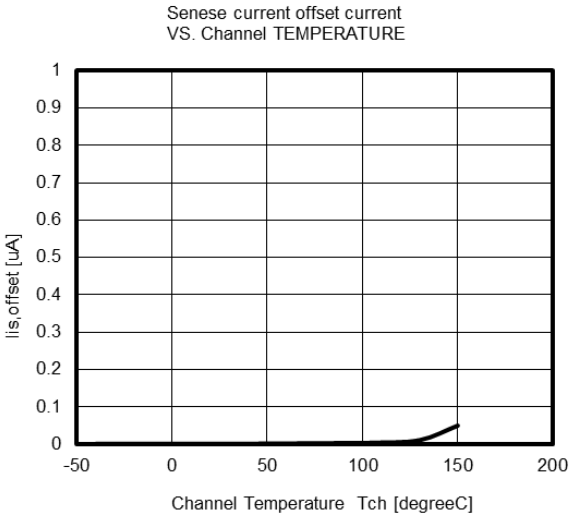

Slew rate off
VS. Channel TEMPERATURE
dV/dtoff [V/us]
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
-50
0
50
100
150
200
Channel Temperature Tch [degreeC]

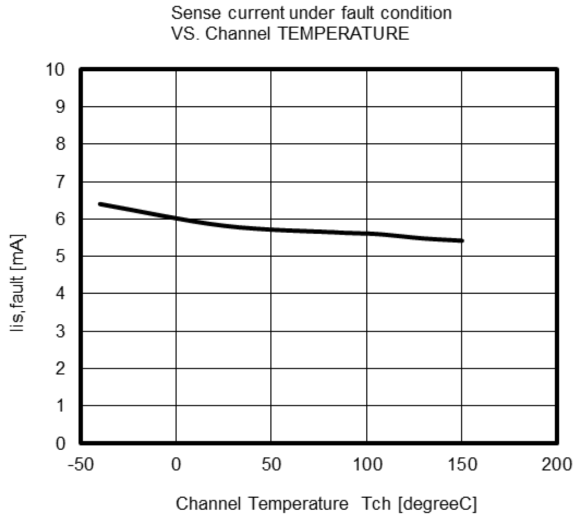

Turn on energy loss
VS. Channel TEMPERATURE
Eon [mJ]
0
0.5
1
1.5
2
2.5
-50
0
50
100
150
200
Channel Temperature Tch [degreeC]

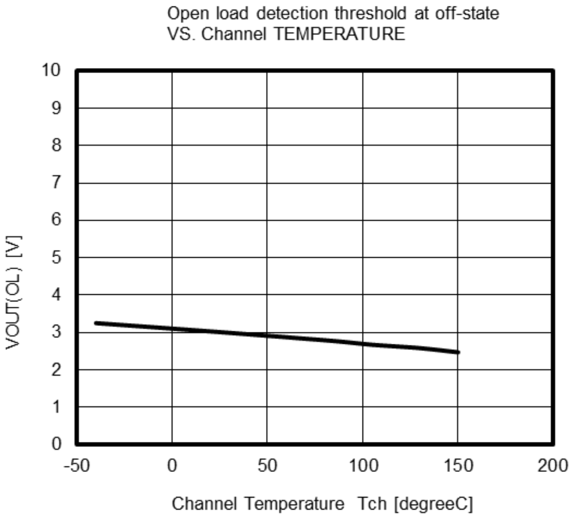

Turn off energy loss
VS. Channel TEMPERATURE
Eoff [mJ]
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
-50
0
50
100
150
200
Channel Temperature Tch [degreeC]


Over current detection current
VS. Channel TEMPERATURE
IL(SC) [A]
0
20
40
60
80
100
120
140
160
180
200
-50
0
50
100
150
200
Channel Temperature Tch [degreeC]

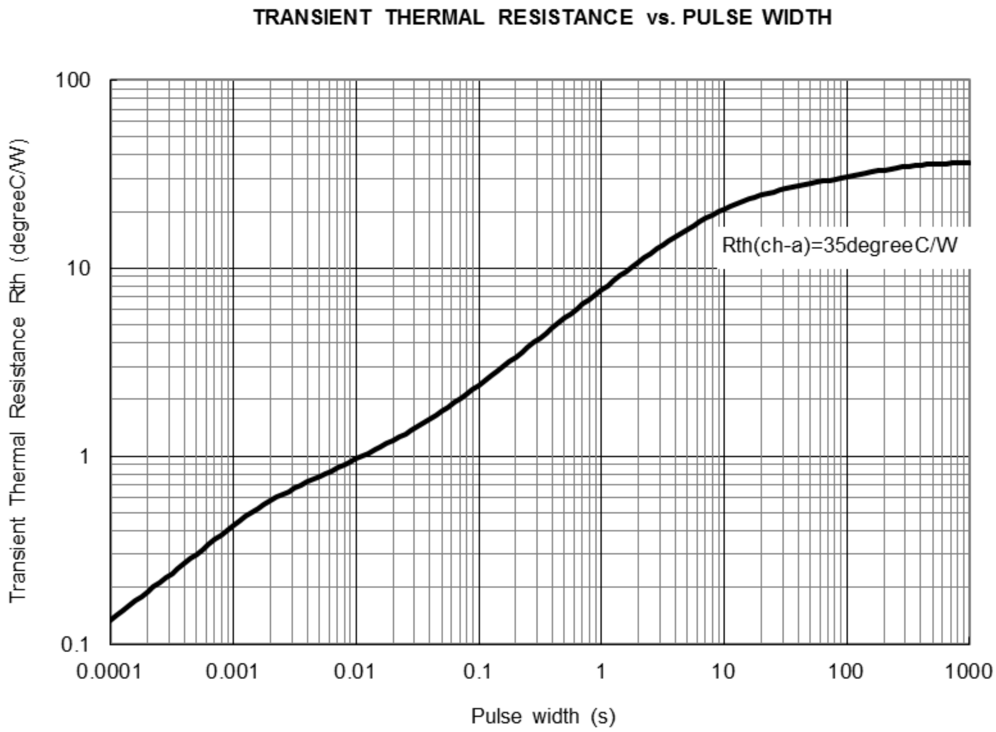

Output clamp at inductive load switch off
VS. Channel TEMPERATURE
Von,clamp [V]
0
5
10
15
20
25
30
35
40
45
50
-50
0
50
100
150
200
Channel Temperature Tch [degreeC]


Senese current offset current
VS. Channel TEMPERATURE
Iis,offset [uA]
Channel Temperature Tch [degreeC]

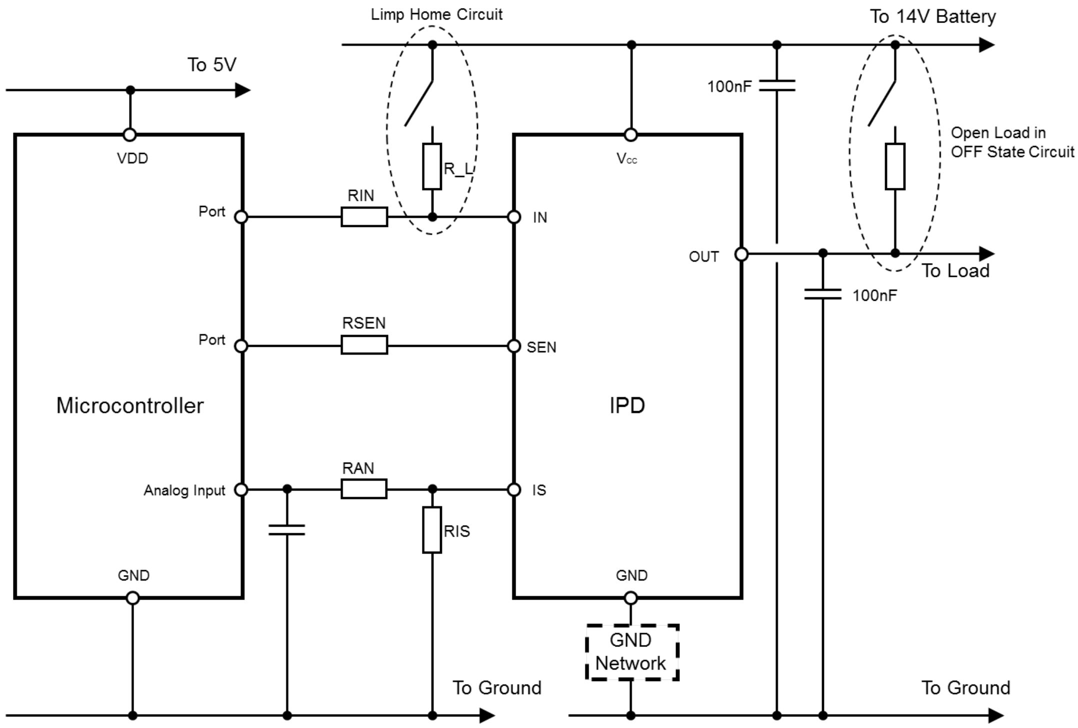

Sense current under fault condition
VS. Channel TEMPERATURE
Iis,fault [mA]
Channel Temperature Tch [degreeC]


Open load detection threshold at off-state
VS. Channel TEMPERATURE
VOUT(OL) [V]
Channel Temperature Tch [degreeC]

5. Thermal characteristics



6. Application example in principle

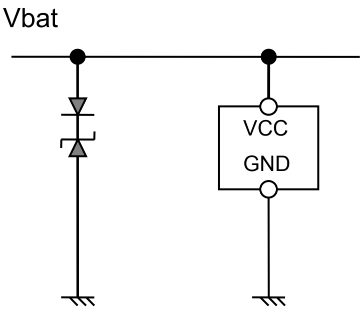


RIN, RSEN, RAN values are in range of 2k to 50kΩ depending microcontroller while R_L value is typically 4kΩ.

If necessary to raise HBM tolerated dose, adding resister between OUT terminal and Ground is effective. Resister's value is typically 100kΩ

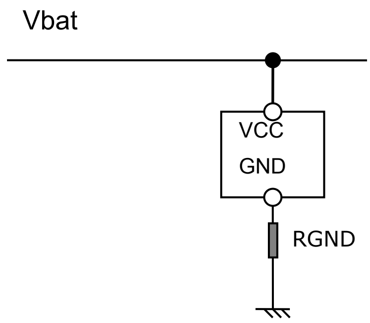
GND Network recommendation

In case of V_loaddump < 35V



No external component is required.

In case of 35V < V_loaddump < 42V



External resistor is recommended in order to limit the current through ZD_{AZ} at load dump condition. 100Ω is recommended as RGND.

Revision History	μPD166034T1U Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Mar 27, 2014	1-38	1st issue
2.00	May 22, 2015	23	"Device behavior at small load current conduction" is added.

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

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