To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

μPD168804

4 CH BUCK OR BOOST SELECTABLE CONSTANT CURRENT DRIVER IC WITH EXTERNAL POWER MOSFETS

DESCRIPTION

μPD168804 is a 4 channel constant current driver IC. One from "Buck" or "Boost" topology is selectable by the arrangement of external components and MODE pin setting. This IC can drive single or multiple current-loads (such as heaters and LEDs) in series with external power MOSFETs.

This IC controls soft-start slope of each channel at initial start-up.

Also it controls intermittent current by PWM signal from PWM0 to 3 independently.

FEATURES

- Flexible choice of Buck or Boost is available (one from Buck topology or Boost topology) by the arrangement of external Power MOSFET, Shottkey barrier diodes and other external components and MODE pin setting.
- High output current
  1500 mA MAX. per each channel (set by external current sense resistor)
- Chopping frequency = 1 MHz MAX.
- Wide input voltage range (Buck mode: $V_{OUT} < V_{IN}$, Boost mode: $V_{OUT} > V_{IN}$)
- On/Off and dimming control for each channel using PWM
- Thermal Protection function
- Over current protection for each channels
- Over voltage protection (Boost mode)
- Low voltage Lock-out function (UVLO)
- Stand-by (Enable) pin
- Efficient software development and various control, combined with All Flush MCU of NEC Electronics Corp

ORDERING INFORMATION

Part Number	Package
μPD168804GA-8EU-A Note	48-pin plastic LQFP (7 x 7) (0.5 mm pitch)

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

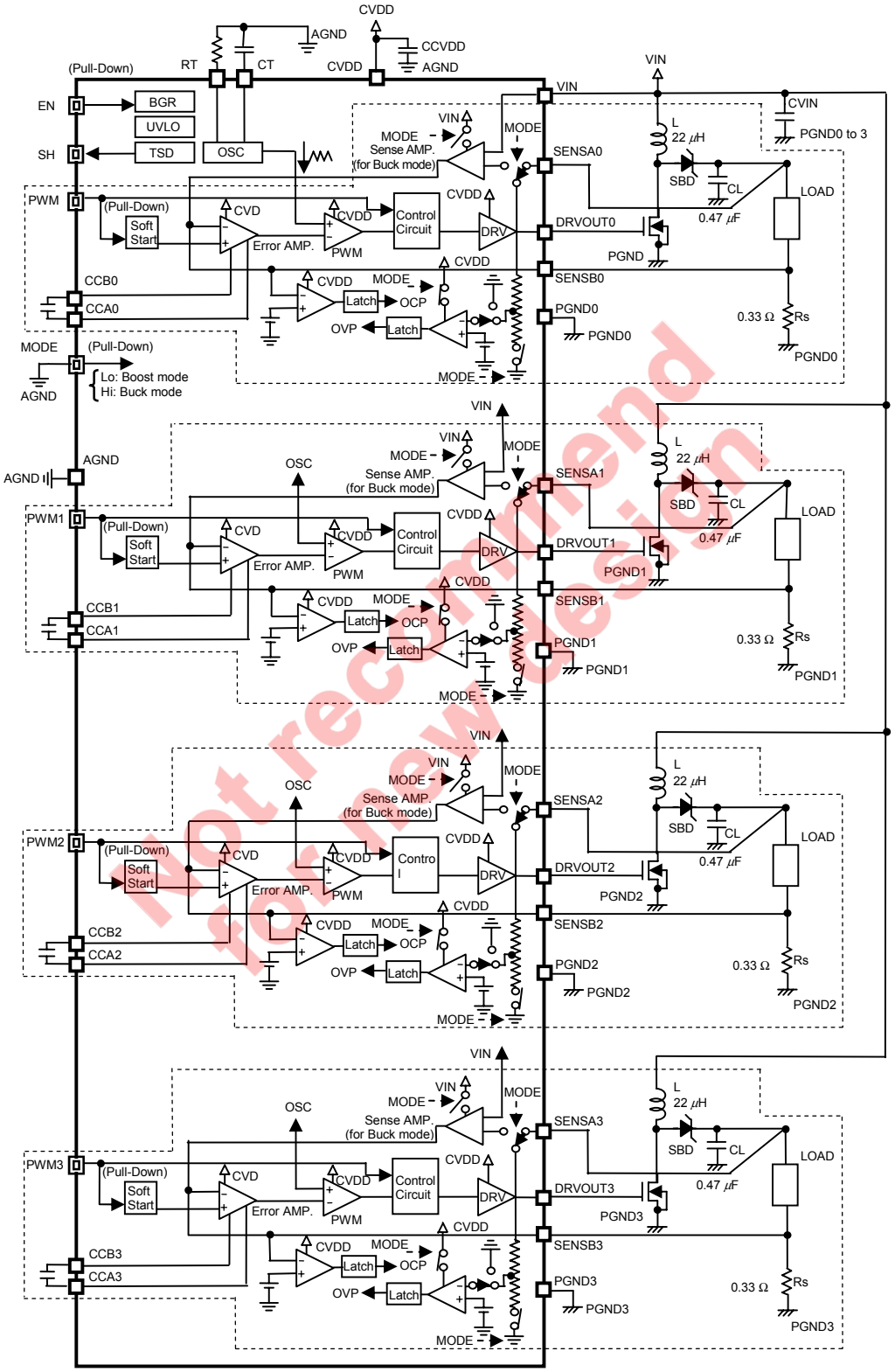
APPLICATION

- Heaters
- Low voltage industrial lighting
- LCD Back-up lighting
- Illuminated signs

Document No. S19652EJ1V0DS00 (1st edition)
Date Published March 2009 NS
Printed in Japan

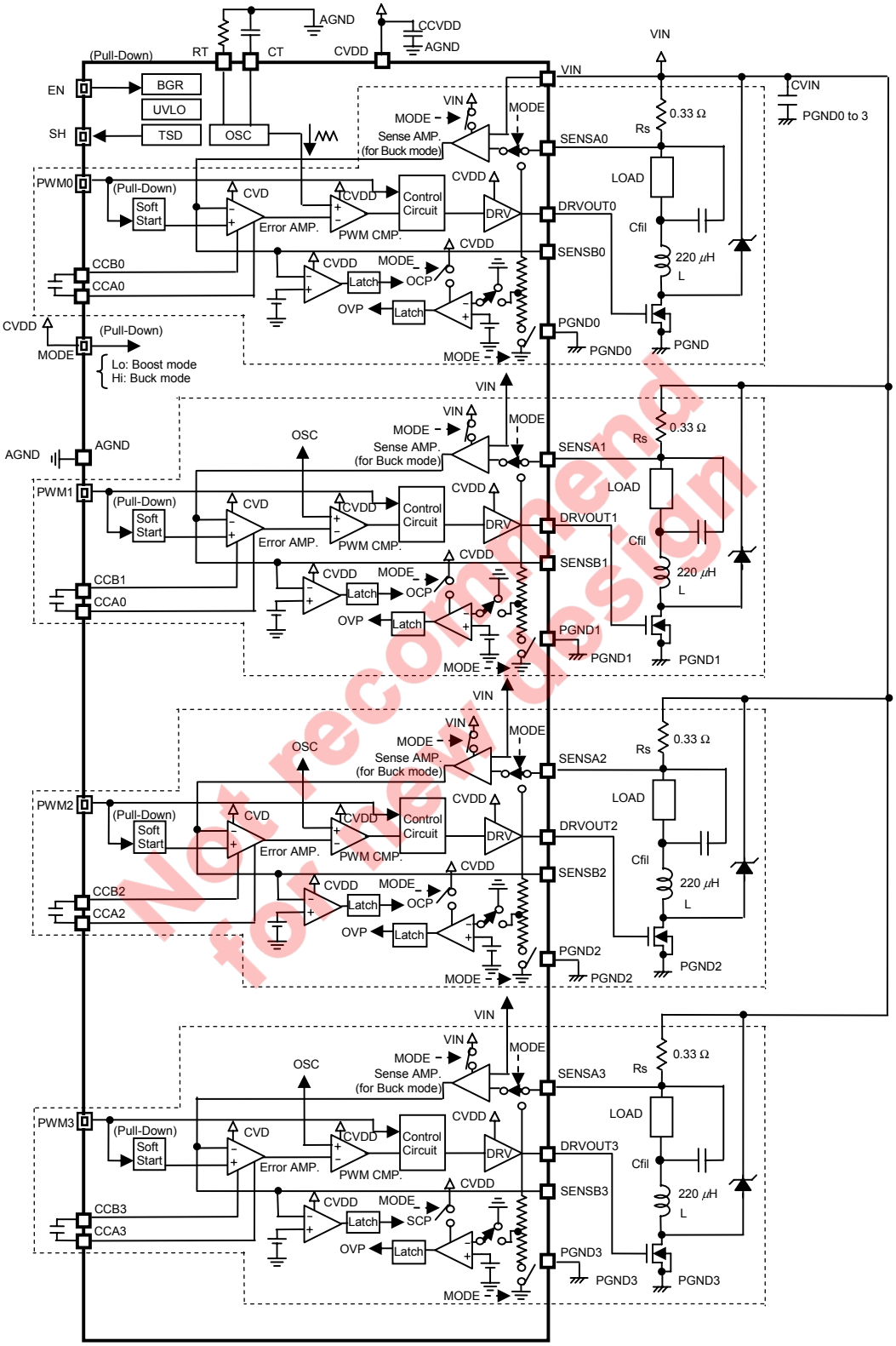
1. BLOCK DIAGRAMS

Boost mode



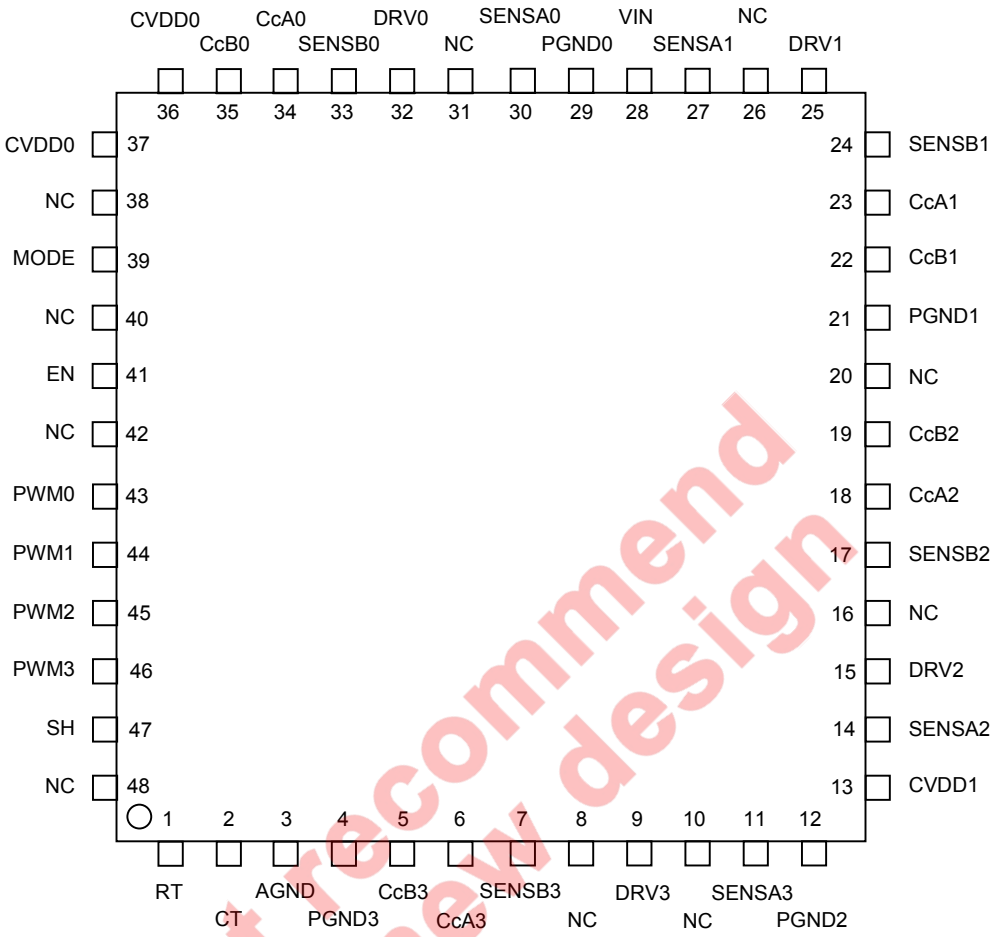
Caution This circuit is only for reference and does not guarantee the actual performance.

Buck mode



Caution This circuit is only for reference and does not guarantee the actual performance.

2. PIN CONFIGURATION



3. PIN FUNCTIONS

(1/2)

Pin No.	Symbol	Function
1	RT	Resistor for triangular oscillator
2	CT	Capacitor for triangular oscillator
3	AGND	Analog ground
4	PGND3	Power ground
5	CcB3	Capacitor for Phase dissipation
6	CcA3	Capacitor for Phase dissipation
7	SENSB3	Current sense for each channel at Boost mode
8	NC	Non connection
9	DRV3	Gate drive output for Nch MOSFET
10	NC	Non connection
11	SENSA3	Current sense for each channel at Buck mode / voltage monitor pin for over voltage protection at Boost mode
12	PGND2	Power ground
13	CVDD1	Power supply for Control section 1
14	SENSA2	Current sense for each channel at Buck mode / voltage monitor pin for over voltage protection at Boost mode
15	DRV2	Gate drive output for Nch MOSFET
16	NC	Non connection
17	SENSB2	Current sense for each channel at Boost mode
18	CcA2	Capacitor for Phase dissipation
19	CcB2	Capacitor for Phase dissipation
20	NC	Non connection
21	PGND1	Power ground
22	CcB1	Capacitor for Phase dissipation
23	CcA1	Capacitor for Phase dissipation
24	SENSB1	Current sense for each channel at Boost mode
25	DRV1	Gate drive output for Nch MOSFET
26	NC	Non connection
27	SENSA1	Current sense for each channel at Buck mode / voltage monitor pin for over voltage protection at Boost mode
28	VIN	Power supply for load
29	PGND0	Power ground
30	SENSA0	Current sense for each channel at Buck mode / voltage monitor pin for over voltage protection at Boost mode
31	NC	Non connection
32	DRV0	Gate drive output for Nch MOSFET
33	SENSB0	Current sense for each channel at Boost mode
34	CcA0	Capacitor for Phase dissipation
35	CcB0	Capacitor for Phase dissipation

(2/2)

Pin No.	Symbol	Function
36	CVDD0	Power supply for control and gate-driver section
37	CVDD0	Power supply for control and gate-driver section
38	NC	Non connection
39	MODE	Mode select input (H: Buck, L: Boost) with pull-down (200 kΩ)
40	NC	Internal option pin (normally open)
41	EN	Enable signal with pull-down (200 kΩ) high active
42	NC	Internal test control only at mass-production (normally open)
43	PWM0	PWM pulse input pin for dimming control with pull-down (200 kΩ), high active
44	PWM1	PWM pulse input pin for dimming control with pull-down (200 kΩ), high active
45	PWM2	PWM pulse input pin for dimming control with pull-down (200 kΩ), high active
46	PWM3	PWM pulse input pin for dimming control with pull-down (200 kΩ), high active
47	SH	Alert output indicating thermal shut down, "H" only at TSD
48	NC	Non connection

Note The 40 and 42 pin are unused but connected inside. Please keep them opened.

4. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

(unless otherwise specified, T_A = 25°C, PWB: based on JEDEC, FR-4, 4 layers 101.5 mm x 114.5 mm x 1.6 mmt)

Parameter	Symbol	Conditions	Rating	Unit
Input voltage	V_{IN}		–0.3 to +42	V
Power supply voltage	CVDD		–0.3 to +6	V
Current sense voltage	VsensA	SENSA0 to 3 at Boost	–0.3 to +42	V
		SENSA0 to 3 at Buck	V_{IN} – 5 to V_{IN}	V
Current sense voltage	VsensB	SENSB0 to 3 at Boost	–0.3 to CVDD	V
Drive output voltage	Vdrvout		–0.3 to CVDD	V
Logic input voltage	VI	EN, PWMn	–0.3 to CVDD	V
Gate drive peak current	Idrv_peak	To drive Power MOSFET, fchop = 1 MHz, pulse width = 10 ns	700	mA
Total power dissipation	Pt		1.0	W
Strage temperature	Tst		–55 to +150	°C
Junction temperature	Tj		150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

(unless otherwise specified, T_A = 25°C, PWB: based on JEDEC, FR-4, 4 layers 101.5 mm x 114.5 mm x 1.6 mmt)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage Note1	V_{IN}	At Buck mode (V_{IN} > V_{OUT})	9		38	V
		At Boost mode (V_{IN} < V_{OUT})	9		28	V
Output voltage Note2	VsensA	At Boost mode (V_{IN} < V_{OUT})			37	V
Power supply voltage Note1	CVDD		4.5	5.0	5.5	V
Recommended frequency for PWMn	Fpwm	PWM Duty = 50%			500	Hz
Recommended duty cycle range for PWMn pins Note3	Dpwm	PWMn	0		100	%
Operating temperature	Top		–40		85	°C
Junction temperature	Tj		–40		125	°C
PWM wait time	Twait	Wait time after EN rise	100			μs
Gate driver output average current	Idrv	Cload = 1000 pF		60		mA

Notes1. Power on: CVDD have to be started before V_{IN} is supplied.
Power off: V_{IN} have to be dropped before CVDD is stopped.

2. Recommended maximum LOAD number in series: 7 pcs in case of LED (depends on maximum chopping PWM duty)

3. Duty ratio of load current versus that of “PWMn” around 0% and 100% are not linear. The compensation by MCU is recommended.

Electrical Characteristics (tested at wafer level)

(Test conditions: Buck mode, unless otherwise specified, T_A = 25°C, V_{IN} = 30 V, CVDD = 5 V, no-external power MOSFET)

Total						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating current consumption	Iop CVDD	EN = High, PWMn = High, CVDD pin	-	3.3	7	mA
	Iop V_{IN}	VIN pin at Buck	-	-	250	μA
		VIN pin at Boost	-	-	250	μA
Standby current consumption	Istby1	Mode = Low (at Boost mode), EN = Low, CVDD pin	-	-	10	μA
	Istby2	Mode = High (at Buck mode), EN = Low, CVDD pin	-	-	60	μA
Gate driver switch section						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Driver on resistance	$R_{on(source)}$	Isource = 100 mA	-	7	12	Ω
	$R_{on(sink)}$	Isink = 100 mA	-	7	12	Ω
Protection circuit						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UVLO threshold voltage	Vluvlo	Lower threshold	-	3.3	-	V
	Vhys_uvlo	Hysteresis width	-	0.3	-	V
SH output high voltage	VSHH	I_{OUT} = 10 mA	0.8 x CVDD	-	CVDD	V
SH output low voltage	VSHL	I_{OUT} = –10 mA	0	-	0.2 x CVDD	V
Over current protection threshould voltage Note1	Vtsensb	At Boost mode	0.315	0.35	0.385	V
Over voltage protection Note2	Vovp	At Boost mode	38	39.5	41	V
Logic control circuit section						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High input level	VIH	EN with internal Pull-down (200 kΩ)	0.7 x CVDD	-	CVDD	V
Low input level	VIL		0	-	0.3 x CVDD	V
Pull-down resistance	Rpd		100	200	300	kΩ
Reference voltage section etc.						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Reference voltage timing section	Vref	Tested at Comparator-output	0.102	0.115	0.128	V
Soft-start time	tso	Internal timing	32	-	128	μs
Current Amp. Output (high voltage (V_{IN}) side						
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage	Vtcsens	MODE = High, V_{IN}–Vsensa = 0.115 V, Measused at VSENSB	0.105	0.115	0.125	V

Notes1. Eounce time at Boost mode is 8 μs MIN..

2. Thermal shutdown should work over 150°C.

5. DEVICE DESCRIPTIONS

μPD168804 is the 4 channel constant current driver IC with external power MOSFETs. One of "Buck" or "Boost" topology can be chosen. Power supply voltage of 9 to 38 V is recommended and 5 V for control section is needed. Constant load current upto 1.5 A is set by external current sensing resister "R_S" as R_S = 0.115 (V)/I_{LOAD}. Dimming is controlled by the PWM signal input to turn on/off each control circuit. And at the initial start-up, the digital soft-start function controls rush current.

Choice of Topology

One from "Buck" or "Boost" topology can be selected by the arrangement of external components and MODE pin setting.

MODE pin should be fixed to GND directly to choose "Boost" topology. Or MODE pin should be fixed to CVDD to choose "Buck" topology. Please never connect unsuitable external components against MODE setting.

MODE	Topology
L	Boost
H	Buck

Remark For "Boost", refer to the **1. BLOCK DIAGRAMS** in **Boost mode**, and for "Buck" refer to the **1. BLOCK DIAGRAMS** in **Buck mode**.

Load Current Setting

Target Current value is set by the value of current sensing resistor "R_S" for each channel.

Maximum LOAD current of each channel is defined by R_S x I_{LOAD} = 0.115 V.

We recommend the tolerance of R_S = ±1% or less, because it effects to the current tolerance directly.

Example

R_S (Ω)	I_{LOAD} (A)	P_{RS} (W)
0.33	0.35	0.04
0.18	0.64	0.073
0.12	0.96	0.11
0.082	1.4	0.16

Caution R_S of unused channel must be fixed to "0 Ω".

Choice of External Power MOSFET

External power MOSFET can be selected in accordance to the necessary voltage, current and heating.

We recommend High speed MOSFETs for DC/DC converters which can be drived at Vgs = 5 V. It helps to improve the total efficiency.

Reference

Recommended external power MOSFET (unless otherwise specified, T_A = 25°C,)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Threshould gate voltage of external MOSFET	Vgst		1.5	2.0	2.5	V
Gate voltage at on state of external MOSFET	Vgs		4	4.5	5	V

Remark External power MOSFET for example

I_{LOAD} ≤ 0.75 A: μPA2756GR (NEC: Dual, Nch)

0.75 < I_{LOAD} ≤ 1.5 A: 2SK2414Z (NEC, Nch)

Connection of Unused Pins

If you do not use one or more channels, please set the unused pins as indicated in the following table.

Pin name	For Boost operation	For Buck operation
PWM0 to 3	Open or pull-down	Open or pull-down
SENSA0 to 3	Connect to VIN	Connect to VIN
SENSB0 to 3	Connect to GND	Open
DRVOUT0 to 3	Open	Open
CCA0 to 3	Open	Open
CCB0 to 3	Open	Open

Protection Circuit

μPD168804 has four kinds of protection circuits. Each protection works as indicated bellow.

Protection	Stop operation	Status after operation	SH output
Thermal	All channel	Protection kept (latched operation)	H
Over voltage	Protected channel only	Protection kept (latched operation)	L
Over current	Protected channel only	Protection kept (latched operation)	L
Low voltage (UVLO)	All channel	Automatic recovery	L

Thermal shut-down function is the final protection for safety and it works higher than 150°C.

Once junction temperature exceeds 150°C, reliability of device is not guaranteed any more.

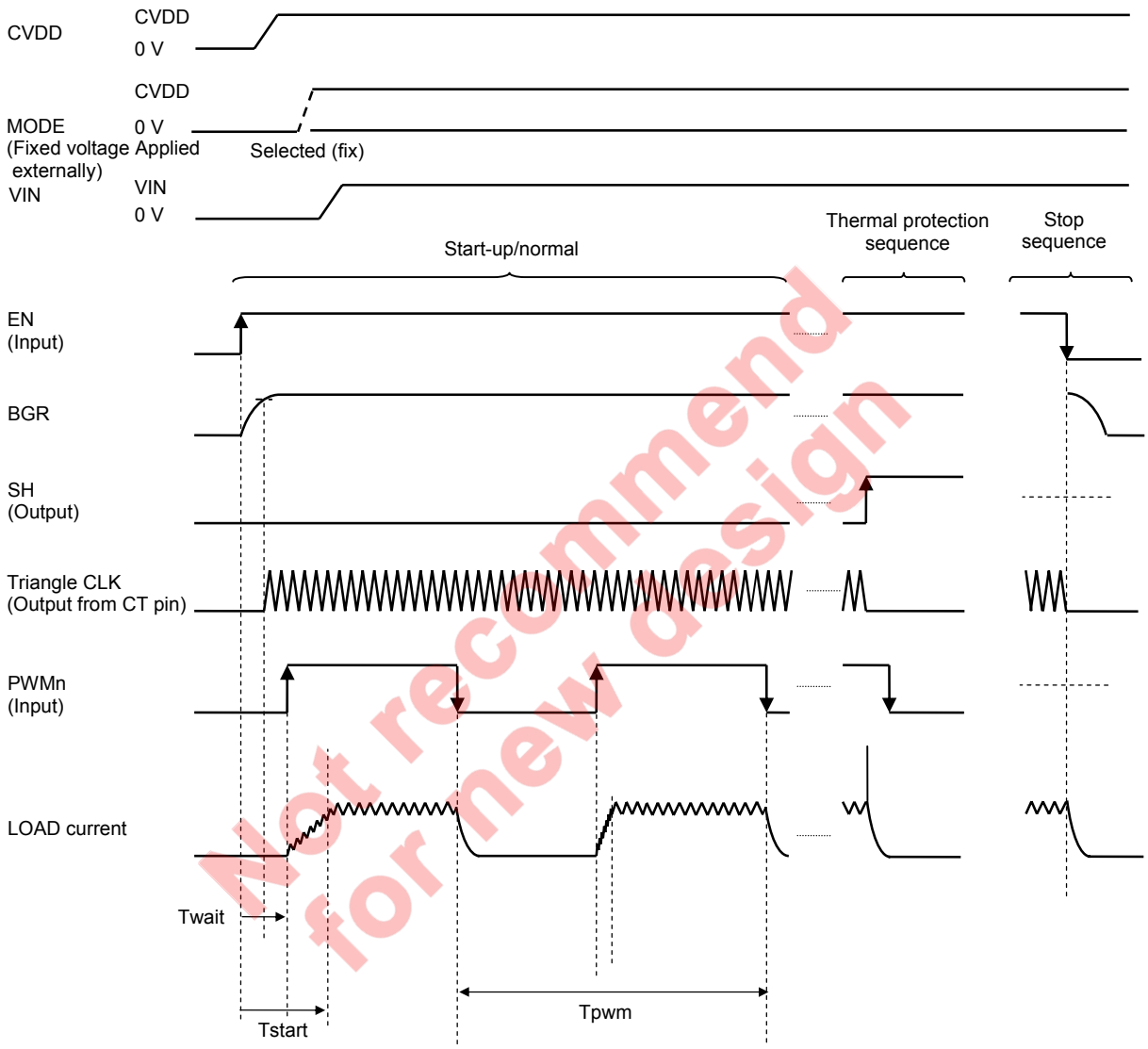
Thermal shut-down starts to function from 400 μs after EN rises.

Over voltage and over current protection neglect the pulse shorter than 12 μs TYP.. To avoid miss-operation caused by noise.

Maximum chopping duty is limited to 80% MAX. to avoid to reduce over shoot current.

6. FUNCTIONAL DESCRIPTION AND TIMING CHART

Average LOAD current of each channel is controlled by the PWM signal applied to each PWMn pin.
Soft-start will be added automatically by internal current.



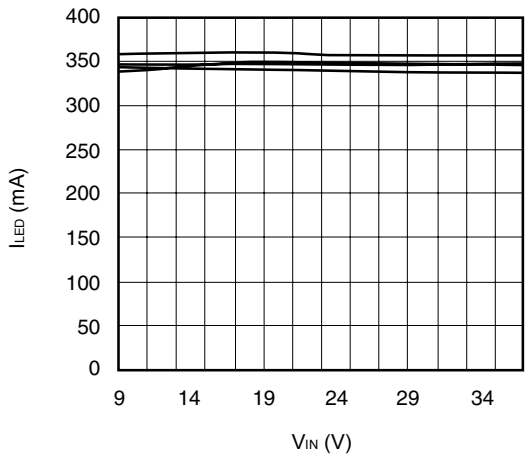
Caution CPU must wait for PWM wait time (Twait) before it send PWM signal.

Remark Tstart: Total start-up time (from EN = Low→High upto LOAD current = 90% of nominal)
Tpwm: Cycle time of PWM

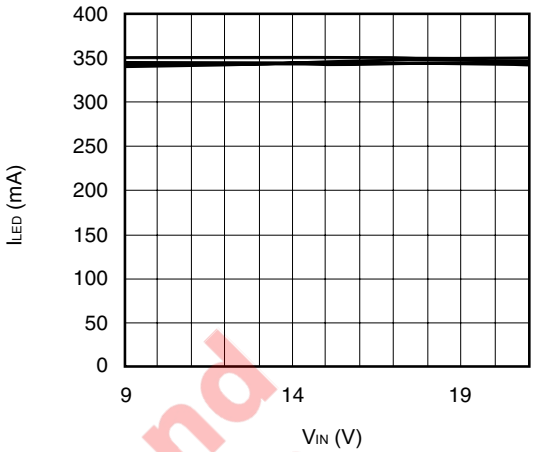
7. TYPICAL OPERATION DATA

Current tolerance (R_S = 0.33 Ω±1%)

Buck (two LEDs)

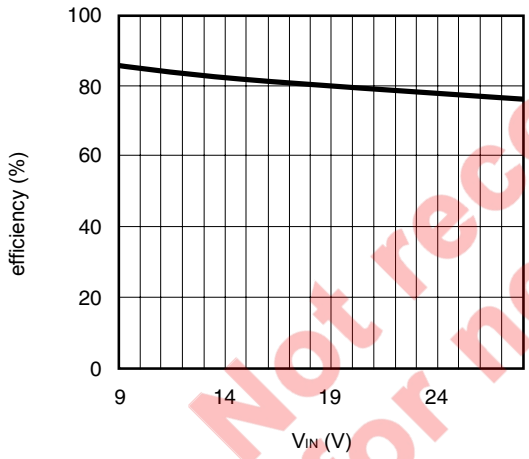


Boost (eight LEDs)

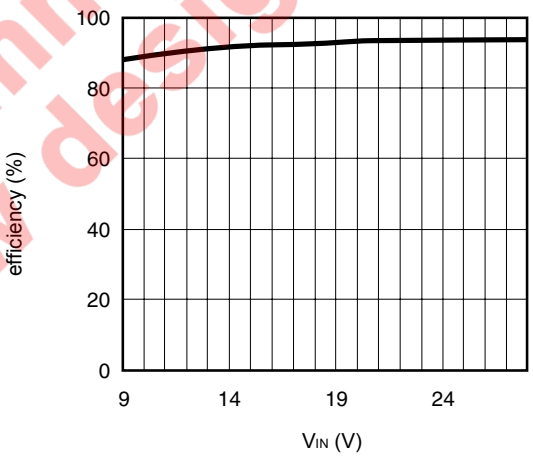


Efficiency

Buck (one LED)

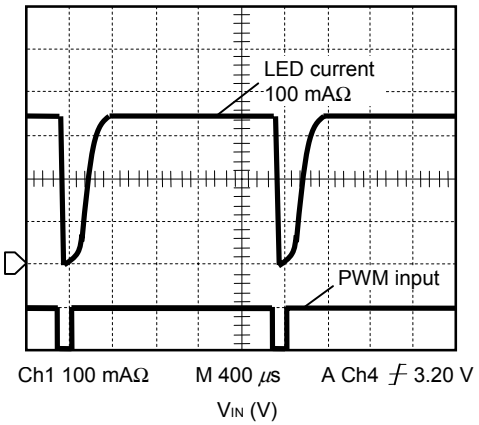


Boost (nine LEDs)

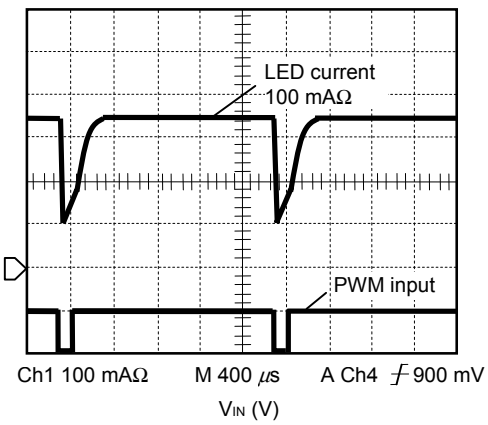


Operating waveform (load current measured by current probe vs. PWM input)

Buck (two LEDs) L = 68 μH

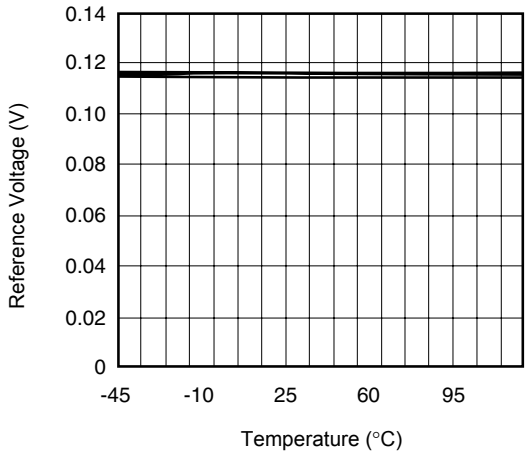


Boost (eight LEDs) L = 22 μH, CL = 0.47 μF

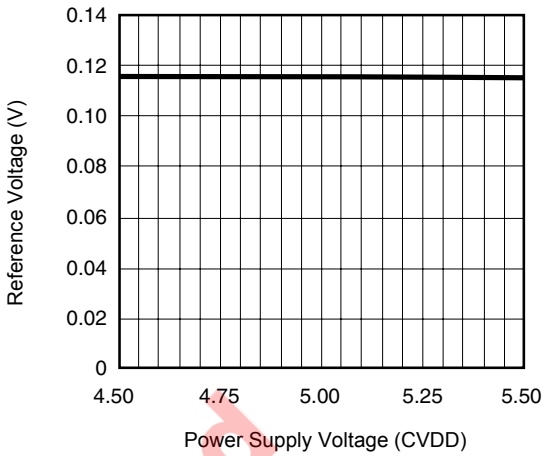


Caution These data are only for reference and does not guarantee actual performance.

Reference Voltage vs. Temperature



Reference Voltage vs. Power Supply Voltage (CVDD)

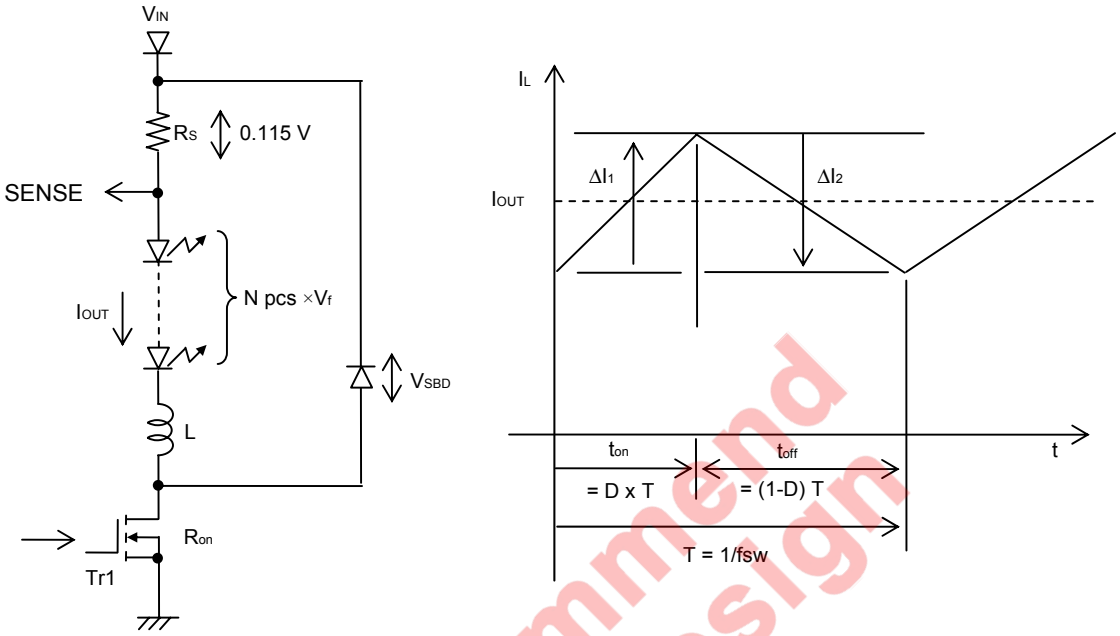


Caution These data are only for reference and does not guarantee actual performance.

8. APPLICATION NOTE

(1) Buck Topology

The circuit diagram of major parts and Inductor current waveform is described below.



Remark D: ON-Duty of chopping PWM
fsw: Oscillating frequency of internal oscillator

Examination of ON-Duty at Operation

When Tr1 is ON:

$$\Delta I_1 = \frac{V_{IN} - 0.115 - N \times V_f - R_{on} \times I_{OUT}}{L} DT$$

When Tr1 is OFF :

$$\Delta I_2 = \frac{V_{IN} - 0.115 - N \times V_f - (V_{IN} + V_{SBD})}{L} (1 - D) T$$

$$= \frac{- N \times V_f - 0.115 - V_{SBD}}{L} (1 - D) T$$

When load current is controlled constantly, $\Delta I_1 + \Delta I_2 = 0$

$$\frac{1}{L} ((V_{IN} - 0.115 - N \times V_f - R_{on} \times I_{OUT}) D - (N \times V_f + 0.115 + V_{SBD}) (1 - D) T) = 0$$

If we set

$V_{on} = V_{IN} - 0.115 - N \times V_f - R_{on} \times I_{OUT}$

$V_{off} = N \times V_f + 0.115 + V_{SBD}$

$V_{on} \times t_{on} - V_{off} \times t_{off} = 0$

$V_{on} \times t_{on} - V_{off} (T - t_{on}) = 0$

On-Duty "D" is described as $D = \frac{V_{off}}{V_{on} + V_{off}}$

Maximum ON-Duty for chopping control (not PWM dimming duty) is limited to 80%, we have to confirm actual Duty is less than 80% with this formula.

Calculation of Inductance

Next we will calculate the inductance value from the target ripple current as,

$$\Delta I_1 = \frac{V_{on}}{L} DT$$

$$= \frac{V_{on}}{L} \times \frac{1}{fsw} \times \frac{V_{off}}{V_{on} + V_{off}}$$

Therefore,

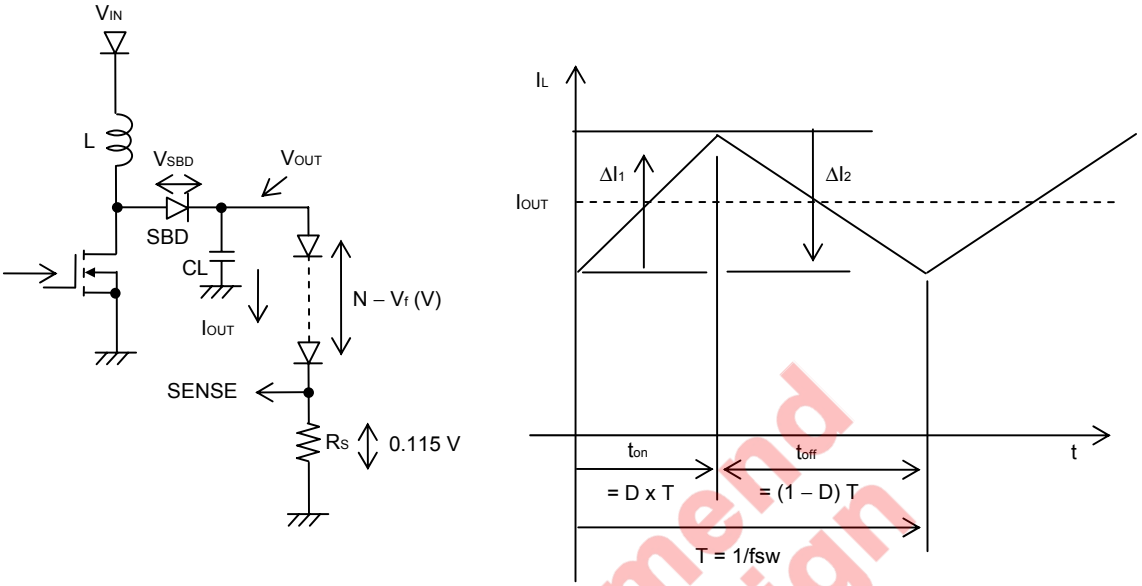
$$L = \frac{V_{on}}{\Delta I_1} \times \frac{1}{fsw} \times \frac{V_{off}}{V_{on} + V_{off}}$$

$\Delta I_1, \Delta I_2 \leq I_{OUT}$ to keep the current continuous.

Remark The inductance value should be greater than the calculated here.
Please down load the calculation sheet to help calculation from our web site.

(2) Boost Topology

The circuit diagram of major parts and Inductor current waveform is described below.



Remark D: ON-Duty of chopping PWM (PWM0 to 3 = 5 V)

fsw: Oscillating frequency of internal oscillator

Calculation of Inductance

We will calculate the inductance value from the target ripple current ΔI_2 as,

If we set ON-Duty as "D"

$$V_{OUT} + V_{SBD} - V_{IN} = L \frac{\Delta I_2}{(1 - D)\,T}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad \text{from} \quad \frac{1}{1 - D} = \frac{V_{OUT}}{V_{IN}}$$

Therefore,

$$L = \frac{V_{OUT} + V_{SBD} - V_{IN}}{\Delta I_2} (1 - D)\,T$$

$$= \frac{V_{OUT} + V_{SBD} - V_{IN}}{\Delta I_2} \times \frac{V_{IN}}{V_{OUT}} \times T$$

$$= \frac{N \times V_f + 0.115 + V_{SBD} - V_{IN}}{\Delta I_2} \times \frac{V_{IN}}{N \times V_f + 0.115} \times \frac{1}{fsw}$$

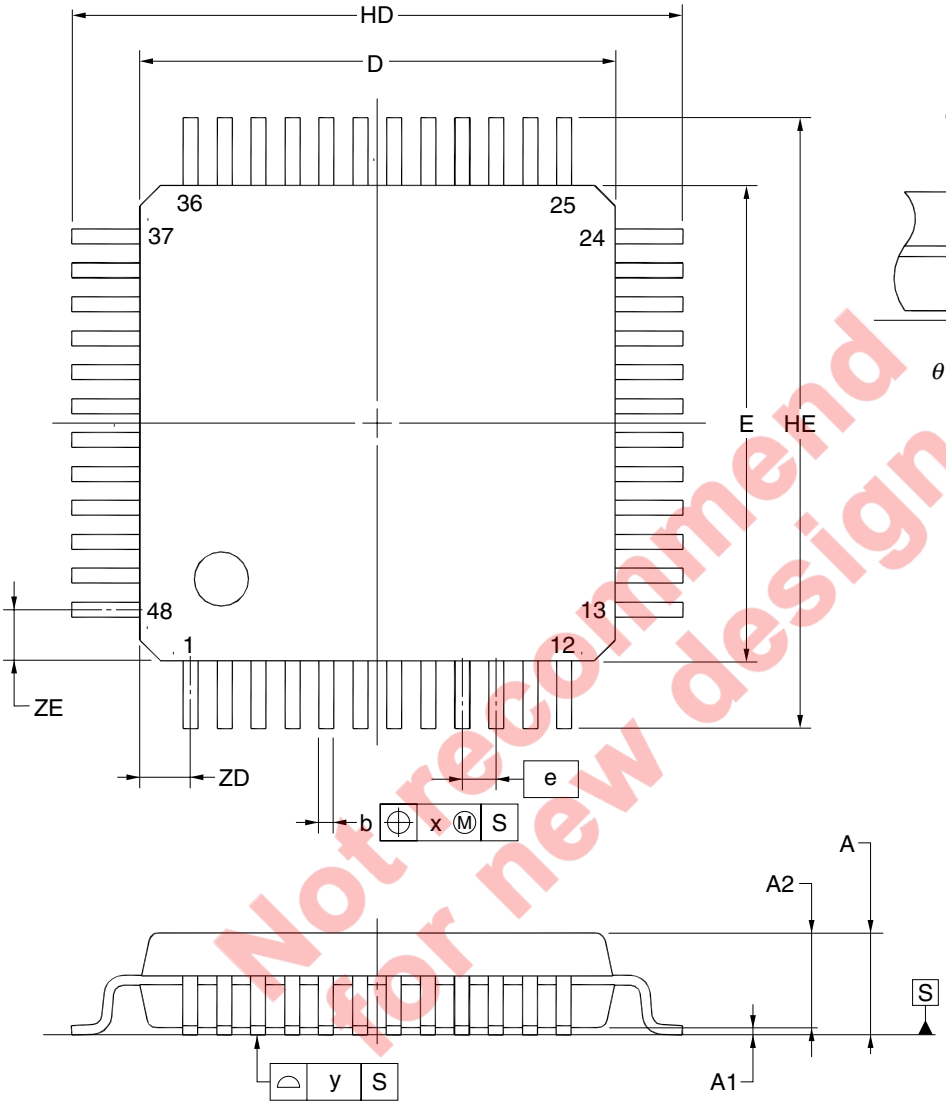
Caution The inductance should be greater the calculated here.

The ripple current flows the load is less than this calculated value by the effect of CL.

And if you change CL from 0.47 μF, you have to check the phase compensation of feed-back amplifier.

9. PACKAGE DRAWING

48-PIN PLASTIC LQFP (FINE PITCH)(7x7)



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

P48GA-50-8EU

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

10. RECOMMENDED SOLDERING CONDITIONS

The μPD168804 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

μPD168804GA-8EU-A [Note1]: 48-pin plastic LQFP (7 x 7) (0.5 mm pitch)

Soldering	Soldering Conditions	Recommended Method Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds MAX. (at 220°C or higher), Count: Three times. Exposure limit: 7 days [Note2] (after that, prebake at 125°C for 10 hours). Flux: Rosin flux with few chlorine (0.2 Wt% or below) recommended. <Precaution> Products other than in heat-resistant trays (such as those packaged in a magazine, taping, or non-thermal-resistant tray) cannot be baked in their taping package.	IR60-107-3

Notes 1. Pb-free (This product does not contain Pb in external electrode and other parts.)

2. After opening the dry pack, store it at 5 to 30°C or less and 70% RH or less for the allowable storage period.

Caution Do not use different soldering methods together.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

- **The information in this document is current as of March, 2009. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**
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