To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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April 1st, 2010
Renesas Electronics Corporation

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PRELIMINARY DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

μPD703130

V850E/MS2
32-BIT SINGLE-CHIP MICROCONTROLLER

The μPD703130 is a member of the V850 Series of 32-bit single-chip microcontrollers designed for real-time control operations. These microcontrollers provide on-chip features, including a 32-bit CPU, RAM, interrupt controller, real-time pulse unit, serial interface, A/D converter, and DMA controller.

The μPD703130 is a ROMless version product.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850E/MS2 User's Manual Hardware:	**U14985E**
V850E/MS1, V850E/MS2 User's Manual Architecture:	**U12197E**

FEATURES

- Number of instructions: 81
- Minimum instruction execution time 30 ns (@ 33 MHz operation)
- General-purpose registers 32 bits × 32
- Instruction set suitable for control applications
- Internal memory ROM: None
  RAM: 4 KB
- Advanced on-chip interrupt controller
- Real-time pulse unit suitable for control operations
- Powerful serial interface (on-chip dedicated baud rate generator)
- On-chip clock generator
- 10-bit resolution A/D converter: 4 channels
- DMA controller: 4 channels
- Power saving functions

APPLICATIONS

- Optical storage equipment (DVD players, etc.)
- System control for digital consumer equipment, etc.

The information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion, may withdraw the product prior to its production.
Not all products and/or types are availabe in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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Printed in Japan

The mark ★ shows major revised points.

ORDERING INFORMATION

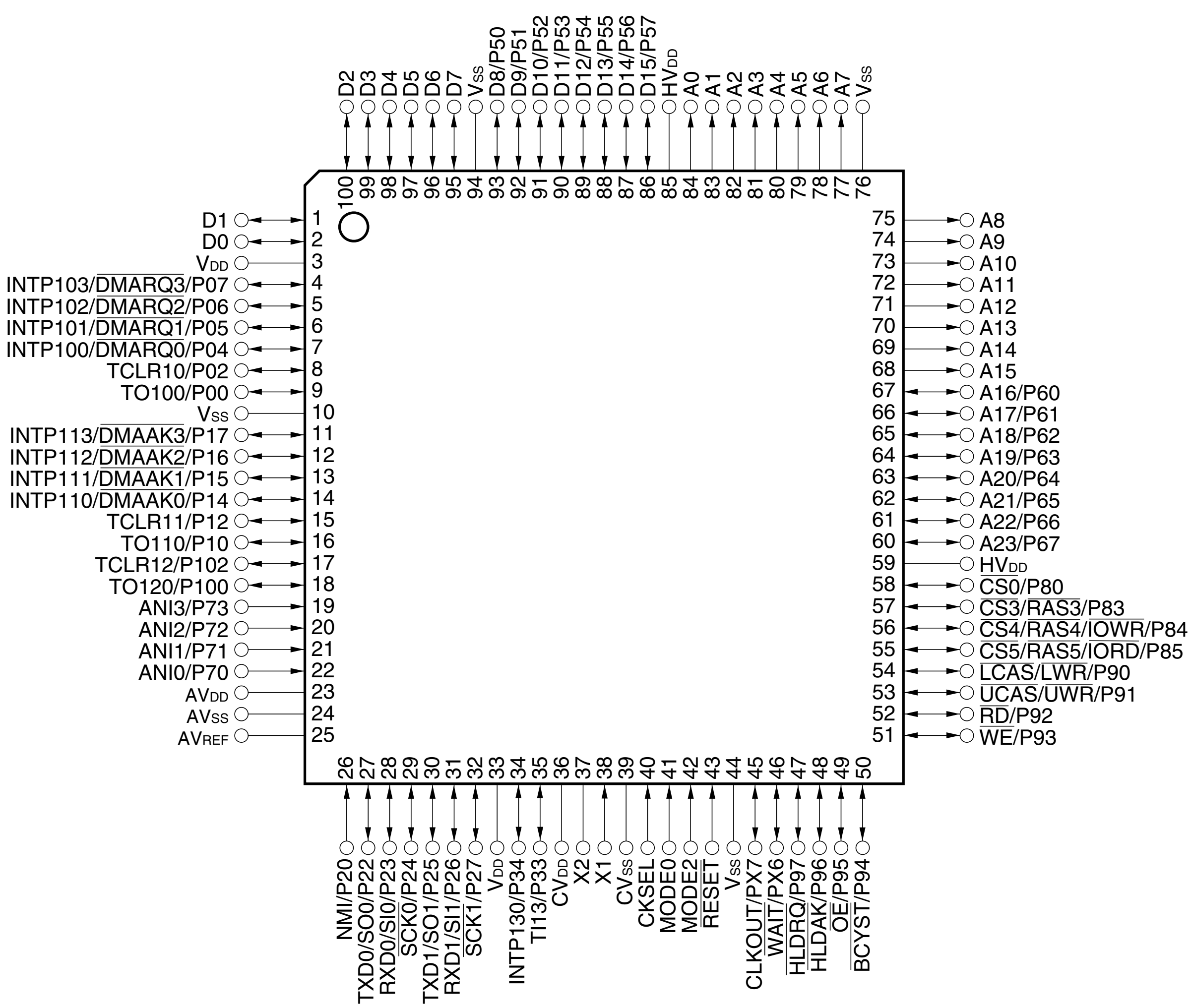
Part Number	Package	Maximum Operating Frequency	Internal ROM
μPD703130GC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	33 MHz	None
★ μPD703130GC-8EU-A	100-pin plastic LQFP (fine pitch) (14 × 14)	33 MHz	None

Remark Products with -A at the end of the part number are lead-free products.

PIN CONFIGURATION (TOP VIEW)

100-pin plastic LQFP (fine pitch) (14 × 14)

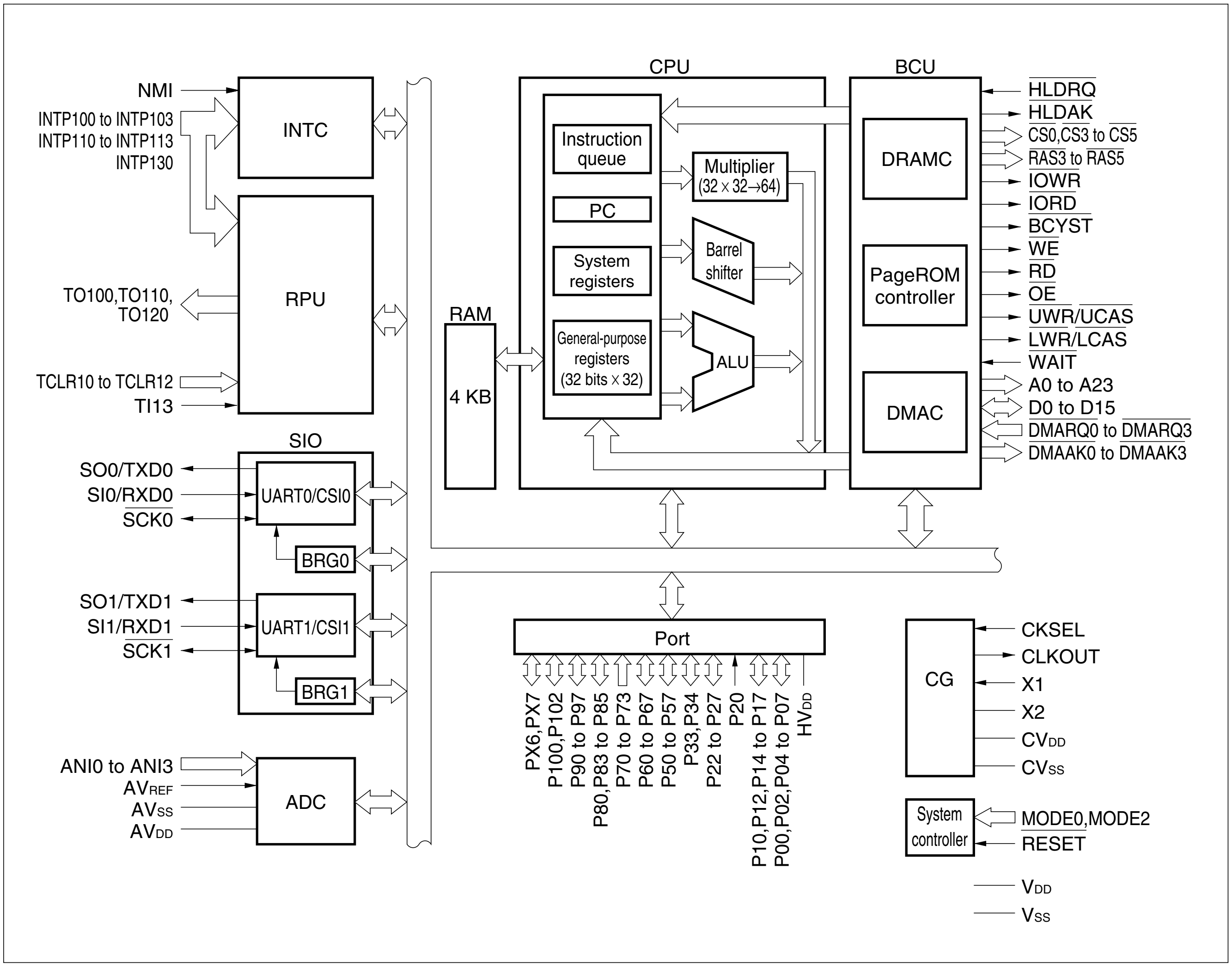
- μPD703130GC-8EU
- ★ μPD703130GC-8EU-A



PIN NAMES

A0 to A23:	Address bus
ANI0 to ANI3:	Analog input
AV_{DD}:	Analog power supply
AV_{REF}:	Analog reference voltage
AV_{SS}:	Analog ground
$\overline{BCYST}$:	Bus cycle start timing
CKSEL:	Clock generator operating mode select
CLKOUT:	Clock output
$\overline{CS0}$, $\overline{CS3}$ to $\overline{CS5}$:	Chip select
CV_{DD}:	Clock generator power supply
CV_{SS}:	Clock generator ground
D0 to D15:	Data bus
$\overline{DMAAK0}$ to $\overline{DMAAK3}$:	DMA acknowledge
$\overline{DMARQ0}$ to $\overline{DMARQ3}$:	DMA request
$\overline{HLDAK}$:	Hold acknowledge
$\overline{HLDRQ}$:	Hold request
HV_{DD}:	Power supply for external pins
INTP100 to INTP103, : INTP110 to INTP113, INTP130	Interrupt request from peripherals
$\overline{IORD}$:	I/O read strobe
$\overline{IOWR}$:	I/O write strobe
$\overline{LCAS}$:	Lower column address strobe
$\overline{LWR}$:	Lower write strobe
MODE0, MODE2:	Mode
NMI:	Non-maskable interrupt request
$\overline{OE}$:	Output enable
P00, P02, P04 to P07:	Port 0
P10, P12, P14 to P17:	Port 1
P20, P22 to P27:	Port 2
P33, P34:	Port 3
P50 to P57:	Port 5
P60 to P67:	Port 6
P70 to P73:	Port 7
P80, P83 to P85:	Port 8
P90 to P97:	Port 9
P100, P102:	Port 10
PX6, PX7:	Port X
$\overline{RAS3}$ to $\overline{RAS5}$:	Row address strobe
$\overline{RD}$:	Read
$\overline{RESET}$:	Reset
RXD0, RXD1:	Receive data
$\overline{SCK0}$, $\overline{SCK1}$:	Serial clock
SI0, SI1:	Serial input
SO0, SO1:	Serial output
TCLR10 to TCLR12:	Timer clear
TI13:	Timer input
TO100, TO110: TO120	Timer output
TXD0, TXD1:	Transmit data
$\overline{UCAS}$:	Upper column address strobe
$\overline{UWR}$:	Upper write strobe
V_{DD}:	Power supply for internal unit
V_{SS}:	Ground
$\overline{WAIT}$:	Wait
$\overline{WE}$:	Write enable
X1, X2:	Crystal

INTERNAL BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN V850E/MS2 AND V850E/MS1

Item \ Product Name	V850E/MS2	V850E/MS1	
	μPD703130	μPD703100-33	μPD703102-33
Internal ROM	None	None	128 KB (mask ROM)
Maximum operating frequency	33 MHz	33 MHz	
Memory space	64 MB linear (only 22 MB supports on-chip $\overline{\text{CS}}$ signal)	64 MB linear	
Chip select output	4 spaces	8 spaces	
Interrupt function	External: 10, internal: 35	External: 25, internal: 47	
I/O lines	Input: 5, I/O: 52	Input: 9, I/O: 114	
Timer	16-bit timer/event counter: 4 channels 16-bit timer: 2 channels	16-bit timer/event counter: 6 channels 16-bit timer: 2 channels	
Serial interface	CSI/UART: 2 channels Dedicated baud rate generator: 2 channels	CSI: 2 channels CSI/UART: 2 channels Dedicated baud rate generator: 3 channels	
A/D converter	10-bit resolution × 4 channels	10-bit resolution × 8 channels	
Package	100-pin plastic LQFP (fine-pitch) (14 × 14)	144-pin plastic LQFP (fine-pitch) (20 × 20)	
Other	Noise tolerance and noise radiation will differ due to differences in circuit scale and mask layout.		

2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 6-bit I/O port Input/output can be specified in 1-bit units.	TO100
P02			TCLR10
P04			INTP100/$\overline{\text{DMARQ0}}$
P05			INTP101/$\overline{\text{DMARQ1}}$
P06			INTP102/$\overline{\text{DMARQ2}}$
P07			INTP103/$\overline{\text{DMARQ3}}$
P10	I/O	Port 1 6-bit I/O port Input/output can be specified in 1-bit units.	TO110
P12			TCLR11
P14			INTP110/$\overline{\text{DMAAK0}}$
P15			INTP111/$\overline{\text{DMAAK1}}$
P16			INTP112/$\overline{\text{DMAAK2}}$
P17			INTP113/$\overline{\text{DMAAK3}}$
P20	Input	Port 2 P20 is an input only port. When a valid edge is input, this pin operates as NMI input. Also, bit 0 of the P2 register indicates the NMI input status. P22 to P27 are 6-bit I/O port. Input/output can be specified in 1-bit units.	NMI
P22	I/O		TXD0/SO0
P23			RXD0/SI0
P24			$\overline{\text{SCK0}}$
P25			TXD1/SO1
P26			RXD1/SI1
P27			$\overline{\text{SCK1}}$
P33	I/O	Port 3 2-bit I/O port Input/output can be specified in 1-bit units.	TI13
P34			INTP130
P50 to P57	I/O	Port 5 8-bit I/O port Input/output can be specified in 1-bit units.	D8 to D15
P60 to P67	I/O	Port 6 8-bit I/O port Input/output can be specified in 1-bit units.	A16 to A23
P70 to P73	Input	Port 7 4-bit input only port	ANI0 to ANI3
P80	I/O	Port 8 4-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{CS0}}$
P83			$\overline{\text{CS3}}$/$\overline{\text{RAS3}}$
P84			$\overline{\text{CS4}}$/$\overline{\text{RAS4}}$/$\overline{\text{IOWR}}$
P85			$\overline{\text{CS5}}$/$\overline{\text{RAS5}}$/$\overline{\text{IORD}}$

(2/2)

Pin Name	I/O	Function	Alternate Function
P90	I/O	Port 9 8-bit I/O port Input/output can be specified in 1-bit units.	$\overline{LCAS}$/$\overline{LWR}$
P91			$\overline{UCAS}$/$\overline{UWR}$
P92			$\overline{RD}$
P93			$\overline{WE}$
P94			$\overline{BCYST}$
P95			$\overline{OE}$
P96			$\overline{HLDAK}$
P97			$\overline{HLDRQ}$
P100	I/O	Port 10 2-bit I/O port Input/output can be specified in 1-bit units.	TO120
P102			TCLR12
PX6	I/O	Port X 2-bit I/O port Input/output can be specified in 1-bit units.	$\overline{WAIT}$
PX7			CLKOUT

2.2 Non-Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
TO100	Output	Pulse signal output for timers 10 to 12	P00
TO110			P10
TO120			P100
TCLR10	Input	External clear signal input for timers 10 to 12	P02
TCLR11			P12
TCLR12			P102
TI13	Input	External count clock input for timer 13	P33
INTP100	Input	External maskable interrupt request input, shared as external capture trigger input for timer 10	P04/$\overline{\text{DMARQ0}}$
INTP101			P05/$\overline{\text{DMARQ1}}$
INTP102			P06/$\overline{\text{DMARQ2}}$
INTP103			P07/$\overline{\text{DMARQ3}}$
INTP110	Input	External maskable interrupt request input, shared as external capture trigger input for timer 11	P14/$\overline{\text{DMAAK0}}$
INTP111			P15/$\overline{\text{DMAAK1}}$
INTP112			P16/$\overline{\text{DMAAK2}}$
INTP113			P17/$\overline{\text{DMAAK3}}$
INTP130	Input	External maskable interrupt request input, shared as external capture trigger input for timer 13	P34
SO0	Output	Serial transmit data output (3-wire) for CSI0 and CSI1	P22/TXD0
SO1			P25/TXD1
SI0	Input	Serial receive data input (3-wire) for CSI0 and CSI1	P23/RXD0
SI1			P26/RXD1
$\overline{\text{SCK0}}$	I/O	Serial clock I/O (3-wire) for CSI0 and CSI1	P24
$\overline{\text{SCK1}}$			P27
TXD0	Output	Serial transmit data output for UART0 and UART1	P22/SO0
TXD1			P25/SO1
RXD0	Input	Serial receive data input for UART0 and UART1	P23/SI0
RXD1			P26/SI1
D0 to D7	I/O	16-bit data bus for external memory	–
D8 to D15			P50 to P57
A0 to A15	Output	24-bit address bus for external memory	–
A16 to A23			P60 to P67
$\overline{\text{LWR}}$	Output	Lower byte write-enable signal output for external data bus	P90/$\overline{\text{LCAS}}$
$\overline{\text{UWR}}$	Output	Higher byte write-enable signal output for external data bus	P91/$\overline{\text{UCAS}}$
$\overline{\text{RD}}$	Output	Read strobe signal output for external data bus	P92
$\overline{\text{WE}}$	Output	Write enable signal output for DRAM	P93
$\overline{\text{OE}}$	Output	Output enable signal output for DRAM	P95

(2/2)

Pin Name	I/O	Function	Alternate Function
$\overline{LCAS}$	Output	Column address strobe signal output for DRAM's lower data	P90/$\overline{LWR}$
$\overline{UCAS}$	Output	Column address strobe signal output for DRAM's higher data	P91/$\overline{UWR}$
$\overline{RAS3}$	Output	Row address strobe signal output for DRAM	P83/$\overline{CS3}$
$\overline{RAS4}$			P84/$\overline{CS4}$/$\overline{IOWR}$
$\overline{RAS5}$			P85/$\overline{CS5}$/$\overline{IORD}$
$\overline{BCYST}$	Output	Strobe signal output indicating start of bus cycle	P94
$\overline{CS0}$	Output	Chip select signal output	P80
$\overline{CS3}$			P83/$\overline{RAS3}$
$\overline{CS4}$			P84/$\overline{RAS4}$/$\overline{IOWR}$
$\overline{CS5}$			P85/$\overline{RAS5}$/$\overline{IORD}$
$\overline{WAIT}$	Input	Control signal input for inserting waits in bus cycle	PX6
$\overline{IOWR}$	Output	DMA write strobe signal output	P84/$\overline{RAS4}$/$\overline{CS4}$
$\overline{IORD}$	Output	DMA read strobe signal output	P85/$\overline{RAS5}$/$\overline{CS5}$
$\overline{DMARQ0}$ to $\overline{DMARQ3}$	Input	DMA request signal input	P04/INTP100 to P07/INTP103
$\overline{DMAAK0}$ to $\overline{DMAAK3}$	Output	DMA acknowledge signal output	P14/INTP110 to P17/INTP113
$\overline{HLDAK}$	Output	Bus hold acknowledge output	P96
$\overline{HLDRQ}$	Input	Bus hold request input	P97
ANI0 to ANI3	Input	Analog input to A/D converter	P70 to P73
NMI	Input	Non-maskable interrupt request input	P20
CLKOUT	Output	System clock output	PX7
CKSEL	Input	Input for specifying clock generator's operation mode	–
MODE0, MODE2	Input	Specify operation modes	–
$\overline{RESET}$	Input	System reset input	–
X1	Input	Connecting resonator for system clock. Input is via X1 when using an external clock.	–
X2	–		–
AV_{REF}	Input	Reference voltage input for A/D converter	–
AV_{DD}	–	Positive power supply for A/D converter	–
AV_{SS}	–	Ground potential for A/D converter	–
CV_{DD}	–	Positive power supply for dedicated clock generator	–
CV_{SS}	–	Ground potential for dedicated clock generator	–
V_{DD}	–	Positive power supply (power supply for internal units)	–
HV_{DD}	–	Positive power supply (power supply for external pins)	–
V_{SS}	–	Ground potential	–

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-1 shows the I/O circuit type of each pin and recommended connection of unused pins. Figure 2-1 shows the various circuit types using partially abridged diagrams.

When connecting to V_{DD} or V_{SS} via a resistor, a resistance value in the range of 1 to 10 kΩ is recommended.

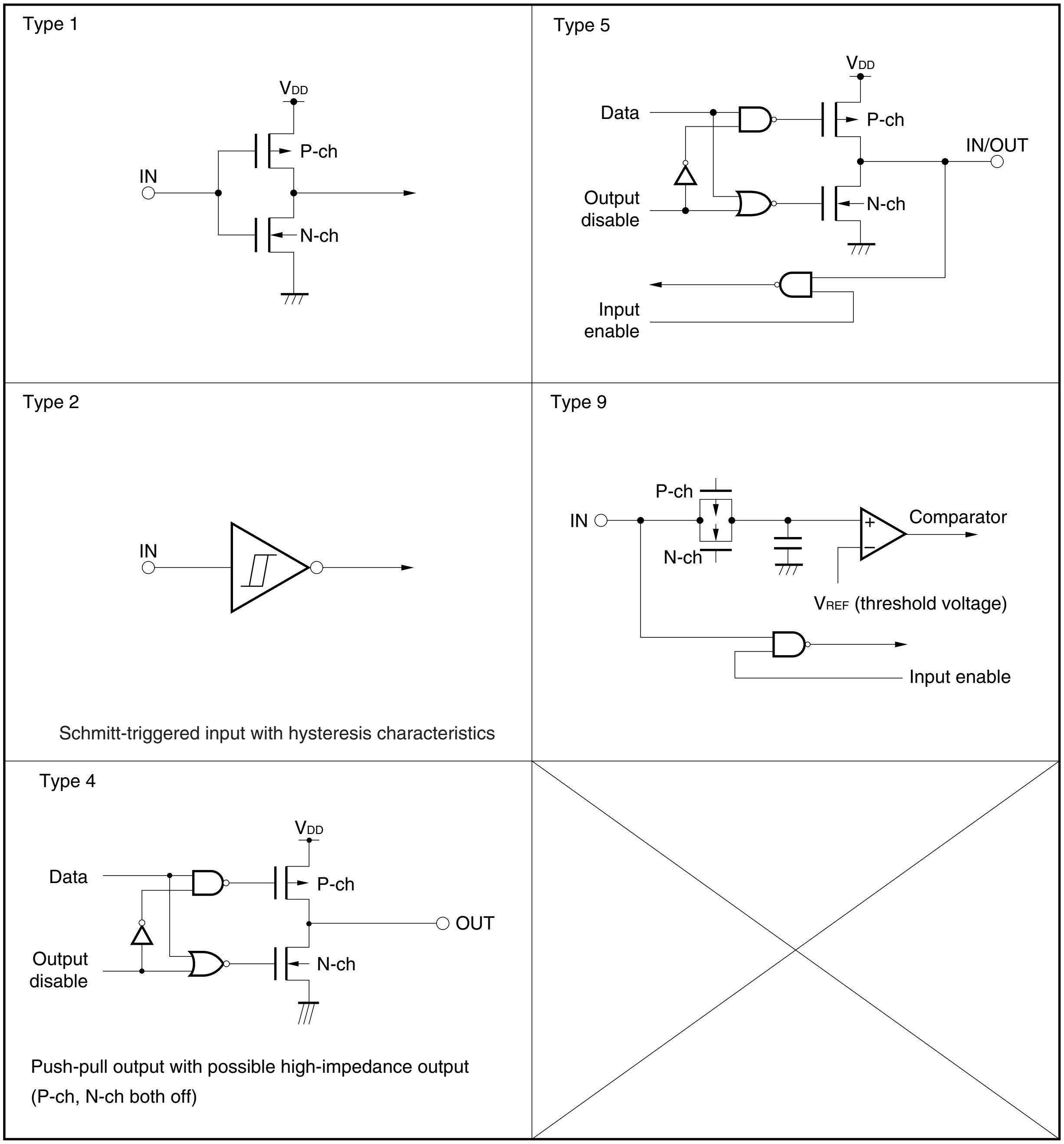
Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (1/2)

Pin	I/O Circuit Type	Recommended Connection of Unused Pins
P00/TO100	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
P02/TCLR10		
P04/INTP100/$\overline{DMARQ0}$ to P07/INTP103/$\overline{DMARQ3}$		
P10/TO110		
P12/TCLR11		
P14/INTP110/$\overline{DMAAK0}$ to P17/INTP113/$\overline{DMAAK3}$		
P20/NMI	2	Connect directly to V_{SS}
P22/TXD0/SO0	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
P23/RXD0/SI0		
P24/$\overline{SCK0}$		
P25/TXD1/SO1		
P26/RXD1/SI1		
P27/$\overline{SCK1}$		
P33/TI13		
P34/INTP130		
P50/D8 to P57/D15		
P60/A16 to P67/A23		
P70/ANI0 to P73/ANI3	9	Connect directly to V_{SS}
P80/$\overline{CS0}$, to P83/$\overline{CS3}$/$\overline{RAS3}$	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
P84/$\overline{CS4}$/$\overline{RAS4}$/$\overline{IOWR}$, P85/$\overline{CS5}$/$\overline{RAS5}$/$\overline{IORD}$		
P90/$\overline{LCAS}$/$\overline{LWR}$		
P91/$\overline{UCAS}$/$\overline{UWR}$		
P92/$\overline{RD}$		
P93/$\overline{WE}$		
P94/$\overline{BCYST}$		
P95/$\overline{OE}$		
P96/$\overline{HLDAK}$		
P97/$\overline{HLDRQ}$		
P100/TO120		
P102/TCLR12		

Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (2/2)

Pin	I/O Circuit Type	Recommended Connection of Unused Pins
PX6/$\overline{WAIT}$	5	Input: Independently connect to HV_{DD} or V_{SS} via a resistor Output: Leave open
PX7/CLKOUT		
A0 to A15	4	–
D0 to D7	5	
CKSEL	1	
$\overline{RESET}$	2	
MODE0, MODE2		
AV_{REF}, AV_{SS}	–	Connect directly to V_{SS}
AV_{DD}	–	Connect directly to HV_{DD}

Figure 2-1. Pin I/O Circuits



Caution Replace V_{DD} by HV_{DD} when referencing the circuit diagrams shown above.

3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition		Rating	Unit
Power supply voltage	V_{DD}	V_{DD} pin		–0.5 to +4.6	V
	HV_{DD}	HV_{DD} pin, $HV_{DD} \geq V_{DD}$		–0.5 to +7.0	V
	CV_{DD}	CV_{DD} pin		–0.5 to +4.6	V
	CV_{SS}	CV_{SS} pin		–0.5 to +0.5	V
	AV_{DD}	AV_{DD} pin		–0.5 to HV_{DD} + 0.5 Note	V
	AV_{SS}	AV_{SS} pin		–0.5 to +0.5	V
Input voltage	V_I	Except X1 pin		–0.5 to HV_{DD} + 0.5 Note	V
Clock input voltage	V_K	X1, V_{DD} = 3.0 to 3.6 V		–0.5 to V_{DD} + 1.0 Note	V
Output current, low	I_{OL}	1 pin		4.0	mA
		Total of all pins		100	mA
Output current, high	I_{OH}	1 pin		–4.0	mA
		Total of all pins		–100	mA
Output voltage	V_O	HV_{DD} = 5.0 V ±10%		–0.5 to HV_{DD} + 0.5 Note	V
Analog input voltage	V_{IAN}	P70/ANI0 to P73 pins	$AV_{DD} > HV_{DD}$	–0.5 to HV_{DD} + 0.5 Note	V
			$HV_{DD} \geq AV_{DD}$	–0.5 to AV_{DD} + 0.5 Note	V
A/D converter reference input voltage	AV_{REF}	$AV_{DD} > HV_{DD}$		–0.5 to HV_{DD} + 0.5 Note	V
		$HV_{DD} \geq AV_{DD}$		–0.5 to AV_{DD} + 0.5 Note	V
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–60 to +150	°C

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of the each power supply voltage.

Cautions 1. Do not make direct connections of the output (or input/output) pins of the IC product with each other, and also avoid direct connections to V_{DD}, V_{CC}, or GND. However, the open drain pins or the open collector pins can be directly connected to each other. A direct connection can also be made for an external circuit designed with timing specifications that prevent conflicting output from pins subject to a high-impedance state.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

Capacitance (T_A = 25°C, V_{DD} = HV_{DD} = CV_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_c = 1 MHz Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (f_X)	Operating Ambient Temperature (T_A)	Power Supply Voltage (V_{DD}, HV_{DD})
Direct mode	10 to 33 MHz[Note 1]	–40 to +85°C	V_{DD} = 3.0 to 3.6 V, HV_{DD} = 5.0 V ±10%
PLL mode[Note 2]	20 to 33 MHz[Note 3]	–40 to +85°C	

Notes 1. Set the input clock frequency used in direct mode to 20 to 66 MHz.

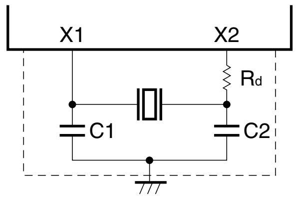
2. The internal operating clock frequency in PLL mode is the value for 5× operation. When used for 1× or 1/2× operation as set by the CKDIVn (n = 0, 1) bit of the CKC register, operation at a frequency of 20 MHz or less is possible.

3. Set the input clock frequency used in PLL mode to 4.0 to 6.6 MHz.

Recommended Oscillator

(a) Ceramic resonator

(i) Murata Mfg. Co., Ltd. (T_A = −40 to +85°C)

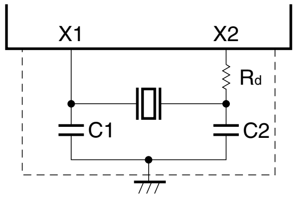


Manu-facturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (kΩ)	MIN. (V)	MAX. (V)	
Murata Mfg.	CSTS400MG06^Note (CSTLS4M00G56-B0)	4.0	On-chip	On-chip	0	3.0	3.6	0.6
	CSTCR4M00G55-R0	4.0	On-chip	On-chip	0	3.0	3.6	0.6
	CSTS0500MG06^Note (CSTLS5M00G56-B0)	5.0	On-chip	On-chip	0	3.0	3.6	0.6
	CSTCR5M00G55-R0	5.0	On-chip	On-chip	0	3.0	3.6	0.6
	CSTS066MG06^Note (CSTLS6M60G56-B0)	6.6	On-chip	On-chip	0	3.0	3.6	0.6
	CSTCR6M60G55-R0	6.6	On-chip	On-chip	0	3.0	3.6	0.6

Note The part number will be changed to the part number in the parentheses from June 2001.

Cautions 1. Connect the oscillator as close to the X1 and X2 pins as possible.
2. Do not wire any other signal lines in the area enclosed by broken lines.
3. Sufficiently evaluate the matching between the μPD703130 and the resonator.

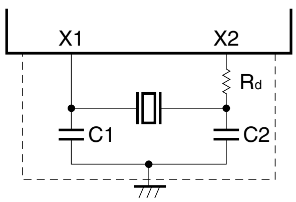
(ii) TDK (T_A = –40 to +85°C)



Manu-facturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (kΩ)	MIN. (V)	MAX. (V)	
TDK	FCR4.0MC5	4.0	On-chip	On-chip	0	3.0	3.6	0.73
	FCR5.0MC5	5.0	On-chip	On-chip	0	3.0	3.6	0.68
	FCR6.0MC5	6.0	On-chip	On-chip	0	3.0	3.6	0.58

Cautions 1. Connect the oscillator as closely to the X1 and X2 pins as possible.
2. Do not wire any other signal lines in the area enclosed by broken lines.
3. Sufficiently evaluate the matching between the μPD703130 and the resonator.

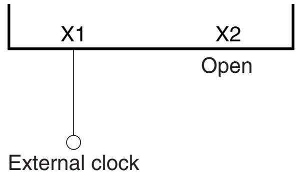
(iii) Kyocera Corporation (T_A = –20 to +80°C)



Type	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (kΩ)	MIN. (V)	MAX. (V)	
Lead	KBR-4.0MKC	4.0	On-chip	On-chip	0	3.0	3.6	0.80
	KBR-5.0MKC	5.0	On-chip	On-chip	0	3.0	3.6	0.70
	KBR-6.0MKC	6.0	On-chip	On-chip	0	3.0	3.6	0.76
SMD	PBRC4.00HR	4.0	On-chip	On-chip	0	3.0	3.6	0.80
	PBRC5.00HR	5.0	On-chip	On-chip	0	3.0	3.6	0.70
	PBRC6.00HR	6.0	On-chip	On-chip	0	3.0	3.6	0.76

Cautions 1. Connect the oscillator as close to the X1 and X2 pins as possible.
2. Do not wire any other signal lines in the area enclosed by broken lines.
3. Sufficiently evaluate the matching between the μPD703130 and the resonator.

(b) External clock input (T$_A$ = –40 to +85°C)



Caution Input CMOS-level voltage to the X1 pin.

DC Characteristics (T$_A$ = –40 to +85°C, V$_{DD}$ = CV$_{DD}$ = 3.0 to 3.6 V, HV$_{DD}$ = 5.0 ±10%, V$_{SS}$ = 0 V)

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input voltage, high		V_{IH}	Except **Note 1**		2.2		HV_{DD} + 0.3	V
			Note 1		$0.8HV_{DD}$		HV_{DD} + 0.3	V
Input voltage, low		V_{IL}	Except **Note 1** and **Note 2**		–0.5		+0.8	V
			Note 1		–0.5		$0.2HV_{DD}$	V
Clock input voltage, high		V_{XH}	X1 pin		$0.8V_{DD}$		V_{DD} + 0.3	V
Clock input voltage, low		V_{XL}	X1 pin		–0.3		$0.15V_{DD}$	V
Schmitt-triggered input threshold voltage		HV_T^+	**Note 1**, rising edge			3.0		V
		HV_T^-	**Note 1**, falling edge			2.0		V
Output voltage, high		V_{OH}	I_{OH} = –2.5 mA		$0.7HV_{DD}$			V
			I_{OH} = –100 μA		HV_{DD} – 0.4			V
Output voltage, low		V_{OL}	I_{OL} = 2.5 mA				0.45	V
Input leakage current, high		I_{LIH}	V_I = HV_{DD}, except **Note 2**				10	μA
Input leakage current, low		I_{LIL}	V_I = 0 V, except **Note 2**				–10	μA
Output leakage current, high		I_{LOH}	V_O = HV_{DD}				10	μA
Output leakage current, low		I_{LOL}	V_O = 0 V				–10	μA
Power supply current	Normal mode	I_{DD1}		V_{DD} + CV_{DD}		2.0 × fx	3.0 × fx	mA
				HV_{DD}		1.5 × fx	2.5 × fx	mA
	HALT mode	I_{DD2}		V_{DD} + CV_{DD}		1.4 × fx	1.8 × fx	mA
				HV_{DD}		0.7 × fx	1.2 × fx	mA
	IDLE mode	I_{DD3}		V_{DD} + CV_{DD}		1.4	2.5	mA
				HV_{DD}		20	100	μA
	STOP mode	I_{DD4}		V_{DD} + CV_{DD}		20	100	μA
				HV_{DD}		10	50	μA

Notes 1. P20/NMI, MODE0, MODE2, CKSEL, $\overline{\text{RESET}}$

2. When the P70/ANI0 to P73/ANI3 pins are used as analog input.

Remarks 1. TYP. values are reference values for when T$_A$ = 25°C, V_{DD} = CV_{DD} = 3.3 V, and HV_{DD} = 5.0 V.

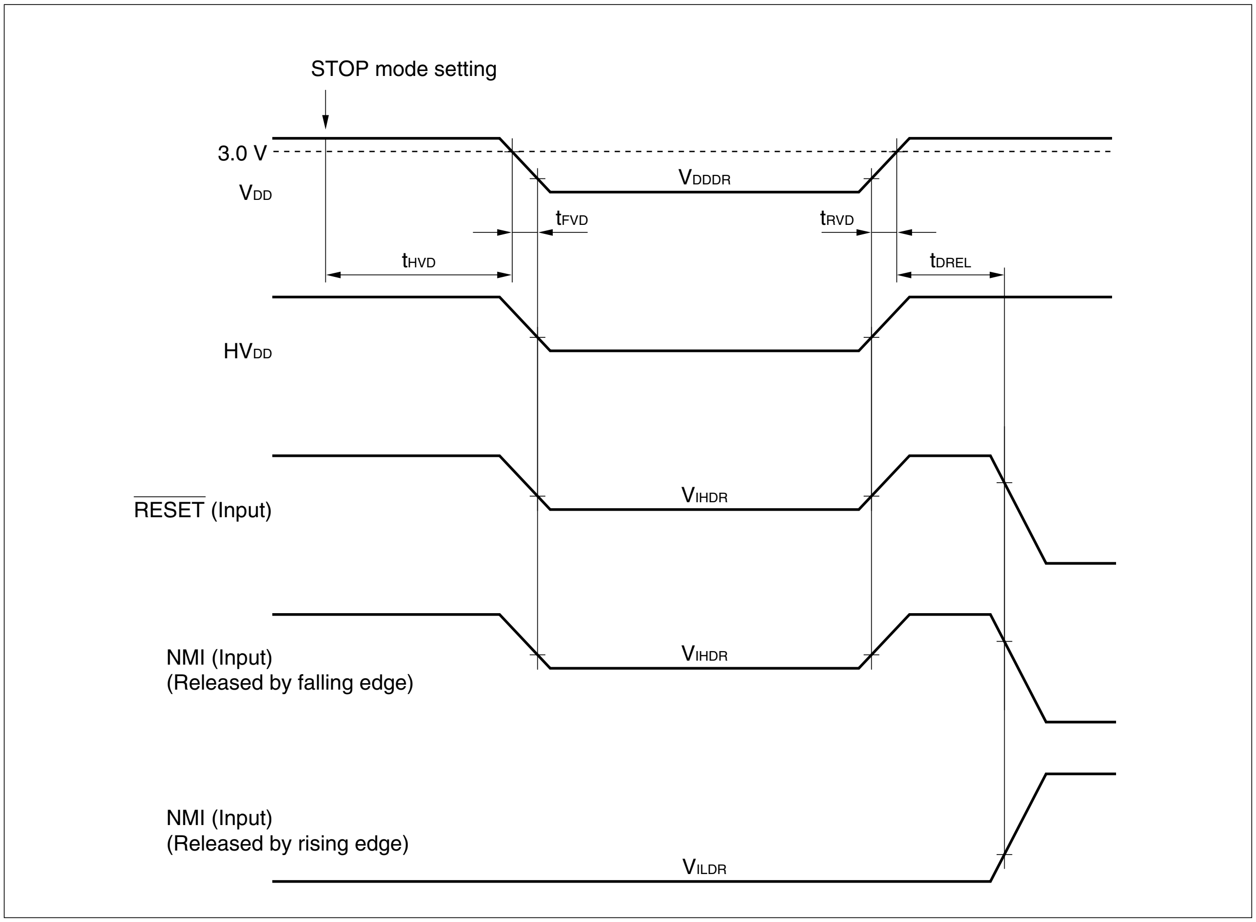
2. Direct mode: f_X = 10 to 33 MHz
PLL mode: f_X = 20 to 33 MHz

3. The unit for f_X is MHz.

Data Hold Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode, $V_{DD} = V_{DDDR}$	1.5		3.6	V
	HV_{DDDR}	STOP mode, $HV_{DD} = HV_{DDDR}$	V_{DDDR}		5.5	V
Data hold current	I_{DDDR}	$V_{DD} = V_{DDDR}$		30	150	μA
Power supply voltage rise time	t_{RVD}		200			μs
Power supply voltage fall time	t_{FVD}		200			μs
Power supply voltage hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP mode release signal input time	t_{DREL}		0			ns
Data hold input voltage, high	V_{IHDR}	P20/NMI, MODE0, MODE2, CKSEL, $\overline{RESET}$	$0.8HV_{DDDR}$		HV_{DDDR}	V
Data hold input voltage, low	V_{ILDR}	P20/NMI, MODE0, MODE2, CKSEL, $\overline{RESET}$	0		$0.2HV_{DDDR}$	V

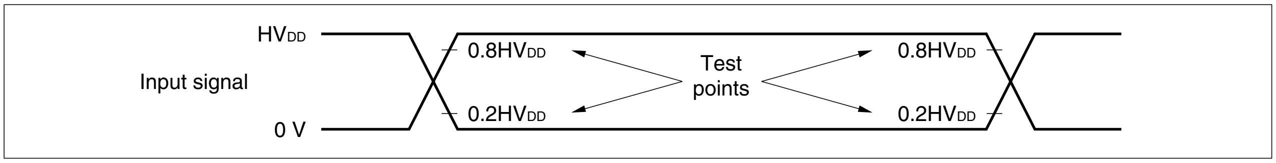
Remark TYP. values are reference values for when T_A = 25°C.



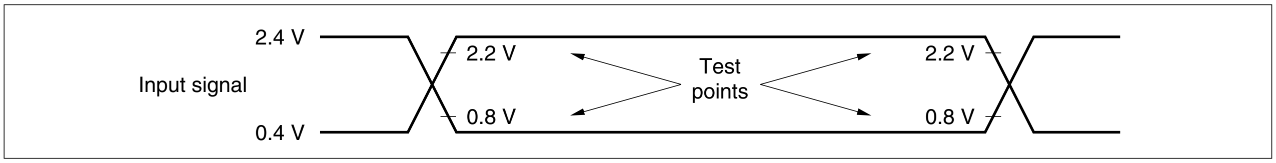
AC Characteristics **(T_A = –40 to +85°C, V_{DD} = CV_{DD} = 3.0 to 3.6 V, HV_{DD} = 5.0 ±10%, V_{SS} = 0 V, output pin load capacitance: C_L = 50 pF)**

AC Test Input Test Points

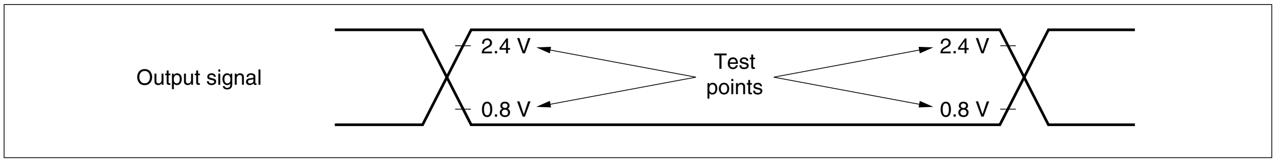
(a) P20/NMI, MODE0, MODE2, CKSEL, $\overline{\text{RESET}}$



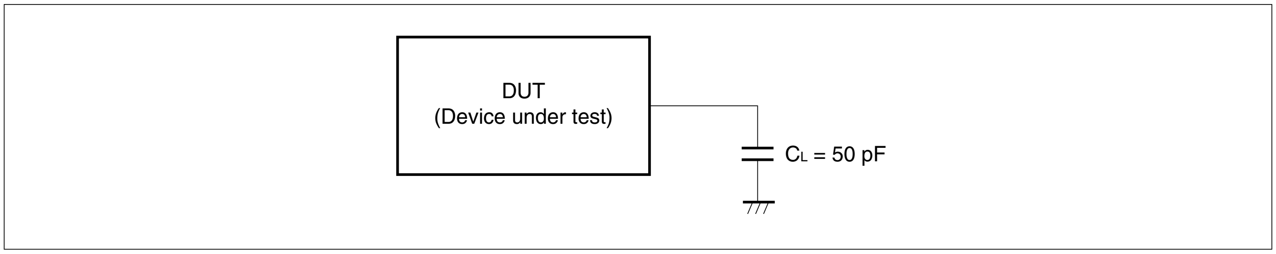
(b) Pins other than those listed in (a) above



AC Test Output Test Points



Load Condition

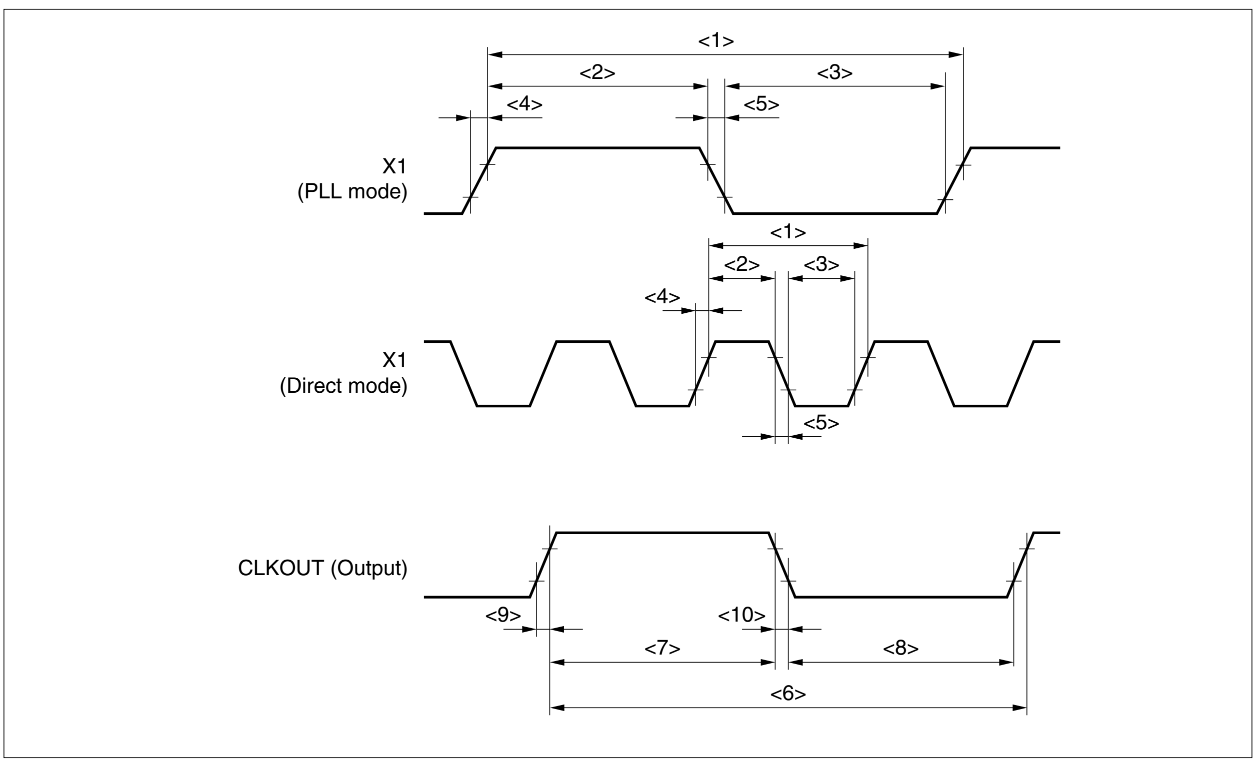


Caution **In cases where the load capacitance is greater than 50 pF due to the circuit configuration, insert a buffer or other element to reduce the device's load capacitance 50 pF.**

(1) Clock timing

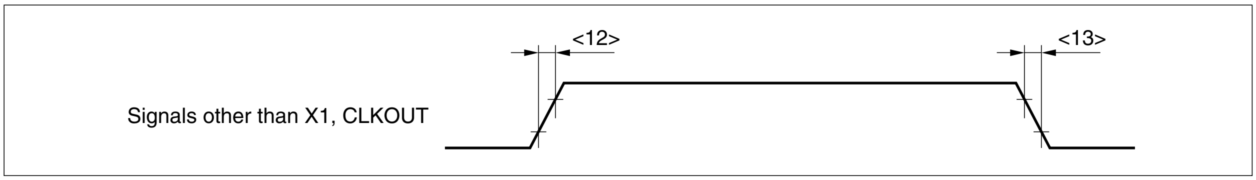
Parameter	Symbol		Condition	MIN.	MAX.	Unit
X1 input cycle	<1>	t_{CYX}	Direct mode	15	50	ns
			PLL mode	150	250	ns
X1 input high-level width	<2>	t_{WXH}	Direct mode	5		ns
			PLL mode	50		ns
X1 input low-level width	<3>	t_{WXL}	Direct mode	5		ns
			PLL mode	50		ns
X1 input rise time	<4>	t_{XR}	Direct mode		4	ns
			PLL mode		10	ns
X1 input fall time	<5>	t_{XF}	Direct mode		4	ns
			PLL mode		10	ns
CLKOUT output cycle	<6>	t_{CYK}		30	100	ns
CLKOUT high-level width	<7>	t_{WKH}		0.5T – 7		ns
CLKOUT low-level width	<8>	t_{WKL}		0.5T – 4		ns
CLKOUT rise time	<9>	t_{KR}			5	ns
CLKOUT fall time	<10>	t_{KF}			5	ns

Remark T = t_{CYK}



(2) Output waveform (other than X1, CLKOUT)

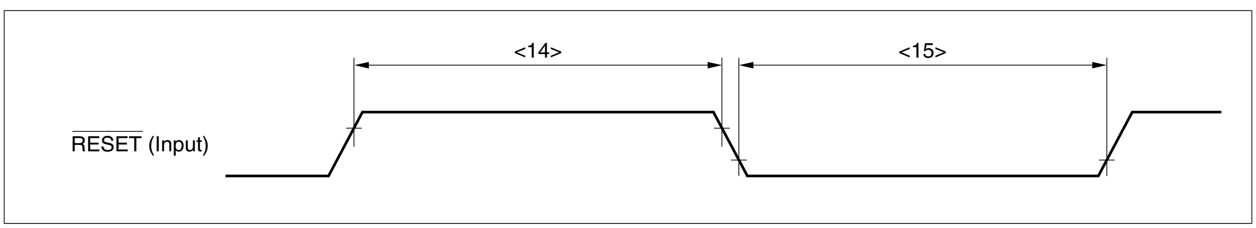
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	<12>	t_{OR}			10	ns
Output fall time	<13>	t_{OF}			10	ns



(3) Reset timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	<14>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ low-level width	<15>	t_{WRSL}	When power supply is on, and STOP mode has been released	500 + T_{OS}		ns
			Other than when power supply is on, and STOP mode has been released	500		ns

Remark T_{OS}: Oscillation stabilization time



(4) SRAM, external ROM, or external I/O access timing

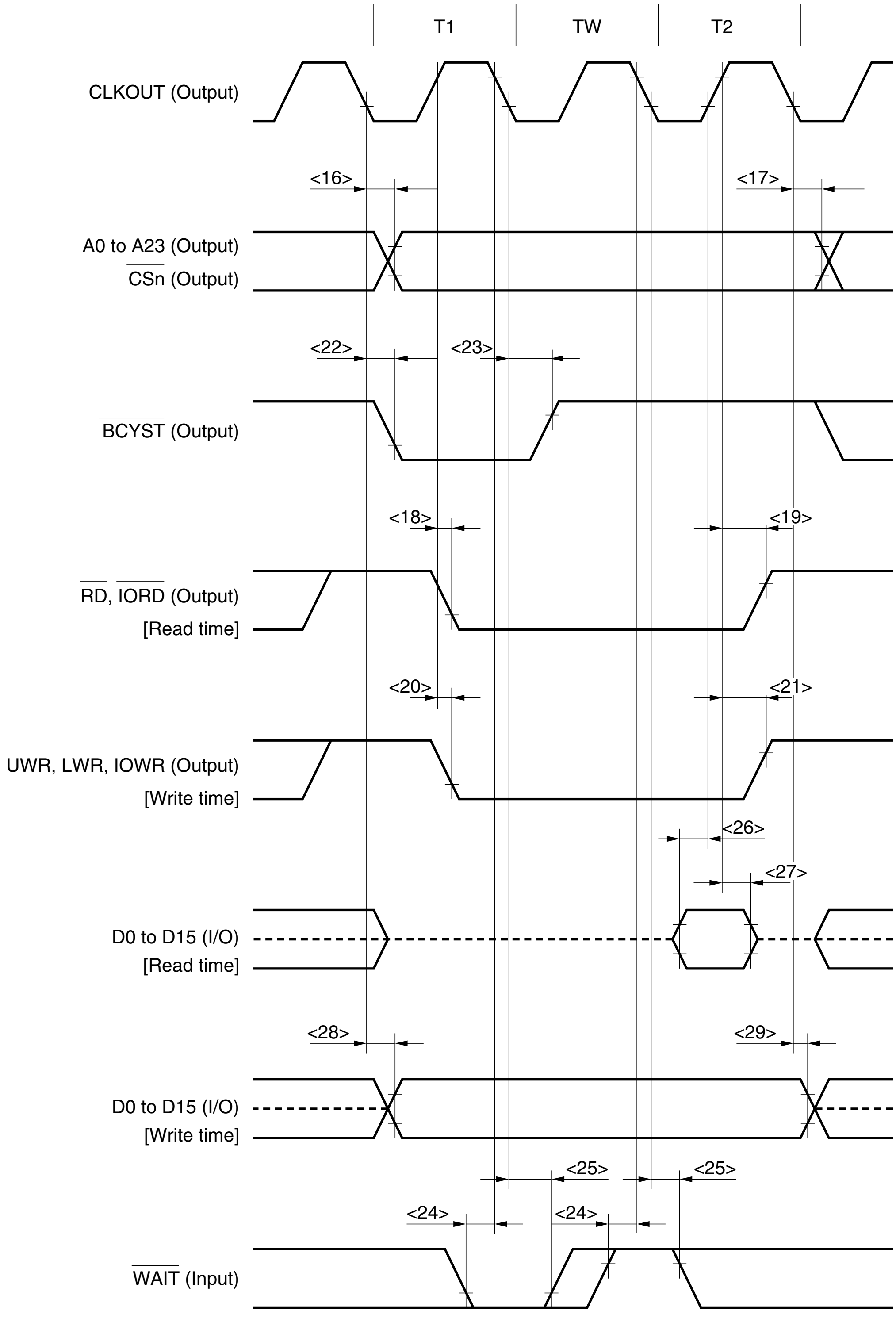
(a) Access timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Address, $\overline{\text{CSn}}$ output delay time (from CLKOUT ↓)	<16>	t_{DKA}		2	10	ns
Address, $\overline{\text{CSn}}$ output hold time (from CLKOUT ↓)	<17>	t_{HKA}		2	10	ns
$\overline{\text{RD}}$, $\overline{\text{IORD}}$ ↓ delay time (from CLKOUT ↑)	<18>	t_{DKRDL}		2	14	ns
$\overline{\text{RD}}$, $\overline{\text{IORD}}$ ↑ delay time (from CLKOUT ↑)	<19>	t_{HKRDH}		2	14	ns
$\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ ↓ delay time (from CLKOUT ↑)	<20>	t_{DKWRL}		2	10	ns
$\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ ↑ delay time (from CLKOUT ↑)	<21>	t_{HKWRH}		2	10	ns
$\overline{\text{BCYST}}$ ↓ delay time (from CLKOUT ↓)	<22>	t_{DKBSL}		2	10	ns
$\overline{\text{BCYST}}$ ↑ delay time (from CLKOUT ↓)	<23>	t_{HKBSH}		2	10	ns
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Data input setup time (to CLKOUT ↑)	<26>	t_{SKID}		18		ns
Data input hold time (from CLKOUT ↑)	<27>	t_{HKID}		2		ns
Data output delay time (from CLKOUT ↓)	<28>	t_{DKOD}		2	10	ns
Data output hold time (from CLKOUT ↓)	<29>	t_{HKOD}		2	10	ns

Remarks 1. Maintain at least one of the data input hold times t_{HKID} and t_{HRDID}.

2. n = 0, 3 to 5

(a) Access timing (SRAM, external ROM, or external I/O) (2/2)



Remarks **1.** This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.

2. The broken lines indicate high impedance.

3. n = 0, 3 to 5

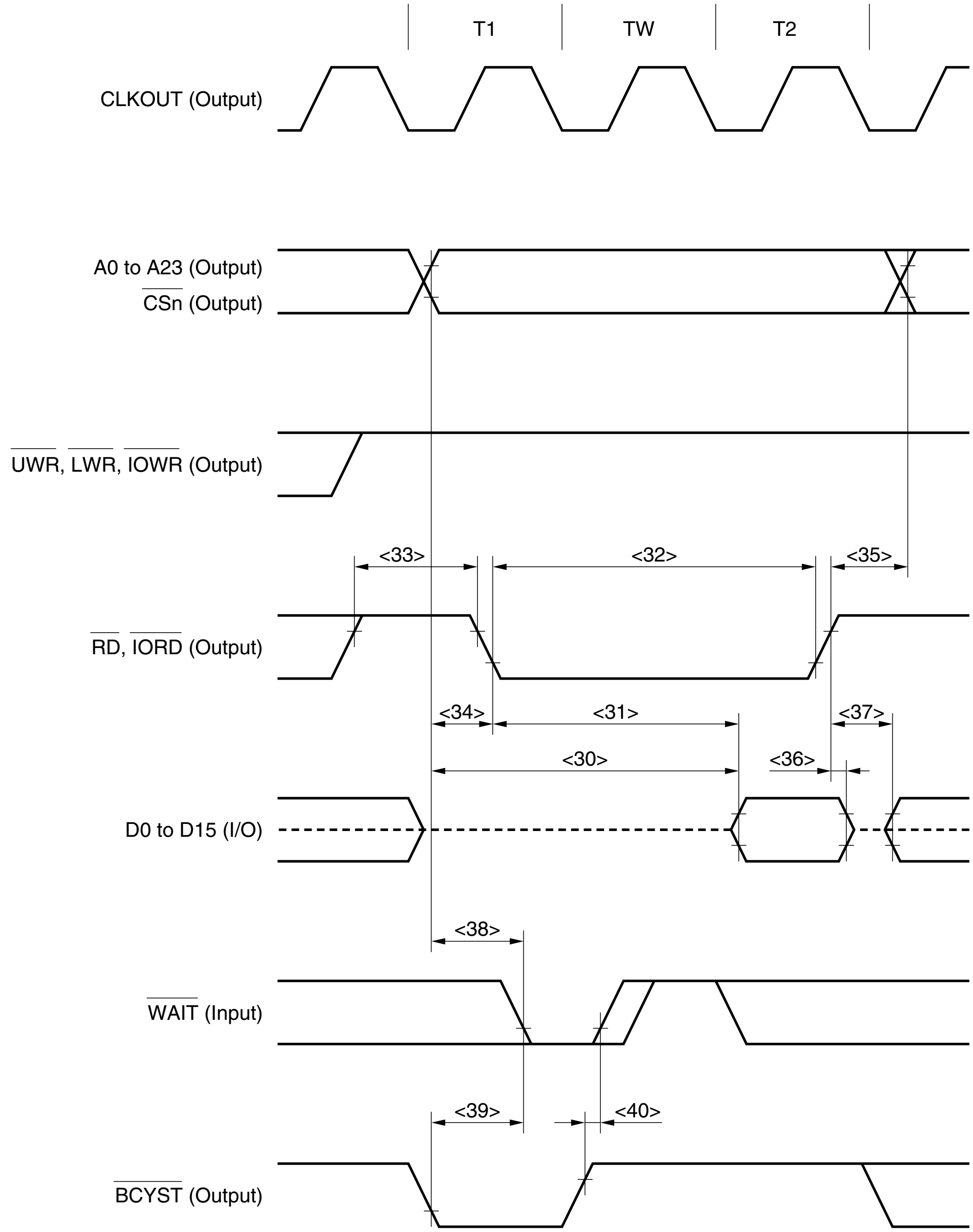
(b) Read timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Data input setup time (to address)	<30>	t_{SAID}			$(1.5 + w_D + w)T - 28$	ns
Data input setup time (to $\overline{RD}$)	<31>	t_{SRDID}			$(1 + w_D + w)T - 32$	ns
$\overline{RD}$, $\overline{IORD}$ low-level width	<32>	t_{WRDL}		$(1 + w_D + w)T - 10$		ns
$\overline{RD}$, $\overline{IORD}$ high-level width	<33>	t_{WRDH}		$T - 10$		ns
Delay time from address, $\overline{CSn}$ to $\overline{RD}$, $\overline{IORD}$ ↓	<34>	t_{DARD}		$0.5T - 10$		ns
Delay time from $\overline{RD}$, $\overline{IORD}$ ↑ to address	<35>	t_{DRDA}		$(0.5 + i)T - 10$		ns
Data input hold time (from $\overline{RD}$, $\overline{IORD}$ ↑)	<36>	t_{HRDID}		0		ns
Delay time from $\overline{RD}$, $\overline{IORD}$ ↑ to data output	<37>	t_{DRDOD}		$(0.5 + i)T - 10$		ns
$\overline{WAIT}$ setup time (to address)	<38>	t_{SAW}	**Note**		$T - 25$	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST}$ ↓)	<39>	t_{SBSW}	**Note**		$T - 25$	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}$ ↑)	<40>	t_{HBSW}	**Note**	0		ns

Note For first $\overline{WAIT}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks
1. $T = t_{CYK}$
2. w: The number of waits due to $\overline{WAIT}$.
3. w_D: The number of waits due to the DWC1 and DWC2 registers.
4. i: The number of idle states that are inserted when a write cycle follows a read cycle.
5. Maintain at least one of the data input hold times, t_{HKID} or t_{HRDID}.
6. n = 0, 3 to 5

(b) Read timing (SRAM, external ROM, or external I/O) (2/2)



Remarks **1.** This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.

2. The broken lines indicate high impedance.

3. n = 0, 3 to 5

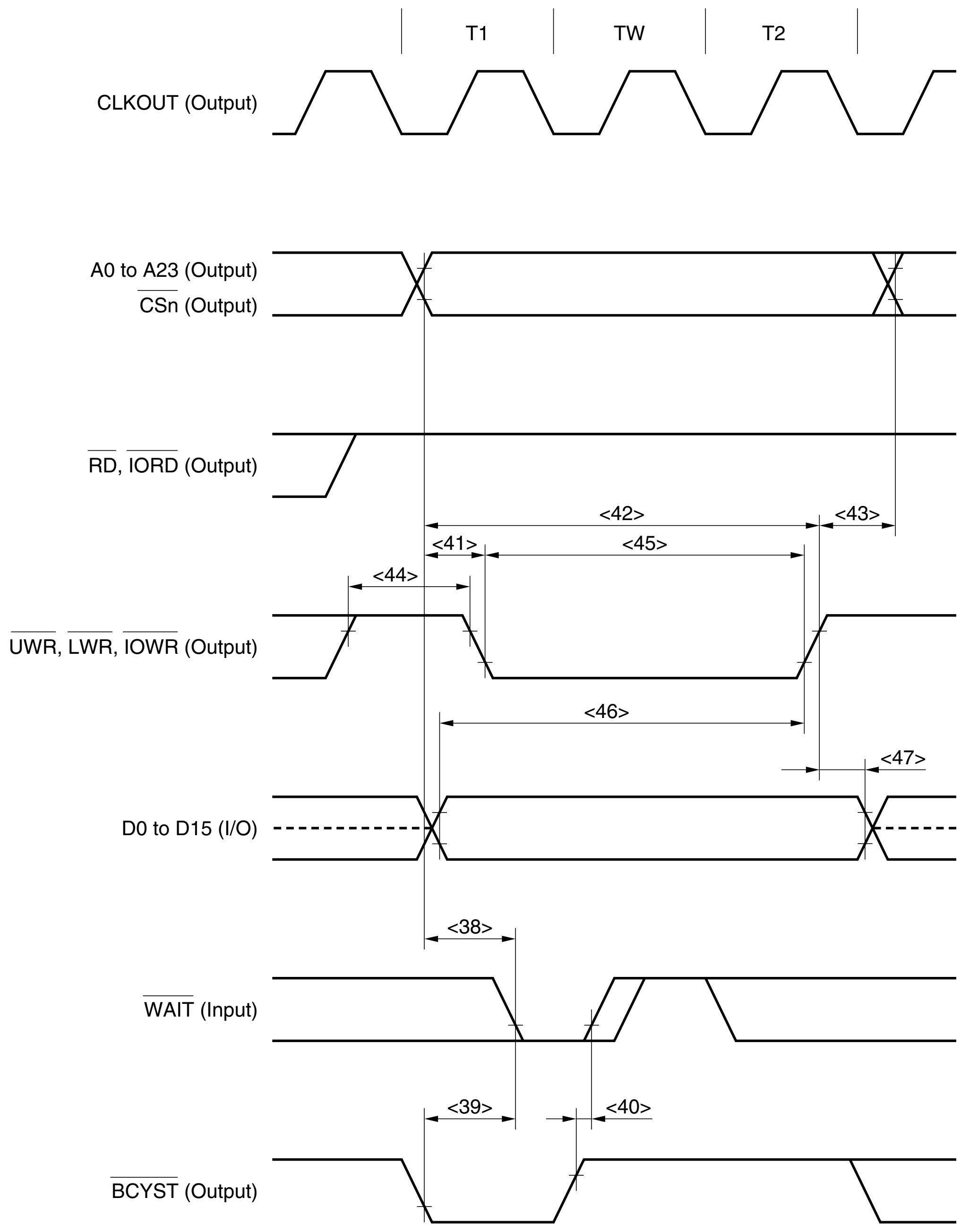
(c) Write timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to address)	<38>	t_{SAW}	**Note**		T – 25	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}}$ ↓)	<39>	t_{SBSW}	**Note**		T – 25	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}$ ↑)	<40>	t_{HBSW}	**Note**	0		ns
Delay time from address, $\overline{\text{CSn}}$ to $\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ ↓	<41>	t_{DAWR}		0.5T – 10		ns
Address setup time (to $\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ ↑)	<42>	t_{SAWR}		(1.5 + w_D + w)T – 10		ns
Delay time from $\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ ↑ to address	<43>	t_{DWRA}		0.5T – 10		ns
$\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ high-level width	<44>	t_{WWRH}		T – 10		ns
$\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ low-level width	<45>	t_{WWRL}		(1 + w_D + w)T – 10		ns
Data output setup time (to $\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ ↑)	<46>	t_{SODWR}		(1.5 + w_D + w)T – 10		ns
Data output hold time (from $\overline{\text{UWR}}$, $\overline{\text{LWR}}$, $\overline{\text{IOWR}}$ ↑)	<47>	t_{HWROD}		0.5T – 10		ns

Note For first $\overline{\text{WAIT}}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks
1. T = t_{CYK}
2. w: The number of waits due to $\overline{\text{WAIT}}$.
3. w_D: The number of waits due to the DWC1 and DWC2 registers.
4. n = 0, 3 to 5

(c) Write timing (SRAM, external ROM, or external I/O) (2/2)



Remarks **1.** This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.

2. The broken lines indicate high impedance.

3. n = 0, 3 to 5

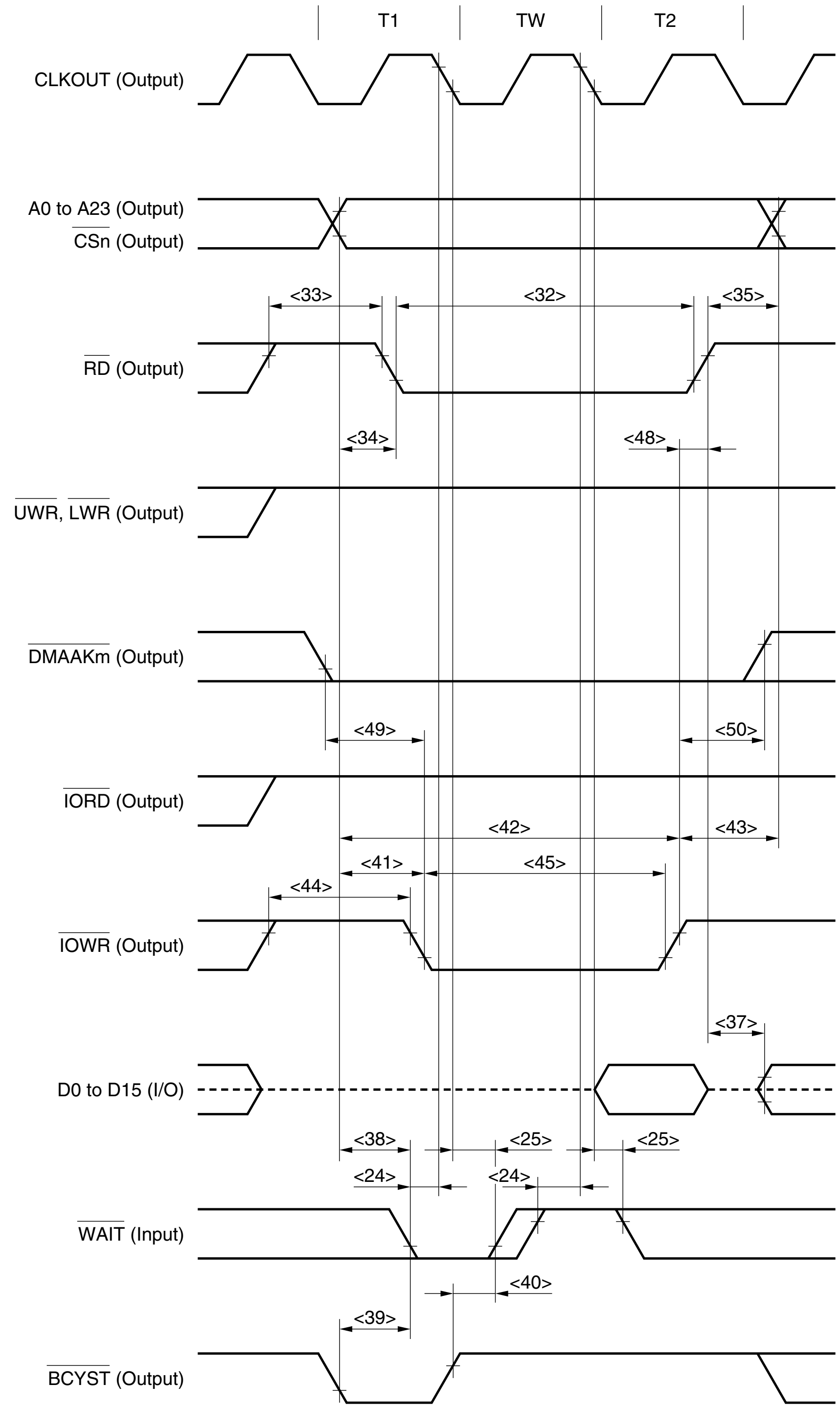
(d) DMA flyby transfer timing (SRAM → external I/O transfer) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
$\overline{\text{RD}}$ low-level width	<32>	t_{WRDL}		$(1 + w_D + w_F + w)T - 10$		ns
$\overline{\text{RD}}$ high-level width	<33>	t_{WRDH}		T – 10		ns
Delay time from address, $\overline{\text{CSn}}$ to $\overline{\text{RD}}$ ↓	<34>	t_{DARD}		0.5T – 10		ns
Delay time from $\overline{\text{RD}}$ ↑ to address	<35>	t_{DRDA}		(0.5 + i)T – 10		ns
Delay time from $\overline{\text{RD}}$ ↑ to data output	<37>	t_{DRDOD}		(0.5 + i)T – 10		ns
$\overline{\text{WAIT}}$ setup time (to address)	<38>	t_{SAW}	**Note**		T – 25	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}}$ ↓)	<39>	t_{SBSW}	**Note**		T – 25	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}$ ↑)	<40>	t_{HBSW}	**Note**	0		ns
Delay time from address to $\overline{\text{IOWR}}$ ↓	<41>	t_{DAWR}		0.5T – 10		ns
Address setup time (to $\overline{\text{IOWR}}$ ↑)	<42>	t_{SAWR}		$(1.5 + w_D + w)T - 10$		ns
Delay time from $\overline{\text{IOWR}}$ ↑ to address	<43>	t_{DWRA}		0.5T – 10		ns
$\overline{\text{IOWR}}$ high-level width	<44>	t_{WWRH}		T – 10		ns
$\overline{\text{IOWR}}$ low-level width	<45>	t_{WWRL}		$(1 + w_D + w)T - 10$		ns
Delay time from $\overline{\text{IOWR}}$ ↑ to $\overline{\text{RD}}$ ↑	<48>	t_{DWRRD}	$w_F = 0$	0		ns
			$w_F = 1$	T – 10		ns
Delay time from $\overline{\text{DMAAKm}}$ ↓ to $\overline{\text{IOWR}}$ ↓	<49>	t_{DDAWR}		0.5T – 10		ns
Delay time from $\overline{\text{IOWR}}$ ↑ to $\overline{\text{DMAAKm}}$ ↑	<50>	t_{DWRDA}		$(0.5 + w_F)T - 10$		ns

Note For first $\overline{\text{WAIT}}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks
1. $T = t_{CYK}$
2. w: The number of waits due to $\overline{\text{WAIT}}$.
3. w_D: The number of waits due to the DWC1 and DWC2 registers.
4. w_F: The number of waits that are inserted for a source-side access during a DMA flyby transfer.
5. i: The number of idle states that are inserted when a write cycle follows a read cycle.
6. n = 0, 3 to 5, m = 0 to 3

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (2/2)



Remarks
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and $w_F = 0$.
2. The broken lines indicate high impedance.
3. n = 0, 3 to 5, m = 0 to 3

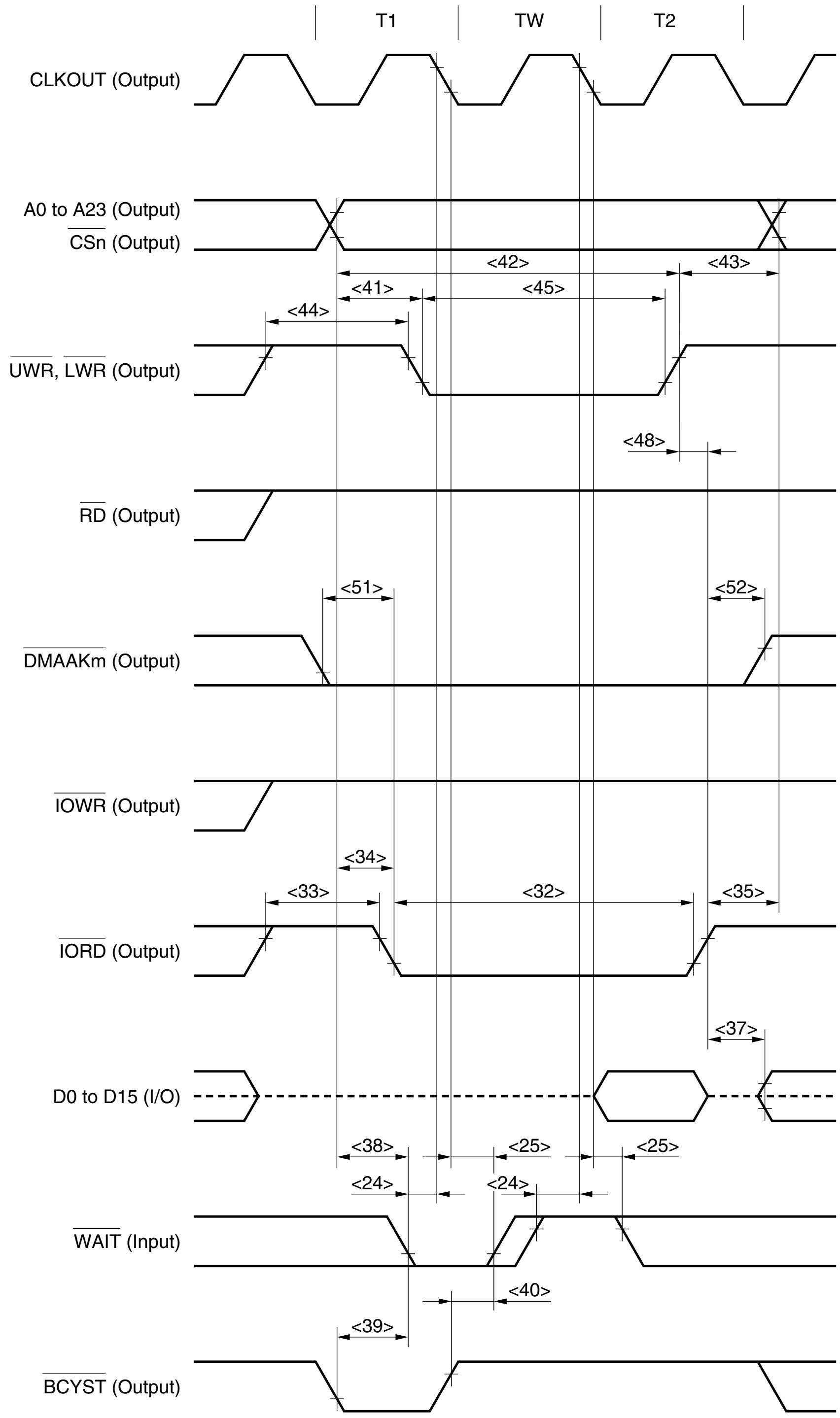
(e) DMA flyby transfer timing (external I/O → SRAM transfer) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
$\overline{\text{IORD}}$ low-level width	<32>	t_{WRDL}		$(1 + w_D + w_F + w)T - 10$		ns
$\overline{\text{IORD}}$ high-level width	<33>	t_{WRDH}		T – 10		ns
Delay time from address, $\overline{\text{CSn}}$ to $\overline{\text{IORD}}$ ↓	<34>	t_{DARD}		0.5T – 10		ns
Delay time from $\overline{\text{IORD}}$ ↑ to address	<35>	t_{DRDA}		(0.5 + i)T – 10		ns
Delay time from $\overline{\text{IORD}}$ ↑ to data output	<37>	t_{DRDOD}		(0.5 + i)T – 10		ns
$\overline{\text{WAIT}}$ setup time (to address)	<38>	t_{SAW}	**Note**		T – 25	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}}$ ↓)	<39>	t_{SBSW}	**Note**		T – 25	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}$ ↑)	<40>	t_{HBSW}	**Note**	0		ns
Delay time from address to $\overline{\text{UWR}}$, $\overline{\text{LWR}}$ ↓	<41>	t_{DAWR}		0.5T – 10		ns
Address setup time (to $\overline{\text{UWR}}$, $\overline{\text{LWR}}$ ↑)	<42>	t_{SAWR}		$(1.5 + w_D + w)T - 10$		ns
Delay time from $\overline{\text{UWR}}$, $\overline{\text{LWR}}$ to address	<43>	t_{DWRA}		0.5T – 10		ns
$\overline{\text{UWR}}$, $\overline{\text{LWR}}$ high-level width	<44>	t_{WWRH}		T – 10		ns
$\overline{\text{UWR}}$, $\overline{\text{LWR}}$ low-level width	<45>	t_{WWRL}		$(1 + w_D + w)T - 10$		ns
Delay time from $\overline{\text{UWR}}$, $\overline{\text{LWR}}$↑ to $\overline{\text{IORD}}$ ↑	<48>	t_{DWRRD}	$w_F = 0$	0		ns
			$w_F = 1$	T – 10		ns
Delay time from $\overline{\text{DMAAKm}}$ ↓ to $\overline{\text{IORD}}$ ↓	<51>	t_{DDARD}		0.5T – 10		ns
Delay time from $\overline{\text{IORD}}$ ↑ to $\overline{\text{DMAAKm}}$ ↑	<52>	t_{DRDDA}		0.5T – 10		ns

Note For first $\overline{\text{WAIT}}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks
1. $T = t_{CYK}$
2. w: The number of waits due to $\overline{\text{WAIT}}$.
3. w_D: The number of waits due to the DWC1 and DWC2 registers.
4. w_F: The number of waits that are inserted for a source-side access during a DMA flyby transfer.
5. i: The number of idle states that are inserted when a write cycle follows a read cycle.
6. n = 0, 3 to 5, m = 0 to 3

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (2/2)



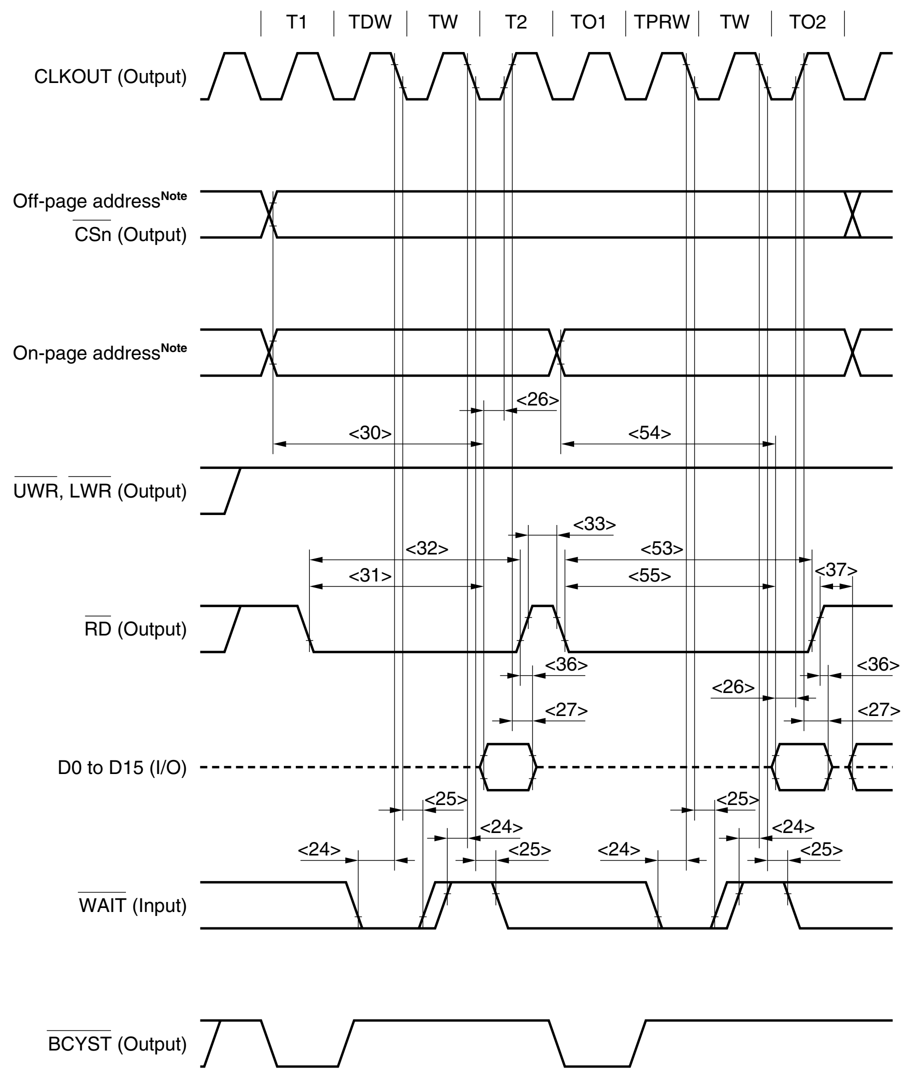
Remarks
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and $w_F = 0$.
2. The broken lines indicate high impedance.
3. n = 0, 3 to 5, m = 0 to 3

(5) Page ROM access timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Data input setup time (to CLKOUT ↑)	<26>	t_{SKID}		18		ns
Data input hold time (from CLKOUT ↑)	<27>	t_{HKID}		2		ns
Off-page data input setup time (to address)	<30>	t_{SAID}			$(1.5 + w_D + w)T - 28$	ns
Off-page data input setup time (to $\overline{RD}$)	<31>	t_{SRDID}			$(1 + w_D + w)T - 32$	ns
Off-page $\overline{RD}$ low-level width	<32>	t_{WRDL}		$(1 + w_D + w)T - 10$		ns
$\overline{RD}$ high-level width	<33>	t_{WRDH}		$0.5T - 10$		ns
Data input hold time (from $\overline{RD}$)	<36>	t_{HRDID}		0		ns
Delay time from $\overline{RD}$ ↑ to data output	<37>	t_{DRDOD}		$(0.5 + i)T - 10$		ns
On-page $\overline{RD}$ low-level width	<53>	t_{WORDL}		$(1.5 + w_{PR} + w)T - 10$		ns
On-page data input setup time (to address)	<54>	t_{SOAID}			$(1.5 + w_{PR} + w)T - 28$	ns
On-page data input setup time (to $\overline{RD}$)	<55>	t_{SORDID}			$(1.5 + w_{PR} + w)T - 32$	ns

Remarks
1. $T = t_{CYK}$
2. w: The number of waits due to $\overline{WAIT}$.
3. w_D: The number of waits due to the DWC1 and DWC2 registers.
4. w_{PR}: The number of waits due to the PRC register.
5. i: The number of idle states that are inserted when a write cycle follows a read cycle.
6. Maintain at least one of the data input hold times, t_{HKID} or t_{HRDID}.

(5) Page ROM access timing (2/2)



Note On-page and off-page addresses are as follows.

PRC Register			On-page Addresses	Off-page Addresses
MA5	MA4	MA3		
0	0	0	A0, A1	A2 to A23
0	0	1	A0 to A2	A3 to A23
0	1	1	A0 to A3	A4 to A23
1	1	1	A0 to A4	A5 to A23

Remarks 1. This is the timing for the following case.
Number of waits due to the DWC1 and DWC2 registers (TDW): 1
Number of waits due to the PRC register (TPRW): 1

2. The broken lines indicate high impedance.

3. n = 0, 3 to 5

(6) DRAM access timing

(a) Read timing (high-speed page DRAM access, normal access: off-page) (1/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Data input setup time (to CLKOUT ↑)	<26>	t_{SKID}		18		ns
Data input hold time (from CLKOUT ↑)	<27>	t_{HKID}		2		ns
Delay time from $\overline{\text{OE}}$ ↑ to data output	<37>	t_{DRDOD}		$(0.5 + i)T - 10$		ns
Row address setup time	<56>	t_{ASR}		$(0.5 + w_{RP})T - 10$		ns
Row address hold time	<57>	t_{RAH}		$(0.5 + w_{RH})T - 10$		ns
Column address setup time	<58>	t_{ASC}		$0.5T - 10$		ns
Column address hold time	<59>	t_{CAH}		$(1.5 + w_{DA} + w)T - 10$		ns
Read/write cycle time	<60>	t_{RC}		$(3 + w_{RP} + w_{RH} + w_{DA} + w)T - 10$		ns
$\overline{\text{RAS}}$ precharge time	<61>	t_{RP}		$(0.5 + w_{RP})T - 10$		ns
$\overline{\text{RAS}}$ pulse time	<62>	t_{RAS}		$(2.5 + w_{RH} + w_{DA} + w)T - 10$		ns
$\overline{\text{RAS}}$ hold time	<63>	t_{RSH}		$(1.5 + w_{DA} + w)T - 10$		ns
Column address read time for $\overline{\text{RAS}}$	<64>	t_{RAL}		$(2 + w_{DA} + w)T - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65>	t_{CAS}		$(1 + w_{DA} + w)T - 10$		ns
$\overline{\text{CAS}}$-$\overline{\text{RAS}}$ precharge time	<66>	t_{CRP}		$(1 + w_{RP})T - 10$		ns
$\overline{\text{CAS}}$ hold time	<67>	t_{CSH}		$(2 + w_{RH} + w_{DA} + w)T - 10$		ns
$\overline{\text{WE}}$ setup time	<68>	t_{RCS}		$(2 + w_{RP} + w_{RH})T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{RAS}}$ ↑)	<69>	t_{RRH}		$0.5T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}$ ↑)	<70>	t_{RCH}		$T - 10$		ns
$\overline{\text{CAS}}$ precharge time	<71>	t_{CPN}		$(2 + w_{RP} + w_{RH})T - 10$		ns
Output enable access time	<72>	t_{OEA}			$(2 + w_{RP} + w_{RH} + w_{DA} + w)T - 28$	ns
$\overline{\text{RAS}}$ access time	<73>	t_{RAC}			$(2 + w_{RH} + w_{DA} + w)T - 28$	ns
Access time from column address	<74>	t_{AA}			$(1.5 + w_{DA} + w)T - 28$	ns
$\overline{\text{CAS}}$ access time	<75>	t_{CAC}			$(1 + w_{DA} + w)T - 28$	ns

Remarks
1. $T = t_{CYK}$
2. w: The number of waits due to $\overline{\text{WAIT}}$.
3. w_{RP}: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. w_{RH}: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
6. i: The number of idle states that are inserted when a write cycle follows a read cycle.

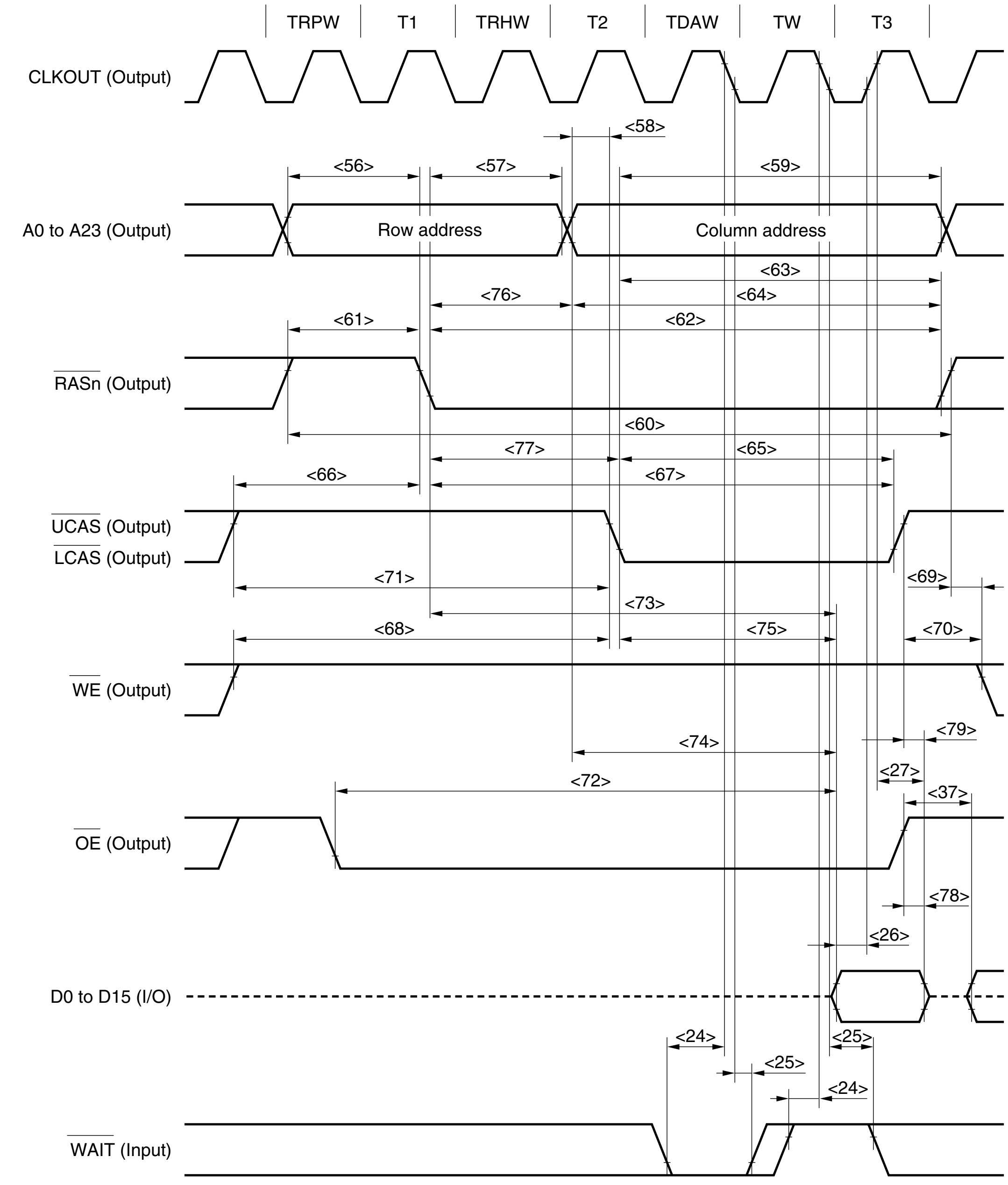
(a) Read timing (high-speed page DRAM access, normal access: off-page) (2/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RAS}}$ column address delay time	<76>	t_{RAD}		$(0.5 + w_{RH})T – 10$		ns
$\overline{\text{RAS}}$-$\overline{\text{CAS}}$ delay time	<77>	t_{RCD}		$(1 + w_{RH})T – 10$		ns
Output buffer turn-off delay time (from $\overline{\text{OE}}$ ↑)	<78>	t_{OEZ}		0		ns
Output buffer turn-off delay time (from $\overline{\text{CAS}}$ ↑)	<79>	t_{OFF}		0		ns

Remarks 1. $T = t_{CYK}$

2. w_{RH}: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(a) Read timing (high-speed page DRAM access, normal access: off-page) (3/3)



Remarks **1.** This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

3. n = 3 to 5

[MEMO]

(b) Read timing (high-speed page DRAM access: on-page) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Data input setup time (to CLKOUT ↑)	<26>	t_{SKID}		18		ns
Data input hold time (from CLKOUT ↑)	<27>	t_{HKID}		2		ns
Delay time from $\overline{\text{OE}}$ ↑ to data output	<37>	t_{DRDOD}		$(0.5 + i)T - 10$		ns
Column address setup time	<58>	t_{ASC}		$(0.5 + w_{CP})T - 10$		ns
Column address hold time	<59>	t_{CAH}		$(1.5 + w_{DA})T - 10$		ns
$\overline{\text{RAS}}$ hold time	<63>	t_{RSH}		$(1.5 + w_{DA})T - 10$		ns
Column address read time for $\overline{\text{RAS}}$	<64>	t_{RAL}		$(2 + w_{CP} + w_{DA})T - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65>	t_{CAS}		$(1 + w_{DA})T - 10$		ns
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}}$ ↓)	<68>	t_{RCS}		$(1 + w_{CP})T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{RAS}}$ ↑)	<69>	t_{RRH}		$0.5T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}$ ↑)	<70>	t_{RCH}		$T - 10$		ns
Output enable access time	<72>	t_{OEA}			$(1 + w_{CP} + w_{DA})T - 28$	ns
Access time from column address	<74>	t_{AA}			$(1.5 + w_{CP} + w_{DA})T - 28$	ns
$\overline{\text{CAS}}$ access time	<75>	t_{CAC}			$(1 + w_{DA})T - 28$	ns
Output buffer turn-off delay time (from $\overline{\text{OE}}$ ↑)	<78>	t_{OEZ}		0		ns
Output buffer turn-off delay time (from $\overline{\text{CAS}}$ ↑)	<79>	t_{OFF}		0		ns
Access time from $\overline{\text{CAS}}$ precharge	<80>	t_{ACP}			$(2 + w_{CP} + w_{DA})T - 28$	ns
$\overline{\text{CAS}}$ precharge time	<81>	t_{CP}		$(1 + w_{CP})T - 10$		ns
High-speed page mode cycle time	<82>	t_{PC}		$(2 + w_{CP} + w_{DA})T - 10$		ns
$\overline{\text{RAS}}$ hold time for $\overline{\text{CAS}}$ precharge	<83>	t_{RHCP}		$(2.5 + w_{CP} + w_{DA})T - 10$		ns

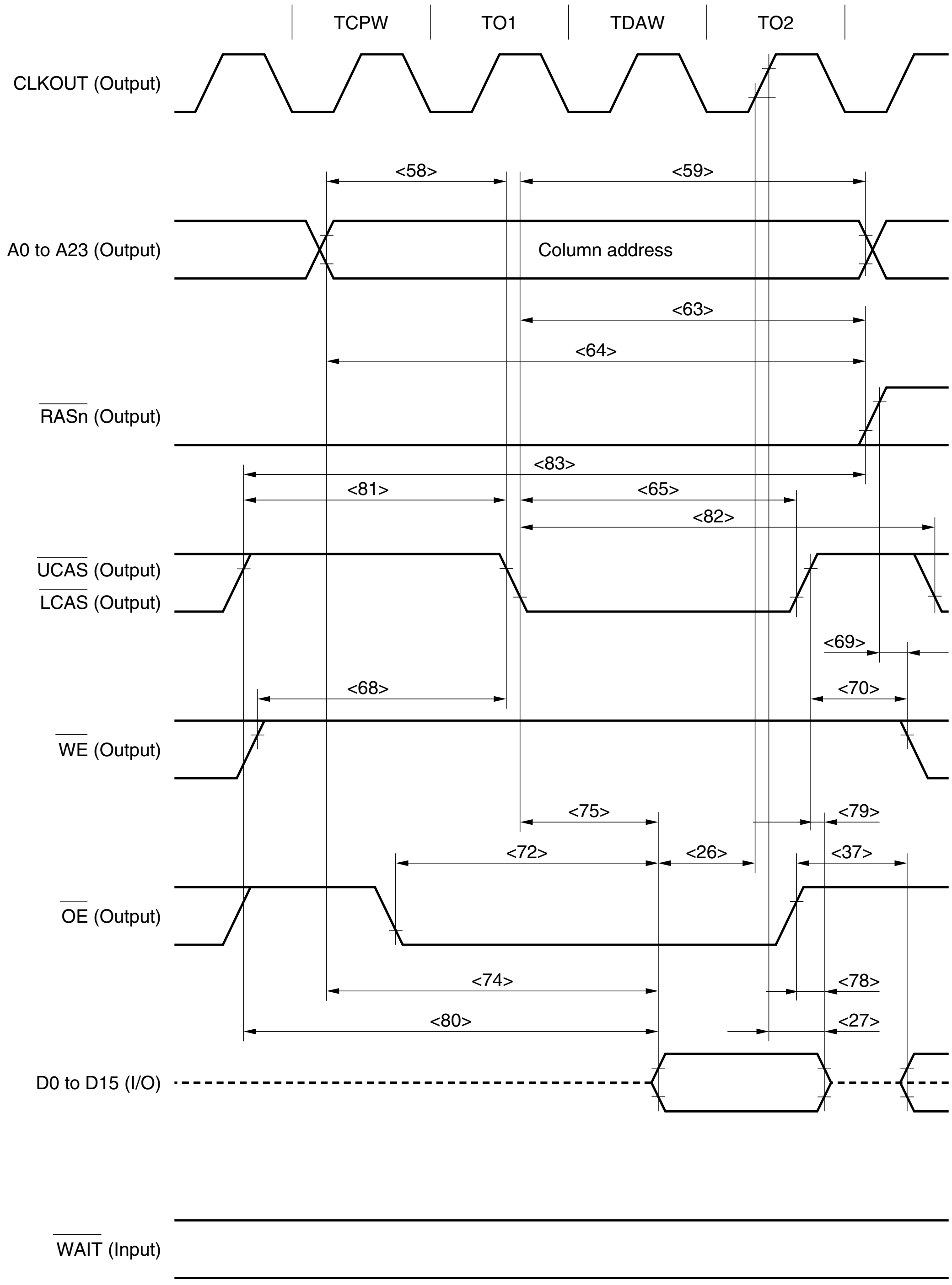
Remarks **1.** $T = t_{CYK}$

2. w_{CP}: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. i: The number of idle states that are inserted when a write cycle follows a read cycle.

(b) Read timing (high-speed page DRAM access: on-page) (2/2)



Remarks **1.** This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

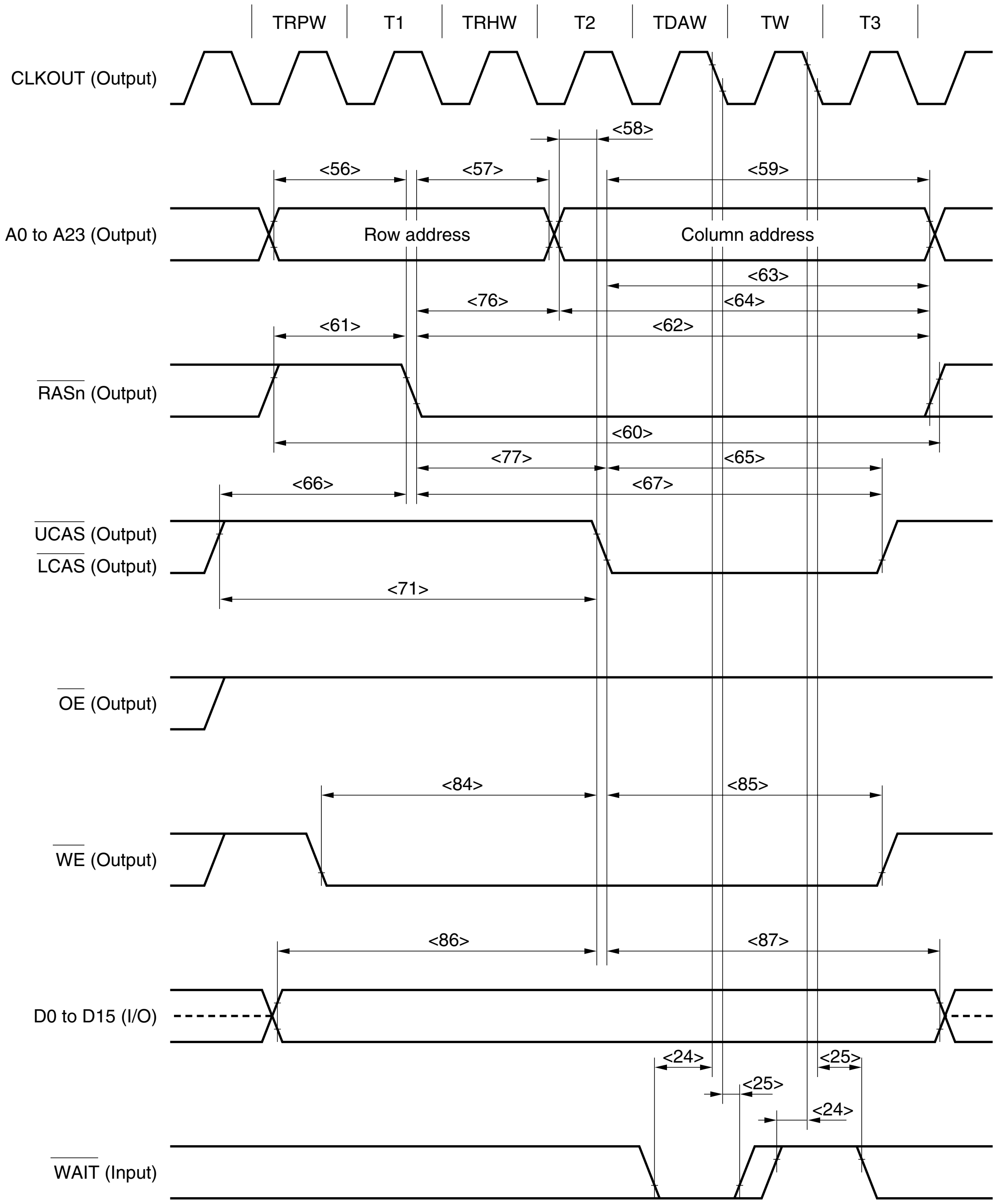
3. n = 3 to 5

(c) Write timing (high-speed page DRAM access, normal access: off-page) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Row address setup time	<56>	t_{ASR}		$(0.5 + w_{RP})T - 10$		ns
Row address hold time	<57>	t_{RAH}		$(0.5 + w_{RH})T - 10$		ns
Column address setup time	<58>	t_{ASC}		$0.5T - 10$		ns
Column address hold time	<59>	t_{CAH}		$(1.5 + w_{DA} + w)T - 10$		ns
Read/write cycle time	<60>	t_{RC}		$(3 + w_{RP} + w_{RH} + w_{DA} + w)T - 10$		ns
$\overline{\text{RAS}}$ precharge time	<61>	t_{RP}		$(0.5 + w_{RP})T - 10$		ns
$\overline{\text{RAS}}$ pulse time	<62>	t_{RAS}		$(2.5 + w_{RH} + w_{DA} + w)T - 10$		ns
$\overline{\text{RAS}}$ hold time	<63>	t_{RSH}		$(1.5 + w_{DA} + w)T - 10$		ns
Column address read time (from $\overline{\text{RAS}}$ ↑)	<64>	t_{RAL}		$(2 + w_{DA} + w)T - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65>	t_{CAS}		$(1 + w_{DA} + w)T - 10$		ns
$\overline{\text{CAS}}$-$\overline{\text{RAS}}$ precharge time	<66>	t_{CRP}		$(1 + w_{RH})T - 10$		ns
$\overline{\text{CAS}}$ hold time	<67>	t_{CSH}		$(2 + w_{RH} + w_{DA} + w)T - 10$		ns
$\overline{\text{CAS}}$ precharge time	<71>	t_{CPN}		$(2 + w_{RP} + w_{RH})T - 10$		ns
$\overline{\text{RAS}}$ column address delay time	<76>	t_{RAD}		$(0.5 + w_{RH})T - 10$		ns
$\overline{\text{RAS}}$-$\overline{\text{CAS}}$ delay time	<77>	t_{RCD}		$(1 + w_{RH})T - 10$		ns
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}}$ ↓)	<84>	t_{WCS}		$(1 + w_{RP} + w_{RH})T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}$ ↓)	<85>	t_{WCH}		$(1 + w_{DA} + w)T - 10$		ns
Data setup time (to $\overline{\text{CAS}}$ ↓)	<86>	t_{DS}		$(1.5 + w_{RP} + w_{RH})T - 10$		ns
Data hold time (from $\overline{\text{CAS}}$ ↓)	<87>	t_{DH}		$(1.5 + w_{DA} + w)T - 10$		ns

Remarks
1. $T = t_{CYK}$
2. w: The number of waits due to $\overline{\text{WAIT}}$.
3. w_{RP}: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. w_{RH}: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(c) Write timing (high-speed page DRAM access, normal access: off-page) (2/2)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

2. The broken lines indicate high impedance.

3. n = 3 to 5

(d) Write timing (high-speed page DRAM access: on-page) (1/2)

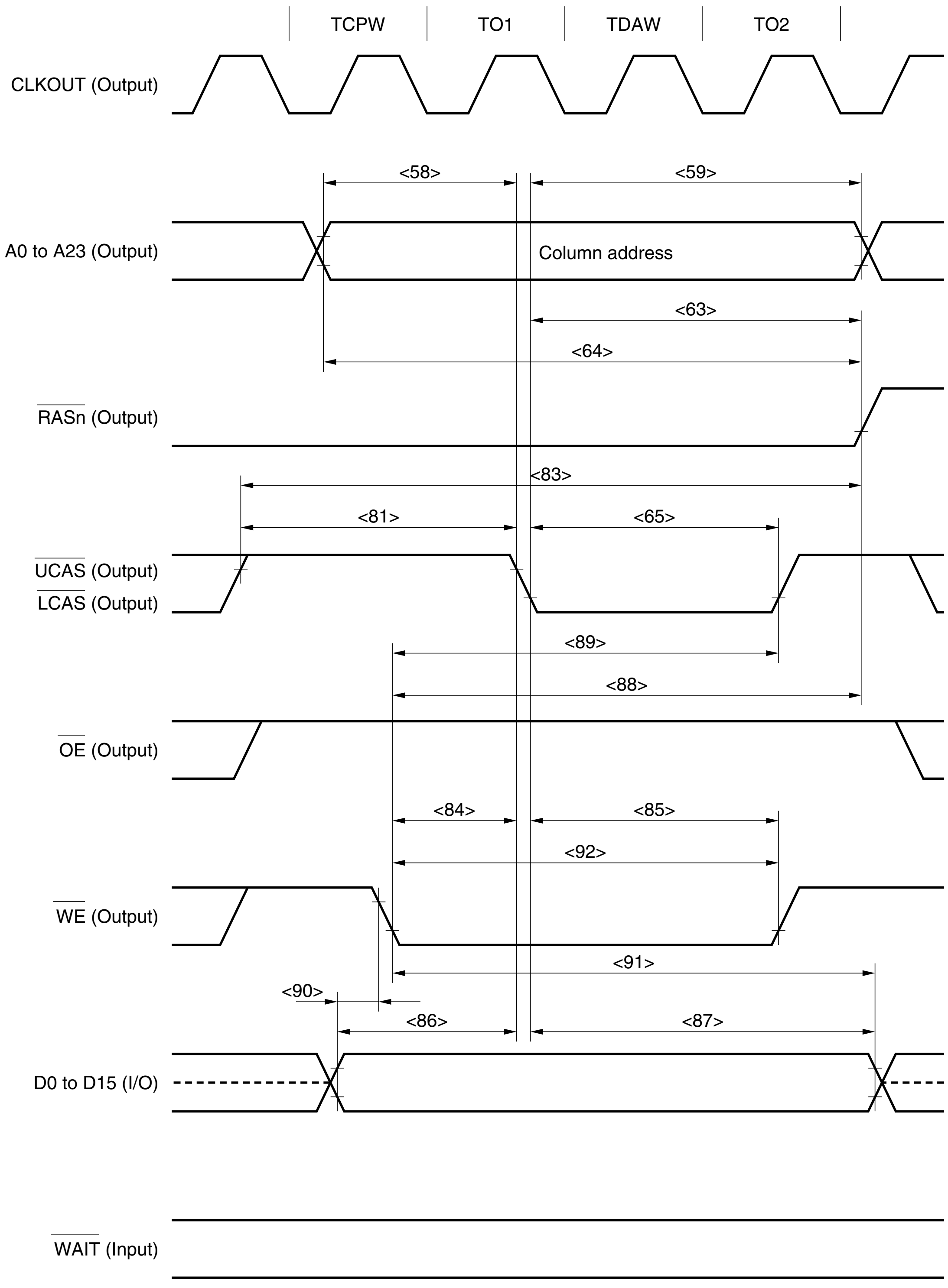
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Column address setup time	<58>	t_{ASC}		$(0.5 + w_{CP})T - 10$		ns
Column address hold time	<59>	t_{CAH}		$(1.5 + w_{DA})T - 10$		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		$(1.5 + w_{DA})T - 10$		ns
Column address read time (from $\overline{RAS}$ ↑)	<64>	t_{RAL}		$(2 + w_{CP} + w_{DA})T - 10$		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		$(1 + w_{DA})T - 10$		ns
$\overline{CAS}$ precharge time	<81>	t_{CP}		$(1 + w_{CP})T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge	<83>	t_{RHCP}		$(2.5 + w_{CP} + w_{DA})T - 10$		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	<84>	t_{WCS}	$w_{CP} \geq 1$	$w_{CP}T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↓)	<85>	t_{WCH}		$(1 + w_{DA})T - 10$		ns
Data setup time (to $\overline{CAS}$ ↓)	<86>	t_{DS}		$(0.5 + w_{CP})T - 10$		ns
Data hold time (from $\overline{CAS}$ ↓)	<87>	t_{DH}		$(1.5 + w_{DA})T - 10$		ns
$\overline{WE}$ read time (from $\overline{RAS}$ ↑)	<88>	t_{RWL}	$w_{CP} = 0$	$(1.5 + w_{DA})T - 10$		ns
$\overline{WE}$ read time (from $\overline{CAS}$ ↑)	<89>	t_{CWL}	$w_{CP} = 0$	$(1 + w_{DA})T - 10$		ns
Data setup time (to $\overline{WE}$ ↓)	<90>	t_{DSWE}	$w_{CP} = 0$	$0.5T - 10$		ns
Data hold time (from $\overline{WE}$ ↓)	<91>	t_{DHWE}	$w_{CP} = 0$	$(1.5 + w_{DA})T - 10$		ns
$\overline{WE}$ pulse width	<92>	t_{WP}	$w_{CP} = 0$	$(1 + w_{DA})T - 10$		ns

Remarks 1. $T = t_{CYK}$

2. w_{CP}: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(d) **Write timing (high-speed page DRAM access: on-page) (2/2)**



Remarks **1.** This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
2. The broken lines indicate high impedance.
3. n = 3 to 5

(e) Read timing (EDO DRAM) (1/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
Data input setup time (to CLKOUT ↑)		<26>	t_{SKID}		18		ns
Data input hold time (from CLKOUT ↑)		<27>	t_{HKID}		2		ns
Delay time from $\overline{OE}$ ↑ to data output		<37>	t_{DRDOD}		(0.5 + i)T – 10		ns
Row address setup time		<56>	t_{ASR}		(0.5 + w_{RP})T – 10		ns
Row address hold time		<57>	t_{RAH}		(0.5 + w_{RH})T – 10		ns
Column address setup time		<58>	t_{ASC}		0.5T – 10		ns
Column address hold time		<59>	t_{CAH}		(0.5 + w_{DA})T – 10		ns
$\overline{RAS}$ precharge time		<61>	t_{RP}		(0.5 + w_{RP})T – 10		ns
Column address read time (from $\overline{RAS}$ ↑)		<64>	t_{RAL}		(2 + w_{CP} + w_{DA})T – 10		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time		<66>	t_{CRP}		(1 + w_{RP})T – 10		ns
$\overline{CAS}$ hold time		<67>	t_{CSH}		(1.5 + w_{RH} + w_{DA})T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)		<68>	t_{RCS}		(2 + w_{RP} + w_{RH})T – 10		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)		<69>	t_{RRH}		0.5T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)		<70>	t_{RCH}		1.5T – 10		ns
$\overline{RAS}$ access time		<73>	t_{RAC}			(2 + w_{RH} + w_{DA})T – 28	ns
Access time from column address		<74>	t_{AA}			(1.5 + w_{DA})T – 28	ns
$\overline{CAS}$ access time		<75>	t_{CAC}			(1 + w_{DA})T – 28	ns
Delay time from $\overline{RAS}$ to column address		<76>	t_{RAD}		(0.5 + w_{RH})T – 10		ns
$\overline{RAS}$-$\overline{CAS}$ delay time		<77>	t_{RCD}		(1 + w_{RH})T – 10		ns
Output buffer turn-off delay time (from $\overline{OE}$)		<78>	t_{OEZ}		0		ns
Access time from $\overline{CAS}$ precharge		<80>	t_{ACP}			(1.5 + w_{CP} + w_{DA})T – 28	ns
$\overline{CAS}$ precharge time		<81>	t_{CP}		(0.5 + w_{CP})T – 10		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge		<83>	t_{RHCP}		(2 + w_{CP} + w_{DA})T – 10		ns
Read cycle time		<93>	t_{HPC}		(1 + w_{DA} + w_{CP})T – 10		ns
$\overline{RAS}$ pulse width		<94>	t_{RASP}		(2.5 + w_{RH} + w_{DA})T – 10		ns
$\overline{CAS}$ pulse width		<95>	t_{HCAS}		(0.5 + w_{DA})T – 10		ns
$\overline{CAS}$ hold time from $\overline{OE}$	Off-page	<96>	t_{OCH1}		(2 + w_{RH} + w_{DA})T – 10		ns
	On-page	<97>	t_{OCH2}		(0.5 + w_{DA})T – 10		ns
Data input hold time (from $\overline{CAS}$ ↓)		<98>	t_{DHC}		0		ns

Remarks
1. T = t_{CYK}
2. w_{RP}: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
3. w_{RH}: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. w_{CP}: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. i: The number of idle states that are inserted when a write cycle follows a read cycle.

(e) Read timing (EDO DRAM) (2/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
Output enable access time	Off-page	<99>	t_{OEA1}			$(2 + w_{RP} + w_{RH} + w_{DA})T - 28$	ns
	On-page	<100>	t_{OEA2}			$(1 + w_{CP} + w_{DA})T - 28$	ns

Remarks 1. $T = t_{CYK}$

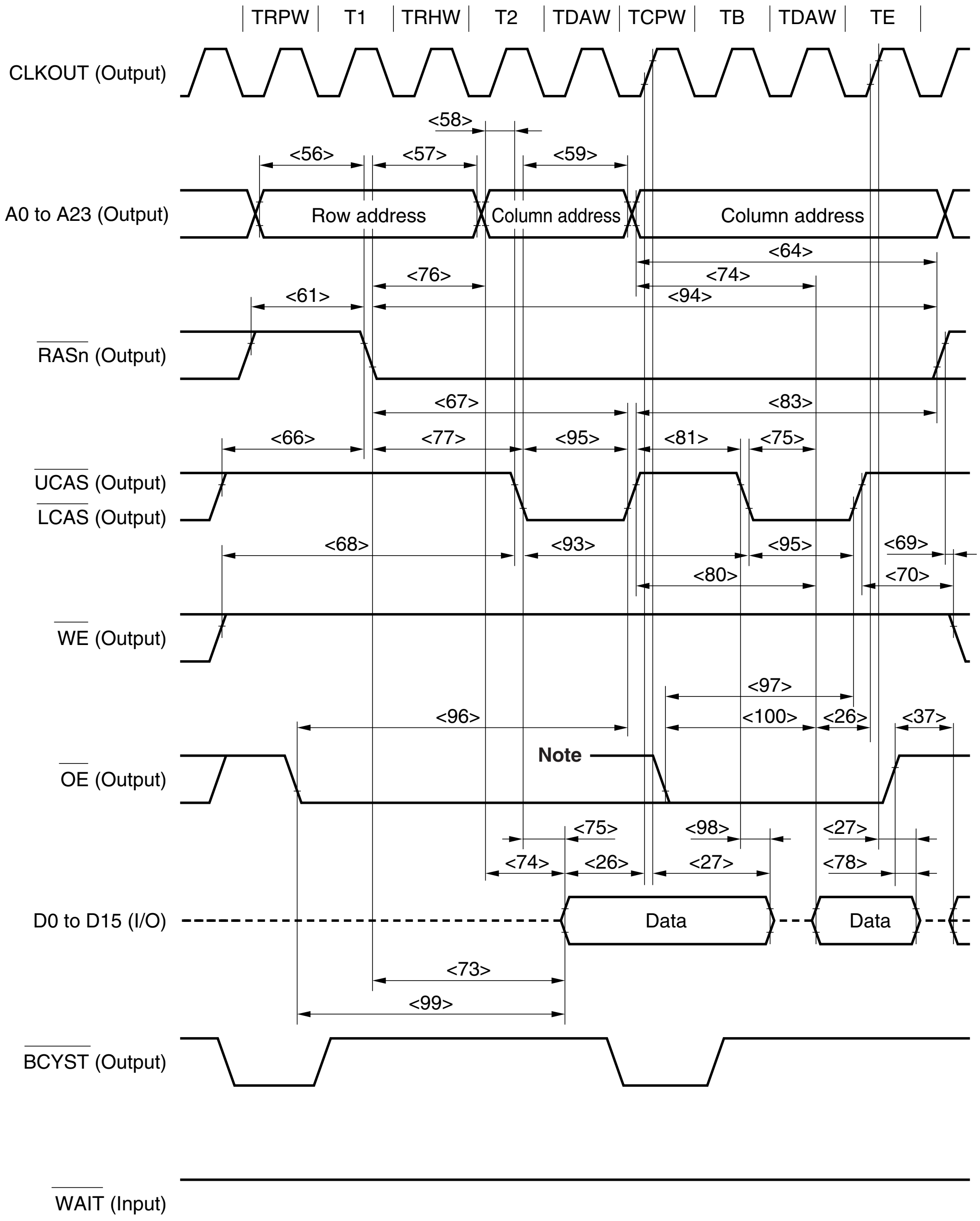
2. w_{RP}: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

3. w_{RH}: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

4. w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

5. w_{CP}: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(e) Read timing (EDO DRAM) (3/3)



Note For on-page access from another cycle during the $\overline{\text{RASn}}$ low-level signal.

Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1

2. The broken lines indicate high impedance.

3. n = 3 to 5

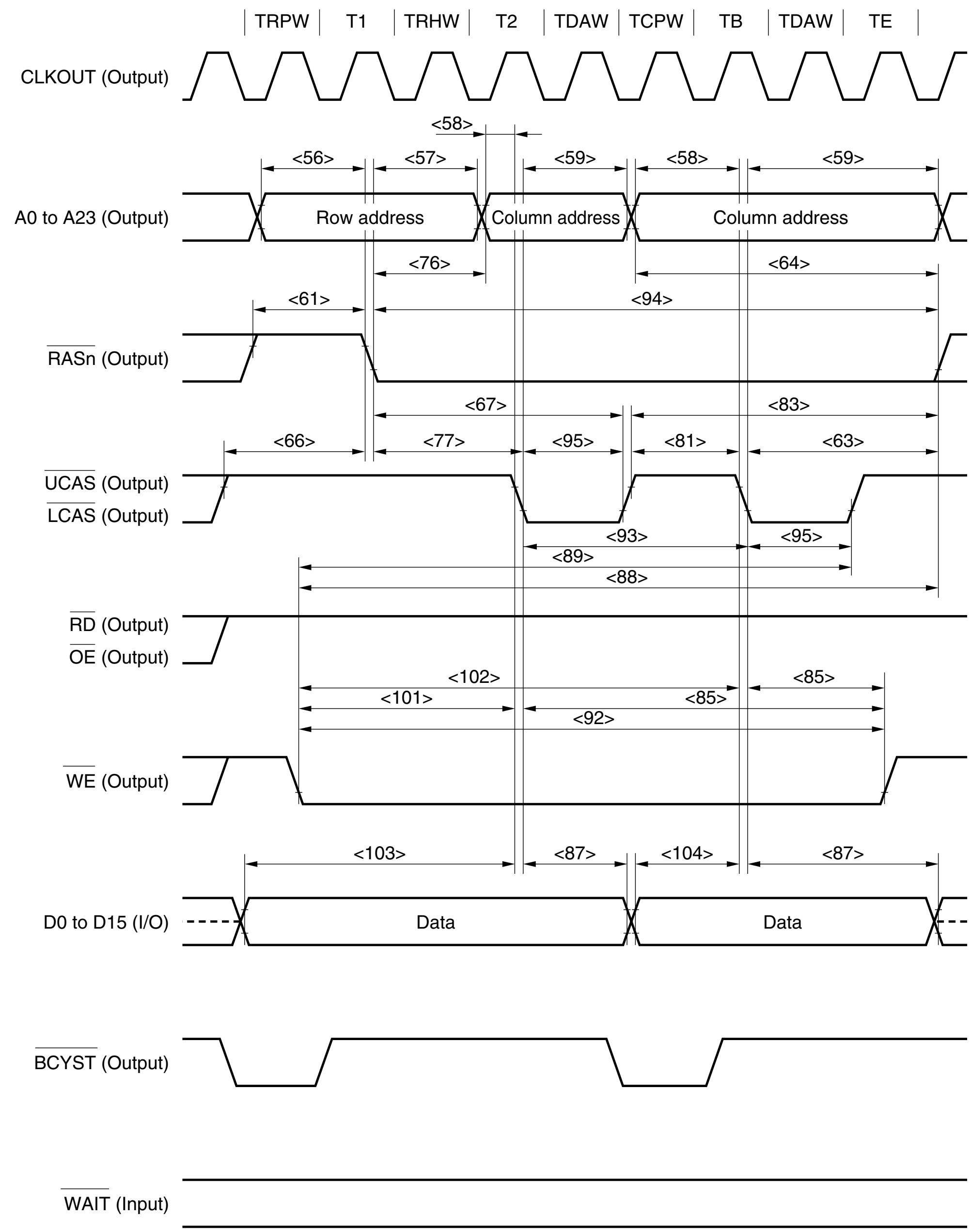
[MEMO]

(f) Write timing (EDO DRAM) (1/2)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
Row address setup time		<56>	t_{ASR}		$(0.5 + w_{RP})T - 10$		ns
Row address hold time		<57>	t_{RAH}		$(0.5 + w_{RH})T - 10$		ns
Column address setup time		<58>	t_{ASC}		$0.5T - 10$		ns
Column address hold time		<59>	t_{CAH}		$(0.5 + w_{DA})T - 10$		ns
$\overline{\text{RAS}}$ precharge time		<61>	t_{RP}		$(0.5 + w_{RP})T - 10$		ns
$\overline{\text{RAS}}$ hold time		<63>	t_{RSH}		$(1.5 + w_{DA})T - 10$		ns
Column address read time (from $\overline{\text{RAS}}$ ↑)		<64>	t_{RAL}		$(2 + w_{CP} + w_{DA})T - 10$		ns
$\overline{\text{CAS}}$-$\overline{\text{RAS}}$ precharge time		<66>	t_{CRP}		$(1 + w_{RP})T - 10$		ns
$\overline{\text{CAS}}$ hold time		<67>	t_{CSH}		$(1.5 + w_{RH} + w_{DA})T - 10$		ns
Delay time from $\overline{\text{RAS}}$ to column address		<76>	t_{RAD}		$(0.5 + w_{RH})T - 10$		ns
$\overline{\text{RAS}}$-$\overline{\text{CAS}}$ delay time		<77>	t_{RCD}		$(1 + w_{RH})T - 10$		ns
$\overline{\text{CAS}}$ precharge time		<81>	t_{CP}		$(0.5 + w_{CP})T - 10$		ns
$\overline{\text{RAS}}$ hold time for $\overline{\text{CAS}}$ precharge		<83>	t_{RHCP}		$(2 + w_{CP} + w_{DA})T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}$ ↓)		<85>	t_{WCH}		$(1 + w_{DA})T - 10$		ns
Data hold time (from $\overline{\text{CAS}}$ ↓)		<87>	t_{DH}		$(0.5 + w_{DA})T - 10$		ns
$\overline{\text{WE}}$ read time (from $\overline{\text{RAS}}$ ↑)	On-page	<88>	t_{RWL}	$w_{CP} = 0$	$(1.5 + w_{DA})T - 10$		ns
$\overline{\text{WE}}$ read time (from $\overline{\text{CAS}}$ ↑)	On-page	<89>	t_{CWL}	$w_{CP} = 0$	$(0.5 + w_{DA})T - 10$		ns
$\overline{\text{WE}}$ pulse width	On-page	<92>	t_{WP}	$w_{CP} = 0$	$(1 + w_{DA})T - 10$		ns
Write cycle time		<93>	t_{HPC}		$(1 + w_{DA} + w_{CP})T - 10$		ns
$\overline{\text{RAS}}$ pulse width		<94>	t_{RASP}		$(2.5 + w_{RH} + w_{DA})T - 10$		ns
$\overline{\text{CAS}}$ pulse width		<95>	t_{HCAS}		$(0.5 + w_{DA})T - 10$		ns
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}}$ ↓)	Off-page	<101>	t_{WCS1}		$(1 + w_{RP} + w_{RH})T - 10$		ns
	On-page	<102>	t_{WCS2}	$w_{CP} \geq 1$	$w_{CP}T - 10$		ns
Data setup time (to $\overline{\text{CAS}}$ ↓)	Off-page	<103>	t_{DS1}		$(1.5 + w_{RP} + w_{RH})T - 10$		ns
	On-page	<104>	t_{DS2}		$(0.5 + w_{CP})T - 10$		ns

Remarks
1. $T = t_{CYK}$
2. w_{RP}: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
3. w_{RH}: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. w_{CP}: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

(f) Write timing (EDO DRAM) (2/2)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1

2. The broken lines indicate high impedance.

3. n = 3 to 5

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (1/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{WAIT}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
Delay time from $\overline{OE}$ ↑ to data output	<37>	t_{DRDOD}		(0.5 + i)T – 10		ns
Delay time from address to $\overline{IOWR}$ ↓	<41>	t_{DAWR}		(0.5 + w_{RP})T – 10		ns
Address setup time (to $\overline{IOWR}$ ↑)	<42>	t_{SAWR}		(2 + w_{RP} + w_{RH} + w_{DA} + w)T – 10		ns
Delay time from $\overline{IOWR}$ ↑ to address	<43>	t_{DWRA}		0.5T – 10		ns
Delay time from $\overline{IOWR}$ ↑ to $\overline{RD}$ ↑	<48>	t_{DWRRD}	w_F = 0	0		ns
			w_F = 1	T – 10		ns
$\overline{IOWR}$ low-level width	<50>	t_{WWRL}		(2 + w_{RH} + w_{DA} + w)T – 10		ns
Row address setup time	<56>	t_{ASR}		(0.5 + w_{RP})T – 10		ns
Row address hold time	<57>	t_{RAH}		(0.5 + w_{RH})T – 10		ns
Column address setup time	<58>	t_{ASC}		0.5T – 10		ns
Column address hold time	<59>	t_{CAH}		(1.5 + w_{DA} + w_F + w)T – 10		ns
Read/write cycle time	<60>	t_{RC}		(3 + w_{RP} + w_{RH} + w_{DA} + w_F + w)T – 10		ns
$\overline{RAS}$ precharge time	<61>	t_{RP}		(0.5 + w_{RP})T – 10		ns
$\overline{RAS}$ hold time	<63>	t_{RSH}		(1.5 + w_{DA} + w_F + w)T – 10		ns
Column address read time for $\overline{RAS}$	<64>	t_{RAL}		(2 + w_{CP} + w_{DA} + w_F + w)T – 10		ns
$\overline{CAS}$ pulse width	<65>	t_{CAS}		(1 + w_{DA} + w_F + w)T – 10		ns
$\overline{CAS}$-$\overline{RAS}$ precharge time	<66>	t_{CRP}		(1 + w_{RP})T – 10		ns
$\overline{CAS}$ hold time	<67>	t_{CSH}		(2 + w_{RH} + w_{DA} + w_F + w)T – 10		ns

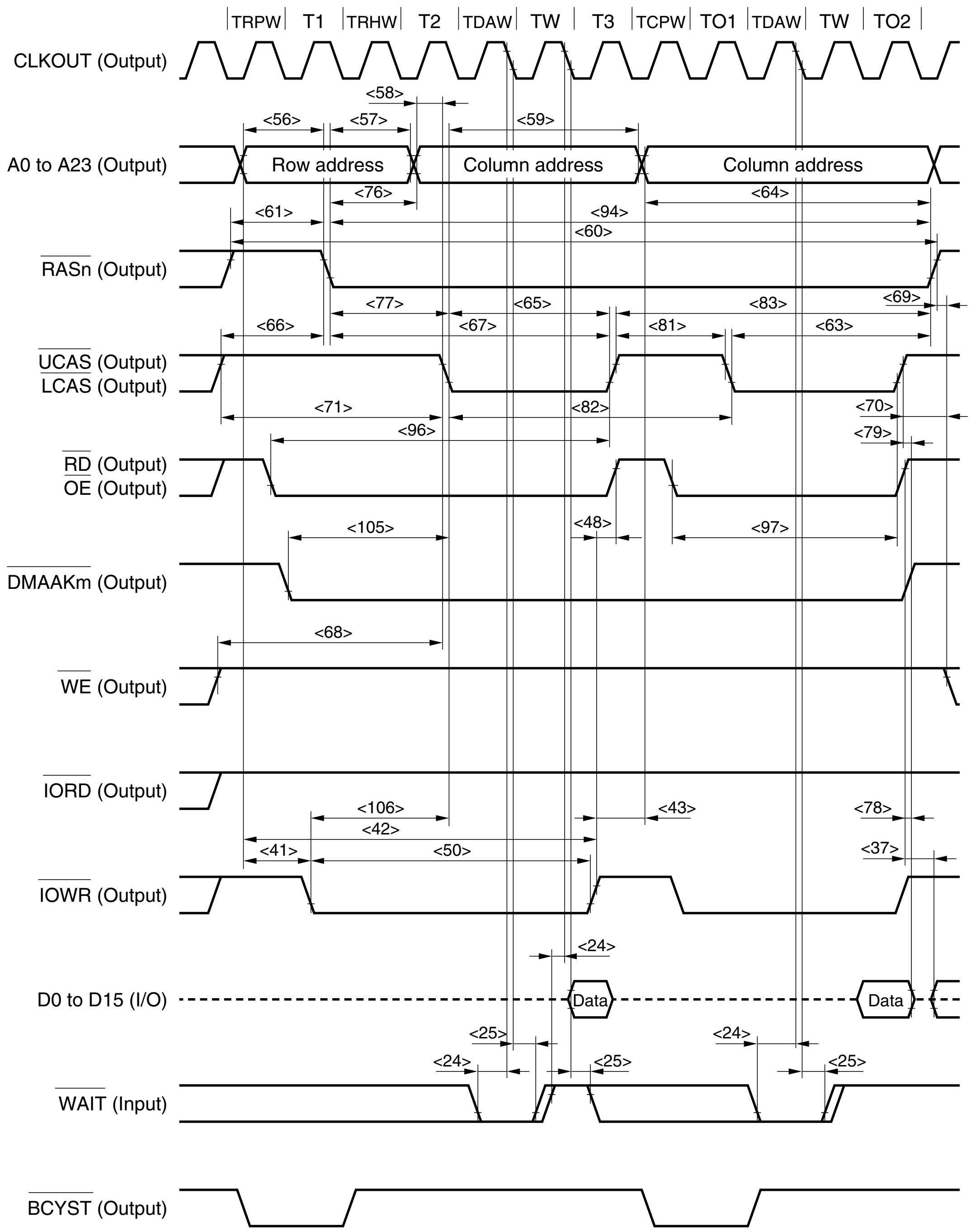
Remarks
1. T = t_{CYK}
2. w: The number of waits due to $\overline{WAIT}$.
3. w_{RP}: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. w_{RH}: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
6. w_{CP}: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
7. w_F: The number of waits that are inserted for a source-side access during a DMA flyby transfer.
8. i: The number of idle states that are inserted when a write cycle follows a read cycle.

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (2/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)		<68>	t_{RCS}		$(2 + w_{RP} + w_{RH})T - 10$		ns
$\overline{WE}$ hold time (from $\overline{RAS}$ ↑)		<69>	t_{RRH}		$0.5T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}$ ↑)		<70>	t_{RCH}		$1.5T - 10$		ns
$\overline{CAS}$ precharge time		<71>	t_{CPN}		$(2 + w_{RP} + w_{RH})T - 10$		ns
Delay time from $\overline{RAS}$ to column address		<76>	t_{RAD}		$(0.5 + w_{RH})T - 10$		ns
$\overline{RAS}$-$\overline{CAS}$ delay time		<77>	t_{RCD}		$(1 + w_{RH})T - 10$		ns
Output buffer turn-off delay time (from $\overline{OE}$ ↑)		<78>	t_{OEZ}		0		ns
Output buffer turn-off delay time (from $\overline{CAS}$ ↑)		<79>	t_{OFF}		0		ns
$\overline{CAS}$ precharge time		<81>	t_{CP}		$(0.5 + w_{CP})T - 10$		ns
High-speed page mode cycle time		<82>	t_{PC}		$(2 + w_{CP} + w_{DA} + w_F + w)T - 10$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge		<83>	t_{RHCP}		$(2.5 + w_{CP} + w_{DA} + w_F + w)T - 10$		ns
$\overline{RAS}$ pulse width		<94>	t_{RASP}		$(2.5 + w_{RH} + w_{DA} + w_F + w)T - 10$		ns
$\overline{CAS}$ hold time from $\overline{OE}$ (from $\overline{CAS}$ ↑)	Off-page	<96>	t_{OCH1}		$(2.5 + w_{RP} + w_{RH} + w_{DA} + w_F + w)T - 10$		ns
	On-page	<97>	t_{OCH2}		$(1.5 + w_{CP} + w_{DA} + w_F + w)T - 10$		ns
Delay time from $\overline{DMAAKm}$ ↓ to $\overline{CAS}$ ↓		<105>	t_{DDACS}		$(1.5 + w_{RH})T - 10$		ns
Delay time from $\overline{IOWR}$ ↓ to $\overline{CAS}$ ↓		<106>	t_{DRDCS}		$(1 + w_{RH})T - 10$		ns

Remarks
1. $T = t_{CYK}$
2. w: The number of waits due to $\overline{WAIT}$.
3. w_{CP}: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. w_{RH}: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
6. w_{RP}: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
7. w_F: The number of waits that are inserted for a source-side access during a DMA flyby transfer.
8. m = 0 to 3

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (3/3)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).

Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1

Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1

Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1

Number of waits that are inserted for a source-side access during a DMA flyby transfer: 0

2. The broken lines indicate high impedance.

3. n = 3 to 5, m = 0 to 3

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (1/3)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<24>	t_{SWK}		15		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<25>	t_{HKW}		2		ns
$\overline{\text{IORD}}$ low-level width	<32>	t_{WRDL}		$(2 + w_{RH} + w_{DA} + w_F + w)T - 10$		ns
$\overline{\text{IORD}}$ high-level width	<33>	t_{WRDH}		$T - 10$		ns
Delay time from address to $\overline{\text{IORD}}$ ↑	<34>	t_{DARD}		$0.5T - 10$		ns
Delay time from $\overline{\text{IORD}}$ ↑ to address	<35>	t_{DRDA}		$(0.5 + i)T - 10$		ns
Row address setup time	<56>	t_{ASR}		$(0.5 + w_{RP})T - 10$		ns
Row address hold time	<57>	t_{RAH}		$(0.5 + w_{RH})T - 10$		ns
Column address setup time	<58>	t_{ASC}		$0.5T - 10$		ns
Column address hold time	<59>	t_{CAH}		$(1.5 + w_{DA} + w_F)T - 10$		ns
Read/write cycle time	<60>	t_{RC}		$(3 + w_{RP} + w_{RH} + w_{DA} + w_F + w)T - 10$		ns
$\overline{\text{RAS}}$ precharge time	<61>	t_{RP}		$(0.5 + w_{RP})T - 10$		ns
$\overline{\text{RAS}}$ hold time	<63>	t_{RSH}		$(1.5 + w_{DA} + w_F)T - 10$		ns
Column address read time for $\overline{\text{RAS}}$	<64>	t_{RAL}		$(2 + w_{CP} + w_{DA} + w_F + w)T - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65>	t_{CAS}		$(1 + w_{DA} + w_F)T - 10$		ns
$\overline{\text{CAS}}$-$\overline{\text{RAS}}$ precharge time	<66>	t_{CRP}		$(1 + w_{RP})T - 10$		ns
$\overline{\text{CAS}}$ hold time	<67>	t_{CSH}		$(2 + w_{RH} + w_{DA} + w_F + w)T - 10$		ns
$\overline{\text{CAS}}$ precharge time	<71>	t_{CPN}		$(2 + w_{RP} + w_{RH} + w)T - 10$		ns
Delay time from $\overline{\text{RAS}}$ to column address	<76>	t_{RAD}		$(0.5 + w_{RH})T - 10$		ns
$\overline{\text{RAS}}$-$\overline{\text{CAS}}$ delay time	<77>	t_{RCD}		$(1 + w_{RH} + w)T - 10$		ns
$\overline{\text{CAS}}$ precharge time	<81>	t_{CP}		$(0.5 + w_{CP} + w)T - 10$		ns
High-speed page mode cycle time	<82>	t_{PC}		$(2 + w_{CP} + w_{DA} + w_F + w)T - 10$		ns
$\overline{\text{RAS}}$ hold time for $\overline{\text{CAS}}$ precharge	<83>	t_{RHCP}		$(2.5 + w_{CP} + w_{DA} + w)T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}$ ↓)	<85>	t_{WCH}		$(1 + w_{DA})T - 10$		ns
$\overline{\text{WE}}$ read time (from $\overline{\text{RAS}}$ ↑)	<88>	t_{RWL}	$w_{CP} = 0$	$(1.5 + w_{DA} + w)T - 10$		ns

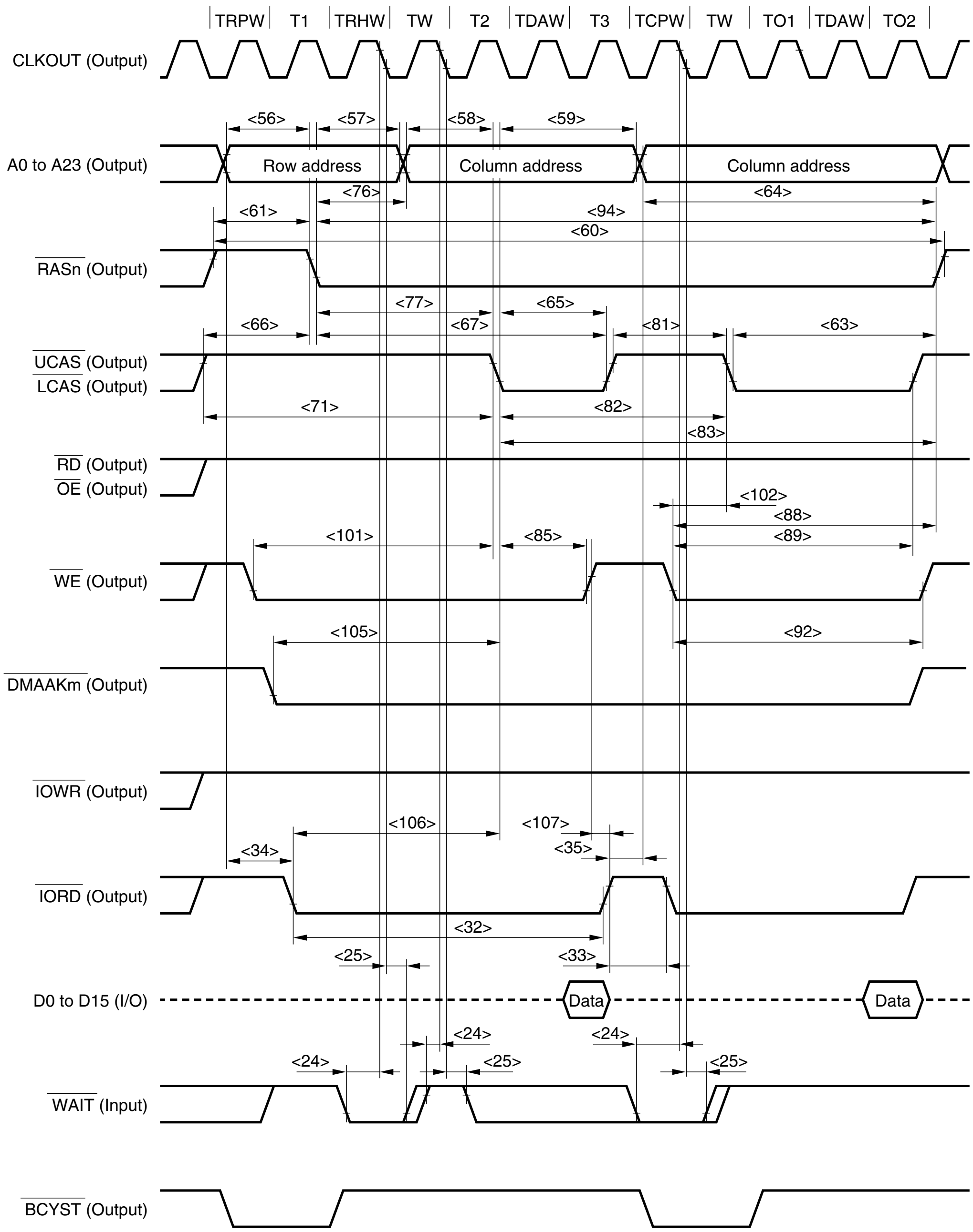
Remarks
1. $T = t_{CYK}$
2. w: The number of waits due to $\overline{\text{WAIT}}$.
3. w_{RH}: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. w_{RP}: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
6. w_{CP}: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
7. w_F: The number of waits that are inserted for a source-side access during a DMA flyby transfer.
8. i: The number of idle states that are inserted when a write cycle follows a read cycle.

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (2/3)

Parameter		Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{WE}}$ read time (from $\overline{\text{CAS}}$ ↑)		<89>	t_{CWL}	$w_{CP} = 0$	$(1 + w_{DA} + w)T - 10$		ns
$\overline{\text{WE}}$ pulse width		<92>	t_{WP}	$w_{CP} = 0$	$(1 + w_{DA} + w)T - 10$		ns
$\overline{\text{RAS}}$ pulse width		<94>	t_{RASP}		$(2.5 + w_{RH} + w_{DA} + w_F + w)T - 10$		ns
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}}$ ↓)	Off-page	<101>	t_{WCS1}	$w_{CP} = 0$	$(1 + w_{RH} + w_{RP} + w)T - 10$		ns
	On-page	<102>	t_{WCS2}	$w_{CP} \geq 1$	$w_{CP}T - 10$		ns
Delay time from $\overline{\text{DMAAKm}}$ ↓ to $\overline{\text{CAS}}$ ↓		<105>	t_{DDACS}		$(1.5 + w_{RH} + w)T - 10$		ns
Delay time from $\overline{\text{IORD}}$ ↓ to $\overline{\text{CAS}}$ ↓		<106>	t_{DRDCS}		$(1 + w_{RH} + w)T - 10$		ns
Delay time from $\overline{\text{WE}}$ ↑ to $\overline{\text{IORD}}$ ↑		<107>	t_{DWERD}	$w_F = 0$	0		ns
				$w_F = 1$	$T - 10$		ns

Remarks
1. $T = t_{CYK}$
2. w: The number of waits due to $\overline{\text{WAIT}}$.
3. w_{RH}: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
4. w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
5. w_{RP}: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
6. w_{CP}: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
7. w_F: The number of waits that are inserted for a source-side access during a DMA flyby transfer.
8. m = 0 to 3

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (3/3)



Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).

Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1

Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1

Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1

Number of waits that are inserted for a source-side access during a DMA flyby transfer: 0

2. The broken lines indicate high impedance.

3. n = 3 to 5, m = 0 to 3

(i) CBR refresh timing

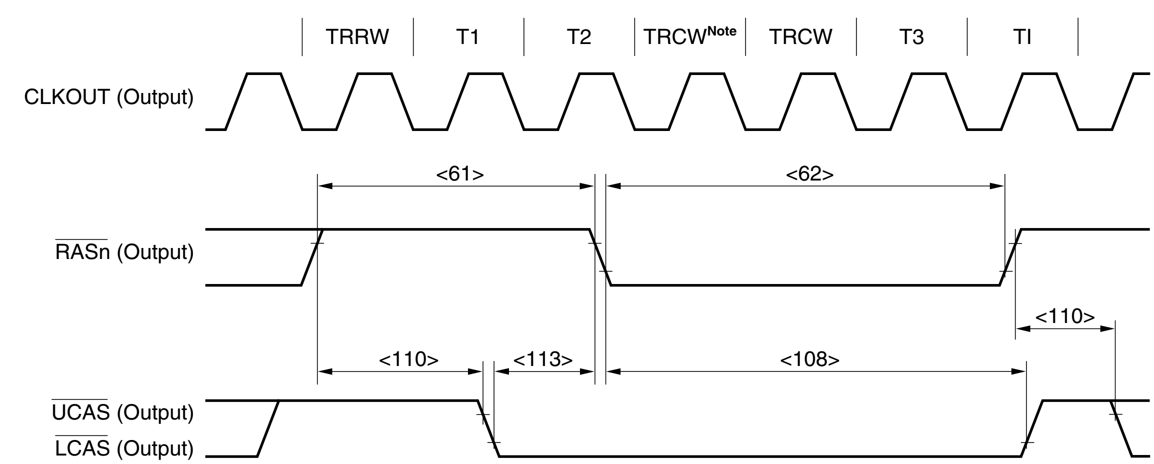
Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RAS}}$ precharge time	<61>	t_{RP}		$(1.5 + w_{RRW})T - 10$		ns
$\overline{\text{RAS}}$ pulse width	<62>	t_{RAS}		$(1.5 + w_{RCW}{}^{\text{Note}})T - 10$		ns
$\overline{\text{CAS}}$ hold time	<108>	t_{CHR}		$(1.5 + w_{RCW}{}^{\text{Note}})T - 10$		ns
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	<110>	t_{RPC}		$(0.5 + w_{RRW})T - 10$		ns
$\overline{\text{CAS}}$ setup time	<113>	t_{CSR}		$T - 10$		ns

Note At least one clock cycle is inserted by default for w_{RCW} regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

Remarks 1. $T = t_{CYK}$

2. w_{RRW}: The number of waits due to the RRW0 and RRW1 bits of the RWC register.

3. w_{RCW}: The number of waits due to the RCW0 to RCW2 bits of the RWC register.



Note This TRCW is always inserted regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

Remarks 1. This is the timing for the following case.

Number of waits due to the RRW0 and RRW1 bits of the RWC register (TRRW): 1

Number of waits due to the RCW0 to RCW2 bits of the RWC register (TRCW): 2

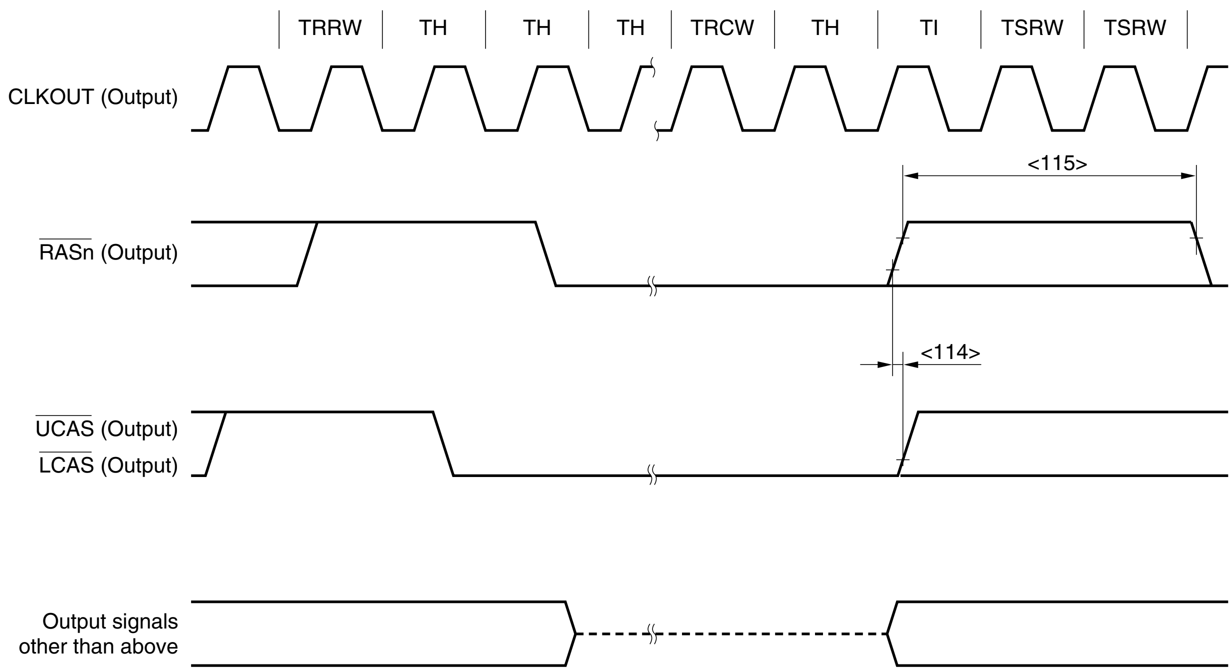
2. n = 3 to 5

(j) CBR self-refresh timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{CAS}$ hold time	<114>	t_{CHS}		–5		ns
$\overline{RAS}$ precharge time	<115>	t_{RPS}		$(1 + 2w_{SRW})T – 10$		ns

Remarks 1. $T = t_{CYK}$

2. w_{SRW}: The number of waits due to the SRW0 to SRW2 bits of the RWC register.



Remarks 1. This is the timing for the following case.

Number of waits due to the RRW0 and RRW1 bits of the RWC register (TRRW): 1

Number of waits due to the RCW0 to RCW2 bits of the RWC register (TRCW): 1

Number of waits due to the SRW0 to SRW2 bits of the RWC register (TSRW): 2

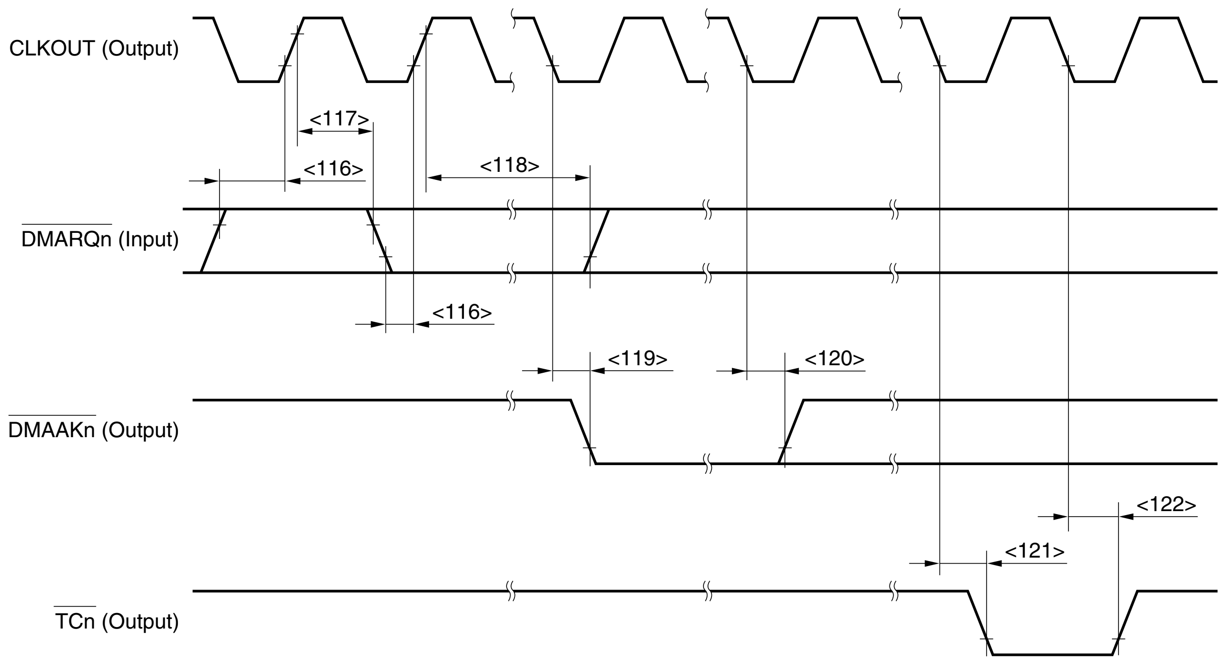
2. The broken lines indicate high impedance.

3. n = 3 to 5

(7) DMAC timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{DMARQn}}$ setup time (to CLKOUT ↑)	<116>	t_{SDRK}		15		ns
$\overline{\text{DMARQn}}$ hold time (from CLKOUT ↑)	<117>	t_{HKDR1}		2		ns
	<118>	t_{HKDR2}		Until $\overline{\text{DMAAKn}}$ ↓		ns
$\overline{\text{DMAAKn}}$ output delay time (from CLKOUT ↓)	<119>	t_{DKDA}		2	10	ns
$\overline{\text{DMAAKn}}$ output hold time (from CLKOUT ↓)	<120>	t_{HKDA}		2	10	ns
$\overline{\text{TCn}}$ output delay time (from CLKOUT ↓)	<121>	t_{DKTC}		2	10	ns
$\overline{\text{TCn}}$ output hold time (from CLKOUT ↓)	<122>	t_{HKTC}		2	10	ns

Remark n = 0 to 3



Remark n = 0 to 3

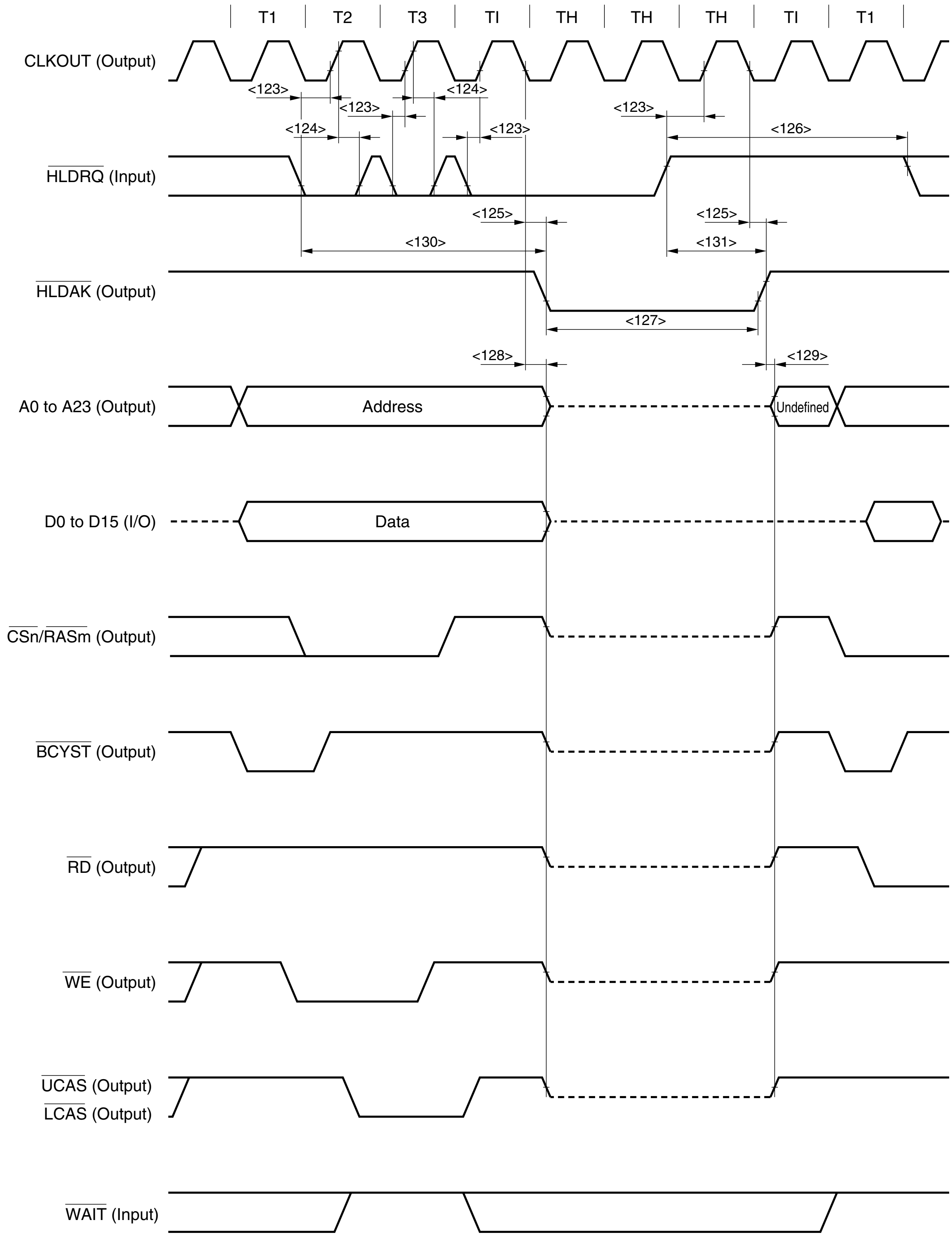
[MEMO]

(8) Bus hold timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (to CLKOUT ↑)	<123>	t_{SHRK}		15		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT ↑)	<124>	t_{HKHR}		2		ns
Delay time from CLKOUT ↓ to $\overline{\text{HLDAK}}$	<125>	t_{DKHA}		2	10	ns
$\overline{\text{HLDRQ}}$ high-level width	<126>	t_{WHQH}		T + 17		ns
$\overline{\text{HLDAK}}$ low-level width	<127>	t_{WHAL}		T – 8		ns
Delay time from $\overline{\text{CLKOUT}}$ ↓ to bus float	<128>	t_{DKCF}			10	ns
Delay time from $\overline{\text{HLDAK}}$ ↑ to bus output	<129>	t_{DHAC}		0		ns
Delay time from $\overline{\text{HLDRQ}}$ ↓ to $\overline{\text{HLDAK}}$ ↓	<130>	t_{DHQHA1}		2.5T		ns
Delay time from $\overline{\text{HLDRQ}}$ ↑ to $\overline{\text{HLDAK}}$ ↑	<131>	t_{DHQHA2}		0.5T	1.5T	ns

Remark $T = t_{CYK}$

(8) Bus hold timing (2/2)



Remarks **1.** The broken lines indicate high impedance.

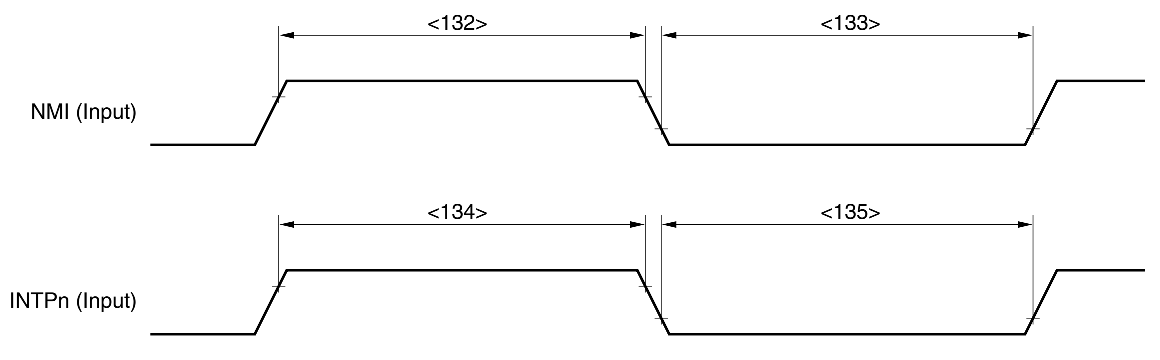
2. n = 0, 3 to 5, m = 3 to 5

(9) Interrupt timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
NMI high-level width	<132>	t_{WNIH}		500		ns
NMI low-level width	<133>	t_{WNIL}		500		ns
INTPn high-level width	<134>	t_{WITH}		4T + 10		ns
INTPn low-level width	<135>	t_{WITL}		4T + 10		ns

Remarks 1. n = 100 to 103, 110 to 113, 130

2. T = t_{CYK}



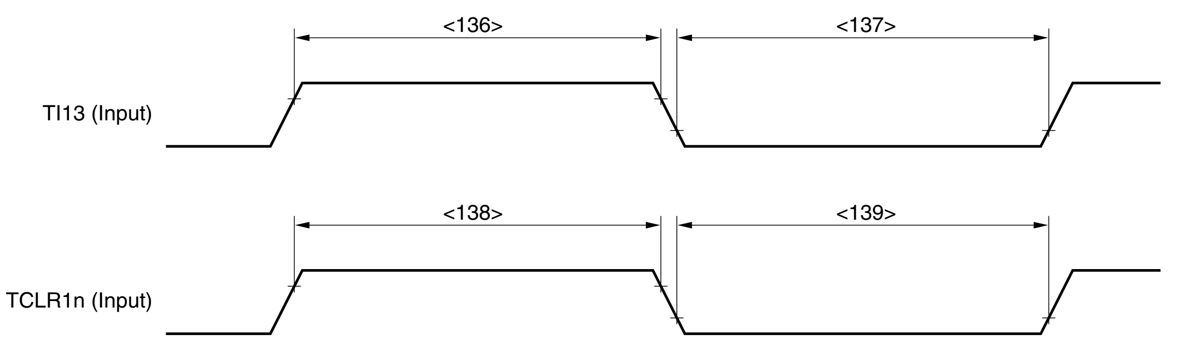
Remark n = 100 to 103, 110 to 113, 130

(10) RPU timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
TI13 high-level width	<136>	t_{WTIH}		3T + 18		ns
TI13 low-level width	<137>	t_{WTIL}		3T + 18		ns
TCLR1n high-level width	<138>	t_{WTCH}		3T + 18		ns
TCLR1n low-level width	<139>	t_{WTCL}		3T + 18		ns

Remarks 1. n = 0 to 2

2. T = t_{CYK}

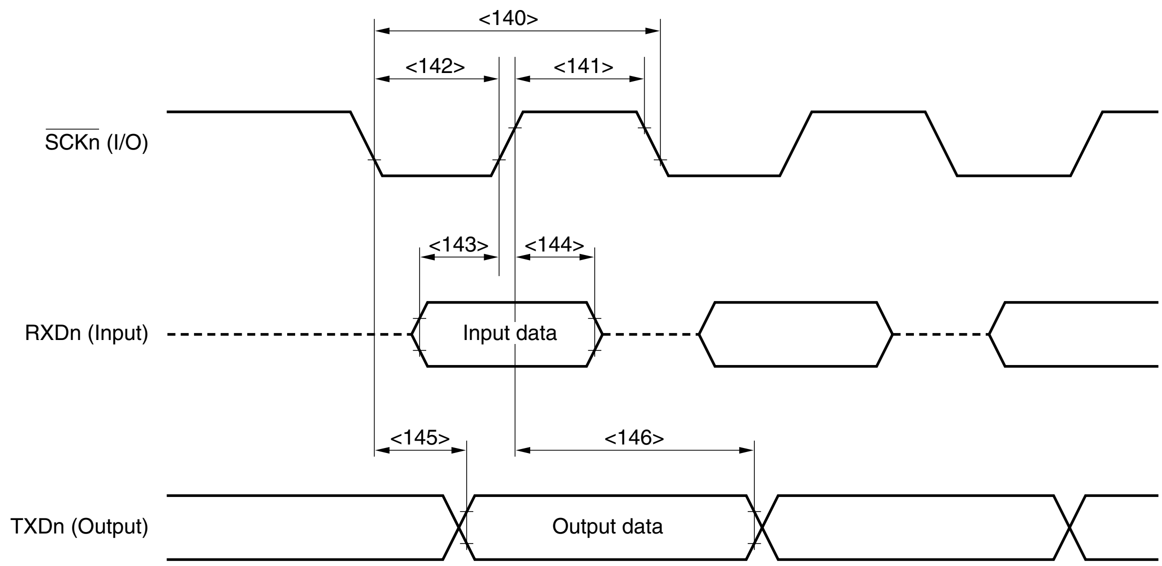


Remark n = 0 to 2

(11) UART0, UART1 timing (clock-synchronized or master mode only)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{SCKn}}$ cycle	<140>	t_{CYSK0}	Output	250		ns
$\overline{\text{SCKn}}$ high-level width	<141>	t_{WSK0H}	Output	$0.5t_{CYSK0} - 20$		ns
$\overline{\text{SCKn}}$ low-level width	<142>	t_{WSK0L}	Output	$0.5t_{CYSK0} - 20$		ns
RXDn setup time (to $\overline{\text{SCKn}}$ ↑)	<143>	t_{SRXSK}		30		ns
RXDn hold time (from $\overline{\text{SCKn}}$ ↑)	<144>	t_{HSKRX}		0		ns
TXDn output delay time (from $\overline{\text{SCKn}}$ ↓)	<145>	t_{DSKTX}			20	ns
TXDn output hold time (from $\overline{\text{SCKn}}$ ↑)	<146>	t_{HSKTX}		$0.5t_{CYSK0} - 5$		ns

Remark n = 0, 1



Remarks **1.** The broken lines indicate high impedance.
2. n = 0, 1

(12) CSI0, CSI1 timing

(a) Master mode

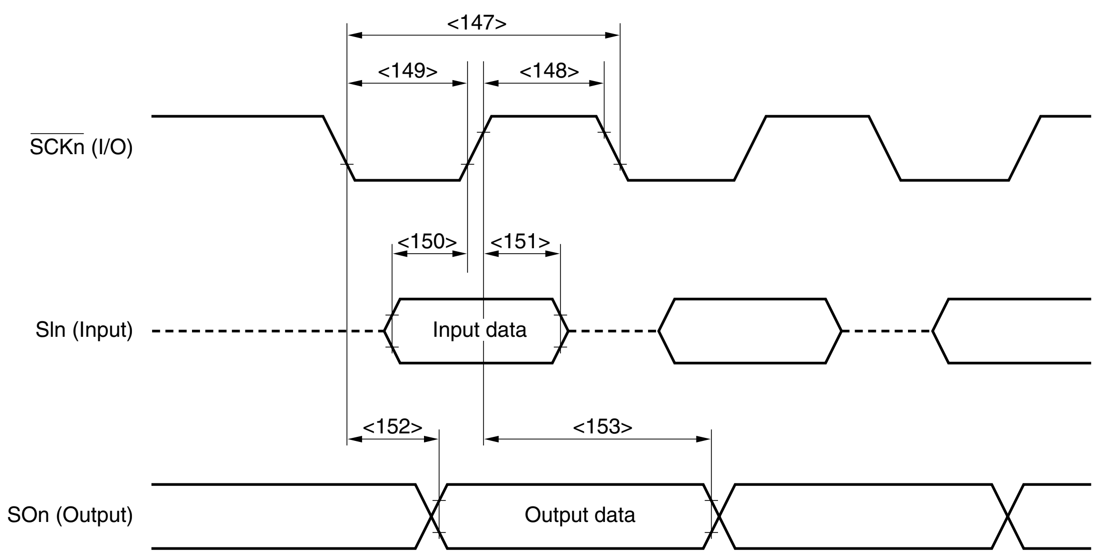
Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<147>	t_{CYSK1}	Output	100		ns
$\overline{SCKn}$ high-level width	<148>	t_{WSK1H}	Output	$0.5t_{CYSK1} - 20$		ns
$\overline{SCKn}$ low-level width	<149>	t_{WSK1L}	Output	$0.5t_{CYSK1} - 20$		ns
SIn setup time (to $\overline{SCKn}$ ↑)	<150>	t_{SSISK}		30		ns
SIn hold time (from $\overline{SCKn}$ ↑)	<151>	t_{HSKSI}		0		ns
SOn output delay time (from $\overline{SCKn}$ ↓)	<152>	t_{DSKSO}			20	ns
SOn output hold time (from $\overline{SCKn}$ ↑)	<153>	t_{HSKSO}		$0.5t_{CYSK1} - 5$		ns

Remark n = 0, 1

(b) Slave mode

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<147>	t_{CYSK1}	Input	100		ns
$\overline{SCKn}$ high-level width	<148>	t_{WSK1H}	Input	30		ns
$\overline{SCKn}$ low-level width	<149>	t_{WSK1L}	Input	30		ns
SIn setup time (to $\overline{SCKn}$ ↑)	<150>	t_{SSISK}		10		ns
SIn hold time (from $\overline{SCKn}$ ↑)	<151>	t_{HSKSI}		10		ns
SOn output delay time (from $\overline{SCKn}$ ↓)	<152>	t_{DSKSO}			30	ns
SOn output hold time (from $\overline{SCKn}$ ↑)	<153>	t_{HSKSO}		t_{WSK1H}		ns

Remark n = 0, 1



Remarks **1.** The broken lines indicate high impedance.
2. n = 0, 1

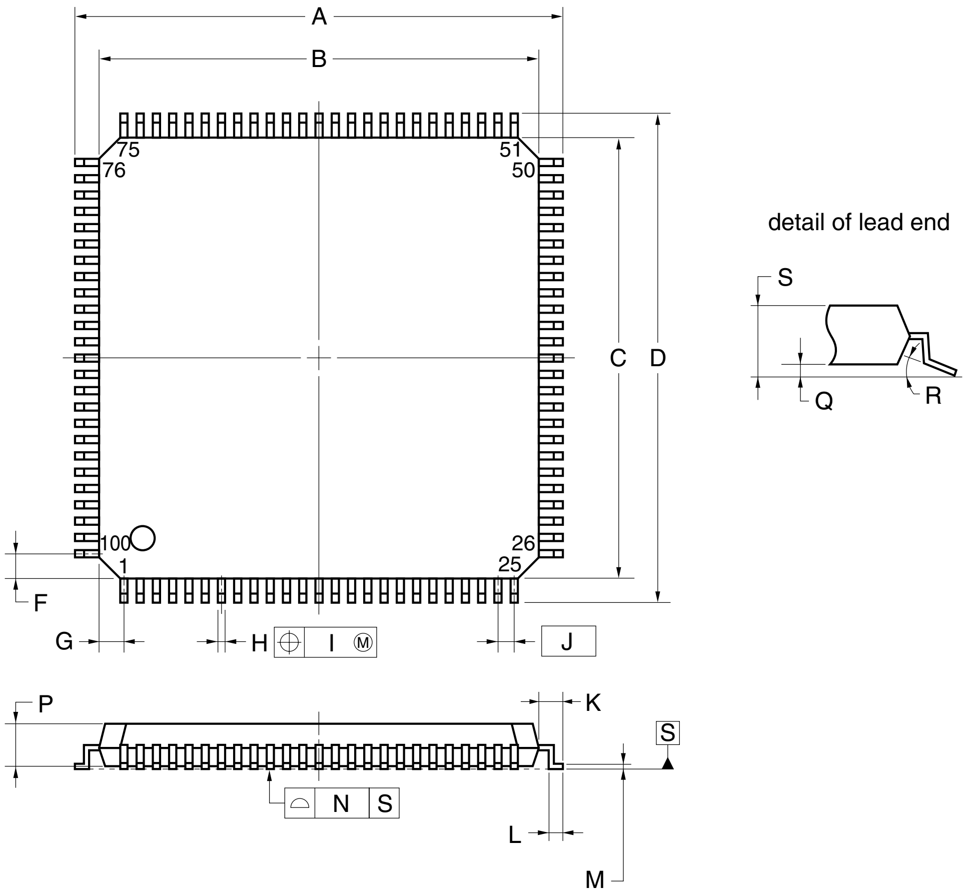
A/D Converter Characteristics **(T_A = –40 to +85°C, V_{DD} = CV_{DD} = 3.0 to 3.6 V, HV_{DD} = 5.0 V ±10%, V_{SS} = 0 V, HV_{DD} – 0.5 V ≤ AV_{DD} ≤ HV_{DD}, output pin load capacitance: C_L = 50 pF)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	–		10			bit
Overall error	–				±4	LSB
Quantization error	–				±1/2	LSB
Conversion time	t_{CONV}		5		10	μs
Sampling time	t_{SAMP}		Conversion clock[Note]/6			ns
Zero scale error	–				±4	LSB
Scale error	–				±4	LSB
Linearity error	–				±3	LSB
Analog input voltage	V_{IAN}		–0.3		AV_{REF} + 0.3	V
Analog input resistance	R_{AN}			2		MΩ
AV_{REF} input voltage	AV_{REF}	AV_{REF} = AV_{DD}	4.5		5.5	V
AV_{REF} input current	AI_{REF}				2.0	mA
AV_{DD} current	AI_{DD}				6	mA

Note Conversion clock is the number of clocks set by the ADM1 register.

4. PACKAGE DRAWING

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3°^{+7°}_{-3°}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

5. RECOMMENDED SOLDERING CONDITIONS

TBD

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Reference materials Electrical Characteristics for Microcomputer (U15170J[Note])

Note This document number is that of Japanese version.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.