Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.



Notice

- 1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
- Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights
 of third parties by or arising from the use of Renesas Electronics products or technical information described in this document.
 No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights
 of Renesas Electronics or others.
- 3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
- 4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
- 5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
- 6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
- 7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
 - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
 - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
 - "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
- 8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
- 9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
- 10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
- 11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics
- 12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.
- (Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.
- (Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

PRELIMINARY DATA SHEET



MOS INTEGRATED CIRCUIT

μ PD703130

V850E/MS2 32-BIT SINGLE-CHIP MICROCONTROLLER

The μ PD703130 is a member of the V850 Series of 32-bit single-chip microcontrollers designed for real-time control operations. These microcontrollers provide on-chip features, including a 32-bit CPU, RAM, interrupt controller, real-time pulse unit, serial interface, A/D converter, and DMA controller.

The μ PD703130 is a ROMless version product.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850E/MS2 User's Manual Hardware: U14985E V850E/MS1, V850E/MS2 User's Manual Architecture: U12197E

FEATURES

- Number of instructions: 81
- Minimum instruction execution time 30 ns (@ 33 MHz operation)
- General-purpose registers 32 bits × 32
- · Instruction set suitable for control applications
- Internal memory ROM: None RAM: 4 KB
- · Advanced on-chip interrupt controller
- Real-time pulse unit suitable for control operations
- · Powerful serial interface (on-chip dedicated baud rate generator)
- · On-chip clock generator
- 10-bit resolution A/D converter: 4 channels
- DMA controller: 4 channels
- · Power saving functions

APPLICATIONS

- Optical storage equipment (DVD players, etc.)
- · System control for digital consumer equipment, etc.

The information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion, may withdraw the product prior to its production. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.



ORDERING INFORMATION

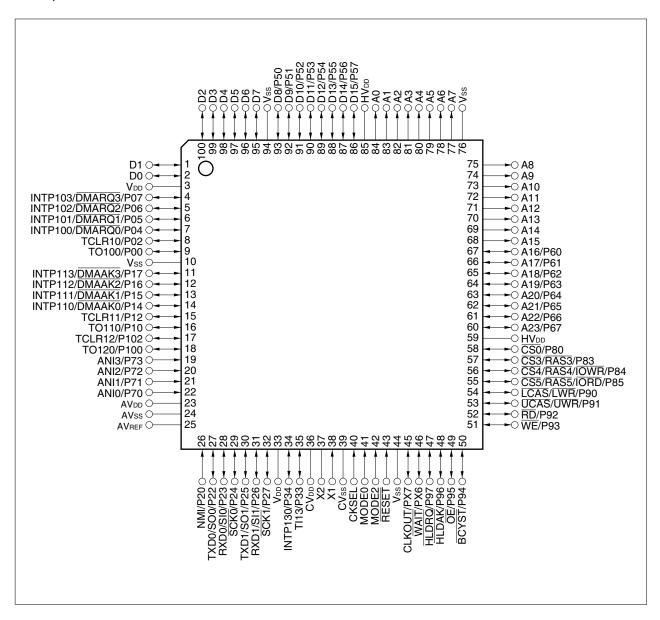
	Part Number	Package	Maximum Operating Frequency	Internal ROM
	μPD703130GC-8EU	100-pin plastic LQFP (fine pitch) (14 \times 14)	33 MHz	None
*	μPD703130GC-8EU-A	100-pin plastic LQFP (fine pitch) (14 \times 14)	33 MHz	None

Remark Products with -A at the end of the part number are lead-free products.

PIN CONFIGURATION (TOP VIEW)

100-pin plastic LQFP (fine pitch) (14 × 14)

- μPD703130GC-8EU
- μPD703130GC-8EU-A





PIN NAMES

A0 to A23: Address bus P20, P22 to P27: Port 2 ANIO to ANI3: Port 3 Analog input P33, P34: AVDD: Analog power supply P50 to P57: Port 5 AVREF: Analog reference voltage Port 6 P60 to P67: AVss: Analog ground P70 to P73: Port 7 BCYST: Bus cycle start timing P80, P83 to P85: Port 8 CKSEL: Clock generator operating mode select P90 to P97: Port 9 CLKOUT: Clock output P100, P102: Port 10

CS0, CS3 to CS5: Chip select

CV_{DD}: Clock generator power supply CVss: Clock generator ground

D0 to D15: Data bus

DMAAK0 to DMAAK3: DMA acknowledge DMARQ0 to DMARQ3: DMA request HLDAK: Hold acknowledge HLDRQ: Hold request

HV_{DD}: Power supply for external pins INTP100 to INTP103,: Interrupt request from peripherals

INTP110 to INTP113,

INTP130

IORD: I/O read strobe **IOWR**: I/O write strobe

LCAS: Lower column address strobe

LWR: Lower write strobe

MODE0, MODE2: Mode

NMI: Non-maskable interrupt request

OE: Output enable P00, P02, P04 to P07: Port 0

P10, P12, P14 to P17: Port 1

Port X PX6, PX7:

RAS3 to RAS5: Row address strobe

RD: Read **RESET**: Reset

Receive data RXD0, RXD1: SCK0, SCK1: Serial clock SI0, SI1: Serial input SO0, SO1: Serial output TCLR10 to TCLR12: Timer clear TI13: Timer input Timer output

TO100, TO110:

TO120

TXD0, TXD1: Transmit data

UCAS: Upper column address strobe

ŪWR: Upper write strobe

V_{DD}: Power supply for internal unit

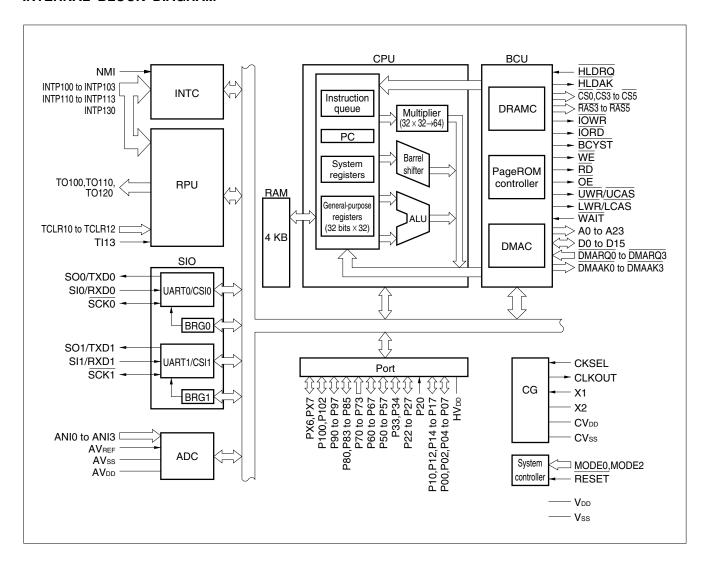
Vss: Ground WAIT: Wait WE: Write enable

X1, X2:

Crystal



INTERNAL BLOCK DIAGRAM



CONTENTS

1.	DIFFERENCES BETWEEN V850E/MS2 AND V850E/MS1	6
2.	PIN FUNCTIONS	
	2.1 Port Pins	
	2.2 Non-Port Pins	9
	2.3 Pin I/O Circuits and Recommended Connection of Unused Pins	11
3.	ELECTRICAL SPECIFICATIONS	14
4.	PACKAGE DRAWING	68
5.	RECOMMENDED SOLDERING CONDITIONS	69



1. DIFFERENCES BETWEEN V850E/MS2 AND V850E/MS1

Product Name	V850E/MS2	V850E/MS1			
ltem μPD703130		μPD703100-33	μPD703102-33		
Internal ROM	None	None	128 KB (mask ROM)		
Maximum operating frequency	33 MHz	33 MHz			
Memory space					
Chip select output	4 spaces	8 spaces			
Interrupt function					
I/O lines	Input: 5, I/O: 52	Input: 9, I/O: 114			
Timer	16-bit timer/event counter: 4 channels 16-bit timer: 2 channels	16-bit timer/event counter 16-bit timer: 2 channels	: 6 channels		
Serial interface	CSI/UART: 2 channels Dedicated baud rate generator: 2 channels	CSI: 2 channels CSI/UART: 2 channels Dedicated baud rate gener	ator: 3 channels		
A/D converter	10-bit resolution × 4 channels	10-bit resolution × 8 channels			
Package	100-pin plastic LQFP (fine-pitch) (14 × 14) 144-pin plastic LQFP (fine-pitch) (20 × 20				
Other Noise tolerance and noise radiation will differ due to differences in circuit scale and mask layout.					



2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0	TO100
P02		6-bit I/O port Input/output can be specified in 1-bit units.	TCLR10
P04		impuvoutput can be specified in 1-bit units.	INTP100/DMARQ0
P05			INTP101/DMARQ1
P06			INTP102/DMARQ2
P07			INTP103/DMARQ3
P10	I/O	I/O Port 1	TO110
P12		6-bit I/O port	TCLR11
P14		Input/output can be specified in 1-bit units.	INTP110/DMAAK0
P15			INTP111/DMAAK1
P16			INTP112/DMAAK2
P17			INTP113/DMAAK3
P20	Input	Port 2	NMI
P22	I/O	P20 is an input only port.	TXD0/SO0
P23		When a valid edge is input, this pin operates as NMI input. Also, bit 0 of the P2 register indicates the NMI input status. P22 to P27 are 6-bit I/O port.	RXD0/SI0
P24			SCK0
P25		Input/output can be specified in 1-bit units.	TXD1/SO1
P26			RXD1/SI1
P27			SCK1
P33	I/O	Port 3	TI13
P34		2-bit I/O port Input/output can be specified in 1-bit units.	INTP130
P50 to P57	I/O	Port 5 8-bit I/O port Input/output can be specified in 1-bit units.	D8 to D15
P60 to P67	I/O	Port 6 8-bit I/O port Input/output can be specified in 1-bit units.	A16 to A23
P70 to P73	Input	Port 7 4-bit input only port	ANI0 to ANI3
P80	I/O	Port 8	CS0
P83		4-bit I/O port Input/output can be specified in 1-bit units.	CS3/RAS3
P84		impuroutput carr be specified in 1-bit utilits.	CS4/RAS4/IOWR
P85			CS5/RAS5/IORD

(2/2)

Pin Name	I/O	Function	Alternate Function
P90	I/O	Port 9	LCAS/LWR
P91]	8-bit I/O port Input/output can be specified in 1-bit units.	UCAS/UWR
P92		inpuroutput can be specified in 1-bit units.	RD
P93			WE
P94			BCYST
P95			ŌE
P96			HLDAK
P97			HLDRQ
P100	I/O	Port 10	TO120
P102		2-bit I/O port Input/output can be specified in 1-bit units.	TCLR12
PX6	I/O	Port X	WAIT
PX7		2-bit I/O port Input/output can be specified in 1-bit units.	CLKOUT



2.2 Non-Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
TO100	Output	Pulse signal output for timers 10 to 12	P00
TO110			P10
TO120			P100
TCLR10	Input	External clear signal input for timers 10 to 12	P02
TCLR11			P12
TCLR12			P102
TI13	Input	External count clock input for timer 13	P33
INTP100	Input	External maskable interrupt request input, shared as external capture	P04/DMARQ0
INTP101		trigger input for timer 10	P05/DMARQ1
INTP102			P06/DMARQ2
INTP103			P07/DMARQ3
INTP110	Input	External maskable interrupt request input, shared as external capture	P14/DMAAK0
INTP111		trigger input for timer 11	P15/DMAAK1
INTP112			P16/DMAAK2
INTP113			P17/DMAAK3
INTP130	Input	External maskable interrupt request input, shared as external capture trigger input for timer 13	P34
SO0	Output	Serial transmit data output (3-wire) for CSI0 and CSI1	P22/TXD0
SO1			P25/TXD1
SI0	Input	Serial receive data input (3-wire) for CSI0 and CSI1	P23/RXD0
SI1			P26/RXD1
SCK0	I/O	Serial clock I/O (3-wire) for CSI0 and CSI1	P24
SCK1			P27
TXD0	Output	Serial transmit data output for UART0 and UART1	P22/SO0
TXD1			P25/SO1
RXD0	Input	Serial receive data input for UART0 and UART1	P23/SI0
RXD1			P26/SI1
D0 to D7	I/O	16-bit data bus for external memory	_
D8 to D15			P50 to P57
A0 to A15	Output	24-bit address bus for external memory	
A16 to A23			P60 to P67
LWR	Output	Lower byte write-enable signal output for external data bus	P90/LCAS
UWR	Output	Higher byte write-enable signal output for external data bus	P91/UCAS
RD	Output	Read strobe signal output for external data bus	P92
WE	Output	Write enable signal output for DRAM	P93
ŌE	Output	Output enable signal output for DRAM	P95



(2/2)

Pin Name	I/O	Function	Alternate Function
LCAS	Output	Column address strobe signal output for DRAM's lower data	P90/LWR
UCAS	Output	Column address strobe signal output for DRAM's higher data	P91/UWR
RAS3	Output	Row address strobe signal output for DRAM	P83/CS3
RAS4			P84/CS4/IOWR
RAS5]		P85/CS5/IORD
BCYST	Output	Strobe signal output indicating start of bus cycle	P94
CS0	Output	Chip select signal output	P80
CS3			P83/RAS3
CS4			P84/RAS4/IOWR
CS5]		P85/RAS5/IORD
WAIT	Input	Control signal input for inserting waits in bus cycle	PX6
ĪOWR	Output	DMA write strobe signal output	P84/RAS4/CS4
IORD	Output	DMA read strobe signal output	P85/RAS5/CS5
DMARQ0 to	Input	DMA request signal input	P04/INTP100 to P07/INTP103
DMAAK0 to	Output	DMA acknowledge signal output	P14/INTP110 to P17/INTP113
HLDAK	Output	Bus hold acknowledge output	P96
HLDRQ	Input	Bus hold request input	P97
ANI0 to ANI3	Input	Analog input to A/D converter	P70 to P73
NMI	Input	Non-maskable interrupt request input	P20
CLKOUT	Output	System clock output	PX7
CKSEL	Input	Input for specifying clock generator's operation mode	_
MODE0, MODE2	Input	Specify operation modes	-
RESET	Input	System reset input	-
X1	Input	Connecting resonator for system clock. Input is via X1 when using an	-
X2	-	external clock.	-
AVREF	Input	Reference voltage input for A/D converter	-
AV _{DD}	_	Positive power supply for A/D converter	-
AVss	_	Ground potential for A/D converter	
CV _{DD}	-	Positive power supply for dedicated clock generator	-
CVss	_	Ground potential for dedicated clock generator	-
V _{DD}	_	Positive power supply (power supply for internal units)	-
HV _{DD}	_	Positive power supply (power supply for external pins)	-
Vss	_	Ground potential	_



2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-1 shows the I/O circuit type of each pin and recommended connection of unused pins. Figure 2-1 shows the various circuit types using partially abridged diagrams.

When connecting to V_{DD} or V_{SS} via a resistor, a resistance value in the range of 1 to 10 $k\Omega$ is recommended.

Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (1/2)

Pin	I/O Circuit Type	Recommended Connection of Unused Pins
P00/TO100	5	Input: Independently connect to HVDD or Vss via a resistor
P02/TCLR10		Output: Leave open
P04/INTP100/DMARQ0 to P07/INTP103/DMARQ3		
P10/TO110		
P12/TCLR11		
P14/INTP110/DMAAK0 to P17/INTP113/DMAAK3		
P20/NMI	2	Connect directly to Vss
P22/TXD0/SO0	5	Input: Independently connect to HVDD or Vss via a resistor
P23/RXD0/SI0		Output: Leave open
P24/SCK0		
P25/TXD1/SO1		
P26/RXD1/SI1		
P27/SCK1		
P33/TI13		
P34/INTP130		
P50/D8 to P57/D15		
P60/A16 to P67/A23		
P70/ANI0 to P73/ANI3	9	Connect directly to Vss
P80/CS0, to P83/CS3/RAS3	5	Input: Independently connect to HV _{DD} or V _{SS} via a resistor
P84/CS4/RAS4/IOWR, P85/CS5/RAS5/IORD		Output: Leave open
P90/LCAS/LWR		
P91/UCAS/UWR		
P92/RD		
P93/WE		
P94/BCYST		
P95/OE		
P96/HLDAK		
P97/HLDRQ		
P100/TO120		
P102/TCLR12		

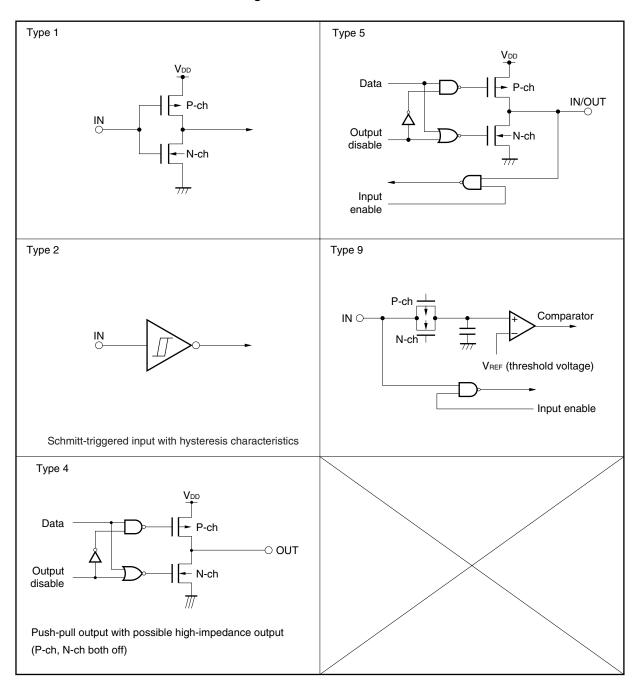


Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (2/2)

Pin	I/O Circuit Type	Recommended Connection of Unused Pins
PX6/WAIT	5	Input: Independently connect to HVDD or Vss via a resistor
PX7/CLKOUT		Output: Leave open
A0 to A15	4	-
D0 to D7	5	
CKSEL	1	
RESET	2	
MODE0, MODE2		
AVREF, AVSS	-	Connect directly to Vss
AVDD	_	Connect directly to HVDD



Figure 2-1. Pin I/O Circuits



Caution Replace VDD by HVDD when referencing the circuit diagrams shown above.

3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (TA = 25°C)

Parameter	Symbol	Condition		Rating	Unit		
Power supply voltage	V _{DD} V _{DD} pin		V _{DD} pin		٧		
	HV _{DD}	HV _{DD} pin, HV _{DD} ≥ V _{DI})	-0.5 to +7.0	٧		
	CV _{DD}	CV _{DD} pin		-0.5 to +4.6	٧		
	CVss	CVss pin		-0.5 to +0.5	V		
	AV _{DD}	AV _{DD} pin		-0.5 to HV _{DD} + 0.5 ^{Note}	V		
	AVss	AVss pin		-0.5 to +0.5	V		
Input voltage	Vı	Except X1 pin -0.5 to HV		-0.5 to HV _{DD} + 0.5 ^{Note}	V		
Clock input voltage	Vĸ	X1, V _{DD} = 3.0 to 3.6 V		-0.5 to V _{DD} + 1.0 ^{Note}	V		
Output current, low	loL	1 pin		1 pin		4.0	mA
		Total of all pins	Total of all pins		mA		
Output current, high	Іон	1 pin		-4.0	mA		
		Total of all pins		-100	mA		
Output voltage	Vo	HV _{DD} = 5.0 V ±10%		-0.5 to HV _{DD} + 0.5 ^{Note}	V		
Analog input voltage	VIAN	P70/ANI0 to P73	AVDD > HVDD	-0.5 to HV _{DD} + 0.5 ^{Note}	V		
		pins	HV _{DD} ≥ AV _{DD}	-0.5 to AV _{DD} + 0.5 ^{Note}	٧		
A/D converter reference input	AVREF	$AV_{DD} > HV_{DD}$ $HV_{DD} \ge AV_{DD}$		-0.5 to HV _{DD} + 0.5 ^{Note}	٧		
voltage				-0.5 to AV _{DD} + 0.5 ^{Note}	V		
Operating ambient temperature	Та			-40 to +85	°C		
Storage temperature	T _{stg}			-60 to +150	°C		

Note Be sure not to exceed the absolute maximum ratings (MAX. value) of the each power supply voltage.

Cautions 1. Do not make direct connections of the output (or input/output) pins of the IC product with each other, and also avoid direct connections to VDD, VCC, or GND. However, the open drain pins or the open collector pins can be directly connected to each other. A direct connection can also be made for an external circuit designed with timing specifications that prevent conflicting output from pins subject to a high-impedance state.

- 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
 - The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.



Capacitance (TA = 25°C, VDD = HVDD = CVDD = Vss = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Сі	fc = 1 MHz			15	pF
I/O capacitance	Сю	Unmeasured pins returned to 0 V.			15	pF
Output capacitance	Co				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (fx)	Operating Ambient Temperature (T _A)	Power Supply Voltage (Vdd, HVdd)
Direct mode	10 to 33 MHz ^{Note 1}	−40 to +85°C	$V_{DD} = 3.0 \text{ to } 3.6 \text{ V},$
PLL mode ^{Note 2}	20 to 33 MHz Note 3	−40 to +85°C	$HVDD = 5.0 V \pm 10\%$

Notes 1. Set the input clock frequency used in direct mode to 20 to 66 MHz.

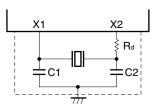
- 2. The internal operating clock frequency in PLL mode is the value for $5\times$ operation. When used for $1\times$ or $1/2\times$ operation as set by the CKDIVn (n = 0, 1) bit of the CKC register, operation at a frequency of 20 MHz or less is possible.
- 3. Set the input clock frequency used in PLL mode to 4.0 to 6.6 MHz.

15

Recommended Oscillator

(a) Ceramic resonator

(i) Murata Mfg. Co., Ltd. ($T_A = -40 \text{ to } +85^{\circ}\text{C}$)



Manu- Part Number facturer	Part Number	Oscillation Frequency	Recommer	nded Circuit	Constant	Oscillation Voltage Range		Oscillation Stabilization
	fxx (MHz)	C1 (pF)	C2 (pF)	R _d (kΩ)	MIN. (V)	MAX. (V)	Time (MAX.) Tost (ms)	
Murata Mfg.	CSTS400MG06 ^{Note} (CSTLS4M00G56-B0)	4.0	On-chip	On-chip	0	3.0	3.6	0.6
	CSTCR4M00G55-R0	4.0	On-chip	On-chip	0	3.0	3.6	0.6
	CSTS0500MG06 ^{Note} (CSTLS5M00G56-B0)	5.0	On-chip	On-chip	0	3.0	3.6	0.6
	CSTCR5M00G55-R0	5.0	On-chip	On-chip	0	3.0	3.6	0.6
	CSTS066MG06 ^{Note} (CSTLS6M60G56-B0)	6.6	On-chip	On-chip	0	3.0	3.6	0.6
	CSTCR6M60G55-R0	6.6	On-chip	On-chip	0	3.0	3.6	0.6

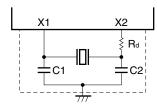
Note The part number will be changed to the part number in the parentheses from June 2001.

Cautions 1. Connect the oscillator as close to the X1 and X2 pins as possible.

- 2. Do not wire any other signal lines in the area enclosed by broken lines.
- 3. Sufficiently evaluate the matching between the μ PD703130 and the resonator.



(ii) TDK $(T_A = -40 \text{ to } +85^{\circ}\text{C})$

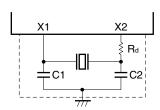


Manu- facturer	Part Number	Oscillation Frequency	Recomme	ended Circuit Co	onstant		llation Range	Oscillation Stabilization Time
		fxx (MHz)	C1 (pF)	C2 (pF)	R _d (kΩ)	MIN. (V)	MAX. (V)	(MAX.) Tost (ms)
TDK	FCR4.0MC5	4.0	On-chip	On-chip	0	3.0	3.6	0.73
	FCR5.0MC5	5.0	On-chip	On-chip	0	3.0	3.6	0.68
	FCR6.0MC5	6.0	On-chip	On-chip	0	3.0	3.6	0.58

Cautions 1. Connect the oscillator as closely to the X1 and X2 pins as possible.

- 2. Do not wire any other signal lines in the area enclosed by broken lines.
- 3. Sufficiently evaluate the matching between the μ PD703130 and the resonator.

(iii) Kyocera Corporation ($T_A = -20 \text{ to } +80^{\circ}\text{C}$)



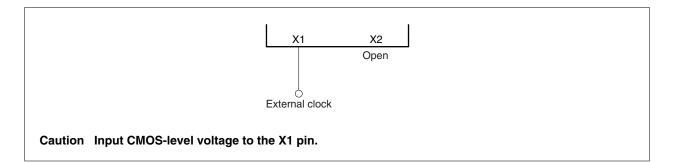
Туре	Part Number	Oscillation Frequency fxx (MHz)	Recomme	ended Circuit (Constant		llation e Range	Oscillation Stabilization Time	
			C1 (pF)	C2 (pF)	R _d (kΩ)	MIN. (V)	MAX. (V)	(MAX.) Tost (ms)	
Lead	KBR-4.0MKC	4.0	On-chip	On-chip	0	3.0	3.6	0.80	
	KBR-5.0MKC	5.0	On-chip	On-chip	0	3.0	3.6	0.70	
	KBR-6.0MKC	6.0	On-chip	On-chip	0	3.0	3.6	0.76	
SMD	PBRC4.00HR	4.0	On-chip	On-chip	0	3.0	3.6	0.80	
	PBRC5.00HR	5.0	On-chip	On-chip	0	3.0	3.6	0.70	
	PBRC6.00HR	6.0	On-chip	On-chip	0	3.0	3.6	0.76	

Cautions 1. Connect the oscillator as close to the X1 and X2 pins as possible.

- 2. Do not wire any other signal lines in the area enclosed by broken lines.
- 3. Sufficiently evaluate the matching between the μ PD703130 and the resonator.

17

(b) External clock input $(T_A = -40 \text{ to } +85^{\circ}\text{C})$





DC Characteristics (T_A = -40 to +85°C, V_{DD} = CV_{DD} = 3.0 to 3.6 V, HV_{DD} = 5.0 ± 10 %, V_{SS} = 0 V)

Paran	neter	Symbol	Cond	lition	MIN.	TYP.	MAX.	Unit
Input voltage, h	igh	VIH	Except Note 1		2.2		HV _{DD} + 0.3	V
			Note 1		0.8HV _{DD}		HV _{DD} + 0.3	V
Input voltage, lo	w	VIL	Except Note 1	and Note 2	-0.5		+0.8	V
			Note 1		-0.5		0.2HV _{DD}	V
Clock input volta	Clock input voltage, high		X1 pin		0.8Vpp		VDD + 0.3	V
Clock input volta	age, low	VxL	X1 pin		-0.3		0.15V _{DD}	V
Schmitt-triggere	ed input	HV⊤⁺	Note 1, rising e	dge		3.0		V
threshold voltag	je	HV⊤⁻	Note 1, falling e	edge		2.0		V
Output voltage,	high	Vон	Iон = -2.5 mA		0.7HV _{DD}			V
			IoH = −100 μA		HV _{DD} - 0.4			V
Output voltage,	low	Vol IoL = 2.5 mA					0.45	V
Input leakage co	urrent, high	Ішн	VI = HVDD, exc	ept Note 2			10	μΑ
Input leakage co	urrent, low	ILIL	Vı = 0 V, excep	VI = 0 V, except Note 2			-10	μΑ
Output leakage	current, high	Ісон	Vo = HVDD				10	μΑ
Output leakage	current, low	ILOL	Vo = 0 V				-10	μΑ
Power supply	Normal	IDD1		V _{DD} + CV _{DD}		2.0 × fx	3.0 × fx	mA
current	mode			HV _{DD}		1.5 × fx	2.5 × fx	mA
	HALT mode	IDD2		V _{DD} + CV _{DD}		1.4 × fx	1.8 × fx	mA
				HV _{DD}		$0.7 \times fx$	1.2 × fx	mA
	IDLE mode	IDD3		V _{DD} + CV _{DD}		1.4	2.5	mA
				HV _{DD}		20	100	μΑ
	STOP mode	IDD4		V _{DD} + CV _{DD}		20	100	μΑ
				HV _{DD}		10	50	μΑ

Notes 1. P20/NMI, MODE0, MODE2, CKSEL, RESET

2. When the P70/ANI0 to P73/ANI3 pins are used as analog input.

Remarks 1. TYP. values are reference values for when $T_A = 25$ °C, $V_{DD} = CV_{DD} = 3.3$ V, and $HV_{DD} = 5.0$ V.

2. Direct mode: fx = 10 to 33 MHz PLL mode: fx = 20 to 33 MHz

3. The unit for fx is MHz.

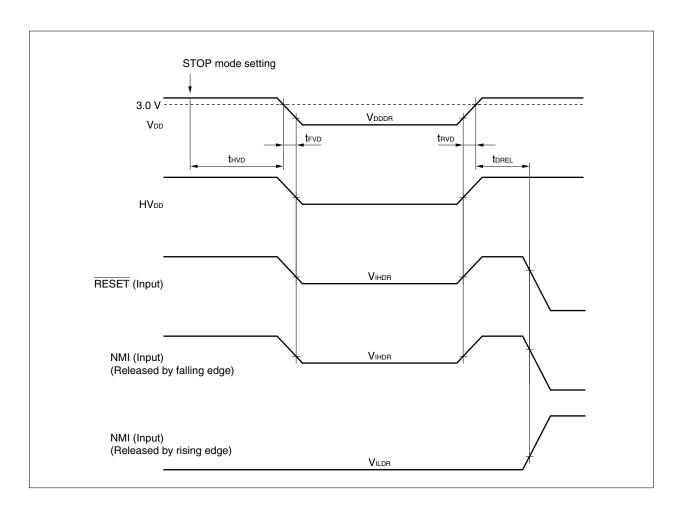
19



Data Hold Characteristics ($T_A = -40 \text{ to } +85^{\circ}\text{C}$)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data hold voltage	VDDDR	STOP mode, VDD = VDDDR	1.5		3.6	V
	HVDDDR	STOP mode, HVDD = HVDDDR	VDDDR		5.5	V
Data hold current	IDDDR	V _{DD} = V _{DDDR}		30	150	μΑ
Power supply voltage rise time	trvd		200			μs
Power supply voltage fall time	tFVD		200			μs
Power supply voltage hold time (from STOP mode setting)	thvd		0			ms
STOP mode release signal input time	tDREL		0			ns
Data hold input voltage, high	VIHDR	P20/NMI, MODE0, MODE2, CKSEL, RESET	0.8HVDDDR		HVDDDR	V
Data hold input voltage, low	VILDR	P20/NMI, MODE0, MODE2, CKSEL, RESET	0		0.2HVDDDR	V

Remark TYP. values are reference values for when $T_A = 25^{\circ}C$.

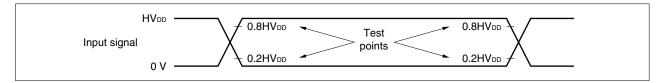




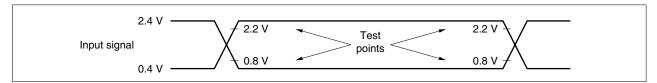
AC Characteristics (T_A = -40 to +85°C, V_{DD} = CV_{DD} = 3.0 to 3.6 V, HV_{DD} = $5.0 \pm 10\%$, Vss = 0 V, output pin load capacitance: C_L = 50 pF)

AC Test Input Test Points

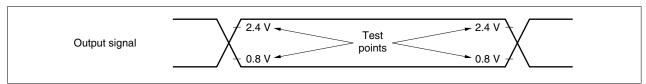
(a) P20/NMI, MODE0, MODE2, CKSEL, RESET



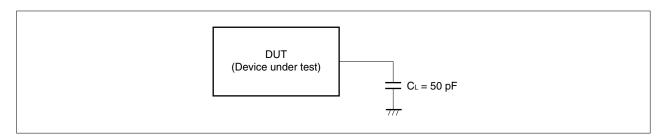
(b) Pins other than those listed in (a) above



AC Test Output Test Points



Load Condition



Caution In cases where the load capacitance is greater than 50 pF due to the circuit configuration, insert a buffer or other element to reduce the device's load capacitance 50 pF.

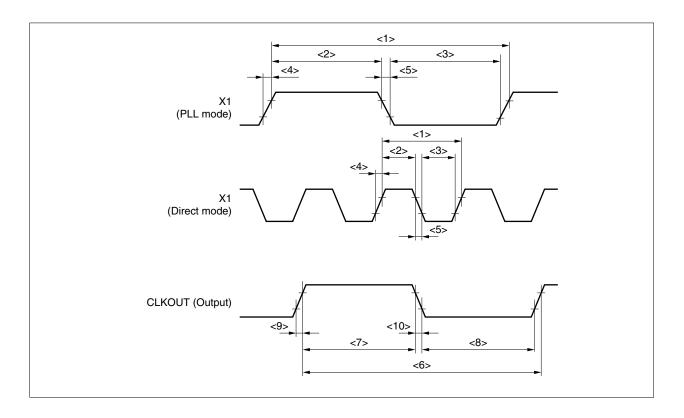
21



(1) Clock timing

Parameter	Syr	nbol	Condition	MIN.	MAX.	Unit
X1 input cycle	<1>	tcyx	Direct mode	15	50	ns
			PLL mode	150	250	ns
X1 input high-level width	<2>	twxн	Direct mode	5		ns
			PLL mode	50		ns
X1 input low-level width	<3>	twx∟	Direct mode	5		ns
			PLL mode	50		ns
X1 input rise time	<4>	txR	Direct mode		4	ns
			PLL mode		10	ns
X1 input fall time	<5>	txF	Direct mode		4	ns
			PLL mode		10	ns
CLKOUT output cycle	<6>	t cyk		30	100	ns
CLKOUT high-level width	<7>	twкн		0.5T – 7		ns
CLKOUT low-level width	<8>	twĸ∟		0.5T – 4		ns
CLKOUT rise time	<9>	t kR			5	ns
CLKOUT fall time	<10>	t kF			5	ns

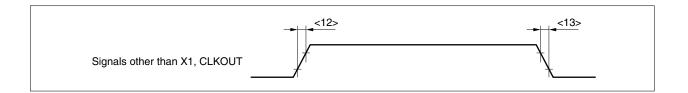
Remark $T = t_{CYK}$





(2) Output waveform (other than X1, CLKOUT)

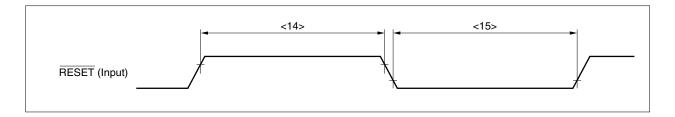
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	<12>	tor			10	ns
Output fall time	<13>	tor			10	ns



(3) Reset timing

Parameter	Syn	nbol	Condition	MIN.	MAX.	Unit
RESET high-level width	<14>	twrsh		500		ns
RESET low-level width	<15>	twrsl	When power supply is on, and STOP mode has been released	500 + Tos		ns
			Other than when power supply is on, and STOP mode has been released	500		ns

Remark Tos: Oscillation stabilization time





(4) SRAM, external ROM, or external I/O access timing

(a) Access timing (SRAM, external ROM, or external I/O) (1/2)

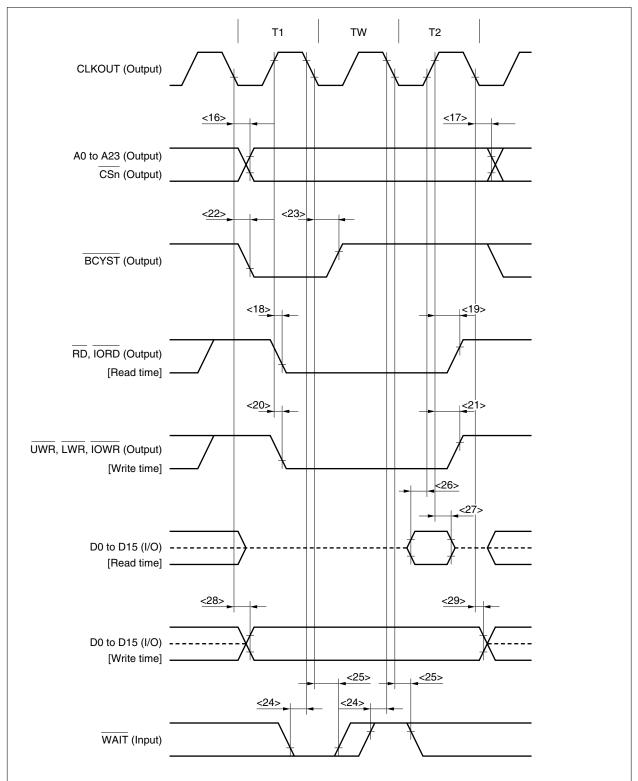
Parameter	Syr	nbol	Condition	MIN.	MAX.	Unit
Address, CSn output delay time (from CLKOUT ↓)	<16>	t dka		2	10	ns
Address, CSn output hold time (from CLKOUT ↓)	<17>	tнка		2	10	ns
RD, IORD ↓ delay time (from CLKOUT ↑)	<18>	t DKRDL		2	14	ns
RD, IORD ↑ delay time (from CLKOUT ↑)	<19>	tнкпон		2	14	ns
UWR, LWR, IOWR ↓ delay time (from CLKOUT ↑)	<20>	t DKWRL		2	10	ns
UWR, LWR, IOWR ↑ delay time (from CLKOUT ↑)	<21>	thkwrh		2	10	ns
BCYST ↓ delay time (from CLKOUT ↓)	<22>	t DKBSL		2	10	ns
BCYST ↑ delay time (from CLKOUT ↓)	<23>	t HKBSH		2	10	ns
WAIT setup time (to CLKOUT ↓)	<24>	t swk		15		ns
\overline{WAIT} hold time (from CLKOUT \downarrow)	<25>	thkw		2		ns
Data input setup time (to CLKOUT ↑)	<26>	tskid		18		ns
Data input hold time (from CLKOUT ↑)	<27>	thkid		2		ns
Data output delay time (from CLKOUT ↓)	<28>	t DKOD		2	10	ns
Data output hold time (from CLKOUT ↓)	<29>	tнкор		2	10	ns

Remarks 1. Maintain at least one of the data input hold times thkid and thkid.

2. n = 0, 3 to 5



(a) Access timing (SRAM, external ROM, or external I/O) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.

- 2. The broken lines indicate high impedance.
- **3.** n = 0, 3 to 5



(b) Read timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Syn	nbol	Condition	MIN.	MAX.	Unit
Data input setup time (to address)	<30>	t said			(1.5 + w _D + w)T – 28	ns
Data input setup time (to RD)	<31>	tsrdid			(1 + w _D + w)T - 32	ns
RD, IORD low-level width	<32>	twrdl		(1 + w _D + w)T – 10		ns
RD, IORD high-level width	<33>	twrdh		T – 10		ns
	<34>	t DARD		0.5T – 10		ns
Delay time from RD, IORD ↑ to address	<35>	t drda		(0.5 + i)T - 10		ns
Data input hold time (from RD, IORD ↑)	<36>	throid		0		ns
Delay time from RD, IORD ↑ to data output	<37>	tordod		(0.5 + i)T - 10		ns
WAIT setup time (to address)	<38>	tsaw	Note		T – 25	ns
WAIT setup time (to BCYST ↓)	<39>	tsssw	Note		T – 25	ns
WAIT hold time (from BCYST ↑)	<40>	tнвsw	Note	0		ns

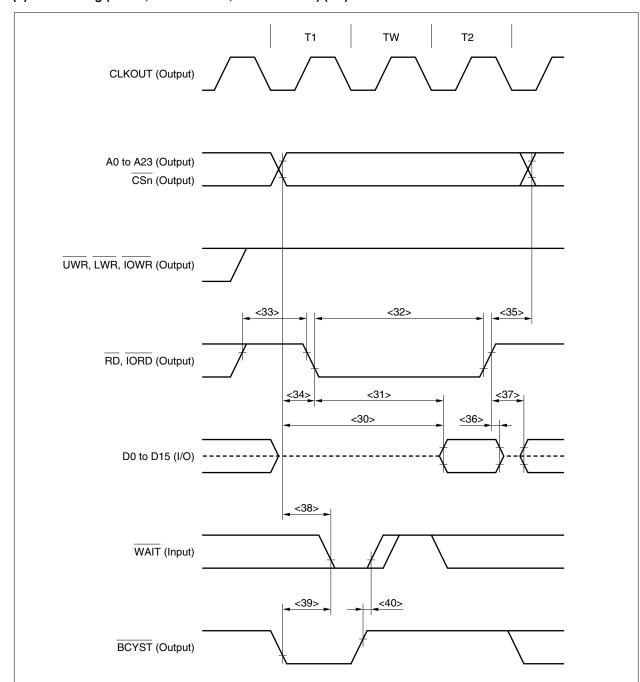
Note For first WAIT sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

- 2. w: The number of waits due to $\overline{\text{WAIT}}$.
- 3. wb: The number of waits due to the DWC1 and DWC2 registers.
- **4.** i: The number of idle states that are inserted when a write cycle follows a read cycle.
- 5. Maintain at least one of the data input hold times, thkid or throld.
- **6.** n = 0, 3 to 5



(b) Read timing (SRAM, external ROM, or external I/O) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.

- 2. The broken lines indicate high impedance.
- **3.** n = 0, 3 to 5



(c) Write timing (SRAM, external ROM, or external I/O) (1/2)

Parameter	Syn	nbol	Condition	MIN.	MAX.	Unit
WAIT setup time (to address)	<38>	tsaw	Note		T – 25	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}} \downarrow$)	<39>	tsssw	Note		T – 25	ns
WAIT hold time (from BCYST ↑)	<40>	tнвsw	Note	0		ns
Delay time from address, CSn to UWR, LWR, IOWR ↓	<41>	tdawr		0.5T – 10		ns
Address setup time (to UWR, LWR, IOWR ↑)	<42>	tsawr		(1.5 + wd + w)T - 10		ns
Delay time from ŪWR, ŪWR, ĪOWR ↑ to address	<43>	towra		0.5T – 10		ns
UWR, LWR, IOWR high-level width	<44>	twwrh		T – 10		ns
UWR, LWR, IOWR low-level width	<45>	twwrL		(1 + wp + w)T - 10		ns
Data output setup time (to UWR, LWR, IOWR ↑)	<46>	tsodwr		(1.5 + wd + w)T - 10		ns
Data output hold time (from UWR, LWR, IOWR ↑)	<47>	thwrod		0.5T – 10		ns

Note For first WAIT sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

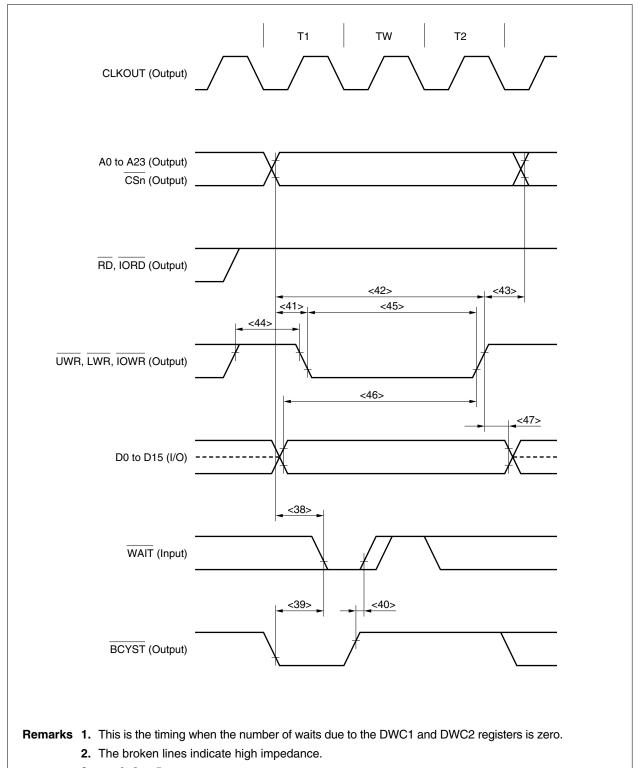
2. w: The number of waits due to $\overline{\text{WAIT}}$.

3. wb: The number of waits due to the DWC1 and DWC2 registers.

4. n = 0, 3 to 5



(c) Write timing (SRAM, external ROM, or external I/O) (2/2)



3. n = 0, 3 to 5



(d) DMA flyby transfer timing (SRAM \rightarrow external I/O transfer) (1/2)

Parameter	Syn	nbol	Condition	MIN.	MAX.	Unit
WAIT setup time (to CLKOUT ↓)	<24>	t swĸ		15		ns
\overline{WAIT} hold time (from CLKOUT \downarrow)	<25>	tнкw		2		ns
RD low-level width	<32>	twrdl		(1 + WD + WF + W)T - 10		ns
RD high-level width	<33>	twrdh		T – 10		ns
Delay time from address, $\overline{\text{CSn}}$ to $\overline{\text{RD}}$ \downarrow	<34>	tdard		0.5T – 10		ns
Delay time from RD ↑ to address	<35>	t DRDA		(0.5 + i)T - 10		ns
Delay time from \overline{RD} \uparrow to data output	<37>	tordod		(0.5 + i)T - 10		ns
WAIT setup time (to address)	<38>	tsaw	Note		T – 25	ns
WAIT setup time (to BCYST ↓)	<39>	tsssw	Note		T – 25	ns
WAIT hold time (from BCYST ↑)	<40>	tнвsw	Note	0		ns
Delay time from address to $\overline{\text{IOWR}} \downarrow$	<41>	tdawr		0.5T – 10		ns
Address setup time (to IOWR ↑)	<42>	tsawr		(1.5 + wd + w)T - 10		ns
Delay time from IOWR ↑ to address	<43>	t dwra		0.5T – 10		ns
IOWR high-level width	<44>	twwrh		T – 10		ns
IOWR low-level width	<45>	twwnL		(1 + wp + w)T – 10		ns
Delay time from IOWR ↑ to RD ↑	<48>	towrrd	w _F = 0	0		ns
			WF = 1	T – 10		ns
Delay time from $\overline{\mathrm{DMAAKm}} \downarrow$ to $\overline{\mathrm{IOWR}} \downarrow$	<49>	tddawr		0.5T – 10		ns
Delay time from IOWR ↑ to DMAAKm ↑	<50>	t DWRDA		(0.5 + w⊧)T − 10		ns

Note For first WAIT sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

2. w: The number of waits due to $\overline{\text{WAIT}}$.

3. wp: The number of waits due to the DWC1 and DWC2 registers.

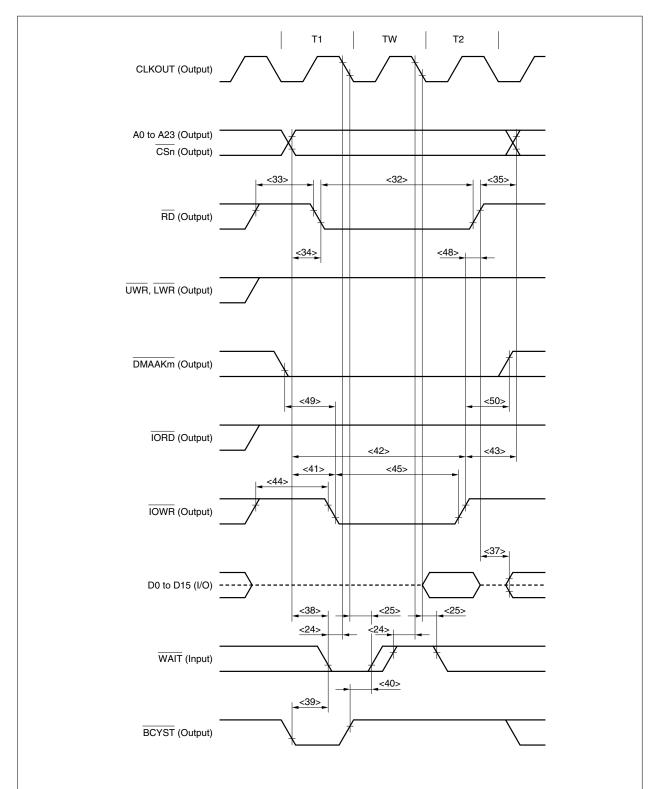
4. WF: The number of waits that are inserted for a source-side access during a DMA flyby transfer.

5. i: The number of idle states that are inserted when a write cycle follows a read cycle.

6. n = 0, 3 to 5, m = 0 to 3



(d) DMA flyby transfer timing (SRAM \rightarrow external I/O transfer) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and $w_F = 0$.

- 2. The broken lines indicate high impedance.
- **3.** n = 0, 3 to 5, m = 0 to 3



(e) DMA flyby transfer timing (external I/O \rightarrow SRAM transfer) (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
WAIT setup time (to CLKOUT ↓)	<24>	t swĸ		15		ns
WAIT hold time (from CLKOUT ↓)	<25>	thkw		2		ns
IORD low-level width	<32>	twrdl		(1 + WD + WF + W)T - 10		ns
IORD high-level width	<33>	twrdh		T – 10		ns
Delay time from address, CSn to IORD ↓	<34>	t DARD		0.5T - 10		ns
Delay time from IORD ↑ to address	<35>	t DRDA		(0.5 + i)T - 10		ns
Delay time from IORD ↑ to data output	<37>	tordod		(0.5 + i)T - 10		ns
WAIT setup time (to address)	<38>	tsaw	Note		T – 25	ns
WAIT setup time (to BCYST ↓)	<39>	tsssw	Note		T – 25	ns
WAIT hold time (from BCYST ↑)	<40>	tнвsw	Note	0		ns
Delay time from address to $\overline{\text{UWR}}$, $\overline{\text{LWR}} \downarrow$	<41>	tdawr		0.5T – 10		ns
Address setup time (to UWR, LWR↑)	<42>	tsawr		(1.5 + wD + w)T - 10		ns
Delay time from UWR, LWR to address	<43>	towra		0.5T - 10		ns
UWR, LWR high-level width	<44>	twwrh		T – 10		ns
UWR, LWR low-level width	<45>	twwnL		(1 + wD + w)T – 10		ns
Delay time from UWR, LWR↑ to IORD↑	<48>	towrrd	w _F = 0	0		ns
			WF = 1	T – 10		ns
Delay time from DMAAKm ↓ to IORD ↓	<51>	tddard		0.5T – 10		ns
Delay time from IORD ↑ to DMAAKm ↑	<52>	tordda		0.5T – 10		ns

Note For first $\overline{\text{WAIT}}$ sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

2. w: The number of waits due to \overline{WAIT} .

3. wb: The number of waits due to the DWC1 and DWC2 registers.

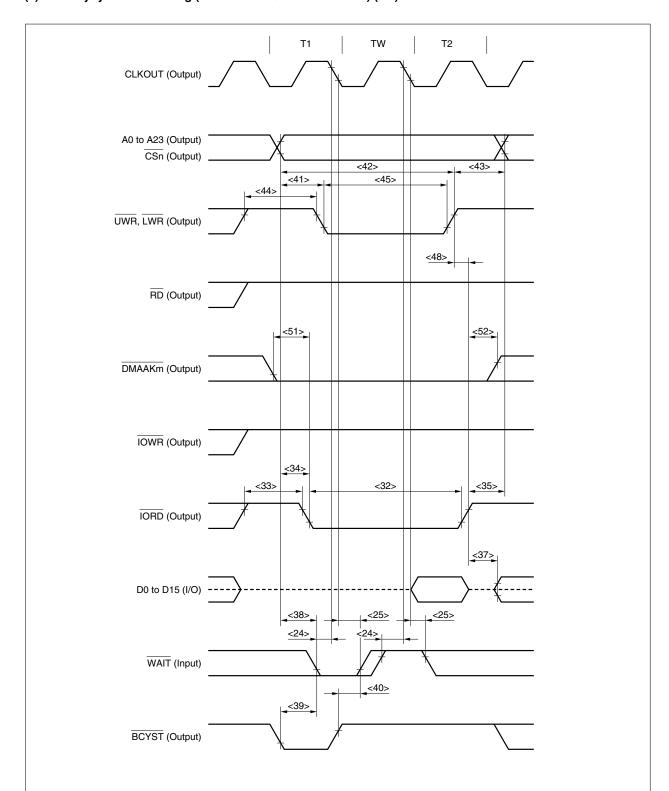
4. WF: The number of waits that are inserted for a source-side access during a DMA flyby transfer.

5. i: The number of idle states that are inserted when a write cycle follows a read cycle.

6. n = 0, 3 to 5, m = 0 to 3



(e) DMA flyby transfer timing (external I/O \rightarrow SRAM transfer) (2/2)



Remarks 1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and $w_F = 0$.

- 2. The broken lines indicate high impedance.
- **3.** n = 0, 3 to 5, m = 0 to 3



(5) Page ROM access timing (1/2)

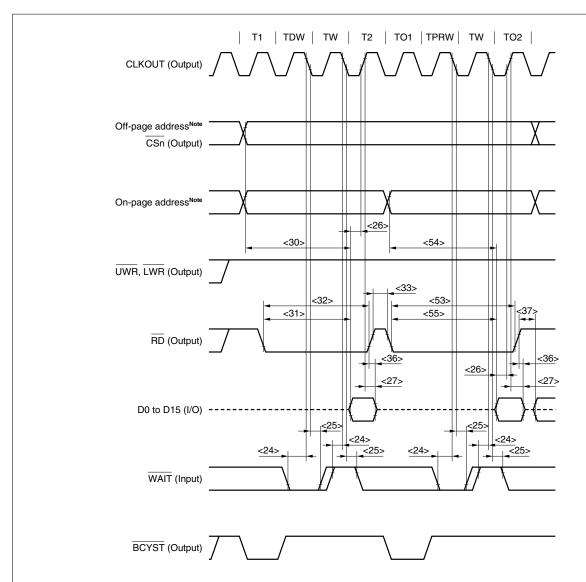
Parameter	Symbol		Condition	MIN.	MAX.	Unit
WAIT setup time (to CLKOUT ↓)	<24>	tswĸ		15		ns
\overline{WAIT} hold time (from CLKOUT \downarrow)	<25>	thkw		2		ns
Data input setup time (to CLKOUT ↑)	<26>	tskid		18		ns
Data input hold time (from CLKOUT ↑)	<27>	tнкid		2		ns
Off-page data input setup time (to address)	<30>	tsaid			(1.5 + w _D + w)T – 28	ns
Off-page data input setup time (to RD)	<31>	tsrdid			(1 + w _D + w)T − 32	ns
Off-page RD low-level width	<32>	twrdl		(1 + w□ + w)T – 10		ns
RD high-level width	<33>	twrdh		0.5T – 10		ns
Data input hold time (from \overline{RD})	<36>	throid		0		ns
Delay time from RD ↑ to data output	<37>	t DRDOD		(0.5 + i)T - 10		ns
On-page RD low-level width	<53>	twordl		(1.5 + WPR + W)T - 10		ns
On-page data input setup time (to address)	<54>	tsoaid			(1.5 + WPR + W)T - 28	ns
On-page data input setup time (to RD)	<55>	tsordid			(1.5 + WPR + W)T - 32	ns

Remarks 1. $T = t_{CYK}$

- **2.** w: The number of waits due to \overline{WAIT} .
- 3. wp: The number of waits due to the DWC1 and DWC2 registers.
- 4. WPR: The number of waits due to the PRC register.
- 5. i: The number of idle states that are inserted when a write cycle follows a read cycle.
- 6. Maintain at least one of the data input hold times, thkid or throld.



(5) Page ROM access timing (2/2)



Note On-page and off-page addresses are as follows.

	PRC Regist	er	On many Addresses	Off many Andreas			
MA5	MA4	MA3	On-page Addresses	Off-page Addresses			
0	0	0	A0, A1	A2 to A23			
0	0	1	A0 to A2	A3 to A23			
0	1	1	A0 to A3	A4 to A23			
1	1	1	A0 to A4	A5 to A23			

Remarks 1. This is the timing for the following case.

Number of waits due to the DWC1 and DWC2 registers (TDW): 1 Number of waits due to the PRC register (TPRW): 1

- 2. The broken lines indicate high impedance.
- **3.** n = 0, 3 to 5



(6) DRAM access timing

(a) Read timing (high-speed page DRAM access, normal access: off-page) (1/3)

Parameter	Syr	nbol	Condition	MIN.	MAX.	Unit
\overline{WAIT} setup time (to CLKOUT \downarrow)	<24>	t swĸ		15		ns
WAIT hold time (from CLKOUT ↓)	<25>	thkw		2		ns
Data input setup time (to CLKOUT ↑)	<26>	t skid		18		ns
Data input hold time (from CLKOUT ↑)	<27>	tнкір		2		ns
Delay time from OE ↑ to data output	<37>	tdrdod		(0.5 + i)T - 10		ns
Row address setup time	<56>	tasr		(0.5 + WRP)T - 10		ns
Row address hold time	<57>	tпан		(0.5 + w _{RH})T – 10		ns
Column address setup time	<58>	tasc		0.5T – 10		ns
Column address hold time	<59>	t CAH		(1.5 + WDA + W)T - 10		ns
Read/write cycle time	<60>	trc		(3 + WRP + WRH + WDA + W)T - 10		ns
RAS precharge time	<61>	t _{RP}		(0.5 + WRP)T - 10		ns
RAS pulse time	<62>	tras		(2.5 + WRH + WDA + W)T - 10		ns
RAS hold time	<63>	t rsh		(1.5 + WDA + W)T - 10		ns
Column address read time for RAS	<64>	tral		(2 + WDA + W)T - 10		ns
CAS pulse width	<65>	tcas		(1 + wda + w)T - 10		ns
CAS-RAS precharge time	<66>	tcrp		(1 + WRP)T - 10		ns
CAS hold time	<67>	tсsн		(2 + WRH + WDA + W)T - 10		ns
WE setup time	<68>	trcs		(2 + WRP + WRH)T - 10		ns
WE hold time (from RAS ↑)	<69>	t rrh		0.5T – 10		ns
WE hold time (from CAS ↑)	<70>	t rch		T – 10		ns
CAS precharge time	<71>	t CPN		(2 + WRP + WRH)T - 10		ns
Output enable access time	<72>	t oea			(2 + WRP + WRH + WDA + W)T - 28	ns
RAS access time	<73>	trac			(2 + WRH + WDA + W)T - 28	ns
Access time from column address	<74>	taa			(1.5 + WDA + W)T - 28	ns
CAS access time	<75>	tcac			(1 + wda + w)T – 28	ns

Remarks 1. $T = t_{CYK}$

- **2.** w: The number of waits due to $\overline{\text{WAIT}}$.
- 3. WRP: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **4.** WRH: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **5.** WDA: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- 6. i: The number of idle states that are inserted when a write cycle follows a read cycle.



(a) Read timing (high-speed page DRAM access, normal access: off-page) (2/3)

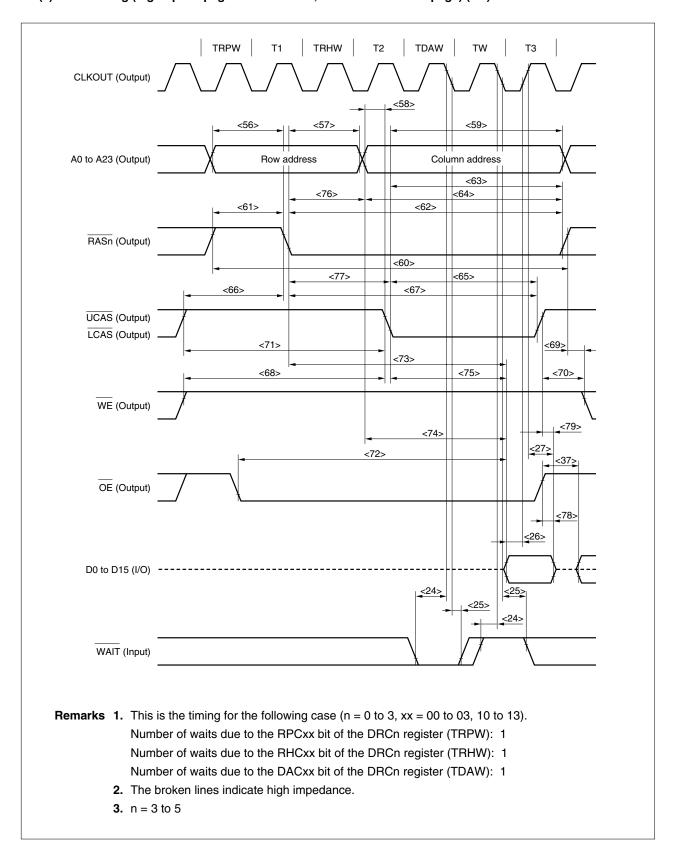
Parameter	Syn	nbol	Condition	MIN.	MAX.	Unit
RAS column address delay time	<76>	tRAD		(0.5 + wвн)T – 10		ns
RAS-CAS delay time	<77>	tRCD		(1 + WRH)T - 10		ns
Output buffer turn-off delay time (from OE 1)	<78>	toez		0		ns
Output buffer turn-off delay time (from CAS ↑)	<79>	toff		0		ns

Remarks 1. $T = t_{CYK}$

2. WRH: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).



(a) Read timing (high-speed page DRAM access, normal access: off-page) (3/3)



[MEMO]



(b) Read timing (high-speed page DRAM access: on-page) (1/2)

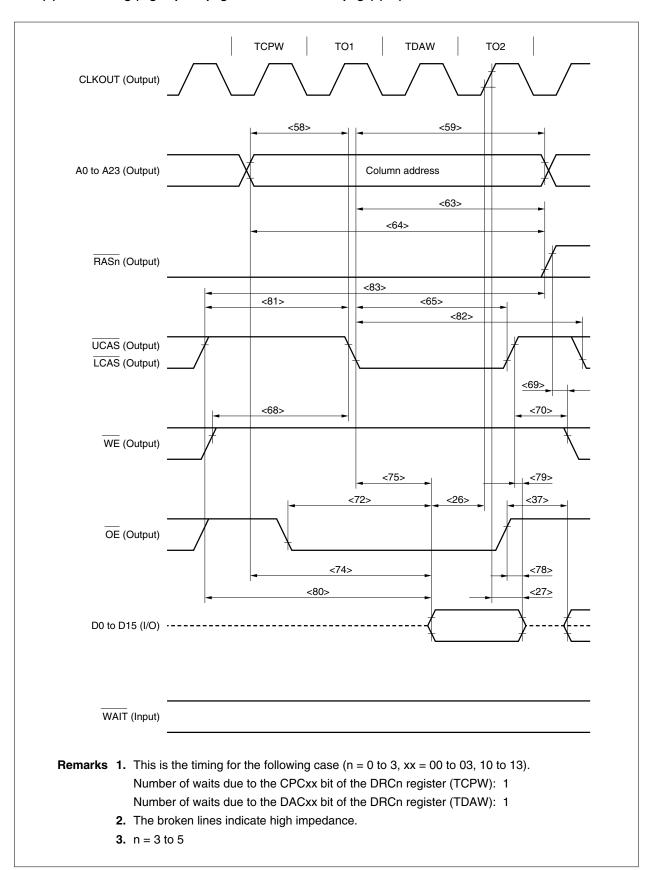
Parameter	Syn	nbol	Condition	MIN.	MAX.	Unit
Data input setup time (to CLKOUT ↑)	<26>	tskid		18		ns
Data input hold time (from CLKOUT ↑)	<27>	thkid		2		ns
Delay time from OE ↑ to data output	<37>	tdRDOD		(0.5 + i)T - 10		ns
Column address setup time	<58>	tasc		(0.5 + WCP)T - 10		ns
Column address hold time	<59>	t CAH		(1.5 + WDA)T - 10		ns
RAS hold time	<63>	t RSH		(1.5 + WDA)T - 10		ns
Column address read time for RAS	<64>	t RAL		(2 + WCP + WDA)T - 10		ns
CAS pulse width	<65>	tcas		(1 + WDA)T - 10		ns
WE setup time (to CAS ↓)	<68>	trcs		(1 + WCP)T - 10		ns
WE hold time (from RAS ↑)	<69>	tп		0.5T – 10		ns
WE hold time (from CAS ↑)	<70>	t RCH		T – 10		ns
Output enable access time	<72>	t oea			(1 + WCP + WDA)T - 28	ns
Access time from column address	<74>	taa			(1.5 + WCP + WDA)T - 28	ns
CAS access time	<75>	tcac			(1 + WDA)T – 28	ns
Output buffer turn-off delay time (from OE ↑)	<78>	toez		0		ns
Output buffer turn-off delay time (from CAS ↑)	<79>	toff		0		ns
Access time from CAS precharge	<80>	t acp			(2 + WCP + WDA)T - 28	ns
CAS precharge time	<81>	t cp		(1 + WCP)T - 10		ns
High-speed page mode cycle time	<82>	t PC		(2 + WCP + WDA)T - 10		ns
RAS hold time for CAS precharge	<83>	t RHCP		(2.5 + WCP + WDA)T - 10		ns

Remarks 1. $T = t_{CYK}$

- 2. wcp: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- 3. WDA: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- 4. i: The number of idle states that are inserted when a write cycle follows a read cycle.



(b) Read timing (high-speed page DRAM access: on-page) (2/2)





(c) Write timing (high-speed page DRAM access, normal access: off-page) (1/2)

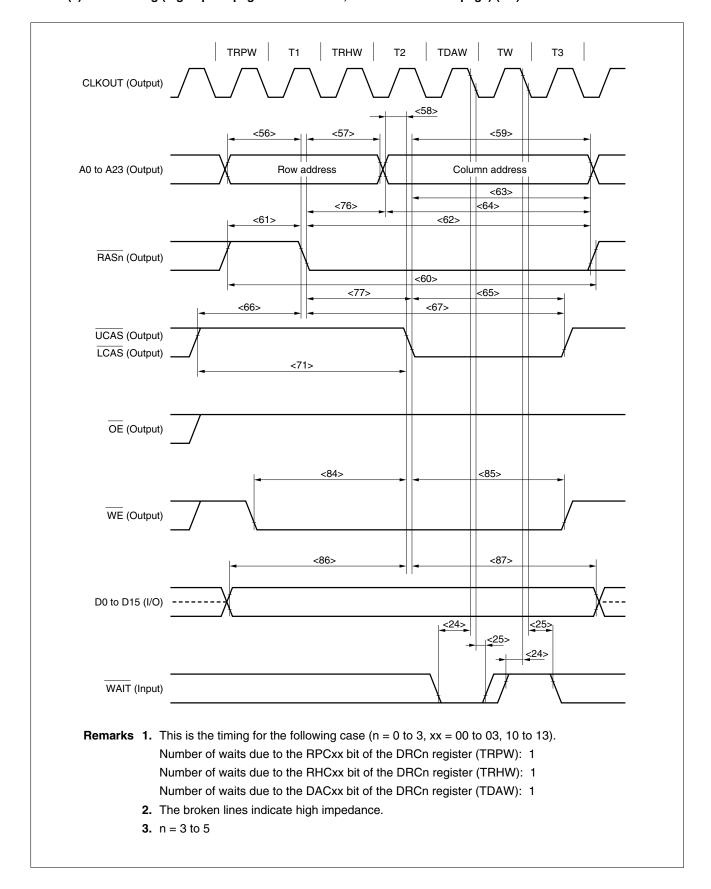
Parameter	Syn	nbol	Condition	MIN.	MAX.	Unit
\overline{WAIT} setup time (to CLKOUT \downarrow)	<24>	t swĸ		15		ns
WAIT hold time (from CLKOUT ↓)	<25>	tнкw		2		ns
Row address setup time	<56>	tasr		(0.5 + WRP)T - 10		ns
Row address hold time	<57>	t rah		(0.5 + wrн)T – 10		ns
Column address setup time	<58>	tasc		0.5T – 10		ns
Column address hold time	<59>	t CAH		(1.5 + WDA + W)T - 10		ns
Read/write cycle time	<60>	trc		(3 + WRP + WRH + WDA + W)T - 10		ns
RAS precharge time	<61>	t _{RP}		(0.5 + WRP)T - 10		ns
RAS pulse time	<62>	tras		(2.5 + WRH + WDA + W)T - 10		ns
RAS hold time	<63>	t rsh		(1.5 + WDA + W)T - 10		ns
Column address read time (from RAS ↑)	<64>	tral		(2 + WDA + W)T - 10		ns
CAS pulse width	<65>	tcas		(1 + WDA + W)T - 10		ns
CAS-RAS precharge time	<66>	tcrp		(1 + w _{RH})T - 10		ns
CAS hold time	<67>	tсsн		(2 + WRH + WDA + W)T - 10		ns
CAS precharge time	<71>	t CPN		(2 + WRP + WRH)T - 10		ns
RAS column address delay time	<76>	tRAD		(0.5 + w _{RH})T – 10		ns
RAS-CAS delay time	<77>	t RCD		(1 + w _{RH})T - 10		ns
WE setup time (to CAS ↓)	<84>	twcs		(1 + WRP + WRH)T - 10		ns
WE hold time (from CAS ↓)	<85>	twcн		(1 + WDA + W)T - 10		ns
Data setup time (to CAS ↓)	<86>	t DS		(1.5 + WRP + WRH)T - 10		ns
Data hold time (from CAS ↓)	<87>	tон		(1.5 + WDA + W)T - 10		ns

Remarks 1. $T = t_{CYK}$

- **2.** w: The number of waits due to $\overline{\text{WAIT}}$.
- 3. wrp: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **4.** WRH: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **5.** WDA: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).



(c) Write timing (high-speed page DRAM access, normal access: off-page) (2/2)





(d) Write timing (high-speed page DRAM access: on-page) (1/2)

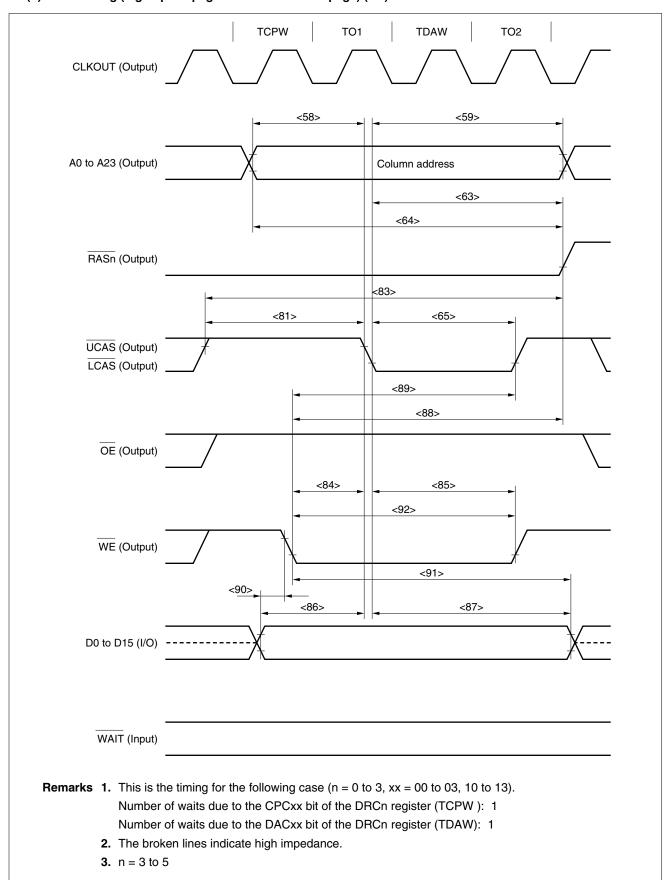
Parameter	Syn	nbol	Condition	MIN.	MAX.	Unit
Column address setup time	<58>	tasc		(0.5 + wcp)T - 10		ns
Column address hold time	<59>	t CAH		(1.5 + WDA)T - 10		ns
RAS hold time	<63>	t RSH		(1.5 + WDA)T - 10		ns
Column address read time (from RAS ↑)	<64>	tral		(2 + WCP + WDA)T - 10		ns
CAS pulse width	<65>	tcas		(1 + WDA)T - 10		ns
CAS precharge time	<81>	t CP		(1 + WCP)T - 10		ns
RAS hold time for CAS precharge	<83>	t RHCP		(2.5 + WCP + WDA)T - 10		ns
WE setup time (to CAS ↓)	<84>	twcs	WCP ≥ 1	WCPT - 10		ns
WE hold time (from CAS ↓)	<85>	twcн		(1 + WDA)T - 10		ns
Data setup time (to CAS ↓)	<86>	tos		(0.5 + WCP)T - 10		ns
Data hold time (from CAS ↓)	<87>	tон		(1.5 + WDA)T - 10		ns
WE read time (from RAS ↑)	<88>	trwL	WCP = 0	(1.5 + WDA)T - 10		ns
WE read time (from CAS ↑)	<89>	tcwL	wcp = 0	(1 + WDA)T - 10		ns
Data setup time (to $\overline{\text{WE}}\downarrow$)	<90>	toswe	WCP = 0	0.5T – 10		ns
Data hold time (from $\overline{\text{WE}} \downarrow$)	<91>	tohwe	WCP = 0	(1.5 + WDA)T - 10		ns
WE pulse width	<92>	twp	WCP = 0	(1 + WDA)T - 10		ns

Remarks 1. $T = t_{CYK}$

- **2.** wcp: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- 3. WDA: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).



(d) Write timing (high-speed page DRAM access: on-page) (2/2)





(e) Read timing (EDO DRAM) (1/3)

Parameter		Syn	nbol	Condition	MIN.	MAX.	Unit
Data input setup time (to C	CLKOUT 1)	<26>	tskid		18		ns
Data input hold time (from CLKOUT ↑)		<27>	t HKID		2		ns
Delay time from OE ↑ to d	ata output	<37>	tordod		(0.5 + i)T - 10		ns
Row address setup time		<56>	tasr		(0.5 + WRP)T - 10		ns
Row address hold time		<57>	t rah		(0.5 + w _{RH})T – 10		ns
Column address setup tim	е	<58>	tasc		0.5T – 10		ns
Column address hold time		<59>	t cah		(0.5 + WDA)T - 10		ns
RAS precharge time		<61>	t _{RP}		(0.5 + WRP)T - 10		ns
Column address read time (from RAS ↑)	<64>	tral		(2 + WCP + WDA)T - 10		ns
CAS-RAS precharge time		<66>	tcrp		(1 + WRP)T - 10		ns
CAS hold time		<67>	tсsн		(1.5 + WRH + WDA)T - 10		ns
WE setup time (to CAS ↓)		<68>	trcs		(2 + WRP + WRH)T - 10		ns
WE hold time (from RAS ↑)		<69>	trrh		0.5T – 10		ns
WE hold time (from CAS 1	`)	<70>	t rch		1.5T – 10		ns
RAS access time	RAS access time		t rac			(2 + WRH + WDA)T - 28	ns
Access time from column a	address	<74>	taa			(1.5 + WDA)T – 28	ns
CAS access time		<75>	tcac			(1 + wda)T – 28	ns
Delay time from RAS to co	olumn address	<76>	tRAD		(0.5 + w _{RH})T – 10		ns
RAS-CAS delay time		<77>	t RCD		(1 + w _{RH})T - 10		ns
Output buffer turn-off delay OE)	y time (from	<78>	toez		0		ns
Access time from CAS pre	charge	<80>	tacp			(1.5 + WCP + WDA)T - 28	ns
CAS precharge time		<81>	t cp		(0.5 + WCP)T - 10		ns
RAS hold time for CAS pre	echarge	<83>	t RHCP		(2 + WCP + WDA)T - 10		ns
Read cycle time		<93>	thpc		(1 + WDA + WCP)T - 10		ns
RAS pulse width		<94>	trasp		(2.5 + WRH + WDA)T - 10		ns
CAS pulse width		<95>	thcas		(0.5 + WDA)T - 10		ns
CAS hold time from OE	Off-page	<96>	toch1		(2 + WRH + WDA)T - 10		ns
	On-page	<97>	toch2		(0.5 + WDA)T - 10		ns
Data input hold time (from	CAS ↓)	<98>	t DHC		0		ns

Remarks 1. $T = t_{CYK}$

- 2. WRP: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- 3. WRH: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **4.** w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- 5. wcp: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).

6. i: The number of idle states that are inserted when a write cycle follows a read cycle.

(e) Read timing (EDO DRAM) (2/3)

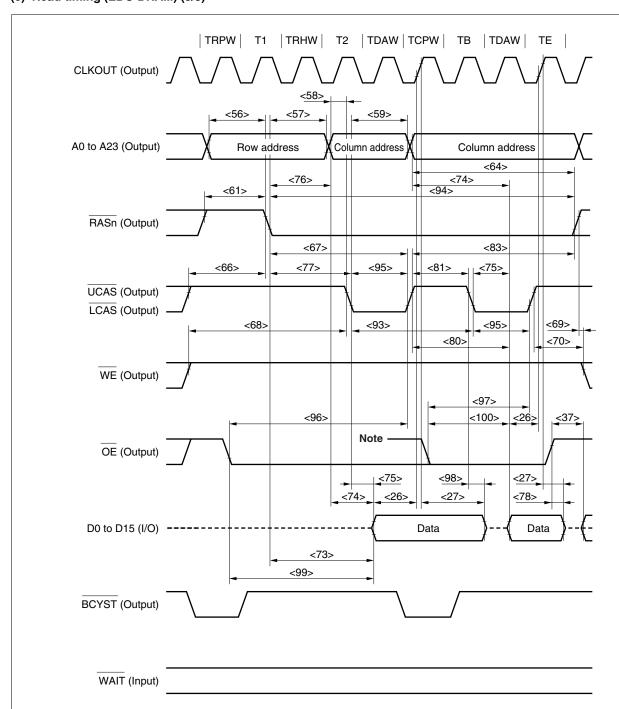
Parameter		Symbol		Condition	MIN.	MAX.	Unit
Output enable access time	Off-page	<99>	toea1			(2 + WRP + WRH + WDA)T - 28	ns
	On-page	<100>	toea2			(1 + WCP + WDA)T - 28	ns

Remarks 1. $T = t_{CYK}$

- **2.** wRP: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **3.** wRH: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **4.** w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
- **5.** wcp: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).



(e) Read timing (EDO DRAM) (3/3)



Note For on-page access from another cycle during the RASn low-level signal.

Remarks 1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).

Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1

Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1

Number of waits due to the DACxx bit of the DRCn register (TDAW): 1

Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1

- 2. The broken lines indicate high impedance.
- **3.** n = 3 to 5

[MEMO]



(f) Write timing (EDO DRAM) (1/2)

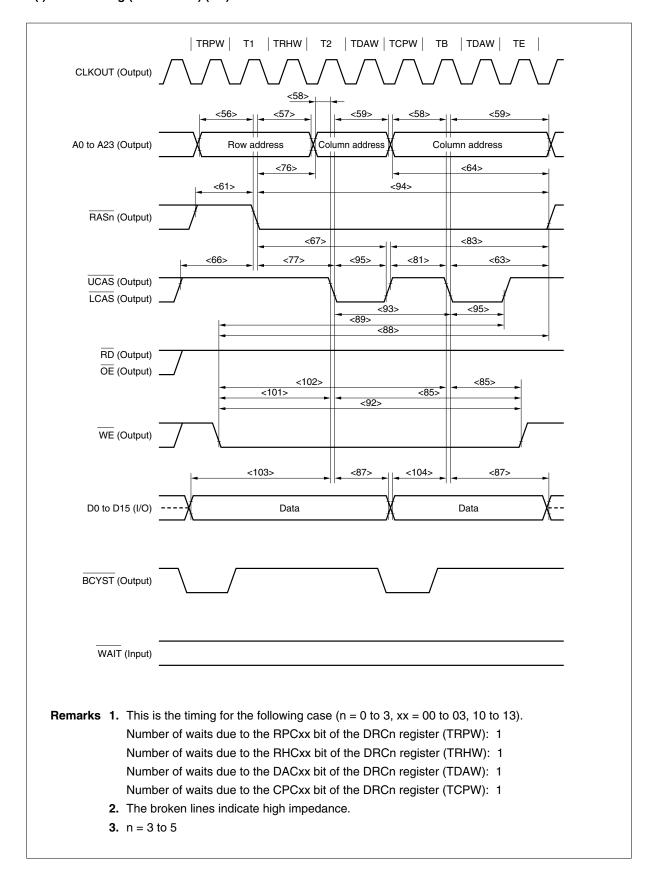
Parameter		Syn	nbol	Condition	MIN.	MAX.	Unit
Row address setup time		<56>	tasr		(0.5 + WRP)T - 10		ns
Row address hold time		<57>	t rah		(0.5 + w _{RH})T – 10		ns
Column address setup tir	ne	<58>	tasc		0.5T – 10		ns
Column address hold tim	е	<59>	t cah		(0.5 + WDA)T - 10		ns
RAS precharge time		<61>	t RP		(0.5 + WRP)T - 10		ns
RAS hold time		<63>	tпsн		(1.5 + WDA)T - 10		ns
Column address read time (from RAS ↑)	е	<64>	tral		(2 + WCP + WDA)T - 10		ns
CAS-RAS precharge time)	<66>	torp		(1 + WRP)T - 10		ns
CAS hold time		<67>	tсsн		(1.5 + WRH + WDA)T - 10		ns
Delay time from RAS to column address		<76>	t RAD		(0.5 + w _{RH})T – 10		ns
RAS-CAS delay time		<77>	t RCD		(1 + WRH)T - 10		ns
CAS precharge time		<81>	t CP		(0.5 + WCP)T - 10		ns
RAS hold time for CAS precharge		<83>	t RHCP		(2 + WCP + WDA)T - 10		ns
WE hold time (from CAS	↓)	<85>	twcн		(1 + WDA)T - 10		ns
Data hold time (from CAS	S ↓)	<87>	tон		(0.5 + WDA)T - 10		ns
WE read time (from RAS ↑)	On-page	<88>	trwL	WCP = 0	(1.5 + WDA)T - 10		ns
WE read time (from CAS ↑)	On-page	<89>	tcwL	WCP = 0	(0.5 + WDA)T - 10		ns
WE pulse width	On-page	<92>	twp	wcp = 0	(1 + WDA)T - 10		ns
Write cycle time		<93>	t HPC		(1 + WDA + WCP)T - 10		ns
RAS pulse width		<94>	trasp		(2.5 + WRH + WDA)T - 10		ns
CAS pulse width		<95>	thcas		(0.5 + WDA)T - 10		ns
WE setup time	Off-page	<101>	twcs1		(1 + WRP + WRH)T - 10		ns
(to CAS ↓)	On-page	<102>	twcs2	W CP ≥ 1	WCPT - 10		ns
Data setup time	Off-page	<103>	t _{DS1}		(1.5 + WRP + WRH)T - 10		ns
(to CAS ↓)	On-page	<104>	t _{DS2}		(0.5 + WCP)T - 10		ns

Remarks 1. T = tcyk

- 2. WRP: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- 3. WRH: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **4.** WDA: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **5.** wcp: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).



(f) Write timing (EDO DRAM) (2/2)





(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (1/3)

Parameter	Syr	nbol	Condition	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT \downarrow)	<24>	t swĸ		15		ns
WAIT hold time (from CLKOUT ↓)	<25>	tнкw		2		ns
Delay time from OE ↑ to data output	<37>	tordod		(0.5 + i)T - 10		ns
Delay time from address to IOWR ↓	<41>	tdawr		(0.5 + WRP)T - 10		ns
Address setup time (to lOWR ↑)	<42>	tsawr		(2 + WRP + WRH + WDA + W)T - 10		ns
Delay time from IOWR ↑ to address	<43>	t dwra		0.5T – 10		ns
Delay time from IOWR ↑ to RD ↑	<48>	towrrd	w _F = 0	0		ns
			WF = 1	T – 10		ns
IOWR low-level width	<50>	twwrL		(2 + WRH + WDA + W)T - 10		ns
Row address setup time	<56>	tasr		(0.5 + WRP)T - 10		ns
Row address hold time	<57>	tпан		(0.5 + w _{RH})T – 10		ns
Column address setup time	<58>	tasc		0.5T – 10		ns
Column address hold time	<59>	t cah		(1.5 + WDA + WF + W)T - 10		ns
Read/write cycle time	<60>	trc		(3 + WRP + WRH + WDA + WF + W)T - 10		ns
RAS precharge time	<61>	t _{RP}		(0.5 + WRP)T - 10		ns
RAS hold time	<63>	tяsн		(1.5 + WDA + WF + W)T - 10		ns
Column address read time for RAS	<64>	tral		(2 + WCP + WDA + WF + W)T - 10		ns
CAS pulse width	<65>	tcas		(1 + WDA + WF + W)T - 10		ns
CAS-RAS precharge time	<66>	tcrp		(1 + WRP)T - 10		ns
CAS hold time	<67>	tсsн		(2 + WRH + WDA + WF + W)T - 10		ns

Remarks 1. T = tcyk

- 2. w: The number of waits due to \overline{WAIT} .
- 3. WRP: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **4.** WRH: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **5**. w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **6.** wcp: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- 7. wr: The number of waits that are inserted for a source-side access during a DMA flyby transfer.
- **8.** i: The number of idle states that are inserted when a write cycle follows a read cycle.



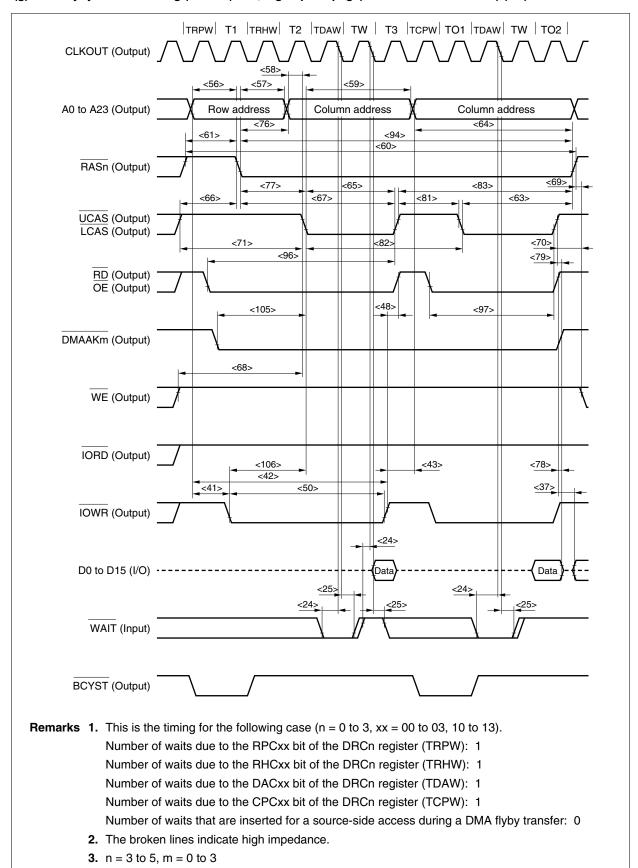
(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (2/3)

Parameter		Syn	nbol	Condition	MIN.	MAX.	Unit
WE setup time (to CAS ↓)	1	<68>	trcs		(2 + WRP + WRH)T - 10		ns
WE hold time (from RAS ↑)		<69>	trrh		0.5T – 10		ns
WE hold time (from CAS	^)	<70>	t RCH		1.5T – 10		ns
CAS precharge time		<71>	t CPN		(2 + WRP + WRH)T - 10		ns
Delay time from RAS to co	olumn address	<76>	tRAD		(0.5 + WRH)T - 10		ns
RAS-CAS delay time		<77>	tRCD		(1 + WRH)T - 10		ns
Output buffer turn-off delay time (from $\overline{\sf OE}$ \uparrow)		<78>	toez		0		ns
Output buffer turn-off delay time (from CAS ↑)		<79>	toff		0		ns
CAS precharge time		<81>	t CP		(0.5 + WCP)T - 10		ns
High-speed page mode cy	cle time	<82>	t PC		(2 + WCP + WDA + WF + W)T - 10		ns
RAS hold time for CAS pr	echarge	<83>	trhcp		(2.5 + WCP + WDA + WF + W)T - 10		ns
RAS pulse width		<94>	trasp		(2.5 + WRH + WDA + WF + W)T - 10		ns
CAS hold time from OE (from CAS ↑)	Off-page	<96>	tocн1		(2.5 + WRP + WRH + WDA + WF + W)T - 10		ns
	On-page	<97>	t осн2		(1.5 + WCP + WDA + WF + W)T - 10		ns
Delay time from DMAAKn	to CAS ↓	<105>	tddacs		(1.5 + wrн)T – 10		ns
Delay time from IOWR ↓ t	o CAS ↓	<106>	tordcs		(1 + wвн)T – 10		ns

Remarks 1. T = tcyk

- 2. w: The number of waits due to \overline{WAIT} .
- 3. wcp: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **4.** w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
- **5.** WRH: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
- **6.** wRP: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
- 7. wr: The number of waits that are inserted for a source-side access during a DMA flyby transfer.
- **8.** m = 0 to 3

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (3/3)





(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (1/3)

Parameter	Syn	nbol	Condition	MIN.	MAX.	Unit
\overline{WAIT} setup time (to CLKOUT \downarrow)	<24>	tswĸ		15		ns
WAIT hold time (from CLKOUT ↓)	<25>	thkw		2		ns
IORD low-level width	<32>	twrdl		(2 + WRH + WDA + WF + W)T - 10		ns
IORD high-level width	<33>	twrdh		T – 10		ns
Delay time from address to IORD ↑	<34>	t DARD		0.5T – 10		ns
Delay time from IORD ↑ to address	<35>	t DRDA		(0.5 + i)T – 10		ns
Row address setup time	<56>	tasr		(0.5 + WRP)T - 10		ns
Row address hold time	<57>	t RAH		(0.5 + w _{RH})T - 10		ns
Column address setup time	<58>	tasc		0.5T – 10		ns
Column address hold time	<59>	t CAH		(1.5 + WDA + WF)T - 10		ns
Read/write cycle time	<60>	trc		(3 + WRP + WRH + WDA + WF + W)T - 10		ns
RAS precharge time	<61>	tre		(0.5 + WRP)T - 10		ns
RAS hold time	<63>	t RSH		(1.5 + WDA + WF)T - 10		ns
Column address read time for RAS	<64>	t RAL		(2 + WCP + WDA + WF + W)T - 10		ns
CAS pulse width	<65>	tcas		(1 + WDA + WF)T - 10		ns
CAS-RAS precharge time	<66>	tcrp		(1 + WRP)T - 10		ns
CAS hold time	<67>	tсsн		(2 + WRH + WDA + WF + W)T - 10		ns
CAS precharge time	<71>	t CPN		(2 + WRP + WRH + W)T - 10		ns
Delay time from RAS to column address	<76>	tRAD		(0.5 + w _{RH})T - 10		ns
RAS-CAS delay time	<77>	tRCD		(1 + WRH + W)T - 10		ns
CAS precharge time	<81>	t CP		(0.5 + WCP + W)T - 10		ns
High-speed page mode cycle time	<82>	t PC		(2 + WCP + WDA + WF + W)T - 10		ns
RAS hold time for CAS precharge	<83>	t RHCP		(2.5 + WCP + WDA + W)T - 10		ns
WE hold time (from CAS ↓)	<85>	twcн		(1 + WDA)T - 10		ns
WE read time (from RAS ↑)	<88>	trwL	WCP = 0	(1.5 + WDA + W)T - 10		ns

Remarks 1. T = tcyk

- 2. w: The number of waits due to \overline{WAIT} .
- 3. WRH: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **4.** WDA: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **5.** wRP: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **6.** wcp: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- 7. wr: The number of waits that are inserted for a source-side access during a DMA flyby transfer.
- **8.** i: The number of idle states that are inserted when a write cycle follows a read cycle.



(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (2/3)

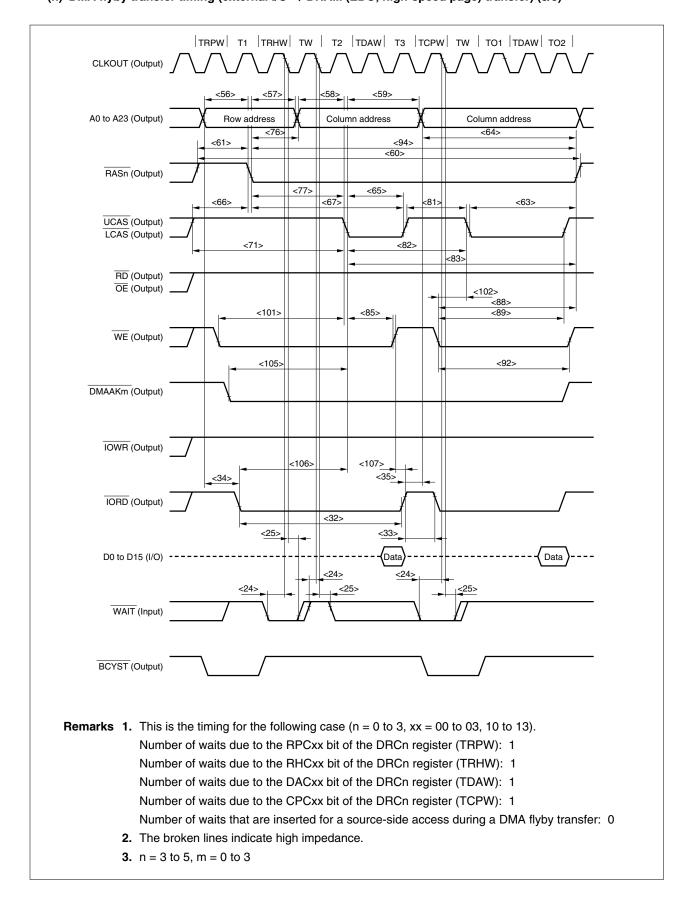
Parameter	meter Symbol Condition		MIN.	MAX.	Unit		
WE read time (from CAS	<u>^</u>)	<89>	t cwL	wcp = 0	(1 + WDA + W)T - 10		ns
WE pulse width		<92>	twp	WCP = 0	(1 + WDA + W)T – 10		ns
RAS pulse width		<94>	t RASP		(2.5 + WRH + WDA + WF + W)T – 10		ns
WE setup time	Off-page	<101>	twcs1	wcp = 0	(1 + WRH + WRP + W)T - 10		ns
(to CAS ↓)	On-page	<102>	twcs2	w cp ≥ 1	WCPT - 10		ns
Delay time from DMAAKm	to CAS↓	<105>	tddacs		(1.5 + WRH + W)T - 10		ns
Delay time from IORD ↓ t	o CAS ↓	<106>	tordes		(1 + WRH + W)T - 10		ns
Delay time from WE ↑ to	IORD ↑	<107>	towerd	wF = 0	0		ns
				WF = 1	T – 10		ns

Remarks 1. T = tcyk

- 2. w: The number of waits due to $\overline{\text{WAIT}}$.
- 3. WRH: The number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **4.** w_{DA}: The number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **5.** wRP: The number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- **6.** wcp: The number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13).
- 7. wr: The number of waits that are inserted for a source-side access during a DMA flyby transfer.
- **8.** m = 0 to 3



(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (3/3)





(i) CBR refresh timing

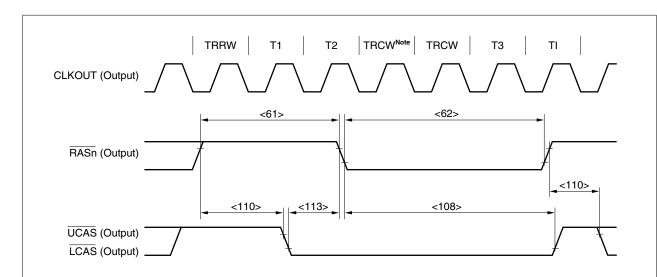
Parameter	Symbol		Condition	MIN.	MAX.	Unit
RAS precharge time	<61>	t RP		(1.5 + WRRW)T - 10		ns
RAS pulse width	<62>	tras		$(1.5 + WRCW^{Note})T - 10$		ns
CAS hold time	<108>	tchr		$(1.5 + WRCW^{Note})T - 10$		ns
RAS precharge CAS hold time	<110>	t RPC		(0.5 + WRRW)T - 10		ns
CAS setup time	<113>	tcsr		T – 10		ns

Note At least one clock cycle is inserted by default for wncw regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

Remarks 1. $T = t_{CYK}$

2. WRRW: The number of waits due to the RRW0 and RRW1 bits of the RWC register.

3. wacw: The number of waits due to the RCW0 to RCW2 bits of the RWC register.



Note This TRCW is always inserted regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

Remarks 1. This is the timing for the following case.

Number of waits due to the RRW0 and RRW1 bits of the RWC register (TRRW): 1 Number of waits due to the RCW0 to RCW2 bits of the RWC register (TRCW): 2

2. n = 3 to 5

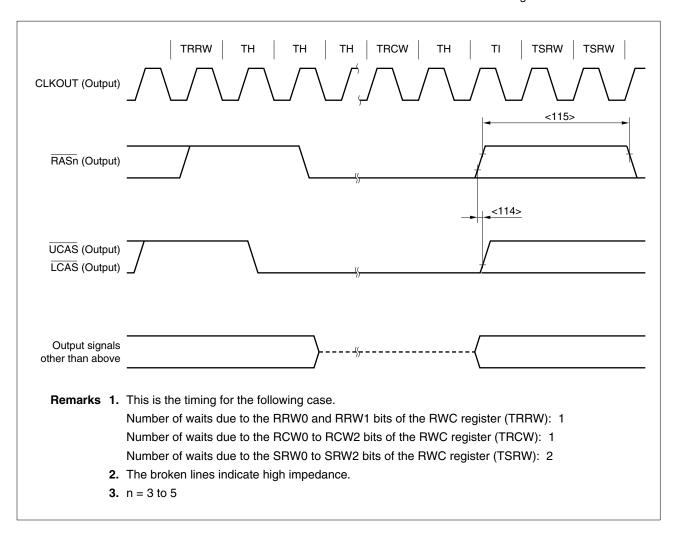


(j) CBR self-refresh timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CAS hold time	<114>	tснs		-5		ns
RAS precharge time	<115>	trps		(1 + 2wsrw)T - 10		ns

Remarks 1. $T = t_{CYK}$

2. wsrw: The number of waits due to the SRW0 to SRW2 bits of the RWC register.

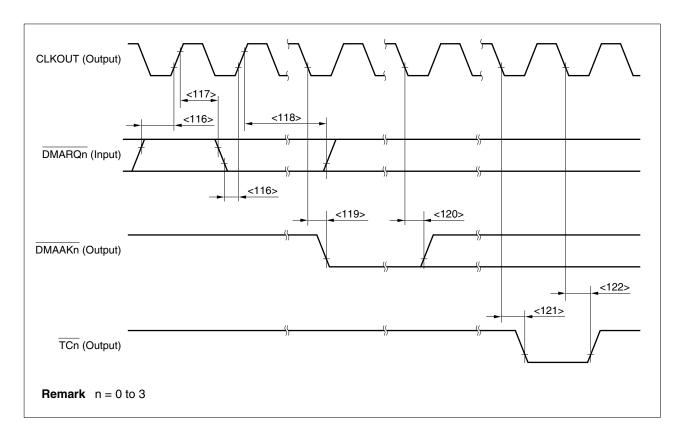




(7) DMAC timing

Parameter	Syn	nbol	Condition	MIN.	MAX.	Unit
DMARQn setup time (to CLKOUT ↑)	<116>	tsdrk		15		ns
DMARQn hold time (from CLKOUT ↑)	<117>	thkdr1		2		ns
	<118>	thkdr2		Until DMAAKn ↓		ns
DMAAKn output delay time (from CLKOUT ↓)	<119>	t DKDA		2	10	ns
DMAAKn output hold time (from CLKOUT ↓)	<120>	thkda		2	10	ns
TCn output delay time (from CLKOUT ↓)	<121>	tokto		2	10	ns
TCn output hold time (from CLKOUT ↓)	<122>	tнктс		2	10	ns

Remark n = 0 to 3



[MEMO]



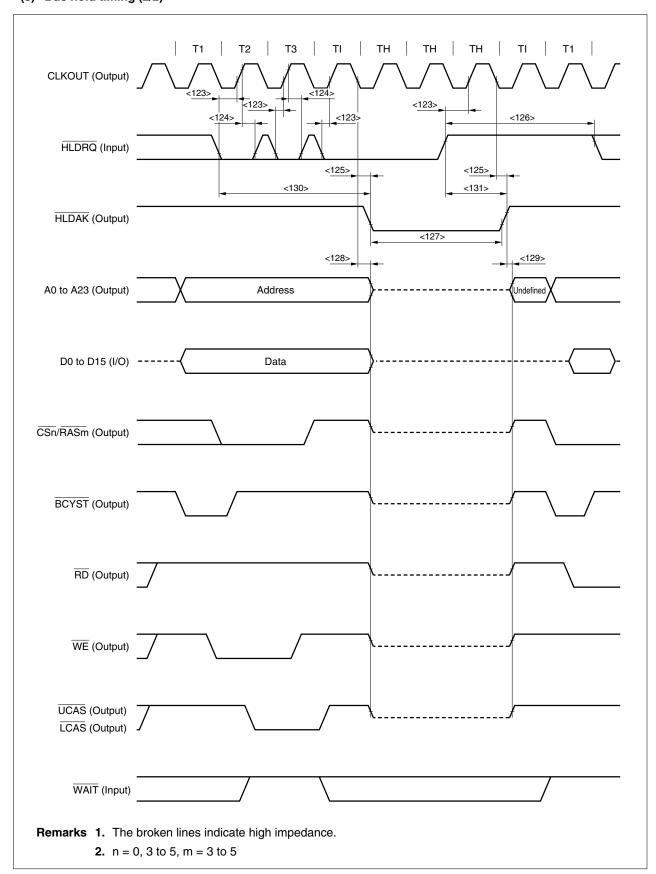
(8) Bus hold timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
HLDRQ setup time (to CLKOUT ↑)	<123>	tshrk		15		ns
HLDRQ hold time (from CLKOUT ↑)	<124>	thkhr		2		ns
Delay time from CLKOUT ↓ to HLDAK	<125>	t DKHA		2	10	ns
HLDRQ high-level width	<126>	twнqн		T + 17		ns
HLDAK low-level width	<127>	twhal		T – 8		ns
Delay time from $\overline{CLKOUT} \downarrow to$ bus float	<128>	tokcf			10	ns
Delay time from HLDAK ↑ to bus output	<129>	t DHAC		0		ns
Delay time from $\overline{\text{HLDRQ}}\downarrow$ to $\overline{\text{HLDAK}}\downarrow$	<130>	tdhqha1		2.5T		ns
Delay time from $\overline{\text{HLDRQ}} \uparrow$ to $\overline{\text{HLDAK}} \uparrow$	<131>	tdhqha2		0.5T	1.5T	ns

Remark T = tcyk



(8) Bus hold timing (2/2)



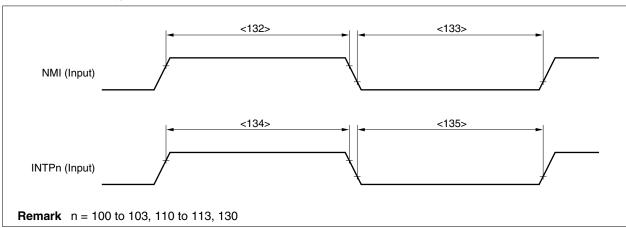


(9) Interrupt timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
NMI high-level width	<132>	twnih		500		ns
NMI low-level width	<133>	twnil		500		ns
INTPn high-level width	<134>	twiтн		4T + 10		ns
INTPn low-level width	<135>	twi⊤∟		4T + 10		ns

Remarks 1. n = 100 to 103, 110 to 113, 130

2. $T = t_{CYK}$

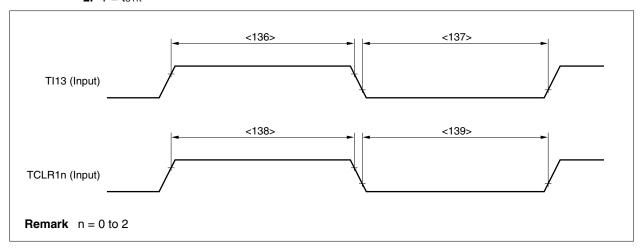


(10) RPU timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
TI13 high-level width	<136>	twтıн		3T + 18		ns
TI13 low-level width	<137>	twtiL		3T + 18		ns
TCLR1n high-level width	<138>	t wtch		3T + 18		ns
TCLR1n low-level width	<139>	t wtcl		3T + 18		ns

Remarks 1. n = 0 to 2

2. $T = t_{CYK}$

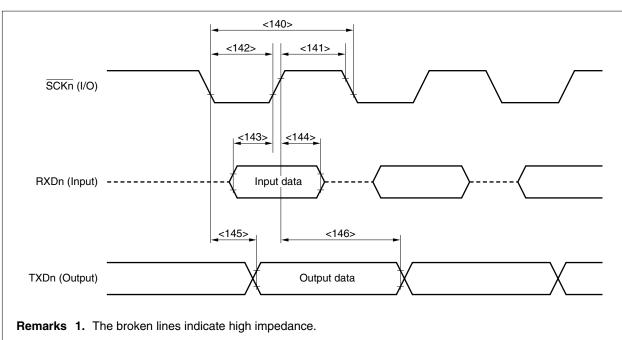




(11) UART0, UART1 timing (clock-synchronized or master mode only)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
SCKn cycle	<140>	tcysko	Output	250		ns
SCKn high-level width	<141>	twsкон	Output	0.5tcysко — 20		ns
SCKn low-level width	<142>	twskoL	Output	0.5tcysко — 20		ns
RXDn setup time (to SCKn ↑)	<143>	t srxsk		30		ns
RXDn hold time (from SCKn ↑)	<144>	thskrx		0		ns
TXDn output delay time (from $\overline{\text{SCKn}} \downarrow$)	<145>	t DSKTX			20	ns
TXDn output hold time (from SCKn ↑)	<146>	t HSKTX		0.5tсүѕко — 5		ns

Remark n = 0, 1



2. n = 0, 1



(12) CSI0, CSI1 timing

(a) Master mode

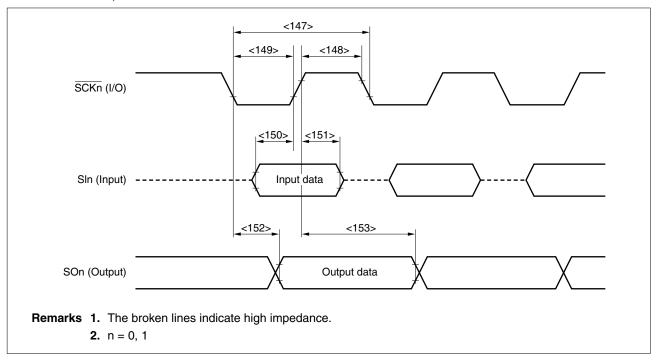
Parameter	Symbol		Condition	MIN.	MAX.	Unit
SCKn cycle	<147>	tcysk1	Output	100		ns
SCKn high-level width	<148>	twsk1H	Output	0.5tcүsк1 – 20		ns
SCKn low-level width	<149>	twsk1L	Output	0.5tcүsк1 — 20		ns
SIn setup time (to SCKn ↑)	<150>	tssisk		30		ns
SIn hold time (from SCKn ↑)	<151>	thsksi		0		ns
SOn output delay time (from SCKn ↓)	<152>	toskso			20	ns
SOn output hold time (from SCKn ↑)	<153>	thskso		0.5tcүsк1 — 5		ns

Remark n = 0, 1

(b) Slave mode

Parameter	Symbol		Condition	MIN.	MAX.	Unit
SCKn cycle	<147>	tcysk1	Input	100		ns
SCKn high-level width	<148>	twsk1H	Input	30		ns
SCKn low-level width	<149>	twsk1L	Input	30		ns
SIn setup time (to SCKn ↑)	<150>	tssisk		10		ns
SIn hold time (from SCKn ↑)	<151>	thsksi		10		ns
SOn output delay time (from SCKn ↓)	<152>	toskso			30	ns
SOn output hold time (from SCKn ↑)	<153>	thskso		twsĸıн		ns

Remark n = 0, 1





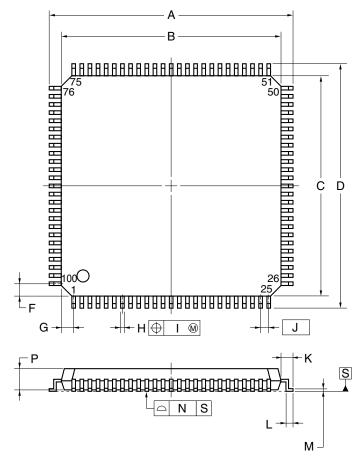
A/D Converter Characteristics (TA = -40 to +85°C, VDD = CVDD = 3.0 to 3.6 V, HVDD = 5.0 V \pm 10%, Vss = 0 V, HVDD - 0.5 V \leq AVDD \leq HVDD, output pin load capacitance: CL = 50 pF)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Resolution	_		10			bit
Overall error	_				±4	LSB
Quantization error	_				±1/2	LSB
Conversion time	tconv		5		10	μs
Sampling time	tsamp		Conversion clock ^{Note} /6			ns
Zero scale error	_				±4	LSB
Scale error	_				±4	LSB
Linearity error	_				±3	LSB
Analog input voltage	VIAN		-0.3		AVREF + 0.3	V
Analog input resistance	Ran			2		МΩ
AV _{REF} input voltage	AVREF	AVREF = AVDD	4.5		5.5	V
AV _{REF} input current	Alref				2.0	mA
AVDD current	Aldd				6	mA

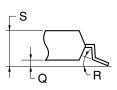
Note Conversion clock is the number of clocks set by the ADM1 register.

4. PACKAGE DRAWING

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



detail of lead end



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
Α	16.00±0.20
В	14.00±0.20
С	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
Н	$0.22^{+0.05}_{-0.04}$
ı	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
М	$0.17^{+0.03}_{-0.07}$
N	0.08
Р	1.40±0.05
Q	0.10±0.05
R	3° ^{+7°} -3°
S	1.60 MAX.
\$1000	3C-50-8FII 8FA-2

S100GC-50-8EU, 8EA-2

5. RECOMMENDED SOLDERING CONDITIONS

TBD

NOTES FOR CMOS DEVICES -

1 VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{\rm IL}$ (MAX) and $V_{\rm IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{\rm IL}$ (MAX) and $V_{\rm IH}$ (MIN).

(2) HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

6 INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC Electronics product in your application, please contact the NEC Electronics office in your country to obtain a list of authorized representatives and distributors. They will verify:

- · Device availability
- · Ordering information
- · Product release schedule
- · Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

[GLOBAL SUPPORT]

http://www.necel.com/en/support/support.html

Santa Clara, California Tel: 408-588-6000 800-366-9782

NEC Electronics America, Inc. (U.S.) NEC Electronics (Europe) GmbH

Duesseldorf, Germany Tel: 0211-65030

• Sucursal en España

Madrid, Spain Tel: 091-504 27 87

• Succursale Française

Vélizy-Villacoublay, France Tel: 01-30-675800

Filiale Italiana

Milano, Italy Tel: 02-66 75 41

• Branch The Netherlands

Eindhoven. The Netherlands Tel: 040-2654010

Tyskland Filial

Taeby, Sweden Tel: 08-63 87 200

United Kingdom Branch

Milton Keynes, UK Tel: 01908-691-133

NEC Electronics Hong Kong Ltd.

Hong Kong Tel: 2886-9318

NEC Electronics Hong Kong Ltd.

Seoul Branch Seoul, Korea Tel: 02-558-3737

NEC Electronics Shanghai Ltd.

Shanghai, P.R. China Tel: 021-5888-5400

NEC Electronics Taiwan Ltd.

Taipei, Taiwan Tel: 02-2719-2377

NEC Electronics Singapore Pte. Ltd.

Novena Square, Singapore

Tel: 6253-8311

J05.6

NEC μ PD703130

Reference materials Electrical Characteristics for Microcomputer (U15170J^{Note})

Note This document number is that of Japanese version.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- The information contained in this document is being issued in advance of the production cycle for the product. The parameters for the product may change before final production or NEC Electronics Corporation, at its own discretion, may withdraw the product prior to its production.
- Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent
 of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property
 rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other
 liability arising from the use of such products. No license, express, implied or otherwise, is granted under any
 patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes
 in semiconductor product operation and application examples. The incorporation of these circuits, software and
 information in the design of a customer's equipment shall be done under the full responsibility of the customer. NEC
 Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of
 these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific".
 The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics products depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.
 - "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.
 - "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).
 - "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.

(Note)

- (1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.
- (2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).