PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD70F3080(A)

V850/DB1™ AVALON 32-/16-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The V850/DB1 ("AVALON") single chip microcontroller, is a member of NEC's V850 32-bit RISC family, which match the performance gains attainable with RISC-based controllers to the needs of embedded control applications. The V850 CPU offers easy pipeline handling and programming, resulting in compact code size comparable to 16-bit CISC CPUs.

The V850/DB1 ("AVALON") offers an excellent combination of general purpose peripheral functions, like serial communication interfaces (UART, clocked SI), display drivers, measurement inputs (A/D converter) and Meter Controller/Driver, with dedicated CAN network support. To support more than one CAN network, two CAN interfaces are implemented on chip.

The device offers power-saving modes to manage the power consumption effectively under varying conditions.

Thus equipped, the V850/DB1 ("AVALON") is ideally suited for automotive applications especial dashboard. It is also an excellent choice for other applications where a combination of sophisticated peripheral functions and CAN network support is required.

Functions in detail are described in the following user's manuals. Be sure to read these manuals when you design your systems.

V850/DB1 User's Manual - Hardware	**: U15011EE2V0UM00**
V850 Family™ User's Manual - Architecture	**: U10243EJ6V0UM00**

FEATURES

- 32-bit RISC CPU with Harvard Architecture
- DCAN Interface: 2 channels
- Serial Interfaces: 5 channels
  - 3-wire mode: 3 channels
  - UART mode: 2 channels
- Timers: 7 channels
  - 16-bit dual timebase timer/event counter: 1 channel
  - 16-bit general purpose timer/event counter: 2 channel
  - 8-bit timer: 2 channel
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- 36 x 4 LCD controller/driver
- Meter Controller/Driver: 6 channels
- 10-bit resolution A/D Converter: 8 channels
- Input/Output lines: 107
  - 83 Input/Output Ports
  - 8 Input Ports
  - 16 Output Ports
- Power supply voltage range: 4.0 V ≤ V_{DD} ≤ 5.5 V
- System Frequency: 16 MHz
- Crystal frequency: 4 MHz
- Built-in low power saving mode
- Built-in clock oscillator circuit with internal PLL
- Vectored interrupts: 45
- Temperature range: -40°C to +85°C
- Package: 128 LQFP, 0.5 mm pin-pitch (20 × 20 mm)

ORDERING INFORMATION

Device	Part Number	Package	ROM	RAM	DCAN Option	Oper. Freq.
V850/DB1	μPD70F3080GJ-UEU	LQFP128 20 × 20 mm	128 K Flash	6 K	2 Channels	16 MHz

The information contained in this document is released in advance of the production cycle for the device. The parameters for the device may change before final production, or NEC Corporation may, at its own discretion, withdraw the device prior to production.

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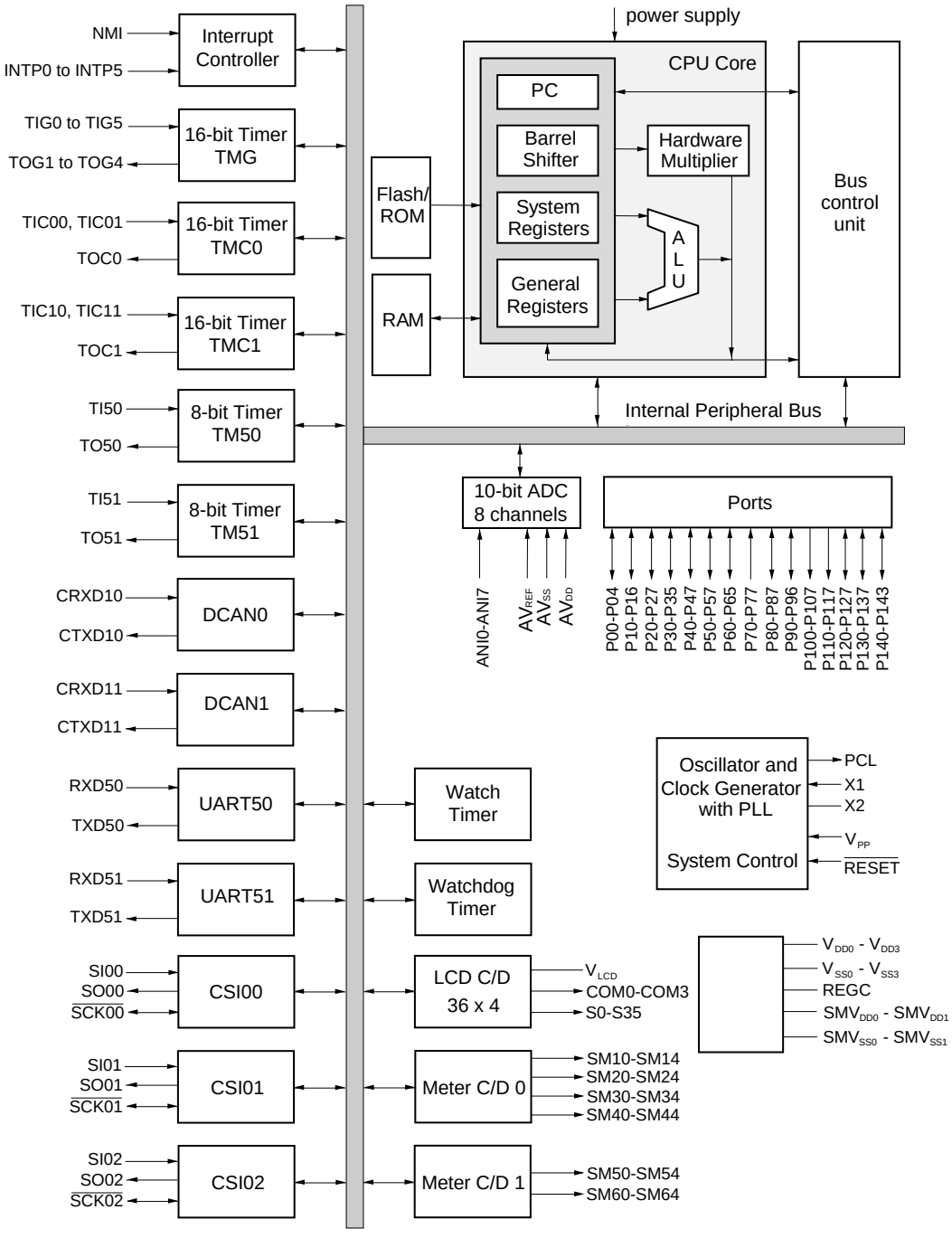
INTERNAL BLOCK DIAGRAM

Figure In-1: Internal Block Diagram



PIN IDENTIFICATION

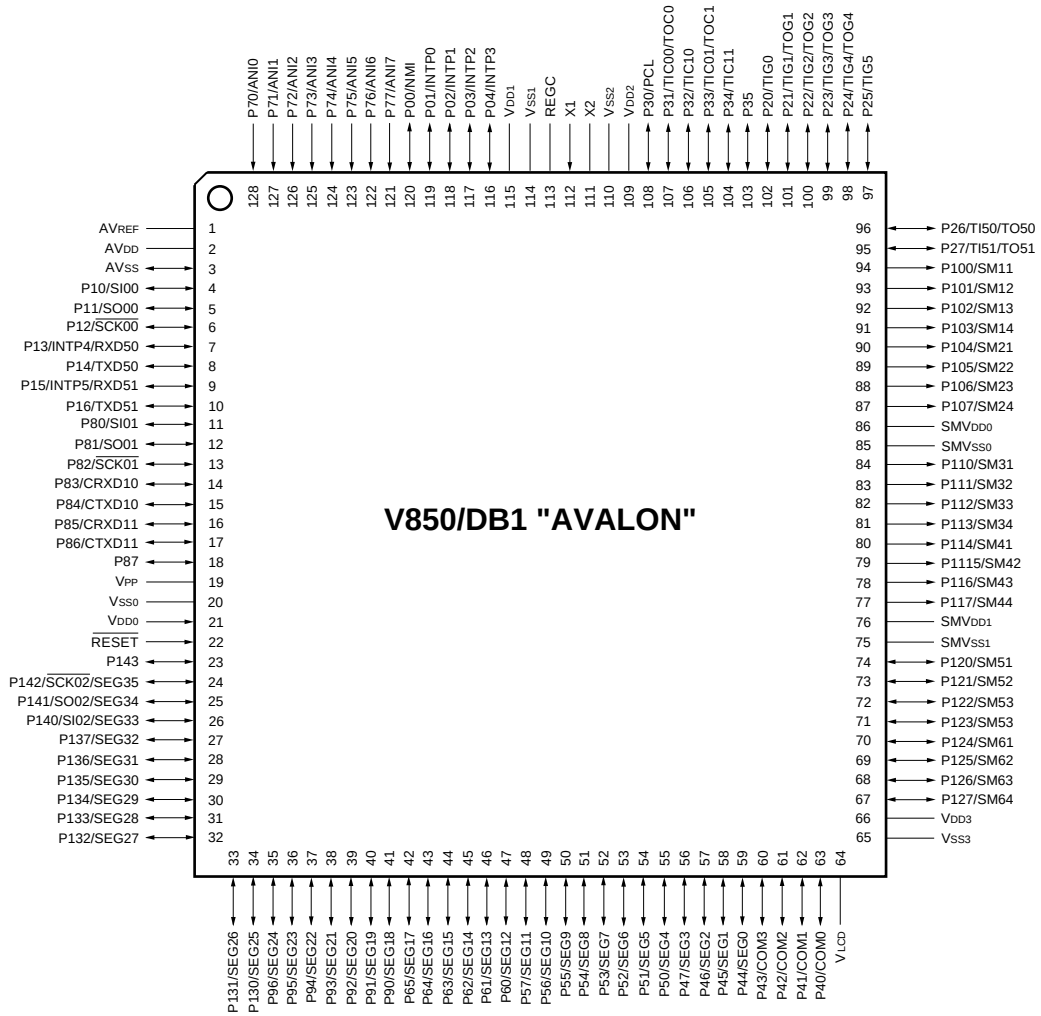
ANI0 to ANI7	Analog Input	$\overline{\text{RESET}}$	Reset Input
AV_{DD}	Analog Power Supply	RXD50, RXD51	UART Receive Data
AV_{REF}	Reference Voltage ADC	$\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$, $\overline{\text{SCK02}}$	Synchronous Interface Clock
AV_{SS}	Ground	SEG0 to SEG35	LCD Segment Line
COM0 to COM3	LCD Common Line	SI00, SI01, SI02	Synchronous Interface Input
CRXD10, CRXD11	CAN Receive Data	SO00, SO01, SO02	Synchronous Interface Output
CTXD10, CTXD11	CAN Transmit Data	SM11 to SM14	Meter C/D Output (channel 1)
INTP0 to INTP5	External Interrupt Input	SM21 to SM24	Meter C/D Output (channel 2)
NMI	Non-Maskable Interrupt Input	SM31 to SM34	Meter C/D Output (channel 3)
P00 to P04	Port 0	SM41 to SM44	Meter C/D Output (channel 4)
P10 to P16	Port 1	SM51 to SM54	Meter C/D Output (channel 5)
P20 to P27	Port 2	SM61 to SM64	Meter C/D Output (channel 6)
P30 to P35	Port 3	SMV_{DD0}, SMV_{DD1}	Power Supply for Stepper Motor Ports
P40 to P47	Port 4	SMV_{SS0}, SMV_{SS1}	Ground for Stepper Motor Ports
P50 to P57	Port 5	TI50, TI51	TM5 Count Input
P60 to P65	Port 6	TIC00, TIC01	TMC0 Capture Input
P70 to P77	Port 7	TIC10, TIC11	TMC1 Capture Input
P80 to P87	Port 8	TIG0 to TIG5	TMG Capture Input
P90 to P96	Port 9	TO50, TO51	TM5 Compare Output
P100 to 107	Port 10	TOC0, TOC1	TMC Compare Output
P110 to P117	Port 11	TOG1 to TOG4	TMG Compare Output
P120 t P127	Port 12	TXD50, TXD51	UART Transmit Data
P130 to P137	Port 13	V_{DD0} to V_{DD3}	Digital Power Supply
P140 to P143	Port 14	V_{LCD}	External LCD Voltage Input
PCL	Processor Clock Output	V_{PP}	Programming Voltage
REGC	Voltage Regulator Output	V_{SS0} to V_{SS3}	Ground
		X1, X2	Main System Clock

1. Pin Functions

128-Pin Plastic LQFP (fine pitch) (20 mm × 20 mm)

- μPD70F3080(A)

Figure 1-1: Pinout



1.1 Port Pins

Table 1-1: Port Pins (1/3)

Pin Name	I/O	Function	Driver Type	Alternate
P00	I/O	Port 0: 5-bit input/output port	8-A	NMI
P01				INTP0
P02				INTP1
P03				INTP2
P04				INTP3
P10	I/O	Port 1: 7-bit input/output port	8-A	SI00
P11			5-A	SO00
P12			8-A	$\overline{\text{SCK00}}$
P13				INTP4/RXD50
P14			5-A	TXD50
P15			8-A	INTP5/RXD51
P16			5-A	TXD51
P20	I/O	Port 2: 8-bit input/output port	8-A	TIG0
P21				TIG1/TOG1
P22				TIG2/TOG2
P23				TIG3/TOG3
P24				TIG4/TOG4
P25				TIG5
P26				TI50/TO50
P27				TI51/TO51
P30	I/O	Port 3: 6-bit input/output port	5-A	PCL
P31			8-A	TIC00/TOC0
P32				TIC10
P33				TIC01/TOC1
P34				TIC11
P35			5-A	-
P40	I/O	Port 4: 8-bit input/output port	18-C	COM0
P41				COM1
P42				COM2
P43				COM3
P44			17-G	SEG0
P45				SEG1
P46				SEG2
P47				SEG3

Table 1-1: Port Pins (2/3)

Pin Name	I/O	Function	Driver Type	Alternate
P50	I/O	Port 5: 8-bit input/output port	17-G	SEG4
P51				SEG5
P52				SEG6
P53				SEG7
P54				SEG8
P55				SEG9
P56				SEG10
P57				SEG11
P60	I/O	Port 6: 6-bit input/output port	17-G	SEG12
P61				SEG13
P62				SEG14
P63				SEG15
P64				SEG16
P65				SEG17
P70	I	Port 7: 8-bit input port	9	ANI0
P71				ANI1
P72				ANI2
P73				ANI3
P74				ANI4
P75				ANI5
P76				ANI6
P77				ANI7
P80	I/O	Port 8: 8-bit input/output port	8-A	SI01
P81			5-A	SO01
P82			8-A	$\overline{\text{SCK01}}$
P83				CRXD10
P84			5-A	CTXD10
P85			8-A	CRXD11
P86			5-A	CTXD11
P87				-
P90	I/O	Port 9: 7-bit input/output port	17-G	SEG18
P91				SEG19
P92				SEG20
P93				SEG21
P94				SEG22
P95				SEG23
P96				SEG24

Table 1-1: Port Pins (3/3)

Pin Name	I/O	Function	Driver Type	Alternate
P100	O	Port 10: 8-bit output port	4	SM11
P101				SM12
P102				SM13
P103				SM14
P104				SM21
P105				SM22
P106				SM23
P107				SM24
P110	O	Port 11: 8-bit output port	4	SM31
P111				SM32
P112				SM33
P113				SM34
P114				SM41
P115				SM42
P116				SM43
P117				SM44
P120	I/O	Port 12: 8-bit input/output port	5	SM51
P121				SM52
P122				SM53
P123				SM54
P124				SM61
P125				SM62
P126				SM63
P127				SM64
P130	I/O	Port 13: 8-bit input/output port	17-G	SEG25
P131				SEG26
P132				SEG27
P133				SEG28
P134				SEG29
P135				SEG30
P136				SEG31
P137				SEG32
P140	I/O	Port 14: 4-bit input/output port	17-G	SI02/SEG33
P141			17-G	SO02/SEG34
P142			17-G	$\overline{\text{SCK02}}$/SEG35
P143			5	-

1.2 Non-port Pins

Table 1-2: Non-port Pins (1/2)

Pin Name	I/O	Function	Alternate Function
Only Port Pins	I/O	Input/output port	P35, P87, P143
ANI0 to ANI7	Input	A/D converter input pin	P70 to P77
AV_{DD}	-	Power supply pin for A/D converter	-
AV_{REF}	-	Reference-Voltage supply pin for A/D converter	-
AV_{SS}	-	Ground potential for A/D converter	-
COM0 to COM3	Output	LCD common signal output pin	P40 to P43
CRXD10	Input	CAN channel 0 serial data input pin	P83
CRXD11	Input	CAN channel 1 serial data input pin	P85
CTXD10	Output	CAN channel 0 serial data output pin	P84
CTXD11	Output	CAN channel 1 serial data output pin	P86
INTP0 to INTP3	Input	Maskable interrupt input pin	P01 to P04
INTP4	Input	Maskable interrupt input pin	P13/RXD50
INTP5	Input	Maskable interrupt input pin	P15/RXD51
NMI	Input	Non-maskable interrupt input pin	P00
PCL	Output	Clock output pin	P30
REGC	-	Pin for external 3.3 V Back-Up-Capacitor	-
$\overline{RESET}$	Input	System reset input	-
RXD50	Input	Serial data input channel 0 pin	P13/INTP4
RXD51	Input	Serial data input channel 1 pin	P15/INTP5
$\overline{SCK00}$	I/O	Serial clock input channel 0 pin	P12
$\overline{SCK01}$	I/O	Serial clock input channel 1 pin	P82
$\overline{SCK02}$	I/O	Serial clock input channel 2 pin	P142/SEG35
SEG0 to SEG3	Output	LCD segment signal output pin	P44 to P47
SEG4 to SEG11	Output	LCD segment signal output pin	P50 to P57
SEG12 to SEG17	Output	LCD segment signal output pin	P60 to P65
SEG18 to SEG24	Output	LCD segment signal output pin	P90 to P96
SEG25 to SEG32	Output	LCD segment signal output pin	P130 to P137
SEG33	Output	LCD segment signal output pin	P140/SI02
SEG34	Output	LCD segment signal output pin	P141/SO02
SEG35	Output	LCD segment signal output pin	P142/$\overline{SCK02}$
SI00	Input	Serial data input channel 0 pin	P10
SI01	Input	Serial data input channel 1 pin	P80
SI02	Input	Serial data input channel 2 pin	P140/SEG33
SM11 to SM24	Output	Meter drive output pin	P100 to P107
SM31 to SM44	Output	Meter drive output pin	P110 to P117
SM51 to SM64	Output	Meter drive output pin	P120 to P127
SMV_{DD0}	-	Power supply pin for Meter Controller/Driver for SM11 - SM34 P100 - P107, P110 - P113	-
SMV_{DD1}	-	Power supply pin for Meter Controller/Driver for SM41 - SM64 P114 - P117, P120 - P127	-

Table 1-2: Non-port Pins (2/2)

Pin Name	I/O	Function	Alternate Function
SMV_{SS0}	-	Ground potential for Meter Controller/Driver for SM11 - SM34 P100 - P107, P110 - P113	-
SMV_{SS1}	-	Ground potential for Meter Controller/Driver for SM41 - SM64 P114 - P117, P120 - P127	-
SO00	Output	Serial data output channel 0 pin	P11
SO01	Output	Serial data output channel 1 pin	P81
SO02	Output	Serial data output channel 2 pin	P141/SEG34
TI50	Input	Event counter input channel 0 pin	P26/TO50
TI51	Input	Event counter input channel 1 pin	P27/TO51
TIC00	Input	Timer C0 Capture trigger input pin	P31/TOC0
TIC01	Input	Timer C1 Capture trigger input pin	P33/TOC1
TIC10	Input	Timer C0 Capture trigger input pin	P32
TIC11	Input	Timer C1 Capture trigger input pin	P34
TIG0	Input	Timer G Capture trigger input pin	P20
TIG5	Input	Timer G Capture trigger input pin	P25
TO50	Output	Timer 50 PWM output channel 0 pin	P26/TI50
TO51	Output	Timer 51 PWM output channel 1 pin	P27/TI51
TOC0	Output	Timer C0 output pin	P31/TIC00
TOC1	Output	Timer C1 output pin	P33/TIC01
TOG1 to TOG4	Output	Timer G PWM output pin	P21 to P24
TXD50	Output	Serial data output channel 0 pin	P14
TXD51	Output	Serial data output channel 1 pin	P16
V_{DD0} to V_{DD3}	-	Power supply pin	-
V_{LCD}	-	Power supply pin for external LCD-Voltage supply	-
V_{PP}	-	High Voltage apply pin for program write/verify	-
V_{SS0} to V_{SS3}	-	GND potential pin	-
X1, X2	-	Resonator connection for main-clock	-

1.3 Unused pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in the following Table.

Table 1-3: Recommended Connection for Unused Pins (1/4)

Pin Name	I/O	I/O Circuit Type	Recommend Connection for Unused Pins
P00/INTP0	I/O	8-A	For input: Individually connect to V_{DD} or V_{SS} via a resistor For output: Leave open
P01/INTP1			
P02/INTP2			
P03/INTP3			
P04/INTP4			
P10/SI00	I/O	8-A	For input: Individually connect to V_{DD} or V_{SS} via a resistor For output: Leave open
P11/SO00		5-A	
P12/$\overline{\text{SCK00}}$		8-A	
P13/INTP5/RXD50			
P14/TXD50		5-A	
P15/INTP6/RXD51		8-A	
P16/TXD51		5-A	
P20/TIG0	I/O	8-A	For input: Individually connect to V_{DD} or V_{SS} via a resistor For output: Leave open
P21/TIOG1			
P22/TIOG2			
P23/TIOG3			
P24/TIOG4			
P25/TIG5			
P26/TIO50			
P27/TIO51			
P30/PCL	I/O	5-A	
P31/TIC00/TOC0		8-A	
P32/TIC10			
P33/TIC01/TOC1			
P34/TIC11			
P35		5-A	
P40/COM0	I/O	18-C	For input: Individually connect to V_{DD} or V_{SS} via a resistor For output: Leave open
P41/COM1			
P42/COM2			
P43/COM3			
P44/SEG0		17-G	
P45/SEG1			
P46/SEG2			
P47/SEG3			

Table 1-3: Recommended Connection for Unused Pins (2/4)

Pin Name	I/O	I/O Circuit Type	Recommend Connection for Unused Pins
P50/SEG4	I/O	17-G	For input: Individually connect to V_{DD} or V_{SS} via a resistor For output: Leave open
P51/SEG5			
P52/SEG6			
P53/SEG7			
P54/SEG8			
P55/SEG9			
P56/SEG10			
P57/SEG11			
P60/SEG12	I/O	17-G	For input: Individually connect to V_{DD} or V_{SS} via a resistor For output: Leave open
P61/SEG13			
P62/SEG14			
P63/SEG15			
P64/SEG16			
P65/SEG17			
P70/ANI0	I	9	Individually connect to AV_{DD} or AV_{SS} via a resistor
P71/ANI1			
P72/ANI2			
P73/ANI3			
P74/ANI4			
P75/ANI5			
P76/ANI6			
P77/ANI7			
P80/SI01	I/O	8-A	For input: Individually connect to V_{DD}or V_{SS} via a resistor For output: Leave open
P81/SO01		5-A	
P82/$\overline{\text{SCK01}}$		8-A	
P83/CRXD10			
P84/CTXD10		5-A	
P85/CRXD11		8-A	
P86/CTXD11		5-A	
P87			
P90/SEG18	I/O	17-G	For input: Individually connect to V_{DD} or V_{SS} via a resistor For output: Leave open
P91/SEG19			
P92/SEG20			
P93/SEG21			
P94/SEG22			
P95/SEG23			
P96/SEG24			

Table 1-3: Recommended Connection for Unused Pins (3/4)

Pin Name	I/O	I/O Circuit Type	Recommend Connection for Unused Pins
P100/SM11	O	4	Leave open
P101/SM12			
P102/SM13			
P103/SM14			
P104/SM21			
P105/SM22			
P106/SM23			
P107/SM24			
P110/SM31	O	4	Leave open
P111/SM32			
P112/SM33			
P113/SM34			
P114/SM41			
P115/SM42			
P116/SM43			
P117/SM44			
P120/SM51	I/O	5	For input: Individually connect to SMV_{DD} or SMV_{SS} via a resistor For output: Leave open
P121/SM52			
P122/SM53			
P123/SM54			
P124/SM61			
P125/SM62			
P126/SM63			
P127/SM64			
P130/SEG25	I/O	17-G	For input: Individually connect to V_{DD} or V_{SS} via a resistor For output: Leave open
P131/SEG26			
P132/SEG27			
P133/SEG28			
P134/SEG29			
P135/SEG30			
P136/SEG31			
P137/SEG32			
P140/SI02/SEG33	I/O	17-G	
P141/SO02/SEG34		17-G	
P142/$\overline{SCK02}$/SEG35		17-G	
P143		5	
X1,X2	-	-	-
$\overline{RESET}$	-	-	-
V_{LCD}	-	-	Leave open
SMV_{DD0} [for SM11-SM34]	-	-	-

Table 1-3: Recommended Connection for Unused Pins (4/4)

Pin Name	I/O	I/O Circuit Type	Recommend Connection for Unused Pins
SMV_{DD1} [for SM41-SM64]	-	-	-
SMV_{SS0} [for SM11-SM34]	-	-	-
SMV_{SS1} [for SM41-SM64]	-	-	-
V_{DD0}[for External]	-	-	-
V_{DD1}[for Internal]	-	-	-
V_{DD2}[for External]	-	-	-
V_{DD3}[for External]	-	-	-
V_{SS0}[for External]	-	-	-
V_{SS1}[for Internal]	-	-	-
V_{SS2}[for External]	-	-	-
V_{SS3}[for External]	-	-	-
AV_{DD}	-	-	Connect to V_{DD}
AV_{REF}	-	-	
AV_{SS}	-	-	Connect to V_{SS}
V_{PP}	-	-	
REGC	-	-	-

For the input/output schematic circuit diagram of each type, refer to the Figures 1-2 and 1-3.

1.4 I/O Circuits

Figure 1-2: Driver Types (4, 5, 5-A, 8-A, 9)

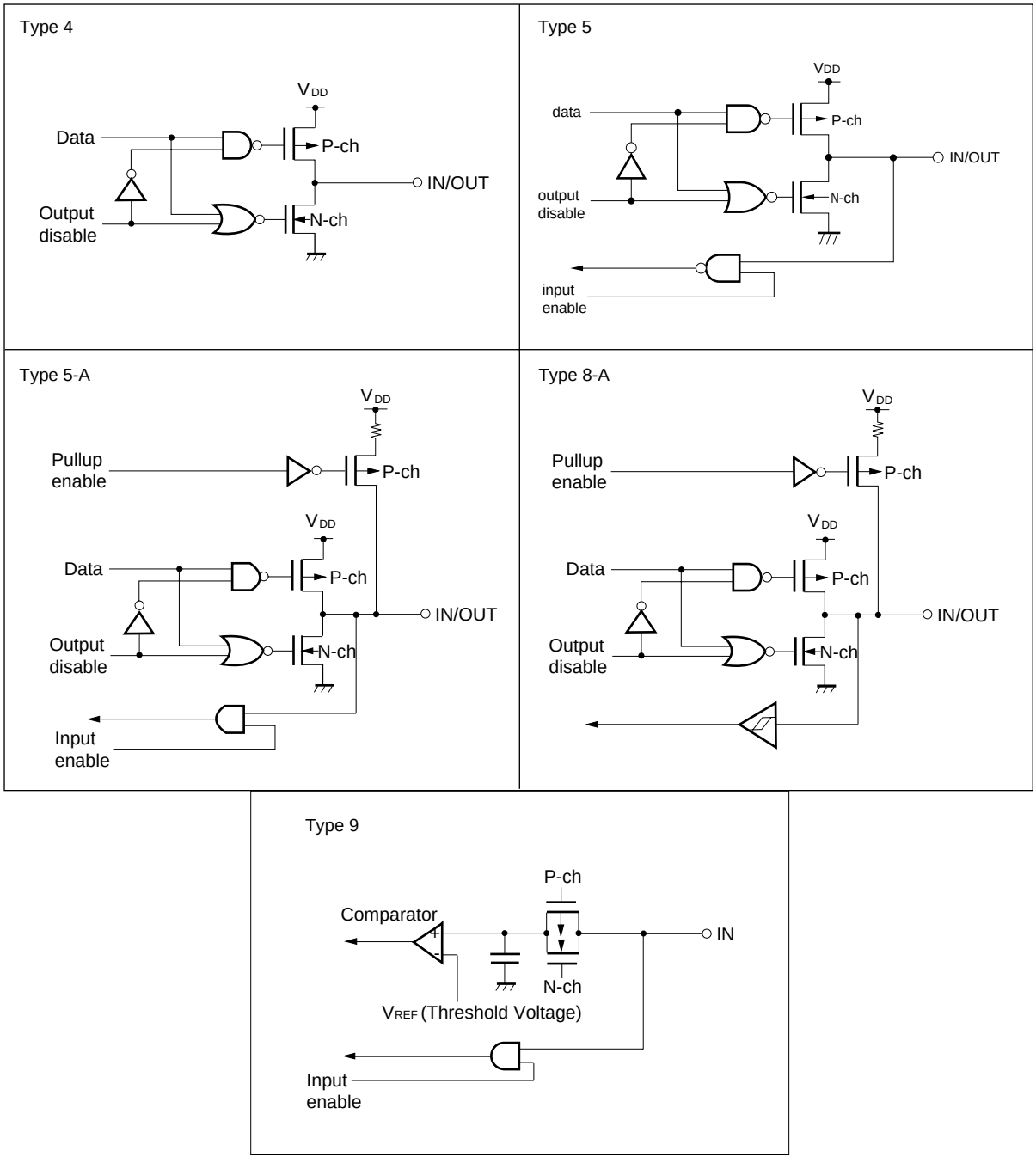
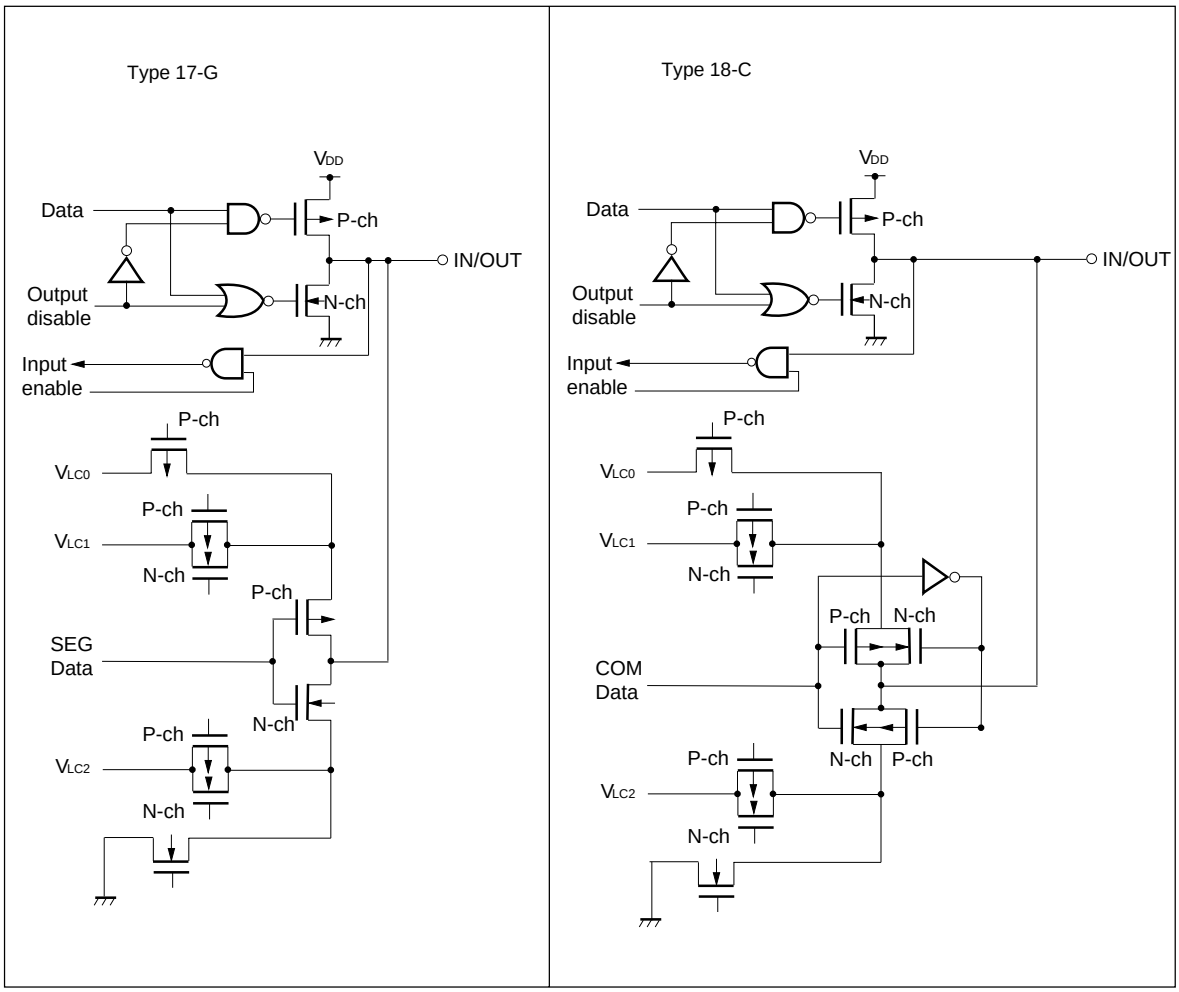


Figure 1-3: Driver Types (17-G, 18-C)



2. Programming Flash Memory

The device μPD70F3080(A) supports the programming of the internal flash in two ways: either by using the *flash*MASTER programming tool or by performing self-programming using software functions and I/O communications.
For programming details about both methods, see the User's Manual. For timing characteristics about the initial programming using *flash*MASTER and some more electrical data about the Flash Memory, see Section 3.5 "Flash EEPROM Characteristics" on page 33.

3. Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3-1: Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}	$V_{DD0} = V_{DD1} = V_{DD2} = V_{DD3}$		-0.5 ~ +6.0	V
	V_{SS}	$V_{SS0} = V_{SS1} = V_{SS2} = V_{SS3}$		-0.5 ~ +0.5	V
	SMV_{DD}	$SMV_{DD} = V_{DD}$		-0.5 ~ +6.0	V
	SMV_{SS}	$SMV_{SS} = V_{SS}$		-0.5 ~ +0.5	V
	AV_{DD}	$AV_{DD} \leq V_{DD}$		-0.5 ~ +6.0	V
	AV_{REF}	$AV_{REF} \leq 6.0$ V		-0.5 ~ AV_{DD} +0.5	V
	AV_{SS}			-0.5 ~ +0.5	V
Input voltage	V_I			-0.5 ~ V_{DD} +0.5	V
	V_{PP}	Normal operating mode		-0.5 ~ V_{DD} +0.5	V
		Flash programming mode		-0.5 ~ +8.5	V
Analog input voltage	V_{AN}	ANI0 - ANI7 ≤ 6.0 V		-0.5 ~ AV_{DD} +0.5	V
High level output current	I_{OH}	P10 - P16, P40 - P47, P50 -P57, P60 - P65, P80 - P87, P90 - P96, P130 - P137, P140 - P143	1 pin	-4	mA
			Total	-70	mA
		P00 - P04, P20 - P27, P30 - P35	1 pin	-4	mA
			Total	-70	mA
		P100 - P107, P110 - P113	1 pin	-45	mA
			Total	-200	mA
		P114 - P117, P120 - P127	1 pin	-45	mA
			Total	-200	mA
Low level output current	I_{OL}	P10 - P16, P40 - P47, P50 - P57, P60 - P65, P80 - P87, P90 - P96, P130 - P137, P140 - P143	1 pin	4	mA
			Total	70	mA
		P00 - P04, P20 - P27, P30 - P35	1 pin	4	mA
			Total	70	mA
		P100 - P107, P110 - P113	1 pin	45	mA
			Total	200	mA
		P114 - P117, P120 - P127	1 pin	45	mA
			Total	200	mA
Operating ambient temperature	T_A	Normal operating mode		-40 ~ +85	°C
		Flash programming mode		-20 ~ +85	°C
Storage temperature	T_{STG}	Before flash program		-55 ~ +125	°C

3.2 General Characteristics

3.2.1 Oscillation Circuit

Table 3-2: Main System Clock Oscillation Circuit Characteristics

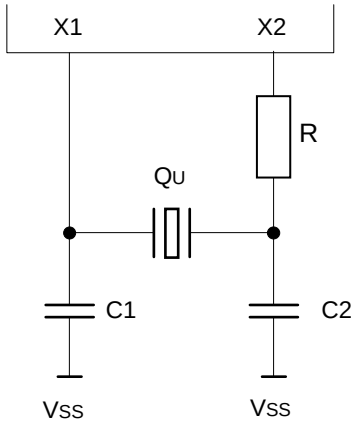
(T_A = - 40 to +85°C, V_{DD} = SMV_{DD} = 4.0 to 5.5 V, V_{SS} = SMV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN	TYP	MAX	Unit
Ceramic resonator	Refer to Figure 3-1	Oscillator frequency (f_X)**Note1**		4		4	MHz
		Oscillation stabilization time**Note2**	After V_{DD} reaches oscillator voltage range MIN. 4.0 V			8	ms
Crystal resonator	Refer to Figure 3-1	Oscillator frequency (f_X)**Note1**		4		4	MHz
		Oscillation stabilization time**Note2**	After V_{DD} reaches oscillator voltage range MIN. 4.0 V			8	ms

Notes: 1. Indicates only the oscillation circuit characteristics. Refer to “AC Characteristic” for CPU operation clock.

2. Time required to stabilize oscillation after reset or STOP mode release.

Figure 3-1: Schematic of Oscillator Circuit



Note: Values of capacitors C1, C2 depends on used resonator and must be specified in cooperation with the resonator manufacturer.

Table 3-3: Standby Mode Characteristics

(T_A = -40 to +85°C, V_{DD} = SMV_{DD} = 4.0 to 5.5 V, V_{SS} = SMV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Watch mode release time	t_{WATCH}	After watch mode release	1 **Note**			ms
Stop mode release time	t_{STOP}	After stop mode release	8 **Note**			ms

Note: Minimum time, which is required for internal stabilization. The OSTS register has to be set to a time, which is longer than above defined values, before entering either WATCH or STOP mode.

Table 3-4: Capacitance

(T_A = 25°C, V_{DD} = SMV_{DD} = V_{SS} = AV_{DD} = AV_{REF} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Input capacitance	C_I	f = 1 MHz Other than measured pins: 0 V	P70 - P77			15	pF
Input/output capacitance	C_{IO}		P00 - P04, P10 -P16, P20 - P27, P30 -P35, P40 - P47, P50 - P57, P60 - P65, P80 -P87, P90 - P96, P130 -P137, P140 - P143			15	pF
			P120 - P127			40	pF
Output capacitance	C_O		P100 - P107, P110 - P117			40	pF

3.3 DC Characteristics

Table 3-5: DC Characteristics (1/2)

(T_A = -40 to +85°C, V_{DD} = SMV_{DD} = 4.0 to 5.5 V, 4.5 V ≤ AV_{DD} ≤ V_{DD}, V_{SS} = SMV_{SS} = AV_{SS} = 0 V)

Parameter	Sym-bol	Conditions	MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH1}	P11, P14, P16, P30, P35, P40-P47, P50-P57, P60-P65, P81, P84, P86, P87, P90-P96, P130-P137, P140-P143	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00-P04, P10, P12, P13, P15, P20-P27, P31-P34, P80, P82	0.8 V_{DD}		V_{DD}	V
	V_{IH3}	P83, P85	0.8 V_{DD}		V_{DD}	V
	V_{IH4}	P70-P77**Note**	0.7 AV_{DD}		AV_{DD}	V
	V_{IH5}	P120-P127	0.7 SMV_{DD}		SMV_{DD}	V
	V_{IH6}	$\overline{RESET}$	0.8 V_{DD}		V_{DD}	V
Low level input voltage	V_{IL1}	P11, P14, P16, P30, P35, P40-P47, P50-P57, P60-P65, P81, P84, P86, P87, P90-P96, P130-P137, P140-P143	V_{SS}		0.3 V_{DD}	V
	V_{IL2}	P00-P04, P10, P12, P13, P15, P20-P27, P31-P34, P80, P82	V_{SS}		0.2 V_{DD}	V
	V_{IL3}	P83, P85	V_{SS}		0.4 V_{DD}	V
	V_{IL4}	P70-P77**Note**	AV_{SS}		0.3 AV_{DD}	V
	V_{IL5}	P120-P127	SMV_{SS}		0.3 SMV_{DD}	V
	V_{IL6}	$\overline{RESET}$	V_{SS}		0.2 V_{DD}	V
High level output voltage	V_{OH1}	I_{OH} = -1.0 mA	V_{DD} - 1.0		V_{DD}	V
		I_{OH} = -100 μA	V_{DD} - 0.5		V_{DD}	V
	V_{OH2}	SMV_{DD} = 4.5 to 5.5 V AOUT bit = 0 (Meter PWM mode)	SMV_{DD} - 0.5		SMV_{DD}	V
		P100-P107, P110-P117, P120-P127: I_{OH} = -27 mA (T_A = 85°C); I_{OH} = -30 mA (T_A = 25°C); I_{OH} = -40 mA (T_A = -40°C)				
	V_{OH3}	SMV_{DD} = 4.5 to 5.5 V AOUT bit = 1 (PWM mode)	SMV_{DD} - 0.5		SMV_{DD}	V
		P100-P107, P110-P113: I_{OH} = -27 mA/pin, I_{OH} = -120 mA/total				
		P114-P117, P120-P127: I_{OH} = -27 mA/pin, I_{OH} = -120 mA/total				

Note: Can only be use as digital input port when AV_{DD} = V_{DD}.

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

Table 3-5: DC Characteristics (2/2)

(T_A = -40 to +85°C, V_{DD} = SMV_{DD} = 4.0 to 5.5 V, 4.5 V ≤ AV_{DD} ≤ V_{DD}, V_{SS} = SMV_{SS} = AV_{SS} = 0 V)

Parameter	Sym-bol	Conditions		MIN.	TYP.	MAX.	Unit
Low level output voltage	V_{OL1}	I_{OL} = 1.6 mA		0		1.0	V
		I_{OL} = 400 μA		0		0.5	V
	V_{OL2}	SMV_{DD} = 4.5 to 5.5 V AOUT bit = 0 (Meter PWM mode)		0		0.5	V
		P100-P107, P110-P117, P120-P127	I_{OL} = 27 mA (T_A = 85°C) I_{OL} = 30 mA (T_A = 25°C) I_{OL} = 40 mA (T_A = -40°C)				
	V_{OL3}	SMV_{DD} = 4.5 to 5.5 V AOUT bit = 1 (PWM mode)		0		0.5	V
		P100-P107, P110-P113	I_{OL} = 27 mA/pin I_{OL} = 120 mA/total				
		P114-P117, P120-P127	I_{OL} = 27 mA/pin I_{OL} = 120 mA/total				
High level input leakage current	I_{LIH1}	$V_I = V_{DD}$	Except for X1, X2			5	μA
Low level input leakage current	I_{LIL1}	V_I = 0 V	Except for X1, X2			-5	μA
High level output leakage current	I_{LOH1}	$V_O = V_{DD}$	Except for X1, X2			5	μA
Low level output leakage current	I_{LOL1}	V_O = 0 V	Except for X1, X2			-5	μA
Software pull-up resistor	R1	V_I = 0 V		10	30	100	kΩ

Remark: The characteristics of the dual-function pins are the same as those of the port pins unless otherwise specified.

3.3.1 Supply Current

(T_A = -40 to +85°C, V_{DD} = SMV_{DD} = 4.0 to 5.5 V, 4.5 V ≤ AV_{DD} ≤ V_{DD}, V_{SS} = SMV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current **Note**	I_{DD1}	Operating mode	f_{XX} = 16 MHz, PCC = 00H		36	72	mA
	I_{DD2}	HALT mode			10	20	mA
	I_{DD3}	WATCH mode			500	1000	μA
	I_{DD4}	STOP mode			10	60	μA

Note: AV_{REF}, SMV_{DD} current, port current (including a current flowing through the on-chip pull-up resistors) and LCD split resistors are not included.

3.3.2 LCD C/D 1/3 bias method

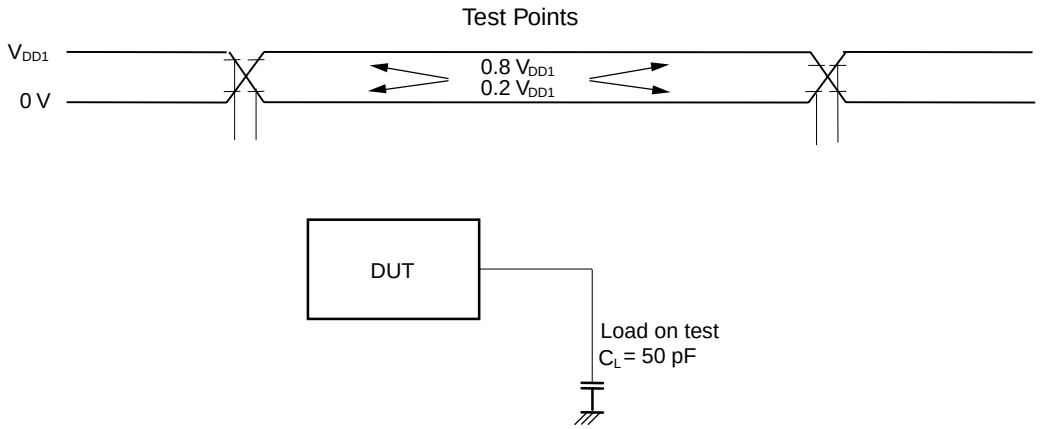
(T_A = -40 to +85°C, V_{DD} = 4.0 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			4.0		V_{DD}	V
LCD split resistor	R_{LCD}	Total split resistor		15	45		kΩ
LCD output voltage deviation **Note** (COM)	V_{ODC}	I_O = ±5 μA	4.0 V ≤ V_{LCD} ≤ V_{DD} V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD} x 2/3 V_{LCD2} = V_{LCD} x 1/3	0		±0.2	V
LCD output voltage deviation **Note** (SEG)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Note: The voltage deviation is the difference from the output voltage corresponding to the ideal value (V_{LCD0} to V_{LCD2}) of the segment and common output.

3.4 AC Characteristics

Figure 3-2: AC Test Input Waveform, AC Test Load Condition



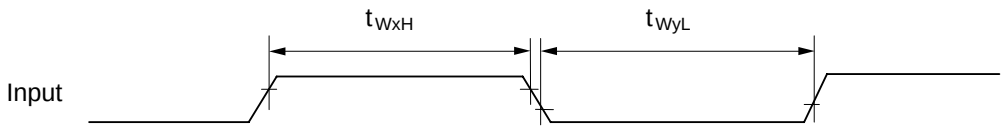
General (if not otherwise noted):

(T_A = -40 to +85°C, V_{DD} = SMV_{DD} = 4.0 to 5.5 V, V_{SS} = SMV_{SS} = 0 V, Output port load capacitance = 50 pF)

3.4.1 Basic Operation

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU Operation clock	f_{CPU}				16	MHz
$\overline{\text{RESET}}$ input low level width	t_{WRSL}		500			ns
NMI input high level width	t_{WNIH}	analog filter	500			ns
NMI input low level width	t_{WNIL}	analog filter	500			ns
INTPn input high level width	t_{WITH}	analog filter, n = 0 - 5	500			ns
INTPn input low level width	t_{WITL}	analog filter, n = 0 - 5	500			ns

Figure 3-3: Basic Operation Timing



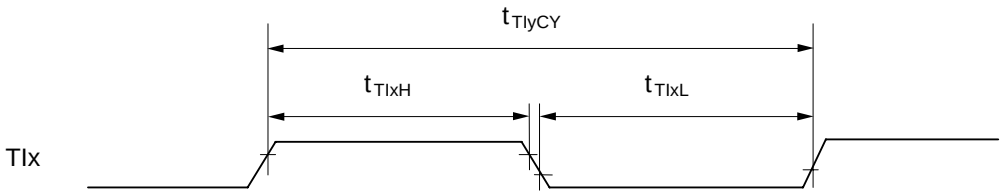
Remark: x = NI, IT
y = RS, NI, IT

3.4.2 TIx input timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TIGn input high level width	t_{TIGH}	n = 0 to 5	**Note**			ns
TIGn input low level width	t_{TIGL}	n = 0 to 5	**Note**			ns
TICn input high level width	t_{TICH}	n = 00, 10, 01, 11	145			ns
TICn input low level width	t_{TICL}	n = 00, 10, 01, 11	145			ns
TI5n input cycle time	t_{TI5CY}	n = 0, 1	120			ns
TI5n input high level width	t_{TI5H}	n = 0, 1	48			ns
TI5n input low level width	t_{TI5L}	n = 0, 1	48			ns

Note: TMG0/TMG1 count clock x 2 + 20

Figure 3-4: TIx Input Timing



Remark: x = G, C, 5

y = 5

3.4.3 Serial Interfaces

(1) DCAN0, DCAN1

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		f_{XX} = 16 MHz			1	Mbps

(2) UART50, UART51

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					312.5	kbps

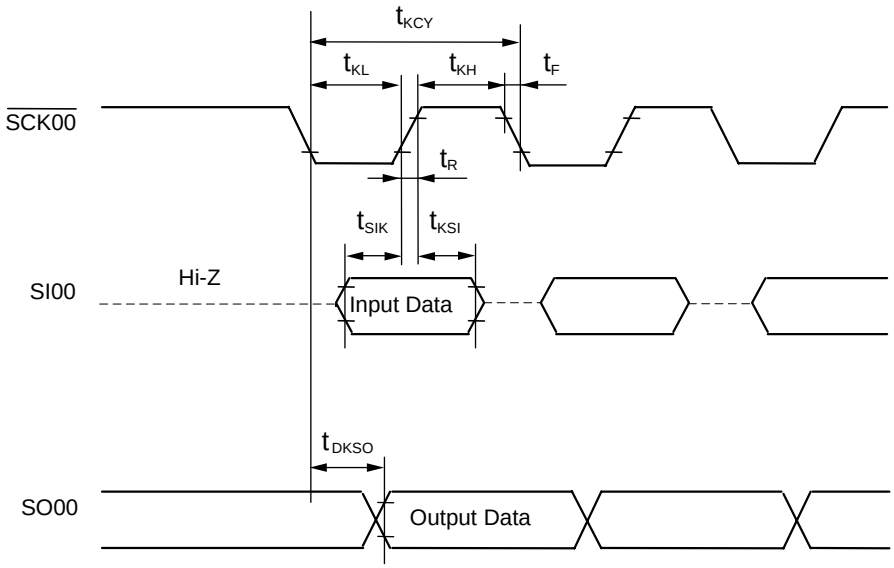
(3) CSI00, CSI01, CSI02 (Master Mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0n}$ cycle time	t_{KCYM}	n = 0 to 2	200			ns
$\overline{SCK0n}$ high/low level width	t_{KHM}, t_{KLM}	n = 0 to 2	$(t_{KCY1}/2) - 10$			ns
SI0n setup time (v.s. $\overline{SCK0n}$)	t_{SIKM}	n = 0 to 2	30			ns
SI0n hold time (v.s. $\overline{SCK0n}$)	t_{KSIM}	n = 0 to 2	30			ns
SO0n output delay time (v.s. $\overline{SCK0n}$)	t_{DKSOM}	n = 0 to 2			30	ns

(4) CSI00, CSI01, CSI02 (Slave Mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0n}$ cycle time	t_{KCYS}	n = 0 to 2	200			ns
$\overline{SCK0n}$ high/low level width	t_{KHS}, t_{KLS}	n = 0 to 2	$(t_{KCY2}/2) - 10$			ns
$\overline{SCK0n}$ rise/fall time	t_{RS}, t_{FS}	n = 0 to 2			50	ns
SI0n setup time (v.s. $\overline{SCK0n}$)	t_{SIKS}	n = 0 to 2	50			ns
SI0n hold time (v.s. $\overline{SCK0n}$)	t_{KSIS}	n = 0 to 2	50			ns
SO0n output delay time (v.s. $\overline{SCK0n}$)	t_{DKSOS}	n = 0 to 2			50	ns

Figure 3-5: CSI Slave Mode Characteristics



3.4.4 A/D Converter Characteristics

(4.5 V ≤ AV_{DD} ≤ V_{DD}, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error **Note**					±0.5	%FSR
Conversion time	t_{CONV}		5		12	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		4.5		AV_{DD}	V
AV_{REF} current	I_{AVREF}	A/D Converter is operating		1.0	2.0	mA
		A/D Converter is stopped		1	10	μA

Note: Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

3.4.5 Voltage Regulator

(T_A = -40 to +85°C, V_{DD} = 4.0 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage stabilization time	t_{REG}	After V_{DD} reaches operating voltage range MIN. 4.0 V (C = 22 μF) **Note**			1	ms

Note: The recommended nominal Capacitor value is 22 μF with a maximum tolerance of ± 30% overall. It have to be remarked that tolerance, temperature and aging effects can reduce the actual value of the capacitor.

3.4.6 Data Retention Characteristics

Data memory stop mode low supply voltage data retention characteristics (T_A = -40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}	STOP mode	3.8		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 3.8 V		10	60	μA
STOP release signal input time	t_{DREL}	After V_{DD} reaches operating voltage range MIN. 4.0 V	0			μs

3.5 Flash EEPROM Characteristics

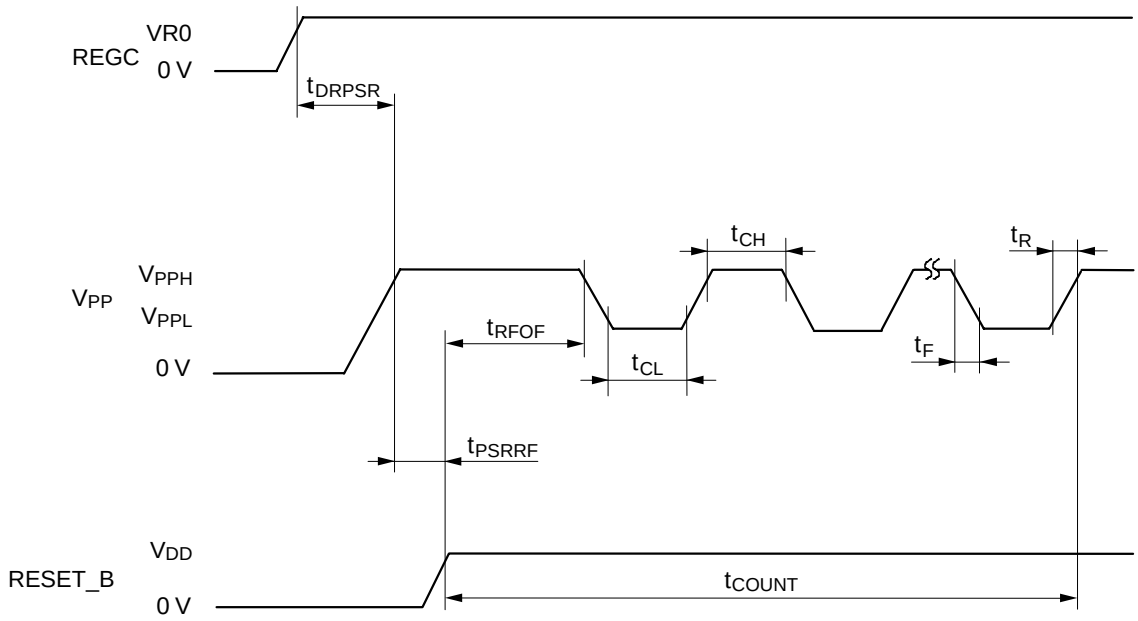
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{FLASH}		4		16	MHz
Supply voltage	V_{DD}		4.0		5.5	V
	V_{PP}	V_{DD} High level detect	0.8 V_{DD}	V_{DD}	1.2 V_{DD}	V
	V_{PPH}	Programming mode	7.5	7.8	8.1	V
V_{PP} supply current	I_{PP}	Programming mode		40	80	mA
Minimum times of reprogramming	C_{WRT}		100			times
Write time	t_{WRT}	Byte **Note**		20	200	μs
Write back time	t_{WRTB}	Block (4 K Bytes) **Note**		1	300	ms
Erase time	t_{ERASEB}	Block (64 K Bytes) **Note**		0.2	20	s
	t_{ERASEC}	Chip (128 K Bytes) **Note**		0.4	40	s
Programming temperature	T_{PRG}		0		+70	°C

Note: Exclusive recovery time, firmware execution and verify.

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} ↑ setup time (to V_{PP} ↑)	t_{DRPSR}		10			μs
V_{PP} ↑ setup time (to $\overline{RESET}$ ↑)	t_{PSRRF}		1			μs
$\overline{RESET}$ ↑ count start setup time (to V_{PPH} level)	t_{RFOF}	$V_{PP} = V_{PPH}$ $T = 1/f_{XX}$	5T + 500			μs
Times of V_{PP} counting	t_{COUNT}				10	ms
V_{PP} count Hi/Low level width	t_{CH}/t_{CL}		1			μs
V_{PP} count rise/fall time	t_R/t_F				250	μs

Note: Exclusive recovery time, firmware execution and verify.

Figure 3-6: Flash EPROM Serial Programming Operation Characteristics

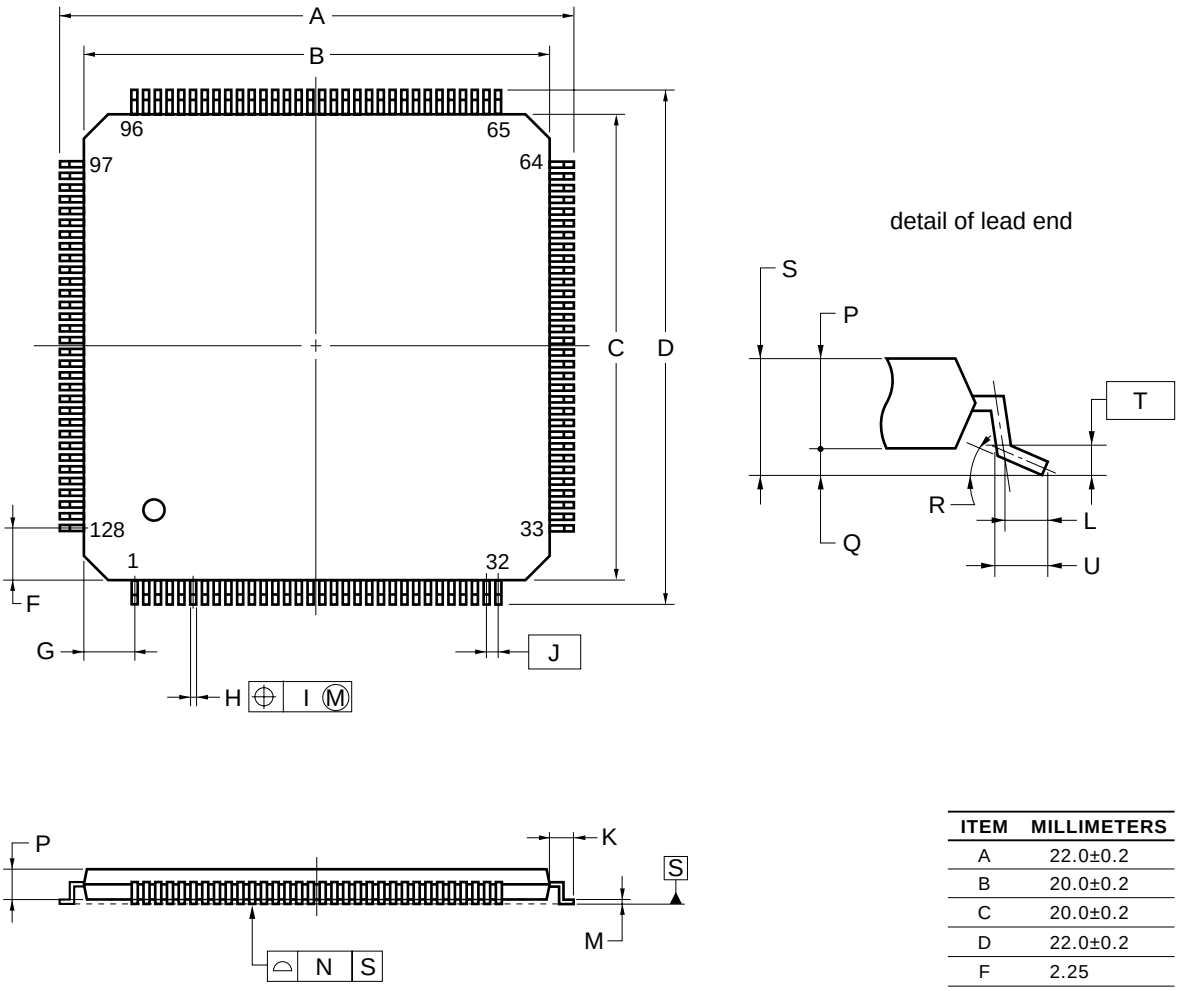


Remark: VRO: Internal Voltage Regulator Output

4. Package Drawing

Figure 4-1: Package Drawing

128-PIN PLASTIC LQFP (FINE PITCH) (20x20)



ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	2.25
G	2.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.6 MAX.
T	0.25
U	0.60±0.15

P128GJ-50-UEU

Note: Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

5. Recommended Soldering Conditions

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to information document Semiconductor Device:

Mounting Technology Manual (C10535E).

For soldering methods and conditions other than those recommended please consult NEC.

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max., Number of days: 3 **Note**	IR30-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	P300

Note: After that, prebaking is necessary at 125°C for 10 hours.
The number of days refers to storage at 25°C, 65% RH MAX after the dry pack has been opened.

Caution: Do not use two or more soldering methods in combination (except partial heating method).

6. Revision History

Rev.	Date	Author	Modifications

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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