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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS Integrated Circuit

V850ES/IE2

32-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The V850ES/IE2 is a 32-bit single chip microcontroller of the V850ES series. 32-bit CPU, ROM, RAM, timer/counters, serial interface, A/D converter, Inverter control function and so on are integrated on a single chip.

FEATURES

- V850ES core, 32-bit RISC architecture
- Instruction execution time: 50ns(min.) @20MHz , Integrated PLL(x8) circuit
- On-chip FlsahROM , RAM

Type / Part Number	Program Memory (Flash Memory Size)	Data Memory (RAM Size)
μPD70F3713	**64KB**	**6KB**
μPD70F3714	**128KB**	**6KB**

- Timer:
  - 16-bit timer (Type TMP) : 4 channels
  - 16-bit timer (Type TMQ) : 2 channels
    (The TMQ1(TimerQ1) and the TMQOP1(TMQ1 option) can be used as an inverter control function.
  - 16-bit timer (Type TMM) : 1 channels
  - Watchdog timer : 1 channel
- Serial interface :
  - CSI : 1 channel
  - UART : 2 channels
- A/D converter : 10-bit resolution : 4 channels + 4 channels (2ch A/D macro)
- Operation Voltage :
  - 4.5V to 5.5V: 20MHz max. (OSC=2.5MHz x8)
  - 3.5V to 5.5V: 20MHz max. (OSC=2.5MHz x8, without A/D converter)
- Package :
  - 64-pin LQFP (14 x 14mm, 0.8mm pitch)

Please note: The information in this document is subject to change without notice

Document No. U18131EE1V0PM00 (1st edition)

V850ES/IE2 PPI (Ver. 1.0)
NEC Electronics Corporation November 2005

Function Table

Device name		V850ES/IE2	
		μPD 70F3713	μPD 70F3714
CPU core		V850ES	
CPU performance		26MIPS(@20MHz)	
Internal flash memory		64KB	128KB
Internal RAM		6KB	6KB
Interrupt sources	Internal	7	
	External	35	
Timer/counter		16-bit timer(TMP) x 4 ch 16-bit timer(TMQ) x 2 ch 16-bit timer(TMM) x 1 ch Watchdog timer x 1 ch	
Serial interface		CSI x 1 ch UART x 2 ch	
A/D converter		10-bit x 4ch, 10-bit x 4ch	
Ports	I/O	39	
Operating frequency		20MHz (Resonator clock 2.5MHz)	
Power supply voltage		4.5 to 5.5V(@20MHz) 3.5 to 5.5V(@20MHz, without A/D converter)	
Package		64-pin LQFP (14x14mm)	
Operating ambient temperature		-40°C to +85°C	

Timer & Serial interface functions overview

Function	Overview
CSI	➢ Transfer rate: 5Mbps to 156.25kbps (fxx=20MHz, using internal clock) ➢ Master mode and slave mode selectable ➢ 8-bit to 16-bit transfer, 3-wire serial interface ➢ interrupt request signals (INTCB0T, INTCB0R, INTCB0RE) ➢ Serial clock and data phase switchable ➢ Transfer data length selectable in 1-bit units between 8 and 16 bits ➢ Transfer data MSB-first/LSB-first swichable ➢ 3-wire transfer SOB0 : Serial data output SIB0 : Serial data input SCKB0 : Serial clock input/output Transmission mode, reception mode, and transmission/reception mode specifiable
UART	➢ Transfer rate : 1.25Mbps to 300bps (using internal system clock of 20MHz and dedicated baud rate generator) ➢ Full-duplex commucication: Internal UARTAn receive data register(UAnRX) Internal UARTAn transmit data register(UAnTX) ➢ 2-pin configuration: TXDAn: Transmit data output pin RXDAn: Receive data input pin ➢ Interrupt sources: 3 ✓ Reception complete interrupt(INTUAnR): This interrupt occurs upon transfer of receive data from the receive shift register to receive data register after serial transfer completion, in the reception enabled status. ✓ Transmission enable interrupt(INTUAnT): This interrupt occurs upon transfer of transmit data from the transmit data register to the transmit shift register in the transmission enabled status. ✓ Reception error interrupt(INTUAnRE) Parity error Framing error Overrun error ➢ Character length: 7, 8 bits ➢ Parity function: Odd, even, 0, none ➢ Transmission stop bit: 1, 2 bits ➢ On-chip dedicated baud rate generator ➢ MSB-/LSB-first transfer selectable ➢ Transmit/receive data inverted input/output possible **Remark** n = 0 to 1
16-bit timer/event counter (TMP0)	➢ Clock selection: 8 ways ➢ Capture trigger input pins: 2 ➢ External event count input pins: 1 ➢ External trigger input pins: 1 ➢ Timer/counters: 1 ➢ Capture/compare registers: 2 ➢ Capture/compare match interrupt request signals: 2 ➢ Timer output pins: 2 ➢ TMP0 has the following functions. ✓ Interval timer ✓ External event counter ✓ External trigger pulse output ✓ One-shot pulse output ✓ PWM output ✓ Free-running timer ✓ Pulse width Pulse width measurement

Timer & Serial interface functions overview

Function	Overview
16-bit timer counter (TMP1)	➢ Clock selection: 8 ways ➢ Capture trigger input pins: non ➢ External event count input pins: non ➢ External trigger input pins: non ➢ Timer/counters: 1 ➢ Compare registers: 2 ➢ Compare match interrupt request signals: 2 ➢ Timer output pins: non ➢ TMP1 has the following functions. ✓ Interval timer ✓ Free-running timer ✓ Timer tuning operation function (tunable with TMQ1)
16-bit timer/event counter (TMP2)	➢ Clock selection: 8 ways ➢ Capture trigger input pins: 2 ➢ External event count input pins: 1 ➢ External trigger input pins: 1 ➢ Timer/counters: 1 ➢ Capture/compare registers: 2 ➢ Capture/compare match interrupt request signals: 2 ➢ Timer output pins: 1 ➢ TMP0 has the following functions. ✓ Interval timer ✓ External event counter ✓ External trigger pulse output ✓ One-shot pulse output ✓ PWM output ✓ Free-running timer ✓ Pulse width Pulse width measurement
16-bit timer counter (TMP3)	➢ Clock selection: 8 ways ➢ Capture trigger input pins: non ➢ External event count input pins: non ➢ External trigger input pins: non ➢ Timer/counters: 1 ➢ Compare registers: 2 ➢ Compare match interrupt request signals: 2 ➢ Timer output pins: 1 ➢ TMP0 has the following functions. ✓ Interval timer ✓ External event counter ✓ External trigger pulse output with software ✓ One-shot pulse output with software ✓ PWM output ✓ Free-running timer

Timer & Serial interface functions overview

16-bit timer/event counter (TMQ0)	➢ Clock selection: 8 ways ➢ Capture/trigger input pins: 4 ➢ External event count input pins: 1 ➢ External trigger input pins: non ➢ Timer/counters: 1 ➢ Capture/compare registers: 4 ➢ Capture/compare match interrupt request signals: 4 ➢ Timer output pins: 4 ➢ TMQ0 has the following functions. ✓ Interval timer ✓ External event counter ✓ External trigger pulse output ✓ One-shot pulse output ✓ PWM output ✓ Free-running timer ✓ Pulse width measurement
16-bit timer counter (TMQ1)	➢ Clock selection: 8 ways ➢ Capture/trigger input pins: non ➢ External event count input pins: non ➢ External trigger input pins: non ➢ Timer/counters: 1 ➢ Compare registers: 4 ➢ Compare match interrupt request signals: 4 ➢ Timer output pins: 1 ➢ TMQ1 has the following functions. ✓ 6phase PWM output (with TMQOP1) ✓ Interval timer ✓ Free-running timer
16-bit interval timer (TMM)	➢ Interval function ➢ 8 clocks selectable ➢ 16-bit counter x 1 (The 16-bit counter cannot be read during timer count operation.) ➢ Compare register x 1 (The compare register cannot be written during timer counter operation.) ➢ Compare match interrupt x 1
Watchdog timer (WDT)	➢ Default-stop watchdog timer ✓ Reset mode: Reset operation upon overflow of watchdog timer (generation of WDTRES signal) ✓ Non-maskable interrupt request mode: NMI operation upon overflow of watchdog timer (generation of INTWDT signal)
Inverter control function (TMQOP1 :TMQ option)	➢ The TMQ1 and the TMQOP1 can be used as an inverter control function. ✓ 6-phase PWM output function with 16-bit accuracy (with dead-timer, for upper and lower arms) ✓ Timer tuning operation function (tunable with TMP1) ✓ Cycle setting function (cycle can be changed during operation of crest or valley interrupt) ✓ Compare register rewriting: Anytime rewrite, batch rewrite, or intermittent rewrite (selectable during TMQ1 operation) ✓ Interrupt and transfer culling functions ✓ A/D trigger timing function of A/D converters 0 and 1 ✓ 0% output and 100% output available ✓ Forced output stop function ✓ At valid edge detection by external pin input ✓ At main clock oscillation stop detection by clock monitor function

Other functions overview

Function	Overview
A/D converter	➢ Two 10-bit resolution A/D converter circuits (A/D converters 0 and 1) ✓ Simultaneous sampling of two circuits possible ✓ A/D converter 0: ANI00 to ANI03 (4 channels) ✓ A/D converter 1: ANI10 to ANI13 (4 channels) ✓ A/D conversion result registers 0m and 1m (ADA0CRm and ADA1CRm) ➢ A/D conversion trigger mode ✓ Software trigger mode ✓ Hardware trigger mode External trigger mode Timer trigger mode ➢ Operating voltage range ✓ VDD = EVDD = AVDDn = AVREFn = 4.5 to 5.5 V **Remark** m = 0 to 3, n = 0, 1
Interrupt/exception processing	➢ Interrupts ✓ Non-maskable interrupts: 1 sources (Internal) ✓ Maskable interrupts: External: 7, Internal: 35 sources ✓ 8 levels of programmable priorities (maskable interrupts) ✓ Multiple interrupt control according to priority ✓ Masks can be specified for each maskable interrupt request. ➢ Exceptions ✓ Software exceptions: 32 sources ➢ Exception trap: 2 sources (illegal op code exception and debug trap)
Standby modes	➢ The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application. ✓ HALT mode: Mode to stop only the operating clock of the CPU ✓ IDLE mode: Mode to stop all the operations of the internal circuits except the oscillator and PLL. ✓ STOP mode: Mode to stop all the operations of the internal circuits except the oscillator.
Clock monitor	➢ The clock monitor samples the main clock by using the internal oscillation clock and generates a reset request signal and turn to the 6-phase PWM output ports and TOP21 when oscillation of the main clock is stopped.
Low-voltage Detector (LVI)	➢ Compares the supply voltage (VDD) and detected voltage (VLVI) and generates an internal interrupt signal or internal reset signal when VDD < VLVI. ➢ The level of the supply voltage to be detected can be changed by software (in two steps). ➢ Interrupt or reset signal can be selected by software. ➢ Can operate in STOP mode.

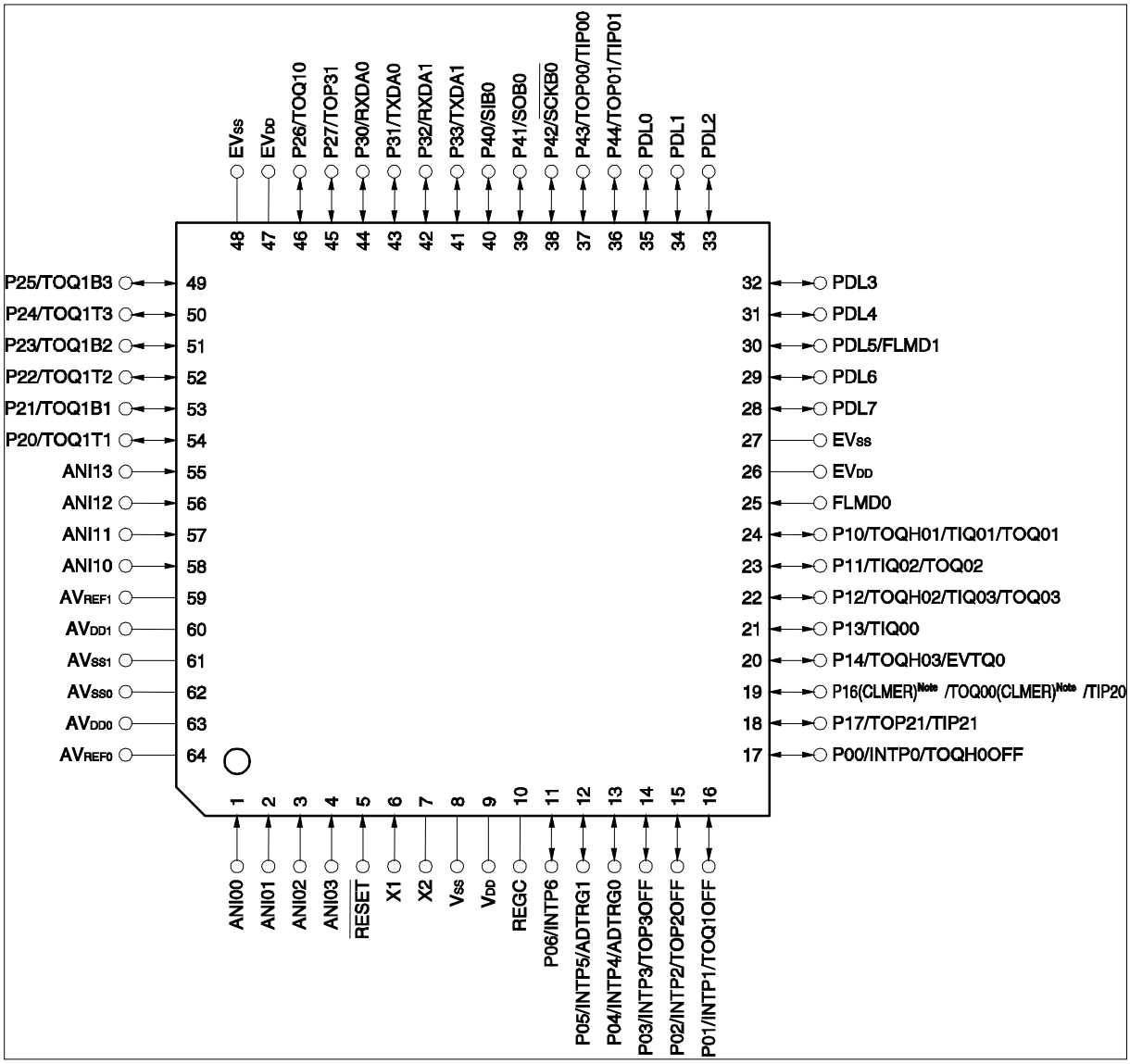
Pin configuration (TOP VIEW)

64-pin plastic LQFP (14 x 14 mm, 0.8mm pitch)

μPD70F3713GC-8BS-A

μPD70F3714GC-8BS-A

Top View



Notes The CLMER signal is enabled only when P16 is specified as an output port or the output function of TOQ00. When an error (oscillator stop) is detected by the clock monitor, a low level is forcibly output. Low-level output is released by reset signal.

List of Pin Functions

(1) Port pins

Pin Name	Pin No.	I/O	Function	Alternate Function
P00	17	I/O	Port 0 7-bit I/O port Input data read/output data write is enabled in 1-bit units. Use of an on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected only in the input mode of the port mode and when the alternate function of the pin is used).	INTP0/TOQH0OFF
P01	16			INTP1/TOQ1OFF
P02	15			INTP2/TOP2OFF
P03	14			INTP3/TOP3OFF
P04	13			INTP4/ADTRG0
P05	12			INTP5/ADTRG1
P06	11			INTP6
P10	24	I/O	Port 1 7-bit I/O port Input data read/output data write is enabled in 1-bit units. Use of an on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected only in the input mode of the port mode, when the input mode of alternate function of the pin is used, and when TOP21 and TOQH01 to TOQH03 pins, which function as output pins when their alternate function is used, go into a high-impedance state).	TOQH01/TIQ01/TOQ01
P11	23			TIQ02/TOQ02
P12	22			TOQH02/TIQ03/TOQ03
P13	21			TIQ00
P14	20			TOQH03/EVTQ0
P16 (CLMER)[Note]	19			TOQ00 (CLMER)[Note]/TIP20
P17	18			TOP21/TIP21
P20	54	I/O	Port 2 8-bit I/O port Input data read/output data write is enabled in 1-bit units. Use of an on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected only in the input mode of the port mode, or when TOQ1T1 to TOQ1T3 and TOQ1B1 to TOQ1B3 and TOP31 pins, which function as output pins when their alternate function is used, go into a high-impedance state).	TOQ1T1
P21	53			TOQ1B1
P22	52			TOQ1T2
P23	51			TOQ1B2
P24	50			TOQ1T3
P25	49			TOQ1B3
P26	46			TOQ10
P27	45			TOP31
P30	44	I/O	Port 3 4-bit I/O port Input data read/output data write is enabled in 1-bit units. Use of an on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected only in the input mode of the port mode and when the input mode of the alternate function of the pin is used).	RXDA0
P31	43			TXDA0
P32	42			RXDA1
P33	41			TXDA1
PDL0	35	I/O	Port DL 8-bit I/O port Input data read/output data write is enabled in 1-bit units. An on-chip pull-up resistor can be specified in 1-bit units (the on-chip pull-up resistor can be connected when the pins are in the port mode and input mode).	–
PDL1	34			–
PDL2	33			–
PDL3	32			–
PDL4	31			–
PDL5	30			FLMD1
PDL6	29			–
PDL7	28			–

Note The CLMER signal is enabled only when P16 is specified as an output port or the output function of TOQ00. When an error (oscillator stop) is detected by the clock monitor, a low level is forcibly output. Low-level output is released by reset signal.

(2) Non-port pins

Pin Name	Pin No.	I/O	Function	Alternate Function
ADTRG0	13	Input	External trigger input for A/D converters 0, 1	INTP4/P04
ADTRG1	12	Input		INTP5/P05
ANI00	1	Input	Analog input to A/D converters 0, 1	–
ANI01	2	Input		–
ANI02	3	Input		–
ANI03	4	Input		–
ANI10	58	Input		–
ANI11	57	Input		–
ANI12	56	Input		–
ANI13	55	Input		–
AV_{DD0}	63	–	Positive power supply for A/D converters 0, 1 (same potential as V_{DD})	–
AV_{DD1}	60	–		–
AV_{REF0}	64	–	Reference voltage input for A/D converters 0, 1 (same potential as AV_{DD0} and AV_{DD1})	–
AV_{REF1}	59	–		–
AV_{SS0}	62	–	Ground potential for A/D converters 0, 1 (same potential as V_{SS})	–
AV_{SS1}	61	–		–
EV_{DD}	26, 47	–	Positive power supply for external pin	–
EV_{SS}	27, 48	–	Ground potential for external pin	–
EVTQ0	20	Input	External event count input of TMQ0	TOQH03/P14
FLMD0	25	Input	Pin for setting flash memory programming mode	–
FLMD1	30	Input		PDL5
INTP0	17	Input	External maskable interrupt request input	TOQH0OFF/P00
INTP1	16			TOQ1OFF/P01
INTP2	15			TOP2OFF/P02
INTP3	14			TOP3OFF/P03
INTP4	13			ADTRG0/P04
INTP5	12			ADTRG1/P05
INTP6	11			P06
REGC	10	–	Regulator output stabilization capacitance connection	–
$\overline{\text{RESET}}$	5	Input	System reset input	–
RXDA0	44	Input	Serial receive data input of UARTA0, UARTA1	P30
RXDA1	42			P32
$\overline{\text{SCKB0}}$	38	I/O	Serial clock I/O of CSIB0	P42
SIB0	40	Input	Serial receive data input of CSIB0	P40
SOB0	39	Output	Serial transmit data output of CSIB0	P41

Pin Name	Pin No.	I/O	Function	Alternate Function
TIP00	37	Input	External timer trigger input of TMP0, TMP2	TOP00/P43
TIP01	36			TOP01/P44
TIP20	19			TOQ00 (CLMER)[Note]/ P16 (CLMER)[Note]
TIP21	18			TOP21/P17
TIQ00	21	Input	External timer trigger input of TMQ0	P13
TIQ01	24			TOQH01/TOQ01/P10
TIQ02	23			TOQ02/P11
TIQ03	22			TOQH02/TOQ03/P12
TOP00	37	Output	Pulse signal output of TMP0, TMP2	TIP00/P43
TOP01	36			TIP01/P44
TOP21	18			TIP21/P17
TOP2OFF	15	Input	High-impedance output control signal input	INTP2/P02
TOP31	45	Output	Pulse signal output of TMP3	P27
TOP3OFF	14	Input	High-impedance output control signal input	INTP3/P03
TOQ00 (CLMER)[Note]	19	Output	Pulse signal output of TMQ0	TIP20/P16 (CLMER)[Note]
TOQ01	24			TOQH01/TIQ01/P10
TOQ02	23			TIQ02/P11
TOQ03	22			TOQH02/TIQ03/P12
TOQ10	46	Output	Pulse signal output of TMQ1	P26
TOQ1B1	53	Output	Pulse signal output for 6-phase PWM	P21
TOQ1B2	51			P23
TOQ1B3	49			P25
TOQ1OFF	16	Input	High-impedance output control signal input	INTP1/P01
TOQ1T1	54	Output	Pulse signal output for 6-phase PWM	P20
TOQ1T2	52			P22
TOQ1T3	50			P24
TOQH01	24	Output	High-impedance output by TMQ0 pulse signal output and valid edge of TOQH0OFF pin input	TIQ01/TOQ01/P10
TOQH02	22			TIQ03/TOQ03/P12
TOQH03	20			EVTQ0/P14
TOQH0OFF	17	Input	High-impedance output control signal input	INTP0/P00
TXDA0	43	Output	Serial transmit data output of UARTA0, UARTA1	P31
TXDA1	41			P33
V_{DD}	9	–	Positive power supply for internal unit	–
V_{SS}	8	–	Ground potential for internal unit	–
X1	6	Input	Crystal connection pin for system clock oscillation	–
X2	7	–		–

Note The CLMER signal is enabled only when P16 is specified as an output port or the output function of TOQ00. When an error (oscillator stop) is detected by the clock monitor, a low level is forcibly output. Low-level output is released by reset signal.