

## Brief Description

The ZSPM4523 is a DC/DC synchronous switching super capacitor charger with fully integrated power switches, internal compensation, and full fault protection. It uses a temperature-independent photo-voltaic maximum power point tracking (MPPT) calculator to optimize power output from the source during Full-Charge Mode. Its 1MHz switching frequency allows using small filter components, which results in smaller board space and reduced bill-of-material costs.

In Full-Charge Mode, the duty cycle is controlled by the MPPT function. Once the termination voltage is reached, the regulator operates in Constant Voltage Mode. When the regulator is disabled (the EN pin is low), the device draws 10 $\mu$ A (typical) quiescent current from V<sub>OUT</sub>.

The ZSPM4523 integrates a wide range of protection circuitry, including input supply under-voltage lockout, output over-voltage protection, current limiting, and thermal shutdown.

The ZSPM4523 includes supervisory reporting via the NFLT (Inverted Fault) open-drain output to interface other components in the system. Device programming is achieved by the I<sup>2</sup>C™\* interface through the SCL and SDA pins.

## Benefits

- Up to 1.5A continuous output current
- High efficiency – up to 92% at typical load

## Features

- Temperature-independent MPPT regulation
- V<sub>OUT</sub> reverse-current blocking
- Programmable temperature-compensated termination voltage: 2.48 to 2.74 V  $\pm$  1%
- User programmable maximum charge current: 50mA to 1500mA
- Input supply under-voltage lockout
- Full protection for V<sub>OUT</sub> over-voltage
- I<sup>2</sup>C™ program interface with EEPROM registers
- Charge status indication

## Related IDT Smart Power Products

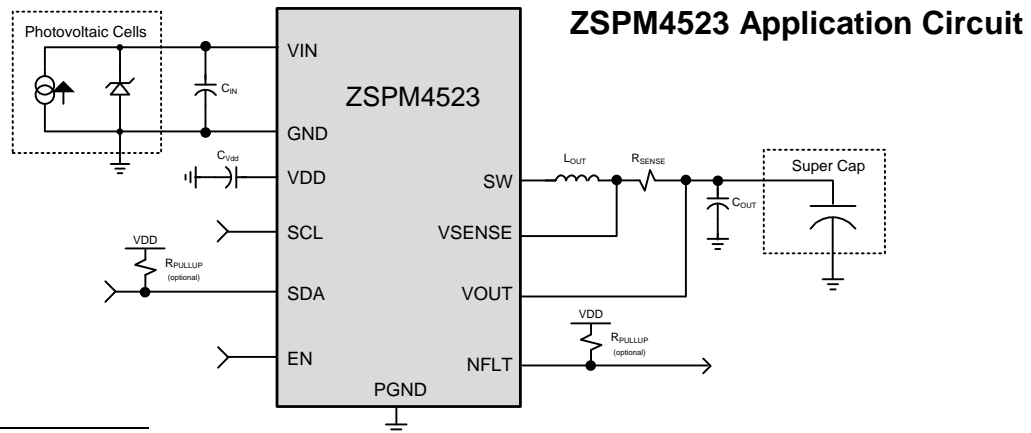
- ZSPM4521 High-Efficiency Charger for Li-Ion Batteries with MPPT Regulator
- ZSPM4551 High-Efficiency Charger for Li-Ion Batteries
- ZSPM4121 Ultra-low Power Under-Voltage Switch
- ZSPM4141 Ultra-Low-Power Linear Regulator

## Available Support

- Evaluation Kit
- Support Documentation

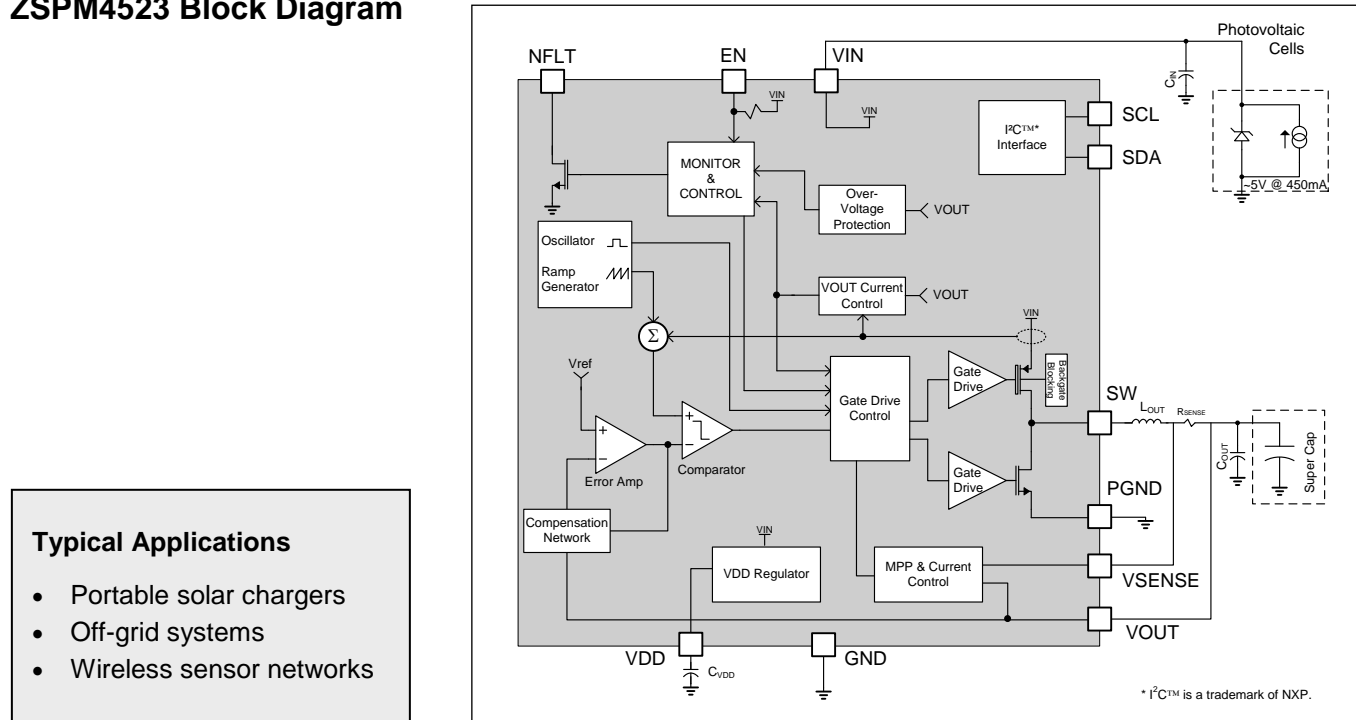
## Physical Characteristics

- Wide input voltage range: 3.2V to 7.2V
- Junction operating temperature -40°C to 125°C
- Packaged in a 16-pin PQFN (4mm x 4mm)



\* I<sup>2</sup>C™ is a trademark of NXP.

## ZSPM4523 Block Diagram



## Ordering Information

| Ordering Code | Description  | Package                             |
|---------------|--|-------------------------------------|
| ZSPM4523AA1W  | ZSPM4523 High-Efficiency Regulator for Super Cap Systems | 16-pin PQFN / 7" Reel (1000 parts)  |
| ZSPM4523AA1R  | ZSPM4523 High-Efficiency Regulator for Super Cap Systems | 16-pin PQFN / 13" Reel (3300 parts) |
| ZSPM4523KIT   | ZSPM4523 Evaluation Kit                                  |                                     |

## Contents

|        |   |    |
|--------|---|----|
| 1      | ZSPM4523 Characteristics.....   | 5  |
| 1.1.   | Absolute Maximum Ratings.....   | 5  |
| 1.2.   | Thermal Characteristics.....  | 5  |
| 1.3.   | Recommended Operating Conditions .....  | 6  |
| 1.4.   | Electrical Characteristics .....  | 6  |
| 1.5.   | I <sup>2</sup> C™ Interface Timing Requirements.....                              | 9  |
| 2      | Functional Description.....   | 10 |
| 2.1.   | Internal Protection Features .....  | 11 |
| 2.1.1. | VIN Under-Voltage Lockout .....   | 11 |
| 2.1.2. | Internal Current Limit .....  | 11 |
| 2.1.3. | Thermal Shutdown.....   | 11 |
| 2.1.4. | VOOUT Over-Voltage Protection.....  | 11 |
| 3      | Serial Interface .....  | 12 |
| 3.1.   | I <sup>2</sup> C™ Subaddress Definition.....                                      | 12 |
| 3.2.   | I <sup>2</sup> C™ Bus Operation .....   | 12 |
| 3.3.   | Status and Configuration Registers.....   | 14 |
| 4      | Application Circuits.....   | 17 |
| 4.1.   | Typical Application Circuits.....   | 17 |
| 4.2.   | Selection of External Components .....  | 17 |
| 4.2.1. | C <sub>OUT</sub> Output Capacitor .....   | 17 |
| 4.2.2. | L <sub>OUT</sub> Output Inductor .....  | 17 |
| 4.2.3. | C <sub>IN</sub> Bypass Capacitor for Input from Photovoltaic Source .....         | 17 |
| 4.2.4. | C <sub>VDD</sub> Bypass Capacitor for VDD Internal Reference Voltage Output ..... | 17 |
| 4.2.5. | R <sub>SENSE</sub> Output Sensing Resistor .....                                  | 18 |
| 4.2.6. | Pull-up Resistors .....   | 18 |
| 5      | Pin Configuration and Package.....  | 18 |
| 5.1.   | ZSPM4523 Package Dimensions.....  | 18 |
| 5.2.   | Pin Assignments.....  | 19 |
| 5.3.   | Pin Description.....  | 19 |
| 5.4.   | Package Markings .....  | 20 |
| 6      | Layout Recommendations.....   | 21 |
| 6.1.   | Multi-Layer PCB Layout.....   | 21 |
| 6.2.   | Single-Layer PCB Layout .....   | 22 |
| 7      | Ordering Information .....  | 23 |
| 8      | Related Documents.....  | 23 |
| 9      | Document Revision History.....  | 24 |

## List of Figures

|            |  |    |
|------------|--|----|
| Figure 2.1 | ZSPM4523 Block Diagram .....   | 10 |
| Figure 3.1 | Subaddress in I <sup>2</sup> C™ Transmission .....                   | 12 |
| Figure 3.2 | I <sup>2</sup> C™ STOP/START Protocol .....                          | 13 |
| Figure 3.3 | I <sup>2</sup> C™ Data Transmission Timing .....                     | 13 |
| Figure 4.1 | Application Circuit .....  | 17 |
| Figure 5.1 | PQFN-16 Package Dimensions .....                                     | 18 |
| Figure 5.2 | ZSPM4523 Pin Assignments for 16-Pin 4mm x4mm PQFN .....              | 19 |
| Figure 6.1 | Package and PCB Land Configuration for Multi-Layer PCB .....         | 21 |
| Figure 6.2 | JEDEC Standard FR4 Multi-Layer Board – Cross-Sectional View .....    | 21 |
| Figure 6.3 | Conducting Heat Away from the Die using an Exposed Pad Package ..... | 22 |
| Figure 6.4 | Application Using a Single-Layer PCB .....                           | 23 |

## List of Tables

|           |   |    |
|-----------|---|----|
| Table 1.1 | Absolute Maximum Ratings .....  | 5  |
| Table 1.2 | Thermal Characteristics .....   | 5  |
| Table 1.3 | Recommended Operating Conditions .....                                      | 6  |
| Table 1.4 | Electrical Characteristics .....  | 6  |
| Table 1.5 | I <sup>2</sup> C™ Interface Timing Characteristics .....                    | 9  |
| Table 3.1 | Register Description (Device Address = 48 <sub>HEX</sub> ) .....            | 14 |
| Table 3.2 | STATUS Register—Address 00 <sub>HEX</sub> .....                             | 14 |
| Table 3.3 | Configuration Register CONFIG1—Address 02 <sub>HEX</sub> .....              | 15 |
| Table 3.4 | Configuration Register CONFIG3—Address 04 <sub>HEX</sub> .....              | 15 |
| Table 3.5 | Enable Configuration Register CONFIG_ENABLE—Address 11 <sub>HEX</sub> ..... | 16 |
| Table 3.6 | EEPROM Control Register EEPROM_CTRL—Address 12 <sub>HEX</sub> .....         | 16 |
| Table 5.1 | ZSPM4523 Pin Description .....  | 19 |

# 1 ZSPM4523 Characteristics

Important: Stresses beyond those listed under “Absolute Maximum Ratings” (section 1.1) might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Thermal Characteristics” (section 1.2) and “Recommended Operating Conditions” (section 1.3) is not implied. Exposure to absolute–maximum–rated conditions for extended periods might affect device reliability.

## 1.1. Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted.

**Table 1.1 Absolute Maximum Ratings**

| Parameter  | Value <sup>1)</sup> | Unit |
|--|---------------------|------|
| VIN, EN, NFLT, SCL, SDA, VOUT, VSENSE  | -0.3 to 8           | V    |
| SW   | -1 to 8.8           | V    |
| VDD  | -0.3 to 3.6         | V    |
| Operating Junction Temperature Range, T <sub>J</sub>   | -40 to 125          | °C   |
| Storage Temperature Range, T <sub>STOR</sub>   | -65 to 150          | °C   |
| Electrostatic Discharge – Human Body Model <sup>2)</sup>   | +/-2k               | V    |
| Electrostatic Discharge – Machine Model <sup>2)</sup>  | +/-200              | V    |
| Lead Temperature (soldering, 10 seconds)   | 260                 | °C   |
| <sup>1)</sup> All voltage values are with respect to network ground terminal.<br><sup>2)</sup> ESD testing is performed according to the respective JESD22 JEDEC standard. |                     |      |

## 1.2. Thermal Characteristics

**Table 1.2 Thermal Characteristics**

| Parameter  | Symbol        | Value | Unit |
|--|---------------|-------|------|
| Thermal Resistance Junction to Air <sup>1)</sup>   | $\theta_{JA}$ | 50    | °C/W |
| <sup>1)</sup> Assumes 4x4mm QFN-16 in 1 in <sup>2</sup> area of 2 oz. copper and 25°C ambient temperature. |               |       |      |

### 1.3. Recommended Operating Conditions

**Table 1.3 Recommended Operating Conditions**

| Parameter  | Symbol        | Min | Typ | Max | Unit |
|--|---------------|-----|-----|-----|------|
| Photovoltaic Input Operating Voltage   | $V_{IN}$      | 3.2 | 5.3 | 7.2 | V    |
| Sense Resistor   | $R_{SENSE}$   |     | 50  |     | mΩ   |
| Output Filter Inductor Typical Value <sup>1)</sup>   | $L_{OUT}$     |     | 4.7 |     | μH   |
| Output Filter Capacitor Typical Value <sup>2)</sup>  | $C_{OUT}$     |     | 4.7 |     | μF   |
| Output Filter Capacitor ESR  | $C_{OUT-ESR}$ |     |     | 100 | mΩ   |
| Input Supply Bypass Capacitor Typical Value <sup>3)</sup>  | $C_{IN}$      | 3.3 | 10  |     | μF   |
| VDD Supply Bypass Capacitor Value <sup>2)</sup>  | $C_{VDD}$     | 70  | 100 | 130 | nF   |
| Operating Free Air Temperature   | $T_A$         | -40 |     | 85  | °C   |
| Operating Junction Temperature   | $T_J$         | -40 |     | 125 | °C   |
| 1) For best performance, use an inductor with a saturation current rating higher than the maximum $V_{OUT}$ load requirement plus the inductor current ripple.<br>2) For best performance, use a low ESR ceramic capacitor.<br>3) For best performance, use a low ESR ceramic capacitor. If $C_{IN}$ is not a low ESR ceramic capacitor, add a 0.1μF ceramic capacitor in parallel to $C_{IN}$ . |               |     |     |     |      |

### 1.4. Electrical Characteristics

Electrical Characteristics,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = 5.3\text{V}$  (unless otherwise noted).

**Table 1.4 Electrical Characteristics**

| Parameter                          | Symbol           | Condition   | Min | Typ | Max | Unit |
|------------------------------------|------------------|---|-----|-----|-----|------|
| <b>VIN Supply Voltage</b>          |                  |   |     |     |     |      |
| Photovoltaic Voltage Input         | $V_{IN}$         |   | 3.2 | 5.3 | 7.2 | V    |
| Quiescent Current<br>Normal Mode   | $I_{CC-NORM}$    | $I_{LOAD} = 0\text{A}$ , $EN \geq 2.2\text{V}$ (HIGH) |     | 3   |     | mA   |
| Quiescent Current<br>Disabled Mode | $I_{CC-DISABLE}$ | $EN = 0\text{V}$                                      |     | 10  | 50  | μA   |
| <b>VOUT Leakage</b>                |                  |   |     |     |     |      |
| Leakage Current From<br>Output     | $I_{OUT-LEAK}$   | $EN = 0\text{V}$ , $V_{OUT} = 2.7\text{V}$            |     |     | 10  | μA   |
| Reverse Current                    | $I_{OUT-BACK}$   | $V_{OUT} > V_{IN}$ , $V_{OUT} = 2.7\text{V}$          |     |     | 10  | μA   |

| Parameter                                       | Symbol            | Condition           | Min | Typ  | Max | Unit        |
|---|-------------------|---------------------|-----|------|-----|-------------|
| <b>VIN Under-Voltage Lockout</b>                |                   |                     |     |      |     |             |
| Input Supply Under Voltage Threshold            | $V_{IN-UV}$       | $V_{IN}$ increasing |     | 3.15 |     | V           |
| Input Supply Under Voltage Threshold Hysteresis | $V_{IN-UV\_HYST}$ |                     | 100 | 200  |     | mV          |
| <b>OSC</b>                                      |                   |                     |     |      |     |             |
| Oscillator Frequency                            | $f_{OSC}$         |                     | 0.9 | 1    | 1.1 | MHz         |
| <b>NFLT Open Drain Output</b>                   |                   |                     |     |      |     |             |
| High-Level Output Leakage                       | $I_{OH-NFLT}$     | $V_{NFLT} = 5.3V$   |     | 0.1  |     | $\mu A$     |
| Low-Level Output Voltage                        | $V_{OL-NFLT}$     | $I_{NFLT} = -1mA$   |     |      | 0.4 | V           |
| <b>EN/SCL/SDA Input Voltage Thresholds</b>      |                   |                     |     |      |     |             |
| High Level Input Voltage                        | $V_{IH}$          |                     | 2.2 |      |     | V           |
| Low Level Input Voltage                         | $V_{IL}$          |                     |     |      | 0.8 | V           |
| Input Hysteresis – EN, SCL, SCA Pins            | $V_{HYST}$        |                     |     | 200  |     | mV          |
| Input Leakage – EN Pin                          | $I_{IN-EN}$       | $V_{EN}=VIN$        |     | 0.1  |     | $\mu A$     |
|   |                   | $V_{EN}=0V$         |     | -2.0 |     | $\mu A$     |
| Input Leakage – SCL Pin                         | $I_{IN-SCL}$      | $V_{SCL}=VIN$       |     | 55   |     | $\mu A$     |
|   |                   | $V_{SCL}=0V$        |     | -0.1 |     | $\mu A$     |
| Input Leakage – SDA Pin                         | $I_{IN-SDA}$      | $V_{SDA}=VIN$       |     | 0.1  |     | $\mu A$     |
|   |                   | $V_{SDA}=0V$        |     | -0.1 |     | $\mu A$     |
| Low-Level Output Voltage                        | $V_{OL-SDA}$      | $I_{SDA} = -1mA$    |     |      | 0.4 | V           |
| <b>Thermal Shutdown</b>                         |                   |                     |     |      |     |             |
| Thermal Shutdown Junction Temperature           | $T_{SD}$          |                     | 150 | 170  |     | $^{\circ}C$ |
| TSD Hysteresis                                  | $T_{SD-HYST}$     |                     |     | 10   |     | $^{\circ}C$ |

| Parameter  | Symbol           | Condition                                      | Min             | Typ            | Max             | Unit       |
|--|------------------|--|-----------------|----------------|-----------------|------------|
| <b>Charging Regulator with <math>L_{OUT}=4.7\mu H</math> and <math>C_{OUT}=4.7\mu F</math></b> |                  |  |                 |                |                 |            |
| Output Current Limit in Full Charge Mode   | $I_{OUT-FC}$     | $I_{OUT}$ is user programmable; see Table 3.4. | $I_{OUT} - 5\%$ | $I_{OUT}$      | $I_{OUT} + 5\%$ | A          |
| Termination Voltage  | $V_{OUT}$        | $V_{OUT}$ is user-programmable; see Table 3.3. | $V_{OUT} - 1\%$ | $V_{OUT}$      | $V_{OUT} + 1\%$ | V          |
| Full Charge Timer  | $t_{FC}$         |  | 200             |                | 1400            | min        |
| High-Side (HS) Switch On Resistance  | $R_{DSON}$       | $I_{SW} = -1A, T_J=25^\circ C$                 |                 | 250            |                 | m $\Omega$ |
| Low-Side (LS) Switch On Resistance   |                  | $I_{SW} = 1A, T_J=25^\circ C$                  |                 | 150            |                 | m $\Omega$ |
| Output Current   | $I_{OUT}$        |  |                 |                | 1.5             | A          |
| Over-Current Detect  | $I_{OCD}$        | HS switch current                              |                 | 2.5            |                 | A          |
| $V_{OUT}$ Over-Voltage Threshold   | $V_{OUT-OV}$     |  | 101% $V_{OUT}$  | 102% $V_{OUT}$ | 103% $V_{OUT}$  |            |
| $V_{OUT}$ Over-Voltage Hysteresis  | $V_{OUT-OV-HYS}$ |  | 0.2% $V_{OUT}$  | 0.4% $V_{OUT}$ | 0.6% $V_{OUT}$  |            |
| Maximum Duty Cycle   | $DUTY_{MAX}$     |  |                 | 98             |                 | %          |



## 1.5. I<sup>2</sup>C™ Interface Timing Requirements

Electrical characteristics  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = 5.3\text{V}$ . See Figure 3.3 for an illustration of the timing specifications given in Table 1.5.

**Table 1.5 I<sup>2</sup>C™ Interface Timing Characteristics**

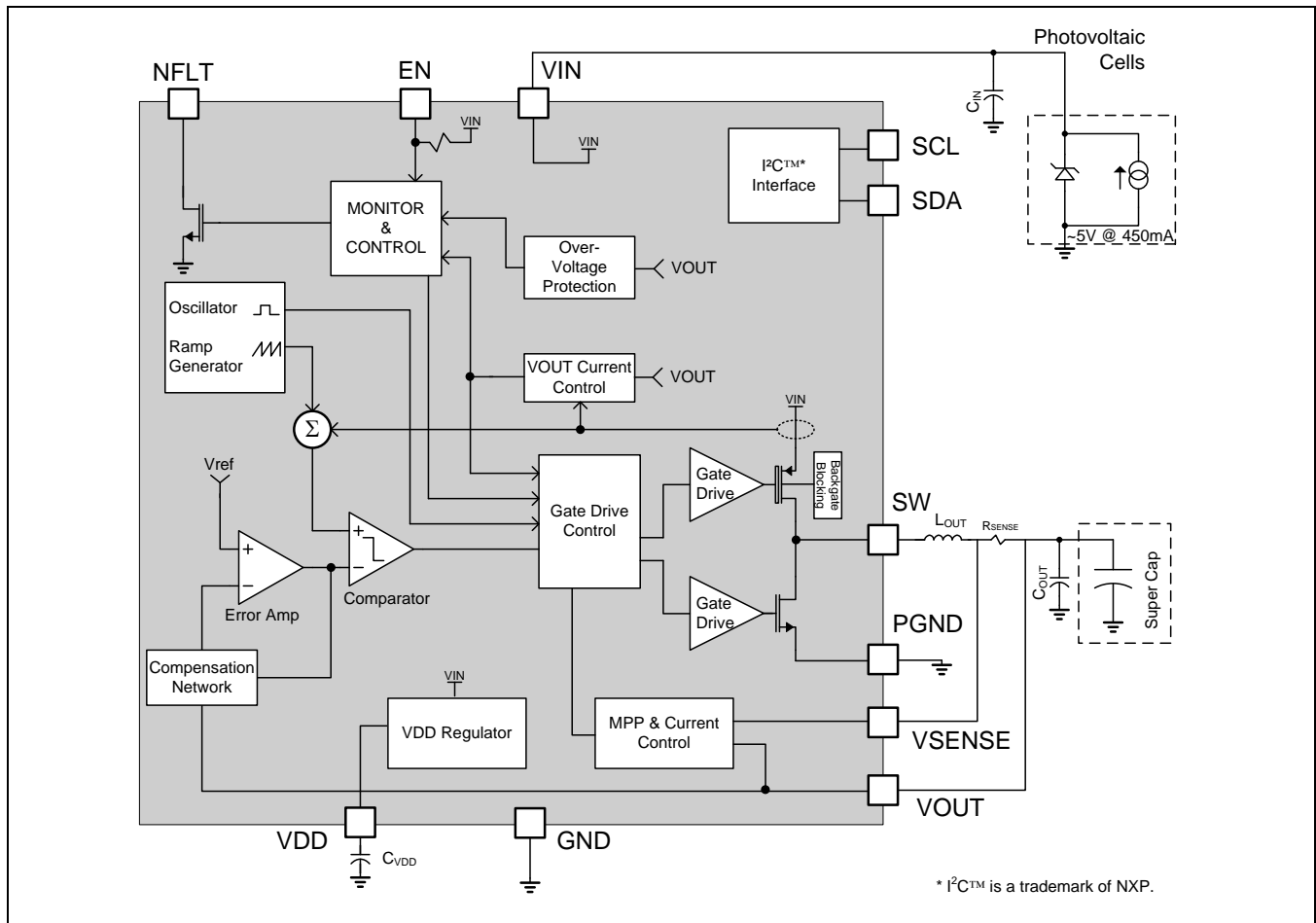
| Parameter  | Symbol    | Standard Mode |      | Fast Mode <sup>1)</sup> |     | Unit          |
|--|-----------|---------------|------|-------------------------|-----|---------------|
|  |           | Min           | Max  | Min                     | Max |               |
| I <sup>2</sup> C™ Clock Frequency  | $f_{scl}$ | 0             | 100  | 0                       | 400 | kHz           |
| I <sup>2</sup> C™ Clock High Time  | $t_{sch}$ | 4             |      | 0.6                     |     | $\mu\text{s}$ |
| I <sup>2</sup> C™ Clock Low Time   | $t_{scl}$ | 4.7           |      | 1.3                     |     | $\mu\text{s}$ |
| I <sup>2</sup> C™ Tolerable Spike Time <sup>2)</sup>   | $t_{sp}$  | 0             | 50   | 0                       | 50  | ns            |
| I <sup>2</sup> C™ Serial Data Setup Time   | $t_{sds}$ | 250           |      | 100                     |     | ns            |
| I <sup>2</sup> C™ Serial Data Hold Time  | $t_{sdh}$ | 0             |      | 0                       |     | $\mu\text{s}$ |
| I <sup>2</sup> C™ Input Rise Time <sup>2)</sup>  | $t_{icr}$ |               | 1000 |                         | 300 | ns            |
| I <sup>2</sup> C™ Input Fall Time <sup>2)</sup>  | $t_{icf}$ |               | 300  |                         | 300 | ns            |
| I <sup>2</sup> C™ Output Fall Time; 10pF to 400pF Bus <sup>2)</sup>  | $t_{ocf}$ |               | 300  |                         | 300 | ns            |
| I <sup>2</sup> C™ Bus Free Time Between Stop and Start   | $t_{buf}$ | 4.7           |      | 1.3                     |     | $\mu\text{s}$ |
| I <sup>2</sup> C™ Start or Repeated Start Condition Setup Time   | $t_{sts}$ | 4.7           |      | 0.6                     |     | $\mu\text{s}$ |
| I <sup>2</sup> C™ Start or Repeated Start Condition Hold Time  | $t_{sth}$ | 4             |      | 0.6                     |     | $\mu\text{s}$ |
| I <sup>2</sup> C™ Stop Condition Setup Time <sup>2)</sup>  | $t_{sps}$ | 4             |      | 0.6                     |     | $\mu\text{s}$ |
| <sup>1)</sup> The I <sup>2</sup> C™ interface will operate in either standard or fast mode.<br><sup>2)</sup> Parameter not tested in production. |           |               |      |                         |     |               |

## 2 Functional Description

The ZSPM4523 is a fully-integrated super capacitor charger IC based on a highly-efficient switching topology. It includes a maximum power point tracking (MPPT) function to optimize its input voltage to extract the maximum possible power from a photovoltaic cell. It includes configurability for termination voltage and charge current. A 1MHz internal switching frequency facilitates low-cost LC filter combinations.

When enabled, the ZSPM4523 will provide the maximum power available from a photovoltaic cell (Full-Charge Mode) until the output voltage reaches its termination point. At that point, it will begin to regulate voltage (Constant Voltage Mode). It will do so until a fault is detected, it is disabled, or the output voltage drops below the termination point.

**Figure 2.1 ZSPM4523 Block Diagram**



## **2.1. Internal Protection Features**

### **2.1.1. VIN Under-Voltage Lockout**

The device is held in the off state until the EN pin voltage is HIGH ( $\geq 2.2\text{V}$ ) and VIN rises to 3.15V (typical). There is a 200mV (typical) hysteresis on this input, which requires the input to fall below 2.95V (typical) before the device will disable.

### **2.1.2. Internal Current Limit**

The current through the  $L_{\text{OUT}}$  inductor is sensed on a cycle-by-cycle basis, and if the current limit ( $I_{\text{OCD}}$ , see section 1.4) is reached, it will abbreviate the cycle. Current limit is always active when the regulator is enabled.

### **2.1.3. Thermal Shutdown**

If the junction temperature of the ZSPM4523 exceeds 170°C (typical), the SW output will tri-state to protect the device from damage. The NFLT and all other protection circuitry will stay active to inform the system of the failure mode. Once the device cools to 160°C (typical), the device will attempt to start up again. If the device reaches 170°C, the shutdown/restart sequence will repeat.

### **2.1.4. VOUT Over-Voltage Protection**

The ZSPM4523 has an output protection circuit designed to shut down the charging profile if the output voltage is greater than the termination voltage. The termination voltage can be selected by user programming, so the protection threshold is set to 2% above the termination voltage. Shutting down the charging profile puts the ZSPM4523 in a fault condition.

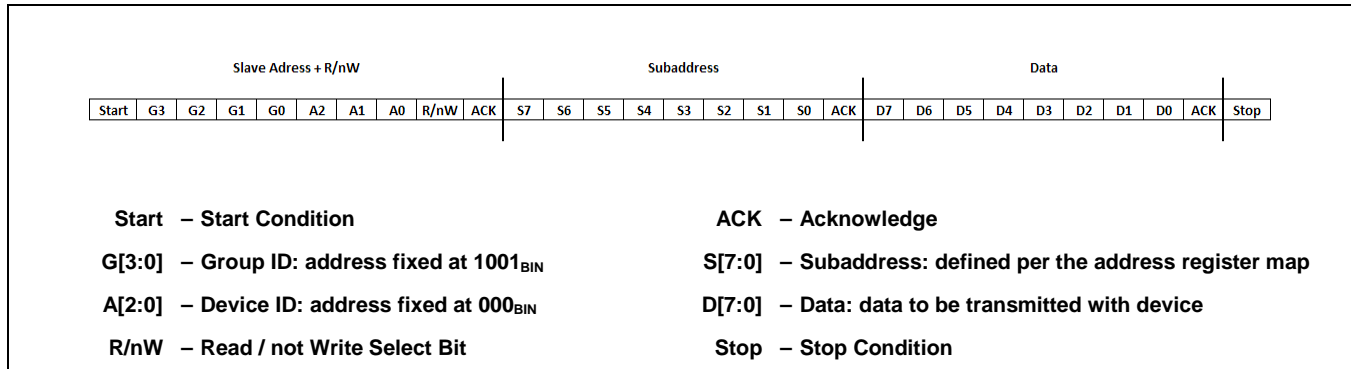
### 3 Serial Interface

The ZSPM4523 features an I<sup>2</sup>C™ slave interface that offers advanced control and diagnostic features. It supports standard and fast mode data rates and auto-sequencing, and it is compliant to I<sup>2</sup>C™ standard version 3.0.

I<sup>2</sup>C™ operation offers configuration control for termination voltages, charge currents, and charge timeouts. This configurability allows optimum charging conditions. I<sup>2</sup>C™ operation also offers fault and warning indicators. Whenever a fault is detected, the associated status bit in the STATUS register is set and the NFLT pin is pulled low. If a warning is detected, the associated status bit in the STATUS register is set, but the NFLT pin is not pulled low. (See Table 3.2.) Reading of the STATUS register resets the fault and warning status bits, and the NFLT pin is released after all fault status bits have been reset.

#### 3.1. I<sup>2</sup>C™ Subaddress Definition

**Figure 3.1 Subaddress in I<sup>2</sup>C™ Transmission**



#### 3.2. I<sup>2</sup>C™ Bus Operation

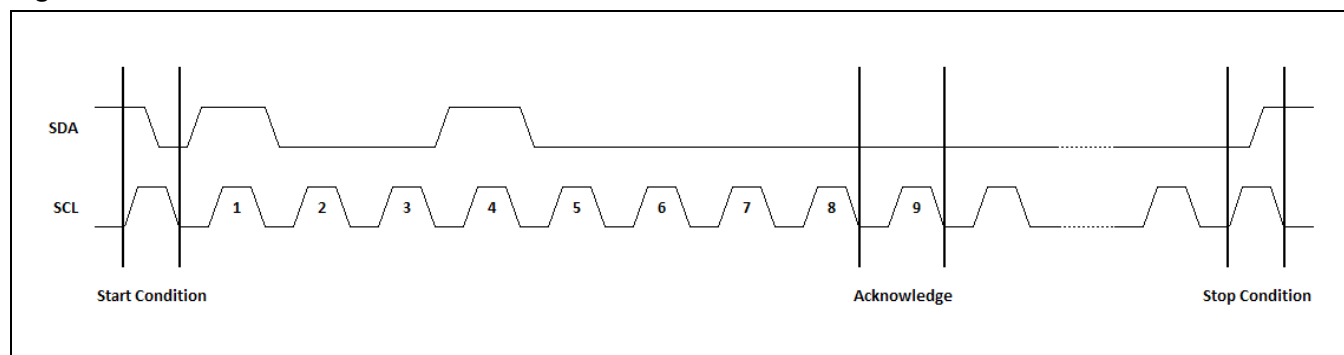
The ZSPM4523's I<sup>2</sup>C™ bus is a two-wire serial interface; the two lines are serial clock (SCL) and serial data (SDA) (see Figure 3.2). SDA must be connected to a positive supply (e.g., the VDD pin) through an external pull-up resistor. The devices communicating on this bus can drive the SDA line low or release it to high impedance. To ensure proper operation, setup, and hold times must be met. The device that initiates the I<sup>2</sup>C™ transaction becomes the master of the bus.

Communication is initiated by the master sending a START condition, which is a high-to-low transition on SDA while the SCL line is high. After the START condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (read = 1; write = 0). After receiving the valid address byte, the device responds with an acknowledge (ACK). An ACK is a low on SDA during the high of the ACK-related clock pulse. On the I<sup>2</sup>C™ bus, during each clock pulse only one data bit is transferred. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as START or STOP control commands. A low-to-high transition on SDA while the SCL input is high indicates a STOP condition and is sent by the master (see Figure 3.2).

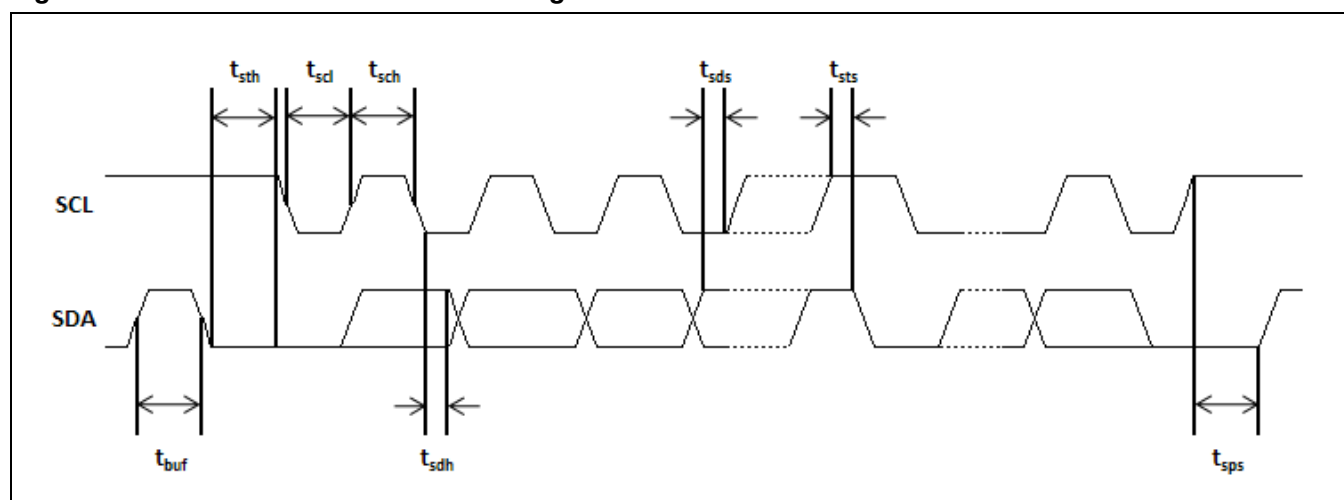
Any number of data bytes can be transferred from the transmitter to receiver between the START and the STOP conditions. Each byte of eight bits is followed by one ACK bit from the receiver. The SDA line must be released by the transmitter before the receiver can send an ACK bit. The receiver that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. An end of data is signaled by the master receiver to the slave transmitter by not generating an acknowledge after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. The transmitter must then release the data line to enable the master to generate a STOP condition.

See section 1.5 for the timing for the periods labeled in Figure 3.3.

**Figure 3.2**  $I^2C^{\text{TM}}$  STOP/START Protocol



**Figure 3.3**  $I^2C^{\text{TM}}$  Data Transmission Timing



### 3.3. Status and Configuration Registers

**Table 3.1 Register Description (Device Address = 48<sub>HEX</sub>)**

| Register   | Address (HEX) | Name                      | Default (HEX) | Description                           |
|--|---------------|---------------------------|---------------|---------------------------------------|
| 0  | 00            | STATUS                    | 00            | Status bit register.                  |
| 1  | N/A           | N/A                       | N/A           | Register not implemented.             |
| 2  | 02            | CONFIG1 <sup>1)</sup>     | EEPROM        | Configuration register.               |
| 3  | N/A           | N/A                       | N/A           | Register not implemented.             |
| 4  | 04            | CONFIG3 <sup>1)</sup>     | EEPROM        | Configuration register.               |
| 5-16   | N/A           | N/A                       | N/A           | Registers not implemented.            |
| 17   | 11            | CONFIG_ENABLE             | 00            | Enable configuration register access. |
| 18   | 12            | EEPROM_CTRL <sup>1)</sup> | 00            | EEPROM control register.              |
| <sup>1)</sup> CONFIGx and EEPROM_CTRL registers are only accessible when CONFIG_ENABLE register is written with the EN_CFG bit set to 1 (see Table 3.5). |               |                           |               |                                       |

**Table 3.2 STATUS Register—Address 00<sub>HEX</sub>**

Note: All of the STATUS register bits are READ-only.

| Data Bit   | D7      | D6                | D5       | D4       | D3  | D2                       | D1     | D0       |
|--|---------|-------------------|----------|----------|-----|--------------------------|--------|----------|
| Field Name   | VOUT_OV | Not Used          | Not Used | Not Used | TSD | Not Used                 | VIN_UV | Not Used |
| Field Name   |         | Bit Definition    |          |          |     | Indication <sup>1)</sup> |        |          |
| VOUT_OV  |         | VOUT Over-Voltage |          |          |     | Fault                    |        |          |
| TSD  |         | Thermal Shutdown  |          |          |     | Warning                  |        |          |
| VIN_UV   |         | VIN Under-Voltage |          |          |     | Warning                  |        |          |
| 1) Faults cause the NFLT pin to be pulled low. Warnings do not cause the NFLT pin to be pulled low. All status bits are cleared after register read access. NFLT pin will go high impedance (open drain output) after the status register has been read and all status bits have been reset. |         |                   |          |          |     |                          |        |          |

**Table 3.3 Configuration Register CONFIG1—Address 02<sub>HEX</sub>**

Note: All of the CONFIG1 register bits are READ/WRITE.

| Data Bit     | D7       | D6  | D5           | D4 | D3 | D2       | D1 | D0 |
|--------------|----------|---|--------------|----|----|----------|----|----|
| Field Name   | Not Used |   | V_TERM [2:0] |    |    | Not Used |    |    |
| Field Name   |          | Bit Definition  |              |    |    |          |    |    |
| V_TERM [2:0] |          | Voltage Termination (V <sub>OUT</sub> ) Configuration:<br>000 – 2.48V<br>001 – 2.54V<br>010 – 2.60V<br>011 – 2.66V<br>100 – 2.68V<br>101 – 2.72V<br>110 – 2.74V<br>111 – (Factory use only) |              |    |    |          |    |    |

**Table 3.4 Configuration Register CONFIG3—Address 04<sub>HEX</sub>**

Note: All of the CONFIG3 register bits are READ/WRITE.

| Data Bit            | D7                  | D6  | D5 | D4 | D3            | D2 | D1 | D0 |
|---------------------|---------------------|---|----|----|---------------|----|----|----|
| Field Name          | MAX_CHRG_CURR [3:0] |   |    |    | Not Used      |    |    |    |
| Field Name          |                     | Bit Definition  |    |    |               |    |    |    |
| MAX_CHRG_CURR [3:0] |                     | Maximum Charge Current (I <sub>OUT</sub> ) Configuration: |    |    |               |    |    |    |
|                     |                     | 0000 – 50mA   |    |    | 1000 – 800mA  |    |    |    |
|                     |                     | 0001 – 100mA  |    |    | 1001 – 900mA  |    |    |    |
|                     |                     | 0010 – 200mA  |    |    | 1010 – 1000mA |    |    |    |
|                     |                     | 0011 – 300mA  |    |    | 1011 – 1100mA |    |    |    |
|                     |                     | 0100 – 400mA  |    |    | 1100 – 1200mA |    |    |    |
|                     |                     | 0101 – 500mA  |    |    | 1101 – 1300mA |    |    |    |
|                     |                     | 0110 – 600mA  |    |    | 1110 – 1400mA |    |    |    |
|                     |                     | 0111 – 700mA  |    |    | 1111 – 1500mA |    |    |    |

**Table 3.5 Enable Configuration Register CONFIG\_ENABLE—Address 11<sub>HEX</sub>**

Note: The reset value for all of the CONFIG\_ENABLE register bits is 0.

| Data Bit   | D7  | D6       | D5       | D4       | D3       | D2       | D1       | D0     |
|------------|---|----------|----------|----------|----------|----------|----------|--------|
| Field Name | Not Used  | Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | EN_CFG |
| READ/WRITE | R   | R        | R        | R        | R        | R        | R        | R/W    |
| Field Name | Bit Definition  |          |          |          |          |          |          |        |
| EN_CFG     | Enable Access Control Bit for Configuration Registers 02 and 04:<br>0 – Disable access<br>1 – Enable access |          |          |          |          |          |          |        |

**Table 3.6 EEPROM Control Register EEPROM\_CTRL—Address 12<sub>HEX</sub>**

Note: The reset value for all of the EEPROM\_CTRL register bits is 0.

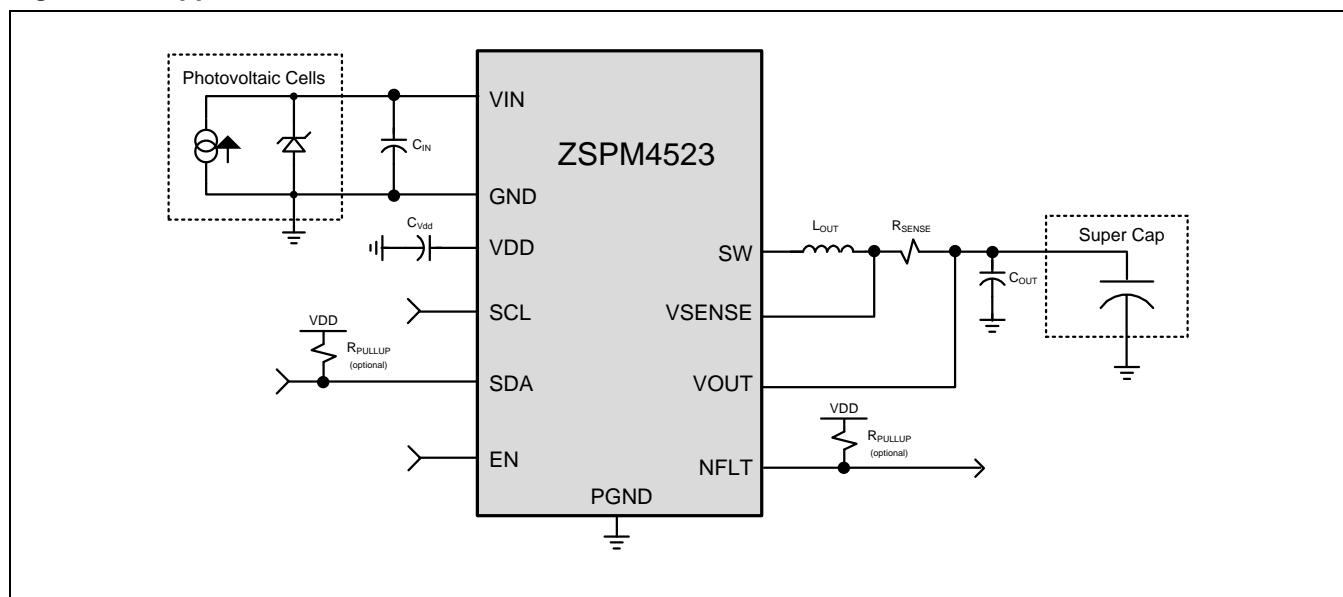
| Data Bit  | D7       | D6  | D5       | D4       | D3       | D2       | D1       | D0      |
|---|----------|---|----------|----------|----------|----------|----------|---------|
| Field Name  | Not Used | Not Used  | Not Used | Not Used | Not Used | Not Used | Not Used | EE_PROG |
| READ/WRITE  | R        | R   | R        | R        | R        | R        | R        | R/W     |
| Field Name  |          | Bit Definition  |          |          |          |          |          |         |
| EE_PROG <sup>1)</sup>   |          | EEPROM Program Control Bit for Configuration Registers 02 and 04:<br>0 – Disable EEPROM programming<br>1 – Enable EEPROM programming with data from configuration registers 2 and 4 |          |          |          |          |          |         |
| 1) EE_PROG Note: Inputs VIN and EN must be present for 200ms. |          |   |          |          |          |          |          |         |



## 4 Application Circuits

### 4.1. Typical Application Circuits

Figure 4.1 Application Circuit



### 4.2. Selection of External Components

Note that the internal compensation is optimized for a 4.7 $\mu$ F output capacitor ( $C_{OUT}$ ) and a 4.7 $\mu$ H output inductor ( $L_{OUT}$ ). Table 1.3 provides recommended ranges for most of the following components.

#### 4.2.1. $C_{OUT}$ Output Capacitor

To keep the output ripple low, a low ESR (less than 35m $\Omega$ ) ceramic capacitor is recommended for the 4.7 $\mu$ F output filter capacitor. The ESR should not exceed 100m $\Omega$ .

#### 4.2.2. $L_{OUT}$ Output Inductor

For best performance, an inductor with a saturation current rating higher than the maximum  $V_{OUT}$  load requirement plus the inductor current ripple should be used for the 4.7 $\mu$ H output filter inductor.

#### 4.2.3. $C_{IN}$ Bypass Capacitor for Input from Photovoltaic Source

For best performance, a low ESR ceramic capacitor should be used for the 10 $\mu$ F input supply bypass capacitor. If it is not a low ESR ceramic capacitor, a 0.1 $\mu$ F ceramic capacitor should be added in parallel to  $C_{IN}$ .

#### 4.2.4. $C_{VDD}$ Bypass Capacitor for VDD Internal Reference Voltage Output

For best performance, a low ESR ceramic capacitor should be used for the 100nF bypass capacitor from the VDD pin to ground.

#### 4.2.5. $R_{SENSE}$ Output Sensing Resistor

The typical value for the output sensing resistor is 50m $\Omega$ .

#### 4.2.6. Pull-up Resistors

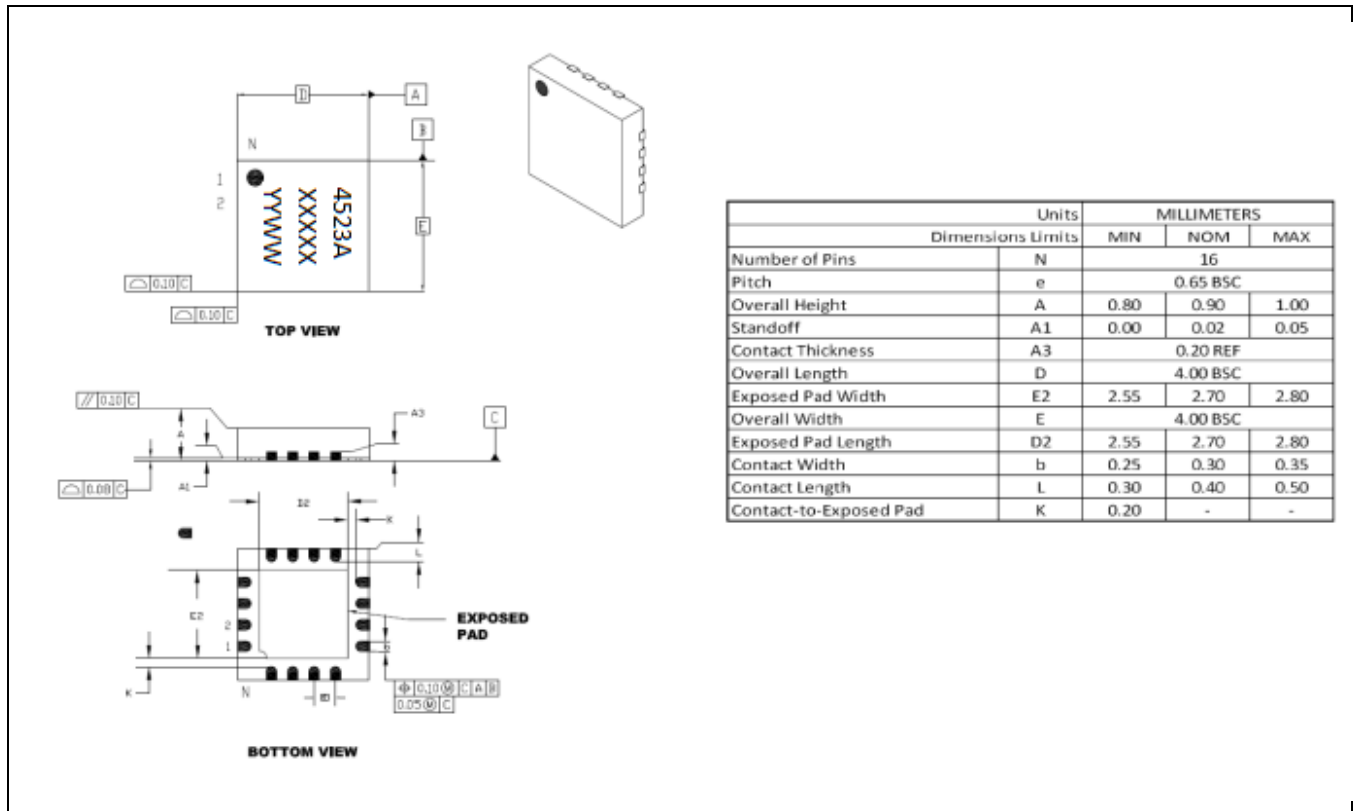
For proper function of the I<sup>2</sup>C™ interface, the SDA pin must be connected to a positive supply (e.g., the VDD pin) through an external pull-up resistor.

For proper function of the fault-warning signal on the NFLT pin, it must be connected to a positive supply (VDD) through an external pull-up resistor.

## 5 Pin Configuration and Package

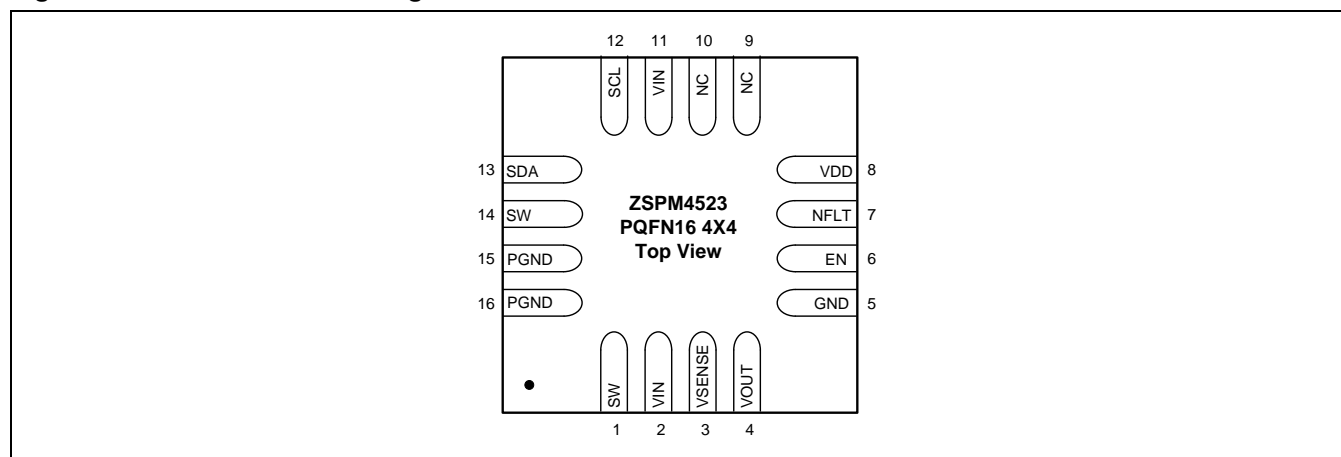
### 5.1. ZSPM4523 Package Dimensions

Figure 5.1 PQFN-16 Package Dimensions



## 5.2. Pin Assignments

Figure 5.2 ZSPM4523 Pin Assignments for 16-Pin 4mm x4mm PQFN



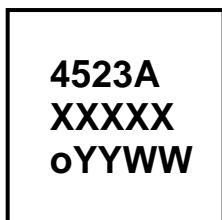
## 5.3. Pin Description

Table 5.1 ZSPM4523 Pin Description

| Pin # | Name   | Function                     | Description  |
|-------|--------|------------------------------|--|
| 1     | SW     | Switching Voltage Node       | Connected to 4.7μH (typical) inductor L <sub>OUT</sub> . Also connect to additional SW pin 14.   |
| 2     | VIN    | Photovoltaic Input Voltage   | Input voltage for the photovoltaic cell. Also connect to C <sub>IN</sub> . Also connect to additional VIN pin 11.                            |
| 3     | VSENSE | Current Sense Positive Input | Positive input for the MPPT current loop. Connect to the R <sub>SENSE</sub> resistor to VOUT and the L <sub>OUT</sub> inductor to SW.        |
| 4     | VOUT   | Super Cap Voltage            | Regulator feedback input. Connect to the R <sub>SENSE</sub> resistor to VSENSE and the C <sub>OUT</sub> capacitor to ground across the load. |
| 5     | GND    | GND                          | Primary ground for the majority of the device except the low-side power FET.   |
| 6     | EN     | Enable Input                 | When EN is high (≥ 2.2V), the device is enabled. Ground the pin to disable the device. Includes internal pull-up.                            |
| 7     | NFLT   | Inverted Fault               | Open-drain output.   |
| 8     | VDD    | Internal 3.3V Supply Output  | Connect to a 100nF capacitor to GND.   |
| 9     | NC     | Unused                       | Ground this pin for applications.  |
| 10    | NC     | Unused                       | Ground this pin for applications.  |
| 11    | VIN    | Photovoltaic Input Voltage   | Additional VIN pin for input voltage from the photovoltaic cell; connect to VIN pin 2.   |
| 12    | SCL    | Clock Input                  | I <sup>2</sup> C™ clock input.   |

| Pin # | Name | Function               | Description  |
|-------|------|------------------------|--|
| 13    | SDA  | Data Input/Output      | I <sup>2</sup> C™ data (open-drain output).  |
| 14    | SW   | Switching Voltage Node | Additional SW pin; connect to SW pin 1.  |
| 15    | PGND | Power GND              | GND supply for internal low-side FET/integrated diode. Also connect to additional PGND pin 16. |
| 16    | PGND | Power GND              | GND supply for internal low-side FET/integrated diode. Also connect to additional PGND pin 15. |

#### 5.4. Package Markings



XXXXX: Lot Number (last five digits)

O: Pin 1 mark

YY: Year

WW: Work Week

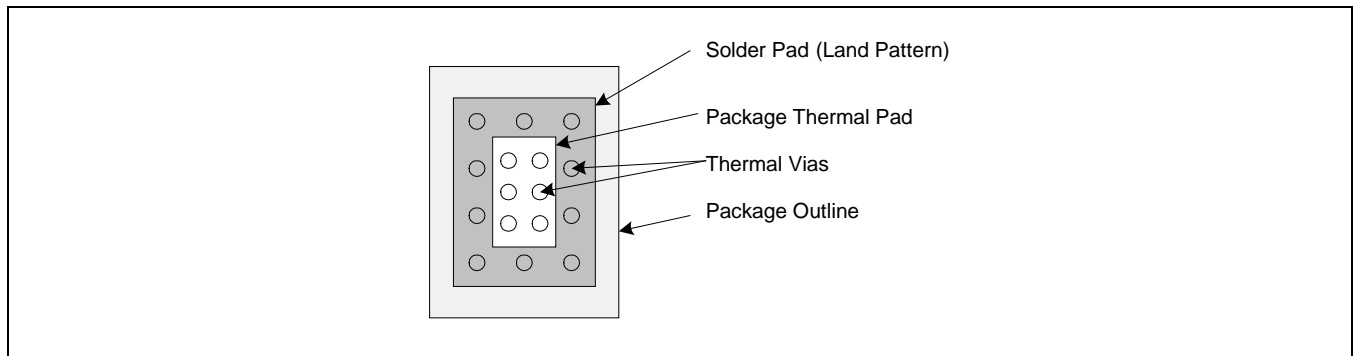
## 6 Layout Recommendations

To maximize the efficiency of this package for application on a single layer or multi-layer PCB, certain guidelines must be followed when laying out this part on the PCB.

### 6.1. Multi-Layer PCB Layout

The following are guidelines for mounting the exposed pad ZSPM4523 on a multi-Layer PCB with ground a plane. In a multi-layer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors, including die area, number of thermal vias, and thickness of copper, etc.

**Figure 6.1 Package and PCB Land Configuration for Multi-Layer PCB**



**Figure 6.2 JEDEC Standard FR4 Multi-Layer Board – Cross-Sectional View**

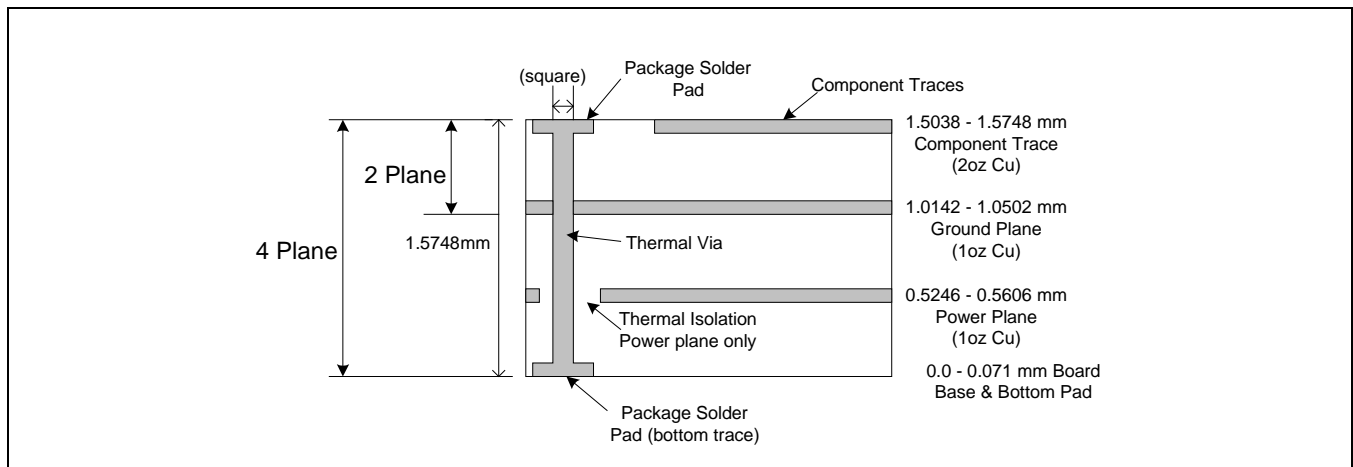
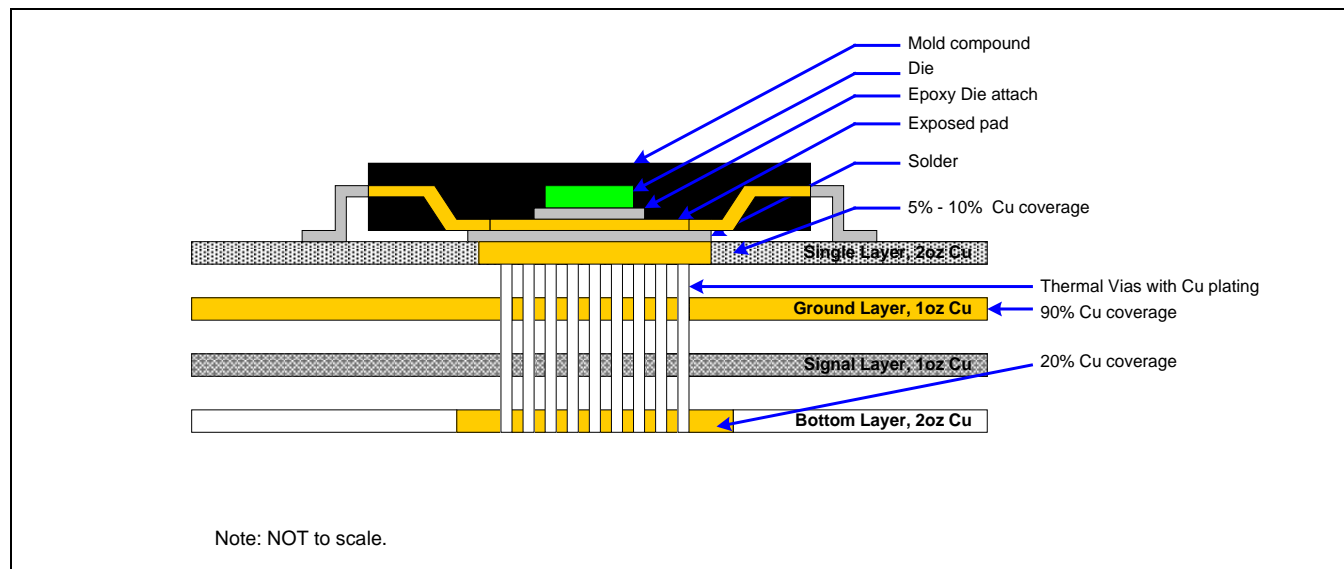


Figure 6.3 is a representation of how the heat can be conducted away from the die using an exposed pad package. Each application will have different requirements and limitations, and therefore the user should use sufficient copper to dissipate the power in the system. The output current rating for the linear regulators might need to be de-rated for higher ambient temperatures. The de-rated value will depend on calculated worst case power dissipation and the thermal management implementation in the application.

**Figure 6.3 Conducting Heat Away from the Die using an Exposed Pad Package**

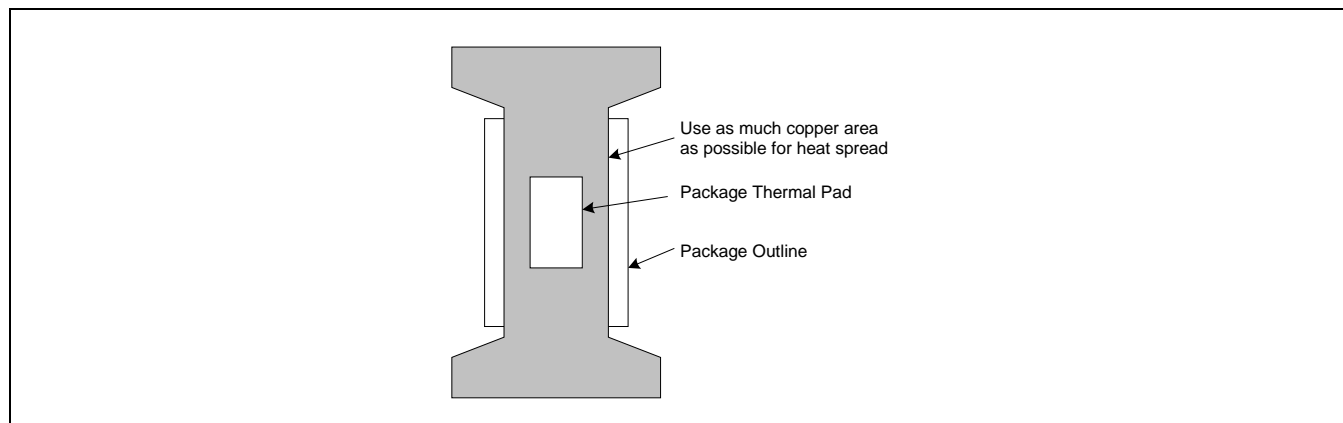


## 6.2. Single-Layer PCB Layout

Layout recommendations for a single-layer PCB: Utilize as much copper area for power management as possible. In a single-layer board application, the thermal pad is attached to a heat spreader (copper areas) by using a low thermal impedance attachment method (solder paste or thermal conductive epoxy).

In both of the methods mentioned above, it is advisable to use as much copper trace as possible to dissipate the heat.

**Figure 6.4 Application Using a Single-Layer PCB**



**Important:** If the attachment method is NOT implemented correctly, the functionality of the product is NOT guaranteed. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.

## 7 Ordering Information

| Ordering Code | Description  | Package                             |
|---------------|--|-------------------------------------|
| ZSPM4523AA1W  | ZSPM4523 High-Efficiency Regulator for Super Capacitor Systems | 16-pin PQFN / 7" Reel (1000 parts)  |
| ZSPM4523AA1R  | ZSPM4523 High-Efficiency Regulator for Super Capacitor Systems | 16-pin PQFN / 13" Reel (3300 parts) |
| ZSPM4523KIT   | ZSPM4523 Evaluation Kit  |                                     |

## 8 Related Documents

| Document   |
|--|
| <i>ZSPM4523 Feature Sheet</i>  |
| <i>ZSPM4523 Evaluation Kit Description</i>   |
| <i>ZSPM4523 Application Note – Solar Powered Battery Management and Charging Solutions</i> |

Visit IDT's website [www.IDT.com](http://www.IDT.com) or contact your nearest sales office for the latest version of these documents.

## 9 Document Revision History

| Revision | Date              | Description  |
|----------|-------------------|--|
| 1.00     | February 14, 2013 | First release  |
| 1.01     | October 5, 2014   | Update for contacts and imagery for cover and headers. |
|          | January 29, 2016  | Changed to IDT branding.                               |



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.