ZSSC3286 (FW v1.3.0)

IO-Link Ready Dual Channel Resistive Sensor Signal Conditioner IC

Description

The ZSSC3286 is a dual path sensor signal conditioning IC (SSC) for highly accurate amplification, digitization, and sensor-specific correction of sensor signals.

The ZSSC3286 supports IO-Link connectivity with an integrated IO-Link stack running the IO-Link Smart Sensor Profile for digital measuring and switching sensors.

The device is suitable for resistive bridge and half-bridge sensors, capacitive sensing elements as well as external voltage source elements, and single-element sensors (for example, Pt100 and external temperature sensor diodes) powered by an on-chip current source for temperature sensing.

Digital compensation of the sensor offset, sensitivity, temperature drift, and nonlinearity is accomplished via a 32-bit ARM M3 based math core running a correction algorithm with calibration coefficients stored in a non-volatile, reprogrammable memory.

The programmable, integrated sensor front-end allows optimally applying various sensors for a broad range of applications.

The ZSSC3286 supports system calibration and firmware update via the IO-Link or I2C interface.

Applications

- Industrial sensors with IO-Link interface
- Smart and digital sensors for energy-efficient solutions
- Single/Dual/Differential sensing
- Factory automation
- Process automation
- Calibrated, continuously operating sensors for flow, pressure, load, level, or temperature

Features

- IO-Link stack embedded
- Smart Sensor Profile in COM3 mode
- Firmware update via IO-Link
- Calibration and configuration via IO-Link
- Zero Adjustment via IO-Link and GPIO
- Clock recovery system, no external crystal needed
- IODD generator included
- Accommodates nearly all resistive bridge sensors in various configurations:
  - Resistive bridge or half-bridge
  - Resistive divider string
  - Voltage source
- Accommodates nearly all capacitive sensor types
  - Single or dual capacitive cells
  - Isolated or grounded
  - Shield driver available
- On-chip temperature sensor
- External temperature sensing supported
- Programmable 16-bit digital-to-analog-converter and output (supporting “True-0Volt”-output):
  - Absolute voltage output (supporting 0V to 1V, 0V to 5V, or 0V to 10V applications)
  - 4mA to 20mA current-loop output supported
- Wide operational temperature and supply range
- On-chip voltage regulators for sensor supply, and IC operation
- Programmable sensor-signal-conditioning math core
- Reprogrammable, non-volatile memory (NVM)
- On-chip diagnostics:
  - Sensor connection
  - AFE self-test
  - Memory integrity

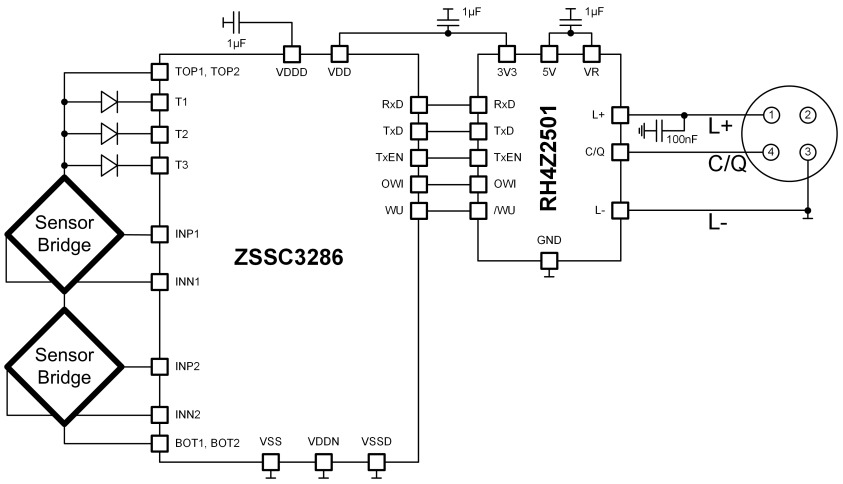

Figure 1. Typical Application Diagram

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1 Overview

1.1 Block Diagram

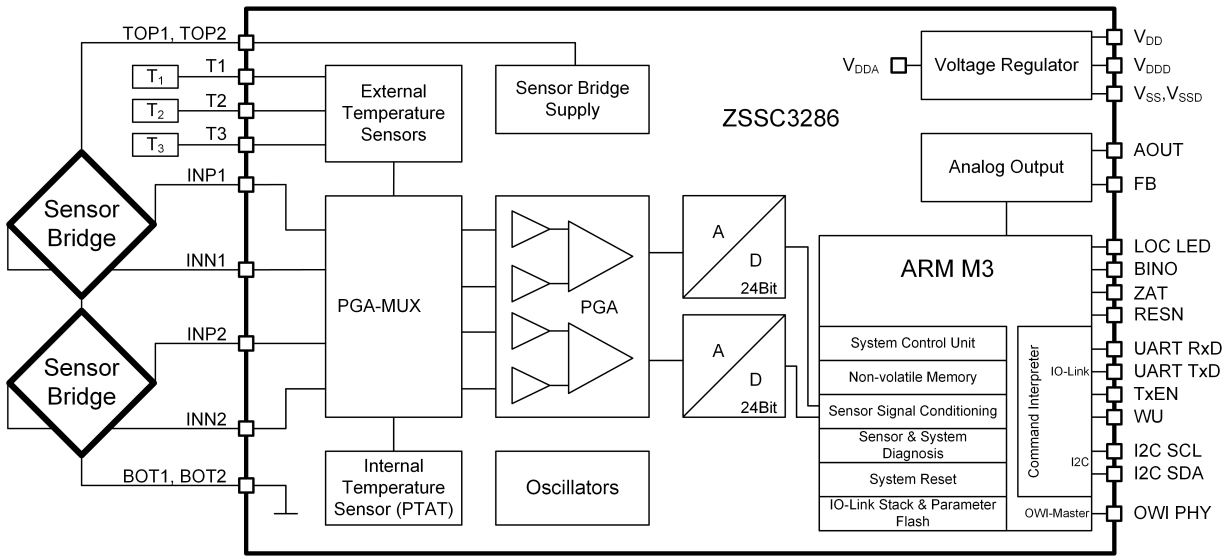

Figure 2. Block Diagram

1.2 Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature Range
ZSSC3286CI1B	DICE on 304µm wafer no inking		Wafer Box	-40°C to 125°C
ZSSC3286CI5B	DICE on 304µm wafer with inking		Wafer Box	-40°C to 125°C
ZSSC3286CI1C	DICE on 304µm wafer no inking		Wafer Sawn on Frame	-40°C to 125°C
ZSSC3286CI1D-ES	DICE on 304µm wafer no inking		Waffle Pack (Engineering Samples)	-40°C to 125°C
ZSSC3286CI3R	5 x 5 mm2 NDG40S1 (40-VFQFPN)	MSL1	13 inch Reel	-40°C to 125°C
ZSSC3286CI8R	WLCSP	MSL1	13 inch Reel	-40°C to 125°C
ZSSC3286KIT	Modular ZSSC3286 SSC Evaluation Kit including three interconnecting boards, five ZSSC3286 QFN40 samples, one RH4Z2501 PMOD, one two channel IO-Link master and cable. Software is available for download on www.renesas.com/ZSSC3286.			

Note: All ZSSC3286 product options will be delivered with firmware version 1.2.0. An update of the firmware to 1.3.0 is possible and described in section 11.

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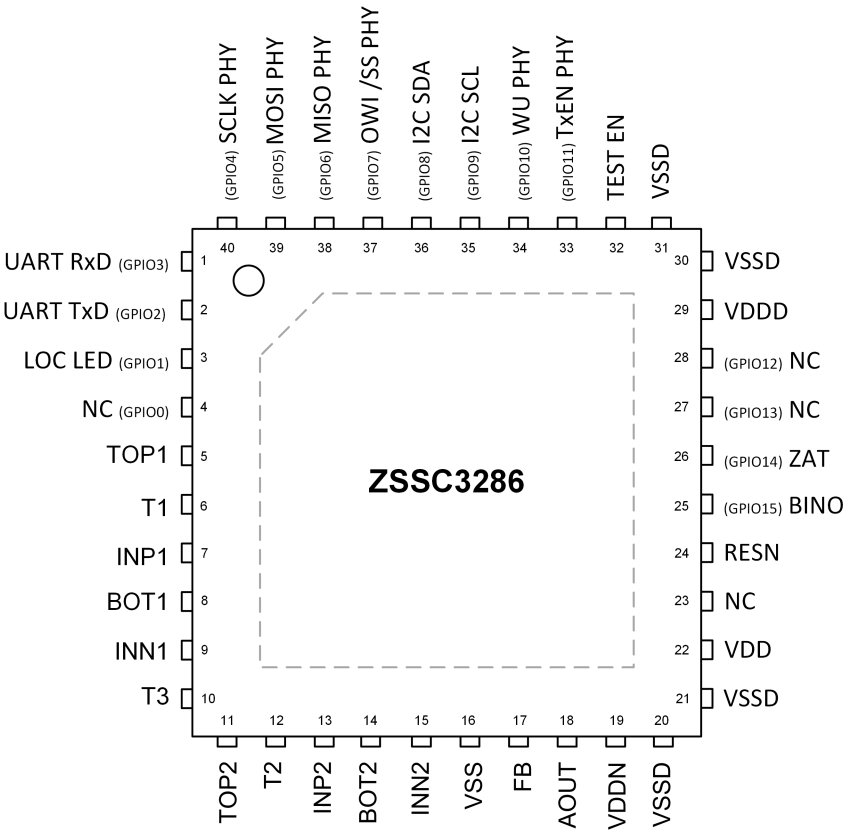
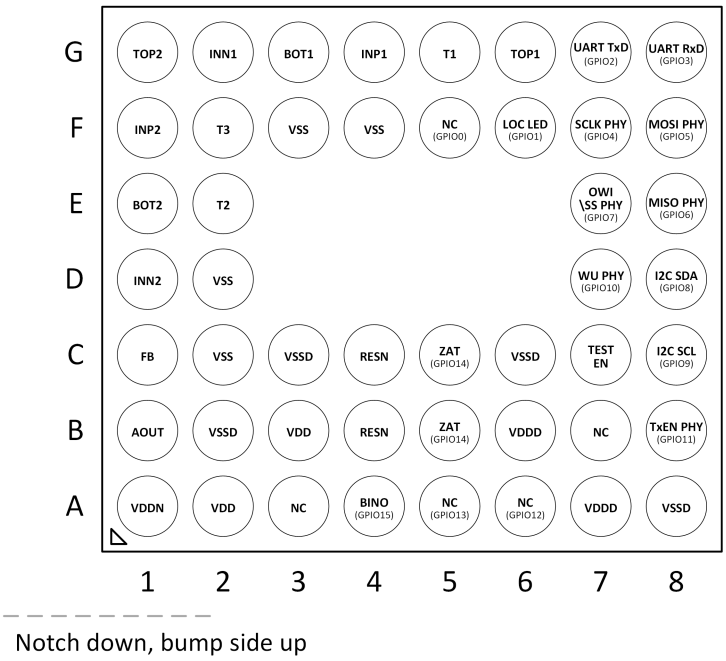
2 Pin Information

2.1 Pin Assignments



QFN-bottom plate, exposed pad.

Figure 3. Pin Assignments - QFN40



Notch down, bump side up

Figure 4. Pin Assignments - WLCSP

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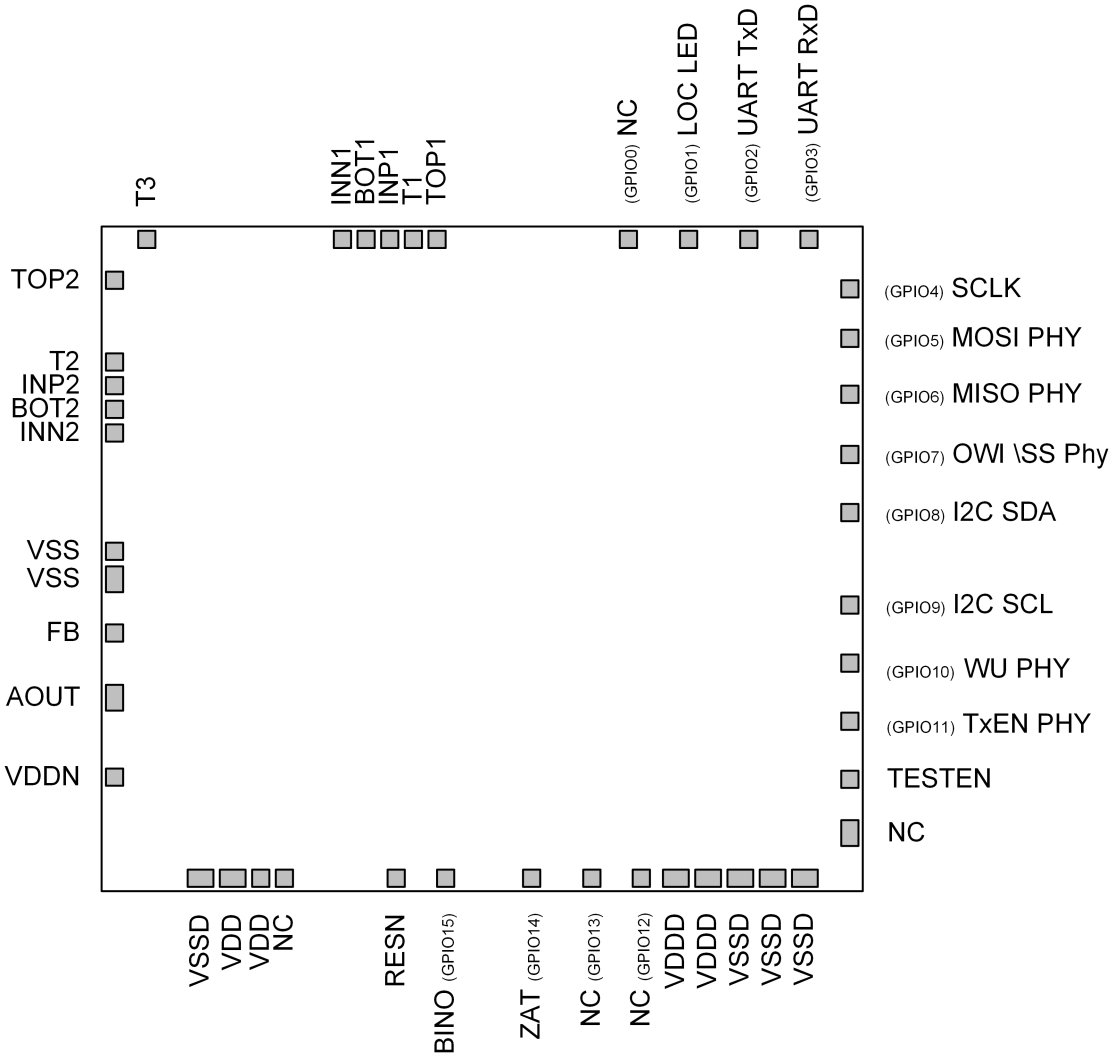

Figure 5. Pad Layout Bare Die

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2.2 Pin Descriptions

QFN40 Pin Number	WLCSP Pin Number	Name	Type	Description
2	G7	UART TxD	Digital Output	GPIO2: UART transmit function for IO-Link PHY communication
1	G8	UART RxD	Digital Input	GPIO3: UART receive function for IO-Link PHY communication
3	F6	LOC LED	Digital Output	GPIO1: Timer functionality for Locator LED
4	F5	NC	Digital Input/Output	GPIO0: Not connected. Leave pin floating.
5	G6	TOP1	Analog Input/Output	Positive sensor (bridge 1) supply or sensor-signal input
6	G5	T1	Analog Input/Output	External temperature sensor
7	G4	INP1	Analog Input/Output	Positive sensor (bridge 1) signal
8	G3	BOT1	Analog Input/Output	Sensor (bridge 1) ground or sensor-signal input
9	G2	INN1	Analog Input/Output	Negative sensor (bridge 1) signal
10	F2	T3	Analog Input/Output	External temperature sensor 3
11	G1	TOP2	Analog Input/Output	Positive sensor (bridge 2) supply or sensor-signal input
12	E2	T2	Analog Input/Output	External temperature sensor 2
13	F1	INP2	Analog Input/Output	Positive sensor (bridge 2) signal
14	E1	BOT2	Analog Input/Output	Sensor (bridge 2) ground or sensor-signal input
15	D1	INN2	Analog Input/Output	Negative sensor (bridge 2) signal
16	C2, D2, F3, F4	VSS	Ground	Power supply ground
17	C1	FB	Analog Output	Feedback pin for AOUT. No connection if not used.
18	B1	AOUT	Analog Output	Analog smart-sensor output signal
19	A1	VDDN	Analog Output	Negative voltage output, charge pump buffer capacitor
20	A8, B2, C3, C6	VSSD	Ground	Digital power supply ground
21	A8, B2, C3, C6	VSSD	Ground	Digital power supply ground
22	A2, B3	VDD	Supply	Power supply
23	A3, B7	NC	Analog Output	Not connected. Leave pin floating.
24	B4	RESN	Digital Input	Digital IC reset (low active); internal pull-up
25	A4	BINO	Digital Output	GPIO15: Binary Output (BINO) for Sensor Switching Signal
26	B5, C5	ZAT	Digital Input/Output	GPIO14: Zero Adjustment Trigger (ZAT) for Zero Adjustment feature
27	A5	NC	Digital Input/Output	GPIO13: Not connected. Leave pin floating.
28	A6	NC	Digital Input/Output	GPIO12: Not connected. Leave pin floating.
29	A7, B6	VDDD	Analog I/O	Buffer cap connection for internal VDDD
30	A8, B2, C3, C6	VSSD	Ground	Digital power supply ground
31	A8, B2, C3, C6	VSSD	Ground	Digital power supply ground
32	C7	TEST EN	–	Renesas internal use only. Connect to VSSD
33	B8	TxEn PHY	Digital Output	GPIO11: UART transmit enable function for IO-Link PHY communication
34	D7	WU PHY	Digital Output	GPIO10: Wake-Up for IO-Link PHY communication
35	C8	I2C SCL	Digital Input	GPIO9: I2C SCL
36	D8	I2C SDA	Digital Input/Output	GPIO8: I2C SDA
37	E7	OWI /SS PHY	Digital Input/Output	GPIO7: OWI master interface or Slave Select for IO-Link PHY communication
38	E8	MISO PHY	Digital Input	GPIO6: SPI master function - MISO for IO-Link PHY communication
39	F8	MOSI PHY	Digital Output	GPIO5: SPI master function - MOSI for IO-Link PHY communication
40	F7	SCLK PHY	Digital Output	GPIO4: SPI master function - Clock for IO-Link PHY communication
N/A	B7	NC	Analog Output	Not connected. Leave pin floating.
	N/A	exposed pad	-	QFN-bottom plate, Die-bottom/substrate. Recommendation is to connect to VSS, PAD to be used for heat dissipation and additional EMC robustness.

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3 Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to the absolute maximum conditions for extended periods may affect the device reliability.

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
T_J	Junction temperature		–	135	°C
T_S	Storage temperature		-45	150	°C
	ESD: Human Body Model tested per JS-001-2017	Pins: INPx, INNx, TOPx, BOTx, Tx, VDDD	–	2000	V
		Pins: GPIOx, VDD, VDDN, VSS, VSSD, AOUT, FB, RESN, NC	–	4000	V
	ESD: Charged Device Model tested per JS-002-2014 (OFN package)	All Pins	–	750	V
	ESD: Charged Device Model tested per JS-002-2014 (WLCSP package)	All Pins	–	500	V
	Latch-up	Tested per JESD78E; Class 2, Level A	-100	+100	mA
V_{DD_max}	Maximum allowed for voltage supply	Referenced to VSS	-0.3	6.5	V
V_{IF_max}	Voltage at digital I/O	Referenced to VSSD	-0.3	5.5	V

3.2 Thermal Information

Table 2. Thermal Information

Symbol	Parameter	Conditions	Typical	Unit
θ_{JA}	Theta JA	40Ld 5×5 QFN Package, 0 m/s air flow	25.8	°C/W
		40Ld 5×5 QFN Package, 1 m/s air flow	22.4	°C/W
		40Ld 5×5 QFN Package, 2 m/s air flow	20.8	°C/W
θ_{JB}	Theta JB	40Ld 5×5 QFN Package	1.3	°C/W
θ_{JC}	Theta JC	40Ld 5×5 QFN Package	24.4	°C/W

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3.3 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DD}	Power supply voltage	1.8	–	5.5	V
	Flash write/erase	2.7			
	With optional “True-0V” at analog output	2.7			
T_J	Junction temperature (depending on the ordered device, see section 1.2 for details.)	-40	–	125	°C
C_{VDD}	External capacitance between VDD and VSS	10 ±20%		22 ±20%	µF
C_{V3D}	External capacitance between VDDD and VSS	1 -20%	–	1 +20%	µF
C_{VDDN}	External capacitance between VDDN and VSS, with optional “True-0V” at analog output	1 -20%	–	1 +20%	µF
C_{TOP_EMC}	Recommended, external capacitance between TOP and VSS for electro-magnetic immunity (EMI)	0	6.8	8	nF
C_{AOUT_EMC}	Recommended, external capacitance between AOUT versus VDD and VSS for EMI suppression [1]	0	22	33	nF
I_{Sensor}	Load current through external sensor element [2]	0.005	0.5	2	mA
$V_{DioDrop}$	External temperature diode and RTD input range, drop over external element referenced to T1, T2, T3 pin	0.2	–	1.2	V
V_{Sens_in}	Absolute sensor signal input level, INN, INP pins	0.2	–	1.2	V
$I_{max\_AOUT\_V}$	Maximum current load at AOUT pin for voltage outputs	0	5	–	mA
S_{RVDD_POR}	Recommended VDD rise slew rate for power-on-reset (POR)	1.5	–	–	V/ms
I_{max_GPIO}	Maximum overall GPIO driver strength	–	–	120	mA

1 For applications with OWI interface or analog voltage-output.

2 With ratiometric sensor supply configuration, for example, a ratiometric bridge or bridge as temperature sensor with internal or external temperature sensitive resistor

3.4 Electrical Specifications

All parameter values are valid only under operating conditions specified in section 3.3. All voltages are referenced to VSS.

Table 4. IC Supply

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{IC}	Current consumption, active mode (depending on settings)	Excluding connected sensor elements	–	8	15	mA
VDDA	Internally generated analog supply		1.6	1.65	1.85	V

Table 5. Sensor Supply

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{TOP}	Sensor bias voltage in ratiometric Supply Mode	Ratiometric sensor voltage supply	–	VDDA	–	V
I_{bias_TOP}	Sensor bias current used in Source Mode	Programmable in 10 steps: 0µA, 5µA, 10µA, 20µA, 40µA, 80µA, 100µA, 160µA, 200µA, 500µA	0	–	500	µA
I_{biasN_BOT}	Sensor current used in Sink Mode	Programmable in 2 steps: 20µA, 100µA	20	–	100	µA
I_{ERR}	Relative bias current (I_{bias_TOP} and I_{biasN_BOT}) error	Overall	-10	–	10	%
		Over temperature range	-1	–	1	
R_{TH}, R_{TL}	TOP/BOT bias resistor	Programmable in 12 steps: open, 1.33kΩ, 2kΩ, 4kΩ, 8kΩ, 10kΩ, 14kΩ, 18kΩ, 20kΩ, 24kΩ, 28kΩ, 40kΩ	1.3	–	40	kΩ
dR_{TH}, dR_{TL}	TOP/BOT bias resistor process variation		-30	–	30	%
TK of R_{TH}, R_{TL}	TOP/BOT bias resistor temperature variation	T = -55°C to 125°C	–	–	1.3	%

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Table 6. Analog-to-Digital Converter (ADC, A2D)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
r_{ADC}	Resolution		10	16	24	Bit
V_{ADCmid} (AGND)	Differential ADC input Common Mode	With internal regulator supplying TOP pin, typical: $V_{TOP/2}$ = 875mV (=PGA output Common Mode level)	–	0.5	–	V_{TOP}
$\Delta_{ADC,c}$	Differential input offset shift	Sensor signal offset versus maximum sensor signal. Programmable in 8 steps.	0	–	7/8	V_{shift}/V_{fs}
$ENOB_{Res}$ [1]	Effective number of bits for resistive Analog Front End, $3\sigma_{Noise}$ based	Gain = 1.32, r_{ADC} = 24 bit, no oversampling	–	17	–	Bit
		Gain = 28, r_{ADC} = 16 bit, no oversampling	–	12	–	Bit
		Gain = 100, r_{ADC} = 15 bit, no oversampling	–	10	–	Bit
		Gain = 495, r_{ADC} = 24 bit, no oversampling	–	11	–	Bit

1 $ENOB_{Res} = LOG2\left(\frac{2^{r_{ADC}}}{3\sigma_{Noise}}\right)$ with for example, r_{ADC} [Bit] = 24.

Table 7. Digital-to-Analog Converter (DAC) and Analog Output

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
VDD	VDD operating range	AOUT modes using 1V buffer	1.8	–	5.5	V
		AOUT modes using VDD buffer	2.7		5.5	
$t_{AOUTsettle}$	Time from digital value applied at DAC and voltage at VOUT	10% to 90% input step: V_{AOUT} at 90% of final value	–	–	100	µs
V_{OUT_START}	Voltage at AOUT during startup		–	0	–	V
V_{AOUT}	Output voltage at pin AOUT	Ratiometric Voltage Mode (VDD Buffer)	0	–	VDD	V
		1V absolute Voltage Mode (1V Buffer)	0	–	1	
I_{OUTMAX}	Short current limit at pin AOUT	AOUT modes using VDD Buffer • short to VDD or VSS • programmable in 4 steps	3	5	9	mA
			8	12	20	
			13	19	25	
			18	25	32	
C_{load}	Load capacitance at AOUT	For example: cap for EMC: 33nF, ECU load: 10nF)	10 [1]	–	50	nF
r_{DAC}	Resolution		–	16	–	Bit

1 In case of enabled Power-Ground Loss detection minimum 10nF on AOUT is required.

Table 8. Programmable-Gain Amplifier (PGA)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
G_{amp}	Gain	120 steps	1.32	–	495	V/V
G_{err}	Gain error	Referenced to nominal gain: Gain = 1.32 to 5	-2.5	0	-2.5	%
		Gain = 6 to 125	-5		5	
		Gain = 126 to 495	-10		10	
$G_{errTemp}$	Gain error over-temperature	Temperature compensated sensors do not require calibration over temperature.	-0.2	–	0.2	%
V_{CMin}	Supported input Common Mode		20	50	70	% V_{TOP}
V_{ioffsc}	Differential input offset shift	Programmable in 30 steps: Gain1 ≤ 223	-28.1	0	28.1	mV
		Gain1 = 275	-22.5	0	22.5	

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Table 9. Sensor Signal Conditioning (SSC) Performance for Resistive Sensor

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
OUR	Output Update Rate	• **3 measurements: signal+, signal-, auxiliary** • r_{ADC} = 16bit (main) • bridge settling = 20µs (main) • r_{ADC} = 15bit (temp) • diagnosis ≤ 350µs • SSC-corrected digital output	–	1.15	–	kHz
		• **2 measurements: signal+, auxiliary** • r_{ADC} = **15bit** (main) • bridge settling = 20µs (main) • r_{ADC} = 15bit (temp) • diagnosis ≤ 350µs • SSC-corrected digital output	–	1.82	–	kHz
		• **2 measurements: signal+, auxiliary** • r_{ADC} = **16bit** (main) • bridge settling = 20µs (main) • r_{ADC} = 15bit (temp) • diagnosis ≤ 350µs • SSC-corrected digital output	–	1.63	–	kHz
t_{AOUT_SR}	Step response (AOUT)	• **3 measurements: signal+, signal-, auxiliary** • r_{ADC} = 16bit (main) • bridge settling = 20µs (main) • r_{ADC} = 15bit (temp) • diagnosis ≤ 350µs • at AOUT (90% final)	–	–	1.51	ms
		• **2 measurements: signal+, auxiliary** • r_{ADC} = **15bit** (main) • bridge settling = 20µs (main) • r_{ADC} = 15bit (temp) • diagnosis ≤ 350µs • at AOUT (90% final)	–	–	0.86	ms
		• **2 measurements: signal+, auxiliary** • r_{ADC} = **16bit** (main) • bridge settling = 20µs (main) • r_{ADC} = 15bit (temp) • diagnosis ≤ 350µs • at AOUT (90% final)	–	–	0.99	ms
$t_{IO\text{-}Link\_SR}$	Step response (IO-LINK)	• 2 measurements: signal+, auxiliary • r_{ADC} = 15bit (main) • bridge settling = **20µs** (main) • r_{ADC} = **15bit** (temp) • diagnosis **≤ 350µs** • IO-Link cycle time = 600µs	–	–	1.98	ms
		• 2 measurements: signal+, auxiliary • r_{ADC} = 15bit (main) • bridge settling = **80µs** (main) • r_{ADC} = **14bit** (temp) • diagnosis **disabled** • IO-Link cycle time = 600µs	–	–	2.00	ms

The performance of the capacitive front end is summarized in tables Table 28 to Table 33.

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Table 10. Analog Inputs for Resistive Sensor

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{INP1}, V_{INN1}, V_{INP2}, V_{INN2}	Absolute sensor input	Voltages at INPx and INNx pin; resulting minimum/maximum differential voltages: -800mV < V_{INdiff} < 800mV	0.2	–	1.2	V
V_{TEXT}	External temperature diode or RTD input range	At T1, T2, T3 pin (see Table 5 and *ExtTempBrdgIBias* for available configuration options)	0.3	–	1.2	V
R_{SENSOR}	External sensor (bridge) resistance		0.825	–	60	kΩ
$\|V_{DIFFin}\|$	Differential input signal range	Referenced to sensor supply (V_{TOP})	–	–	800	mV

Table 11. Diagnostics for Resistive Sensor

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_{open}	Broken sensor: values >R_{open} set a failure flag	• INP1 vs. INN1 • INP2 vs. INN2 **Note:** INN is drawn to VSS! This is not applicable in sensor configuration with one bridge at both frontends!	100	120	150	kΩ
R_{short}	Shorted sensor: values <R_{short} set a failure flag	• INP1 vs. INN1 • INP2 vs. INN2 • INP1 vs. INP2 • INP2 vs. INN1	120	–	220	Ω
V_{RDAC}	RDAC differential output voltage	VDDA = 1.65V: • S = 00	–	2	–	mV
		• S = 01	–	10	–	
		• S = 10	–	100	–	
		• S = 11	–	200	–	
R_{T_open}	T1, T2, T3 connection check: open	Broken Tx sensor: values >R_{T_open} set a failure flag and can be configured in 3 level **Note:** INN is drawn to VSS! This is not applicable in sensor configuration with one bridge at both frontends!	1.6	2	3	MΩ
			0.4	0.5	0.6	
			0.07	0.1	0.13	
t_{T_open}	Diagnosis time; depends on C_{ts} and R_{T_open}	Time spent between failure occurrence and output signalization.	0.1	–	10	ms
R_{T_short}	T1, T2, T3 connection check: short to TOP, BOT, INP, INN	Shorted Tx sensor: values <R_{T_short} set a failure flag: • configuration for Pt1000	320	500	650	Ω
$VDDD_{BOD}$	VDDD brown out detection	VDDD < $VDDD_{BOD}$ system is in reset state	85	90	92	%VDDD
V_{LOSS}	Power/ground loss with respect to AOUT	• V_{AOUT} – VDD > V_{LOSS} • V_{AOUT} – VSS < V_{LOSS}	–	0.2	–	V

Table 12. Power-Up

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t_{STA1}	Startup time	VDD ramp up to interface communication	–	7.5	10	ms
t_{STA2}		VDD ramp up to analog operation; depends on the configuration used	–	7.5	10	ms

Table 13. Oscillator

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{CLK_HF}	Internal HF-oscillator frequency	At T=27°C	15.8	16	16.2	MHz
		Across temperature range	15	–	17	
f_{CLK_LF}	Internal LF-oscillator frequency		25	32	41	kHz

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Table 14. Internal Temperature Sensor

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
r_{Temp}	Internal temperature sensor resolution	Differential output voltage	–	220	–	µV/K

Table 15. Digital IO Pins

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IL}	Input low Voltage	voltage level where the input is recognized as low level	–	–	30	%VDD
V_{IH}	Input high Voltage	voltage level where the input is recognized as high level	70	–	–	%VDD
V_{Ihys}	Input hysteresis		10	–	35	%VDD
V_{OL}	Output low Voltage		–	–	8	%VDD
V_{OH}	Output high Voltage		92	–	–	%VDD
I_{OL}	Output drive low current	$V_{PAD} = V_{OL}$: VDD = 1.8V	1	–	2.4	mA
		VDD = 2.6V	2.7		6.6	
		VDD = 5V	9		20	
I_{OH}	Output drive high current	$V_{PAD} = V_{OH}$: VDD = 1.8V	1.2	–	2.3	mA
		VDD = 2.6V	3.2		6.4	
		VDD = 5V	10.9		20.2	
I_{pullup}	Weak pull-up current at pins RESN & ZAT	V_{PAD} = 0V: VDD = 1.8V	5	–	13	µA
		VDD = 2.6V	17		50	
		VDD = 5V	84		250	
$I_{pulldown}$	Weak pull-down current at pin WAKEUP	V_{PAD} = VDD: VDD = 1.8V	5	–	11	µA
		VDD = 2.6V	17		35	
		VDD = 5V	80		160	

Table 16. Serial Interfaces

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$f_{C,UART}$	UART clock frequency (for IO-Link protocol)		–	230.4	–	kBit/s
$f_{C,I2C}$	I2C clock frequency		–	–	1	MHz
CD_{OWI}	OWI data rate		–	4	–	kBit/s

Table 17. Flash Memory

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t_{PROG}	NVM program time	Programming time for complete configuration and calibration page	–	360	–	ms
n_{NVM}	NVM endurance	Number of reprogramming cycles	20000	–	–	Numeric
$t_{RET, NVM}$	Data retention		10	–	–	Years

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4 Basic System Configuration

4.1 System Modes/System Start

The ZSSC3286 can operate in three different main operating modes:

Bootloader — It is started after successfully passing the initialization phase of the ZSSC3286 hardware. ZSSC3286 checks that firmware and CCP CRC are correct to allow starting the firmware in SIO Mode. The bootloader allows to update the CCP content and firmware. The bootloader itself can not be updated.

Standard I/O Mode (SIO) — It is the startup operation mode after passing the bootloader. The SIO mode supports the Command Mode and Cyclic Mode operational states. The ZSSC3286 waits for actions on I2C interface or the wakeup request (WURQ) to start transition to IO-Link COM Mode.

I/O-Link COM Mode — It is the default operation mode if IO-Link communication is established during operation in the field or during calibration process. The I/O Link COM mode supports the Command Mode and Cyclic Mode operational states.

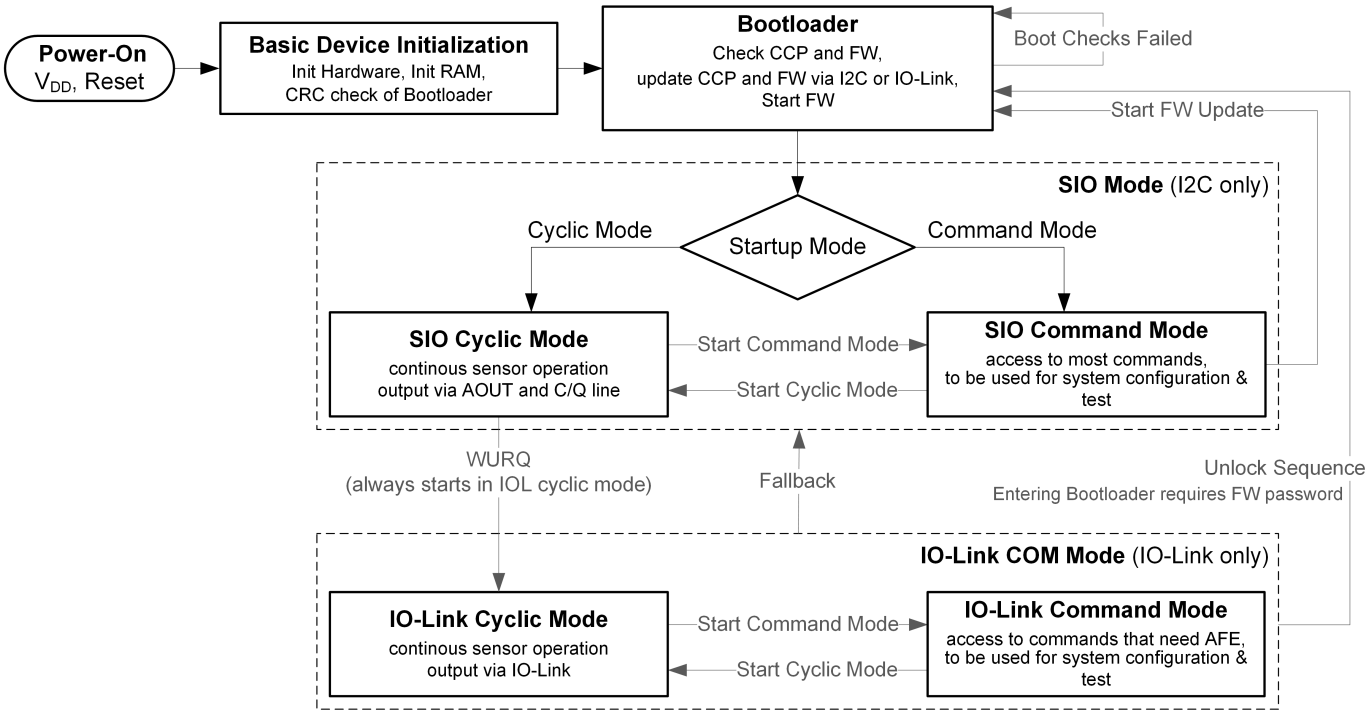

Figure 6. Main Operation Modes

SIO Mode and I/O-Link Mode will support the following operation states:

Cyclic Mode — This is the default mode for continuously operating sensors. In this mode autonomous, cyclically repeated sensor measurements are performed and related digital (via IO-Link in IO-Link COM Mode), and/or analog output (via AOUT in SIO Mode) and/or digital alarm output (C/Q line in SIO Mode) updates are provided. The cyclic sequences for sensor measurements and system diagnostic measurements are configurable and allow to define the output update rate of the conditioned sensor signals.

Command Mode — This is the most appropriate mode for evaluation, test, and calibration purposes. In this mode, all commands to support calibration process via serial interface commands are available. Command Mode is intended for applications that require repeated digital interaction on functions that are not available in Cyclic Mode or certain system configuration changes.

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After power-on (reset) the ZSSC3286 always enters the Basic Device Initialization phase. In this phase the firmware is still in boot-up and command interpreter is not yet functional. Therefore write access and command execution is not supported. If Basic Device Initialization is successful, the ZSSC3286 enters bootloader operation mode.

Finally the ZSSC3286 will enter SIO mode. In SIO mode the programmed operation state is started (System Startup Mode set by CCP register *0x2E – StartupParamCfg*). The System Startup Mode can be configured via GUI path: Configure\System Control\System Startup.

Changing the ZSSC3286 to another operation mode or operating state is possible via the start commands START_CM and START_CYC (see section 10.7 for details).

The ZSSC3286 supports three different types of digital interfaces: IO-Link, I2C, and OWI while OWI is only used to control the IO-Link physical layer transceiver.

4.2 System Clocks

4.2.1 Main Internal Oscillators and Specifications

The ZSSC3286 is equipped with the following internal oscillators:

- Calibrated, first order temperature compensated 16MHz system clock oscillator
- Un-calibrated, first order temperature compensated 32kHz ultra low power oscillator

4.2.2 Main System Clock

The Main System Clock, which drives the ARM MCU, the memories (ROM, Flash, SRAM), and the peripherals is derived from the internal System Clock Oscillator. By default, the oscillator frequency (16MHz) is directly applied across the entire system without further down division. Hardware and software driven clock gating are applied to maintain a low power consumption.

4.2.3 Always-On Clock

The 32kHz always-on clock is used by the System Management Unit to control the Basic Device Initialization (power-up sequence) of the ZSSC3286 device, as well as by the internal low speed timer.

4.3 System Reset

The ZSSC3286 resets at following scenarios:

- Power-On-Reset Brown out — Voltage at VDD or VDDD is below the specified limits (see Table 11)
- External reset — RESN pin of the ZSSC3286 is set to LOW.
- Command (via I2C) — Start Firmware Update command
- Command sequence (via IO-Link) — Unlock sequence

Table 18. VDDD Power-On-Reset Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{riseVDDD}$	Reset release voltage	VDDD level where reset is released	1.35		1.8	V
$V_{fallVDDD}$	Reset voltage	VDDD level where reset is generated	1.1		1.6	V
$V_{hysVDDD}$	Reset hysteresis voltage		50		500	mV

4.4 Flash Memory

The ZSSC3286's flash memory is derived into different subsections supporting different functions. Each function will have its own read and write access and additional access rights. Intention of FW password and CCP password is to protect changing the ZSSC3286's configuration that must not be changed in end application while allowing changes for example via Teach or Zero Adjustment feature.

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Table 19. Flash Memory Overview

Flash Section	Usage	Write Commands	Read Commands	Limitations
Bootloader	This section contains the bootloader and is intended for updates of firmware and CCP.	Writing to bootloader is not possible.	Reading is not possible.	Entering bootloader can be protected with firmware password as described in section 11.
Application Firmware	This section contains the firmware provided by Renesas. This firmware contains functionality described in this document.	Writing is possible via ISDUs + BLOB transfer as described in section 11.	Reading is not possible.	Updating firmware requires entering bootloader. Entering bootloader can be protected with firmware password as described in section 11.
Info Page	Info Page contains trim data from Renesas.	Writing is not possible.	Reading is possible via ISDUs (Hidden Command) and command 0x84 (Read device info page in burst)	Limitation of reading is given by the usage of the Hidden Command ISDUs.
Configuration and Calibration Page	The CCP holds configuration and calibration data. The CCP is separated into two sub pages: • CCP0 for storing sensor related adjustments for analog front end, calibration coefficients and so on. • CCP1 for storing IO-Link relevant data like SI Unit Scaling coefficients, Vendor Text, Product Text and so on.	Writing is possible via ISDUs (Hidden Command) + BLOB transfer and will write complete CCP. Writing procedure is described in section 12.	• Reading complete CCP is possible via ISDUs (Hidden Command). • Reading the CCP1 sub page is possible via dedicated ISDUs too.	Writing via IO-Link can be protected with CCP password as described in section 12. Since writing is performed via BLOB transfer in bootloader additional firmware password protects writing CCP.
Factory Reset Page	This section holds IO-Link backup data.	Writing is possible via ISDUs (Hidden Command) and command 0xC0 (Store Factory Settings).	Reading is possible via ISDU (System with System Command Back-to-box) and ISDU (System with System Command ApplicationReset)	The read and write access is defined by ISDU implementation and do not have additional protection mechanism. It is intended to use the parameter page within end application. ISDU handling is described in section 10.2.
Parameter Page	The parameter page contains configuration data accessible in end application while running data processing inside firmware in parallel.	Writing is possible via ISDUs.	Reading is possible via ISDUs.	The read and write access is defined by ISDU implementation and do not have additional protection mechanism. It is intended to use the parameter page within end application. ISDU handling is described in section 10.2.

Figure 7 shows access options for each memory section of the ZSSC3286.

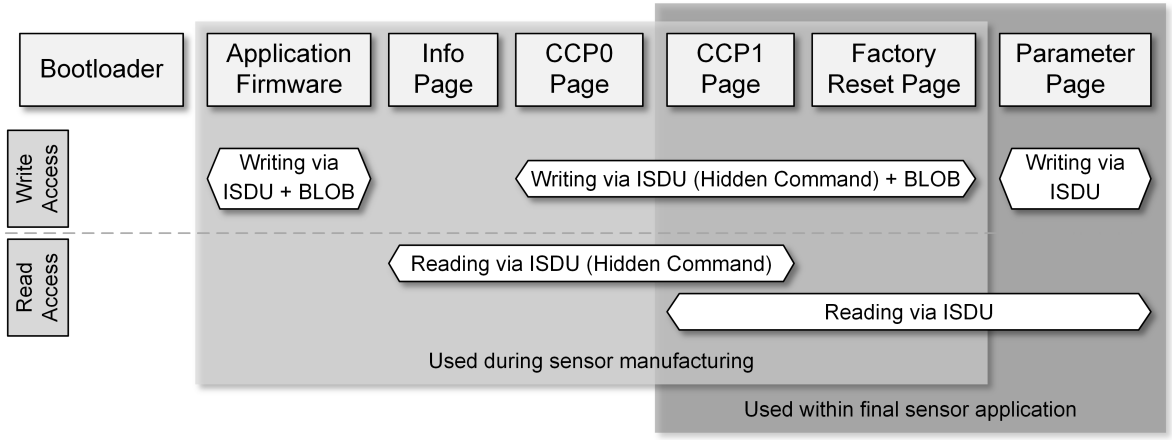

Figure 7. Overview for Access to Flash Memory

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5 Analog Front End (AFE)

The ZSSC3286 features two fully independent Analog Front Ends (AFEs), each capable of measuring both resistive and capacitive sensor elements.

5.1 AFE Signal Path

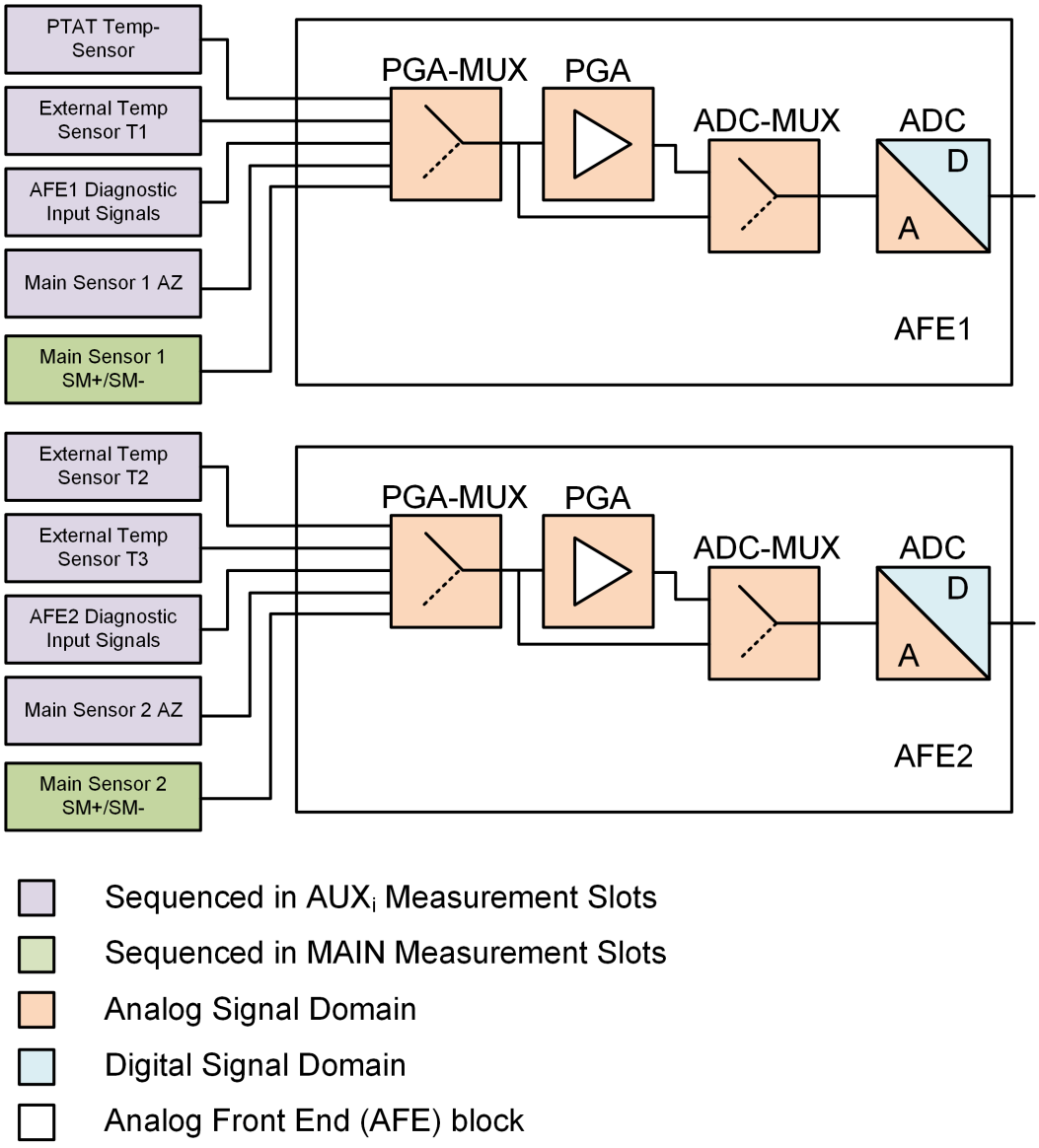

Figure 8. Block Diagram Analog Front End

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5.2 Resistive Bridge Sensors

Table 20. Resistive Bridge Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_{br}	Bridge resistor	Constant Voltage Mode	0.825		60	kΩ
		Constant Current Mode	0.1			
C_{br}	Bridge capacitance, depends on the required resolution: $\tau = R_{br} \times C_{br}$ defines the settle time.	Filter capacitance C_{br} between INNx/INPx and VSS		1		nF
V_{sig}	Signal span	mV/V is related to the bridge supply			500	mV/V
V_{off}	Signal offset	For example: V_{sig} = 1mV allows V_{off} = 20mV			2000	% off V_{sig}
					20	1/ V_{sig}

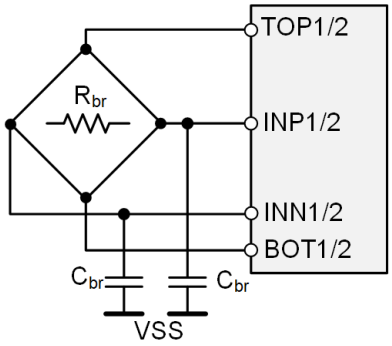

Figure 9. Bridge Sensor Type 1

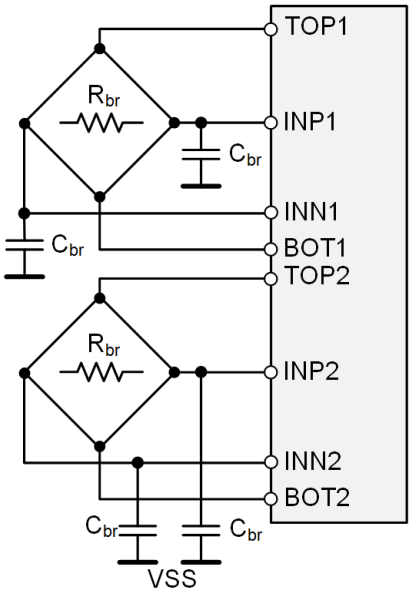

Figure 10. Bridge Sensor Type 2

In single bridge applications shown in Figure 9 the resistive bridge can be connected to either AFE1 or AFE2 depending on PCB layout requirements.

The resistive bridge can be sourced in either Constant Voltage mode (V-source) or in Constant Current mode (I-source).

Note: Constant Current mode requires a low bridge resistance for optimal performance.

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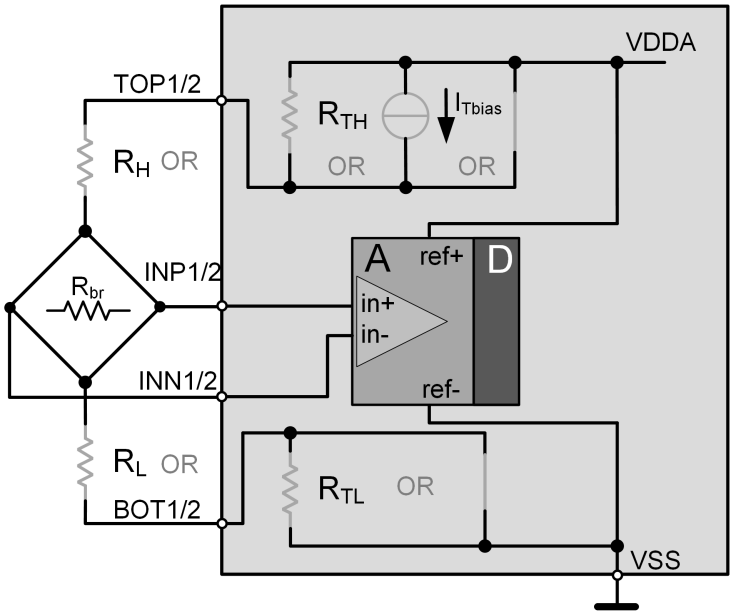

Legend:

Gray components: can be activated “either-or” via the GUI.

Figure 11. Resistive Bridge Bias Configurations

In Constant Current mode the bridge output must be set within the common input range of the PGA. This can be done with a low side external resistor R_L or with the internal resistor R_{TL}. The current that is supplied to the bridge must be adjusted to bridge resistance and this additional R_L or internal R_{TL} to meet the common input range of PGA. To align with the common input range of the PGA, adjust the R_L or the internal R_{TL} as needed.

In Constant Voltage mode the bridge current can be reduced by inserting the internal high and low side resistors R_{TH}, R_{TL} or by adding external resistors R_H and R_L.

Table 21. Resistive Bridge Supply Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{TOP1/2}$	Output voltage at TOP1/2			VDDA		V
I_{load}	Load current	In Constant Voltage mode defined by bridge resistance			2	mA
I_{Rbr_bias}	Current out of TOP1/2	In Constant Current mode adjustable via *BmBrdgIBias*	5		500	µA
C_{TOP_BOT}	Load capacitance				2.2	nF
R_{TH}, R_{TL}	Bias resistor		1.3		40	kΩ

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5.3 Capacitive Sensors

Note: External temperature sensor 2 is unavailable in capacitive mode, and external temperature sensor 3 is also unavailable when the shield driver for AFE2/CVC2 is enabled in specific operating modes.

Note: Prior using the capacitive front end, the device info page must be checked via command 0x84 (Read device info page in burst).
The capacitive front end shall only be used if info page register 0x11 is greater than 0. Reading is performed using command 0x84 with a data request (0x11 0x01), followed by a read request.

Table 22. Parameter Capacitive FE

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
C_{RES}	Result resolution		10		24	bit
$t_{C\_AOUT\ SR}$	Step response 2 * (AZs + SM + aux)	AFE speed, no shield driver, noise mode normal, temperature sensor ADC resolution ≤12bit capacitive sensor ADC resolution				ms
		12bit		1.04		
		14bit		1.85		
		16bit		3.48		
t_{C_CONV}	conversion time for AZS + SM + aux	normal AFE speed, no shield driver, noise mode normal, temperature sensor ADC resolution ≤12bit				ms
		12bit		0.54		
		14bit		0.94		
		16bit		1.75		
C_x, C_y, C_r	input parameter/capacitances	see CVC parameter Table 34				

Table 23. Capacitive Application Configurations

Mode	Application case	AFE1	AFE2	Comment
1	Single Ended / Fully Isolated	x		
2	Single Ended + External Reference / Fully Isolated	x		
3	Differential / Fully Isolated	x		
4	Single ended / Referred to Ground	x		
5	Single ended + External Reference / Referred to Ground	x	x	
6	Differential / Referred to Ground	x		
11	Differential $(C_x-C_y)/(C_x+C_y)$ / Referred to Ground	x	x	

Refer to section 5.7 for detailed descriptions of the different application modes.

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To optimize measurement performance, the following configuration options are available:

- Shield Driver: In ground-referenced systems, enabling the shield driver reduces stray capacitance and improves signal integrity (see Table 24).
- AFE Speed Reduction: Recommended for application modes 1 to 3 ensuring measurement accuracy depending on input capacitance (see Table 25 and Table 26).
- Noise Modes: Two selectable modes that influence sample rate, conversion time, and step response (see Table 28 to Table 33).

Note: These settings directly impact measurement accuracy and timing.

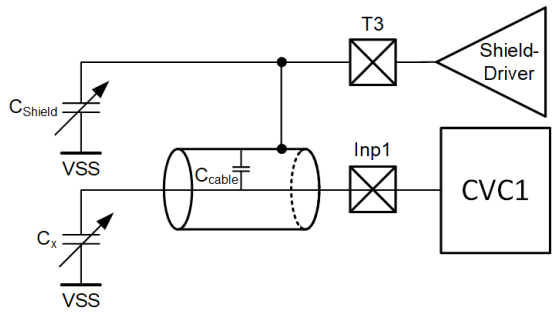

Figure 12. CVC Shield Driver Mode

Table 24. CVC Shield Mode

Mode	CmXEnShieldDrv	CmShieldDriver10nF
no shield driver	0	0
1nF driver mode	1	0
10nF driver mode	1	1

Table 25. Application Modes 1 to 3 AFE Speed Reduction

	Required AFE Speed Reduction	
C_x and C_y	<40 pF	<80 pF
Application Mode 1-3	2x	4x

Table 26. Application Modes 4 to 11 AFE Speed Reduction

	Required AFE Speed Reduction	
C_x and C_y	<50 pF	<100 pF
Application Mode 4-11, no shield driver	1x	2x
Application Mode 4-11, 1nF shield driver	4x	4x
Application Mode 4-11, 10nF shield driver	2x	4x

Note: AFE Speed Reduction value updates automatically when Max Input Cap changes in the GUI. Check the Override box in the GUI to enable manual adjustment.

Table 27. Noise Mode

CmNoiseMode
Normal
Low Noise

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Table 28. Performance Capacitive Front End, AFE Speed Reduction Factor = 1, Cm10nFShieldEn = 0

ADC res/bit	ADC clks	Normal	Low Noise	Normal	Low Noise	Normal	Low Noise	If C_{int}=20pF and 2x ADC Gain enabled
		Conversion Time/µs		Sample Rate/Hz		Step Response Time/ms		Resolution fF/LSB
10	64	301	1016	3322	984	0.60	2.03	19.53
11	91	404	1405	2475	712	0.80	2.80	9.77
12	128	535	1939	1869	516	1.04	3.85	4.88
13	182	706	2695	1416	371	1.39	5.36	2.44
14	256	936	3731	1068	268	1.85	7.44	1.22
15	364	1278	5243	782	191	2.53	10.46	0.61
16	512	1751	7315	571	137	3.48	14.60	0.31
17	728	2435	10339	411	97	4.84	20.65	0.15
18	1024	3368	14483	297	69	6.71	28.94	0.0763
19	1456	4736	20531	211	49	9.45	41.04	0.0381
20	2048	6615	28819	151	35	13.20	57.61	0.0191
21	2912	9351	40915	107	24	18.68	81.80	0.0095
22	4096	13096	57491	76	17	26.17	114.96	0.0048
23	5824	18568	81683	54	12	37.11	163.34	0.0024
24	8192	26071	114835	38	9	52.12	229.64	0.0012

Table 29. Performance Capacitive Front End, AFE Speed Reduction Factor = 1, Cm10nFShieldEn = 1

ADC res/bit	ADC clks	Normal	Low Noise	Normal	Low Noise	Normal	Low Noise	If C_{int}=20pF and 2x ADC Gain enabled
		Conversion Time/µs		Sample Rate/Hz		Step Response Time/ms		Resolution fF/LSB
10	64	521	2336	1919	428	1.04	4.67	19.53
11	91	724	3265	1381	306	1.44	6.52	9.77
12	128	975	4539	1026	220	1.92	9.05	4.88
13	182	1326	6375	754	157	2.63	12.72	2.44
14	256	1796	8891	557	112	3.57	17.76	1.22
15	364	2498	12563	400	80	4.97	25.10	0.61
16	512	3471	17595	288	57	6.92	35.16	0.31
17	728	4875	24939	205	40	9.72	49.85	0.15
18	1024	6788	35003	147	29	13.55	69.98	0.0763
19	1456	9596	49691	104	20	19.17	99.36	0.0381
20	2048	13455	69819	74	14	26.88	139.61	0.0191
21	2912	19071	99195	52	10	38.12	198.36	0.0095
22	4096	26756	139451	37	7	53.49	278.88	0.0048
23	5824	37988	198203	26	5	75.95	396.38	0.0024
24	8192	53391	278715	19	4	106.76	557.40	0.0012

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Table 30. Performance Capacitive Front End, AFE Speed Reduction Factor = 2, Cm10nFShieldEn = 0

ADC res/bit	ADC clks	Normal	Low Noise	Normal	Low Noise	Normal	Low Noise	If C_{int}=20pF and 2x ADC Gain enabled
		Conversion Time/µs		Sample Rate/Hz		Step Response Time/ms		Resolution fF/LSB
10	64	602	2032	1661	492	1.14	4.00	19.53
11	91	808	2810	1238	356	1.53	5.53	9.77
12	128	1070	3878	935	258	2.02	7.63	4.88
13	182	1412	5390	708	186	2.70	10.66	2.44
14	256	1872	7462	534	134	3.62	14.80	1.22
15	364	2556	10486	391	95	4.99	20.85	0.61
16	512	3502	14630	286	68	6.88	29.14	0.31
17	728	4870	20678	205	48	9.62	41.23	0.15
18	1024	6736	28966	148	35	13.35	57.81	0.0763
19	1456	9472	41062	106	24	18.82	82.00	0.0381
20	2048	13230	57638	76	17	26.34	115.15	0.0191
21	2912	18702	81830	53	12	37.28	163.54	0.0095
22	4096	26192	114982	38	9	52.26	229.84	0.0048
23	5824	37136	163366	27	6	74.15	326.61	0.0024
24	8192	52142	229670	19	4	104.16	459.22	0.0012

Table 31. Performance Capacitive Front End, AFE Speed Reduction Factor = 2, Cm10nFShieldEn = 1

ADC res/bit	ADC clks	Normal	Low Noise	Normal	Low Noise	Normal	Low Noise	If C_{int}=20pF and 2x ADC Gain enabled
		Conversion Time/µs		Sample Rate/Hz		Step Response Time/ms		Resolution fF/LSB
10	64	1042	4672	960	214	2.02	9.28	19.53
11	91	1448	6530	691	153	2.81	12.97	9.77
12	128	1950	9078	513	110	3.78	18.03	4.88
13	182	2652	12750	377	78	5.18	25.38	2.44
14	256	3592	17782	278	56	7.06	35.44	1.22
15	364	4996	25126	200	40	9.87	50.13	0.61
16	512	6942	35190	144	28	13.76	70.26	0.31
17	728	9750	49878	103	20	19.38	99.63	0.15
18	1024	13576	70006	74	14	27.03	139.89	0.0763
19	1456	19192	99382	52	10	38.26	198.64	0.0381
20	2048	26910	139638	37	7	53.70	279.15	0.0191
21	2912	38142	198390	26	5	76.16	396.66	0.0095
22	4096	53512	278902	19	4	106.90	557.68	0.0048
23	5824	75976	396406	13	3	151.83	792.69	0.0024
24	8192	106782	557430	9	2	213.44	1114.74	0.0012

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Table 32. Performance Capacitive Front End, AFE Speed Reduction Factor = 4, Cm10nFShieldEn = 0

ADC res/bit	ADC clks	Normal	Low Noise	Normal	Low Noise	Normal	Low Noise	If C_{int}=20pF and 2x ADC Gain enabled
		Conversion Time/µs		Sample Rate/Hz		Step Response Time/ms		Resolution fF/LSB
10	64	1204	4064	831	246	2.20	7.92	19.53
11	91	1616	5620	619	178	2.98	10.99	9.77
12	128	2140	7756	467	129	3.96	15.20	4.88
13	182	2824	10780	354	93	5.33	21.24	2.44
14	256	3744	14924	267	67	7.17	29.53	1.22
15	364	5112	20972	196	48	9.91	41.63	0.61
16	512	7004	29260	143	34	13.69	58.20	0.31
17	728	9740	41356	103	24	19.16	82.40	0.15
18	1024	13472	57932	74	17	26.63	115.55	0.0763
19	1456	18944	82124	53	12	37.57	163.93	0.0381
20	2048	26460	115276	38	9	52.60	230.24	0.0191
21	2912	37404	163660	27	6	74.49	327.00	0.0095
22	4096	52384	229964	19	4	104.45	459.61	0.0048
23	5824	74272	326732	13	3	148.23	653.15	0.0024
24	8192	104284	459340	10	2	208.25	918.36	0.0012

Table 33. Performance Capacitive Front End, AFE Speed Reduction Factor = 4, Cm10nFShieldEn = 1

ADC res/bit	ADC clks	Normal	Low Noise	Normal	Low Noise	Normal	Low Noise	If C_{int}=20pF and 2x ADC Gain enabled
		Conversion Time/µs		Sample Rate/Hz		Step Response Time/ms		Resolution fF/LSB
10	64	2084	9344	480	107	3.96	18.48	19.53
11	91	2896	13060	345	77	5.54	25.87	9.77
12	128	3900	18156	256	55	7.48	36.00	4.88
13	182	5304	25500	189	39	10.29	50.68	2.44
14	256	7184	35564	139	28	14.05	70.81	1.22
15	364	9992	50252	100	20	19.67	100.19	0.61
16	512	13884	70380	72	14	27.45	140.44	0.31
17	728	19500	99756	51	10	38.68	199.20	0.15
18	1024	27152	140012	37	7	53.99	279.71	0.0763
19	1456	38384	198764	26	5	76.45	397.21	0.0381
20	2048	53820	279276	19	4	107.32	558.24	0.0191
21	2912	76284	396780	13	3	152.25	793.24	0.0095
22	4096	107024	557804	9	2	213.73	1115.29	0.0048
23	5824	151952	792812	7	1	303.59	1585.31	0.0024
24	8192	213564	1114860	5	1	426.81	2229.40	0.0012

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Table 34. Parameter CVC

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
C_{shift}	Internal shift capacitance	Programmable in 31 steps, step size 2pF	0		62	pF
C_{int}	Internal reference capacitance	Programmable in 31 steps, step size 2pF	20		82	pF
C_{offset}	Compensate-able absolute sensor offset	For single ended input, single cap. C_x		C_{shift}		
ERR_{rel} C_{int}	Measurement error C_{int}	Application Mode 1, 2, 3, 4, 5, 6 and 11	-1		1	%
ERR_{rel} C_{shift}	Measurement error C_{shift}	Application Mode 1, 2, 4, 5 and 11	-1		1	%
		Application Mode 3 and 6 C_{shift} is effectively not trimmed	-15		15	
C_{shield}	Capacitive load at shield driver to GND	Driver mode 1nF	0.05		1	nF
		Driver mode 10nF	1		10	
C_{cable}	Capacitance between shield and C_x, C_r (cable capacitance) see also Table 24				500	pF

5.4 Auxiliary Temperature Sensor Inputs

5.4.1 Internal PTAT Temperature Sensor

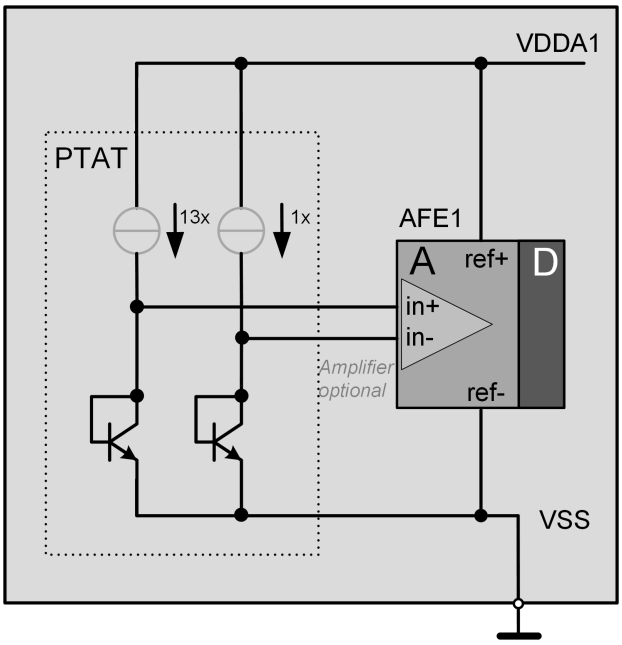

Figure 13. PTAT Sensor Configuration

Table 35. Internal PTAT Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
T_{meas}	Measurement range		-55		125	°C
E_T	Measurement error	Calibrated	-5		5	K
ADC_{res}	Resolution	Programmable ADC resolution	10		15	bit
T_{res}	Effective resolution	±1.5sigma	2			LSB/°C
S	Sensitivity	Differential output voltage	218		230	µV/K

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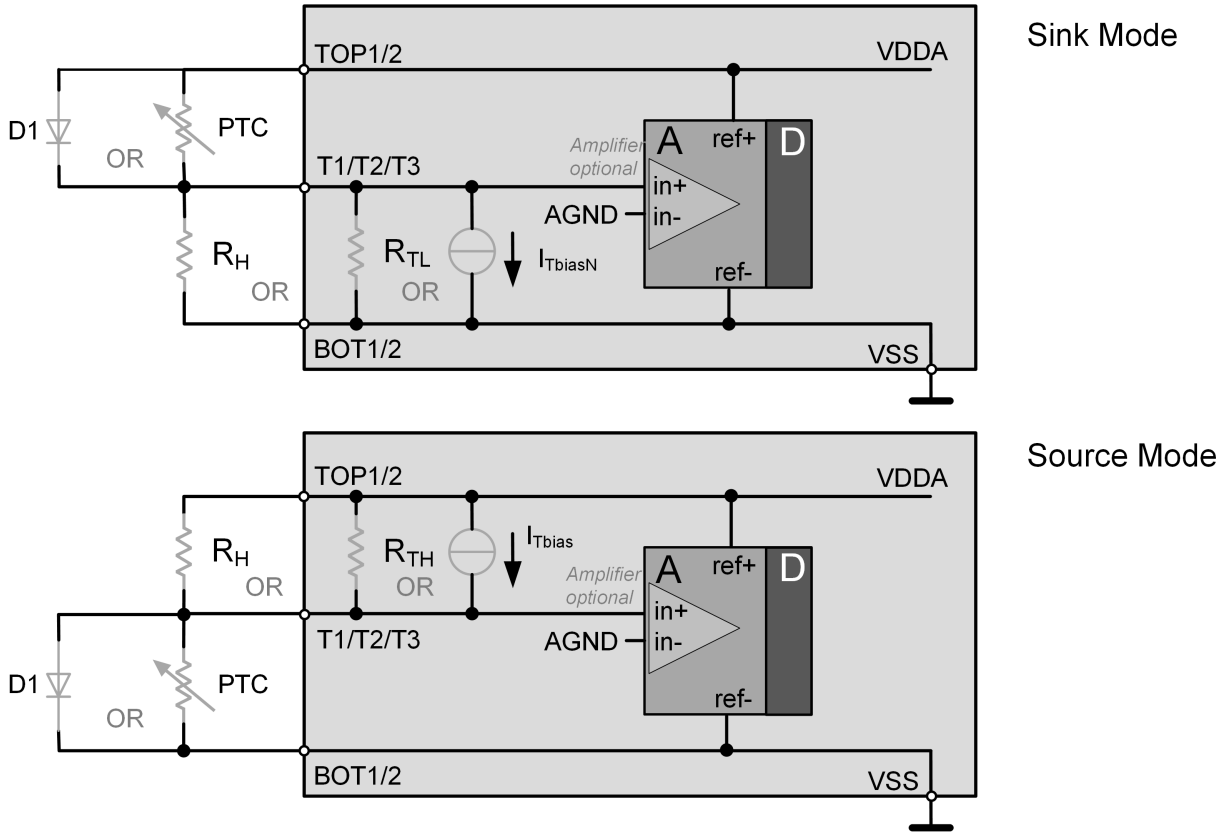
5.4.2 External Temperature Sensors

Three different external sensor types can be used to measure the temperature of the main sensor or a media temperature in the auxiliary signal path of the AFEs:

- PTC
- Diode
- TC Bridge Sensor

The PTC and Diode Sensors can be supplied either in Sink Mode or in Source Mode as shown in Figure 14. The gray marked components can be activated “either-or” via the GUI. The AGND potential is at VDDA/2.



Legend:

Gray components: can be activated “either-or” via the GUI. The AGND potential is at VDDA/2.

Figure 14. PTC, Diode Sensor Bias Configurations

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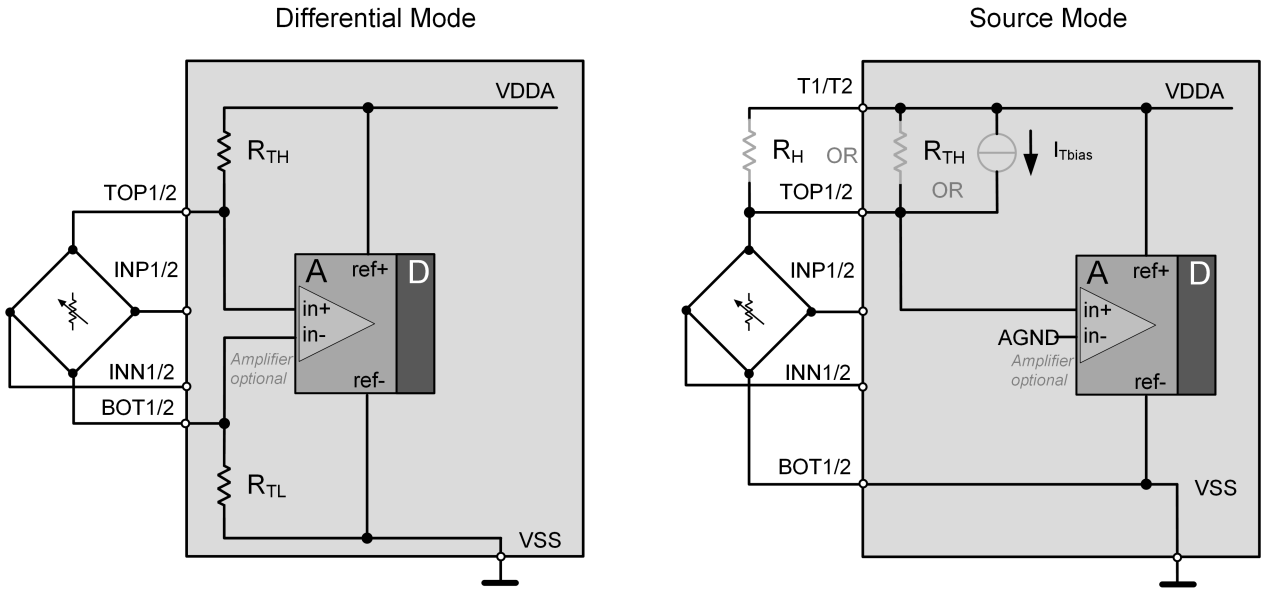
TC Bridge Sensor configurations can be supplied in Differential Mode or Source Mode as shown in Figure 15.



Legend:

Gray components: can be activated “either-or” via the GUI. The AGND potential is at VDDA/2.

Figure 15. TC Bridge Sensor Bias Configurations

Table 36. External Temperature Sensor Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
R_{sensor}	Sensor resistance (PTC/TC Bridge Sensor)		50		1M	Ω
ADC_{res}	ADC resolution	Programmable ADC resolution	10		15	bit
ENOB	Effective resolution	±1.5sigma	14			bit

5.5 Programmable Gain Amplifier (PGA)

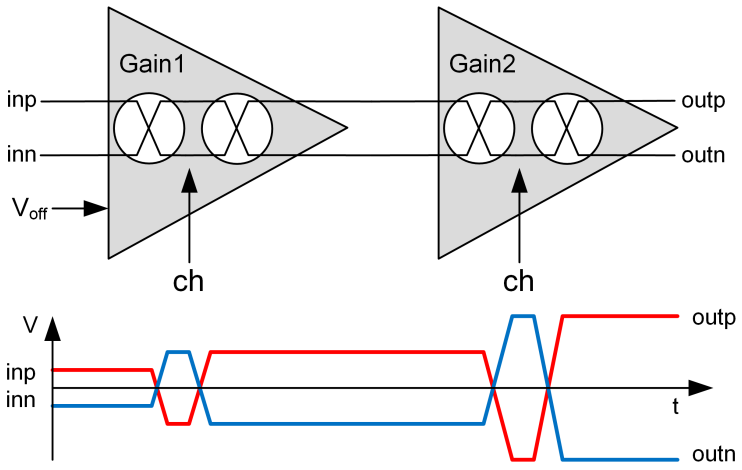


Figure 16. PGA Architecture

The first amplifier (Gain1) has a built in PGA offset compensation (auto-zero) that is refreshed at the beginning of every measurement. The second stage has no offset compensation. The second stage amplifier offset is present at the PGA output with offset × Gain2. Both PGA amplifier stages have built-in chopper functionality to suppress 1/f noise.

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The gain settings that can be selectively programmed for both PGA stages are listed in Table 37.

Table 37. PGA Gain Steps

Gain1	Gain2
1.2	1.1
2	1.2
4	1.3
5.97	1.4
11.9	1.5
19.8	1.6
29.6	1.7
39.2	1.8
58.1	
76.6	
112	
143	
187	
223	
275	

If bridge sensors show noticeable DC offsets (that is offset from 0) in their differential output voltage, it restricts the maximum PGA gain that can be applied without causing saturation. To compensate this, the PGA can be programmed to shift the input signal by an offset voltage, as shown in the Figure 17. The default shift is 0mV, and the offset can be adjusted in 15 steps in both positive and negative directions, see Table 37 and Table 38. This PGA offset shift function is available only for PGA Gain values of 11.9 or higher.

Table 38. PGA Input Offset Compensation Steps

11.9 ≤ Gain1 ≤ 223 [mV]	Gain1 = 275 [mV]
0	0
±1.9	±1.5
±3.8	±3
±5.6	±4.5
±7.5	±6
±9.4	±7.5
±11.3	±9
±13.1	±10.5
±15	±12
±16.9	±13.5
±18.8	±15
±20.6	±16.5
±22.5	±18
±24.4	±19.5
±26.3	±21
±28.1	±22.5

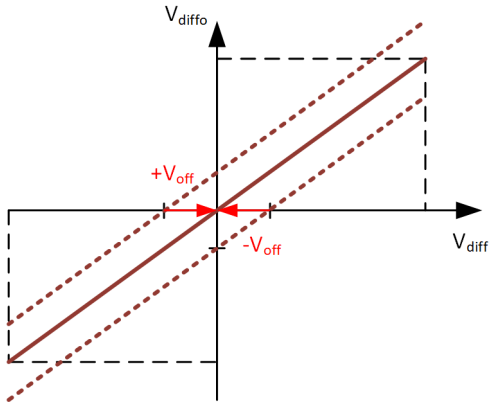

Figure 17. PGA Input Offset Compensation

PGA gain and the Input Offset Compensation value can be programmed separately for the two main bridge sensors and for the three external auxiliary temperature sensors that can be connected to the ZSSC3286. The PGA Input Offset Compensation feature is limited to SM+/SM- and SM+ sequencer configurations which are described in section 5.8.

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Table 39. PGA Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
Gain	Total PGA gain	Programmable in 15/8 steps: • stage1: 15 steps, 1.2 to 275 • stage2: 8 steps, 1.1 to 1.8	1.32		495	V/V
V_{cmi}	Input Common Mode voltage			VDDA/2		V
BW_{PGA}	Bandwidth			5		kHz
t_{az_PGA}	Auto-zero time		10			µs
f_{ch_PGA}	Chopper frequency			100		kHz

5.6 Analog-to-Digital Converter (ADC)

An incremental delta-sigma analog-to-digital converter (ADC) is used to digitize the PGA signal. To allow optimizing the trade-off between conversion time and resolution, the resolution can be programmed from 10-bit to 24-bit. The ADC processes differential input signals around its input Common Mode level VDDA/2. Table 40 lists the ADC resolution, signal ranges and conversion times for a single analog-to-digital conversion at VDDA = 1.65V.

Table 40. ADC Configuration Parameters

ADC Resolution [Bits]	Full Scale Input Voltage Vfs [V]	LSB Size VLSB [µV]	Conversion Time, Typical, TConv [µs]
10	±1.418	2768.638	32.54
11	±1.425	1391.718	43.75
12	±1.431	698.499	59.59
13	±1.434	350.189	81.99
14	±1.437	175.428	113.68
15	±1.439	87.832	158.49
16	±1.440	43.958	221.86
17	±1.441	21.994	311.48
18	±1.442	11.002	438.22
19	±1.443	5.503	617.46
20	±1.443	2.752	870.94
21	±1.443	1.376	1229.41
22	±1.443	0.688	1736.38
23	±1.443	0.344	2453.33
24	±1.444	0.172	3467.25

The ADC can perform an additional offset shift (independent of the PGA shifting) to adapt input signals with offsets to the ADC input range. Enabling the offset shift causes the ADC to perform an additional amplification of the ADC's input signal by factor ×2. This must be considered for a correct PGA configuration setup.

The ADC offset shift feature is limited to SM+/SM- and SM+ sequencer configurations which are described in section 5.8.

The shift values in Table 41 are related to the input voltages at INP, INN:

- Full scale differential input voltage: $V_{INdiff\_fs} = \frac{V_{fs}}{Gain}$
- Differential input shift voltage: V_{INdiff_shift}
- Maximum, minimum differential input voltage: V_{INdiff_max} , V_{INdiff_min}

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Table 41. ADC Input Offset Shift Steps

PGA Polarity	ADC Shift Enable	ADC Gain	ADC Shift	V_{INdiff_shift}/ V_{INdiff_fs}	V_{INdiff_min}/ V_{INdiff_fs}	V_{INdiff_max}/ V_{INdiff_fs}
Positive	0	x1	0	No shift	-1	+1
Negative			0	No shift	+1	-1
Positive	1	×2	1	7/8	-1/16	+15/16
			2	6/8	-2/16	+14/16
			3	5/8	-3/16	+13/16
			4	4/8	-4/16	+12/16
			5	3/8	-5/16	+11/16
			6	2/8	-6/16	+10/16
			7	1/8	-7/16	+9/16
			0	No shift	-1/2	+1/2
Negative			0	No shift	+1/2	-1/2
			1	1/8	-9/16	+7/16
			2	2/8	-10/16	+6/16
			3	3/8	-11/16	+5/16
			4	4/8	-12/16	+4/16
			5	5/8	-13/16	+3/16
			6	6/8	-14/16	+2/16
			7	7/8	-15/16	+1/16

5.7 Capacitive Sensors - CVC Mode

5.7.1 Capacitive Application Mode 1: Single Ended / Fully Isolated

In Capacitive Application Mode 1, a fully isolated, single-ended measurement of a single capacitive cell is performed.

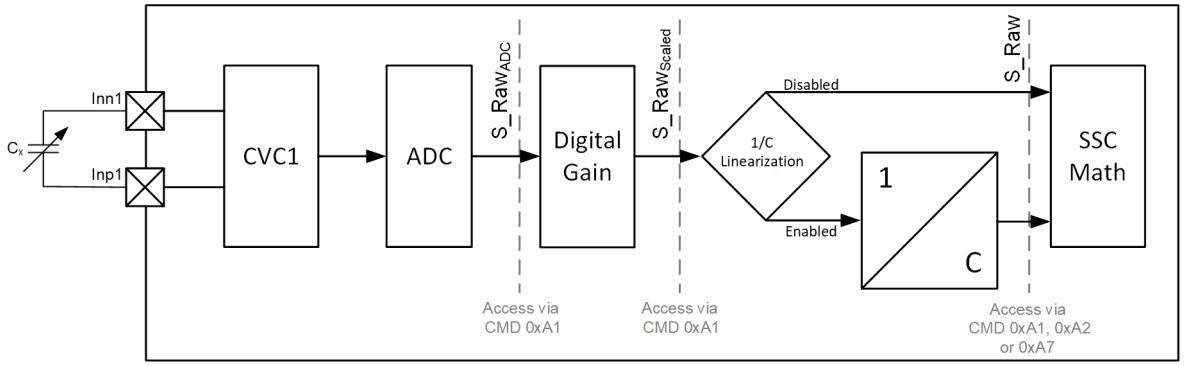

Figure 18. Capacitive Application Mode 1

The Capacitance-to-Voltage Converter (CVC) establishes a ratio between the measured capacitance C_x and an internally selected reference capacitance C_{int}, as shown in Equation 1. Before signal integration, an offset correction can be applied using a capacitance shift value C_{shift}. The adjusted signal is then passed to the ADC for digitization.

$$CVC1 = \frac{(C_x - C_{shift})}{C_{int}} \quad (1)$$

The ADC output is scaled according Equation 2 to amplify low-level input signals. Signal inversion is then applied (Equation 3) to produce a linearized output that corresponds directly to the physical sensor input (for example pressure).

$$S\_Raw_{\text{Scaled}} = CVC1 \times ADC_{Gain} \times Dig_{Gain} \quad (2)$$

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When 1/C linearization is enabled, the physical signal range must be adjusted using a range shift value RValue (Equation 4). This compensation accounts for external stray capacitances C_{stray} introduced during sensor module assembly. Accurate characterization of C_{stray} is critical for effective 1/C linearization.

$$S\_Raw = \begin{cases} \text{1/C Linearization Enabled,} & \frac{1-RValue^2}{S\_Raw_{Scaled}+RValue} + RValue \\ \text{1/C Linearization Disabled,} & S\_Raw_{Scaled} \end{cases} \quad (3)$$

$$RValue = \frac{C_{shift} - C_{stray}}{C_{int}} \times ADC_{Gain} \times Dig_{Gain} \quad (4)$$

		Valid Input Range
CVC1	Capacitance-to-Voltage Converter 1	
S_Raw	Raw sensor reading from ADC	-(0x7FFFFF) to 0x7FFFFF
S_Raw$_{Scaled}$	Raw sensor reading from ADC scaled	-(0x7FFFFF) to 0x7FFFFF
C_{int}	*Cm1Config.CmCapInt* set integration capacity (Step size 2pF)	20pF to 82pF
C_{shift}	*Cm1Config.CmCapShift* set shift capacity (Step size 2pF)	0pF to 62pF
ADC$_{Gain}$	*Cm1Config.CmAdcEnShift* enables selection of value	1 to 2
Dig$_{Gain}$	*MathSbrAlgoSel.DigGain1* applies an digital gain (Step size 0.25)	1 to 8
RValue	*CsInvParam.RValue* Range Shift Value, Only available when 1/C Linearization is enabled	0 to 30

Table 42. Data Format of S_Raw and S_Raw$_{Scaled}$

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	-2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 43. Data Format of RValue

Bit Number	23	22	21	...	18	17	16	...	0
Meaning, Weighting	0 = positive 1 = negative	2^4	2^3	...	2^0	2^{-1}	2^{-2}	...	2^{-18}

5.7.2 Capacitive Application Mode 2: Single Ended + External Reference / Fully Isolated

In Capacitive Application Mode 2, a single-ended measurement is performed using an external reference capacitance C_r.

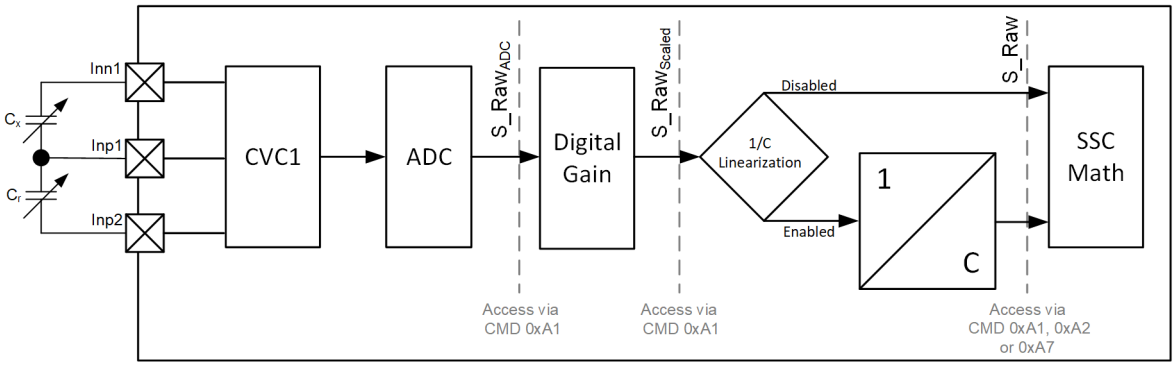

Figure 19. Capacitive Application Mode 2

The CVC calculates the ratio between the measured capacitance C_x and the external reference C_r, as shown in Equation 5. Before the quantitative relation between C_x / C_r is measured, a capacitance shift C_{shift} can be applied to minimize the offset in the measurement signal. The adjusted signal is forwarded to the ADC for digitization.

$$CVC1 = CVC_{out} = \frac{C_x - C_{shift}}{C_r} \quad (5)$$

The digitized output is scaled according to Equation 6, enabling effective use of low input signal levels. Optional signal inversion can be applied, as shown in Equation 7, resulting in a linear output that accurately reflects changes in the physical input quantity.

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$$S\_Raw_{Scaled} = CVC1 \times ADC_{Gain} \times Dig_{Gain} \quad (6)$$

If 1/C linearization is enabled, the signal inversion must also be applied to the physical signal range. This requires shifting the scaled signal S_Raw_{Scaled} by a range shift value R, as defined in Equation 8. The range shift value RValue accounts for the external stray capacitances C_{stray}, which are introduced during sensor module assembly. Accurate consideration of C_{stray} significantly enhances the effectiveness of the 1/C linearization.

$$S\_Raw = \begin{cases} \text{1/C Linearization Enabled,} & \frac{1-RValue^2}{S\_Raw_{Scaled}+RValue} + RValue \\ \text{1/C Linearization Disabled,} & S\_Raw_{Scaled} \end{cases} \quad (7)$$

$$RValue = \frac{C_{shift} - C_{stray}}{mean(C_r)} \times ADC_{Gain} \times Dig_{Gain} \quad (8)$$

		Valid Input Range
CVC1	Capacitance-to-Voltage Converter 1	
S_Raw	Raw sensor reading from ADC	-(0x7FFFFF) to 0x7FFFFF
S_Raw_{Scaled}	Raw sensor reading from ADC scaled	-(0x7FFFFF) to 0x7FFFFF
C_{shift}	*Cm1Config.CmCapShift* set shift capacity (Step size 2pF)	0pF to 62pF
ADC_{Gain}	*Cm1Config.CmAdcEnShift* enables selection of value	1 to 2
Dig_{Gain}	*MathSbrAlgoSel.DigGain1* applies an digital gain (Step size 0.25)	1 to 8

Table 44. Data Format of S_Raw and S_Raw_{Scaled}

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	-2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

5.7.3 Capacitive Application Mode 3: Differential / Fully Isolated

In Capacitive Application Mode 3, a differential measurement of two isolated capacitive sensors (C_x and C_y) is performed.

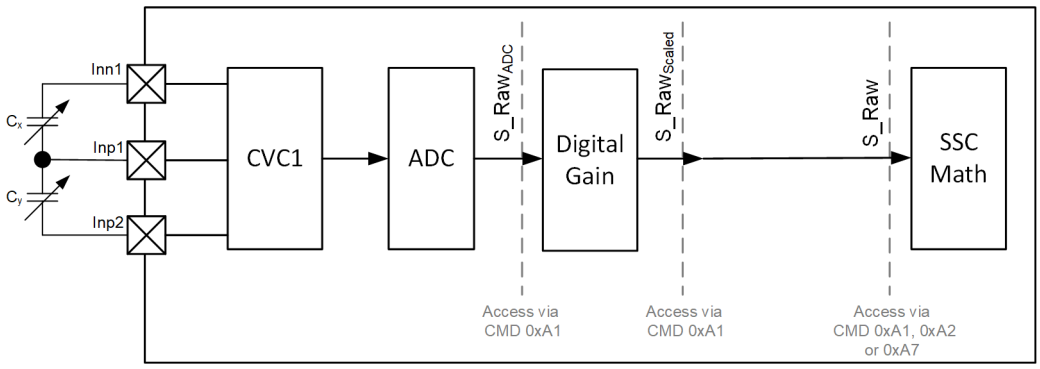

Figure 20. Capacitive Application Mode 3

The CVC calculates the difference between C_x, C_y, and the reference C_{int}, as shown in Equation 9. Before the reference capacitor integrates the signal, a capacitance shift C_{shift} can be applied to reduce offset in the measurement. The adjusted signal is forwarded to the ADC for digitization.

Note: For optimal operation, C_x should be greater than C_y. If no pressure is applied and this is not the case, swap the sensor connections.

$$CVC1 = \frac{C_x - C_y - C_{shift}}{C_{int}} \quad (9)$$

The resulting signal is scaled using Equation 10, effectively amplifying the measurement so that low input signal spans can be utilized.

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$$S\_Raw = S\_Raw_{Scaled} = (CVC1 \times ADC_{Gain} - \frac{AdcShift}{8}) \times Dig_{Gain} \quad (10)$$

		Valid Input Range
CVC1	Capacitance-to-Voltage Converter 1	
S_Raw	Raw sensor reading from ADC	-(0x7FFFFF) to 0x7FFFFF
S_Raw_{Scaled}	Raw sensor reading from ADC scaled	-(0x7FFFFF) to 0x7FFFFF
C_{int}	*Cm1Config.CmCapInt* set integration capacity (Step size 2pF)	20pF to 82pF
C_{shift}	*Cm1Config.CmCapShift* set shift capacity (Step size 2pF)	0pF to 62pF
ADC_{Gain}	*Cm1Config.CmAdcEnShift* enables selection of value	1 to 2
ADC Shift	*Cm1Config.CmAdcShift* enables selection of value (Step size 0.125)	0 to 0.875
Dig_{Gain}	*MathSbrAlgoSel.DigGain1* applies an digital gain (Step size 0.25)	1 to 8
RValue	*CsInvParam.RValue* Range Shift Value, Only available when 1/C Linearization is enabled	0 to 30

Table 45. Data Format of S_Raw and S_Raw_{Scaled}

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	-2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 46. Data Format of RValue

Bit Number	23	22	21	...	18	17	16	...	0
Meaning, Weighting	0 = positive 1 = negative	2^4	2^3	...	2^0	2^{-1}	2^{-2}	...	2^{-18}

5.7.4 Capacitive Application Mode 4: Single ended / Referred to Ground

In Capacitive Application Mode 4, a single-ended measurement is performed on a capacitive sensor C_x that is connected to ground.

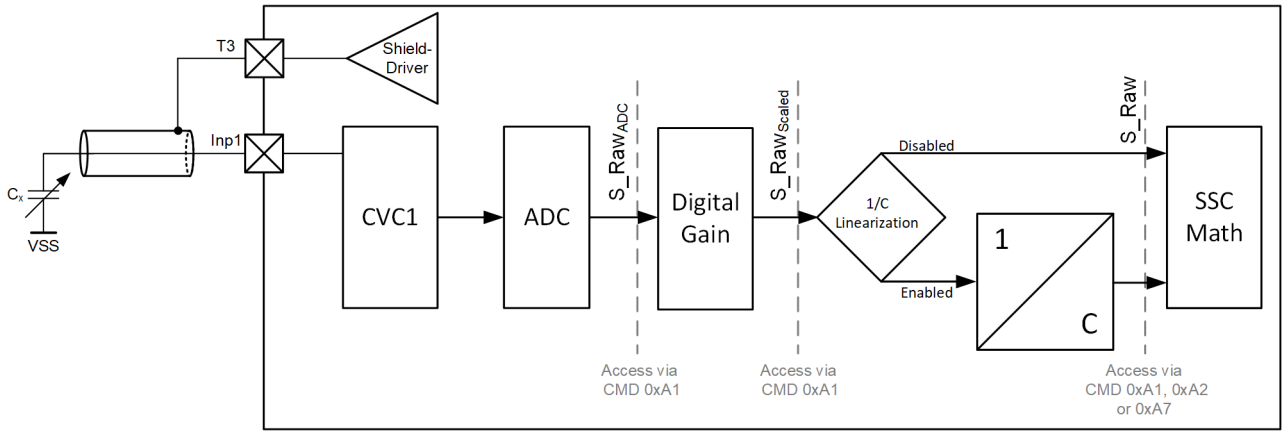

Figure 21. Capacitive Application Mode 4

The capacitance-to-voltage converter (CVC) calculates the ratio between C_x and an internally selected reference capacitance C_{int}, as shown in Equation 11. Before the reference capacitor integrates the signal, a capacitance shift C_{shift} can be applied to reduce offset in the measurement. The adjusted signal is forwarded to the ADC for digitization.

$$CVC1 = \frac{C_x - C_{shift}}{C_{int}} \quad (11)$$

The signal from the ADC is scaled according to Equation 2, effectively amplifying the measurement so that low input signal spans can be utilized. Afterward, signal inversion is applied, as shown in Equation 3, resulting in a linear output that accurately reflects changes in the physical input quantity.

$$S\_Raw_{Scaled} = CVC1 \times ADC_{Gain} \times Dig_{Gain} \quad (12)$$

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If 1/C linearization is enabled, the signal inversion must also be applied to the physical signal range. This requires shifting the scaled signal S_Raw_{Scaled} by a range shift value R, as defined in Equation 14. The range shift value RValue accounts for the external stray capacitances C_{stray}, which are introduced during sensor module assembly. Accurate consideration of C_{stray} significantly enhances the effectiveness of the 1/C linearization.

$$S\_Raw = \begin{cases} \text{1/C Linearization Enabled,} & \frac{1-RValue^2}{S\_Raw_{Scaled}+RValue} + RValue \\ \text{1/C Linearization Disabled,} & S\_Raw_{Scaled} \end{cases} \quad (13)$$

$$RValue = \frac{C_{shift} - C_{stray}}{C_{int}} \times ADC_{Gain} \times Dig_{Gain} \quad (14)$$

		Valid Input Range
CVC1	Capacitance-to-Voltage Converter 1	
S_Raw	Raw sensor reading from ADC	-(0x7FFFFF) to 0x7FFFFF
S_Raw_{Scaled}	Raw sensor reading from ADC scaled	-(0x7FFFFF) to 0x7FFFFF
C_{int}	*Cm1Config.CmCapInt* set integration capacity (Step size 2pF)	20pF to 82pF
C_{shift}	*Cm1Config.CmCapShift* set shift capacity (Step size 2pF)	0pF to 62pF
ADC_{Gain}	*Cm1Config.CmAdcEnShift* enables selection of value	1 to 2
Dig_{Gain}	*MathSbrAlgoSel.DigGain1* applies an digital gain (Step size 0.25)	1 to 8
RValue	*CsInvParam.RValue* Range Shift Value, Only available when 1/C Linearization is enabled	0 to 30

Table 47. Data Format of S_Raw and S_Raw_{Scaled}

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	-2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 48. Data Format of RValue

Bit Number	23	22	21	...	18	17	16	...	0
Meaning, Weighting	0 = positive 1 = negative	2^4	2^3	...	2^0	2^{-1}	2^{-2}	...	2^{-18}

5.7.5 Capacitive Application Mode 5: Single ended + External Reference / Referred to Ground

In Capacitive Application Mode 5, a single-ended measurement is performed using an external reference capacitor C_r, with both measurement and reference nodes connected to ground.

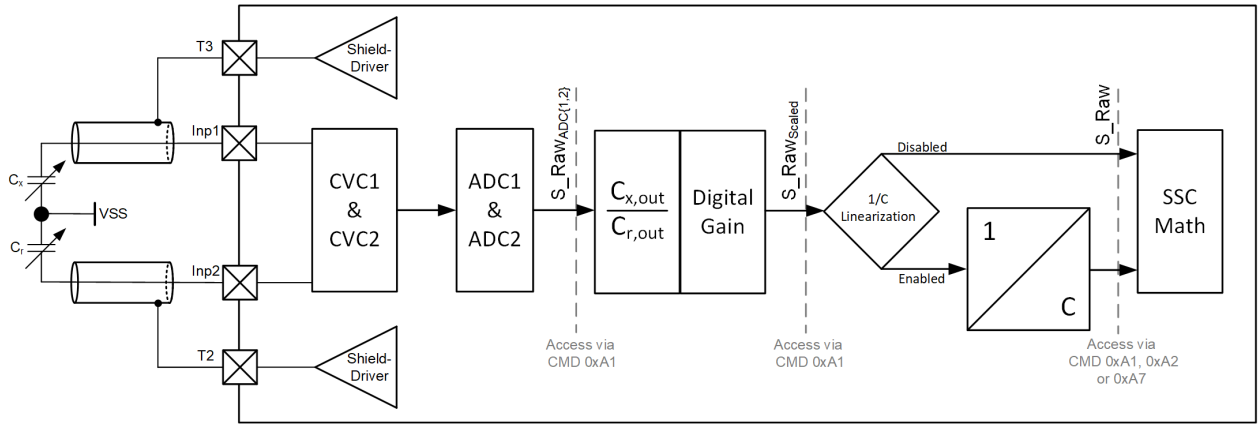

Figure 22. Capacitive Application Mode 5

The capacitance-to-voltage converter (CVC) establishes a ratio between the measured capacitance C_x and reference capacitance C_{int}, as shown in Equation 15, also a ratio between the measured capacitance C_r and an internally selected reference capacitance C_{int}, as shown in Equation 16. Before the reference capacitor integrates the signals, a capacitance shift C_{shift} can be applied to reduce offset in the measurement. The adjusted signal is then forwarded to the ADC for digitization.

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$$CVC1 = \frac{C_x - C_{shift}}{C_{int}} \tag{15}$$

$$CVC2 = \frac{C_r - C_{shift}}{C_{int}} \tag{16}$$

Note: C_{int} and C_{shift} have the same value for both measurements.

The analog signals can be increased in the ADC as shown in Equation 17 and Equation 18, effectively amplifying the measurement so that low input signal spans can be utilized.

$$S\_raw_{Adc1} = CVC1 \times ADC_{Gain} \tag{17}$$

$$S\_rawAdc2 = CVC2 \times ADC_{Gain} \tag{18}$$

Once digitized, the ratio between the input and reference signal is computed and scaled, shown in the Equation 19. After determination an digital gain can be applied.

$$S\_Raw_{Scaled} = \frac{S\_Raw_{Adc1}}{S\_Raw_{Adc2} + \frac{C_{shift}}{C_{int}} \times ADC_{Gain}} \times Dig_{Gain} \tag{19}$$

The Equation 19 can be simplified, shown in Equation 20.

$$S\_Raw_{Scaled} = \frac{C_x - C_{shift}}{C_r} \times Dig_{Gain} \tag{20}$$

If 1/C linearization is enabled, the signal inversion must also be applied to the physical signal range. This requires shifting the scaled signal S_Raw_{Scaled} by a range shift value R, as defined in Equation 22. The range shift value RValue accounts for the external stray capacitance's C_{stray}, which are introduced during sensor module assembly. Accurate consideration of C_{stray} significantly enhances the effectiveness of the 1/C linearization.

$$S\_Raw = \begin{cases} \text{1/C Linearization Enabled,} & \frac{1-RValue^2}{S\_Raw_{Scaled}+RValue} + RValue \\ \text{1/C Linearization Disabled,} & S\_Raw_{Scaled} \end{cases} \tag{21}$$

$$RValue = \frac{C_{shift} - C_{stray}}{mean(C_r)} \times Dig_{Gain} \tag{22}$$

		Valid Input Range
CVC1	Capacitance-to-Voltage Converter 1	
CVC2	Capacitance-to-Voltage Converter 2	
S_Raw	Raw sensor reading from ADC	-(0x7FFFFF) to 0x7FFFFF
S_Raw_{Scaled}	Raw sensor reading from ADC scaled	-(0x7FFFFF) to 0x7FFFFF
C_{int1}	*Cm1Config.CmCapInt* set integration capacity (Step size 2pF)	20pF to 82pF
C_{int2}	*Cm2Config.CmCapInt* set integration capacity (Step size 2pF)	20pF to 82pF
C_{shift1}	*Cm1Config.CmCapShift* set shift capacity (Step size 2pF)	0pF to 62pF
C_{shift2}	*Cm2Config.CmCapShift* set shift capacity (Step size 2pF)	0pF to 62pF
ADC_{Gain}	*Cm1Config.CmAdcEnShift* enables selection of value	1 to 2
Dig_{Gain}	*MathSbrAlgoSel.DigGain1* applies an digital gain (Step size 0.25)	1 to 8
RValue	*CsInvParam.RValue* Range Shift Value, Only available when 1/C Linearization is enabled	0 to 30

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Table 49. Data Format of S_Raw and S_Raw$_{Scaled}$

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	-2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 50. Data Format of RValue

Bit Number	23	22	21	...	18	17	16	...	0
Meaning, Weighting	0 = positive 1 = negative	2^4	2^3	...	2^0	2^{-1}	2^{-2}	...	2^{-18}

5.7.6 Capacitive Application Mode 6: Differential / Referred to Ground

In Capacitive Application Mode 6, a differential measurement is performed between two grounded capacitive sensors C_x and C_y.

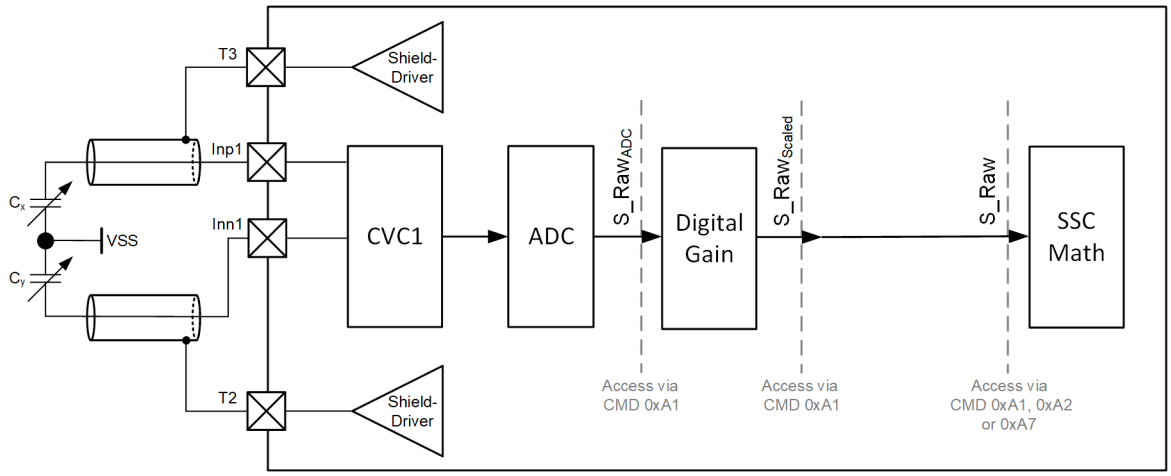

Figure 23. Capacitive Application Mode 6

The CVC calculates the difference between C_x, C_y, and the reference C_{int}, as shown in Equation 23. Before the reference capacitor integrates the signal, a capacitance shift C_{shift} can be applied to reduce offset in the measurement. The adjusted signal is forwarded to the ADC for digitization.

Note: For optimal operation, C_x should be greater than C_y. If no pressure is applied and this is not the case, swap the sensor connections.

$$CVC1 = \frac{C_x - C_y - C_{shift}}{C_{int}} \tag{23}$$

The signal from the ADC is scaled according to Equation 24, effectively amplifying the measurement so that low input signal spans can be utilized.

$$S\_Raw_{Scaled} = S\_Raw = (CVC1 \times ADC_{Gain} - \frac{AdcShift}{8}) \times Dig_{Gain} \tag{24}$$

		Valid Input Range
CVC1	Capacitance-to-Voltage Converter 1	
S_Raw	Raw sensor reading from ADC	-(0x7FFFFF) to 0x7FFFFF
S_Raw$_{Scaled}$	Raw sensor reading from ADC scaled	-(0x7FFFFF) to 0x7FFFFF
C_{int}	*Cm1Config.CmCapInt* set integration capacity (Step size 2pF)	20pF to 82pF
C_{shift}	*Cm1Config.CmCapShift* set shift capacity (Step size 2pF)	0pF to 62pF
ADC$_{Gain}$	*Cm1Config.CmAdcEnShift* enables selection of value	1 to 2
ADC Shift	*Cm1Config.CmAdcShift* enables selection of value (Step size 0.125)	0 to 0.875
Dig$_{Gain}$	*MathSbrAlgoSel.DigGain1* applies an digital gain (Step size 0.25)	1 to 8

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Table 51. Data Format of S_Raw and S_Raw_{Scaled}

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	-2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

5.7.7 Capacitive Application Mode 11: Differential $(C_x-C_y)/(C_x+C_y)$ / Referred to Ground

In Capacitive Application Mode 11, a differential ratio of two grounded capacitive sensors C_x and C_y is measured and processed for linearization.

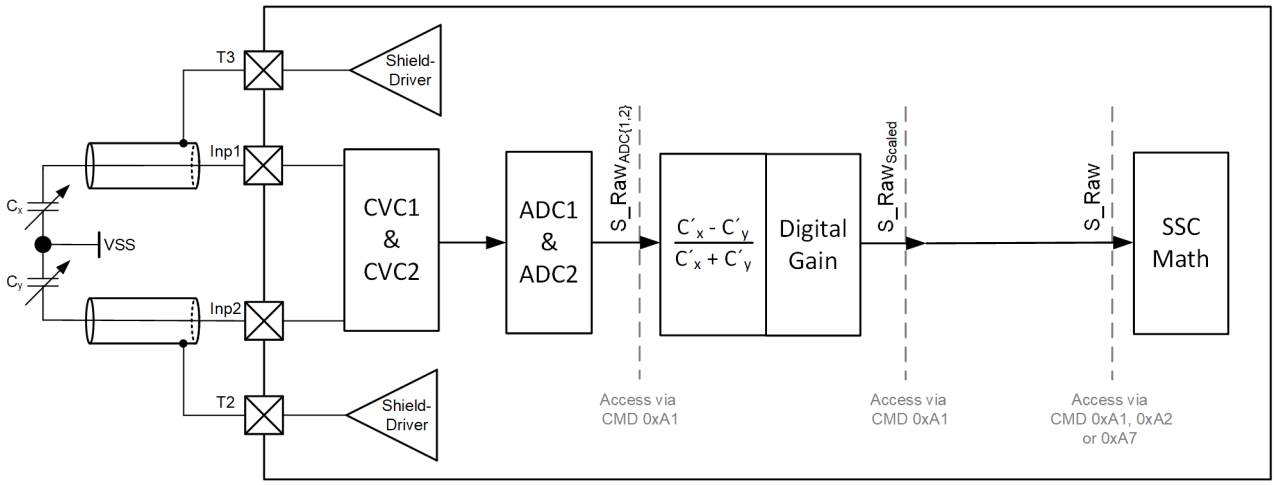

Figure 24. Capacitive Application Mode 11

The CVC calculates a ratio between the measured capacitance C_x and an internally selected reference capacitance C_{int}, as shown in Equation 25, and also a ratio between the measured capacitance C_y and an internally selected reference capacitance C_{int}, as shown in Equation 26. Before the reference capacitor integrates the signals, a capacitance shift C_{shift} can be applied to reduce offset in the measurement. The adjusted signal is forwarded to the ADC for digitization.

$$CVC1 = \frac{C_x - C_{shift1}}{C_{int}} \tag{25}$$

$$CVC2 = \frac{C_y - C_{shift2}}{C_{int}} \tag{26}$$

Note: C_{int} has the same value for both measurements, to ensure a common base.

The analog signals can be amplified by the ADC gain stage as shown in Equation 27 and Equation 28.

$$S\_Raw_{Adc1} = CVC1 \times ADC_{Gain} \tag{27}$$

$$S\_Raw_{Adc2} = CVC2 \times ADC_{Gain} \tag{28}$$

After digitization of both signals, the pure ratio $(C_x-C_y)/(C_x+C_y)$ is obtained by compensating with the range shift value RValue, as shown in Equation 29. This compensation accounts for the average of the capacitance shift values C_{shift1}, C_{shift2}, the internal reference capacitance C_{int}, and the external stray capacitance C_{stray}, which is introduced during sensor module assembly.

$$S\_Raw_{Scaled} = S\_Raw = \frac{S\_Raw_{Adc1} - S\_Raw_{Adc2}}{S\_Raw_{Adc1} + S\_Raw_{Adc2} + 2 \times R} \times Dig_{Gain} \tag{29}$$

$$RValue = \frac{mean(C_{shift1,2}) - C_{stray}}{C_{int}} \times ADC_{Gain} \tag{30}$$

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		Valid Input Range
CVC1	Capacitance-to-Voltage Converter 1	
CVC2	Capacitance-to-Voltage Converter 2	
S_Raw	Raw sensor reading from ADC	-(0x7FFFFF) to 0x7FFFFF
S_Raw_{Scaled}	Raw sensor reading from ADC scaled	-(0x7FFFFF) to 0x7FFFFF
C_{int1}	*Cm1Config.CmCapInt* set integration capacity (Step size 2pF)	20pF to 82pF
C_{int2}	*Cm2Config.CmCapInt* set integration capacity (Step size 2pF)	20pF to 82pF
C_{shift1}	*Cm1Config.CmCapShift* set shift capacity (Step size 2pF)	0pF to 62pF
C_{shift2}	*Cm2Config.CmCapShift* set shift capacity (Step size 2pF)	0pF to 62pF
ADC_{Gain}	*Cm1Config.CmAdcEnShift* enables selection of value	1 to 2
Dig_{Gain}	*MathSbrAlgoSel.DigGain1* applies an digital gain (Step size 0.25)	1 to 8
RValue	*CsInvParam.RValue* Range Shift Value, Only available when 1/C Linearization is enabled	0 to 30

Table 52. Data Format of S_Raw and S_Raw_{Scaled}

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	-2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 53. Data Format of RValue

Bit Number	23	22	21	...	18	17	16	...	0
Meaning, Weighting	0 = positive 1 = negative	2^4	2^3	...	2^0	2^{-1}	2^{-2}	...	2^{-18}

5.8 AFE Sequencer

The measurement flow, especially the frequency of main bridge measurements vs. auxiliary measurements can be configured by the user. Once started by the ARM MCU, the measurement flow runs autonomously controlled by the AFE. The AFE Sequencer state machine ensures predictable measurement timing in the continuous cyclic operation of ZSSC3286.

The AFE sequencer carries out AFE measurements based on a measurement slot mechanism. There can be up to eight measurement slots assigned per AFE, which form a single measurement cycle. A measurement cycle can be executed only once (for example, initiated by a dedicated command request) or continuously cycled in Cyclic Mode operation of ZSSC3286.

Each of the measurement slots inside AFE1 or AFE2 can be individually configured for the following measurement types:

- Sensor Measurement (SM+): bridge inputs INP/INN directly converted (non-inverted)
- Sensor Measurement (SM-): bridge inputs INP/INN flipped (inverted)
- Auxiliary Measurement (aux_i): cycles through the auxiliary measurement vector

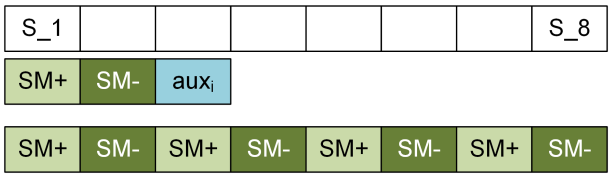

Figure 25. Measurement Slot Configuration with Two Example Configurations

The actual number of measurement slots per measurement cycle can be defined by the user between 1 and 8. The hardware allows to configure any combination, but not all combinations lead to reasonable measurement schemes. The GUI supports the user in selecting proper measurement schemes. Figure 25 shows two example configurations. The measurement schemes are explained in further detail in section 5.8.3, 5.8.4, and 5.8.5.

Auxiliary measurements usually have lower response time requirements than measurements on the main sensor bridge. The auxiliary measurements are therefore cycled orthogonal to the main loop of the sequencer. Activated

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auxiliary measurements become listed in the so called auxiliary measurement vector. The vector index ‘i’ gets increased after each executed aux_i slot and starts over after the entire set of active measurements was completed. The configuration options of auxiliary measurements are further detailed in section 5.8.2.

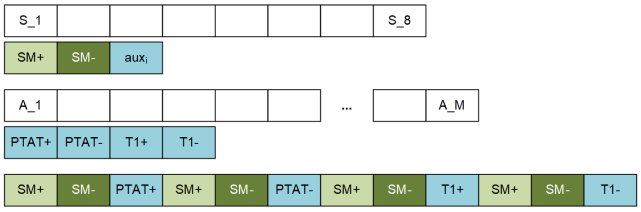

Figure 26. Auxiliary Measurement Configuration, and Corresponding Measurement Flow

Figure 26 shows the sequencer operation with an example configuration using 4 auxiliary measurements. During the 3rd measurement (configured as aux_i), the first enabled auxiliary measurement is executed (”PTAT”, internal temperature sensor). After the measurement sequence (SM+/SM-/aux_i) is executed again in the next measurement slot, the next enabled auxiliary measurement is executed (“T1”, external temperature sensor). Similarly, “Bridge1 open” and “Bridge1 short” diagnostics measurements are carried out in following measurement slots. During the 5th execution of the measurement sequence, the PTAT auxiliary measurement is carried out again.

5.8.1 Bridge Sensor Measurement Configuration

The main bridge sensor signals can be measured in three ways:

- SM+/SM- (or SM-/SM+) measurement
- SM+/AZ measurement (SM+ and auto-zero measurement)
- SM+ without AUX_AZ measurement

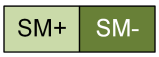

Figure 27. SM+/SM- (or SM-/SM+) Measurement

Figure 28. SM+/AZ Measurement

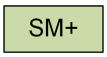

Figure 29. SM+ without AZ Measurement

Configurations in Figure 27 and Figure 28 provide digital offset compensation of the entire signal path in the analog front end. The configuration in Figure 29 only provides analog offset compensation in the first stage of the PGA. The offsets of the second PGA stage and the ADC offset are not compensated.

In the SM+/SM- configuration, the bridge inputs INP/INN are first converted straight forward in the SM+ measurement slot and second with an internally flipped INP/INN input signal in SM- slot. For the SM+/AZ configuration, the second measurement (AZ) is performed without applied input signal. INP/INN become disconnected form the sensor and internally shorted for AZ measurements.

Since signal integration time in SM+/SM- configuration is twice as long as in in the SM+/AZ configuration (same ADC resolution settings assumed), the SM+/SM- configuration achieves approx. 0.5-bit better noise performance than the SM+/AZ configuration. The longer input signal integration time of the SM+/SM- configuration leads to an increased output update rate and step response as described in section 5.8.3 and section 5.8.4.

The auto-zero measurement (AZ) belongs to the group of auxiliary measurements and is cycled less often if either of the following options appears:

- further auxiliary measurements are enabled in the auxiliary measurement vector described in section 5.8.2
- accelerated bridge measurements are enabled as described in section 5.8.5

Since the offset in the internal signal path varies rather slowly, the auto-zero compensation remains very accurate even for a long auxiliary measurement vector.

Because SM- needs to be configured and most sensor applications also require other auxiliary measurements, the assignment of the AZ measurement to the group of auxiliary measurements helps to reduce the worst case step response on the main bridge sensor.

The lowest step response is achieved with the “SM+ only” configuration shown in Figure 29 if no other auxiliary measurements are needed for the desired sensor application.

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A further influence on the overall measurement time (output update rate and worst case response) has the input settling time of each measurement task. This settling is required depending on the output resistance of the external sensors, respective capacitive loads on the signal lines and the ADC resolution selected by the user. The input settling time is always inserted before an ADC conversion starts and can be configured in the GUI for main bridge measurements via Configure\AFE\Bridge\SetTime [µs] and for auxiliary temperature measurements via Configure\AFE\Temperature\SetTime [µs].

Considering achievable measurement latencies and noise performance, configuration shown in Figure 27 is better when higher ADC resolutions are required or for sensor configurations with fast input settling, while configuration shown in Figure 28 and Figure 29 are preferable when lower ADC resolutions become selected or for sensor configurations requiring long input settling times (bridge settling time has a considerable impact on the timing budget).

5.8.2 Auxiliary Measurement Configuration

The supported auxiliary measurements are:

- Auto-zero for internal signal path
- Temperature on sensor input T1
- Temperature on sensor input T2
- Temperature on sensor input T3
- Internal PTAT
- AFE diagnostic checks
  - Sensor connection checks for all external sensors (Short to TOPx pin or BOTx pin and Open)
  - Bridge signal range check
  - AFE gain and offset drift supervision via internal reference DAC

They can be activated in the GUI via tabs Configure\AFE\Sequencer, Configure\AFE\Temperature Selection and Diagnostic\Sensor\AFE.

5.8.3 Timings with SM+/SM- Configuration

As described in section 5.8.1, sensor configurations with fast input settling or applications requiring higher ADC resolutions are better served with the SM+/SM- scheme for the main bridge measurement. For the step response consideration the following application example is used:

- Sensor Measurement (non-inverted)
- Sensor Measurement (inverted)
- Auxiliary Measurement (for example, for sensor temperature)

Note: SM+ and SM- can be exchanged yielding to the same result.

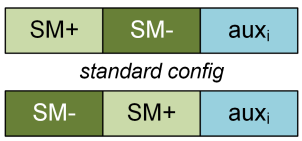

Figure 30. SM+/SM- Configuration

For SM+/SM- configuration, the measurement cycle and output update rate is shown in Figure 31 for an example involving three enabled auxiliary measurement tasks. After the final main measurement task is completed, the firmware starts data processing as detailed in section 6 and section 7. The conditioned output signal is then recorded into the output registers.

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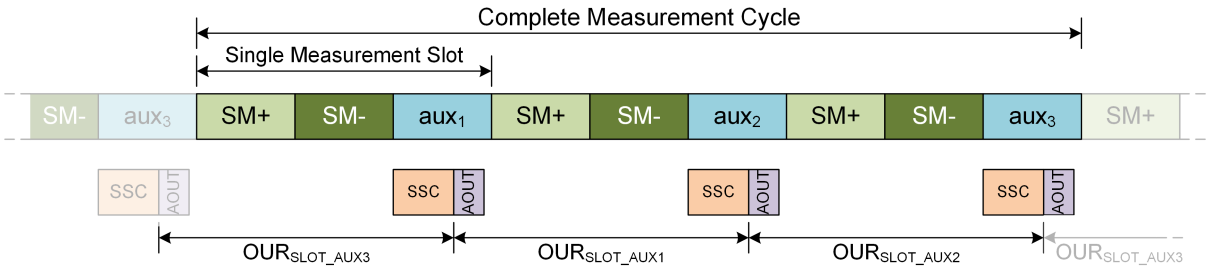

Figure 31. SM+/SM- Measurement Cycle and Output Update Rate

For SM+/SM- configuration the worst-case step response is shown in Figure 32 and consists of:

- 4 sensor ADC-conversion times (duration depending on selected ADC resolution)
- 1 auxiliary conversion time (fixed duration, based on longest auxiliary conversion timing)
- 1 SSC calculation

Additionally, there is a delay that depends on the selected interface:

- 1 settling time at AOUT for all analog output options
- 2 cycle times for IO-Link communication

In a worst-case scenario, intermediate results can occur due to the asynchronous nature of input changes and data readout relative to the internal measurement cycle.

Worst-case scenario for IO-Link communication depends on IO-Link master since it defines the cycle time. ZSSC3286 defines minimum cycle time of 600µs.

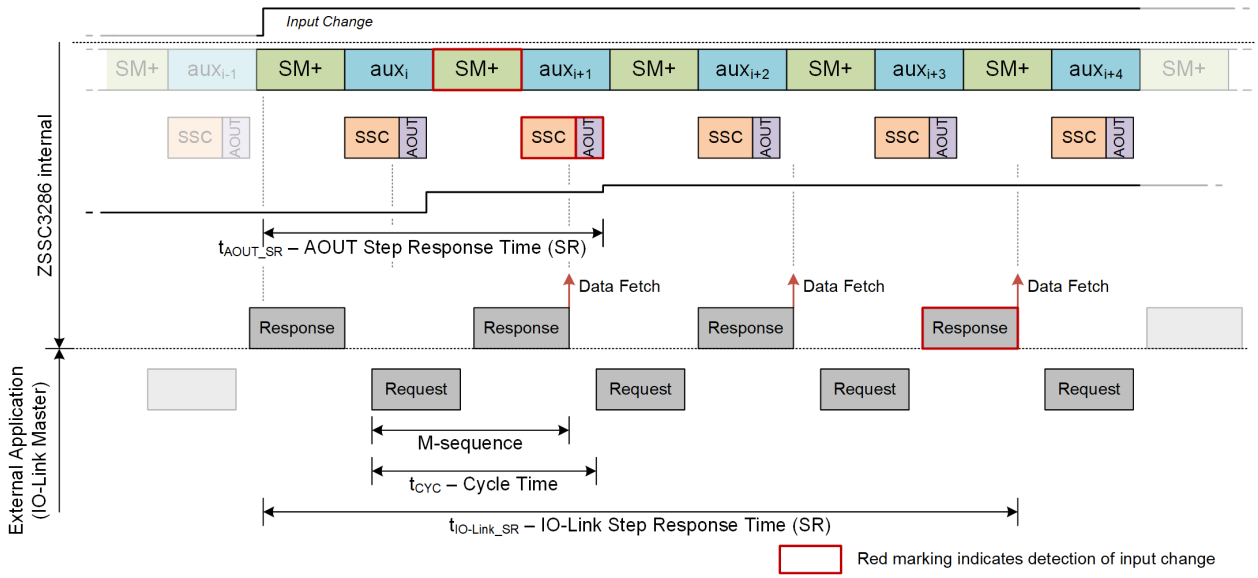

Figure 32. SM+/SM-Step Response

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5.8.4 Deterministic Input Step Response with SM+/AZ Configuration

Since the SM+/SM- configuration samples the input signal twice as long as the SM+/AZ configuration and it suffers a noticeable timing overhead for sensor configurations with slow sensor input signal settling, a second SM+/AZ measurement scheme with deterministic step response times is available. For the step response consideration, the following application example is used:

- Sensor measurement (non-inverted)
- Auxiliary measurement (for example, for sensor path auto-zero and/or sensor temperature) within the auxiliary measurement vector

Figure 33. SM+/AZ Configuration

For SM+/SM- configuration, the measurement cycle and output update rate is shown in Figure 31 for an example involving three enabled auxiliary measurement tasks. After the final main measurement task is completed, the firmware starts data processing as detailed in section 6 and section 7. The conditioned output signal is then recorded into the output registers.
Assuming equal ADC resolution settings for the SM+/SM- configuration as described in section 5.8.3 and the SM+/AZ configuration described in this section, the worst case step response is shorter by two sensor AD-conversion times in case of the SM+/AZ setup. The auxiliary measurement duration in the SM+/AZ setup may become slightly longer than for the SM+/SM- configuration, since it is determined by the AZ measurement time if the selected resolution of the main bridge is larger than the resolutions of all other active auxiliary measurements. This is because the resolution of the AZ measurement is set by the resolution of the SM+ measurement and the longest measurement of the auxiliary measurement vector determines the duration of the aux_i slot(s)

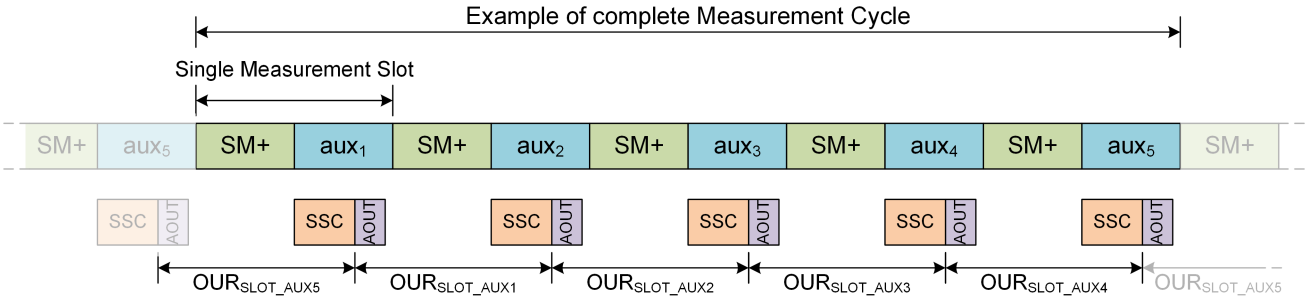

Figure 34. SM+/AZ Measurement Cycle and Output Update Rate

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As shown in Figure 35, the worst-case latency consists of:

- 2 sensor AD-conversion times (duration depending on selected ADC resolution)
- 1 auxiliary conversion time (fixed duration, based on longest auxiliary conversion timing)
- 1 SSC calculation

Additionally, there is a delay that depends on the selected interface:

- 1 settling time at AOUT for all analog output options
- 2 cycle times for IO-Link communication

In a worst-case scenario, intermediate results can occur due to the asynchronous nature of input changes and data readout relative to the internal measurement cycle.

Worst-case scenario for IO-Link communication depends on IO-Link master since it defines the cycle time. ZSSC3286 defines minimum cycle time of 600µs.

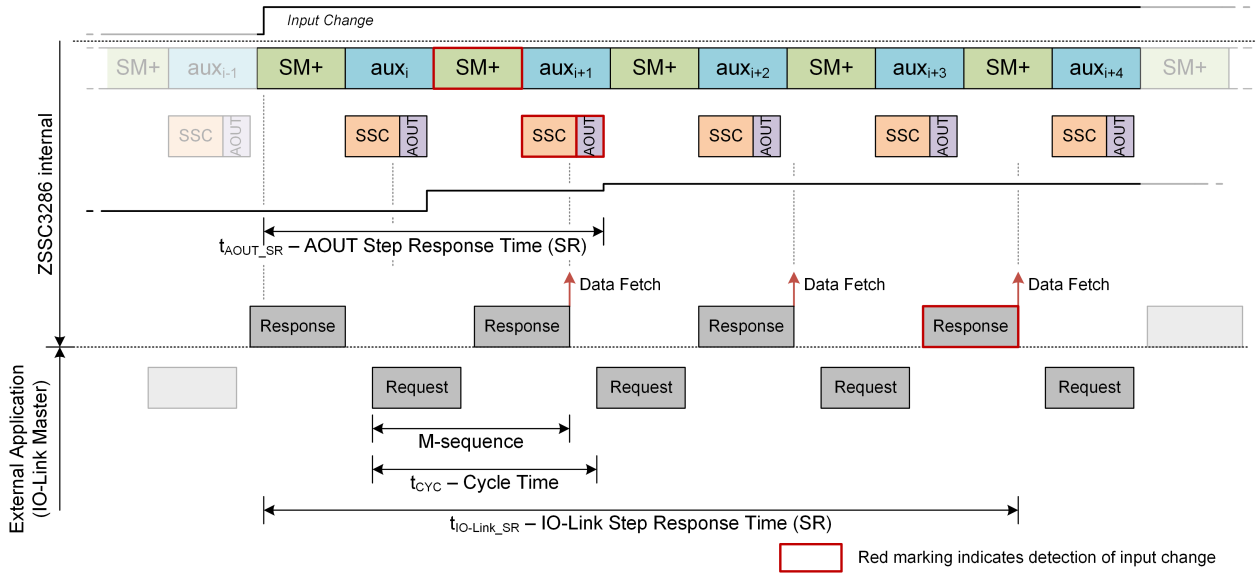

Figure 35. Measurement Flow and Latency for SM+/AZ Configuration

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5.8.5 Accelerated Bridge Measurements with Sparsely Inserted Auxiliary Measurements

For applications which focus on highest conversion rates at the bridge sensor input but do not require a deterministic maximum input to output latency of the corrected sensor signal, auxiliary measurements can be sparsely inserted to occur only after a certain number of measurement sequences were executed by the AFE sequencer. This way, auxiliary measurements become executed even more seldom, giving the main sensor bridge measurements priority.

The AFE sequencer can be configured such that an aux_i measurement is only executed (inserted) after every Px measurement sequence. P can be selected as 2, 4, or 8. Figure 36 shows an example of a measurement flow with P = 2 while Figure 37 uses P = 8 where aux_i measurements are executed after eighth measurement sequences.

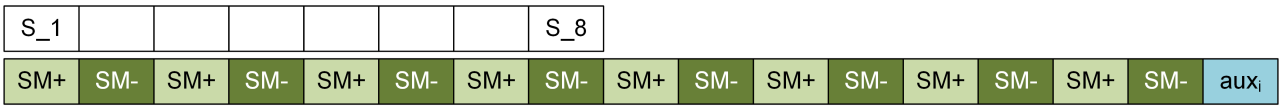

Figure 36. Auxiliary Measurement Executed after Every Second Measurement Cycle

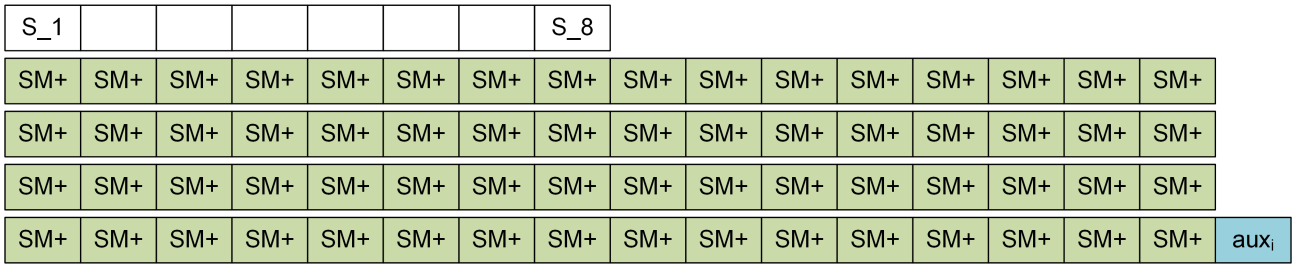

Figure 37. Sequencer Setup for Highest Update Rate on Bridge Sensor

For the use case of SM+/SM- measurement sequencer, the output update rate is shown in Figure 38. The complete measurement cycle is finished after finishing the last auxiliary measurement task. After finishing the SM+ main measurement task, firmware starts with data processing as described in section 6 and section 7. Since the auxiliary measurement tasks are inserted only after every 2nd, 4th, or 8th measurement sequence, the output update rate also varies in the same period. The same description is also valid if SM+/AZ only measurement sequencer is used.

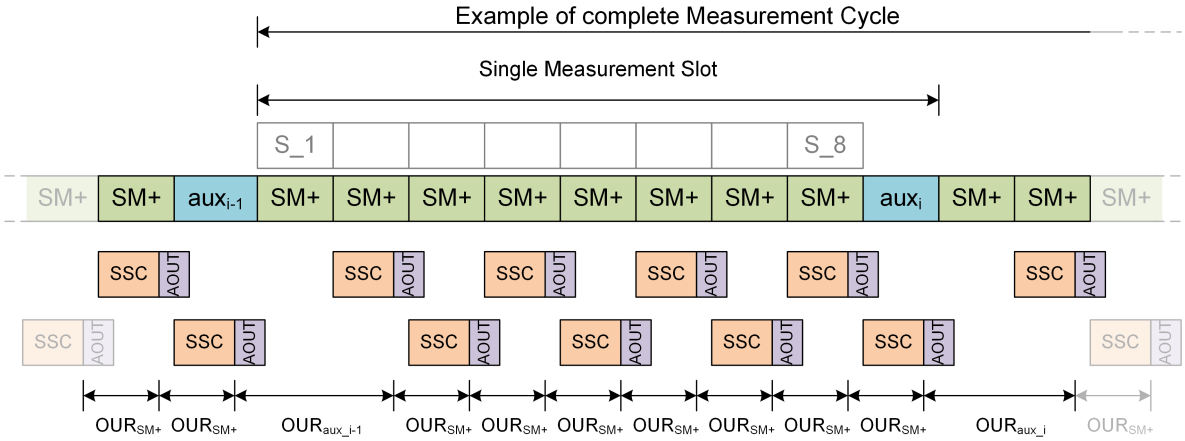

Figure 38. SM+ Accelerated Measurement Cycle and Output Update Rate

The worst-case step response primarily depends on the selected AFE sequencer mode as the following:

- SM+/SM- configuration: refer to Figure 32 and description for step response in section 5.8.3
- SM+/AZ configuration: refer to Figure 35 and description for step response in section 5.8.4

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6 Sensor Signal Conditioning

6.1 Signal Conditioning Data Path

Figure 39 shows the sensor signal conditioning flow that is applied for AFE output data to compensate for offset, gain, non-linearity, and temperature effects and to calculate the conditioned data for further output processing. See section 6.2 to section 6.7 for more information on the basis mathematical subfunctions.

The signal path from conditioned data to individual output signals is described in section 7.

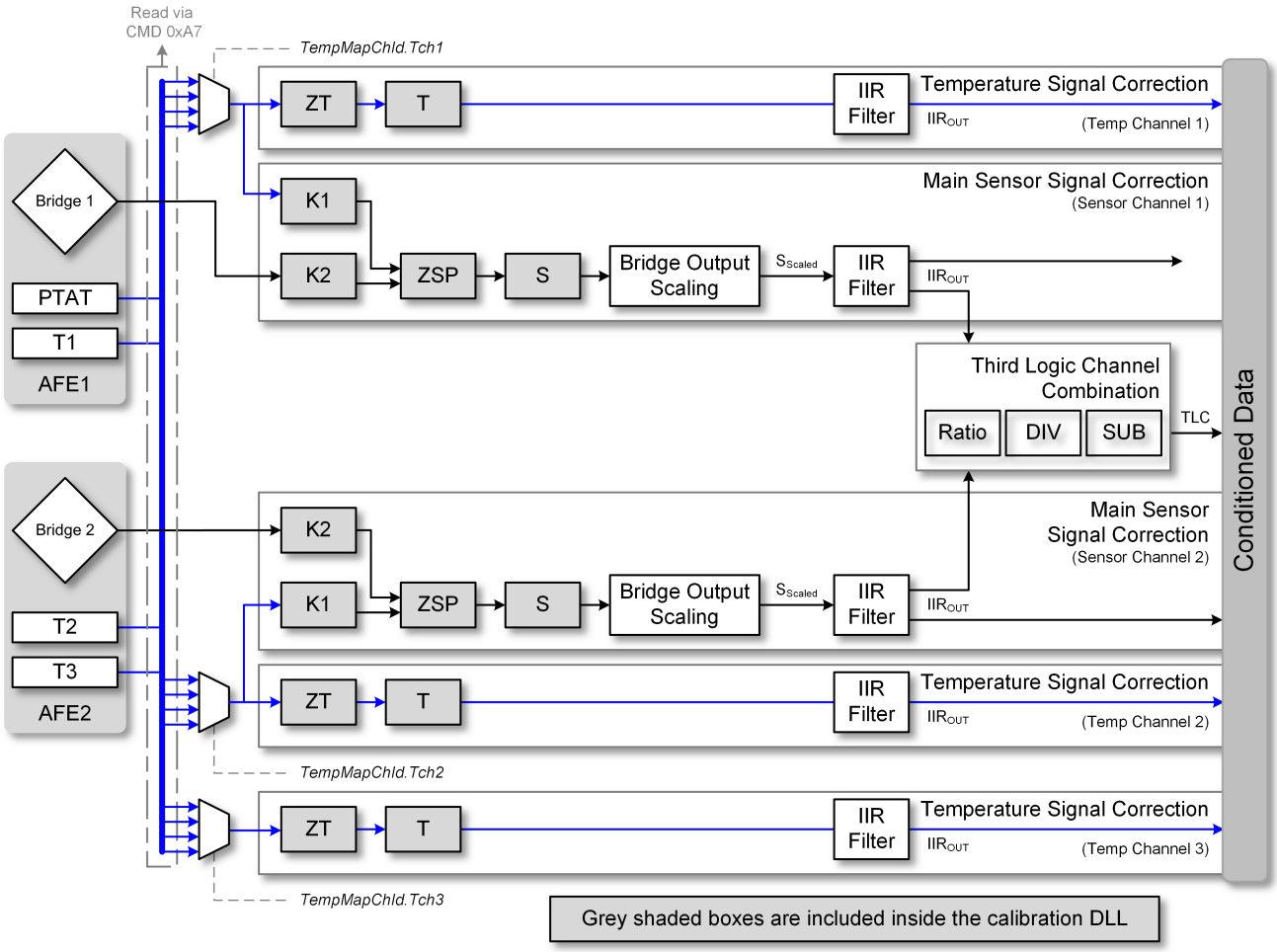

Figure 39. Sensor Signal Flow Chart from Input to Conditioned Data

6.2 Main Sensor Signal Correction

The ZSSC3286 supports basic second-order compensation of sensor nonlinearities. The following basic SSC math options are available:

- Sensor signal correction
  - SOT Curve-0: Parabolic compensation curve
  - SOT Curve-1: S-shaped compensation curve
- Temperature signal correction

The parabolic compensation is recommended for most sensor types. The applied SSC math option can be selected in the GUI through the field Calibration\Curve.

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The available SSC capabilities for SOT Curve-0 and SOT Curve-1 are described in Table 54, Table 55, and Table 56. The used equation terms are as follows:

		Valid Input Range
S	Compensated sensor signal	0x0 to 0xFFFFFF
S_Raw	Raw sensor reading from ADC (after AZ correction, depends on Afe1SmConfig and/or Afe2SmConfig)	-(0x7FFFFF) to 0x7FFFFF
T_Raw	Raw temperature reading (after AZ correction)	-(0x7FFFFF) to 0x7FFFFF
Gain_S	Coefficient of sensor gain term	-(0x7FFFFF) to 0x7FFFFF
Offset_S	Coefficient of sensor offset term	-(0x7FFFFF) to 0x7FFFFF
Tcg	Temperature coefficient gain term	-(0x7FFFFF) to 0x7FFFFF
Tco	Temperature coefficient offset term	-(0x7FFFFF) to 0x7FFFFF
SOT_tcg	Second-order term for Tcg non-linearity	-(0x7FFFFF) to 0x7FFFFF
SOT_tco	Second-order term for Tco non-linearity	-(0x7FFFFF) to 0x7FFFFF
SOT_sens	Second-order term for sensor non-linearity	-(0x7FFFFF) to 0x7FFFFF
SENS_shift	Post-calibration, post-assembly offset shift	-(0x7FFFFF) to 0x7FFFFF
|...|	Absolute value	
$[...]_{ll}^{ul}$	Bound/saturation number range from *ll* to *ul*, overflow and/or underflow is reported as saturation in the Status Byte	

All raw data and compensation coefficients supplied to the formulas are required in 24-bit data format shown in Table 54 and Table 55.

Table 54. Data Format of Raw ADC Readings

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	-2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 55. Data Format of 24-bit SSC Coefficients

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	0 = positive 1 = negative	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

The compensated result data is supplied in 24-bit data format as shown in Table 56.

Table 56. Data Format of Corrected SSC Result

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

6.2.1 Pre-calculation

Simplified:

$$K_1 = 2^{23} + \frac{T\_Raw}{2^{23}} \times \left(\frac{4 \times SOT\_tcg}{2^{23}} \times T\_Raw + 4 \times Tcg \right) \tag{31}$$

$$K_2 = 4 \times Offset\_S + S\_Raw + \frac{T\_Raw}{2^{23}} \times \left(\frac{4 \times SOT\_tco}{2^{23}} \times T\_Raw + 4 \times Tco \right) \tag{32}$$

Complete:

$$K_1 = \left[2^{23} + \left[\frac{T\_Raw}{2^{23}} \times \left[\left[\frac{SOT\_tcg}{2^{21}} \times T\_Raw \right]_{-2^{25}}^{2^{25}-1} + 4 \times Tcg \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \tag{33}$$

$$K_2 = \left[4 \times Offset\_S + \left[S\_Raw + \left[\frac{T\_Raw}{2^{23}} \times \left[\left[\frac{SOT\_tco}{2^{21}} \times T\_Raw \right]_{-2^{25}}^{2^{25}-1} + 4 \times Tco \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \tag{34}$$

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6.2.2 SOT Curve-0 (Parabolic Compensation)

Simplified:

$$Z_{SP} = \frac{4 \times Gain\_S}{2^{23}} \times \frac{K_1}{2^{23}} \times K_2 + 2^{23} \tag{35}$$

$$S = \frac{Z_{SP}}{2^{23}} \times \left(\frac{4 \times SOT\_sens}{2^{23}} \times Z_{SP} + 2^{23} \right) + SENS\_shift \tag{36}$$

Note: Z_{SP} and S are delimited to positive number range.

Complete:

$$Z_{SP} = \left[\left[\frac{Gain\_S}{2^{21}} \times \left[\frac{K_1}{2^{23}} \times K_2 \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{0}^{2^{25}-1} \tag{37}$$

$$S = \left[\left[\frac{Z_{SP}}{2^{23}} \times \left[\left[\frac{SOT\_sens}{2^{21}} \times Z_{SP} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + SENS\_shift \right]_{0}^{2^{24}-1} \tag{38}$$

The coefficient *SENS_shift* will be set automatically by the firmware if *ZeroAdjEna* in section 13.9.1 is enabled. Refer section 6.3 for further details about auto zero adjustment and handling of *SENS_shift*.

6.2.3 SOT Curve-1 (S-shaped Compensation)

Simplified:

$$Z_{SS} = \frac{4 \times Gain\_S}{2^{23}} \times \frac{K_1}{2^{23}} \times K_2 \tag{39}$$

Note: K_1 and K_2 according to Equation 33 and Equation 34.

$$S = \frac{Z_{SS}}{2^{23}} \times \left(\frac{4 \times SOT\_sens}{2^{23}} \times |Z_{SS}| + 2^{23} \right) + 2^{23} + SENS\_shift \tag{40}$$

Note: S is delimited to positive number range.

Complete:

$$Z_{SS} = \left[\frac{Gain\_S}{2^{21}} \times \left[\frac{K_1}{2^{23}} \times K_2 \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \tag{41}$$

$$S = \left[\left[\left[\frac{Z_{SS}}{2^{23}} \times \left[\left[\frac{SOT\_sens}{2^{21}} \times |Z_{SS}| \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} + SENS\_shift \right]_{0}^{2^{24}-1} \tag{42}$$

The coefficient *SENS_shift* will be set automatically by the firmware if *ZeroAdjEna* in section 13.9.1 is enabled. Refer section 6.3 for further details about auto zero adjustment and handling of *SENS_shift*.

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6.3 Zero Adjustment

The ZSSC3286 has an in-field offset correction feature called Zero Adjustment. This feature allows end users to compensate for sensor drift (for example, due to mechanical tension or aging) during the operational life of a sensor application via dedicated IO-Link ISDUs or triggered by the Zero Adjustment Trigger (ZAT) GPIO without knowledge of additional coefficients stored inside the CCP. This feature will overwrite the *SENS_shift* coefficient described in section 6.2 for main sensor signal or *T_shift* coefficient described in section 6.4 for temperature signal depending on selected MDC channel and the mapped SSC result to this channel defined in section 13.17.6.

The Zero Adjustment feature is enabled using *ZeroAdjEna* in section 13.17.6. If *ZeroAdjEna* is disabled, the *SENS_shift* and *T_shift* coefficients stored in CCP (Configuration and Calibration Page) are used for offset compensation. In this case ZeroAdjustment ISDUs and ZAT GPIO are also disabled.

The ZeroAdjustment ISDU or ZAT GPIO will trigger a single AFE measurement and its internal mathematics model backward, and based on this, defining new *SENS_shift* or *T_shift* coefficients. This backwards calculation requires storing a target output value (that is, Reference Value) upfront in CCP registers individually for each output channel, see section 13.17.1, section 13.17.2, section 13.17.3, section 13.17.4, and section 13.17.5. Each Reference Value represents one single point of the compensated result *S* (see Equation 36 or Equation 40) or *T* (see Equation 44), and therefore use the same format as the compensated data and is shown in the following table.

Table 57. Data Format of Reference Value

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	2^{0}	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Note: Reference Value uses the same data format used for corrected signal conditioning results S and T.

Additionally, an individual Offset Window is defined for each channel. This window is stored in the same registers as the Reference Values. It specifies the allowable range of the *Offset*, defined as the deviation between the stored Reference Value and the actual SSC measurement result. If the calculated *Offset* exceeds this predefined range, it is considered invalid and no Zero Adjustment is performed. The Offset Window values stored in NVM are internally converted into a 24-bit representation by division with 200 and rescaling with factor of 2^{24}. This representation defines the permissible *Offset* drift in discrete steps of 0.5% of the respective conditioning results *S* and *T*, as described in Table 58 and shown in Figure 40.

Table 58. Data Format of Offset Window

Bit Number	7	6	5	4	3	2	1	0
Meaning, Interpretation	64.0%	32.0%	16.0%	8.0%	4.0%	2.0%	1.0%	0.5%

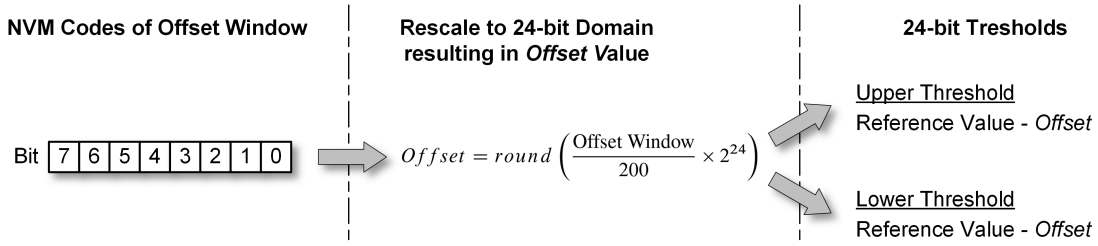

Figure 40. Calculation of *Offset* based on Offset Window

Note: Reference Value and Offset Window must fall within the Measurement Range defined in SSP Scaling described in section 7.3.

The Zero Adjustment feature does not support Third Logic Channel (TLC).

Note: Since Zero Adjustment will overwrite selected *SENS_shift* or *T_shift*, this will have an impact on the analog output signal if the same signal is mapped to AOUT.

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6.3.1 Process of Zero Adjustment

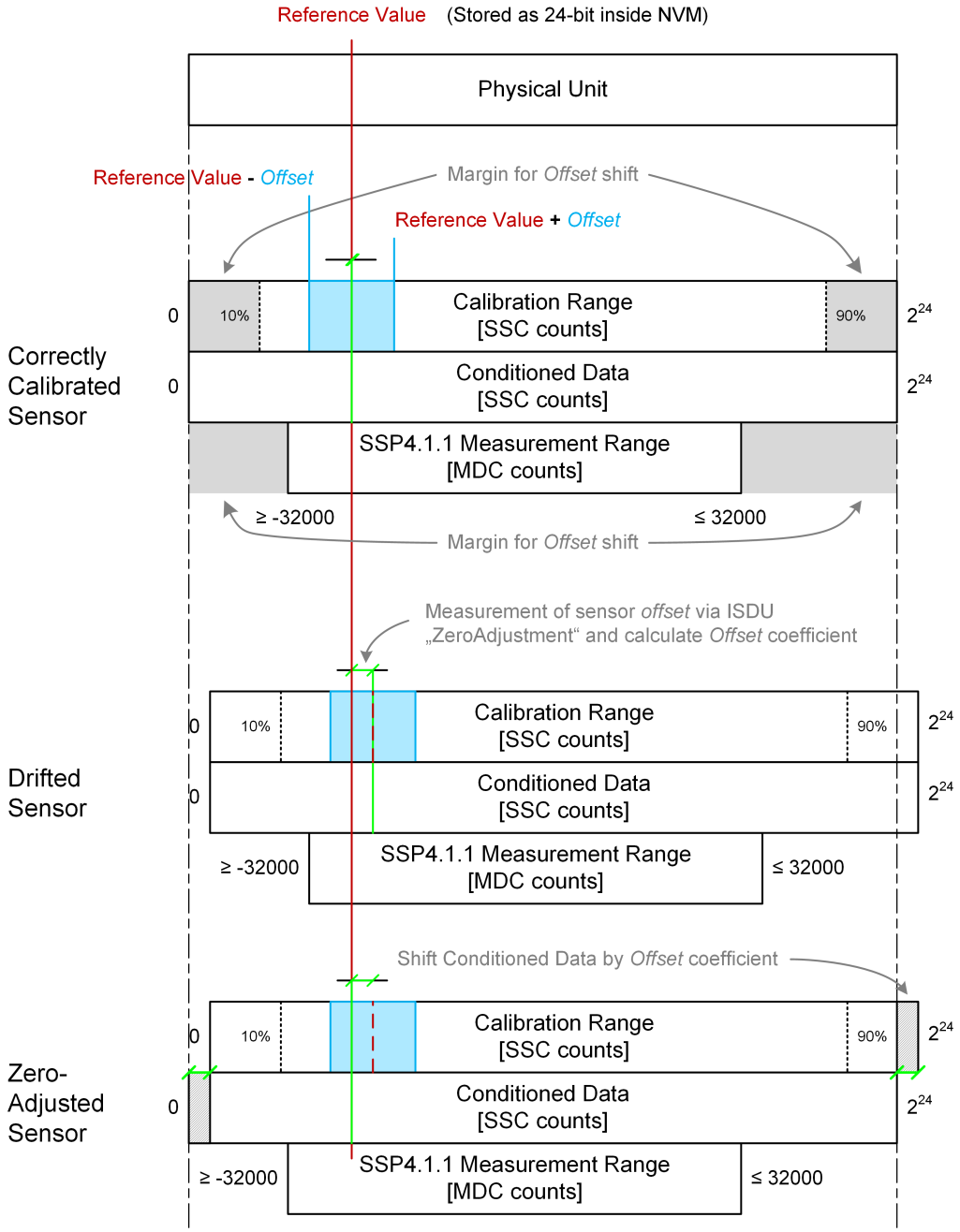

Figure 41. Range Shift by Zero Adjustment

Figure 41 shows the Zero Adjustment feature.

- Correctly Calibrated Sensor: The calibration range maps directly to the physical environment (Physical Unit range). The *Offset* is still zero. Therefore, the SSC conditioned data equals the calibration range. The IO-Link measurement range is a subset of the conditioned data generated by IO-Link rescaling feature described in section 7.3, reaching from maximum -32000 to +32000 for SSP4.1.1.

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During calibration, sensor targets must be chosen in a way to leave margin for *Offset* shift. Thus the Offset Window must be equal or smaller than:

- the difference between Reference Value and lower or upper Measurement Range value, whichever is smaller
- the difference between (whichever is smaller)
  - lower Measurement Range value and 0 SSC counts of calibration range (or unshifted conditioned data)
  - upper Measurement Range value and 2^{24}-1 SSC counts of calibration range (or unshifted conditioned data)

Furthermore, the AFE must be able to measure the offset drift defined by Offset Window shift.

- Drifted Sensor: The Physical Unit range mismatches the calibration range (green horizontal line). The mismatch is quantified with the Zero Adjustment Routine (ISDU 0x0400): At a physical environment set to the Reference Value, a measurement of conditioned data is performed (green vertical line) and compared to the Reference Value.
- Zero-Adjusted Sensor: The *Offset* is applied to the conditioned data. The conditioned data and thus the SSP measurement range are matching the physical environment again. Due to calibration range mismatch, both the usable conditioned data range and calibration range are reduced by the Offset on opposite ends of those ranges. Therefore, the 10% sensor target margin during calibration is a good practice.

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6.4 Temperature Signal Correction

Temperature is measured either internally by the ZSSC3286, through an additional external element, or by means of a combination of the ZSSC3286 internal and external temperature sensing capabilities. Temperature correction contains both linear gain and offset terms as well as a second-order term to correct for any nonlinearities. For temperature, second-order compensation is always parabolic.

The correction equation terms are as follows:

		Valid Input Range
T	Corrected temperature sensor data	0x0 to 0xFFFFFF
T_Raw	Raw temperature reading after AZ correction	-(0x7FFFFF) to 0x7FFFFF
Gain_T	Gain coefficient for temperature	-(0x7FFFFF) to 0x7FFFFF
Offset_T	Offset coefficient for temperature	-(0x7FFFFF) to 0x7FFFFF
SOT_T	Second-order term for temperature source nonlinearity	-(0x7FFFFF) to 0x7FFFFF
T_shift	Shift for post-calibration/post-assembly offset compensation	-(0x7FFFFF) to 0x7FFFFF

The correction formula is best represented as a two-step process as follows:

Simplified:

$$Z_T = \frac{4 \times Gain\_T}{2^{23}} \times (T\_Raw + 4 \times Offset\_T) + 2^{23} \tag{43}$$

$$T = \frac{Z_T}{2^{23}} \times \left(\frac{4 \times SOT\_T}{2^{23}} \times Z_T + 2^{23} \right) \tag{44}$$

Note: Z_T and T are delimited to positive number range.

Complete:

$$Z_T = \left[\left[\frac{Gain\_T}{2^{21}} \times [T\_Raw + 4 \times Offset\_T]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{0}^{2^{25}-1} \tag{45}$$

$$T = \left[\left[\frac{Z_T}{2^{23}} \times \left[\left[\frac{SOT\_T}{2^{21}} \times Z_T \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + T\_shift \right]_{0}^{2^{24}-1} \tag{46}$$

The coefficient *T_shift* will be set automatically by the firmware if *ZeroAdjEna* in section 13.9.1 is enabled. Refer section 6.3 for further details about auto zero adjustment and handling of *T_shift*.

All raw data and compensation coefficients supplied to the formulas are required in 24-bit data format shown in Table 59 and Table 60.

Table 59. Data Format of Raw Temperature ADC Readings

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	-2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 60. Data Format of 24-bit SSC Coefficients for Temperature Compensation

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	0 = positive 1 = negative	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

The compensated result data is supplied in 24-bit data format as shown in Table 61.

Table 61. Data Format of Corrected Temperature SSC Results

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	2^0	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

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6.5 Bridge Output Scaling

The ZSSC3286 offers a linear rescaling function to amplify or compress a partial region of the sensor input range to the desired signal output range. Figure 42 shows the rescaling on an example where the 25% to 75% calibrated signal input range is mapped to the output range of 0% to 100%. The feature is intended for customers who need to separate product derivatives after a common sensor calibration step.

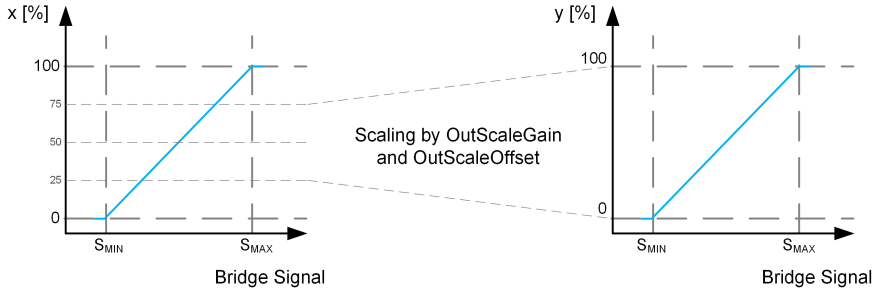

Figure 42. Example: Bridge Output Scaling Function for Scaling 25% - 75%, to final 0% - 100%

The rescaling feature applies the following formula to the SSC conditioned outputs of the main bridge sensor:

$$S_{Scaled} = \left[\frac{8 \times OutScaleGain}{2^{23}} \times (S + 8 \times OutScaleOffset)\right]_{0}^{2^{24}-1} \quad (47)$$

The rescaling equation terms are as follows:

		Valid Input Range
S_{Scaled}	Rescaled sensor signal	0x0 to 0xFFFFFF
S	Compensated sensor signal	0x0 to 0xFFFFFF
OutScaleGain	Raw temperature reading after AZ correction	-(0x7FFFFF) to 0x7FFFFF
OutScaleOffset	Gain coefficient for temperature	-(0x7FFFFF) to 0x7FFFFF

The Coefficients *OutScaleGain* and *OutScaleOffset* are stored in the CCP (Configuration and Calibration Page) of the ZSSC3286 in signed magnitude format. According to Table 62 *OutScaleGain* is limited to a maximum gain of 4 and the *OutScaleOffset* can vary from -1.5 to 0 related to the SSC result number range 0 to ~2.

Table 62. Examples for Bridge Output Scaling

Input Relative – x [%]		OutScaleGain		OutScaleOffset		Output Relative – y [%]	
		real	CCP Content (Decimal)	real	CCP Content (Decimal)		
0	50.0	2.000	2097152	0.0	0	0	100
0	33.3	3.003	3148876	0.0	0	0	100
0	25.0	4.000	4194304	0.0	0	0	100
25	50.0	4.000	4194304	-0.5	-524288	0	100
25	75.0	2.000	2097152	-0.5	-524288	0	100
50	100.0	2.000	2097152	-1.0	-1048576	0	100
75	100.0	4.000	4194304	-1.5	-1572864	0	100

Table 63 lists the mapping of CCP register content to output scaling coefficients.

Table 63. Data Format of Output Scaling Coefficients in CCP

Bit Number	23	22	21	20	19	...	1	0
Meaning, Weighting	0 = positive 1 = negative	2^2	2^1	2^0	2^{-1}	...	2^{-19}	2^{-20}

The GUI supports the calculation of *OutScaleGain* and *OutScaleOffset* based on provided relative input and output range specifications (Can be configured on the GUI tab Configure\Output Scaling).

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6.6 IIR Filter

The conditioned outputs of the two main sensor channels and the conditioned outputs of the temperature channels TCh1, TCh2 and TCh3 can be low pass filtered for noise reduction. Each channel is equipped with an independent configurable IIR Filter. The mathematical filter description is as follows:

$$IIR_{Out(0)} = \begin{cases} S_{Scaled(0)} & \text{for sensor channel} \\ T_0 & \text{for temperature channel} \end{cases} \tag{48}$$

$$IIR_{Out(i)} = \begin{cases} S_{Scaled(i-1)} & \text{for sensor} \\ T_{i-1} & \text{for temperature} \end{cases} + \left(\frac{Diff \times \left(\begin{cases} S_{Scaled(i)} & \text{for sensor} \\ T_i & \text{for temperature} \end{cases} - IIR_{Out(i-1)} \right)}{Avg} \right) \tag{49}$$

where:

$$Diff = FiltDiff + 1 \tag{50}$$

$$Avg = 2^{FiltAvg} \tag{51}$$

The IIR equation terms are as follows:

		Valid Input Range
IIR_{Out}	Output of IIR filter	0x0 to 0xFFFFFF
S_{Scaled}	Rescaled sensor signal	0x0 to 0xFFFFFF
T	Corrected temperature sensor data	0x0 to 0xFFFFFF
FiltDiff	Coefficient for differential coefficient stored in CCP	0x0 to 0x7
FiltAvg	Coefficient for average coefficient stored in CCP	0x0 to 0x7
Diff	Differential coefficient used for IIR filter	1 to 8
Avg	Average coefficient used for IIR filter	1 to 128

FiltDiff and *FiltAvg* represent the filter coefficients which are stored as unsigned 3-bit values per filter channel in IirFiltCoeffReg inside the CCP of ZSSC3286. They are determined by the GUI (Configure\Filter) depending on the filter Tau selections made by the user. For a stable system, the *Diff* ≤ *Avg* must be ensured.

The filter Tau can be calculated by:

$$\frac{Diff}{Avg} = \alpha \approx \frac{1}{\tau_{dig}} = \frac{\Delta T}{\tau_{ana}} \tag{52}$$

$$\tau_{dig} = -\frac{1}{\ln(1-\alpha)} \tag{53}$$

τ_{dig} is given in number of digital samples.

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6.7 Third Logic Channel Combination

The potentially pre-scaled and filtered IIR_{Out} for sensor channel 1 and 2 of the ZSSC3286 can be mathematically combined to calculate the output of a third logic channel TLC. The TLC channel is only available in the synchronized AFE mode which is enabled via the GUI menu Configure\AFE\Sequencer \AFE Selection and Configurability\selection: “AFE1+AFE2, config equally”.

The calculation result on TLC is available through serial interface read out. The digital output format is signed 32-bit (two’s complement), see Table 64. Outputting the TLC result via analog output is possible for subtraction and ratio. Division is readable via digital interfaces only.

The Third Logic Channel (TLC) can be configured via the GUI menu Configure\TLC menu.

TLC supports mathematical operation for subtraction, division and ratio. The operations will be executed based on TLC selection defined in *MathSbrAlgoSel.TlcOp*. The IIR_{Out_CH1} and IIR_{Out_CH2} for sensor channel 1 and 2 used in Equation 54 can be swapped by *MathSbrAlgoSel.TlcChOrder*.

$$TLC = \begin{cases} IIR_{Out\_CH1} - IIR_{Out\_CH2} & \text{for subtraction operation} \\ \hline \frac{IIR_{Out\_CH1}}{IIR_{Out\_CH2}} & \text{for division operation} \\ \hline \begin{cases} 1 & \text{if } IIR_{Out\_CH1} == IIR_{Out\_CH2} \\ \hline \frac{IIR_{Out\_CH1}}{IIR_{Out\_CH2}} & \text{if } IIR_{Out\_CH1} < IIR_{Out\_CH2} \\ \hline 2 - \frac{IIR_{Out\_CH2}}{IIR_{Out\_CH2}} & \text{else} \end{cases} & \text{for ratio operation} \end{cases} \quad (54)$$

Note: Division calculation can lead to math saturation, which is not suppressed by firmware.

Calibration of the sensor channels and respective output of IIR filter with IIR_{Out_CH1} and IIR_{Out_CH2} must still be done independently applying the single channel calibration routines.

Table 64. Data Format of Logic Output Channel *TLC* at Serial Interface

Bit Number	31	30	29	...	24	23	22	21	...	2	1	0
Meaning, Weighting	-2^8	2^7	2^6	...	2^1	2^0	2^{-1}	2^{-2}	...	2^{-21}	2^{-22}	2^{-23}

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7 Post Processing Options for Conditioned Sensor Signals

7.1 Signal Post Processing Flow Chart

Figure 43 shows the signal flow from conditioned data to individual output signals. All basis mathematical functions are described within the section 7.2, section 7.3, section 7.4, and section 7.5.

The signal path from AFE output data to conditioned data is described in section 6.2.

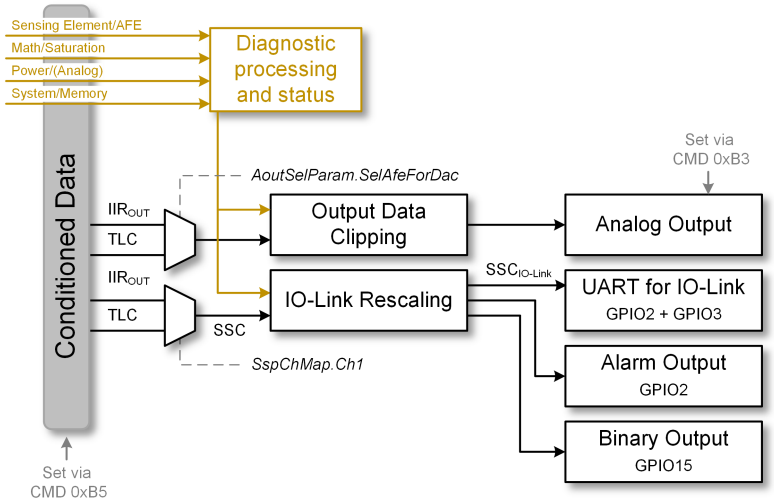

Figure 43. Sensor Signal Flow Chart from Input to Output

7.2 Output Data Clipping

The signaling of a diagnosis failure state can also be activated on the analog output AOUT via GUI tab Diagnostic\General. If the signalization of Diagnostic State at AOUT is enabled, discovered diagnostic failure states can be either mapped to the Upper or the Lower Diagnostic Range (UDR and LDR) of the output span (GUI tab Diagnostic\Sensor/AFE).

The boundaries of the upper and lower diagnostic ranges are configurable via the GUI tab Configure\Output Preprocess. They are typically set to 5% and 95% of the full scale output level but can be modified to the application needs.
To prevent false interpretation of very large or very low output signals, the conditioned data is clipped according to Figure 44 to fit into the remaining output range between UDR and LDR before it is forwarded to the AOUT output.

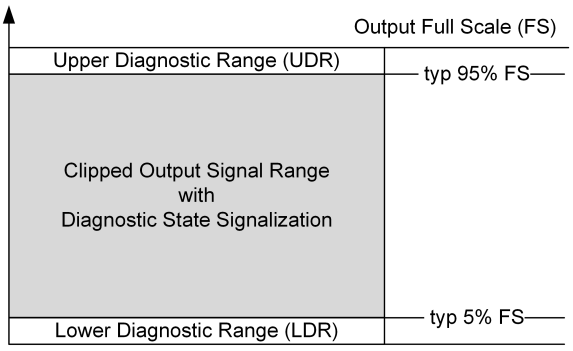

Figure 44. AOUT Output Ranges with Active Diagnostic State Signalization

Notes:
- There is no rescaling of the conditioned data performed at this stage.
  If rescaling of the conditioned data to the clipped output signal range is required, use the Bridge Output Scaling feature (see section 6.5) or use different target values during the SSC calibration process.
- UDR has higher priority than LDR.
  Each sensor and AFE diagnostic feature described in section 8.1 individually assigns either a UDR or LDR. This assignment necessitates an internal prioritization process when multiple malfunctions are detected.

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7.3 IO-Link Rescaling

The purpose of rescaling is to implement a simple algorithm for scaling and offsetting the 24-bit SSC corrected data so that it can be provided in SI Units as the IO-Link Smart Sensor Profile (SSP) process data requests. As described in section 10.2 the ZSSC3286 features SSP 4.1.1.

Therefore all 24-bit SSC corrected data is shifted to 32-bit domain and then compensated by the following compensation mathematics and Equation 55:

		Valid Input Range
SSC	Corrected 24-bit sensor signal selected for IO-Link Output	0x0 to 0xFFFFFF
$SSC_{IO\text{-}Link}$	Rescaled for IO-Link Output	-(0x7FFFFFFF) to 0x7FFFFFFF
$Gain_{Rescale}$	Gain term for IO-Link rescaling	-(0x7FFFFFFF) to 0x7FFFFFFF
$Offset_{Rescale}$	Offset term for IO-Link rescaling	-(0x7FFFFFFF) to 0x7FFFFFFF
$Offset_{Scalar}$	Offset shift for $Offset_{Rescale}$ parameter	0x0 to 0xFF

The IO-Link rescaling is supported by the GUI within the tab IO-Link\SSP Scaling.

All data and compensation coefficients supplied to the formulas are required in the 32-bit data format described in Table 65, Table 66, Table 67, Table 68, and Equation 55.

Table 65. Data Format of Corrected SSC Result

Bit Number	23	22	21	20	...	2	1	0
Meaning, Weighting	2^{0}	2^{-1}	2^{-2}	2^{-3}	...	2^{-21}	2^{-22}	2^{-23}

Table 66. Data Format of IO-Link rescaled Output for SSP 4.1.1

Bit Number	15	14	13	12	...	2	1	0
Meaning, Weighting	$-(2^{0})$	2^{-1}	2^{-2}	2^{-3}	...	2^{-13}	2^{-14}	2^{-15}

Table 67. Data Format of 32-bit $Gain_{Rescale}$ and $Offset_{Rescale}$ Coefficients

Bit Number	31	30	29	28	27	...	1	0
Meaning, Weighting	0 = positive 1 = negative	2^{2}	2^{1}	2^{0}	2^{-1}	...	2^{-27}	2^{-28}

Table 68. Data Format of 8-bit $Offset_{Scalar}$ Coefficient

Bit Number	7	6	5	4	3	2	1	0
Meaning, Weighting	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

$$SSC_{IO-Link} = \left(SSC \times 2^{8} \times Gain_{Rescale}\right) + \left(Offset_{Rescale} \times Offset_{Scalar}\right) \quad (55)$$

7.4 Alarm Function

In SIO mode, the pin UART TxD (GPIO2) can be assigned a binary ALARM signal. This ALARM signal is output on C/Q line of IO-Link via the PHY as TxEN is always active in SIO mode.

Any Sensor Switching Channel from the IO-Link SSP can be mapped to the ALARM function. The ALARM switching behavior thus is completely dependent on IO-Link Sensor Switching Channel configuration. The ALARM signal can be inverted before being output on pin UART TxD (GPIO2).

In Cyclic Mode, the ALARM signal will be constantly updated when new measurement results are available. In Command Mode, the last switching level is kept and output stays constantly. On Fallback from IO-Link COM Mode, the ALARM signal automatically will be output if the ALARM function is enabled in CCP. On WURQ, pin UART TxD automatically switches to IO-Link COM operation.

The activation and configuration of ALARM Function is done in CCP register 0x04 – IolMisc.

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7.5 Binary Output

The BINO pin (GPIO 15) can be configured as a binary output signal. This functionality is active in both SIO and IO-Link Cyclic Modes.

The switching behavior of the binary output signal is determined by the IO-Link Sensor Switching Channel configuration parameters. Additionally, the binary output signal can be inverted prior to output through the BINO pin (GPIO15).

Any Sensor Switching Channel from the IO-Link SSP can be mapped to the binary output function. The binary output switching behavior thus is completely dependent on IO-Link Sensor Switching Channel configuration. The binary output signal can be inverted before being output to pin BINO (GPIO15).

In Cyclic Mode, the binary output signal is continuously updated whenever new measurement results become available. In Command Mode, the output maintains the last switching level and remains constant.

When the binary output function is deactivated, the BINO pin (GPIO 15) enters a high-impedance state.

Configuration and activation of the binary output function are managed through the CCP register 0x04 – IolMisc.

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8 Sensor and System Diagnosis

The ZSSC3286 sensor and system diagnosis function can detect several false conditions on externally connected sensors and monitor long term gain and offset drifts of the analog front end. This makes the ZSSC3286 well suited for sensing applications that require increased system reliability as well as for predictive maintenance supervision done by the host system.

8.1 Sensor and AFE Diagnostic Features

The supported sensor and AFE diagnostic features are summarized in Table 69.

Table 69. Sensor and AFE Diagnosis Functions

Monitored Input or Component	Failure Category	Failure Condition [1]
Main sensor bridge 1	INP or INN open	INP to INN resistance >125kΩ
	INP or INN shorted	INP to INN resistance <170Ω
Main sensor bridge 2	INP or INN open	INP to INN resistance >125kΩ
	INP or INN shorted	INP to INN resistance <170Ω
Temperature sensor T1	Short to Top (TOP)	T1 to TOP resistance <500Ω
	Short to Bottom (BOT)	T1 to BOT resistance <500Ω
	Open	T1 resistance >2MΩ, 500kΩ, 100kΩ
Temperature sensor T2	Short to Top (TOP)	T2 to TOP resistance <500Ω
	Short to Bottom (BOT)	T2 to BOT resistance <500Ω
	Open	T2 resistance >2MΩ, 500kΩ, 100kΩ
Temperature sensor T3	Short to Top (TOP)	T3 to TOP resistance <500Ω
	Short to Bottom (BOT)	T3 to BOT resistance <500Ω
	Open	T3 resistance >2MΩ, 500kΩ, 100kΩ
CVC1 (capacitive sensor)	Leakage 1	Leakage measurement exceeds the defined tolerance
	Leakage 2	Leakage measurement exceeds the defined tolerance
CVC2 (capacitive sensor)	Leakage 1	Leakage measurement exceeds the defined tolerance
	Leakage 2	Leakage measurement exceeds the defined tolerance

1 Typical values. Further specifications are provided in Table 11.

For all active sensor inputs and AFEs, the checks can be enabled selectively on the GUI tab Diagnostic\Sensor/AFE.

To run single tests for sensor and AFE diagnosis features, 0xB4 command can be used which triggers a single measurement returning a pass or fail criteria as shown in Table 70. Complete update of all enabled sensor checks can be performed by the command 0xB2.

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Table 70. 0xB4 - Self Diagnostic Measurement Command

Command Code	Description	Return
0xB4 followed by 0x0XYY	**Self-Diagnostic Measure** for AFE1 and AFE2 • 0x0X ◦ AFE1: 0x00 ◦ AFE2: 0x01 • 0xYY - see below	2 Bytes
0xYY	**Measurement**	**Return**
0x05	External temperature sensor, T1, check short to top	0b0000_0000_0000_000X
0x06	External temperature sensor, T1, check short to bottom	0b0000_0000_0000_000X
0x07	External temperature sensor, T1, check open	0b0000_0000_0000_000X
0x0A	External temperature sensor, T2, check short to top	0b0000_0000_0000_000X
0x0B	External temperature sensor, T2, check short to bottom	0b0000_0000_0000_000X
0x0C	External temperature sensor, T2, check open	0b0000_0000_0000_000X
0x0F	External temperature sensor, T3 (pin GUARD), check short to top	0b0000_0000_0000_000X
0x10	External temperature sensor, T3 (pin GUARD), check short to bottom	0b0000_0000_0000_000X
0x11	External temperature sensor, T3 (pin GUARD), check open	0b0000_0000_0000_000X
0x1B	Main bridge sensor connection check open	0b0000_0000_0000_000X
0x1C	Main bridge sensor connection check short	0b0000_0000_0000_000X
0x29	CVC Leakage 1 (capacitive)	0b0000_0000_0000_000X
0x2A	CVC Leakage 2 (capacitive)	0b0000_0000_0000_000X

8.2 Sensor and System Diagnosis Status

All individual sensor and AFE diagnosis features are able to set an individual bit inside a Fault Memory.

Fault Memory is a nonvolatile memory that tracks all diagnosis bits until they are actively cleared. Clearing is possible only via ClearFaultMem (0xB9) command or a system reset. Thus before checking system diagnosis it is recommend to clear the fault memory. The fault memory can be read via RdFaultMem (0xB8) command. Reading the Fault Memory returns three words as shown in Table 71, Table 72, and Table 73. Updating the complete Fault Memory is possible via command 0xB2.

Any diagnosis listed in Table 71 and Table 72 additionally sets the Sensor Fault bit within the Status Byte. Similarly, any diagnosis listed in Table 73 sets the Saturation bit inside the Status Byte. The Status Byte is further explained in section 10.6.

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Table 71. Fault Memory - Word 0 - Bits 31:0

Bits	Description	Bits	Description
31 : 25	Reserved	11	AFE2 sensor signal range check: INP2
24	AFE2 temperature sensor shorted connection check → T3 – BOT shorted: R < R_{T_SHORT}	10	AFE2 sensor leakage check: INN2 to VSS
23	AFE2 temperature sensor shorted connection check → T3 – TOP shorted: R < R_{T_SHORT}	9	AFE2 sensor leakage check: INP2 to VSS
22	AFE2 temperature sensor broken connection check → T3 open: R > R_{T_OPEN}	8	AFE2 sensor shorted connection check → INP2 – INN2 shorted: R < R_{short}
21	AFE2 temperature sensor shorted connection check → T2 – BOT shorted: R < R_{T_SHORT}	7	AFE2 sensor broken connection check → INP2 or INN2 open: R > R_{broken}
20	AFE2 temperature sensor shorted connection check → T2 – TOP shorted: R < R_{T_SHORT}	6	AFE1 sensor signal range check: INN1
19	AFE2 temperature sensor broken connection check → T2 open: R > R_{T_OPEN}	5	AFE1 sensor signal range check: INP1
18	AFE1 temperature sensor shorted connection check → T1 – BOT shorted: R < R_{T_SHORT}	4	AFE1 sensor leakage check: INN1 to VSS
17	AFE1 temperature sensor shorted connection check → T1 – TOP shorted: R < R_{T_SHORT}	3	AFE1 sensor leakage check: INP1 to VSS
16	AFE1 temperature sensor broken connection check → T1 open: R > R_{T_OPEN}	2	AFE1 sensor shorted connection check → INP1 – INN1 shorted: R < R_{short}
15 : 13	Reserved	1	AFE1 sensor broken connection check → INP1 or INN1 open: R > R_{open}
12	AFE2 sensor signal range check: INN2	0	Reserved

Table 72. Fault Memory - Word 1 - Bits 31:0

Bits	Description
31 : 8	Reserved
7	CVC2 leakage 2
6	CVC2 leakage 1
5	CVC1 leakage 2
4	CVC1 leakage 1
3	AFE2 Offset Drift
2	AFE2 Gain Drift
1	AFE1 Offset Drift
0	AFE1 Gain Drift

Table 73. Fault Memory - Word 2 - Bits 31:0

Bits	Description
31 : 6	Reserved
5	SSC calculation unit OR raw output data saturation channel 3, temperature sensor data
4	SSC calculation unit channel 3, bridge sensor data
3	SSC calculation unit OR raw output data saturation channel 2, temperature sensor data
2	SSC calculation unit OR raw output data saturation channel 2, bridge sensor data
1	SSC calculation unit OR raw output data saturation channel 1, temperature sensor data
0	SSC calculation unit OR raw output data saturation channel 1, bridge sensor data

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9 Analog Output

The conditioned and post processed output data of one of the following channels can be made available as analog output signal at the Analog Output AOUT

- Sensor Channel 1
- Sensor Channel 2
- Third Logic Channel
- Temperature Channel 1
- Temperature Channel 2
- Temperature Channel 3

Depending on the configuration of the Analog Output Driver, two different output modes, (absolute voltage output and current mode output) are supported.

Note: When implementing the analog output functionality of the ZSSC3286, the RESN pin and the ”Restart the Device” command (0x8D) cannot be used for reset operations. In configurations utilizing the analog output, device reset must be performed exclusively through power cycling.

9.1 Analog Output Driver

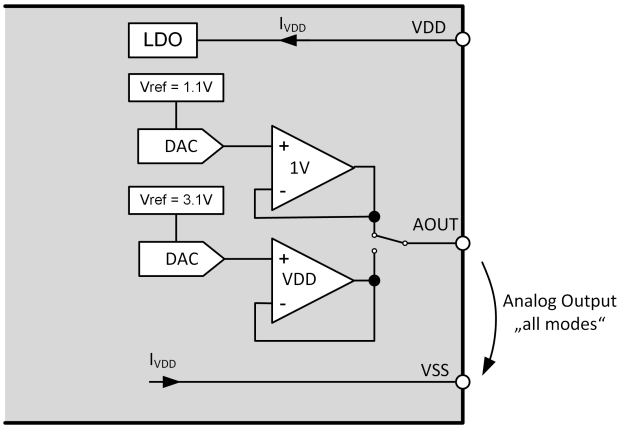

Figure 45. Block Schematic AOUT Driver

The Analog Output Driver features two distinct output buffers: one dedicated to a full-scale voltage of 1V, and another capable of handling full-scale voltages up to VDD. The following functional assignments apply:

- 1V buffer:
  - 1V absolute Voltage Mode
  - 3-wire Current Loop Mode
  - 5V absolute Voltage Mode (with external amplifier)
  - 10V absolute Voltage Mode (with external amplifier)
- VDD buffer:
  - 3V absolute Voltage Mode

Depending on the functional assignment and on the System Mode, the Analog Output Driver is set to the states shown in Table 74.

Table 74. Analog Output Driver States

System Mode	SIO Mode	IO-Link COM Mode
Disabled Mode	floating	floating
Absolute Voltage Mode	voltage following SSC value	0V
3-Wire Current Loop Mode	voltage for current following SSC value	voltage for minimum current (typ. 4mA)

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9.2 Negative Voltage Generation for AOUT

To support True-0V signals on the Analog Output (AOUT), the ZSSC3286 provides an option to externally supply a negative voltage rail for the AOUT buffer at VDDN. VDDN supply specifications are shown in Table 75. The external circuity must ensure to not generate a VDDN voltage of less than -0.5V to prevent latch-up conditions for the internal circuity.

The negative VDDN voltage can also be generated by an internal charge pump circuit. Its maximum current can be adjusted.

The activation of the internal charge pump at VDDN considerably increases the power consumption of the ZSSC3286 and needs to be carefully considered in applications where current consumption of the sensor device (sensing element + ZSSC3286) is a critical parameter. The VDDN charge pump can only be used for VDD ≥ 2.7V.

If no True-0V signals are required at AOUT, the user must disable the VDDN charge pump in the GUI and directly connect VDDN with VSS on PCB level.

The charge pump function is only available for Voltage Output mode. The charge pump circuit requires an external buffer capacitor C_{VDDN} and a Shottky Diode to work properly.

Table 75. Parameter Negative Voltage for AOUT

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
VDD_{CP}	VDD operating range of internal charge pump		2.7		5.5	V
VDDN	Negative voltage supply for analog output (AOUT)	Internally generated, requires activation of VDDN charge pump		$V_{ExtShottky}$		V
		Externally supplied	0	-0.3V	-0.5V	V
I_{VDDN}	Available charge pump load current	Programmable in 4 steps.			0.5	mA
					1	
					3	
					5	
I_{VDD}	Additional charge pump current consumption at VDD	0.5mA load current	0.5	4.5	5	mA
		1.0mA load current	1	9	10	
		3.0mA load current	3	15.5	17	
		5.0mA load current	5	25	30	
C_{VDDN}	Buffer capacitance at pin VDDN			1		µF
$V_{FW-Schottky}$	Forward voltage of external Shottky diode			0.3	0.5	V

9.3 Analog Output Configuration

9.3.1 1V Absolute Output Voltage Mode

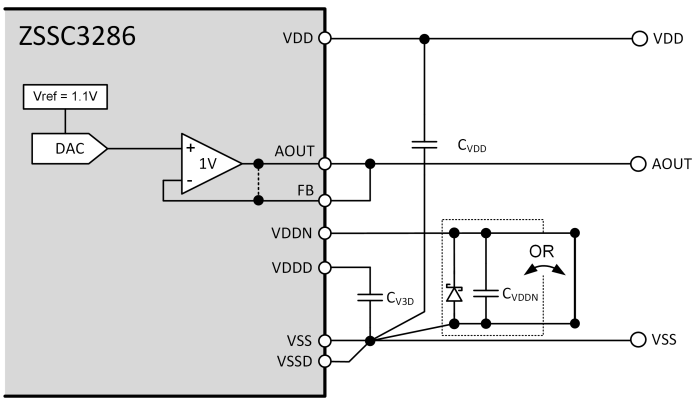

Figure 46. 1V Absolute Output Voltage Configuration at AOUT

The SSC output can be mapped to 0V to 1V voltage range with the application circuit shown in Figure 46 and activation of the 1V absolute Voltage Mode.

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The applied reference voltage for the AOUT DAC is generated from an internal factory calibrated bandgap source.

9.3.2 0V to 5V or 10V Absolute Voltage Mode – External Amplification

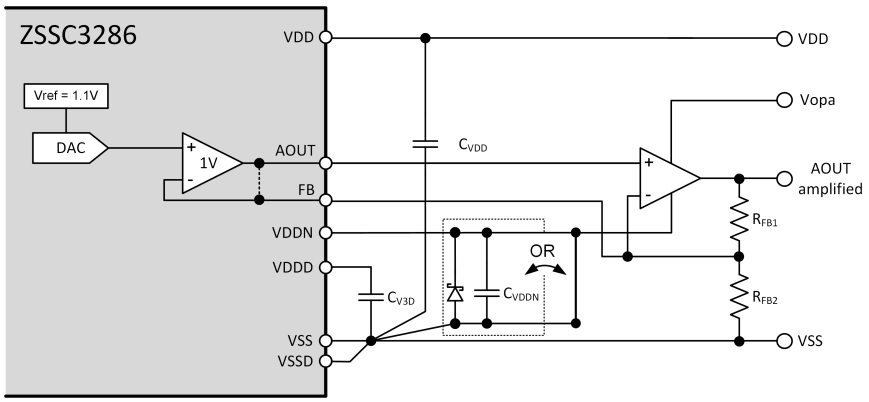

Figure 47. 5V or 10V Absolute Output Voltage Configuration at AOUT

Using an external operational amplifier, the 1V absolute voltage output can be scaled to higher voltages, for example 5V or 10V output. The application circuit is shown in Figure 47. The Feedback Pin FB should be connected to the inverting input of the external operational amplifier for better voltage accuracy. The external operational amplifier should be offset compensated. The external voltage amplification factor calculates as follows:

$$A = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \tag{56}$$

9.3.3 0V to 3V Absolute Voltage Mode

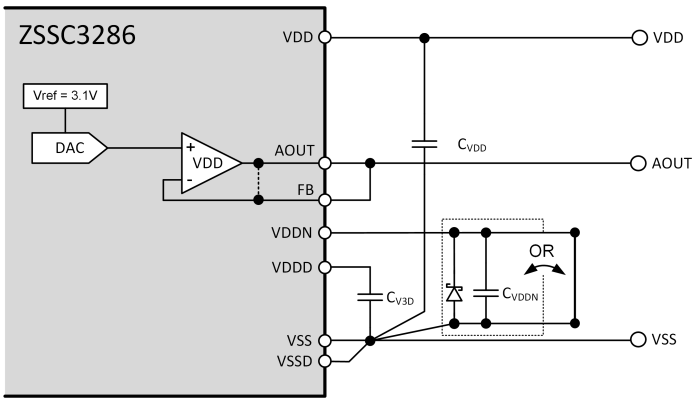

Figure 48. 3V Absolute Output Voltage Configuration at AOUT

The SSC output can be configured to map to a 0V to 3V voltage range by using the application circuit shown in Figure 48 and activation the 3V Absolute Voltage Mode. The reference voltage for the AOUT DAC is derived from an internally factory calibrated bandgap source.

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9.3.4 3-Wire Current Loop Mode

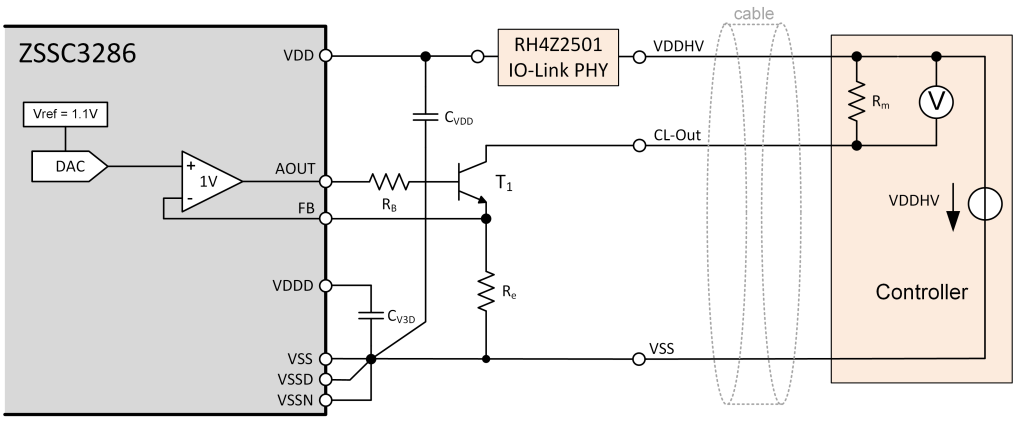

Figure 49. 3-wire NPN Current Loop Configuration at AOUT

Table 76. External Components in 3-Wire Current Loop Mode

Symbol	Parameter	Minimum	Typical	Maximum	Units
R_e	Emitter Resistor [1] for 4 to 20mA output		43	47 ± 5%	Ω
R_b	Base Resistor		4700		Ω
T_1	Bipolar Transistor	for example BCX56-16			N/A

[1] Using a low TC emitter resistor is recommended to minimize spurious temperature influence

Any SSC output can be mapped as input for 3-wire current loop application circuit shown in Figure 49 via *AoutSelParam.SelAfeForDac* and by activation of the 3-wire current loop mode within GUI.

The signal at 3-wire current loop is typically required to range from 4mA to 20mA. The available min/max signal current range at 3-wire current loop depends on the actual value of the external emitter resistor R_e.

3-wire current loop application uses the 1V output buffer. To compensate for tolerances of emitter resistor the ZSSC3286 offers an post output processing described in Equation 57.

$$AOUT_{DacValue} = CL3\_Offset + \frac{CL3\_Delta * SSC\_value}{2^{24}} \quad (57)$$

This equation uses the following parameters:

		Valid Input Range
$AOUT_{DacValue}$	Value that is set by the DAC and transferred to output buffer	0x0 to 0xFFFF
SSC_value	SSC corrected signal selected via *SelAfeForDac*	0x0 to 0xFFFFFF
CL3_Offset	Offset coefficient for post processing	0x0 to 0xFFFF
CL3_Delta	Gain coefficient for post processing	0x0 to 0xFFFF

Calculation of the *CL3_Offset* and *CL3_Delta* coefficients requires knowledge about the *1V_Code* stored inside the device info page. Device info page section can be read via command 0x84 (Read device info page in burst). The *1V_Code* represents the DAC code to set the output to 1V and is stored in bits 31:16 in register 0x9 and so reading is possible via 0x84 and 0x09 0x01.

Furthermore the calculation of the *CL3_Offset* and *CL3_Delta* coefficients requires setting two different DAC values via command 0xB3 (Direct DAC Stimulus). Those two DAC values reflect the minimum and maximum current loop current that will be used in end application. Those DAC values are calculated based on Equation 58 and Equation 59.

$$DAC\_Code_{IoutMin} = \frac{R_e * I_{CL3\_set\_min} * 1000\frac{mA}{A}}{1V} * 1V\_Code \quad (58)$$

$$DAC\_Code_{IoutMax} = \frac{R_e * I_{CL3\_set\_max} * 1000\frac{mA}{A}}{1V} * 1V\_Code \quad (59)$$

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Both equations use the following parameters:

		Valid Input Range
$DAC\_Code_{IoutMin}$	DAC code used by command 0xB3 setting minimum current loop current	0x0 to 0xFFFF
$DAC\_Code_{IoutMax}$	DAC code used by command 0xB3 setting maximum current loop current	0x0 to 0xFFFF
R_e	Selected value for emitter resistor in Ω	33 to 47
$I_{CL3\_set\_min}$	Minimum target current loop current in mA	typically 4
$I_{CL3\_set\_max}$	Maximum target current loop current in mA	typically 20
1V_Code	Code for 1V output buffer read from device info page	0x0 to 0xFFFF

After applying $DAC\_Code_{IoutMin}$ and $DAC\_Code_{IoutMax}$ the output current of current loop needs to be measured due to tolerance of emitter resistor. With those measured $I_{CL3\_meas\_max}$ and $I_{CL3\_meas\_min}$ currents the *CL3_Offset* and *CL3_Delta* coefficients can be calculated based on Equation 61 and Equation 60.

$$CL3\_Delta = \frac{I_{CL3\_set\_max} - I_{CL3\_set\_min}}{I_{CL3\_meas\_max} - I_{CL3\_meas\_min}} * (DAC\_Code_{IoutMax} - DAC\_Code_{IoutMin}) \quad (60)$$

$$CL3\_Offset = \frac{I_{CL3\_set\_min}}{I_{CL3\_meas\_min}} * DAC\_Code_{IoutMin} \quad (61)$$

Both equations use the following parameters:

		Valid Input Range
CL3_Offset	Offset coefficient for post processing (also used in Equation 57)	0x0 to 0xFFFF
CL3_Delta	Gain coefficient for post processing (also used in Equation 57)	0x0 to 0xFFFF
$I_{CL3\_set\_min}$	Minimum target current loop current in mA (same value as used in Equation 58)	typically 4
$I_{CL3\_set\_max}$	Maximum target current loop current in mA (same value as used in Equation 59)	typically 20
$I_{CL3\_meas\_min}$	Measured current loop current in mA for $I_{CL3\_set\_min}$	typically $I_{CL3\_set\_min}$ ± 10%
$I_{CL3\_meas\_max}$	Measured current loop current in mA for $I_{CL3\_set\_max}$	typically $I_{CL3\_set\_max}$ ± 10%

Finally the coefficients *CL3_Offset* and *CL3_Delta* needs to be stored in CCP.

Note: The sum of *CL3_Offset* and *CL3_Delta* must not exceed 0xFFFF to avoid oversteering of the 1V output buffer.

The GUI supports this post calibration option to calibrate the current loop current to the required absolute accuracy (currently only available via I2C).

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10 Digital Interfaces

10.1 Serial Interfaces

The ZSSC3286 features three digital interface protocols, shown in Table 77.

Table 77. Digital Interface Protocols

Protocol	Mode	Function
IO-Link (via UART)	Device	Sensor data read out, SSC configuration and calibration, FW Update
I2C	Slave	Sensor data read out, SSC configuration and calibration, FW Update
OWI	Master	Only for configuring the RH4Z2501 IO-Link PHY

Digital slave / device interfaces do not initiate data communication with the master system themselves but react on arbitrary received read/write requests from the master. I2C and IO-Link (COM mode) cannot be active at the same time.

After power up, the ZSSC3286 starts in SIO mode. In SIO mode, I2C communication is available. When a WURQ is received, the ZSSC3286 switches to IO-Link COM mode (refer to Figure 6).

10.2 UART (IO-Link)

The ZSSC3286 implements a UART interface for realization of IO-Link (SDCI) communication when connected to an IO-Link PHY (for example RH4Z2501, Reference 3, complying to the following standards:

- IO-Link Interface and System Specification V1.1.4 (Reference 1)
- IO-Link Common Profile Specification V1.2 (Reference 2)
- IO-Link Profile Smart Sensors 2nd Edition Specification V1.2
- IO-Link Profile BLOB Transfer & Firmware Update Specification V1.2
- IODD IO Device Description Specification V1.1.4

For connection to the PHY, the following pins are used:

- UART RxD
- UART TxD
- WU PHY
- TxEN PHY
- OWI /SS PHY

The ZSSC3286 only supports COM3 SDCI communication mode with transmission rate of 230.4kbit/s at a cycle time of 600µs. It features the Smart Sensor Profile (SSP) 4.1.1 (Profile-ID 0x0010, Process Data Structure PDI32.MSDC32_1). The ZSSC3286 supports the ISDUs listed in Table 78 to Table 99.

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10.2.1 Direct Parameter Page 1

Table 78. Communication Control

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x0000	0x1	MasterCommand	W	UIntegerT8 / (N/A)		x	x
	0x2	MasterCycleTime	RW	UIntegerT8 / (0x0)	Defined by IO-Link master	x	x
	0x3	MinCycleTime	R	UIntegerT8 / (0x6)	600µs minimum cycle time for SSP 4.1.1		x
	0x3	MinCycleTime	R	UIntegerT8 / (0x16)	2200µs minimum cycle time	x	
	0x4	M-sequenceCapability	R	UIntegerT8 / (0x2B)	• ISDU support bit set • OPERATE with 2 bytes of on-request data • PRE-OPERATE with 8 bytes of on-request data		x
	0x4	M-sequenceCapability	R	UIntegerT8 / (0x2D)	• ISDU support bit set • OPERATE with 8 bytes of on-request data • PRE-OPERATE with 8 bytes of on-request data	x	
	0x5	RevisionID	RW	UIntegerT8 / (0x11)	IO-Link protocol V1.1	x	x
	0x6	ProcessDataIn	R	UIntegerT8 / (0x83)	SSP 4.1.1: • SIO-bit not set (0) • 4 bytes of Process Data SIO-bit depends on ALARM feature setting.		x
	0x6	ProcessDataIn	R	UIntegerT8 / (0x0)	No Process Data in bootloader.	x	
	0x7	ProcessDataOut	R	UIntegerT8 / (0x0)	N/A for sensors, only for actuators	x	x

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Table 79. Identification

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x0000	0x8	VendorID 1 (Octet 1, MSB)	R	UIntegerT8 / (0x1)	Renesas vendor ID: 396 **Note:** Modifiable via CCP	x	x
	0x9	VendorID 2 (Octet 0, LSB)		UIntegerT8 / (0x8C)			
	0xA	DeviceID 1 (Octet 2, MSB)	RW	UIntegerT8 / (0x0)	Value 0x0 is not permitted. Values for active firmware and bootloader shall be different. Write attempt to this parameter has no effect (compatibility mode not supported). **Note:** Modifiable via CCP		x
	0xB	DeviceID 2 (Octet 1)		UIntegerT8 / (0x0)			
	0xC	DeviceID 3 (Octet 0, LSB)		UIntegerT8 / (0x1)			
	0xA	DeviceID 1 (Octet 2, MSB)	RW	UIntegerT8 / (0x0)	Value 0x0 is not permitted. Values for active firmware and bootloader shall be different. Write attempt to this parameter has no effect (compatibility mode not supported). **Note:** Modifiable via CCP	x	
	0xB	DeviceID 2 (Octet 1)		UIntegerT8 / (0x0)			
	0xC	DeviceID 3 (Octet 0, LSB)		UIntegerT8 / (0x2)			
	0xD	FunctionID 1 (MSB)	R	UIntegerT8 / (0x0)	value 0x0 by specification	x	x
	0xE	FunctionID 2 (LSB)					

10.2.2 System

Table 80. System

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x0002	0x0	SystemCommand	W	UIntegerT8 / (N/A)	See supported commands in Table 81, Table 82, Table 83, Table 84 and Table 85	x	x

The following SystemCommands listed in Table 81, Table 82, Table 83, Table 84, and Table 85 are supported:

Table 81. SystemCommands - Block Parametrization

System-Command	Name	Further info	IO-Link Operation Mode	
			Bootloader	COM Mode
0x01	ParamUploadStart			x
0x02	ParamUploadEnd			x
0x03	ParamDownloadStart			x
0x04	ParamDownloadEnd			x
0x05	ParamDownloadStore	Command used to finalize parametrization or to start Data Storage		x
0x06	ParamBreak			x

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Table 82. SystemCommands - Device Reset

System-Command	Name	Further info	IO-Link Operation Mode	
			Bootloader	COM Mode
0x80	DeviceReset		x	x
0x81	ApplicationReset	• reset of application-specific parameters • identification parameters stay unchanged • uninterrupted communication with Master		x
0x83	Back-to-box	• reset of application-specific parameters and identification parameters • Device must be power cycled to reestablish communication with Master		x

Note: Commands in Table 83 are only available if Locator function is enabled in CCP.

Table 83. SystemCommands - Locator

System-Command	Name	Further info	IO-Link Operation Mode	
			Bootloader	COM Mode
0x7E	LocatorStart	Locator sequence restarts in case this command is issued before completion of the previous locator sequence.		x
0x7F	LocatorStop	no effect if locator sequence is not in progress		x

Table 84. SystemCommands - Firmware Update

System-Command	Name	Further info	IO-Link Operation Mode	
			Bootloader	COM Mode
0x50	BM_UNLOCK_S	Start unlocking sequence		x
0x51	BM_UNLOCK_F	Unlocking command 1		x
0x52	BM_UNLOCK_T	Unlocking command 2		x
0x53	BM_ACTIVATE	Activates new firmware	x	

Table 85. SystemCommands - Teach

System-Command	Name	Further info	IO-Link Operation Mode	
			Bootloader	COM Mode
0x40	TeachApply			x
0x41	TeachSP1			x
0x42	TeachSP2			x
0x43	TeachSP1TP1			x
0x44	TeachSP1TP2			x
0x45	TeachSP2TP1			x
0x46	TeachSP12TP2			x
0x47	TeachSP1Start			x
0x48	TeachSP1Stop			x
0x49	TeachSP2Start			x
0x4A	TeachSP2Stop			x
0x4F	TeachCancel			x

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Table 86. DataStorageIndex

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x0003	0x1	DS_Command	RW	UIntegerT8 / (N/A)			x
	0x2	State_Property	R	UIntegerT32 / (N/A)			x
	0x3	Data_Storage_Size	R	UIntegerT32 / (N/A)	sum of the size of all parameters plus 4 bytes per parameter		x
	0x4	Parameter_Checksum	R	UIntegerT32 / (N/A)			x
	0x5	Index_List	R	UIntegerT8[N] / (N/A)	N = (parameter count x 3) + 2 index list contains three bytes for each ISDU parameter that is handled by the data storage mechanism: • upper 8bit of ISDU index • lower 8bit of ISDU index • subindex (usually 0x0) The index list ends with a termination marker of two zero bytes. It does not cover all parameters that are part of the parameter page structure. The index list is fixed for any specific DeviceID.		x

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Note: Table 87 column “ISDU Subindex” commands are not directly accessible. All parameter values within the ISDU Index are returned when sending command containing the ISDU Index with Subindex 0x0.

Table 87. ProfileCharacteristic

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x000D	0x1	SSP: Measuring and Switching Sensor, 1 channel	R	UIntegerT16 / (0x10)	SSP 4.1.1		x
	0x1	BLOB transfer	R	UIntegerT16 / (0x30)	BLOB transfer is used for CCP update.	x	
	0x2	Firmware Update Profile	R	UIntegerT16 / (0x31)		x	x
	0x3	Identification and Diagnosis Profile	R	UIntegerT16 / (0x4000)			x
	0x4	Two Value Teach Function Class	R	UIntegerT16 / (0x8011)			x
	0x5	Dynamic Teach Function Class	R	UIntegerT16 / (0x8012)			x
	0x6	Object Detection Function Class or Quantity Detection Function Class	R	UIntegerT16 / (0x8013) or UIntegerT16 / (0x8014)	Switching Scheme configured via CCP **Note:** Modifiable via CCP (default: quantity detection)		x
	0x7	Locator Function Class	R	UIntegerT16 / (0x8101)	Provides visual recognition of the Device **Note:** Subindex available only if Locator Function is enabled in CCP.		x

Table 88. PDInputDescriptor

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0xE	0x0	SystemCommand	W	UIntegerT8 / (N/A)	SSP 4.1.1: Describes the PDI32.MSDC32_1 layout (one field of size 32bit, starting at offset 0x0).	x	x

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10.2.3 Identification

Table 89. Identification

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x0010	0x0	VendorName	R	StringT48 / (”To be filled by Renesas customer”)	Length of parameters may differ from specification in Reference 1 and Reference 2. **Note:** Modifiable via CCP.	x	x
0x0011	0x0	VendorText	R	StringT48 / (”To be filled by Renesas customer”)			x
0x0012	0x0	ProductName	R	StringT32 / (”To be filled by Renesas customer”)		x	x
0x0013	0x0	ProductID	R	StringT32 / (”To be filled”)			x
0x0014	0x0	ProductText	R	StringT48 / (”To be filled by Renesas customer”)			x
0x0015	0x0	SerialNumber	R	StringT16 / (”To be filled”)			x
0x0016	0x0	HardwareRevision	R	StringT16 / (”To be filled”)		x	x
0x0017	0x0	FirmwareRevision	R	StringT32 / ([Renesas application version])	Contains the ZSSC3286 Renesas application release version. Length of parameter differs from specification in Reference 1 and Reference 2		x
0x0017	0x0	FirmwareRevision	R	StringT32 / ([Bootloader version])	Contains the ZSSC3286 bootloader release version. Length of parameter differs from specification in Reference 1 and Reference 2	x	
0x0018	0x0	ApplicationSpecificTag	RW	StringT32 / (”***”)			x
0x0019	0x0	FunctionTag	RW	StringT32 / (”***”)			x
0x001A	0x0	LocationTag	RW	StringT32 / (”***”)			x

10.2.4 Diagnosis

Table 90. Diagnosis

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x0020	0x0	ErrorCount	R	UIntegerT16 / (0x0)			x
0x0024	0x0	DeviceStatus	R	UIntegerT8 / (0x0			x
0x0025	0x0	DetailedDeviceStatus	R	OctetStringT3 / (0x0)			x

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10.2.5 Process Data

Note: Table 91 column “ISDU Subindex” commands are not directly accessible. All parameter values within the ISDU Index are returned when sending command containing the ISDU Index with Subindex 0x0.

Table 91. Process Data

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x0028	0x1	Measurement value	R	IntegerT16 / (0x0)			x
	0x2	Scale	R	IntegerT8 / (0x0)			x
	0x3	SSC1.1	R	BooleanT / (0x0)	SSC means Sensor Switching Channel in this occasion		x
	0x4	SSC1.2	R	BooleanT / (0x0)			x

10.2.6 BLOB Transfer and Firmware Update

Table 92. BLOB Transfer

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x0031	0x0	BLOB_ID	R	IntegerT16 / (N/A)	BLOB mechanism used for FW and CCP update volatile values used for BLOB transfer	x	
0x0032	0x0	BLOB_CH	RW	variable / (N/A)		x	

Table 93. Firmware Update

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x43BD	0x0	FW-Password	W	StringT16 / (empty string)	no password set by default **Note:** Modifiable via CCP		x
0x43BE	0x0	HW ID Key	R	StringT16 / (”TO BE FILLED”)	**Note:** Modifiable via CCP	x	x
0x43BF	0x0	BootmodeStatus	R	UIntegerT8 / (0x0)			x
0x43BF	0x0	BootmodeStatus	R	UIntegerT8 / (0x1)		x	

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10.2.7 ISDU - Smart Sensor Profile (SSP)

Note: Table 94 column “ISDU Subindex” for ISDU Index 0x3B commands are not directly accessible. All parameter values within the ISDU Index are returned when sending command containing the ISDU Index with Subindex 0x0.

Table 94. Teach

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x003A	0x0	TeachSelect	RW	UIntegerT8 / (0x1)			x
0x003B	0x1	State	R	UIntegerT4 / (0x0)	Teach Result		x
	0x2	Flag SP1 TP1	R	BooleanT / (0x0)			
	0x3	Flag SP1 TP2	R	BooleanT / (0x0)			
	0x4	Flag SP2 TP1	R	BooleanT / (0x0)			
	0x5	Flag SP2 TP2	R	BooleanT / (0x0)			

Table 95. SSP 4.1.1: SSC1.1 Param (Sensor Switching Channel)

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x003C	0x1	Setpoint 1	RW	IntegerT32 / (0x0)	switching channel deactivated by default		x
	0x2	Setpoint 2	RW	IntegerT32 / (0x0)			
0x003D	0x1	Logic	RW	UIntegerT8 / (0x0)	SSC1.1Config (Sensor Switching Channel)		x
	0x2	Mode	RW	UIntegerT8 / (0x0)			
	0x3	Hyst	RW	IntegerT32 / (0x0)			

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Table 96. SSP 4.1.1: SSC1.2 Param (Sensor Switching Channel)

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x003E	0x1	Setpoint 1	RW	IntegerT32 / (0x0)	not used by default		x
	0x2	Setpoint 2	RW	IntegerT32 / (0x0)			
0x003F	0x1	Logic	RW	UIntegerT8 / (0x0)	SSC1.2Config		x
	0x2	Mode	RW	UIntegerT8 / (0x0)			
	0x3	Hyst	RW	IntegerT32 / (0x0)			

Note: Table 97 column “ISDU Subindex” commands are not directly accessible. All parameter values within the ISDU Index are returned when sending command containing the ISDU Index with Subindex 0x0.

Table 97. SSP 4.1.1: MDC1Descr

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x4080	0x1	LowerValue	R	IntegerT32 / (0xFFFF8300)	sign extended to 32bit **Note:** Modifiable via CCP.		x
	0x2	UpperValue	R	IntegerT32 / (0x7D00)	**Note:** Modifiable via CCP.		
	0x3	UnitCode	R	UIntegerT16 / (0d1130)	corresponds to unit kPa by default **Note:** Modifiable via CCP.		
	0x4	Scale	R	IntegerT8 / (0d3)			

10.2.8 ISDU - Vendor specific

Table 98. CCP Handling

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x0200	0x0	CcpState	R	UIntegerT8 / (0x1)	• 0x0: CCP invalid • 0x1: CCP valid	x	
0x0201	0x0	CcpPassword	W	UIntegerT32 / (0xFFFFFFFF)	If password is other than 0xFFFFFFFF, it must be written before access to CCP is possible. Shall not appear in IODD. **Note:** Modifiable via CCP	x	x

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Table 99. HiddenCommand Interpreter

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x0300	0x0	Hidden Command	W	OctetStringT5 / N/A	HiddenCommand of variable length with payload. Shall not appear in IODD. See section 10.7 for details		x
0x0301	0x0	Hidden Command Response	R	OctetString T129 / (0x0)	HiddenCommandResponse of variable length with Payload. Contains response to latest issued HiddenCommand. Shall not appear in IODD. See section 10.7 for details		x

10.2.9 ISDU triggered Zero Adjustment

ZeroAdjEna enables Zero Adjustment feature described in section 6.3 and additional IO-Link ISDUs as described in Table 100. The ISDUs support the following functionality:

- ZeroAdjustment Sets a new *Offset* by performing a measurement and comparing to Reference Value. If calculated *Offset* is within Offset Window, it will be set as new *Offset* in parameter page.
- GetZeroAdjustment Reads the current *Offset*.
- ClearZeroAdjustment Resets the current *Offset* to zero.

Note: Zero Adjustment Offsets are cleared upon Back-to-Box ISDU execution.

Each ISDU is associated with a Subindex that specifies the MDC channel to which the ISDU applies. Subindexes are defined for MDC1 through MDC4. In SSP4.1.1, only subindex 0x0 (MDC1) is supported.

The ISDUs will return an error when:

- Third Logic Channel (TLC) is mapped to MDC
- The calculated *Offset* falls outside the Offset Window

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Table 100. Zero Adjustment ISDUs

ISDU Index	ISDU Subindex	Name	Access	Datatype / (Default Value)	Further Info	IO-Link Operation Mode	
						Bootloader	COM Mode (Active Firmware)
0x0400	0	MDC1 - ZeroAdjustment	W	N/A	Executes the Zero Adjustment Routine to define new Offset for. PAR_VALOUTOFRNG: Error Code - Offset is outside Window FUNC_NOTAVAIL: Error Code if the feature is not enabled or TLC is mapped to MDC SUBIDX_NOTAVAIL: Error Code - subindex other than zero		x
0x0401	0	MDC1 - GetZeroAdjustment	R	IntegerT32 / (0x0)	Returns current scaled IO-Link Process Data value (MDC value with applied Scale). FUNC_NOTAVAIL: Error Code if the feature is not enabled or TLC is mapped to MDC		x
0x0402	0	MDC1 - ClearZeroAdjustment	W	N/A	Resets the current Offset to 0. FUNC_NOTAVAIL: Error Code if the feature is not enabled or TLC is mapped to MDC SUBIDX_NOTAVAIL: Error Code - subindex other than zero		x

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10.3 GPIO triggered Zero Adjustment

ZeroAdjEna enables Zero Adjustment feature described in section 6.3, Zero Adjustment ISDUs that are described in section 10.2.9, and allows enabling the option for Zero Adjustment Trigger (ZAT) via a separate GPIO using *Gpio14Func*.

Enabled ZAT via GPIO option configured via *Gpio14Func* will enable the internal weak pull-up current on the ZAT pin. The operation mode for the ZAT GPIO must be configured inside the CCP according to section 13.17.6. Those adjustments are explained in Figure 50 and include:

- ZAT Trigger Polarity (rising or falling)
- ZAT Channel Selection (all channels, MDC1, MDC2, MDC3, or MDC4)
- ZAT Trigger Mode (Disabled, SIO mode, COM mode, or SIO and COM mode)

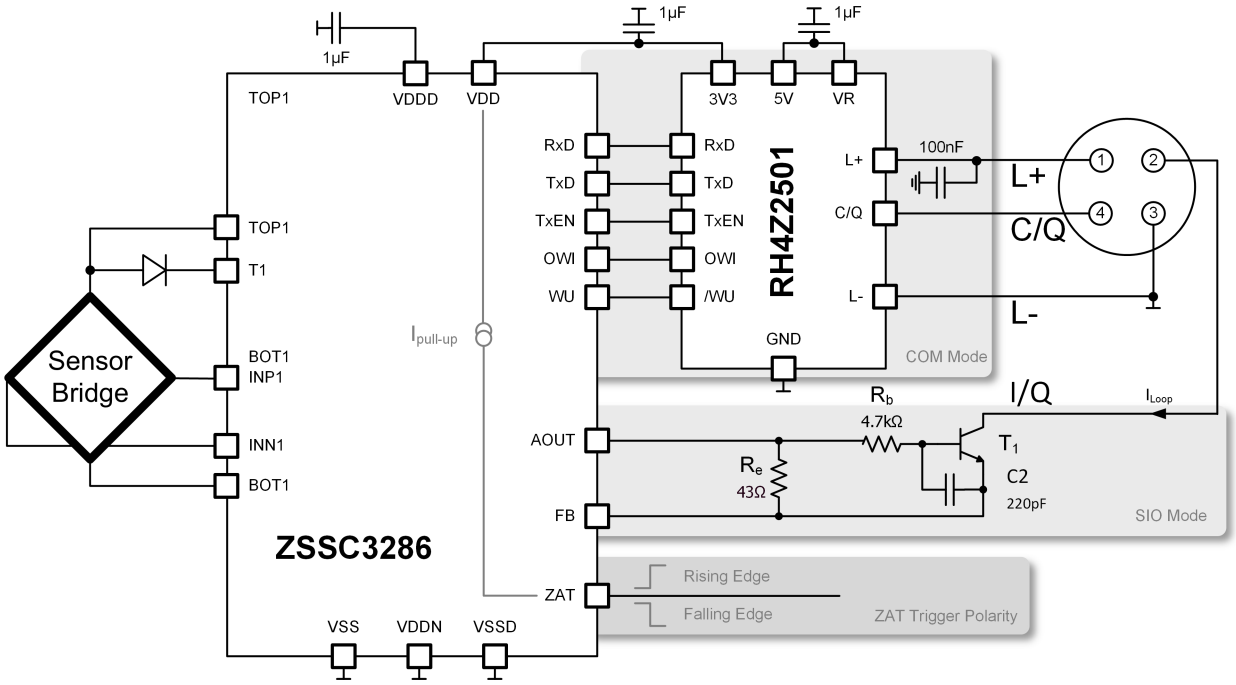

Figure 50. Zero Adjustment Trigger via GPIO

10.4 I2C

The ZSSC3286 supports I2C communication in Standard Mode, Fast Mode and Fast Mode+ on I2C SCL and I2C SDA pins. The I2C interface is listening to receive a telegram after system startup and whenever no IO-Link connection has been established.

I2C communication mode is selected and locked after I2C address match was passed and the first 8-bit of telegram data were received.

Table 101. I2C Interface Parameter

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
SlvAddr	I2C slave address	ZSSC3286 delivery default		0x3C		
f_{SCL} Interface	Clock	I2C Mode	0.1		1.0	MHz
D_{I2C} Duty	Cycle		33	–	50	%

Timing and protocol details of the I2C communication in Standard Mode, Fast Mode, and Fast Mode+ are given in I2C-Bus Specification, Rev.6, UM10204. SCL clock stretching is not supported by the ZSSC3286.

Note: When using third party tools for configuring the ZSSC3286 via I2C, it is recommended to wait at least 100ms after power up before sending I2C commands to ensure a stable communication.

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In I2C Mode, each command request follows the structure shown in Figure 51. Only the number of data bytes needed by the command must be sent. See Table 105 for available commands.

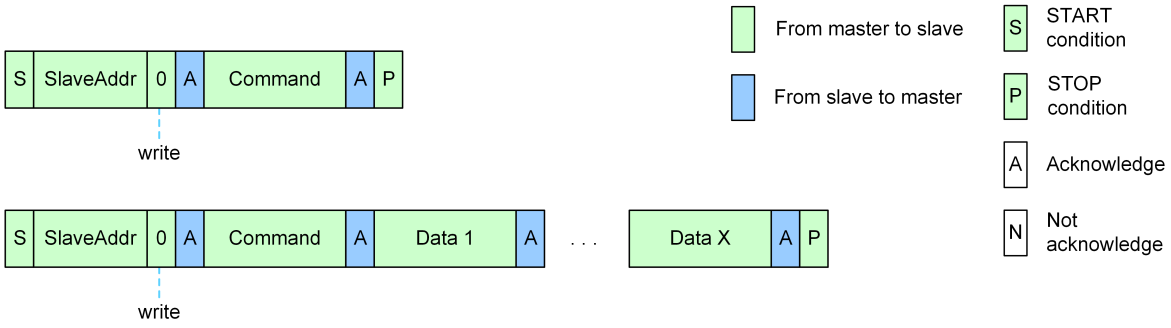

Figure 51. I2C Command Request

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Different available options for a response request are shown in Figure 52.

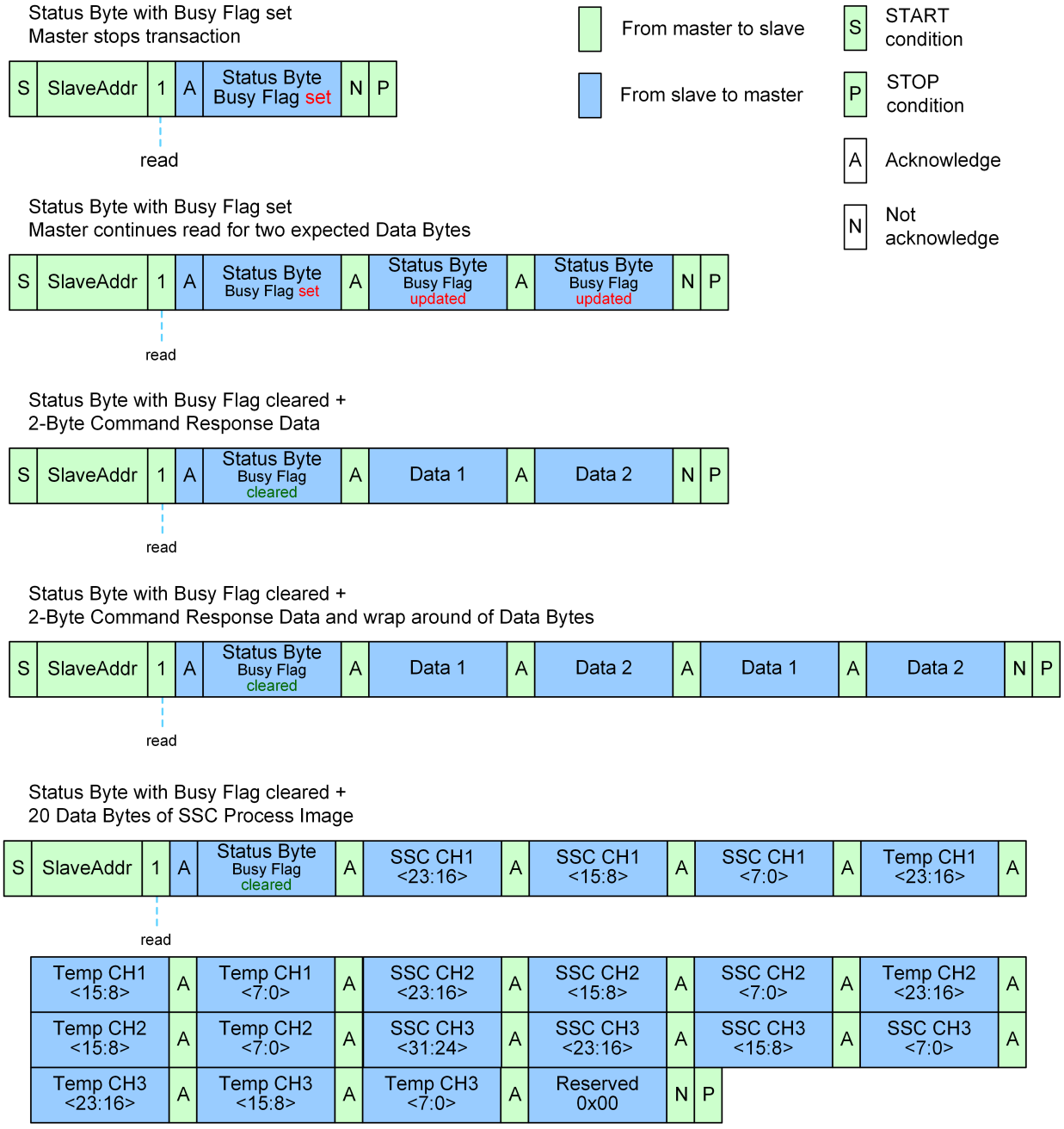

Figure 52. I2C Response Request

10.5 OWI

The ZSSC3286 implements an OWI Master Interface solely used for configuring the RH4Z2501 IO-Link PHY. Register values are taken from PhyCfg1 Register. Refer to Memory Layout (section 13) for configuration options of the RH4Z2501. Refer to Application Notes (section 14.2 and section 14.3) for implementation recommendations.

The RH4Z2501 registers are configured with default values (Reference 3) in the default state of the ZSSC3286. If the IO-Link application requires different register settings for a successful connection, the configuration of the CCP register must be done in advance via I2C. Incorrect configuration may lead to inability to connect via IO-Link.

If the ZSSC3286 starts in bootloader after power up, for example if firmware update fails, the RH4Z2501 registers are not set by the ZSSC3286 and contain default values. This may prevent an IO-Link connection if different values are needed. When switching from TFW (active firmware) to bootloader without a power cycle, the RH4Z2501 registers stay configured as set in CCP.

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10.6 Command / Response Format

All commands follow the same command request (Table 102) format. Command response format will differ slightly for I2C and IO-Link communication according to (Table 103) and (Table 104). The number of data bytes which need to follow the command byte in the command request are returned after the Status Byte in command response, assuming the command execution was completed, is specific to the command code.

Table 102. Command Request Format

Command	Command Byte								Data Bytes
	7	6	5	4	3	2	1	0	
Valid Command	8-bit command								[Data Bytes]

Table 103. I2C Command Response Format

Command	Command Byte								Data Bytes
	7	6	5		4	3	2	1	0	
Previously received command in execution, response pending, New command not accepted, retry later	Telegram Error Flag	Power Supply OK	Busy Flag	1	SSC Mode 00: Command Mode 01: Cyclic Mode 10: Sleep Mode 11: Boot/Diagnosis Mode		Memory Error	Sensor Connection Fault	Saturation[1]	NONE
Command successfully processed				0						[Data Bytes]

1 Cleared before each command execution except for 0xA9 (Start Command Mode).

Table 104. IO-Link Command Response Format

Command	Command Byte								Data Bytes
	7	6	5	4	3	2	1	0	
Previously received command in execution, response pending, New command not accepted, retry later	Reserved (always 0)							Saturation (in commands 0xA7; 0xB2)[1]	NONE
Command successfully processed									[Data Bytes]

1 Cleared before each command execution except for 0xA9 (Start Command Mode).

10.7 Command Interpreter

The availability of commands in Table 105 depends on the active main operating mode (Command or Cyclic Mode) and the current connection mode (I2C or IO-Link COM).

Commands available in IO-Link are called Hidden Commands. Except for commands related to FW Update functionality, the commands are for configuration and calibration purposes and are not required in final product application.

Some commands require an additional argument for successful command execution. If an argument error or missing argument appears, the current command is not executed. For IO-Link, a failure is indicated in the error response. For I2C, no error response is sent.

The commands available using IO-Link are called Hidden Commands. It is required to send commands via ISDU index 0x0300 (subindex 0x0) for writing and index 0x0301 (subindex 0x0) for reading the response. Reading the response requires sending an ISDU write command with the respective command code before sending an ISDU read command, see section 10.2.

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Table 105: Command List

Command Code (Byte)	Return (after Status Byte)	Description	Command Available in		
			Command Mode	Cyclic Mode	Bootloader
0x82 followed by 0xXX + 0xWW	0xWW × 4 bytes	**Read configuration data in burst** Reads content of Configuration and Calibration Page (CCP) in burst mode: • 0xXX selects the 32-bit word in CCP which is read first • 0xWW defines the number of words which is read from output memory **Note:** Maximum supported 0xWW is 0x20 **Note:** Before sending this command via IO-Link, set CCP Password must be sent via ISDU 0x0201.	I2C IO-Link	IO-Link	
0x83 followed by 0xXXYY + Data bytes (multiple of 4)	1 byte (ACK / NACK)	**Send CCP Update Chunk** Sends a data chunk during CCP Update • 0xXXYY - chunk counter • Data bytes - chunk fixed to size of 128 bytes **Note:** CCP Update via I2C is not protected by CCP Password mechanism.			I2C
0x84 followed by 0xXX + 0xWW	0xWW × 4 bytes	**Read device info page in burst** Reads device info page in burst mode : • 0xXX selects the word in InfoPage which is read first • 0xWW defines the number of words which is read from output memory **Note:** Maximum supported 0xXX is 0x1F **Note:** Maximum supported 0xWW is 0x20 **Note:** If 0xXX + 0xWW is > 0x20, the command fails.	I2C IO-Link	IO-Link	
0x89	4 bytes (CCP version with PID)	**Read expected CCP Version**	I2C IO-Link	IO-Link	
0x8A	2 bytes	**Read chip revision** Returns 0x0003	I2C IO-Link	IO-Link	I2C
0x8B	3 bytes (Bootloader Version)	**Read Bootloader Version**	I2C		I2C
0x8C	N/A (Execution jumps directly to the FW update routines)	**Start Firmware Update** Triggers Firmware update procedure **Note:** This command is designed exclusively for use with the ZSSC3286 GUI (see section 11)	I2C		
	1 byte (ACK / NACK)	**Send Firmware Update Chunk** Sends a data chunk during Firmware Update • 0xXXYY - chunk counter • Data bytes - chunk fixed to size of 128 bytes			I2C
0x8D	N/A (Device is immediately restarted)	**Restart the Device**	I2C		I2C
0x8E	8 bytes (APP Firmware Version)	**Read Application Firmware Version**	I2C		

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Table 105: Command List (Continued)

Command Code (Byte)	Return (after Status Byte)	Description	Command Available in		
			Command Mode	Cyclic Mode	Bootloader
0xA7 followed by 0xXX + 0xYY	20 bytes (Raw data)	**Snapshot calibration all sensors** [1] Returns unconditioned raw sensor and temperature data of all AFE channels that are activated in CCP. Other auxiliary measurement tasks will be excluded within the execution of this command. • 0xXX minimum average count for AFE1 data • 0xYY minimum average count for AFE2 data 0xXX and 0xYY must be in range 1 to 32 (=0x20). ”Minimum average count” refers to the minimum number of measurement tasks executed within a single measurement cycle. These typically include single temperature or auto-zero measurement tasks. As a result, primary measurements such as SM+ and SM- can be performed more frequently. The output data format is as follows: • Raw Data Bridge Sensor1 (24-bit) • Raw Data Temperature Channel1 (24-bit) • Raw Data Bridge Sensor2 (24-bit) • Raw Data Temperature Channel2 (24-bit) • 0x00000000 (4 bytes 0x0) (32-bit) • Raw Data Temperature Channel3 (24-bit) • 0x00 (1 byte 0x0) (8-bit)	I2C IO-Link		
0xA9	N/A	**Start Command Mode** Exit Cyclic Mode and transition to Command Mode	I2C IO-Link	I2C IO-Link	
0xAB	N/A	**Start Cyclic Mode** Enter Cyclic Mode based on configuration in Shadow RAM: continuous measurement cycles, SSC corrections, and automatic, continuous digital and/or analog output updates	I2C IO-Link	IO-Link	
0xB2 followed by data (0x0000 to 0xFFFF)	N/A	**Update diagnosis status** Executes all activated sensor and system diagnosis checks	I2C IO-Link		
0xB3 followed by data (0x0000 to 0xFFFF)	N/A	**Direct DAC Stimulus** Set the DAC output register with the data in the command and enable/output the respective analog signal through AOUT (according to the AOUT_setup)	I2C		
0xB4 followed by 0x0X + 0xYY	2 bytes	**Self-diagnostic measure** for AFE1 and AFE2 Parameter 0x0X: • AFE1: 0x00 • AFE2: 0x01 • Parameter 0xYY See description in Table 70	I2C IO-Link		
0xB5 followed by 0xXX 0xYY 0xYY 0xYY	N/A	**Direct linear stimulus of analog output path** Stimulates the output path, linear relation between input data and pin output. Parameter 0xXX - Output Selection: • 0: reserved • 1: AOUT • 2: reserved • 3: reserved Parameter 0xYYYYYY – Output Value: • 24bit data value for output, unsigned integer (as SSC value format) • assigned output is static (the output can be switched off by the RESN pin, POR, or a change in the main operating mode) **Note:** The following workflow for the given command must be ensured: • Start Command Mode (0xA9) • Set Direct linear stimulus of output path (0xB5) • Reset the device	I2C IO-Link		

Continued on next page

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Table 105: Command List (Continued)

Command Code (Byte)	Return (after Status Byte)	Description	Command Available in		
			Command Mode	Cyclic Mode	Bootloader
0xB8	12 bytes (diagnostic result data)	**Read fault memory** Responds with the detailed fault-memory status (see section 8)	I2C IO-Link	IO-Link	
0xB9	N/A	**Reset fault memory** Resets the contents of the fault memory to 0x0	I2C IO-Link	IO-Link	
0xC0	N/A	**Store Factory Settings** Stores parameters for restoring via SystemCommands “Back-to-box” and “ApplicationReset”	IO-Link	IO-Link	

1 These commands can be used to conduct a measurement without SSC conditioning, for example during the smart sensor calibration procedure. No digital correction is performed on the measurement result. The setup and configuration for the raw measurement is the content in the shadow registers that is automatically loaded from the NVM during power-on.

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11 Firmware Update

The ZSSC3286 offers a firmware update function via IO-Link and via I2C interface for Renesas provided application firmware. Current firmware version can be read via command 0x8E (Read Application Firmware Version). IO-Link uses the BLOB transfer mechanism to download the IOLFW update file to the device.
Figure 53 shows the high-level firmware update flow. After Initiating the firmware update, the device switches to bootloader mode. After the data is successfully transferred, the device is restarted.

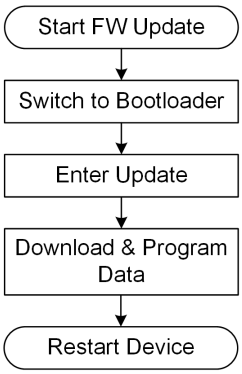

Figure 53. High-level Firmware Update Flow

The Firmware Update access via IO-Link can be protected with the firmware password (FwPassword described in section 13.26), as shown in Figure 54. If the FW-Password is other than an empty String, it must be entered via ISDU Index 0x43BD in IO-Link COM mode before starting Firmware Update. Otherwise, it prevents the device from entering bootloader mode and an error message is sent.

Note: The Firmware Update mechanism via I2C ignores the FW-Password protection.

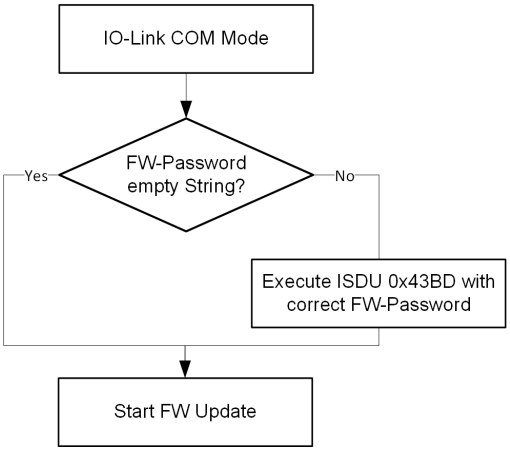

Figure 54. FW-Password Mechanism for Firmware Update

A firmware update is meant to be executed exclusively via the ZSSC3286 GUI and not by third party tools. Since a firmware update technically can be done via third party IO-Link tools, a firmware password should be set to prevent unauthorized firmware updates. It can be initiated at the FW UPDATE tab, where the respective new firmware file can be selected, and the update process can be triggered.

Note: Ensure a stable power supply during update. Power loss during update may cause corruption of the device.

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12 CCP Update

The ZSSC3286 offers a CCP update function via IO-Link and via I2C interface, triggered by the Write Memory button in the Renesas GUI. It uses similar update mechanisms to the Firmware Update described in section 11.
Figure 55 shows the high-level CCP update flow. After Initiating the CCP update, the device switches to bootloader mode. After the data is successfully transferred, the device is restarted.

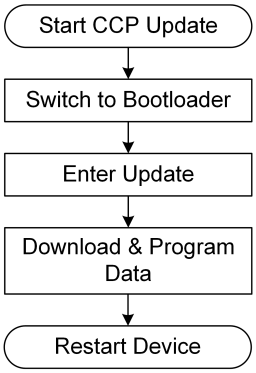

Figure 55. High-level CCP Update Flow

The CCP Update access via IO-Link can be protected with the firmware password (See section 13.26 for *FwPassword* and section 11 for firmware password mechanism) and the CCP password (CcpPassword see section 13.34.1), as shown in Figure 56.

Note: If the CCP-Password is other than 0xFFFFFFFF, it must be entered via ISDU Index 0x0201 in bootloader mode before starting CCP update. Otherwise, it prevents the device from updating CCP via BLOB mechanism and an error message is sent.

Enter the passwords in the following order:

1. Enter FW-Password in IO-Link COM mode
2. Enter bootloader mode
3. Enter CCP-Password in bootloader mode via IO-Link
4. Start CCP Update data transfer

Note: The CCP update mechanism via I2C ignores both the firmware password and the CCP password protection.

Note: The CCP-Password protects the device from reading CCP via IO-Link. The CCP-Password must be entered via ISDU 0x0201 in IO-Link COM mode prior to executing the Hidden Command 0x82 for CCP read.

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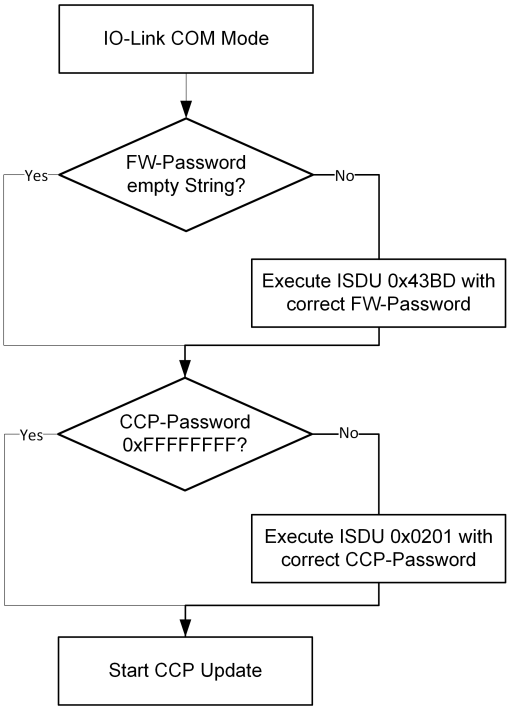

Figure 56. Password Mechanism for CCP Update

Execute the CCP update exclusively via the ZSSC3286 GUI and not by third party tools and set the FW password and CCP password to prevent an unauthorized CCP update.

Note: Ensure a stable power supply during update. Power loss during update may cause corruption of the device.

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13 Configuration and Calibration Page (CCP) Memory Map

This section describes the details and usage of single bitfields of CCP memory. The bitfields have two possible access attributes:

- Reserved: contains data that is set by Renesas and must not be changed from its default value.
- Read/Write: programmable with proper Read/Write access. By default all bitfields can be assumed as read and writable. Thus an empty access information indicates an read and writable bitfield.

13.1 IO-Link Settings

13.1.1 0x01 – PhyCtrl

Address : 0x01		**Register Name : PhyCtrl**		Default: 0x000000FF
Bits	**Access**	**Default**	**Field Name**	**Description**
31:8		0x0	Reserved	
7:0		0xFF	PhySel	Sets the PHY control mode 0x00 : RH4Z2501 0x01 to 0xFE : Reserved 0xFF : OWI DISABLED

13.1.2 0x02 – PhyCfg[0]

The CCP register PhyCfg[0] will contain configuration data for RH4Z2501 that will be transferred after power-on (reset) into the RH4Z2501 registers via OWI interface. For details of the register content refer RH4Z2501 datasheet referred in Table 3.

Address : 0x02		**Register Name : PhyCfg[0]**		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	PhyReg4	Contains register content for *alarm* register of RH4Z2501.
23:16		0x0	PhyReg3	Contains register content for *comCtrl2* register of RH4Z2501.
15:8		0x0	PhyReg2	Contains register content for *comCtrl1* register of RH4Z2501.
7:0		0x0	PhyReg1	Contains register content for *comParam* register of RH4Z2501.

13.1.3 0x03 – PhyCfg[1]

Address : 0x03		**Register Name : PhyCfg[1]**		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	PhyReg4	Unused
23:16		0x0	PhyReg3	Unused
15:8		0x0	PhyReg2	Unused
7:0		0x0	PhyReg1	Unused

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13.1.4 0x04 – IolMisc

Address : 0x04	Register Name : IolMisc			Default: 0x00004006
Bits	**Access**	**Default**	**Field Name**	**Description**
31:19	Reserved	0x0		Reserved
18:15		0x0	Gpio14Func	GPIO triggered Zero Adjustment 0x0 : Disabled 0x1 : Enabled (incl. Weak pull-up on ZAT pin) 0x2 to 0xF : Reserved
14:13		0x2	BinOutMode	Sets mode in which Binary Output signal is active 0x0 : SIO Only 0x1 : IO-Link COM Only 0x2 : SIO and IO-Link COM Only 0x3 : Reserved
12		0x0	BinOutInversion	Inversion of the Binary Output signal 0x0 : Disabled 0x1 : Enabled
11		0x0	BinOutSwitchingSignalNum	Sets the Sensor Switching Channel of the selected MDC for the Binary Output signal 0x0 : SSC.1 0x1 : SSC.2
10:9		0x0	BinOutSwitchingChNum	Sets the Measurement Data Channel (MDC) for the Binary Output signal 0x0 : MDC1 for SSP 4.1.1 0x1 : Reserved 0x2 : Reserved 0x3 : Reserved
8		0x0	BinOutEn	Activation of the Binary Output signal on GPIO15 0x0 : Disabled 0x1 : Enabled
7	Reserved	0x0		Reserved
6		0x0	AlarmInversion	Inversion of ALARM signal 0x0 : Disabled 0x1 : Enabled
5		0x0	AlarmSwitchingSignalNum	Sets the Sensor Switching Channel of the selected MDC for the ALARM signal 0x0 : SSC.1 0x1 : SSC.2
4:3		0x0	AlarmSwitchingChNum	Sets the Measurement Data Channel (MDC) for the ALARM signal 0x0 : MDC1 for SSP 4.1.1 0x1 : Reserved 0x2 : Reserved 0x3 : Reserved
2		0x1	LocatorEna	IO-Link Locator Function Enable - transmitted in ISDU 0x000D Subindex 0x7 0x0 : Disabled 0x1 : Enabled
1		0x1	SspDetectionMode	IO-Link Detection Mode - transmitted in ISDU 0x000D Subindex 0x6 0x0 : Object Detection 0x1 : Quantity Detection
0		0x0	SioPdinFlag	ALARM Function in SIO Mode 0x0 : Disabled 0x1 : Enabled

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13.2 Basic AFE Setups

13.2.1 0x05 – AfeBaseCfgParam

Address : 0x05		Register Name : AfeBaseCfgParam		Default: 0x00000001
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	AfeSyncStatus	AFE1 / AFE2 Synchronization 0x0 : Asynchronous measurement 0x1 : Synchronized measurement
23:16		0x0	Afe2SmConfig	AFE2 Sequencer Configuration 0x0 : SM- and SM+ 0x1 : SM+ and AUX_AZ 0x2 : SM+ only 0x3 : No Main Sensor-Bridge Measurement 0x4 : Capacitive SM+ and SM-
15:8		0x0	Afe1SmConfig	AFE1 Sequencer Configuration 0x0 : SM- and SM+ 0x1 : SM+ and AUX_AZ 0x2 : SM+ only 0x3 : No Main Sensor-Bridge Measurement 0x4 : Capacitive SM+ and SM-
7:0		0x1	AfeActive	AFE Activation configuration 0x0 : None 0x1 : AFE1 only 0x2 : AFE2 only 0x3 : AFE1 and AFE2 0x4 to 0x7 : Reserved

13.2.2 0x06 – AfeBaseCfgParam.AfeDsCfg.Reg1

Address : 0x06		Register Name : AfeBaseCfgParam.AfeDsCfg.Reg1		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	ConvCnt	Feature not implemented
23:0		0x0	Thresh1	Feature not implemented

13.2.3 0x07 – AfeBaseCfgParam.AfeDsCfg.Reg2

Address : 0x07		Register Name : AfeBaseCfgParam.AfeDsCfg.Reg2		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	Thresh2	Feature not implemented

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13.3 Sensor Bridge

13.3.1 0x08 – Bm1Cfg1

Address : 0x08		Register Name : Bm1Cfg1		Default: 0x04000655
Bits	**Access**	**Default**	**Field Name**	**Description**
31		0x0	BmType	Sensor type 0x0 : Resistive Bridge 0x1 : Thermopile / Thermocouple
30	Reserved	0x0	BmTestDac	Reserved
29	Reserved	0x0	BmTest	Reserved
28:26		0x1	BmAdcMux	ADC Input MUX Setting 0x1 : ADC input connected to PGA 0x2 : ADC input connected to input (Gain = 1, PGA bypassed)
25:22		0x0	BmBrdgRtl	Rtl resistor, applicable if BmBrdgType = 1 0x0 : Open | 0x4 : 8000Ω | 0x8 : 20000Ω 0x1 : 1333Ω | 0x5 : 10000Ω | 0x9 : 24000Ω 0x2 : 2000Ω | 0x6 : 14000Ω | 0xA : 28000Ω 0x3 : 4000Ω | 0x7 : 18000Ω | 0xB : 40000Ω
21:18		0x0	BmBrdgRth	Rth resistor, applicable if BmBrdgType = 1 0x0 : Open | 0x4 : 8000Ω | 0x8 : 20000Ω 0x1 : 1333Ω | 0x5 : 10000Ω | 0x9 : 24000Ω 0x2 : 2000Ω | 0x6 : 14000Ω | 0xA : 28000Ω 0x3 : 4000Ω | 0x7 : 18000Ω | 0xB : 40000Ω
17:16		0x0	BmSetTime	Bridge Settling Time before ADC conversion starts 0x0 : 20µs | 0x1 : 40µs | 0x2 : 60µs | 0x3 : 80µs
15		0x0	BmBrdgType	Bridge Supply via TOPx, BOTx 0x0 : Voltage Source 0x1 : Resistor or Current Source
14:12		0x0	BmAdcShift	ADC Shift V_{Shift} / V_{fs} 0x0 : 0 | 0x2 : 0.250 | 0x4 : 0.500 | 0x6 : 0.750 0x1 : 0.125 | 0x3 : 0.375 | 0x5 : 0.625 | 0x7 : 0.875
11:8		0x6	BmAdcReso	ADC Resolution 0x0 : 10 Bit | 0x4 : 14 Bit | 0x8 : 18 Bit | 0xC : 22 Bit 0x1 : 11 Bit | 0x5 : 15 Bit | 0x9 : 19 Bit | 0xD : 23 Bit 0x2 : 12 Bit | 0x6 : 16 Bit | 0xA : 20 Bit | 0xE : 24 Bit 0x3 : 13 Bit | 0x7 : 17 Bit | 0xB : 21 Bit
7		0x0	BmPgaPolarity	PGA Polarity 0x0 : Positive 0x1 : Negative
6:4		0x5	BmPgaGain2	PGA2 Gain 0x0 : 1.1 | 0x2 : 1.3 | 0x4 : 1.5 | 0x6 : 1.7 0x1 : 1.2 | 0x3 : 1.4 | 0x5 : 1.6 | 0x7 : 1.8
3:0		0x5	BmPgaGain1	PGA1 Gain 0x0 : 1.2 | 0x3 : 5.97 | 0x6 : 29.6 | 0x9 : 76.6 | 0xC : 187 0x1 : 2 | 0x4 : 11.9 | 0x7 : 39.2 | 0xA : 112 | 0xD : 223 0x2 : 4 | 0x5 : 19.8 | 0x8 : 58.1 | 0xB : 143 | 0xE : 275

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13.3.2 0x09 – Bm1Cfg2

Address : 0x09		Register Name : Bm1Cfg2		Default: 0x00000210
Bits	**Access**	**Default**	**Field Name**	**Description**
31:15	Reserved	0x0		Reserved
14		0x0	BmSetPerm	Enable permanent bridge supply. In this mode bridge supply (TOP1) will not be switched off during AUX measurement tasks 0x0 : Disabled 0x1 : Enabled **Note:** Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this bitfield to the GUI.
13:12		0x0	BmSetTimeMult	Selects multiplication factor for *Bm1Cfg1.BmSetTime* bridge settling time 0x0 : use selected bridge settling time (x1) 0x1 : use doubled bridge settling time (x2) 0x2 : use tripled bridge settling time (x3) 0x3 : use quadrupled bridge settling time (x4)
11:10		0x0	BmBias	AFE Bias Current Setting 0x0 : normal operation 0x1 : Reserved 0x2 : Reserved 0x3 : Reserved
9		0x1	BmAdcEnShift	ADC Shift & Gain ×2 Enable, activates **BmAdcShift** setting 0x0 : ADC Gain ×1, ADC Shift disabled 0x1 : ADC Gain ×2, ADC Shift enabled
8:5		0x0	BmBrdgIBias	Sensor Supply Current, applicable if BmBrdgType = 1 0x0 : Open/Off 0x1 : 5µA 0x2 : 10µA 0x3 : 20µA 0x4 : 40µA 0x5 : 80µA 0x6 : 100µA 0x7 : 160µA 0x8 : 200µA 0x9 : 500µA
4:0		0x10	BmPgaOffset	PGA Offset Shift 0x1 : -1.9mV 0x2 : -3.8mV 0x3 : -5.6mV 0x4 : -7.5mV 0x5 : -9.4mV 0x6 : -11.3mV 0x7 : -13.1mV 0x8 : -15.0mV 0x9 : -16.9mV 0xA : -18.8mV 0xB : -20.6mV 0xC : -22.5mV 0xD : -24.4mV 0xE : -26.2mV 0xF : -28.1mV 0x10 : 0mV 0x11 : 1.9mV 0x12 : 3.8mV 0x13 : 5.6mV 0x14 : 7.5mV 0x15 : 9.4mV 0x16 : 11.3mV 0x17 : 13.1mV 0x18 : 15.0mV 0x19 : 16.9mV 0x1A : 18.8mV 0x1B : 20.6mV 0x1C : 22.5mV 0x1D : 24.4mV 0x1E : 26.2mV 0x1F : 28.1mV

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13.3.3 0x0A – Bm2Cfg1

Address : 0x0A	Register Name : Bm2Cfg1			Default: 0x04000656
Bits	**Access**	**Default**	**Field Name**	**Description**
31		0x0	BmType	Sensor type 0x0 : Resistive Bridge 0x1 : Thermopile / Thermocouple
30	Reserved	0x0	BmTestDac	Reserved
29	Reserved	0x0	BmTest	Reserved
28:26		0x1	BmAdcMux	ADC Input MUX Setting 0x1 : ADC input connected to PGA 0x2 : ADC input connected to input (Gain = 1, PGA bypassed)
25:22		0x0	BmBrdgRtl	Rtl resistor, applicable if BmBrdgType = 1 0x0 : Open | 0x4 : 8000Ω | 0x8 : 20000Ω 0x1 : 1333Ω | 0x5 : 10000Ω | 0x9 : 24000Ω 0x2 : 2000Ω | 0x6 : 14000Ω | 0xA : 28000Ω 0x3 : 4000Ω | 0x7 : 18000Ω | 0xB : 40000Ω
21:18		0x0	BmBrdgRth	Rth resistor, applicable if BmBrdgType = 1 0x0 : Open | 0x4 : 8000Ω | 0x8 : 20000Ω 0x1 : 1333Ω | 0x5 : 10000Ω | 0x9 : 24000Ω 0x2 : 2000Ω | 0x6 : 14000Ω | 0xA : 28000Ω 0x3 : 4000Ω | 0x7 : 18000Ω | 0xB : 40000Ω
17:16		0x0	BmSetTime	Bridge Settling Time before ADC conversion starts 0x0 : 20µs | 0x1 : 40µs | 0x2 : 60µs | 0x3 : 80µs
15		0x0	BmBrdgType	Bridge Supply via TOPx, BOTx 0x0 : Voltage Source 0x1 : Resistor or Current Source
14:12		0x0	BmAdcShift	ADC Shift V_{Shift} / V_{fs} 0x0 : 0 | 0x2 : 0.250 | 0x4 : 0.500 | 0x6 : 0.750 0x1 : 0.125 | 0x3 : 0.375 | 0x5 : 0.625 | 0x7 : 0.875
11:8		0x6	BmAdcReso	ADC Resolution 0x0 : 10 Bit | 0x4 : 14 Bit | 0x8 : 18 Bit | 0xC : 22 Bit 0x1 : 11 Bit | 0x5 : 15 Bit | 0x9 : 19 Bit | 0xD : 23 Bit 0x2 : 12 Bit | 0x6 : 16 Bit | 0xA : 20 Bit | 0xE : 24 Bit 0x3 : 13 Bit | 0x7 : 17 Bit | 0xB : 21 Bit
7		0x0	BmPgaPolarity	PGA Polarity 0x0 : Positive 0x1 : Negative
6:4		0x5	BmPgaGain2	PGA2 Gain 0x0 : 1.1 | 0x2 : 1.3 | 0x4 : 1.5 | 0x6 : 1.7 0x1 : 1.2 | 0x3 : 1.4 | 0x5 : 1.6 | 0x7 : 1.8
3:0		0x6	BmPgaGain1	PGA1 Gain 0x0 : 1.2 | 0x3 : 5.97 | 0x6 : 29.6 | 0x9 : 76.6 | 0xC : 187 0x1 : 2 | 0x4 : 11.9 | 0x7 : 39.2 | 0xA : 112 | 0xD : 223 0x2 : 4 | 0x5 : 19.8 | 0x8 : 58.1 | 0xB : 143 | 0xE : 275

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13.3.4 0x0B – Bm2Cfg2

Address : 0x0B		Register Name : Bm2Cfg2		Default: 0x00000210
Bits	**Access**	**Default**	**Field Name**	**Description**
31:15	Reserved	0x0		Reserved
14		0x0	BmSetPerm	Enable permanent bridge supply. In this mode bridge supply (TOP2) will not be switched off during AUX measurement tasks 0x0 : Disabled 0x1 : Enabled **Note:** Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this bitfield to the GUI.
13:12		0x0	BmSetTimeMult	Selects multiplication factor for *Bm2Cfg1.BmSetTime* bridge settling time 0x0 : use selected bridge settling time (x1) 0x1 : use doubled bridge settling time (x2) 0x2 : use tripled bridge settling time (x3) 0x3 : use quadrupled bridge settling time (x4)
11:10		0x0	BmBias	AFE Bias Current Setting 0x0 : normal operation 0x1 : Reserved 0x2 : Reserved 0x3 : Reserved
9		0x1	BmAdcEnShift	ADC Shift & Gain ×2 Enable, activates **BmAdcShift** setting 0x0 : ADC Gain ×1, ADC Shift disabled 0x1 : ADC Gain ×2, ADC Shift enabled
8:5		0x0	BmBrdgIBias	Sensor Supply Current, applicable if BmBrdgType = 1 0x0 : Open/Off 0x1 : 5µA 0x2 : 10µA 0x3 : 20µA 0x4 : 40µA 0x5 : 80µA 0x6 : 100µA 0x7 : 160µA 0x8 : 200µA 0x9 : 500µA
4:0		0x10	BmPgaOffset	PGA Offset Shift 0x1 : -1.9mV 0x2 : -3.8mV 0x3 : -5.6mV 0x4 : -7.5mV 0x5 : -9.4mV 0x6 : -11.3mV 0x7 : -13.1mV 0x8 : -15.0mV 0x9 : -16.9mV 0xA : -18.8mV 0xB : -20.6mV 0xC : -22.5mV 0xD : -24.4mV 0xE : -26.2mV 0xF : -28.1mV 0x10 : 0mV 0x11 : 1.9mV 0x12 : 3.8mV 0x13 : 5.6mV 0x14 : 7.5mV 0x15 : 9.4mV 0x16 : 11.3mV 0x17 : 13.1mV 0x18 : 15.0mV 0x19 : 16.9mV 0x1A : 18.8mV 0x1B : 20.6mV 0x1C : 22.5mV 0x1D : 24.4mV 0x1E : 26.2mV 0x1F : 28.1mV

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13.4 External Temperature Sensor

13.4.1 0x0C – ExtTemp1Cfg1

Address : 0x0C		Register Name : ExtTemp1Cfg1		Default: 0x0011C5F1
Bits	**Access**	**Default**	**Field Name**	**Description**
31:28	Reserved	0x0		Reserved
27:24		0x0	ExtTempBrdgRtl	Rtl resistor, applicable if BmBrdgType = 1 0x0 : Open 0x1 : 1333Ω 0x2 : 2000Ω 0x3 : 4000Ω 0x4 : 8000Ω 0x5 : 10000Ω 0x6 : 14000Ω 0x7 : 18000Ω 0x8 : 20000Ω 0x9 : 24000Ω 0xA : 28000Ω 0xB : 40000Ω
23:20		0x1	ExtTempBrdgRth	Rth resistor, applicable if BmBrdgType = 1 0x0 : Open 0x1 : 1333Ω 0x2 : 2000Ω 0x3 : 4000Ω 0x4 : 8000Ω 0x5 : 10000Ω 0x6 : 14000Ω 0x7 : 18000Ω 0x8 : 20000Ω 0x9 : 24000Ω 0xA : 28000Ω 0xB : 40000Ω
19		0x0	ExtTempInput	External Temperature Sensor Input MUX 0x0 : Input connected to PGA 0x1 : Input connected to ADC
18:15		0x3	ExtTempType	External Temperature Sensor Type 0x0 : reserved 0x1 : Diode/NTC/PTC sink mode, internal bias 0x2 : Diode/NTC/PTC, external bias 0x3 : diode/NTC/PTC source mode, internal bias 0x4 : reserved 0x5 : Bridge single ended, internal bias 0x6 : Bridge single ended, external bias 0x7 : Bridge differential
14:12		0x4	ExtTempAdcShift	ADC Shift V_{Shift} / V_{fs} 0x0 : 0 0x1 : 0.125 0x2 : 0.250 0x3 : 0.375 0x4 : 0.500 0x5 : 0.625 0x6 : 0.750 0x7 : 0.875
11:8		0x5	ExtTempAdcReso	ADC Resolution 0x0 : 10 Bit 0x1 : 11 Bit 0x2 : 12 Bit 0x3 : 13 Bit 0x4 : 14 Bit 0x5 : 15 Bit
7		0x1	ExtTempPgaPolarity	PGA Polarity 0x0 : Positive 0x1 : Negative
6:4		0x7	ExtTempPgaGain2	PGA2 Gain 0x0 : 1.1 0x1 : 1.2 0x2 : 1.3 0x3 : 1.4 0x4 : 1.5 0x5 : 1.6 0x6 : 1.7 0x7 : 1.8
3:0		0x1	ExtTempPgaGain1	PGA1 Gain 0x0 : 1.2 0x1 : 2 0x2 : 4 0x3 : 5.97 0x4 : 11.9 0x5 : 19.8 0x6 : 29.6 0x7 : 39.2 0x8 : 58.1 0x9 : 76.6 0xA : 112 0xB : 143 0xC : 187 0xD : 223 0xE : 275

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13.4.2 0x0D – ExtTemp1Cfg2

Address : 0x0D		Register Name : ExtTemp1Cfg2		Default: 0x00000210
Bits	**Access**	**Default**	**Field Name**	**Description**
31:14	Reserved	0x0		Reserved
13:12		0x0	ExtTempSetTime	T1 Input Settling Time before ADC conversion starts 0x0 : 20µs | 0x1 : 40µs | 0x2 : 60µs | 0x3 : 80µs
11:10		0x0	ExtTempBias	AFE Bias Current Setting 0x0 : normal operation 0x1 : Reserved 0x2 : Reserved 0x3 : Reserved
9		0x1	ExtTempAdcEnShift	ADC Shift & Gain ×2 Enable, activates **BmAdcShift** setting 0x0 : ADC Gain ×1, ADC Shift disabled 0x3 : ADC Gain ×2, ADC Shift enabled
8:5		0x0	ExtTempBrdgIBias	Sensor Supply Current, applicable if BmBrdgType = 1 0x0 : Open/Off | 0x4 : 40µA | 0x8 : 200µA 0x1 : 5µA | 0x5 : 80µA | 0x9 : 500µA 0x2 : 10µA | 0x6 : 100µA 0x3 : 20µA | 0x7 : 160µA
4:0		0x10	ExtTempPgaOffset	PGA Offset Shift 0x1 : -1.9mV | 0x10 : 0mV 0x2 : -3.8mV | 0x11 : 1.9mV 0x3 : -5.6mV | 0x12 : 3.8mV 0x4 : -7.5mV | 0x13 : 5.6mV 0x5 : -9.4mV | 0x14 : 7.5mV 0x6 : -11.3mV | 0x15 : 9.4mV 0x7 : -13.1mV | 0x16 : 11.3mV 0x8 : -15.0mV | 0x17 : 13.1mV 0x9 : -16.9mV | 0x18 : 15.0mV 0xA : -18.8mV | 0x19 : 16.9mV 0xB : -20.6mV | 0x1A : 18.8mV 0xC : -22.5mV | 0x1B : 20.6mV 0xD : -24.4mV | 0x1C : 22.5mV 0xE : -26.2mV | 0x1D : 24.4mV 0xF : -28.1mV | 0x1E : 26.2mV 0x1F : 28.1mV

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13.4.3 0x0E – ExtTemp2Cfg1

Address : 0x0E	Register Name : ExtTemp2Cfg1			Default: 0x00118502
Bits	**Access**	**Default**	**Field Name**	**Description**
31:28	Reserved	0x0		Reserved
27:24		0x0	ExtTempBrdgRtl	RtI resistor, applicable if BmBrdgType = 1 0x0 : Open 0x1 : 1333Ω 0x2 : 2000Ω 0x3 : 4000Ω 0x4 : 8000Ω 0x5 : 10000Ω 0x6 : 14000Ω 0x7 : 18000Ω 0x8 : 20000Ω 0x9 : 24000Ω 0xA : 28000Ω 0xB : 40000Ω
23:20		0x1	ExtTempBrdgRth	Rth resistor, applicable if BmBrdgType = 1 0x0 : Open 0x1 : 1333Ω 0x2 : 2000Ω 0x3 : 4000Ω 0x4 : 8000Ω 0x5 : 10000Ω 0x6 : 14000Ω 0x7 : 18000Ω 0x8 : 20000Ω 0x9 : 24000Ω 0xA : 28000Ω 0xB : 40000Ω
19		0x0	ExtTempInput	External Temperature Sensor Input MUX 0x0 : Input connected to PGA 0x1 : Input connected to ADC
18:15		0x3	ExtTempType	External Temperature Type 0x0 : Reserved 0x1 : Diode/NTC/PTC sink mode, internal bias 0x2 : Diode/NTC/PTC, external bias 0x3 : Diode/NTC/PTC source mode, internal bias 0x4 : Reserved 0x5 : Bridge single ended, internal bias 0x6 : Bridge single ended, external bias 0x7 : Bridge differential
14:12		0x0	ExtTempAdcShift	ADC Shift V_{Shift} / V_{fs} 0x0 : 0 0x1 : 0.125 0x2 : 0.250 0x3 : 0.375 0x4 : 0.500 0x5 : 0.625 0x6 : 0.750 0x7 : 0.875
11:8		0x5	ExtTempAdcReso	ADC Resolution 0x0 : 10 Bit 0x1 : 11 Bit 0x2 : 12 Bit 0x3 : 13 Bit 0x4 : 14 Bit 0x5 : 15 Bit
7		0x0	ExtTempPgaPolarity	PGA Polarity 0x0 : Positive 0x1 : Negative
6:4		0x0	ExtTempPgaGain2	PGA2 Gain 0x0 : 1.1 0x1 : 1.2 0x2 : 1.3 0x3 : 1.4 0x4 : 1.5 0x5 : 1.6 0x6 : 1.7 0x7 : 1.8
3:0		0x2	ExtTempPgaGain1	PGA1 Gain 0x0 : 1.2 0x1 : 2 0x2 : 4 0x3 : 5.97 0x4 : 11.9 0x5 : 19.8 0x6 : 29.6 0x7 : 39.2 0x8 : 58.1 0x9 : 76.6 0xA : 112 0xB : 143 0xC : 187 0xD : 223 0xE : 275

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13.4.4 0x0F – ExtTemp2Cfg2

Address : 0x0F		Register Name : ExtTemp2Cfg2		Default: 0x00000010
Bits	**Access**	**Default**	**Field Name**	**Description**
31:14	Reserved	0x0		Reserved
13:12		0x0	ExtTempSetTime	T1 Input Settling Time before ADC conversion starts 0x0 : 20µs | 0x1 : 40µs | 0x2 : 60µs | 0x3 : 80µs
11:10		0x0	ExtTempBias	AFE Bias Current Setting 0x0 : normal operation 0x1 : Reserved 0x2 : Reserved 0x3 : Reserved
9		0x0	ExtTempAdcEnShift	ADC Shift & Gain ×2 Enable, activates **BmAdcShift** setting 0x0 : ADC Gain ×1, ADC Shift disabled 0x3 : ADC Gain ×2, ADC Shift enabled
8:5		0x0	ExtTempBrdgIBias	Sensor Supply Current, applicable if BmBrdgType = 1 0x0 : Open/Off | 0x4 : 40µA | 0x8 : 200µA 0x1 : 5µA | 0x5 : 80µA | 0x9 : 500µA 0x2 : 10µA | 0x6 : 100µA 0x3 : 20µA | 0x7 : 160µA
4:0		0x10	ExtTempPgaOffset	PGA Offset Shift 0x10 : 0mV 0x1 : -1.9mV | 0x11 : 1.9mV 0x2 : -3.8mV | 0x12 : 3.8mV 0x3 : -5.6mV | 0x13 : 5.6mV 0x4 : -7.5mV | 0x14 : 7.5mV 0x5 : -9.4mV | 0x15 : 9.4mV 0x6 : -11.3mV | 0x16 : 11.3mV 0x7 : -13.1mV | 0x17 : 13.1mV 0x8 : -15.0mV | 0x18 : 15.0mV 0x9 : -16.9mV | 0x19 : 16.9mV 0xA : -18.8mV | 0x1A : 18.8mV 0xB : -20.6mV | 0x1B : 20.6mV 0xC : -22.5mV | 0x1C : 22.5mV 0xD : -24.4mV | 0x1D : 24.4mV 0xE : -26.2mV | 0x1E : 26.2mV 0xF : -28.1mV | 0x1F : 28.1mV

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13.4.5 0x10 – ExtTemp3Cfg1

Address : 0x10		Register Name : ExtTemp3Cfg1		Default: 0x00118502
Bits	**Access**	**Default**	**Field Name**	**Description**
31:28	Reserved	0x0		Reserved
27:24		0x0	ExtTempBrdgRtl	RtI resistor, applicable if BmBrdgType = 1 0x0 : Open 0x1 : 1333Ω 0x2 : 2000Ω 0x3 : 4000Ω 0x4 : 8000Ω 0x5 : 10000Ω 0x6 : 14000Ω 0x7 : 18000Ω 0x8 : 20000Ω 0x9 : 24000Ω 0xA : 28000Ω 0xB : 40000Ω
23:20		0x1	ExtTempBrdgRth	Rth resistor, applicable if BmBrdgType = 1 0x0 : Open 0x1 : 1333Ω 0x2 : 2000Ω 0x3 : 4000Ω 0x4 : 8000Ω 0x5 : 10000Ω 0x6 : 14000Ω 0x7 : 18000Ω 0x8 : 20000Ω 0x9 : 24000Ω 0xA : 28000Ω 0xB : 40000Ω
19		0x0	ExtTempInput	External Temperature Sensor Input MUX 0x0 : Input connected to PGA 0x1 : Input connected to ADC
18:15		0x3	ExtTempType	External Temperature Type 0x0 : Reserved 0x1 : Diode/NTC/PTC sink mode, internal bias 0x2 : Diode/NTC/PTC, external bias 0x3 : Diode/NTC/PTC source mode, internal bias 0x4 : Reserved 0x5 : Bridge single ended, internal bias 0x6 : Bridge single ended, external bias 0x7 : Bridge differential
14:12		0x0	ExtTempAdcShift	ADC Shift V_{Shift} / V_{fs} 0x0 : 0 0x1 : 0.125 0x2 : 0.250 0x3 : 0.375 0x4 : 0.500 0x5 : 0.625 0x6 : 0.750 0x7 : 0.875
11:8		0x5	ExtTempAdcReso	ADC Resolution 0x0 : 10 Bit 0x1 : 11 Bit 0x2 : 12 Bit 0x3 : 13 Bit 0x4 : 14 Bit 0x5 : 15 Bit
7		0x0	ExtTempPgaPolarity	PGA Polarity 0x0 : Positive 0x1 : Negative
6:4		0x0	ExtTempPgaGain2	PGA2 Gain 0x0 : 1.1 0x1 : 1.2 0x2 : 1.3 0x3 : 1.4 0x4 : 1.5 0x5 : 1.6 0x6 : 1.7 0x7 : 1.8
3:0		0x2	ExtTempPgaGain1	PGA1 Gain 0x0 : 1.2 0x1 : 2 0x2 : 4 0x3 : 5.97 0x4 : 11.9 0x5 : 19.8 0x6 : 29.6 0x7 : 39.2 0x8 : 58.1 0x9 : 76.6 0xA : 112 0xB : 143 0xC : 187 0xD : 223 0xE : 275

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13.4.6 0x11 – ExtTemp3Cfg2

Address : 0x11		Register Name : ExtTemp3Cfg2		Default: 0x00000010
Bits	**Access**	**Default**	**Field Name**	**Description**
31:14	Reserved	0x0		Reserved
13:12		0x0	ExtTempSetTime	T1 Input Settling Time before ADC conversion starts 0x0 : 20µs | 0x1 : 40µs | 0x2 : 60µs | 0x3 : 80µs
11:10		0x0	ExtTempBias	AFE Bias Current Setting 0x0 : normal operation 0x1 : Reserved 0x2 : Reserved 0x3 : Reserved
9		0x0	ExtTempAdcEnShift	ADC Shift & Gain ×2 Enable, activates **BmAdcShift** setting 0x0 : ADC Gain ×1, ADC Shift disabled 0x3 : ADC Gain ×2, ADC Shift enabled
8:5		0x0	ExtTempBrdgIBias	Sensor Supply Current, applicable if BmBrdgType = 1 0x0 : Open/Off | 0x4 : 40µA | 0x8 : 200µA 0x1 : 5µA | 0x5 : 80µA | 0x9 : 500µA 0x2 : 10µA | 0x6 : 100µA 0x3 : 20µA | 0x7 : 160µA
4:0		0x10	ExtTempPgaOffset	PGA Offset Shift 0x10 : 0mV 0x1 : -1.9mV | 0x11 : 1.9mV 0x2 : -3.8mV | 0x12 : 3.8mV 0x3 : -5.6mV | 0x13 : 5.6mV 0x4 : -7.5mV | 0x14 : 7.5mV 0x5 : -9.4mV | 0x15 : 9.4mV 0x6 : -11.3mV | 0x16 : 11.3mV 0x7 : -13.1mV | 0x17 : 13.1mV 0x8 : -15.0mV | 0x18 : 15.0mV 0x9 : -16.9mV | 0x19 : 16.9mV 0xA : -18.8mV | 0x1A : 18.8mV 0xB : -20.6mV | 0x1B : 20.6mV 0xC : -22.5mV | 0x1C : 22.5mV 0xD : -24.4mV | 0x1D : 24.4mV 0xE : -26.2mV | 0x1E : 26.2mV 0xF : -28.1mV | 0x1F : 28.1mV

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13.4.7 0x12 – Cm1Config

Address : 0x12		Register Name : Cm1Config		Default: 0x0003C004
Bits	**Access**	**Default**	**Field Name**	**Description**
31:20	Reserved	0x0		Reserved
19		0x0	CmEnShieldDrv	Enable active shield drive 0x0 : Disabled 0x1 : Enabled
18		0x0	CmEnShift	Enable internal shift cap 0x0 : Disabled 0x1 : Enabled
17:13		0x1E	CmCapInt	CVC integration capacitance C_{int} 0x0 : 20 pF | 0x8 : 36 pF | 0x10 : 52 pF | 0x18 : 68 pF 0x1 : 22 pF | 0x9 : 38 pF | 0x11 : 54 pF | 0x19 : 70 pF 0x2 : 24 pF | 0xA : 40 pF | 0x12 : 56 pF | 0x1A : 72 pF 0x3 : 26 pF | 0xB : 42 pF | 0x13 : 58 pF | 0x1B : 74 pF 0x4 : 28 pF | 0xC : 44 pF | 0x14 : 60 pF | 0x1C : 76 pF 0x5 : 30 pF | 0xD : 46 pF | 0x15 : 62 pF | 0x1D : 78 pF 0x6 : 32 pF | 0xE : 48 pF | 0x16 : 64 pF | 0x1E : 80 pF 0x7 : 34 pF | 0xF : 50 pF | 0x17 : 66 pF | 0x1F : 82 pF
12:8		0x0	CmCapShift	CVC shift capacitance C_{shift} 0x0 : 0 pF | 0x8 : 16 pF | 0x10 : 32 pF | 0x18 : 48 pF 0x1 : 2 pF | 0x9 : 18 pF | 0x11 : 34 pF | 0x19 : 50 pF 0x2 : 4 pF | 0xA : 20 pF | 0x12 : 36 pF | 0x1A : 52 pF 0x3 : 6 pF | 0xB : 22 pF | 0x13 : 38 pF | 0x1B : 54 pF 0x4 : 8 pF | 0xC : 24 pF | 0x14 : 40 pF | 0x1C : 56 pF 0x5 : 10 pF | 0xD : 26 pF | 0x15 : 42 pF | 0x1D : 58 pF 0x6 : 12 pF | 0xE : 28 pF | 0x16 : 44 pF | 0x1E : 60 pF 0x7 : 14 pF | 0xF : 30 pF | 0x17 : 46 pF | 0x1F : 62 pF
7		0x0	CmAdcEnShift	ADC_{Gain}: Enables 2x gain and ADC shift (on certain application modes) (66) 0x0 : Disabled 0x1 : Enabled
6:4		0x0	CmAdcShift	ADC Shift 0x0 : 0 | 0x2 : 0.25 | 0x4 : 0.5 | 0x6 : 0.75 0x1 : 0.125 | 0x3 : 0.375 | 0x5 : 0.625 | 0x7 : 0.875
3:0		0x4	CmAdcReso	ADC Resolution 0x0 : 10 Bit | 0x4 : 14 Bit | 0x8 : 18 Bit | 0xC : 22 Bit 0x1 : 11 Bit | 0x5 : 15 Bit | 0x9 : 19 Bit | 0xD : 23 Bit 0x2 : 12 Bit | 0x6 : 16 Bit | 0xA : 20 Bit | 0xE : 24 Bit 0x3 : 13 Bit | 0x7 : 17 Bit | 0xB : 21 Bit

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13.4.8 0x13 – Cm2Config

Address : 0x13		Register Name : Cm2Config		Default: 0x0003C004
Bits	**Access**	**Default**	**Field Name**	**Description**
31:20	Reserved	0x0		Reserved
19		0x0	CmEnShieldDrv	Enable active shield drive 0x0 : Disabled 0x1 : Enabled
18		0x0	CmEnShift	Enable internal shift cap 0x0 : Disabled 0x1 : Enabled
17:13		0x1E	CmCapInt	CVC integration capacitance $_{int}$ 0x0 : 20 pF, 0x8 : 36 pF, 0x10 : 52 pF, 0x18 : 68 pF 0x1 : 22 pF, 0x9 : 38 pF, 0x11 : 54 pF, 0x19 : 70 pF 0x2 : 24 pF, 0xA : 40 pF, 0x12 : 56 pF, 0x1A : 72 pF 0x3 : 26 pF, 0xB : 42 pF, 0x13 : 58 pF, 0x1B : 74 pF 0x4 : 28 pF, 0xC : 44 pF, 0x14 : 60 pF, 0x1C : 76 pF 0x5 : 30 pF, 0xD : 46 pF, 0x15 : 62 pF, 0x1D : 78 pF 0x6 : 32 pF, 0xE : 48 pF, 0x16 : 64 pF, 0x1E : 80 pF 0x7 : 34 pF, 0xF : 50 pF, 0x17 : 66 pF, 0x1F : 82 pF
12:8		0x0	CmCapShift	CVC shift capacitance $_{shift}$ 0x0 : 0 pF, 0x8 : 16 pF, 0x10 : 32 pF, 0x18 : 48 pF 0x1 : 2 pF, 0x9 : 18 pF, 0x11 : 34 pF, 0x19 : 50 pF 0x2 : 4 pF, 0xA : 20 pF, 0x12 : 36 pF, 0x1A : 52 pF 0x3 : 6 pF, 0xB : 22 pF, 0x13 : 38 pF, 0x1B : 54 pF 0x4 : 8 pF, 0xC : 24 pF, 0x14 : 40 pF, 0x1C : 56 pF 0x5 : 10 pF, 0xD : 26 pF, 0x15 : 42 pF, 0x1D : 58 pF 0x6 : 12 pF, 0xE : 28 pF, 0x16 : 44 pF, 0x1E : 60 pF 0x7 : 14 pF, 0xF : 30 pF, 0x17 : 46 pF, 0x1F : 62 pF
7		0x0	CmAdcEnShift	ADC_{Gain}: Enables 2x gain and ADC shift (on certain application modes) 0x0 : Disabled 0x1 : Enabled
6:4		0x0	CmAdcShift	ADC Shift 0x0 : 0, 0x2 : 0.25, 0x4 : 0.5, 0x6 : 0.75 0x1 : 0.125, 0x3 : 0.375, 0x5 : 0.625, 0x7 : 0.875
3:0		0x4	CmAdcReso	ADC Resolution 0x0 : 10 Bit, 0x4 : 14 Bit, 0x8 : 18 Bit, 0xC : 22 Bit 0x1 : 11 Bit, 0x5 : 15 Bit, 0x9 : 19 Bit, 0xD : 23 Bit 0x2 : 12 Bit, 0x6 : 16 Bit, 0xA : 20 Bit, 0xE : 24 Bit 0x3 : 13 Bit, 0x7 : 17 Bit, 0xB : 21 Bit

13.4.9 0x14 – CmConfig

Address : 0x14		Register Name : CmConfig		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:10	Reserved	0x0		Reserved
9		0x0	CMShieldDrv10nF	Enable 10nF shield driver mode 0x0 : Disabled 0x1 : Enabled
8		0x0	CmNoiseMode	Noise Mode 0x0 : Normal 0x1 : Low Noise
7		0x0	CmEnRatio	Enable difference measurement mode 0x0 : Disabled 0x1 : Enabled
6:2	Reserved	0x0	CmRefSel	Reserved
1		0x0	CmEnDiff	Enable ratiometric measurement mode 0x0 : Disabled 0x1 : Enabled
0		0x0	CmSenseCapType	Input capacitor type 0x0 : Isolated 0x1 : Grounded

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13.5 PTAT Sensor

13.5.1 0x15 – PtatCfg1

Address : 0x15		Register Name : PtatCfg1		Default: 0x0000F533
Bits	**Access**	**Default**	**Field Name**	**Description**
31:18	Reserved	0x0		Reserved
17:15		0x1	AdcMux	ADC Input MUX Setting 0x1 : ADC input connected to PGA [1]
14:12		0x7	AdcShift	ADC Shift V_{Shift} / V_{fs} 0x0 : 0 | 0x2 : 0.250 | 0x4 : 0.500 | 0x6 : 0.750 0x1 : 0.125 | 0x3 : 0.375 | 0x5 : 0.625 | 0x7 : 0.875 [1]
11:8		0x5	AdcReso	ADC Resolution 0x0 : 10 Bit | 0x2 : 12 Bit | 0x4 : 14 Bit 0x1 : 11 Bit | 0x3 : 13 Bit | 0x5 : 15 Bit
7		0x0	PgaPolarity	PGA Polarity 0x0 : Positive [1] 0x1 : Negative
6:4		0x3	PgaGain2	PGA2 Gain 0x0 : 1.1 | 0x2 : 1.3 | 0x4 : 1.5 | 0x6 : 1.7 0x1 : 1.2 | 0x3 : 1.4 [1] | 0x5 : 1.6 | 0x7 : 1.8
3:0		0x3	PgaGain1	PGA1 Gain 0x0 : 1.2 | 0x3 : 5.97 [1] | 0x6 : 29.6 | 0x9 : 76.6 | 0xC : 187 0x1 : 2 | 0x4 : 11.9 | 0x7 : 39.2 | 0xA : 112 | 0xD : 223 0x2 : 4 | 0x5 : 19.8 | 0x8 : 58.1 | 0xB : 143 | 0xE : 275

[1] Renesas recommended

13.5.2 0x16 – PtatCfg2

Address : 0x16		Register Name : PtatCfg2		Default: 0x00000030
Bits	**Access**	**Default**	**Field Name**	**Description**
31:8	Reserved	0x0		Reserved
7:6		0x0	Bias	AFE Bias Current Setting 0x0 : normal operation 0x1 : Reserved 0x2 : Reserved 0x3 : Reserved
5		0x1	AdcEnShift	ADC Shift & Gain ×2 Enable, activates **AdcShift** setting 0x0 : ADC Gain ×1, ADC Shift disabled 0x3 : ADC Gain ×2, ADC Shift enabled [1]
4:0		0x10	PgaOffset	PGA Offset Shift 0x1 : -1.9mV | 0x10 : 0mV [1] 0x2 : -3.8mV | 0x11 : 1.9mV 0x3 : -5.6mV | 0x12 : 3.8mV 0x4 : -7.5mV | 0x13 : 5.6mV 0x5 : -9.4mV | 0x14 : 7.5mV 0x6 : -11.3mV | 0x15 : 9.4mV 0x7 : -13.1mV | 0x16 : 11.3mV 0x8 : -15.0mV | 0x17 : 13.1mV 0x9 : -16.9mV | 0x18 : 15.0mV 0xA : -18.8mV | 0x19 : 16.9mV 0xB : -20.6mV | 0x1A : 18.8mV 0xC : -22.5mV | 0x1B : 20.6mV 0xD : -24.4mV | 0x1C : 22.5mV 0xE : -26.2mV | 0x1D : 24.4mV 0xF : -28.1mV | 0x1E : 26.2mV 0x1F : 28.1mV

[1] Renesas recommended

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13.6 AFE Sequencer

13.6.1 0x17 – Afe1MeasCfg1

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x17		Register Name : Afe1MeasCfg1		Default: 0x01020036
Bits	**Access**	**Default**	**Field Name**	**Description**
31		0x0	BurstModeSlot8	AFE DMA Burst Mode Data Transfer after Slot_x 0x0 : Disabled 0x1 : Enabled
30		0x0	BurstModeSlot7	
29		0x0	BurstModeSlot6	
28		0x0	BurstModeSlot5	
27		0x0	BurstModeSlot4	
26		0x0	BurstModeSlot3	
25		0x0	BurstModeSlot2	
24		0x1	BurstModeSlot1	
23		0x0	EocIrqSlot8	End of Conversion Interrupt after Slot_x 0x0 : Disabled 0x1 : Enabled
22		0x0	EocIrqSlot7	
21		0x0	EocIrqSlot6	
20		0x0	EocIrqSlot5	
19		0x0	EocIrqSlot4	
18		0x0	EocIrqSlot3	
17		0x1	EocIrqSlot2	
16		0x0	EocIrqSlot1	
15:14		0x0	MeasTypeSlot8	AFE Measurement Type for Slot_x 0x0 : None 0x1 : SM- 0x2 : SM+ 0x3 : AUX_i
13:12		0x0	MeasTypeSlot7	
11:10		0x0	MeasTypeSlot6	
9:8		0x0	MeasTypeSlot5	
7:6		0x0	MeasTypeSlot4	
5:4		0x3	MeasTypeSlot3	
3:2		0x1	MeasTypeSlot2	
1:0		0x2	MeasTypeSlot1	

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13.6.2 0x18 – Afe1MeasCfg2

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x18		**Register Name : Afe1MeasCfg2**		Default: 0x00000013
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:8		0x0	AuxMaxTime	Maximum length of AUX_i measurement slots within a sequence 0x0000 … 0xFFFF AFE clock cycles The parameter is calculated based on the relevant timing setups of all active AUX_i measurements to secure all AUX_i measurements have the same duration. This is mainly required for synchronized AFE operation.
7:6		0x0	AuxInsertRate	Insertion Rate of an AUX_i measurement in „Accelerated main measurement“ setup 0x0 : Disabled 0x1 : Every 2nd 0x2 : Every 4th 0x3 : Every 8th
5:4		0x1	CyclicMode	Sequencer Run Mode 0x0 : Single measurement 0x1 : Continuous cyclic measurement 0x2 : Discontinuous cyclic measurement, started by trigger
3:0		0x3	NrOfSlots	Number of active measurement slots 0x0 … 0x8 selectable

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13.6.3 0x19 – Afe1MeasCfg3

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x19		Register Name : Afe1MeasCfg3		Default: 0x00000018
Bits	**Access**	**Default**	**Field Name**	**Description**
31	Reserved	0x0	AuxMeasEnable0Aux32	Activation of Auxiliary measurements Bit 28 : Bridge Sensor connection check, INP and INN shorted Bit 27 : Bridge Sensor connection check, INP or INN open Bit 17 : T3 Sensor, check open Bit 16 : T3 Sensor, check short to bottom Bit 15 : T3 Sensor, check short to top Bit 14 : T3 Sensor S+ Bit 13 : T3 Sensor S- Bit 12 : T2 Sensor, check open Bit 11 : T2 Sensor, check short to bottom Bit 10 : T2 Sensor, check short to top Bit 9 : T2 Sensor S+ Bit 8 : T2 Sensor S- Bit 7 : T1 Sensor, check open Bit 6 : T1 Sensor, check short to bottom Bit 5 : T1 Sensor, check short to top Bit 4 : T1 Sensor S+ Bit 3 : T1 Sensor S- Bit 2 : PTAT Sensor S+ Bit 1 : PTAT Sensor S- Bit 0 : Auto-zero (AZ) measurement on Sensor Bridge All other bits reserved Bit Value Meaning 0 : Aux measurement Skipped 1 : Aux measurement Executed
30	Reserved	0x0	AuxMeasEnable0Aux31	
29	Reserved	0x0	AuxMeasEnable0Aux30	
28		0x0	AuxMeasEnable0Aux29	
27		0x0	AuxMeasEnable0Aux28	
26	Reserved	0x0	AuxMeasEnable0Aux27	
25	Reserved	0x0	AuxMeasEnable0Aux26	
24	Reserved	0x0	AuxMeasEnable0Aux25	
23	Reserved	0x0	AuxMeasEnable0Aux24	
22	Reserved	0x0	AuxMeasEnable0Aux23	
21		0x0	AuxMeasEnable0Aux22	
20	Reserved	0x0	AuxMeasEnable0Aux21	
19	Reserved	0x0	AuxMeasEnable0Aux20	
18		0x0	AuxMeasEnable0Aux19	
17		0x0	AuxMeasEnable0Aux18	
16		0x0	AuxMeasEnable0Aux17	
15		0x0	AuxMeasEnable0Aux16	
14		0x0	AuxMeasEnable0Aux15	
13		0x0	AuxMeasEnable0Aux14	
12		0x0	AuxMeasEnable0Aux13	
11		0x0	AuxMeasEnable0Aux12	
10		0x0	AuxMeasEnable0Aux11	
9		0x0	AuxMeasEnable0Aux10	
8		0x0	AuxMeasEnable0Aux9	
7		0x0	AuxMeasEnable0Aux8	
6		0x0	AuxMeasEnable0Aux7	
5		0x0	AuxMeasEnable0Aux6	
4		0x1	AuxMeasEnable0Aux5	
3		0x1	AuxMeasEnable0Aux4	
2		0x0	AuxMeasEnable0Aux3	
1		0x0	AuxMeasEnable0Aux2	
0		0x0	AuxMeasEnable0Aux1	

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13.6.4 0x1A – Afe1MeasCfg4

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x1A		**Register Name : Afe1MeasCfg4**		Default: 0x00400000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:25	Reserved	0x0		Reserved
24		0x0	SensBufDepth	Bridge Sensor data buffer depth in SRAM 0x0 : data buffer depth 1 0x1 : data buffer depth 8
23		0x0	IrqEnableEoauxaz	End of AZ Measurement 0x0 : IRQ disabled 0x1 : IRQ enabled
22		0x1	IrqEnableEoauxseq	End of Aux Sequence 0x0 : IRQ disabled 0x1 : IRQ enabled
21		0x0	IrqEnableEoauxins	End of Inserted AUX Measurement 0x0 : IRQ disabled 0x1 : IRQ enabled
20:5		0x0	IdleTime	In continuous cyclic measurement mode idle times up to 10ms can be asserted between two sequences. IdleTime represents a number of AFE clocks – 4MHz by default
4		0x0	AuxMeasEnable1Aux37	Enable CVC diagnosis leak_2 S- 0x0 : Aux measurement Skipped 0x1 : Aux measurement Executed
3		0x0	AuxMeasEnable1Aux36	Enable CVC diagnosis leak_2 S- 0x0 : Aux measurement Skipped 0x1 : Aux measurement Executed
2		0x0	AuxMeasEnable1Aux35	Enable CVC diagnosis leak_1 S+ 0x0 : Aux measurement Skipped 0x1 : Aux measurement Executed
1		0x0	AuxMeasEnable1Aux34	Enable CVC diagnosis leak_1 S- 0x0 : Aux measurement Skipped 0x1 : Aux measurement Executed
0	Reserved	0x0	AuxMeasEnable1Aux33	Reserved

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13.6.5 0x1B – Afe2MeasCfg1

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x1B		Register Name : Afe2MeasCfg1		Default: 0x01020036
Bits	**Access**	**Default**	**Field Name**	**Description**
31		0x0	BurstModeSlot8	AFE DMA Burst Mode Data Transfer after Slot_x 0x0 : Disabled 0x1 : Enabled
30		0x0	BurstModeSlot7	
29		0x0	BurstModeSlot6	
28		0x0	BurstModeSlot5	
27		0x0	BurstModeSlot4	
26		0x0	BurstModeSlot3	
25		0x0	BurstModeSlot2	
24		0x1	BurstModeSlot1	
23		0x0	EocIrqSlot8	End of Conversion Interrupt after Slot_x 0x0 : Disabled 0x1 : Enabled
22		0x0	EocIrqSlot7	
21		0x0	EocIrqSlot6	
20		0x0	EocIrqSlot5	
19		0x0	EocIrqSlot4	
18		0x0	EocIrqSlot3	
17		0x1	EocIrqSlot2	
16		0x0	EocIrqSlot1	
15:14		0x0	MeasTypeSlot8	AFE Measurement Type for Slot_x 0x0 : None 0x1 : SM- 0x2 : SM+ 0x3 : AUX_i
13:12		0x0	MeasTypeSlot7	
11:10		0x0	MeasTypeSlot6	
9:8		0x0	MeasTypeSlot5	
7:6		0x0	MeasTypeSlot4	
5:4		0x3	MeasTypeSlot3	
3:2		0x1	MeasTypeSlot2	
1:0		0x2	MeasTypeSlot1	

13.6.6 0x1C – Afe2MeasCfg2

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x1C		Register Name : Afe2MeasCfg2		Default: 0x00000013
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:8		0x0	AuxMaxTime	Maximum length of AUX_i measurement slots within a sequence 0x0000 … 0xFFFF AFE clock cycles The parameter is calculated based on the relevant timing setups of all active AUX_i measurements to secure all AUX_i measurements have the same duration. This is mainly required for synchronized AFE operation.
7:6		0x0	AuxInsertRate	Insertion Rate of an AUX_i measurement in „Accelerated main measurement“ setup 0x0 : Disabled 0x1 : Every 2nd 0x2 : Every 4th 0x3 : Every 8th
5:4		0x1	CyclicMode	Sequencer Run Mode 0x0 : Single measurement 0x1 : Continuous cyclic measurement 0x2 : Discontinuous cyclic measurement, started by trigger
3:0		0x3	NrOfSlots	Number of active measurement slots 0x0 … 0x8 selectable

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13.6.7 0x1D – Afe2MeasCfg3

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x1D		Register Name : Afe2MeasCfg3		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31	Reserved	0x0	AuxMeasEnable0Aux32	Activation of Auxiliary measurements Bit 28 : Bridge Sensor connection check, INP and INN shorted Bit 27 : Bridge Sensor connection check, INP or INN open Bit 17 : T3 Sensor, check open Bit 16 : T3 Sensor, check short to bottom Bit 15 : T3 Sensor, check short to top Bit 14 : T3 Sensor S+ Bit 13 : T3 Sensor S- Bit 12 : T2 Sensor, check open Bit 11 : T2 Sensor, check short to bottom Bit 10 : T2 Sensor, check short to top Bit 9 : T2 Sensor S+ Bit 8 : T2 Sensor S- Bit 7 : T1 Sensor, check open Bit 6 : T1 Sensor, check short to bottom Bit 5 : T1 Sensor, check short to top Bit 4 : T1 Sensor S+ Bit 3 : T1 Sensor S- Bit 2 : PTAT Sensor S+ Bit 1 : PTAT Sensor S- Bit 0 : Auto-zero (AZ) measurement on Sensor Bridge All other bits reserved Bit Value Meaning 0 : Aux measurement Skipped 1 : Aux measurement Executed
30	Reserved	0x0	AuxMeasEnable0Aux31	
29	Reserved	0x0	AuxMeasEnable0Aux30	
28	Reserved	0x0	AuxMeasEnable0Aux29	
27		0x0	AuxMeasEnable0Aux28	
26		0x0	AuxMeasEnable0Aux27	
25	Reserved	0x0	AuxMeasEnable0Aux26	
24	Reserved	0x0	AuxMeasEnable0Aux25	
23	Reserved	0x0	AuxMeasEnable0Aux24	
22	Reserved	0x0	AuxMeasEnable0Aux23	
21		0x0	AuxMeasEnable0Aux22	
20	Reserved	0x0	AuxMeasEnable0Aux21	
19	Reserved	0x0	AuxMeasEnable0Aux20	
18		0x0	AuxMeasEnable0Aux19	
17		0x0	AuxMeasEnable0Aux18	
16		0x0	AuxMeasEnable0Aux17	
15		0x0	AuxMeasEnable0Aux16	
14		0x0	AuxMeasEnable0Aux15	
13		0x0	AuxMeasEnable0Aux14	
12		0x0	AuxMeasEnable0Aux13	
11		0x0	AuxMeasEnable0Aux12	
10		0x0	AuxMeasEnable0Aux11	
9		0x0	AuxMeasEnable0Aux10	
8		0x0	AuxMeasEnable0Aux9	
7		0x0	AuxMeasEnable0Aux8	
6		0x0	AuxMeasEnable0Aux7	
5		0x0	AuxMeasEnable0Aux6	
4		0x0	AuxMeasEnable0Aux5	
3		0x0	AuxMeasEnable0Aux4	
2		0x0	AuxMeasEnable0Aux3	
1		0x0	AuxMeasEnable0Aux2	
0		0x0	AuxMeasEnable0Aux1	

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13.6.8 0x1E – Afe2MeasCfg4

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x1E		Register Name : Afe2MeasCfg4		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:25	Reserved	0x0		Reserved
24		0x0	SensBufDepth	Bridge Sensor data buffer depth in SRAM 0x0 : data buffer depth 1 0x1 : data buffer depth 8
23		0x0	IrqEnableEoauxaz	End of AZ Measurement 0x0 : IRQ disabled 0x1 : IRQ enabled
22		0x0	IrqEnableEoauxseq	End of Aux Sequence 0x0 : IRQ disabled 0x1 : IRQ enabled
21		0x0	IrqEnableEoauxins	End of Inserted AUX Measurement 0x0 : IRQ disabled 0x1 : IRQ enabled
20:5		0x0	IdleTime	In continuous cyclic measurement mode idle times up to 10ms can be asserted between two sequences. IdleTime represents a number of AFE clocks – 4MHz by default
4		0x0	AuxMeasEnable1Aux37	Enable CVC diagnosis leak_2 S- 0x0 : Aux measurement Skipped 0x1 : Aux measurement Executed
3		0x0	AuxMeasEnable1Aux36	Enable CVC diagnosis leak_2 S- 0x0 : Aux measurement Skipped 0x1 : Aux measurement Executed
2		0x0	AuxMeasEnable1Aux35	Enable CVC diagnosis leak_1 S+ 0x0 : Aux measurement Skipped 0x1 : Aux measurement Executed
1		0x0	AuxMeasEnable1Aux34	Enable CVC diagnosis leak_1 S- 0x0 : Aux measurement Skipped 0x1 : Aux measurement Executed
0	Reserved	0x0	AuxMeasEnable1Aux33	Reserved

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13.7 Diagnosis

13.7.1 0x1F – DiagSen.DiagCfg

Address : 0x1F		Register Name : DiagSen.DiagCfg		Default: 0x10000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:29	Reserved	0x0		Reserved
28:24		0x10	LeakTolVal	The Leakage Tolerance Register Value can be calculated like this: Register Value = (2^5 - 1) * LeakTolVal / 100
23:17	Reserved	0x0		Reserved
16:15		0x0	Extt3Range	Reference for Temp Sensor open check on T3 0x0 : 2MΩ 0x1 : 0.5MΩ 0x2 : 0.1MΩ 0x3 : Reserved
14		0x0	Extt3Pt100	Reference for temperature sensor short measurement on T3 0x0 : RT_SHORT < 500Ω 0x1 : RT_SHORT < 10Ω
13	Reserved	0x0		Reserved
12:11		0x0	Extt2Range	Reference for Temp Sensor open check on T2 0x0 : 2MΩ 0x1 : 0.5MΩ 0x2 : 0.1MΩ 0x3 : Reserved
10		0x0	Extt2Pt100	Reference for temperature sensor short measurement on T2 0x0 : RT_SHORT < 500Ω 0x1 : RT_SHORT < 10Ω
9	Reserved	0x0		Reserved
8:7		0x0	Extt1Range	Reference for Temp Sensor open check on T1 0x0 : 2MΩ 0x1 : 0.5MΩ 0x2 : 0.1MΩ 0x3 : Reserved
6		0x0	Extt1Pt100	Reference for temperature sensor short measurement on T1 0x0 : RT_SHORT < 500Ω 0x1 : RT_SHORT < 10Ω
5:4	Reserved	0x0	Afe2GainChkResDacVal	Reserved
3	Reserved	0x0	Afe2GainChkResDacEn	Reserved
2:1	Reserved	0x0	Afe1GainChkResDacVal	Reserved
0	Reserved	0x0	Afe1GainChkResDacEn	Reserved

13.7.2 0x20 – DiagSen.Range[0].Inp

Address : 0x20		Register Name : DiagSen.Range[0].Inp		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:16		0x0	Max	Reserved
15:0		0x0	Min	Reserved

13.7.3 0x21 – DiagSen.Range[0].Inn

Address : 0x21		Register Name : DiagSen.Range[0].Inn		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:16		0x0	Max	Reserved
15:0		0x0	Min	Reserved

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13.7.4 0x22 – DiagSen.Range[1].Inp

Address : 0x22		Register Name : DiagSen.Range[1].Inp		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:16		0x0	Max	Reserved
15:0		0x0	Min	Reserved

13.7.5 0x23 – DiagSen.Range[1].Inn

Address : 0x23		Register Name : DiagSen.Range[1].Inn		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:16		0x0	Max	Reserved
15:0		0x0	Min	Reserved

13.7.6 0x24 – DiagSen.GainChk[0]

Address : 0x24		Register Name : DiagSen.GainChk[0]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:16	Reserved	0x0	TolVal	Reserved
15:0	Reserved	0x0	RefVal	Reserved

13.7.7 0x25 – DiagSen.GainChk[1]

Address : 0x25		Register Name : DiagSen.GainChk[1]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:16	Reserved	0x0	TolVal	Reserved
15:0	Reserved	0x0	RefVal	Reserved

13.7.8 0x26 – DiagSen.OfstChk[0]

Address : 0x26		Register Name : DiagSen.OfstChk[0]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:16	Reserved	0x0	TolVal	Reserved
15:0	Reserved	0x0	RefVal	Reserved

13.7.9 0x27 – DiagSen.OfstChk[1]

Address : 0x27		Register Name : DiagSen.OfstChk[1]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:16	Reserved	0x0	TolVal	Reserved
15:0	Reserved	0x0	RefVal	Reserved

13.8 Temperature Channel Mapping

13.8.1 0x28 – TempMapChId

Wrong setting of this parameter hinders firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x28		Register Name : TempMapChId		Default: 0x00000002
Bits	**Access**	**Default**	**Field Name**	**Description**
31:9	Reserved	0x0		Reserved
8:6		0x0	Tch3	Temperature Sensor Source for Temperature Channels 1, 2, 3 0x0 : None 0x1 : PTAT 0x2 : T1 0x3 : T2 0x4 : T3 0x5 to 0x7 : Reserved
5:3		0x0	Tch2	
2:0		0x2	Tch1	

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13.9 SSC Algorithm Selection

13.9.1 0x29 – MathSbrAlgoSel

Address : 0x29		Register Name : MathSbrAlgoSel		Default: 0x04040011
Bits	**Access**	**Default**	**Field Name**	**Description**
31	Reserved	0x0		Reserved
30:24		0x4	DigGain2	Digital gain 1 Digital gain that can be used for capacitive measurement. Not all modes allow using full range up to digital gain of 31. 0x0 : 0 0x1 : 0.25 0x2 : 0.5 ... 0x1F : 7.75 0x20 : 8 ... 0x7C : 31
23	Reserved	0x0		Reserved
22:16		0x4	DigGain1	Digital gain 1 Digital gain that can be used for capacitive measurement. Not all modes allow using full range up to digital gain of 31. 0x0 : 0 0x1 : 0.25 0x2 : 0.5 ... 0x1F : 7.75 0x20 : 8 ... 0x7C : 31
15:12	Reserved	0x0		Reserved
11		0x0	TlcChOrder	Third Logic Channel Operand Order 0x0 : CH1 op CH2 0x1 : CH2 op CH1
10:8		0x0	TlcOp	Third Logic Channel Operation 0x0 : Subtraction 0x1 : Division 0x2 : Ratio 0x3 : Reserved
7:4		0x1	Sensor2	SSC Algorithm for Bridge Sensors 1 & 2 0x0 : None 0x1 : SOT Parabolic 0x2 : SOT S-Shaped 0x3 : Reserved
3:0		0x1	Sensor1	

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13.10 Analog Output (AOUT)

13.10.1 0x2A – AoutSelParam

Address : 0x2A		Register Name : AoutSelParam		Default: 0x00000001
Bits	**Access**	**Default**	**Field Name**	**Description**
31:7	Reserved	0x0		Reserved
6:3		0x0	AoutModSel	Analog Output Driver Mode 0x0 : Disabled 0x1 : Absolute Voltage Output 0-10V 0x2 : Absolute Voltage Output 0-5V 0x3 : Absolute Voltage Output 0-1V 0x4 : Reserved 0x5 : Reserved 0x6 : 3-Wire Current Loop 0x7 : Reserved 0x8 : Absolute Voltage Output 0-3V 0x9 to 0xF : Reserved
2:0		0x1	SelAfeForDac	Source Signal for Analog Output 0x0 : None 0x1 : Sensor Channel 1 0x2 : Sensor Channel 2 0x3 : Third Logic Channel (TLC) 0x4 : Temperature Channel 1 0x5 : Temperature Channel 2 0x6 : Temperature Channel 3 0x7 : Reserved

13.10.2 0x2B – AoutRegCtrl

Address : 0x2B		Register Name : AoutRegCtrl		Default: 0x0000001A
Bits	**Access**	**Default**	**Field Name**	**Description**
31:13	Reserved	0x0		Reserved
12:11		0x0	Aout5vRdacRefSel	Selection for RDAC reference voltage 0x0 : VDD 0x1 : internal 3.1V regulator voltage
10:9		0x0	AoutVddnLoad	VDDN Charge Pump Load Current 0x0 : 0.5mA | 0x2 : 3mA 0x1 : 1mA | 0x3 : 5mA
8		0x0	AoutVddnEn	VDDN Charge Pump for Negative Supply 0x0 : Disabled 0x1 : Enabled
7		0x0	AoutOffsetCompOff	Analog Output Offset Compensation 0x0 : Disabled 0x1 : Enabled
6:5		0x0	AoutCurrLim	Analog Driver Output Current Limitation 0x0 : 6mA | 0x2 : 18mA 0x1 : 12mA | 0x3 : 25mA
4		0x1	AoutFeedBackEn	Analog Driver Feedback 0x0 : External 0x1 : Internal
3		0x1	AoutHighPowEn	Analog Driver Output Power 0x0 : Low Power 0x1 : High Power
2:1		0x1	AoutMode	Analog Output Mode 0x0 : Reserved 0x1 : VOUT 5V 0x2 : VOUT 1V 0x3 : Reserved
0		0x0	AoutEn	Analog Output Activation 0x0 : Disabled 0x1 : Enabled

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13.10.3 0x2C – AoutRegDiag

Address : 0x2C	Register Name : AoutRegDiag			Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:4	Reserved	0x0		Reserved
3	Reserved	0x0	AoutDiagVddaEn	Reserved
2:1	Reserved	0x0	AoutDiagOutValue	Reserved
0	Reserved	0x0	AoutDiagOutEn	Reserved

13.10.4 0x2D – AoutCl3Coeff

Address : 0x2D	Register Name : AoutCl3Coeff			Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:16		0x0	ClDelta	3-Wire Current Loop Calibration Coefficient CL3_Delta 16-bit Value
15:0		0x0	ClOffset	3-Wire Current Loop Calibration Coefficient CL3_Offset 16-bit Value

13.11 System Startup

13.11.1 0x2E – StartupParamCfg

Address : 0x2E	Register Name : StartupParamCfg			Default: 0x00000001
Bits	**Access**	**Default**	**Field Name**	**Description**
31:1	Reserved	0x0		Reserved
0		0x1	StartupMode	System Startup Mode 0x0 : Cyclic Mode 0x1 : Command Mode

13.12 IIR Filter

13.12.1 0x2F – IirFiltCoeffReg

Address : 0x2F	Register Name : IirFiltCoeffReg			Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:30	Reserved	0x0		Reserved
29:27		0x0	FiltTemp3Diff	IIR *FiltDiff* Value Temperature Channel 3
26:24		0x0	FiltTemp3Avg	IIR *FiltAvg* Value Temperature Channel 3
23:21		0x0	FiltTemp2Diff	IIR *FiltDiff* Value Temperature Channel 2
20:18		0x0	FiltTemp2Avg	IIR *FiltAvg* Value Temperature Channel 2
17:15		0x0	FiltTemp1Diff	IIR *FiltDiff* Value Temperature Channel 1
14:12		0x0	FiltTemp1Avg	IIR *FiltAvg* Value Temperature Channel 1
11:9		0x0	FiltSbr2Diff	IIR *FiltDiff* Value Sensor Bridge 2
8:6		0x0	FiltSbr2Avg	IIR *FiltAvg* Value Sensor Bridge 2
5:3		0x0	FiltSbr1Diff	IIR *FiltDiff* Value Sensor Bridge 1
2:0		0x0	FiltSbr1Avg	IIR *FiltAvg* Value Sensor Bridge 1

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13.13 General AFE Configuration

13.13.1 0x30 – AfeConfig

Address : 0x30		Register Name : AfeConfig		Default: 0x20000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31	Reserved	0x0	CLMode	Reserved
30:26	Reserved	0x8	AfeMisc	Reserved
25	Reserved	0x0	Afe2LowSpeed	Reserved
24		0x0	CM2En	Capacitive Sensor AFE2 0x0 : Disabled 0x1 : Enabled
23		0x0	CM1En	Capacitive Sensor AFE1 0x0 : Disabled 0x1 : Enabled
22	Reserved	0x0	Vdda3Brownout	Reserved
21	Reserved	0x0	Vdda2Brownout	Reserved
20	Reserved	0x0	Vdda1Brownout	Reserved
19	Reserved	0x0	CMDitheringEnable	Reserved
18	Reserved	0x0	CMNoiseInt1	Reserved
17	Reserved	0x0	TNoiseInt1	Reserved
16	Reserved	0x0	ExtTemp3NoiseInt1	Reserved
15	Reserved	0x0	ExtTemp2NoiseInt1	Reserved
14	Reserved	0x0	ExtTemp1NoiseInt1	Reserved
13	Reserved	0x0	BM2NoiseInt1	Reserved
12	Reserved	0x0	BM1NoiseInt1	Reserved
11:10	Reserved	0x0	TChpMode	Reserved
9:8	Reserved	0x0	ExtTemp3ChpMode	Reserved
7:6	Reserved	0x0	ExtTemp2ChpMode	Reserved
5:4	Reserved	0x0	ExtTemp1ChpMode	Reserved
3:2	Reserved	0x0	BM2ChpMode	Reserved
1:0	Reserved	0x0	BM1ChpMode	Reserved

13.14 Output Clipping, Diagnostic Range Assignment

13.14.1 0x31 – DiagClipOutCfg.SysDiagCfg

Address : 0x31		Register Name : DiagClipOutCfg.SysDiagCfg		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:28	Reserved	0x0		Reserved
27:24	Reserved	0x0	WatchdogTimeout	Reserved
23:16	Reserved	0x0	WatchdogDisableKey	Reserved
15:2	Reserved	0x0		Reserved
1		0x0	ClipOutEn	Two-Sided Clipping to Upper and Lower Diagnostic Limit 0x0 : Disabled 0x1 : Enabled **Note:** Enabling this feature requires enabling ClipOutEn. **Note:** DiagOutEn sets the AOUT to either 0% (LDR) or 100% (UDR) **Note:** UDR will have higher priority than LDR if configuration mixes both failure output signalization states. Failure signalization of saturation requires enabling of any additional AFE or sensor diagnosis functions.
0		0x0	DiagOutEn	Output Signalization of Diagnostic State at AOUT 0x0 : Disabled 0x1 : Enabled **Note:** Clipping limits are defined in DiagClipOutCfg.ClipOutLvl register.

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13.14.2 0x32 – DiagClipOutCfg.DiagOutLvl[0]

Address : 0x32		Register Name : DiagClipOutCfg.DiagOutLvl[0]		Default: 0x00007FFE
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x7FFE	DiagOutLvl[0]	UDR / LDR assignment of diagnostic checks Bit 1 : Br1InpOrInnOpen Bit 2 : Br1InpAndInnShorted Bit 7 : Br2InpOrInnOpen Bit 8 : Br2InpAndInnShorted Bit 16 : T1CheckOpen Bit 17 : T1CheckShortToTop Bit 18 : T1CheckShortToBottom Bit 19 : T2CheckOpen Bit 20 : T2CheckShortToTop Bit 21 : T2CheckShortToBottom Bit 22 : T3CheckOpen Bit 23 : T3CheckShortToTop Bit 24 : T3CheckShortToBottom All other bits reserved Bit Value Meaning 0 : LDR Selection 1 : UDR Selection

13.14.3 0x33 – DiagClipOutCfg.DiagOutLvl[1]

Address : 0x33		Register Name : DiagClipOutCfg.DiagOutLvl[1]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0	Reserved	0x0	DiagOutLvl[1]	Second select register for UDR / LDR assignment of diagnostic checks

13.14.4 0x34 – DiagClipOutCfg.DiagOutLvl[2]

Address : 0x34		Register Name : DiagClipOutCfg.DiagOutLvl[2]		Default: 0x0000003F
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0	Reserved	0x3F	DiagOutLvl[2]	Third select register for UDR / LDR assignment of diagnostic checks

13.14.5 0x35 – DiagClipOutCfg.ClipOutLvl

Address : 0x35		Register Name : DiagClipOutCfg.ClipOutLvl		Default: 0xF3330CCC
Bits	**Access**	**Default**	**Field Name**	**Description**
31:16		0xF333	ClipOutHigh	Upper Clipping Limit 0xF333 : 95% Full Scale
15:0		0xCCC	ClipOutLow	Lower Clipping Limit 0x0CCC : 5% Full Scale

13.15 SSC Coefficients

13.15.1 0x36 – Bs1Coeff.SOffset

Address : 0x36		Register Name : Bs1Coeff.SOffset		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	SOffset	Sensor offset term *Offset_S*

13.15.2 0x37 – Bs1Coeff.SGain

Address : 0x37		Register Name : Bs1Coeff.SGain		Default: 0x00200000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x200000	SGain	Sensor gain term *Gain_S*

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13.15.3 0x38 – Bs1Coeff.SSot

Address : 0x38		Register Name : Bs1Coeff.SSot		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	SSot	Second-order term for sensor non-linearity *SOT_sens*

13.15.4 0x39 – Bs1Coeff.SShift

Address : 0x39		Register Name : Bs1Coeff.SShift		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	SShift	Post-calibration term *SENS_shift*

13.15.5 0x3A – Bs1Coeff.STco

Address : 0x3A		Register Name : Bs1Coeff.STco		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	STco	Temperature coefficient offset term *Tco*

13.15.6 0x3B – Bs1Coeff.SSotTco

Address : 0x3B		Register Name : Bs1Coeff.SSotTco		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	SSotTco	Second-order term for Tco nonlinearity *SOT_tco*

13.15.7 0x3C – Bs1Coeff.STcg

Address : 0x3C		Register Name : Bs1Coeff.STcg		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	STcg	Temperature coefficient gain term *Tcg*

13.15.8 0x3D – Bs1Coeff.SSotTcg

Address : 0x3D		Register Name : Bs1Coeff.SSotTcg		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	SSotTcg	Second-order term for Tcg non-linearity *SOT_tcg*

13.15.9 0x3E – Bs1Coeff.OutScaleGain

Address : 0x3E		Register Name : Bs1Coeff.OutScaleGain		Default: 0x00100000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x100000	OutScaleGain	Post SSC Output Scaling Gain

13.15.10 0x3F – Bs1Coeff.OutScaleOfst

Address : 0x3F		Register Name : Bs1Coeff.OutScaleOfst		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	OutScaleOfst	Post SSC Output Scaling Offset

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13.15.11 0x40 – Bs2Coeff.SOffset

Address : 0x40			Register Name : Bs2Coeff.SOffset		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x0	SOffset	Sensor offset term *Offset_S*	

13.15.12 0x41 – Bs2Coeff.SGain

Address : 0x41			Register Name : Bs2Coeff.SGain		Default: 0x00200000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x200000	SGain	Sensor gain term *Gain_S*	

13.15.13 0x42 – Bs2Coeff.SSot

Address : 0x42			Register Name : Bs2Coeff.SSot		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x0	SSot	Second-order term for sensor non-linearity *SOT_sens*	

13.15.14 0x43 – Bs2Coeff.SShift

Address : 0x43			Register Name : Bs2Coeff.SShift		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x0	SShift	Post-calibration term *SENS_shift*	

13.15.15 0x44 – Bs2Coeff.STco

Address : 0x44			Register Name : Bs2Coeff.STco		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x0	STco	Temperature coefficient offset term *Tco*	

13.15.16 0x45 – Bs2Coeff.SSotTco

Address : 0x45			Register Name : Bs2Coeff.SSotTco		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x0	SSotTco	Second-order term for Tco nonlinearity *SOT_tco*	

13.15.17 0x46 – Bs2Coeff.STcg

Address : 0x46			Register Name : Bs2Coeff.STcg		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x0	STcg	Temperature coefficient gain term *Tcg*	

13.15.18 0x47 – Bs2Coeff.SSotTcg

Address : 0x47			Register Name : Bs2Coeff.SSotTcg		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x0	SSotTcg	Second-order term for Tcg non-linearity *SOT_tcg*	

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13.15.19 0x48 – Bs2Coeff.OutScaleGain

Address : 0x48		Register Name : Bs2Coeff.OutScaleGain			Default: 0x00100000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x100000	OutScaleGain	Post SSC Output Scaling Gain	

13.15.20 0x49 – Bs2Coeff.OutScaleOfst

Address : 0x49		Register Name : Bs2Coeff.OutScaleOfst			Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x0	OutScaleOfst	Post SSC Output Scaling Offset	

13.15.21 0x4A – Tch1Coeff.TOffset

Address : 0x4A		Register Name : Tch1Coeff.TOffset			Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x0	TOffset	Offset coefficient for temperature *Offset_T*	

13.15.22 0x4B – Tch1Coeff.TGain

Address : 0x4B		Register Name : Tch1Coeff.TGain			Default: 0x00200000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x200000	TGain	Gain coefficient for temperature *Gain_T*	

13.15.23 0x4C – Tch1Coeff.TSot

Address : 0x4C		Register Name : Tch1Coeff.TSot			Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x0	TSot	Second-order term for temperature source *SOT_T*	

13.15.24 0x4D – Tch1Coeff.TShift

Address : 0x4D		Register Name : Tch1Coeff.TShift			Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x0	TShift	Shift for post-calibration/post-assembly offset compensation *T_Shift*	

13.15.25 0x4E – Tch2Coeff.TOffset

Address : 0x4E		Register Name : Tch2Coeff.TOffset			Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x0	TOffset	Offset coefficient for temperature *Offset_T*	

13.15.26 0x4F – Tch2Coeff.TGain

Address : 0x4F		Register Name : Tch2Coeff.TGain			Default: 0x00200000
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24	Reserved	0x0		Reserved	
23:0		0x200000	TGain	Gain coefficient for temperature *Gain_T*	

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13.15.27 0x50 – Tch2Coeff.TSot

Address : 0x50		Register Name : Tch2Coeff.TSot		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	TSot	Second-order term for temperature source *SOT_T*

13.15.28 0x51 – Tch2Coeff.TShift

Address : 0x51		Register Name : Tch2Coeff.TShift		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	TShift	Shift for post-calibration/post-assembly offset compensation *T_Shift*

13.15.29 0x52 – Tch3Coeff.TOffset

Address : 0x52		Register Name : Tch3Coeff.TOffset		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	TOffset	Offset coefficient for temperature *Offset_T*

13.15.30 0x53 – Tch3Coeff.TGain

Address : 0x53		Register Name : Tch3Coeff.TGain		Default: 0x00200000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x200000	TGain	Gain coefficient for temperature *Gain_T*

13.15.31 0x54 – Tch3Coeff.TSot

Address : 0x54		Register Name : Tch3Coeff.TSot		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	TSot	Second-order term for temperature source *SOT_T*

13.15.32 0x55 – Tch3Coeff.TShift

Address : 0x55		Register Name : Tch3Coeff.TShift		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x0	TShift	Shift for post-calibration/post-assembly offset compensation *T_Shift*

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13.16 AFE Sequencer - Part II

13.16.1 0x73 – Afe1MeasCfg5

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x73		Register Name : Afe1MeasCfg5		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31		0x0	AuxMeasEmpty0Aux32	Defines Empty Auxiliary Measurement Task AFE1 0x0 : Disabled 0x1 : Enabled
30		0x0	AuxMeasEmpty0Aux31	
29		0x0	AuxMeasEmpty0Aux30	
28		0x0	AuxMeasEmpty0Aux29	
27		0x0	AuxMeasEmpty0Aux28	
26		0x0	AuxMeasEmpty0Aux27	
25		0x0	AuxMeasEmpty0Aux26	
24		0x0	AuxMeasEmpty0Aux25	
23		0x0	AuxMeasEmpty0Aux24	
22		0x0	AuxMeasEmpty0Aux23	
21		0x0	AuxMeasEmpty0Aux22	
20		0x0	AuxMeasEmpty0Aux21	
19		0x0	AuxMeasEmpty0Aux20	
18		0x0	AuxMeasEmpty0Aux19	
17		0x0	AuxMeasEmpty0Aux18	
16		0x0	AuxMeasEmpty0Aux17	
15		0x0	AuxMeasEmpty0Aux16	
14		0x0	AuxMeasEmpty0Aux15	
13		0x0	AuxMeasEmpty0Aux14	
12		0x0	AuxMeasEmpty0Aux13	
11		0x0	AuxMeasEmpty0Aux12	
10		0x0	AuxMeasEmpty0Aux11	
9		0x0	AuxMeasEmpty0Aux10	
8		0x0	AuxMeasEmpty0Aux9	
7		0x0	AuxMeasEmpty0Aux8	
6		0x0	AuxMeasEmpty0Aux7	
5		0x0	AuxMeasEmpty0Aux6	
4		0x0	AuxMeasEmpty0Aux5	
3		0x0	AuxMeasEmpty0Aux4	
2		0x0	AuxMeasEmpty0Aux3	
1		0x0	AuxMeasEmpty0Aux2	
0		0x0	AuxMeasEmpty0Aux1	

13.16.2 0x74 – Afe1MeasCfg6

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x74		Register Name : Afe1MeasCfg6		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:5	Reserved	0x0		Reserved
4		0x0	AuxMeasEmpty1Aux37	Defines Empty Auxiliary Measurement Task AFE1 0x0 : Disabled 0x1 : Enabled
3		0x0	AuxMeasEmpty1Aux36	
2		0x0	AuxMeasEmpty1Aux35	
1		0x0	AuxMeasEmpty1Aux34	
0		0x0	AuxMeasEmpty1Aux33	

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13.16.3 0x75 – Afe2MeasCfg5

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x75		Register Name : Afe2MeasCfg5		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31		0x0	AuxMeasEmpty0Aux32	Defines Empty Auxiliary Measurement Task AFE2 0x0 : Disabled 0x1 : Enabled
30		0x0	AuxMeasEmpty0Aux31	
29		0x0	AuxMeasEmpty0Aux30	
28		0x0	AuxMeasEmpty0Aux29	
27		0x0	AuxMeasEmpty0Aux28	
26		0x0	AuxMeasEmpty0Aux27	
25		0x0	AuxMeasEmpty0Aux26	
24		0x0	AuxMeasEmpty0Aux25	
23		0x0	AuxMeasEmpty0Aux24	
22		0x0	AuxMeasEmpty0Aux23	
21		0x0	AuxMeasEmpty0Aux22	
20		0x0	AuxMeasEmpty0Aux21	
19		0x0	AuxMeasEmpty0Aux20	
18		0x0	AuxMeasEmpty0Aux19	
17		0x0	AuxMeasEmpty0Aux18	
16		0x0	AuxMeasEmpty0Aux17	
15		0x0	AuxMeasEmpty0Aux16	
14		0x0	AuxMeasEmpty0Aux15	
13		0x0	AuxMeasEmpty0Aux14	
12		0x0	AuxMeasEmpty0Aux13	
11		0x0	AuxMeasEmpty0Aux12	
10		0x0	AuxMeasEmpty0Aux11	
9		0x0	AuxMeasEmpty0Aux10	
8		0x0	AuxMeasEmpty0Aux9	
7		0x0	AuxMeasEmpty0Aux8	
6		0x0	AuxMeasEmpty0Aux7	
5		0x0	AuxMeasEmpty0Aux6	
4		0x0	AuxMeasEmpty0Aux5	
3		0x0	AuxMeasEmpty0Aux4	
2		0x0	AuxMeasEmpty0Aux3	
1		0x0	AuxMeasEmpty0Aux2	
0		0x0	AuxMeasEmpty0Aux1	

13.16.4 0x76 – Afe2MeasCfg6

Wrong setting of this parameter can corrupt firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0x76		Register Name : Afe2MeasCfg6		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:5	Reserved	0x0		Reserved
4		0x0	AuxMeasEmpty1Aux37	Defines Empty Auxiliary Measurement Task AFE2 0x0 : Disabled 0x1 : Enabled
3		0x0	AuxMeasEmpty1Aux36	
2		0x0	AuxMeasEmpty1Aux35	
1		0x0	AuxMeasEmpty1Aux34	
0		0x0	AuxMeasEmpty1Aux33	

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13.17 Zero Adjustment

13.17.1 0x77 – ZeroAdjConfig.Channels[0]

Address : 0x77		Register Name : ZeroAdjConfig.Channels[0]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	OffsetWindow	Zero Adjustment: Offset Window for Sensor Channel 1
23:0		0x0	Ref	Zero Adjustment: Reference Value for Sensor Channel 1

13.17.2 0x78 – ZeroAdjConfig.Channels[1]

Address : 0x78		Register Name : ZeroAdjConfig.Channels[1]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	OffsetWindow	Zero Adjustment: Offset Window for Sensor Channel 2
23:0		0x0	Ref	Zero Adjustment: Reference Value for Sensor Channel 2

13.17.3 0x79 – ZeroAdjConfig.Channels[2]

Address : 0x79		Register Name : ZeroAdjConfig.Channels[2]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	OffsetWindow	Zero Adjustment: Offset Window for Temperature Channel 1
23:0		0x0	Ref	Zero Adjustment: Reference Value for Temperature Channel 1

13.17.4 0x7A – ZeroAdjConfig.Channels[3]

Address : 0x7A		Register Name : ZeroAdjConfig.Channels[3]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	OffsetWindow	Zero Adjustment: Offset Window for Temperature Channel 2
23:0		0x0	Ref	Zero Adjustment: Reference Value for Temperature Channel 2

13.17.5 0x7B – ZeroAdjConfig.Channels[4]

Address : 0x7B		Register Name : ZeroAdjConfig.Channels[4]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	OffsetWindow	Zero Adjustment: Offset Window for Temperature Channel 3
23:0		0x0	Ref	Zero Adjustment: Reference Value for Temperature Channel 3

13.17.6 0x7C – ZeroAdjConfig.Options

Address : 0x7C		Register Name : ZeroAdjConfig.Options		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:7	Reserved	0x0		Reserved
6:4		0x0	MdcSel	MDC Channel selection for ZAT 0x0 : All MDCs 0x1 : MDC1 0x2 to 0x7 : Reserved
3		0x0	GpioPolarity	GPIO Trigger select for ZAT 0x0 : Rising Edge 0x1 : Falling Edge
2:1		0x0	TriggerMode	Define Function of ZAT pin 0x0 : Disabled 0x1 : SIO Only 0x2 : IO-Link COM Only 0x3 : SIO an IO-Link COM **Note**: This feature can only be enabled when the *ZeroAdjConfig.Options.FeatureEna* option is enabled.
0		0x0	FeatureEna	Enable Zero Adjustment 0x0 : Disabled 0x1 : Enabled

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13.18 Capacitive Front End

13.18.1 0x7D – CapCtrl

Address : 0x7D		Register Name : CapCtrl		Default: 0x00000100
Bits	**Access**	**Default**	**Field Name**	**Description**
31:14	Reserved	0x0		Reserved
13:12		0x0	FreqDivClkAfe	Clock Divider HighSpeedClock to AFE Clock 0x0 : div4 (4MHz AFE clock) [AFE Speed Reduction 1x] 0x1 : div8 (2MHz AFE clock) [AFE Speed Reduction 2x] 0x2 : div16 (1MHz AFE clock) [AFE Speed Reduction 4x]
11:8		0x1	SensorAppMode	Capacitive sensor application mode 0x0 : Reserved 0x1 : Application Mode 1 0x2 : Application Mode 2 0x3 : Application Mode 3 0x4 : Application Mode 4 0x5 : Application Mode 5 0x6 : Application Mode 6 0x7 to 0xA : Reserved 0xB : Application Mode 11 0xC to 0xF : Reserved
7:5	Reserved	0x0		Reserved
4		0x0	CsInvEnable	Enable 1/C linearization calculation 0x0 : Disabled 0x1 : Enabled
3:2	Reserved	0x0		Reserved
1:0		0x0	ResCapSel	Resistive/Capacitive mode selector 0x0 : Resistive Measurement Only 0x1 : Capacitive Measurement Only

13.18.2 0x7E – CsInvParam

Address : 0x7E		Register Name : CsInvParam		Default: 0x00080000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24	Reserved	0x0		Reserved
23:0		0x80000	RValue	Range-shift value

13.19 CCP CRC

13.19.1 0x7F – CrcCcp0

Address : 0x7F		Register Name : CrcCcp0		Default: 0xB6A91F52
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0xB6A91F52	CrcCcp0	CRC of CCP Page 0

13.20 IO-Link – SI Scaling

13.20.1 0xA0 – SiScaling.Coeff[0].Offset

Address : 0xA0		Register Name : SiScaling.Coeff[0].Offset		Default: 0xFFFF8300
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0xFFFF8300	Offset	SI Scaling Offset for MDC1

13.20.2 0xA1 – SiScaling.Coeff[0].Gain

Address : 0xA1		Register Name : SiScaling.Coeff[0].Gain		Default: 0x00000FA0
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0xFA0	Gain	SI Scaling Gain for MDC1

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13.20.3 0xA2 – SiScaling.Coeff[1].Offset

Address : 0xA2		Register Name : SiScaling.Coeff[1].Offset		Default: 0xFFFF8000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0xFFFF8000	Offset	SI Scaling Offset for MDC2 (N/A for SSP 4.1.1)

13.20.4 0xA3 – SiScaling.Coeff[1].Gain

Address : 0xA3		Register Name : SiScaling.Coeff[1].Gain		Default: 0x00001000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x1000	Gain	SI Scaling Gain for MDC2 (N/A for SSP 4.1.1)

13.20.5 0xA4 – SiScaling.Coeff[2].Offset

Address : 0xA4		Register Name : SiScaling.Coeff[2].Offset		Default: 0xFFFF8000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0xFFFF8000	Offset	SI Scaling Offset for MDC3 (N/A for SSP 4.1.1)

13.20.6 0xA5 – SiScaling.Coeff[2].Gain

Address : 0xA5		Register Name : SiScaling.Coeff[2].Gain		Default: 0x00001000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x1000	Gain	SI Scaling Gain for MDC3 (N/A for SSP 4.1.1)

13.20.7 0xA6 – SiScaling.Coeff[3].Offset

Address : 0xA6		Register Name : SiScaling.Coeff[3].Offset		Default: 0xFFFF8000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0xFFFF8000	Offset	SI Scaling Offset for MDC4 (N/A for SSP 4.1.1)

13.20.8 0xA7 – SiScaling.Coeff[3].Gain

Address : 0xA7		Register Name : SiScaling.Coeff[3].Gain		Default: 0x00001000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x1000	Gain	SI Scaling Gain for MDC4 (N/A for SSP 4.1.1)

13.20.9 0xA8 – SiScaling.OffsetScaler

Address : 0xA8		Register Name : SiScaling.OffsetScaler		Default: 0x01010101
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x1	Ch4	SI Scaling Offset Scaler for MDC4 (N/A for SSP 4.1.1)
23:16		0x1	Ch3	SI Scaling Offset Scaler for MDC3 (N/A for SSP 4.1.1)
15:8		0x1	Ch2	SI Scaling Offset Scaler for MDC2 (N/A for SSP 4.1.1)
7:0		0x1	Ch1	SI Scaling Offset Scaler for MDC1 (N/A for SSP 4.1.1)

13.21 IO-Link – Measurement Data Channel (MDC) Description

13.21.1 0xA9 – MdcDescr[0].LowerValue

Address : 0xA9		Register Name : MdcDescr[0].LowerValue		Default: 0xFFFF8300
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0xFFFF8300	LowerValue	Lower value of measurement range for MDC1 - transmitted in ISDU 0x4080 Subindex 0x1

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13.21.2 0xAA – MdcDescr[0].UpperValue

Address : 0xAA		Register Name : MdcDescr[0].UpperValue		Default: 0x00007D00
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x7D00	UpperValue	Upper value of measurement range for MDC1 - transmitted in ISDU 0x4080 Subindex 0x2

13.21.3 0xAB – MdcDescr[0].Reg1

Address : 0xAB		Register Name : MdcDescr[0].Reg1		Default: 0x0003046A
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Unused	Unused
23:16		0x3	Scale	Range shifting (10scale) for MDC1 - transmitted in ISDU 0x4080 Subindex 0x4
15:0		0x46A	UnitCode	Unit Code (SI unit) for MDC1 - transmitted in ISDU 0x4080 Subindex 0x3

13.21.4 0xAC – MdcDescr[1].LowerValue

Address : 0xAC		Register Name : MdcDescr[1].LowerValue		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x0	LowerValue	Lower value of measurement range for MDC2 (N/A for SSP 4.1.1)

13.21.5 0xAD – MdcDescr[1].UpperValue

Address : 0xAD		Register Name : MdcDescr[1].UpperValue		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x0	UpperValue	Upper value of measurement range for MDC2 (N/A for SSP 4.1.1)

13.21.6 0xAE – MdcDescr[1].Reg1

Address : 0xAE		Register Name : MdcDescr[1].Reg1		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Unused	Unused (N/A for SSP 4.1.1)
23:16		0x0	Scale	Range shifting (10scale) for MDC2 (N/A for SSP 4.1.1)
15:0		0x0	UnitCode	Unit Code (SI unit) for MDC2 (N/A for SSP 4.1.1)

13.21.7 0xAF – MdcDescr[2].LowerValue

Address : 0xAF		Register Name : MdcDescr[2].LowerValue		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x0	LowerValue	Lower value of measurement range for MDC3 (N/A for SSP 4.1.1)

13.21.8 0xB0 – MdcDescr[2].UpperValue

Address : 0xB0		Register Name : MdcDescr[2].UpperValue		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x0	UpperValue	Upper value of measurement range for MDC3 (N/A for SSP 4.1.1)

13.21.9 0xB1 – MdcDescr[2].Reg1

Address : 0xB1		Register Name : MdcDescr[2].Reg1		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Unused	Unused (N/A for SSP 4.1.1)
23:16		0x0	Scale	Range shifting (10scale) for MDC3 (N/A for SSP 4.1.1)
15:0		0x0	UnitCode	Unit Code (SI unit) for MDC3 (N/A for SSP 4.1.1)

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13.21.10 0xB2 – MdcDescr[3].LowerValue

Address : 0xB2		Register Name : MdcDescr[3].LowerValue		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x0	LowerValue	Lower value of measurement range for MDC4 (N/A for SSP 4.1.1)

13.21.11 0xB3 – MdcDescr[3].UpperValue

Address : 0xB3		Register Name : MdcDescr[3].UpperValue		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x0	UpperValue	Upper value of measurement range for MDC4 (N/A for SSP 4.1.1)

13.21.12 0xB4 – MdcDescr[3].Reg1

Address : 0xB4		Register Name : MdcDescr[3].Reg1		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Unused	Unused (N/A for SSP 4.1.1)
23:16		0x0	Scale	Range shifting (10scale) for MDC4 (N/A for SSP 4.1.1)
15:0		0x0	UnitCode	Unit Code (SI unit) for MDC4 (N/A for SSP 4.1.1)

13.22 IO-Link – SSP Channel Mapping

13.22.1 0xB5 – SspChMap

Address : 0xB5		Register Name : SspChMap		Default: 0x00006660
Bits	**Access**	**Default**	**Field Name**	**Description**
31:16	Reserved	0x0		Reserved
15:12		0x6	Ch4	Mapped Data Channel for MDC4 (N/A for SSP 4.1.1)
11:8		0x6	Ch3	Mapped Data Channel for MDC3 (N/A for SSP 4.1.1)
7:4		0x6	Ch2	Mapped Data Channel for MDC2 (N/A for SSP 4.1.1)
3:0		0x0	Ch1	Mapped Data Channel for MDC1 0x0 : Sensor Channel 1 0x1 : Sensor Channel 2 0x2 : Third Logic Channel (TLC) 0x3 : Temperature Channel 1 0x4 : Temperature Channel 2 0x5 : Temperature Channel 3 0x6 : Reserved 0x7 : Reserved

13.23 IO-Link – Vendor Text

13.23.1 0xB6 – VendorText[0]

Address : 0xB6		Register Name : VendorText[0]		Default: 0x62206F54
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x62	Character4	Vendor Text - transmitted in ISDU 0x0011
23:16		0x20	Character3	
15:8		0x6F	Character2	
7:0		0x54	Character1	

13.23.2 0xB7 – VendorText[1]

Address : 0xB7		Register Name : VendorText[1]		Default: 0x69662065
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x69	Character8	Vendor Text - transmitted in ISDU 0x0011
23:16		0x66	Character7	
15:8		0x20	Character6	
7:0		0x65	Character5	

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13.23.3 0xB8 – VendorText[2]

Address : 0xB8		Register Name : VendorText[2]			Default: 0x64656C6C
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24		0x64	Character12	Vendor Text - transmitted in ISDU 0x0011	
23:16		0x65	Character11		
15:8		0x6C	Character10		
7:0		0x6C	Character9		

13.23.4 0xB9 – VendorText[3]

Address : 0xB9		Register Name : VendorText[3]			Default: 0x20796220
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24		0x20	Character16	Vendor Text - transmitted in ISDU 0x0011	
23:16		0x79	Character15		
15:8		0x62	Character14		
7:0		0x20	Character13		

13.23.5 0xBA – VendorText[4]

Address : 0xBA		Register Name : VendorText[4]			Default: 0x656E6552
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24		0x65	Character20	Vendor Text - transmitted in ISDU 0x0011	
23:16		0x6E	Character19		
15:8		0x65	Character18		
7:0		0x52	Character17		

13.23.6 0xBB – VendorText[5]

Address : 0xBB		Register Name : VendorText[5]			Default: 0x20736173
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24		0x20	Character24	Vendor Text - transmitted in ISDU 0x0011	
23:16		0x73	Character23		
15:8		0x61	Character22		
7:0		0x73	Character21		

13.23.7 0xBC – VendorText[6]

Address : 0xBC		Register Name : VendorText[6]			Default: 0x74737563
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24		0x74	Character28	Vendor Text - transmitted in ISDU 0x0011	
23:16		0x73	Character27		
15:8		0x75	Character26		
7:0		0x63	Character25		

13.23.8 0xBD – VendorText[7]

Address : 0xBD		Register Name : VendorText[7]			Default: 0x72656D6F
Bits	**Access**	**Default**	**Field Name**	**Description**	
31:24		0x72	Character32	Vendor Text - transmitted in ISDU 0x0011	
23:16		0x65	Character31		
15:8		0x6D	Character30		
7:0		0x6F	Character29		

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13.23.9 0xBE – VendorText[8]

Address : 0xBE		Register Name : VendorText[8]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character36	Vendor Text - transmitted in ISDU 0x0011
23:16		0x0	Character35	
15:8		0x0	Character34	
7:0		0x0	Character33	

13.23.10 0xBF – VendorText[9]

Address : 0xBF		Register Name : VendorText[9]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character40	Vendor Text - transmitted in ISDU 0x0011
23:16		0x0	Character39	
15:8		0x0	Character38	
7:0		0x0	Character37	

13.23.11 0xC0 – VendorText[10]

Address : 0xC0		Register Name : VendorText[10]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character44	Vendor Text - transmitted in ISDU 0x0011
23:16		0x0	Character43	
15:8		0x0	Character42	
7:0		0x0	Character41	

13.23.12 0xC1 – VendorText[11]

Address : 0xC1		Register Name : VendorText[11]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character48	Vendor Text - transmitted in ISDU 0x0011
23:16		0x0	Character47	
15:8		0x0	Character46	
7:0		0x0	Character45	

13.24 IO-Link – Product Text

13.24.1 0xC2 – ProductText[0]

Address : 0xC2		Register Name : ProductText[0]		Default: 0x62206F54
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x62	Character4	Product Text - transmitted in ISDU 0x0014
23:16		0x20	Character3	
15:8		0x6F	Character2	
7:0		0x54	Character1	

13.24.2 0xC3 – ProductText[1]

Address : 0xC3		Register Name : ProductText[1]		Default: 0x69662065
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x69	Character8	Product Text - transmitted in ISDU 0x0014
23:16		0x66	Character7	
15:8		0x20	Character6	
7:0		0x65	Character5	

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13.24.3 0xC4 – ProductText[2]

Address : 0xC4		Register Name : ProductText[2]		Default: 0x64656C6C
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x64	Character12	Product Text - transmitted in ISDU 0x0014
23:16		0x65	Character11	
15:8		0x6C	Character10	
7:0		0x6C	Character9	

13.24.4 0xC5 – ProductText[3]

Address : 0xC5		Register Name : ProductText[3]		Default: 0x20796220
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x20	Character16	Product Text - transmitted in ISDU 0x0014
23:16		0x79	Character15	
15:8		0x62	Character14	
7:0		0x20	Character13	

13.24.5 0xC6 – ProductText[4]

Address : 0xC6		Register Name : ProductText[4]		Default: 0x656E6552
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x65	Character20	Product Text - transmitted in ISDU 0x0014
23:16		0x6E	Character19	
15:8		0x65	Character18	
7:0		0x52	Character17	

13.24.6 0xC7 – ProductText[5]

Address : 0xC7		Register Name : ProductText[5]		Default: 0x20736173
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x20	Character24	Product Text - transmitted in ISDU 0x0014
23:16		0x73	Character23	
15:8		0x61	Character22	
7:0		0x73	Character21	

13.24.7 0xC8 – ProductText[6]

Address : 0xC8		Register Name : ProductText[6]		Default: 0x74737563
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x74	Character28	Product Text - transmitted in ISDU 0x0014
23:16		0x73	Character27	
15:8		0x75	Character26	
7:0		0x63	Character25	

13.24.8 0xC9 – ProductText[7]

Address : 0xC9		Register Name : ProductText[7]		Default: 0x72656D6F
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x72	Character32	Product Text - transmitted in ISDU 0x0014
23:16		0x65	Character31	
15:8		0x6D	Character30	
7:0		0x6F	Character29	

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13.24.9 0xCA – ProductText[8]

Address : 0xCA		Register Name : ProductText[8]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character36	Product Text - transmitted in ISDU 0x0014
23:16		0x0	Character35	
15:8		0x0	Character34	
7:0		0x0	Character33	

13.24.10 0xCB – ProductText[9]

Address : 0xCB		Register Name : ProductText[9]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character40	Product Text - transmitted in ISDU 0x0014
23:16		0x0	Character39	
15:8		0x0	Character38	
7:0		0x0	Character37	

13.24.11 0xCC – ProductText[10]

Address : 0xCC		Register Name : ProductText[10]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character44	Product Text - transmitted in ISDU 0x0014
23:16		0x0	Character43	
15:8		0x0	Character42	
7:0		0x0	Character41	

13.24.12 0xCD – ProductText[11]

Address : 0xCD		Register Name : ProductText[11]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character48	Product Text - transmitted in ISDU 0x0014
23:16		0x0	Character47	
15:8		0x0	Character46	
7:0		0x0	Character45	

13.25 IO-Link – Serial Number

13.25.1 0xCE – SerialNumber[0]

Address : 0xCE		Register Name : SerialNumber[0]		Default: 0x62206F54
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x62	Character4	Serial Number - transmitted in ISDU 0x0015
23:16		0x20	Character3	
15:8		0x6F	Character2	
7:0		0x54	Character1	

13.25.2 0xCF – SerialNumber[1]

Address : 0xCF		Register Name : SerialNumber[1]		Default: 0x69662065
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x69	Character8	Serial Number - transmitted in ISDU 0x0015
23:16		0x66	Character7	
15:8		0x20	Character6	
7:0		0x65	Character5	

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13.25.3 0xD0 – SerialNumber[2]

Address : 0xD0		Register Name : SerialNumber[2]		Default: 0x64656C6C
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x64	Character12	Serial Number - transmitted in ISDU 0x0015
23:16		0x65	Character11	
15:8		0x6C	Character10	
7:0		0x6C	Character9	

13.25.4 0xD1 – SerialNumber[3]

Address : 0xD1		Register Name : SerialNumber[3]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character16	Serial Number - transmitted in ISDU 0x0015
23:16		0x0	Character15	
15:8		0x0	Character14	
7:0		0x0	Character13	

13.26 IO-Link – Firmware Password

13.26.1 0xD2 – FwPassword[0]

Address : 0xD2		Register Name : FwPassword[0]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character4	Firmware Password - transmitted in ISDU 0x43BD
23:16		0x0	Character3	
15:8		0x0	Character2	
7:0		0x0	Character1	

13.26.2 0xD3 – FwPassword[1]

Address : 0xD3		Register Name : FwPassword[1]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character8	Firmware Password - transmitted in ISDU 0x43BD
23:16		0x0	Character7	
15:8		0x0	Character6	
7:0		0x0	Character5	

13.26.3 0xD4 – FwPassword[2]

Address : 0xD4		Register Name : FwPassword[2]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character12	Firmware Password - transmitted in ISDU 0x43BD
23:16		0x0	Character11	
15:8		0x0	Character10	
7:0		0x0	Character9	

13.26.4 0xD5 – FwPassword[3]

Address : 0xD5		Register Name : FwPassword[3]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character16	Firmware Password - transmitted in ISDU 0x43BD
23:16		0x0	Character15	
15:8		0x0	Character14	
7:0		0x0	Character13	

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13.27 IO-Link – Device IDs

13.27.1 0xD6 – DeviceId

Value 0x0 not allowed.

Address : 0xD6		Register Name : DeviceId		Default: 0x00000001
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x1	DeviceId	Device ID in active Firmware - transmitted in ISDU 0x000A, 0x000B, 0x000C - LSB aligned

13.27.2 0xD7 – BootloaderDeviceId

Value 0x0 not allowed.

Address : 0xD7		Register Name : BootloaderDeviceId		Default: 0x00000002
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x2	BootloaderDeviceId	Device ID in bootloader mode - transmitted in ISDU 0x000A, 0x000B, 0x000C - LSB aligned

13.28 IO-Link – Vendor ID

13.28.1 0xD8 – VendorId

Address : 0xD8		Register Name : VendorId		Default: 0x0000018C
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0x18C	VendorId	Vendor ID - transmitted in ISDU 0x0008 and 0x0009 - LSB aligned

13.29 IO-Link – Vendor Name

13.29.1 0xD9 – VendorName[0]

Address : 0xD9		Register Name : VendorName[0]		Default: 0x62206F54
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x62	Character4	Vendor Name - transmitted in ISDU 0x0010
23:16		0x20	Character3	
15:8		0x6F	Character2	
7:0		0x54	Character1	

13.29.2 0xDA – VendorName[1]

Address : 0xDA		Register Name : VendorName[1]		Default: 0x69662065
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x69	Character8	Vendor Name - transmitted in ISDU 0x0010
23:16		0x66	Character7	
15:8		0x20	Character6	
7:0		0x65	Character5	

13.29.3 0xDB – VendorName[2]

Address : 0xDB		Register Name : VendorName[2]		Default: 0x64656C6C
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x64	Character12	Vendor Name - transmitted in ISDU 0x0010
23:16		0x65	Character11	
15:8		0x6C	Character10	
7:0		0x6C	Character9	

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13.29.4 0xDC – VendorName[3]

Address : 0xDC		Register Name : VendorName[3]		Default: 0x20796220
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x20	Character16	Vendor Name - transmitted in ISDU 0x0010
23:16		0x79	Character15	
15:8		0x62	Character14	
7:0		0x20	Character13	

13.29.5 0xDD – VendorName[4]

Address : 0xDD		Register Name : VendorName[4]		Default: 0x656E6552
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x65	Character20	Vendor Name - transmitted in ISDU 0x0010
23:16		0x6E	Character19	
15:8		0x65	Character18	
7:0		0x52	Character17	

13.29.6 0xDE – VendorName[5]

Address : 0xDE		Register Name : VendorName[5]		Default: 0x20736173
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x20	Character24	Vendor Name - transmitted in ISDU 0x0010
23:16		0x73	Character23	
15:8		0x61	Character22	
7:0		0x73	Character21	

13.29.7 0xDF – VendorName[6]

Address : 0xDF		Register Name : VendorName[6]		Default: 0x74737563
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x74	Character28	Vendor Name - transmitted in ISDU 0x0010
23:16		0x73	Character27	
15:8		0x75	Character26	
7:0		0x63	Character25	

13.29.8 0xE0 – VendorName[7]

Address : 0xE0		Register Name : VendorName[7]		Default: 0x72656D6F
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x72	Character32	Vendor Name - transmitted in ISDU 0x0010
23:16		0x65	Character31	
15:8		0x6D	Character30	
7:0		0x6F	Character29	

13.29.9 0xE1 – VendorName[8]

Address : 0xE1		Register Name : VendorName[8]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character36	Vendor Name - transmitted in ISDU 0x0010
23:16		0x0	Character35	
15:8		0x0	Character34	
7:0		0x0	Character33	

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13.29.10 0xE2 – VendorName[9]

Address : 0xE2		Register Name : VendorName[9]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character40	Vendor Name - transmitted in ISDU 0x0010
23:16		0x0	Character39	
15:8		0x0	Character38	
7:0		0x0	Character37	

13.29.11 0xE3 – VendorName[10]

Address : 0xE3		Register Name : VendorName[10]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character44	Vendor Name - transmitted in ISDU 0x0010
23:16		0x0	Character43	
15:8		0x0	Character42	
7:0		0x0	Character41	

13.29.12 0xE4 – VendorName[11]

Address : 0xE4		Register Name : VendorName[11]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character48	Vendor Name - transmitted in ISDU 0x0010
23:16		0x0	Character47	
15:8		0x0	Character46	
7:0		0x0	Character45	

13.30 IO-Link – Hardware ID Key

13.30.1 0xE5 – HwIdKey[0]

Address : 0xE5		Register Name : HwIdKey[0]		Default: 0x425F4F54
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x42	Character4	Hardware ID Key - transmitted in ISDU 0x43BE
23:16		0x5F	Character3	
15:8		0x4F	Character2	
7:0		0x54	Character1	

13.30.2 0xE6 – HwIdKey[1]

Address : 0xE6		Register Name : HwIdKey[1]		Default: 0x49465F45
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x49	Character8	Hardware ID Key - transmitted in ISDU 0x43BE
23:16		0x46	Character7	
15:8		0x5F	Character6	
7:0		0x45	Character5	

13.30.3 0xE7 – HwIdKey[2]

Address : 0xE7		Register Name : HwIdKey[2]		Default: 0x44454C4C
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x44	Character12	Hardware ID Key - transmitted in ISDU 0x43BE
23:16		0x45	Character11	
15:8		0x4C	Character10	
7:0		0x4C	Character9	

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13.30.4 0xE8 – HwIdKey[3]

Address : 0xE8		Register Name : HwIdKey[3]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character16	Hardware ID Key - transmitted in ISDU 0x43BE
23:16		0x0	Character15	
15:8		0x0	Character14	
7:0		0x0	Character13	

13.31 IO-Link – Hardware Revision

13.31.1 0xE9 – HardwareRevision[0]

Address : 0xE9		Register Name : HardwareRevision[0]		Default: 0x62206F54
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x62	Character4	Hardware Revision - transmitted in ISDU 0x0016
23:16		0x20	Character3	
15:8		0x6F	Character2	
7:0		0x54	Character1	

13.31.2 0xEA – HardwareRevision[1]

Address : 0xEA		Register Name : HardwareRevision[1]		Default: 0x69662065
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x69	Character8	Hardware Revision - transmitted in ISDU 0x0016
23:16		0x66	Character7	
15:8		0x20	Character6	
7:0		0x65	Character5	

13.31.3 0xEB – HardwareRevision[2]

Address : 0xEB		Register Name : HardwareRevision[2]		Default: 0x64656C6C
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x64	Character12	Hardware Revision - transmitted in ISDU 0x0016
23:16		0x65	Character11	
15:8		0x6C	Character10	
7:0		0x6C	Character9	

13.31.4 0xEC – HardwareRevision[3]

Address : 0xEC		Register Name : HardwareRevision[3]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character16	Hardware Revision - transmitted in ISDU 0x0016
23:16		0x0	Character15	
15:8		0x0	Character14	
7:0		0x0	Character13	

13.32 IO-Link – Product Name

13.32.1 0xED – ProductName

Address : 0xED		Register Name : ProductName[0]		Default: 0x62206F54
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x62	Character4	Product Name - transmitted in ISDU 0x0012
23:16		0x20	Character3	
15:8		0x6F	Character2	
7:0		0x54	Character1	

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Address : 0xEE	Register Name : ProductName[1]			Default: 0x69662065
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x69	Character8	Product Name - transmitted in ISDU 0x0012
23:16		0x66	Character7	
15:8		0x20	Character6	
7:0		0x65	Character5	

Address : 0xEF	Register Name : ProductName[2]			Default: 0x64656C6C
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x64	Character12	Product Name - transmitted in ISDU 0x0012
23:16		0x65	Character11	
15:8		0x6C	Character10	
7:0		0x6C	Character9	

Address : 0xF0	Register Name : ProductName[3]			Default: 0x20796220
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x20	Character16	Product Name - transmitted in ISDU 0x0012
23:16		0x79	Character15	
15:8		0x62	Character14	
7:0		0x20	Character13	

Address : 0xF1	Register Name : ProductName[4]			Default: 0x656E6552
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x65	Character20	Product Name - transmitted in ISDU 0x0012
23:16		0x6E	Character19	
15:8		0x65	Character18	
7:0		0x52	Character17	

Address : 0xF2	Register Name : ProductName[5]			Default: 0x20736173
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x20	Character24	Product Name - transmitted in ISDU 0x0012
23:16		0x73	Character23	
15:8		0x61	Character22	
7:0		0x73	Character21	

Address : 0xF3	Register Name : ProductName[6]			Default: 0x74737563
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x74	Character28	Product Name - transmitted in ISDU 0x0012
23:16		0x73	Character27	
15:8		0x75	Character26	
7:0		0x63	Character25	

Address : 0xF4	Register Name : ProductName[7]			Default: 0x72656D6F
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x72	Character32	Product Name - transmitted in ISDU 0x0012
23:16		0x65	Character31	
15:8		0x6D	Character30	
7:0		0x6F	Character29	

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13.33 IO-Link – Product ID

13.33.1 0xF5 – ProductId

Address : 0xF5		Register Name : ProductId[0]		Default: 0x62206F54
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x62	Character4	Product ID - transmitted in ISDU 0x0013
23:16		0x20	Character3	
15:8		0x6F	Character2	
7:0		0x54	Character1	

Address : 0xF6		Register Name : ProductId[1]		Default: 0x69662065
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x69	Character8	Product ID - transmitted in ISDU 0x0013
23:16		0x66	Character7	
15:8		0x20	Character6	
7:0		0x65	Character5	

Address : 0xF7		Register Name : ProductId[2]		Default: 0x64656C6C
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x64	Character12	Product ID - transmitted in ISDU 0x0013
23:16		0x65	Character11	
15:8		0x6C	Character10	
7:0		0x6C	Character9	

Address : 0xF8		Register Name : ProductId[3]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character16	Product ID - transmitted in ISDU 0x0013
23:16		0x0	Character15	
15:8		0x0	Character14	
7:0		0x0	Character13	

Address : 0xF9		Register Name : ProductId[4]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character20	Product ID - transmitted in ISDU 0x0013
23:16		0x0	Character19	
15:8		0x0	Character18	
7:0		0x0	Character17	

Address : 0xFA		Register Name : ProductId[5]		Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character24	Product ID - transmitted in ISDU 0x0013
23:16		0x0	Character23	
15:8		0x0	Character22	
7:0		0x0	Character21	

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Address : 0xFB	Register Name : ProductId[6]			Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character28	Product ID - transmitted in ISDU 0x0013
23:16		0x0	Character27	
15:8		0x0	Character26	
7:0		0x0	Character25	

Address : 0xFC	Register Name : ProductId[7]			Default: 0x00000000
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x0	Character32	Product ID - transmitted in ISDU 0x0013
23:16		0x0	Character31	
15:8		0x0	Character30	
7:0		0x0	Character29	

13.34 CCP Password, Version and CRC

13.34.1 0xFD – CcpPassword

If CCP Password is different from 0xFFFFFFFF, CCP Password protection becomes effective.

Address : 0xFD	Register Name : CcpPassword			Default: 0xFFFFFFFF
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0xFFFFFFFF	CcpPassword	CCP Password to protect CCP read/write actions via IO-Link - transmitted in ISDU 0x0201

13.34.2 0xFE – CcpVersion

Address : 0xFE	Register Name : CcpVersion			Default: 0x86040001
Bits	**Access**	**Default**	**Field Name**	**Description**
31:24		0x86	Pid	Product specific CCP ID
23:16		0x4	PatchVer	Patch Version of CCP
15:8		0x0	MinorVer	Minor Version of CCP
7:0		0x1	MajorVer	Major Version of CCP

13.34.3 0xFF – CrcCcp1

Wrong setting of this parameter hinders firmware execution. Leave the computation of necessary setup for this register to the GUI.

Address : 0xFF	Register Name : CrcCcp1			Default: 0xD3926079
Bits	**Access**	**Default**	**Field Name**	**Description**
31:0		0xD3926079	CrcCcp1	CRC of CCP Page 1

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14 Application Information

14.1 2-Bridge Application 1.8V to 5.5V Supply

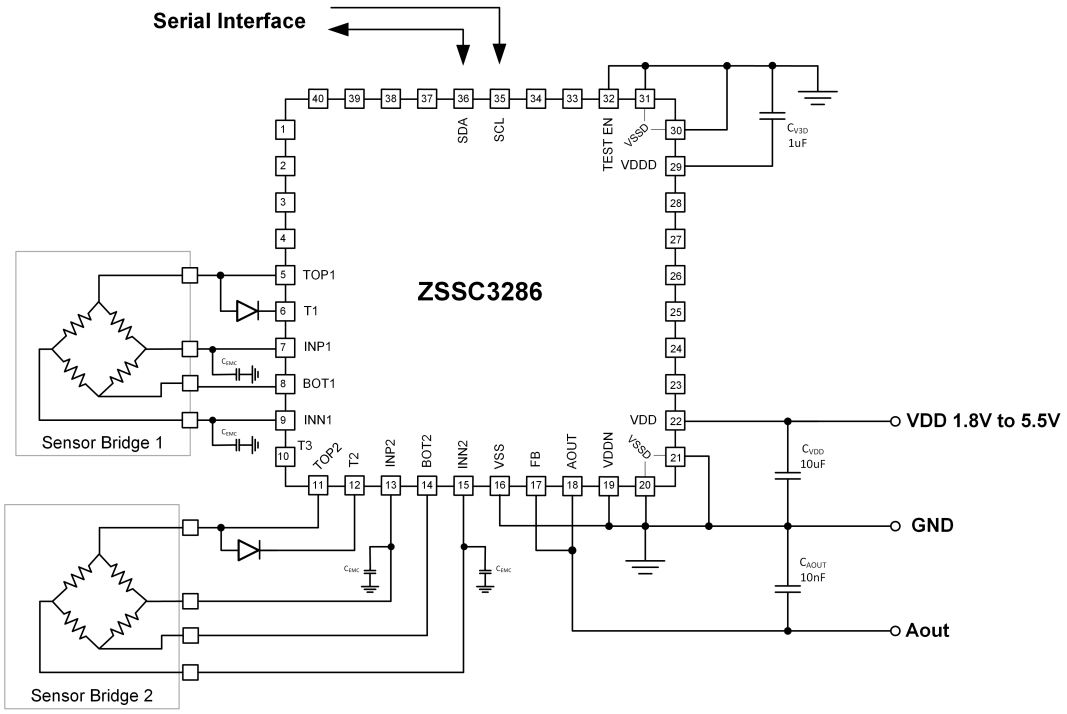

Figure 57. 2-Bridge Application 1.8V to 5.5V Supply

14.2 Single Bridge Application with IO-Link

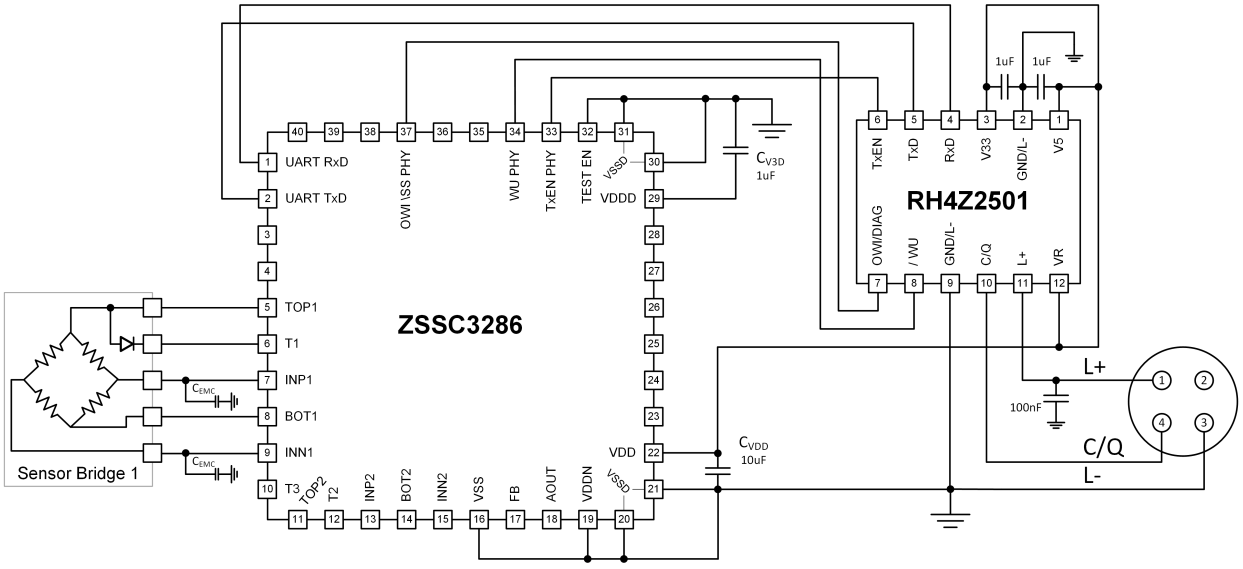

Figure 58. Single Bridge Application with IO-Link

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14.3 Single Bridge Application with IO-Link and Current Loop Output

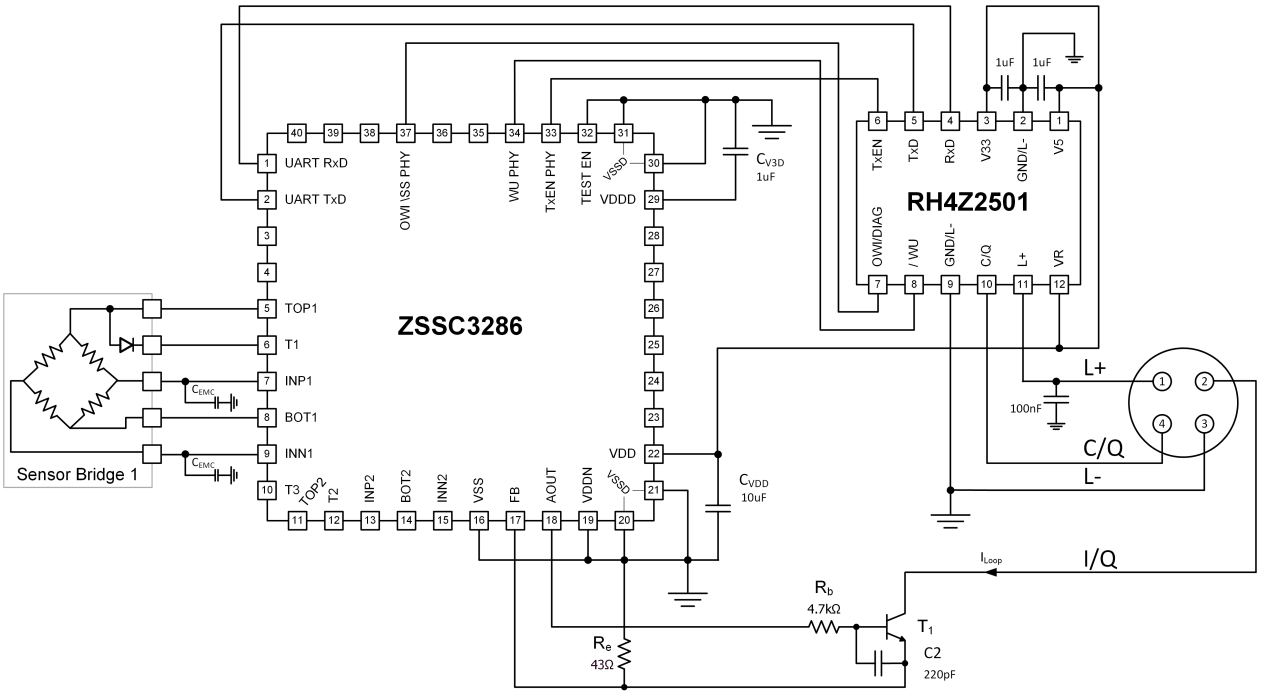

Figure 59. Single Bridge Application with IO-Link and Current Loop Output

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15 Package Information

15.1 Package Outline Drawings

The package outline drawings are accessible from the link below. The package information is the most current data available.

QFN40: Package Outline Drawing Code: NDG40S1 40-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.4 mm Pitch (renesas.com)

WLCSP: Package Outline Drawing Code: AWG48D1 48-DSBGA 3.61 x 3.24 x 0.6 mm Body, 0.4 mm Pitch (renesas.com)

Bare Die: on request

15.2 QFN40 Marking Diagram

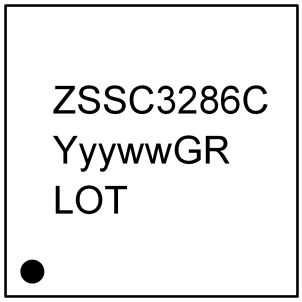

Figure 60. QFN40 Marking Diagram

1. ”ZSSC3286” C is the truncated part number.
2. ”YyywwGR” where ”Y” and ”GR” are fixed and ”yyww” represents the last digits of the year and week that the part was assembled.
3. ”LOT” is the complete lot number of the part.

15.3 WLCSP Marking Diagram

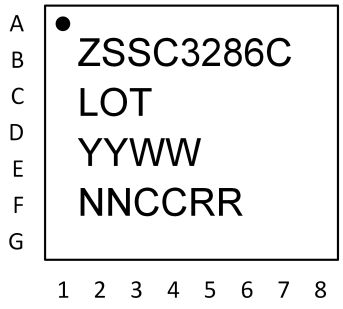

Figure 61. WLCSP Marking Diagram

1. ”ZSSC3286C” is the truncated part number.
2. ”LOT” is the complete lot number of the part.
3. ”YYWW” represents the last digits of the year and week that the part was assembled.
4. ”NNCCRR” contains the wafer position information:
   - ”NN”: Scribe Number
   - ”CC”: Column of die location
   - ”RR”: Row of die location

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16 Glossary

Term	Description
ADC	Analog to Digital Converter
AFE	Analog Front End
ARM	Provider of microcontroller core
AUX	Auxiliary measurement, in addition to main sensor bridge measurement
AZ	Auto-zero
BINO	Binary Output Signal
BLOB	Binary Large Object
BOT	Bottom
CCP	Configuration and Calibration Page
C/Q	C/Q line of IO-Link interface. Connection for communication (C) or switching (Q) signal
DAC	Digital to Analog Converter
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FB	Feedback input for analog output buffer
FS	Full Scale
FW	Firmware
GPIO	General Purpose Input Output
GUI	Graphical User Interface
HF	High Frequency
HW	Hardware
I2C	Inter Integrated Circuit communication protocol
ID	Identification
IIR	Infinite Impulse Response
IODD	IO-Link Device Description
IO-Link	Industrial Communication Standard (IEC 61131-9 Single-drop digital communication interface for small sensors and actuators (SDCI))
ISDU	Indexed Service Data Unit
LDR	Lower Diagnostic Range
LF	Low Frequency
LSB	Least Significant Bit
MDC	Measurement Data Channel
MISO	Master-In Slave-Out
MOSI	Master-Out Slave-In
MSB	Most Significant Bit
NC	Not Connected
OWI	One Wire Interface
PGA	Programmable Gain Amplifier
PHY	Physical Layer
POR	Power-On-Reset
PTAT	Proportional to absolute temperature current source
R	Read
RAM	Random Access Memory
RDAC	Resistive Digital to Analog Converter
RTD	Temperature dependent resistor
RW	Read/Write
SM-	Main Sensor Measurement, inverted signal polarity
SM+	Main Sensor Measurement, standard (non-inverted) signal polarity
SOT	Second Order Term

Continued on next page

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Term	Description
SPI	Serial Peripheral Interface
SS	Slave Select
SSC	Sensor Signal Conditioner
SSP	Smart Sensor Profile
TFW	Technology Firmware
TLC	Third Logic Channel
UART	Universal Asynchronous Receiver / Transmitter
UDR	Upper Diagnostic Range
W	Write
WURQ	Wake-Up Request

17 References

Reference Number	Title
1	IO-Link Interface and System. Specification. Version 1.1.4. June 2024
2	IO-Link Common Profile. Specification. Version 1.2. January 2024
3	RH4Z2501 https://www.renesas.com/RH4Z2501

18 Revision History

18.1 Firmware Revision History

Revision	Date	Description
1.2.0	April 24, 2025	Initial release for revision C
1.3.0	February 28, 2026	Adding Zero Adjustment feature

18.2 Document Revision History

Revision	Date	Description
1.00	July 15, 2026	Initial release for FW V1.3.0

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