ZSSC4165D-01

Automotive Resistive Sensor Signal Conditioner with SENT Output

Description

The ZSSC4165D-01 is a member of Renesas's family of CMOS integrated circuits for highly accurate amplification and sensor-specific correction of differential bridge sensor element signals. Featuring a maximum analog pre-amplification of up to 200, the ZSSC4165D-01 is configurable to nearly all resistive bridges.

Digital compensation of offset, sensitivity, temperature drift, and nonlinearity are accomplished via a 16-bit RISC microcontroller. Calibration coefficients and configuration data are stored in the ZSSC4165D-01 nonvolatile memory (NVM), which is reliable in automotive applications.

The ZSSC4165D-01 supports use of two external Diodes and the internal PTAT as a temperature reference.

Measured values are provided via a digital SENT interface. The SENT interface enables transmission of sensor data via its Fast Channel as well as transmission of supplementary data via its Serial Data Message (SDM) Channel (also referred to as the "slow" channel) using only one output pin. End-of-line calibration is also supported through this output pin via Renesas's ZACwire™ one-wire interface (OWI). The ZSSC4165D-01 and the calibration equipment communicate digitally, so the noise sensitivity is greatly reduced. Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The ZSSC4165D-01 is optimized for automotive environments by over-voltage and reverse polarity protection circuitry, excellent electromagnetic compatibility, and multiple diagnostic features.

Typical Applications

- Dual pressure measurement with optional precise sensing element temperature compensation
- Differential pressure measurement with two single-ended sensing elements
- Flow measurement for gas or fluids with the differential pressure method

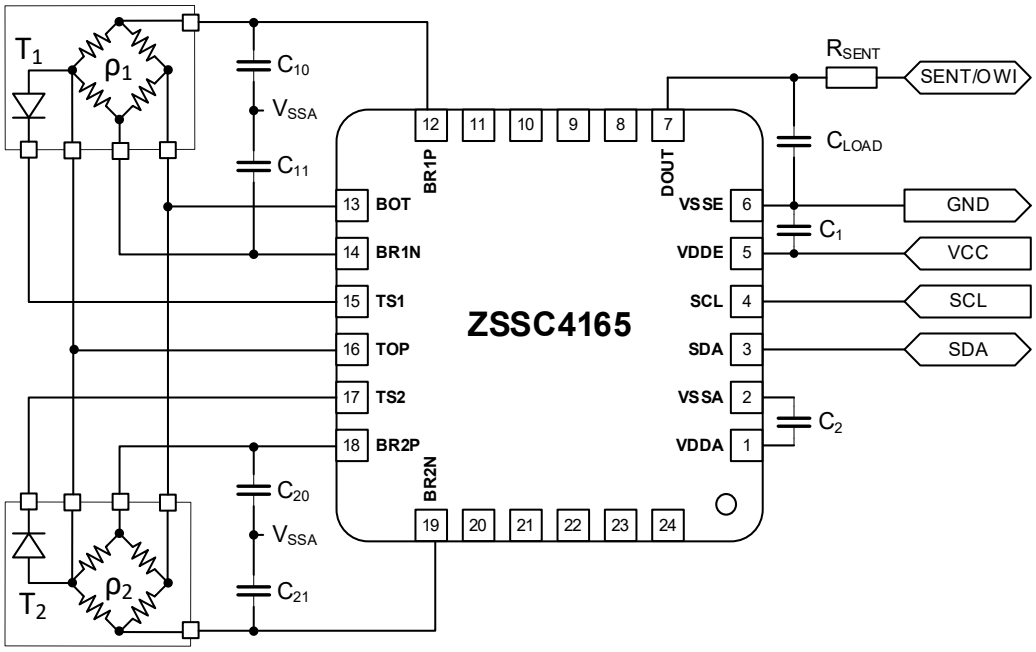
Features

- Two differential full-bridge sensor element measurements
- One internal chip temperature measurement
- Two external Diode temperature measurements
- Digital compensation for offset, gain, and higher order nonlinearity as well as temperature coefficients of the differential sensor element input signals
- Optional channel 1 – channel 2 difference output
- Operating temperature range: -40°C to 150°C
- Accuracy as high as ±0.50% full scale at -40°C to 150°C (see the electrical characteristics table for conditions)
- NVM memory for configuration, calibration data, and configurable measurement and conditioning functionality
- SENT output compliant to SAE J2716 JAN2010 (SENT Rev. 3) and APR2016 (SENT Rev. 4) standards
- Supports output of one or more sensor signals and product identification via a single SENT interface connection
- Configurable for nearly all resistive bridge sensors
- One-pass, end-of-line calibration algorithm minimizes production costs
- No external trimming or components required
- Qualified according to AEC-Q100 Grade 0
- Supply voltage: 4.75V to 5.25V
- Over-voltage and reverse polarity protection up to ±18V
- Bridge sensor input span: 1mV/V to 800mV/V
- Bridge sensor signal ADC resolution: 14 to 18 bit
- Output resolution: 12-bit via SENT interface
- Enhanced diagnostic features for sensor module
- Package: 24-QFN (4 × 4 mm; wettable flanks), 16-TSSOP (4.4 × 5 mm, exposed pad)

Available Support

- Evaluation kit
- Application notes
- Calculation tools

ZSSC4165D-01 Basic Circuit



Contents

Figures

Tables

1. Pin Assignments

The ZSSC4165D-01 is available in a 24-QFN (4 × 4 mm; wettable flanks) RoHS-conformant package.

Note: The backside of the 24-QFN package (exposed pad; see section 13) is electrically connected to VSSA.

Recommendation: Solder the QFN exposed pad to the PCB, even if electrically redundant, to ensure adequate thermal performance and to reduce mechanical stress and solder joint failure risk.

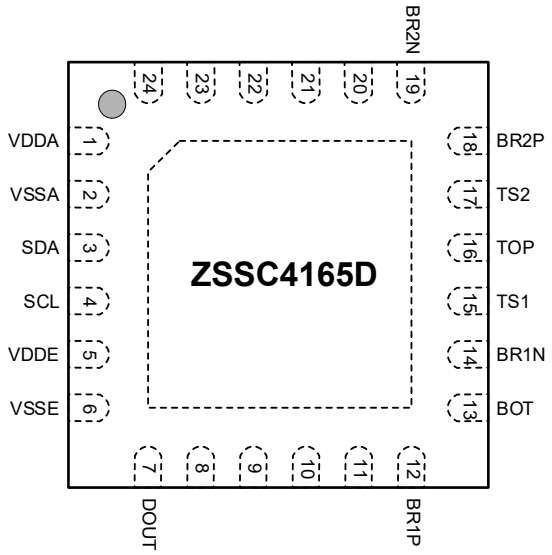


Figure 1. 24-QFN Pin Assignments – Top View

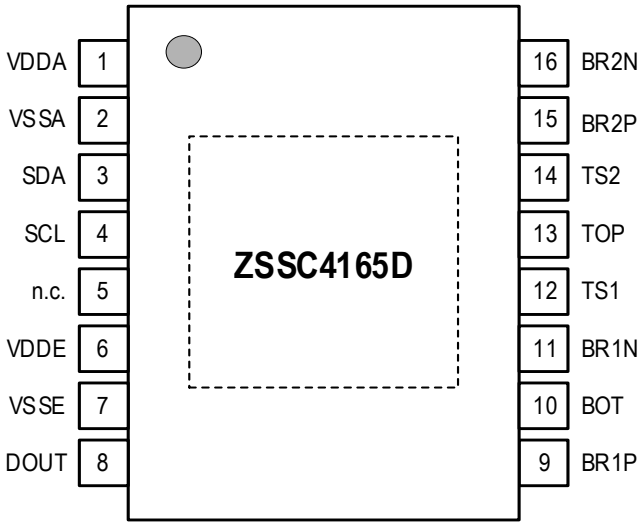


Figure 2. 16-TSSOP Pin Assignments – Top View

2. Pin Descriptions

Table 1. Pin Descriptions

24-QFN Pin #	16-TSSOP Pin#	Pin Name	Type	Description
1	1	VDDA	Supply	Internal supply [a]
2	2	VSSA	Supply	Internal ground
3	3	SDA	Input/Output	I2C data input/output with internal pull-up (optional production communication interface) [b], [c]
4	4	SCL	Input	I2C clock, with internal pull-up (*optional production communication interface*) [b], [c]
–	5	–	–	n.c.
5	6	VDDE	Supply	External supply
6	7	VSSE	Supply	External ground
7	8	DOUT	Input/Output	SENT output and One-Wire Interface (OWI) input/output
8 to 11	–	–	–	n.c.
12	9	BR1P	Input	Positive bridge sensor input
13	10	BOT	Supply	Negative bridge supply voltage
14	11	BR1N	Input	Negative bridge sensor input
15	12	TS1	Input	External temperature sensor input 1
16	13	TOP	Input	Positive bridge supply voltage
17	14	TS2	Input	External temperature sensor input 2 (*optional alternative to TS1*)
18	15	BR2P	Input	Positive bridge sensor input 2
19	16	BR2N	Input	Negative bridge sensor input 2
20 to 24	–	–	–	n.c.
–	–	EPAD	Supply	Internal ground; connected to VSSA [c]

[a] Do not supply VDDA externally.

[b] Internal pull-up.

[c] No connection required.

[d] Ground; can be shorted externally to VSSA (pin 2).

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed in Table 2 can cause permanent damage to the device. Functional operation of the ZSSC4165D-01 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability. In addition, extended exposure to stresses above the operating conditions given in section 4 might affect device reliability.

See section 7.7 for information about over-voltage protection, reverse polarity, and short-circuit protection.

Table 2. Absolute Maximum Ratings

Specification	Symbol	Parameter	Conditions	Min	Typ	Max
DS_001	V_{VDDE_ABS}	Supply voltage		-18	18	V
DS_002	V_{DOUT_ABS}	Voltage at the DOUT pin		-18	18	V
DS_003	V_{DIFF_ABS}	Pin voltage difference	Voltage between any two of these pins: VDDE, DOUT, and VSSE	-18	18	V
DS_004	V_{VDDA_ABS}	Analog supply voltage	On-chip controlled voltage; do not supply VDDA externally	-0.3	6.2	V
DS_005	V_{PIN_ABS}	Voltage at all other pins	Must not exceed VVDDA + 0.3V	-0.3	6.2	V
DS_006	T_{J_ABS}	Junction temperature	Note: See section 7.7 regarding over-voltage protection	-40	160	°C
DS_007	T_{STOR_ABS}	Storage temperature		-55	155	°C

4. Operating Conditions

The operating conditions in Table 3 specify the conditions that the application circuit must provide to the device during operation for proper function. Unless otherwise stated, the parameter limits in this section are applied as test conditions for the electrical parameters specified in section 5.

Table 3. Operating Conditions

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_009	V_{DDE}	Supply voltage	VDDE to VSSE	4.75	5	5.25	V
DS_010	V_{DDE_EXTD}	Extended supply voltage[a]	VDDE to VSSE; de-rated accuracy as specified with specification DS_059	4.5	5	5.5	V
DS_011	V_{DDE_OP}	Operating supply voltage[a]	VDDE to VSSE; de-rated accuracy [f]	4		6	V
DS_012	T_{AMB}	Ambient temperature [b], [c]	Temperature range	-40		150	°C
Informational [d]	$R_{th\_JA\_QFN24}$	Thermal resistance 24-QFN[a]	According to JESD 51		32		K/W
DS_185	R_{BR}	Bridge sensor resistance[a][e]	For each sensor bridge at pins BR1P/BR1N and BR2P/BR2N	1		15	kΩ

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] Temperature stress over lifetime is restricted to the Temperature Profile described in section 12.1 or to similar stress caused by equivalent temperature profiles. Contact Renesas for temperature stress calculation support.

[c] Assuming application conditions according to test board design as per JESD51-7 and natural convection test conditions as per JESD51-2.

[d] Package-related parameter.

[e] Symmetric behavior and identical electrical properties (especially the low-pass characteristic) of the differential bridge sensor inputs are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins can generate a failure in signal operation.

[f] For a supply greater than 5.5V: Above the ZSSC4165D-01 over-voltage limitation threshold, the output potential is clipped at this threshold.

5. Electrical Characteristics

All parameter values are valid under the operating conditions specified in section 4 (unless otherwise stated). All parameters are valid for the ambient temperature range T_{AMB} and for the supply voltage range VVDDE = 4.75V to 5.25V. Unless otherwise defined, the parameters are related to the ZSSC4165D-01 itself. All voltages are referenced to the VSSA pin.

The following parameters are specified based on a ZSSC4165D-01 main channel configuration setup using a PGA gain of 100, and assuming a resulting ADC input range usage of ≥ 50%FS. Further preconditions are an ADC resolution of 14 bits, no additional settle time, and an oscillator frequency of 8MHz.

Table 4. Electrical Parameters

Note: See important table notes at the end of this table.

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Current and System Operating Conditions							
DS_015	I_S	Supply current	Excluding bridge sensors; excluding output current at D_{OUT} pin.	–	8	10	mA
DS_016	P_{OV}	Over-voltage power consumption[a]	5.5V < V_{VDDE} < 18V; excluding sensor and output load.	–	–	300	mW
DS_017	$V_{OV\_LIM\_TH}$	Over-voltage limitation threshold[a]	V_{VDDA} is limited if V_{VDDE} exceeds the threshold $V_{OV\_LIM\_TH}$.	5.55	–	18	V
DS_018	$V_{OV\_OFF\_TH}$	Over-voltage switch-off threshold[a]	The ZSSC4165D-01 is set to the reset state with limited current consumption if V_{VDDE} exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.	7	–	12	V
DS_019	$t_{OV\_OFF\_DLY}$	Over-voltage switch-off delay[a]	The ZSSC4165D-01 is set to the reset state with limited current consumption if V_{VDDE} exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.	–	10	25	ms

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_020	$I_{S\_OV\_OFF}$	Supply current limitation in the event of over-voltage switch-off[a]	Over-voltage switch-off is activated if the supply voltage exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$. V_{VDDE} < 18V; excluding sensor and output load.	–	–	10	mA
DS_171	V_{DDA}	Analog supply voltage	V_{DDA} to V_{SSA}; V_{DDA} is limited to V_{VDDA_ABS} if V_{DDE} exceeds the threshold $V_{OV\_LIM\_TH}$.	0.9	–	1.0	V_{DDE}
DS_021	V_{SENS}	Bridge sensor supply voltage	$V_{SENS} = V_{TOP} – V_{BOT}$ where V_{TOP} is the voltage at the TOP pin and V_{BOT} is the voltage at BOT pin.	0.9	–	1.0	V_{DDA}
DS_022	V_{POR_OFF}	Power-on reset off-threshold	V_{VDDA} measured referenced to V_{SSA}; POR is active until V_{VDDA} exceeds this threshold.	3.3	–	3.8	V
DS_023	V_{POR_ON}	Power-on reset on-threshold	POR is activated if V_{DDA} falls below this threshold.	3.0	–	3.6	V
DS_024	V_{POR_HYST}	Power-on reset hysteresis[a]	$V_{POR\_ON} – VPOR\_OFF$	–	0.4	–	V
DS_025	f_{OSC}	Oscillator frequency	Calibrated oscillator frequency.	7.4	8	8.6	MHz
DS_026	TCOSC	Oscillator frequency temperature coefficient [a]		-200		200	ppm/K
A/D Conversion Refer to section 7.2.4.							
DS_034	DNL_{ADC}	DNL[a]		–	–	0.95	LSB
DS_035	INL_{ADC}	INL	Best fit.	–	3	8	LSB14
DS_030	C_{IN}	Capacitance at input [a]	Capacitance at pins BR1P and BR1N or BR2P and BR2N to VSSA; requirement for timing parameters.	0	–	12	nF
Differential Bridge Sensor Measurement Refer to section 7.3.1							
Informational	–	ADC resolution[a]	Custom adjustable	14	–	18	Bit
DS_027	V_{IN_SPAN}	Differential input span	Analog gain: 1 to 200.	1	–	800	mV/V
	V_{IN_RNG}	Input voltage range (Absolute voltage at bridge input pins)		0.3	–	0.65	VSENS
DS_033	V_{ADC_IN}	ADC input range[a]	Differential input signal range depending on analog gain a_{PGA} and ADC range shift rs_{ADC}: $V_{ADC\_IN} = V_{IN} \times a_{PGA} + rs_{ADC} \times V_{SENS}$	0.05	–	0.95	V_{SENS}
			Restriction for analog gain > 100.	0.1	–	0.9	V_{SENS}
DS_057	ORT	Output response time[a]	100% input step of differential bridge measurement.[b]	–	–	5.0	ms
DS_059	F_{ALL_BR}	Overall failure. Deviation from ideal line including INL, gain, offset, and temperature impacts; excluding sensor-caused effects.	Differential sensor readout. V_{VDDE} = 4.75V to 5.25V	–	–	0.5	%FS
	$F_{ALL\_BR\_EXTD}$[a]		Differential sensor readout. V_{VDDE_EXTD} = 4.5V to 5.5V	–	–	1.0	%FS
	$F_{ALL\_DERATED}$[a]		In the operating supply voltage range V_{VDDE_OP}.	–	–	5.0	%FS
DS_058	RE	Ratiometricity error	Maximum error for V_{VDDE} from 5V to 4.75V or to 5.25V. Ratiometricity error is already contained in overall failure (DS_059).	–	–	500	ppm
Internal Temperature Measurement Refer to section 7.3.3.							
Informational	–	ADC resolution[a]		13	–	13	Bit
Informational	–	Output response time[a]	100% input step of measurement. [b]	–	–	50	ms
DS_036	ST_{TSI}	Internal temperature PTAT sensitivity	Raw values, without conditioning calculation; analog gain = 12.6.	20	–	–	LSB14 /K
External Diode Temperature Measurement Refer to section 7.3.4							
Informational		ADC resolution[a]		13		13	Bit

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Informational		Output response time[a]	100% input step of measurement [b]			50	ms
DS_038	I_{TSE_D}	External temperature diode bias current		10	20	40	µA
DS_039	V_{TSE_D}	External temperature diode input range[a]	Related to V_{TOP}, absolute measurement	-1		-0.2	V
SENT Output Refer to *SAE J2716 Specification JAN2010 and APR2016* for detailed specifications for the SENT Physical and Software Layer.							
DS_048	t_{TICK}	Tick time[a]		3	–	90	µs
DS_049	t_{TICK_JITTER}	Tick time jitter[a], [c]	Valid for tick time ≤ 10µs; 6-sigma value.	–	–	300	ns
DS_050	n_{SDM}	Number of SDMs	Absolute count of different messages.	0	–	32	–
DS_051	n_{SDM_CYC}	Number of SDM in SDM cycle	Message count in SDM cycle, including use of different priority levels.	0	–	64	–
DS_052	n_{SDM_PRIO}	SDM transmission priority levels		1	–	3	–
DS_053	t_{PAUSE}	Pause length	Fixed frame length.	12	–	768	t_{TICK}
DS_054	t_{FRAME}	Frame length	Pause pulse disabled, 6 data nibbles, and variable frame length.	154	–	270	t_{TICK}
			Pause pulse enabled, 6 data nibbles, and fixed frame length.	282	–	922	t_{TICK}
System Response							
DS_047	FMT	Fault messaging time[a]	t_{TICK} = 3µs, SENT pause pulse enabled, and the SENT frame length is set to the minimum.	–	–	50	ms
DS_055	$t_{STARTUP}$	Startup time[a]	Time to first valid output after power-on; V_{VDDE} slew rate > 0.1V/µs. [b]	–	–	10	ms

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] t_{TICK} = 3µs, transmission on SENT Fast Channel, SENT pause pulse enabled, and the SENT frame length is set to the minimum.

[c] Compliant to SENT J2716 APR2016 – JAN2010, which specifies maximum jitter of 50ns at tick time = 3µs and maximum jitter of 250ns at tick time = 10µs.

6. Interface Characteristics and Nonvolatile Memory

Table 5. Interface Characteristics and Nonvolatile Memory

Specification	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ZACwire™ One-Wire Interface One-wire communication at the DOUT pin.							
DS_060	t_{PWRUP}	Power-on time[a]	Time to ready for communication after power-on; V_{VDDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz.	–	–	3.0	ms
DS_061	$t_{OWI\_STARTWIN}$	Start window[a]	OWI enabled latest 5ms after power-on; V_{VDDE} slew rate > 0.1V/µs	–	250	–	ms
DS_062	$V_{OWI\_IN\_H}$	OWI voltage level HIGH	Master to slave.	0.80	–	–	V_{DDE}
DS_063	$V_{OWI\_IN\_L}$	OWI voltage level LOW	Master to slave.	–	–	0.20	V_{DDE}
DS_064	$V_{OWI\_OUT\_L}$	Slave output level LOW	Open drain, I_{OL} < 2mA.	–	–	0.1	V_{DDE}
Selected I2C Interface Parameters The I2C interface complies with the *I2C Bus Specification, Version 6.0, April 4, 2014.*							
DS_171	V_{I2C_HIGH}	I2C input voltage level HIGH	Master to slave	3.0			V
DS_172	V_{I2C_LOW}	I2C input voltage level LOW	Master to slave			0.5	V
DS_173	$V_{I2C\_LOW\_OUT}$	Slave output level LOW	Open drain, I_{OL} < 4mA			0.5	V
DS_174	C_{I2C_SDA}	SDA load capacitance				400	pF
DS_175	f_{I2C}	SCL clock frequency				400	kHz
DS_176	R_{I2C_PULLUP}	Internal pull-up resistor[a]		25		100	kΩ
Nonvolatile Memory (NVM)							
DS_065	T_{AMB_NVM}	Ambient temperature for NVM programming[b]		-40	–	125	°C
DS_066	N_{NVM_PAGE}	NVM page count [a]	Pages available for writing	22	–	–	
DS_067	t_{NVM_RET}	Data retention[a]	Temperature profile.[d]	15	–	–	years
DS_068.1	$t_{NVM\_WRI\_DIFF}$	Programming time without soaking[a]	Per programmed data word in differential mode			1.7	ms
DS_068.2	$t_{NVM\_WRI\_RED}$		Per programmed data word in redundant mode			3.3	

[a] No measurement in volume production; parameter is guaranteed by design and/or quality observation.

[b] Take into consideration additional package and temperature range restrictions.

[c] Differs from the referenced I2C-bus specification.

[d] Over lifetime and valid for the dice. Package can cause additional restrictions.

7. Circuit Description

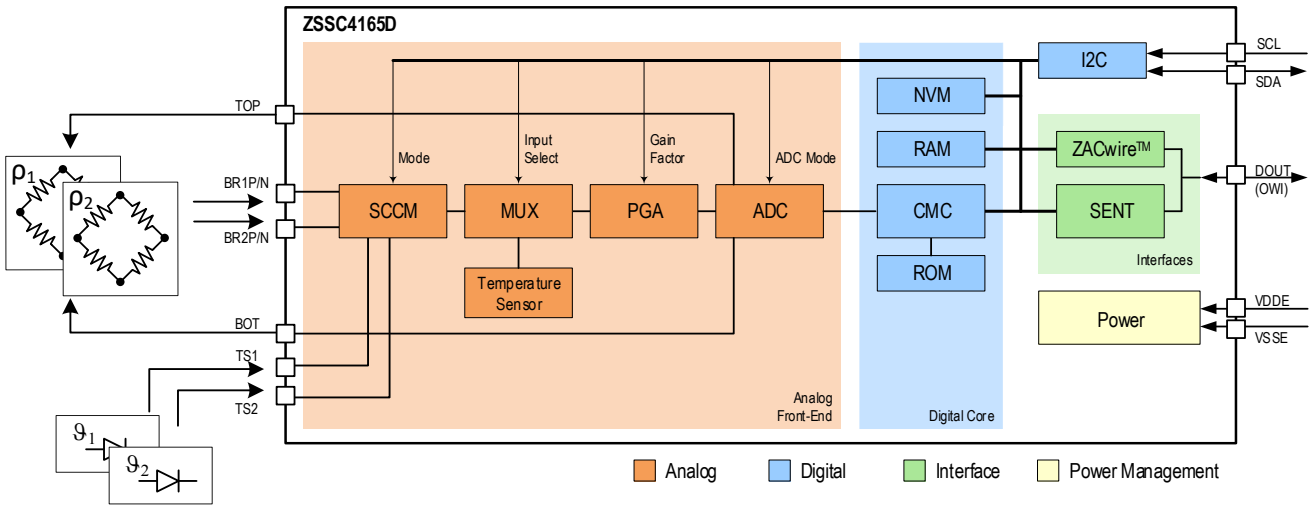
7.1 General Operation Description

The ZSSC4165D-01 is a sensor signal conditioner for readout of resistive bridge sensors by the following process:

1. The sensor signal is pre-amplified and converted to a digital signal by the analog-to-digital-converter (ADC).
2. The digital conversion result is offset compensated and gain adjusted.
   Temperature coefficients and nonlinearity of the sensing element are compensated, if necessary.
3. The calculated conditioning result is output using the SENT protocol.

Signal conditioning processes the following tasks:

- Measurement of the voltage signal of the connected resistive sensing element
- Measurement of temperature
- Conditioning calculation for the sensor signal
- SENT output of the conditioning result



MUX	Multiplexer	NVM Coefficients	Nonvolatile Memory for Configuration and Conditioning
PGA	Programmable Gain Amplifier	RAM	Volatile Memory for Configuration and Conditioning Coefficients
ADC	Analog-to-Digital Converter	SENT	SENT Controller and SENT Physical Layer Output Stage
CMC	Calibration Microcontroller	SCCM	Sensor Check and Common Mode Adjustment Unit
I2C	I2C Digital Interface	ROM	Read-Only Memory for Correction Formula and Algorithm
ZACwire™	Digital One-Wire Interface	Power	Power Management and Protection Unit

Figure 3. Block Diagram

7.2 Analog Front-End

The analog front-end (AFE) consists of the sensor connection check module (SCCM), the multiplexer (MUX), the programmable gain amplifier (PGA), and the analog-to-digital converter (ADC). The internal offset of the AFE is eliminated by an auto-zero compensation. An internal PTAT is used to measure the die temperature.

7.2.1. SCCM

The sensor check and common mode block (SCCM) implements the self-diagnostic features for the AFE. The SCCM provides the sensor connection checks (short and open circuit) as well as several other diagnostic functions (see Table 12. Application Monitors).

7.2.2. Input Multiplexer

The input multiplexer (MUX) selects one of the various inputs and connects it to the signal path allowing the use of a single ADC. It allows a very flexible signal routing between the sensors and the ZSSC4165D-01.

7.2.3. Programmable Gain Amplifier

The sensor signal can be amplified by the on-chip programmable amplifier (PGA) using a gain between 2 and 200. For some BIST measurements, the PGA is bypassed and the sensor signal is put directly to the ADC. The gain is adjustable for the main measurements in order to provide an ADC input signal span of greater than 50% FS.

Recommendation: To achieve the best stability and linearity performance of the AFE, operate the PGA in a differential output voltage range within 10% to 90% of the ratiometric reference voltage $V_{REF} = V_{SENS} = (V_{TOP} – V_{BOT})$. The gain must be selected to guarantee this constraint for the entire operating temperature range of the application and for the specified sensor bridge tolerances.

7.2.4. Analog-to-Digital Converter

The analog-to-digital converter (ADC) is implemented using the full-differential switched-capacitor technique. The conversion is largely insensitive to short-term and long-term instabilities of the clock frequency. The ADC allows adjusting the A/D conversion input voltage range shift.

7.3 Signal Paths

The ZSSC4165D-01 signal path consists of the analog front-end (AFE), the digital signal processing unit, the SENT controller, and the SENT physical interface (SENT PHY).

A multiplexer (MUX) selects and transmits the signals from either the bridge sensor or the selected temperature sensor to the analog-to-digital converter (ADC) in a defined sequence. The temperature sensors can be an external diode or the internal proportional-to-absolute-temperature (PTAT) source as selected by the NVM configuration.

The digital signal correction is processed in the calibration microcontroller (CMC) using ROM-resident correction formulas and sensor-specific coefficients stored in the NVM. The configuration data and the conditioning coefficients are programmed into the NVM during the calibration process by digital one-wire communication via the DOUT pin.

During the calibration process, raw measurement values can be requested via the digital interfaces.

The ZSSC4165D-01 provides SENT transmission according to the *SAE J2716 SENT Specification JAN2010 and APR2016*. Depending on the programmed configuration, there are several SENT output modes. These modes include assignment of the various sensor signals to the SENT Fast and Serial Data Message (SDM) communication channels as well as the configuration of the SENT frame itself.

Note: The P1 and P2 physical input signals are typically pressure but can be any other physical signal input for a resistive bridge.

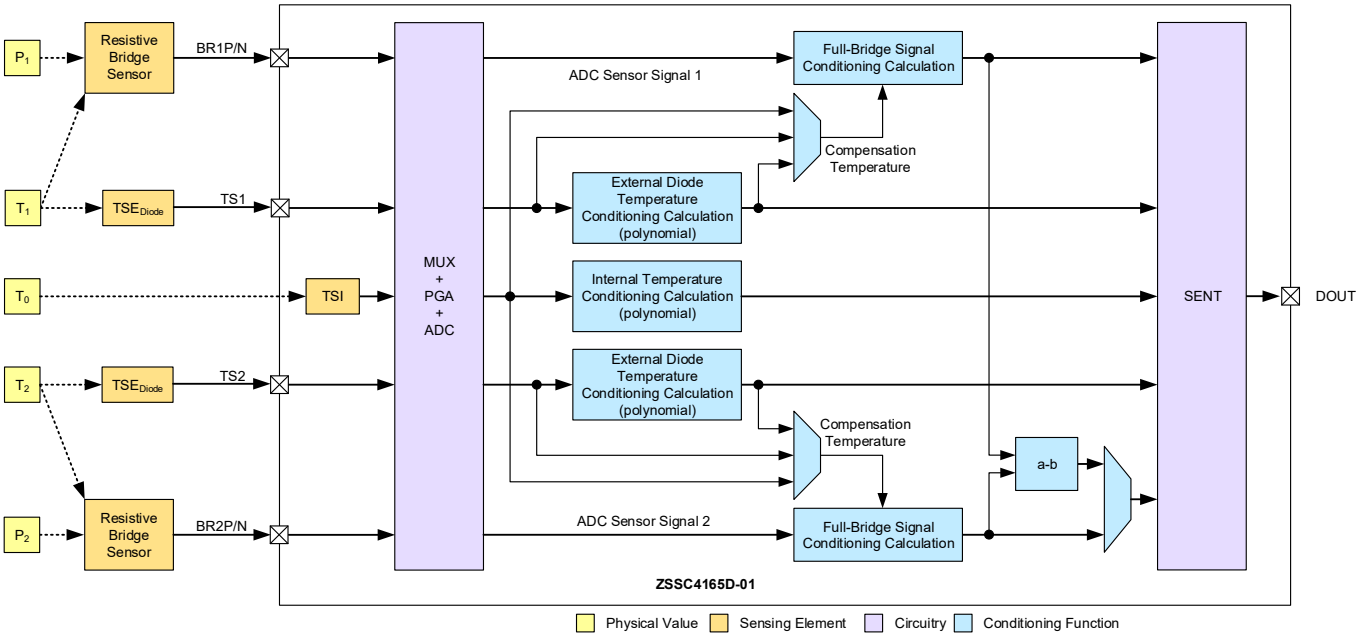


Figure 4. Main Signal Path

7.3.1. Full-Bridge Sensor Path

7.3.1.1. Measurement

The ZSSC4165D-01 measures two differential sensor signals (BR1P/BR1N and BR2P/BR2N) from the bridge. The signal paths are ratiometric, fully differential, and independent from each other. The ratiometric reference voltage is equal to (V_{TOP} – V_{BOT}).

The following parameter settings can be selected by the user for each of the two differential full-bridge measurements independently.

- PgaGainSel: 2.1 to 200
- AdcRngSh: 1/16, 1/8, 1/4, or 1/2
- MuxSel: BR1, BR1i, BR2 or BR2i
- AdcRsl: 14 bits, 15 bits, 16 bits, 17 bits, or 18 bits
- MeasZoom: 0 to 15 (for resolution >= 16 bits)
- SettleTime: 10 steps from 0ms to ~2ms

The measurement result is a 16 bit signed integer value, called ‘Measurand’:

$$Measurand = \left(PgaGainSel \times V\frac{VIN}{VTOP - VBOT} + AdcRngSh - \frac{MeasZoom}{16}\right) \times 2^{15+scale}$$

The input voltage V_{IN} is either from bridge pins BR1P/BR1N or BR2P/BR2N, depending on the MuxSel parameter. The ‘I’ for the MuxSel parameters stand for ‘inverted’.

7.3.1.2. Conditioning

The full-bridge sensor signal conditioning is processed every time when a new Measurand (measurement result) is available for each of the two channels. The conditioning calculation provides compensation of the temperature-dependent offset and gain and of the nonlinearity, independently of both full-bridge signal paths.

The source for the temperature compensation can be selected from two options:

- Internal chip temperature measurement (raw measurement or calibrated value)
- External Diode temperature measurement (raw measurement or calibrated value, independent external diode for both bridge channels)

The transfer function of the conditioning result 'Output', where 'Input' comes from the bridge measurement and 'Compensation' comes from the selected temperature signal, is described in following equations:

$$Output = 2^{wl3-56}C_{l3} \times Y^3 + 2^{wl2-41}C_{l2} \times Y^2 + 2^{wl1-25}C_{l1} \times Y^1 + 2^{wl0-9}C_{l0} \times Y^0$$

$$Y = \frac{Input + f_{offset}}{f_{gain}} \times 2^{14}$$

$$f_{offset} = 2^{wo2-40}C_{o2} \times Compensation^2 + 2^{wo1-25}C_{o1} \times Compensation^1 + 2^{wo0-9}C_{o0} \times Compensation^0$$

$$f_{gain} = 2^{wg2-40}C_{g2} \times Compensation^2 + 2^{wg1-25}C_{g1} \times Compensation^1 + 2^{wg0-9}C_{g0} \times Compensation^0$$

The conditioning coefficients coi, cgi, and cli are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights woi, wgi, and wli are unsigned 4-bit values (uint4).

For the second channel, a difference signal to the first bridge channel is generated. The 16-bit signed integer result of the subtraction can be normalized with a first-order polynomial (gain and offset).

The conditioning result 'Output' of each full-bridge sensor is stored as signed 16-bit value (sint16, two's complement) in the RAM output memory. These values can be low-pass filtered and can be assigned to SENT Fast output channels. The second channel can be configured to transmit the conditioned bridge measurement signal or the normalized result of the subtraction on the SENT interface.

7.3.2. Bridge Channel Difference

The two conditioned bridge values can be subtracted from each other. The difference can be normalized with a 1st order polynomial function and output on the SENT interface using Equation 1 and Equation 2.

$$Difference = (Channel1 - Channel2) \text{ or } (Channel2 - Channel1) \quad \textbf{Equation 1}$$

$$NormedDifference = 2^{w_1-24}c_1 * Difference^1 + 2^{w_0-9}c_0 \quad \textbf{Equation 2}$$

The conditioning coefficients c1 and c0 are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights w1, and w0 are unsigned 4-bit values (uint4).

7.3.3. Internal Temperature Path

7.3.3.1. Measurement

The ZSSC4165D-01 supports temperature measurement by a chip-internal PTAT sensor.

7.3.3.2. Conditioning

The internal temperature sensor signal conditioning is processed every time when a new measurement result value is available from the analog-to-digital conversion. The conditioning calculation provides compensation of offset, gain, and of the nonlinearity.

The transfer function of the conditioning output with input from the measurement is given in Equation 3:

$$Output = 2^{w_2-40}c_2 * Input^2 + 2^{w_1-25}c_1 * Input^1 + 2^{w_0-9}c_0 \quad \textbf{Equation 3}$$

The conditioning coefficients ci are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights wi are unsigned 4-bit values (uint4).

The conditioning result output is stored as a signed 16-bit value (sint16, two's complement) in the RAM output memory. This value can be assigned to a SENT SDM output.

7.3.4. External Temperature Path

7.3.4.1. Measurement

- Following parameters are selectable for the external diode temperature measurement:
- MuxSel: TS1 or TS2
- TsecHigh (the customizable upper threshold of the TSEC monitor)
- TsecLow (the customizable lower threshold of the TSEC monitor)

7.3.4.2. Conditioning

The external diode temperature sensor signal conditioning is processed every time when a new measurement result value is available from the analog-to-digital conversion. The conditioning calculation provides compensation of offset, gain, and of the nonlinearity.

The transfer function of the conditioning output with input from the measurement is shown in Equation 4:

$$Output = 2^{w_2-40}c_2 * Input^2 + 2^{w_1-25}c_1 * Input^1 + 2^{w_0-9}c_0$$ **Equation 4**

The conditioning coefficients ci are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights wi are unsigned 4-bit values (uint4).

The conditioning result output is stored as a signed 16-bit value (sint16, two's complement) in the RAM output memory. This value can be assigned to a SENT SDM output.

7.4 SENT Output

7.4.1. Overview

ZSSC4165D-01 provides three different digital interfaces for the output of data and status messages:

- The SENT controller and physical layer for SENT transmission enable readout of conditioned sensor data in compliance with *SAE J2716 JAN2010* and *SAE J2716 APR2016*.
- The ZACwire™ interface for one-wire communication supports the sensor configuration and manufacturing process.
- The I2C interface supports the sensor configuration and manufacturing process.

The SENT interface is the main application output interface. The configuration of the SENT frame format and the assignment of signals and fault messages to the SENT output channels are selectable.

7.4.2. SENT Fast Channel Modes and Frame Format

The ZSSC4165D-01 SENT interface supports various frame configurations:

- FC Data Format:
  - H.1 (H.5) (Pressure1, Pressure2 or Pressure1, Zero)
  - H.2 (Pressure1)
  - H.4 (Pressure1, Counter)
- Flip FC2: True, False (Flipping the nibbles of second fast channel)
- Frame Length: 282 to 1024 (if pause pulse is enabled)
- Pause Pulse: Enabled, Disabled
- Tick Time: 2.375µs to 90µs

The SENT frame transmission is not synchronized to the ZSSC4165D-01 internal output data update. The internal output data update depends on the parameter settings for the measurement tasks. The output update rate and the SENT frame length are generally different. Depending on the SENT frame length used, it is possible that individual data is either sent twice or it is skipped and not sent at all. After power-on, the initial output values of the SENT Fast data channels are defined by the selected SENT output mode as described in section 7.4.4.

7.4.3. SENT SDM Channel Modes

The ZSSC4165D-01 SENT interface supports up to 32 different serial data messages (SDM) transmitted in the SDM data channels. The SDM format, the number of SDMs, and the transmission priority are configurable as illustrated in the examples given in Table 6 and Figure 5.

The SMDs data format is as following:

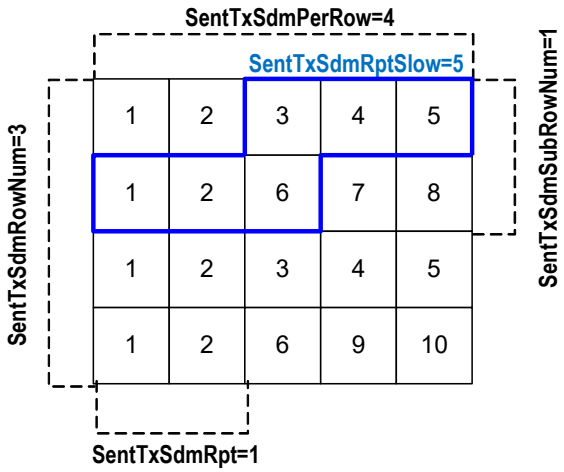
- Enhanced SDM format with up to 32 SDMs.
- Mode with no SDM available (SDM bits in the status nibble are set to “0”).
- Configurable SDM IDs.
- Three priority levels; configurable sequence of SDMs per priority level.

See section 8.2 regarding fault messaging using the SDM Channel. For programming instructions and descriptions of the fields used during configuration, refer to the *ZSSC4165D Functional Description* document included with the product delivery or available on request (see contact information).

Table 6. Example of SDM ID Priority Level and Sequence Configuration

Priority Level	SDM ID			
1	1	2		
2	3	4	5	6
3	7	8	9	10

Configuration via Field	Value
SDM Repeats	1
SDM Rows	3
SDM Columns	4
SDM Sub Repeats	5
SDM Sub Rows	1



Note: The blue line indicates the number of second-priority SDMs that are repeated in a cycle (adjusted by ’SDM Sub Repeats’).

Figure 5. SDM Cycle Example

7.4.4. SENT Output Operation Modes

The ZSSC4165D-01 provides the SENT output of the conditioned sensor element measurement results at the DOUT pin. This pin is also connected to the ZACwire™ interface for “End of Line” communication using a one-wire communication protocol (OWI).

There are four different modes for starting the OWI communication in combination with the SENT output:

- After Initialization:
  - SENT transmission starts immediately after the initialization phase.
  - During the initialization, the DOUT pin is set to the output idle state.
  - SENT data channels are set to their initial value (usually “0”) until the first valid conditioned differential bridge values are available.
  - OWI Rx is enabled in parallel with the SENT output for a time window.
  - OWI communication can be started by transmitting the command for starting Command Mode (CM) during this time window. The communication master must overwrite the output potential at the DOUT pin for transmitting the first command (DOUT pin drive capability is current limited).
- After the First Measurement:
  - SENT transmission starts after the first measurement and conditioning cycle and thus with the first valid conditioned bridge values.
  - During the initialization and the first cycle, the DOUT pin is set to the output idle state.
  - SENT data channels start transmission with valid values.
  - This mode allows the fastest possible transmission of the first conditioned bridge data after power on.
  - OWI Rx is enabled in parallel with the SENT output for a time window.
  - OWI communication can be started by transmitting the command for starting CM during this time window. The communication master must overwrite the output potential at the DOUT pin for transmitting the first command (DOUT pin drive capability is current limited).
- After 250ms:
  - SENT transmission starts only after a time window (about 250ms); the DOUT pin is set to the output idle state.
  - DOUT is weakly pulled to VDDA (pull-up current: about 2.5µA). OWI Rx is enabled for a specified time window.
  - OWI communication can be started by transmitting the command for starting CM during this time window.
- Disable SENT:
  - SENT transmission is disabled. OWI Rx/Tx is enabled without time limitation. OWI communication can be started by transmitting the command for starting CM.

The output idle state of the ZSSC4165D-01 is defined as follows:

- The DOUT pin is switched to high impedance; DOUT is weakly pulled to VDDA (pull-up current: about 2.5µA).
- The final resulting potential at the output is defined by the (pull-up) load resistor at the SENT communication line.

7.4.5. SENT Pulse Shaping

The ZSSC4165D-01 has several fixed adjustment options optimized for rise and fall times depending on the SENT tick time. This helps optimize electromagnetic compatibility (EMC) performance regarding electromagnetic emission.

7.5 Timing Definitions

Timing for the SENT output update and for the fault messaging is defined in Figure 6, relevant timing parameters are listed in Table 7. The output update rate and the output response time depend on the configuration parameters, more information in chapter “Timing Relevant Parameter” in the *ZSSC4165D-01 Functional Description* document.

Table 7. Timing Parameters

Symbol	Parameter	Description
OUR	Output update rate	Internal update rate of the main signal data
ORT	Output response time	Latency from the main signal event to the completion of the SENT transmission of this signal event

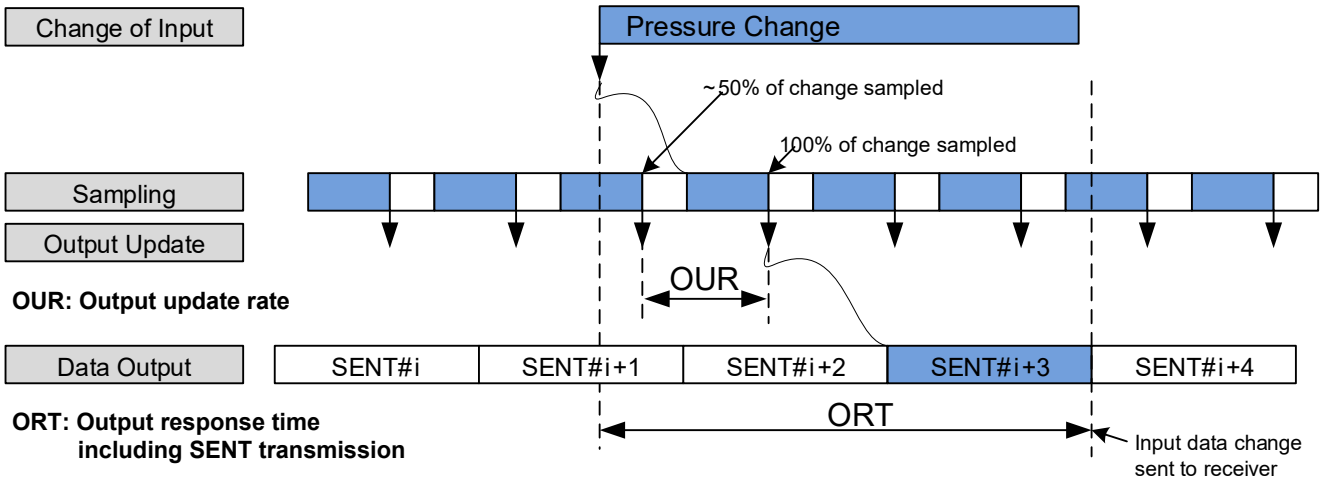


Figure 6. Output Update Timing Diagram

7.6 NVM OEM Data Memory

The ZSSC4165D-01 provides an NVM memory area for the storage of OEM data, which is physically part of the one-time programmable (OTP) NVM memory module, but it is delimited from the configuration and calibration data by dedicated commands for READ and WRITE access. Data protection and multiple-time programming data management must be implemented by the OEM.

There is a total of 128 registers of NVM data memory that are available for use by the customer: 64 registers accessible with the normal command set and 64 registers accessible with the dedicated command set.

Table 8. NVM OEM Data Memory

Requirement	Parameter	Value	Unit
DS_081	NVM OEM data memory (OTP) with normal command set	64	16-bit words
DS_082	NVM OEM data memory (OTP) with dedicated command set	64	16-bit words

7.7 Over-Voltage and Short-Circuit Protection

The ZSSC4165D-01 is designed for a 5V supply provided by an electronic control unit (ECU). The ZSSC4165D-01 and the connected sensor elements are protected from over-voltage and reverse-polarity damage by an internal supply voltage limiter. The DOUT pin is protected from short circuits, over-voltage, and reverse polarity. These functions are described in Table 9 and are valid for operation of the ZSSC4165D-01 in the application circuit shown in section 10 within the specifications of absolute maximum ratings given in section 3.

Note: The specified junction temperature range T_J (see Table 2) is in force not only for operation but also for all protection cases listed in Table 9. In the event of an over-voltage, the device could have increased power

dissipation. Depending on the sensor elements and the output load, this might lead to a violation of the maximum junction temperature.

Table 9. Over-Voltage, Reverse-Polarity, and Short-Circuit Protection

Specification	Symbol	Parameter	Description	Min	Typ	Max	Unit
Over-Voltage and Reverse-Polarity Protection							
DS_085	V_{DDE_OV1}	Maximum voltage at VDDE to VSSE	Independent of resistance between DOUT and VSSE or VDDE	0		18	V
DS_086	V_{DDE_OV2}	Maximum voltage at VDDE to DOUT [a]	Independent of resistance between VSSE and DOUT or VDDE	0		18	V
DS_087	V_{DOUT_OV1}	Maximum voltage at DOUT to VSSE	Independent of resistance between VDDE and DOUT or VSSE	0		18	V
DS_088	V_{DOUT_OV2}	Maximum voltage at DOUT to VDDE[a]	Independent of resistance between VSSE and DOUT or VDDE	0		18	V
DS_089	V_{SSE_OV1}	Maximum voltage at VSSE to VDDE[a]	Independent of resistance between DOUT and VSSE or VDDE	0		18	V
DS_090	V_{SSE_OV2}	Maximum voltage at VSSE to DOUT[a]	Independent of resistance between VDDE and DOUT or VSSE	0		18	V
Short-Circuit Protection							
DS_091	$I_{VDDA\_SHRT\_VSSA}$	Current limitation in the event of a VDDA to VSSA short circuit	The output is deactivated (high Z). The supply current is limited to 60mA.			60	mA
DS_092	$I_{DOUT\_SHRT\_VSSE}$	Current limitation in the event of a DOUT to VSSE short circuit	Output is activated, output current limitation has been adjusted	-10		-2	mA
DS_093	$I_{DOUT\_SHRT\_VDDE}$	Current limitation in the event of a DOUT to VDDE short circuit	Output is activated, output current limitation has been adjusted	2		10	mA

[a] Reverse polarity condition.

8. Fault-Safe Operation

8.1 Fault-Safe Operation Modes

Fault checks verify the operation of the ZSSC4165D-01 and of the connected sensing elements at power-on and during Normal Operation Mode (NOM). If a fault is detected, the Diagnostic Mode (DM) is activated and the fault status is provided via one of the two methods described in sections 8.1.1 and 8.1.2 depending on the diagnostic mode.

The ZSSC4165D-01 differentiates between two DMs with different behavior: Static Diagnostic Mode and Temporary Diagnostic Mode.

8.1.1. Static Diagnostic Mode

Features:

- Measurement and conditioning cycle are interrupted.
- SENT transmission is stopped; the output pin DOUT is driven to HIGH level.
  Static DM is not activated if the high-impedance on the DOUT pin is caused by supply under-voltage (VDDAPOR, VDDDBOD).
- The ZACwire™ interface for one-wire communication (OWI) is enabled. Both RAM output pages are readable. The command StrtCmdMd must be sent to switch to Command Mode for further command processing.
- The watchdog can trigger the Static Diagnostic Mode (or a full chip reset, depending on customizable settings)
- The ZSSC4165D-01 can be restarted by a power-off/power-on sequence.

8.1.2. Temporary Diagnostic Mode

Features:

- Measurement and conditioning cycle are continuously processed.
- Fault checks are continuously processed including fault filtering (see below).
- The ZSSC4165D-01 returns to Normal Operation Mode (NOM), including SENT transmission of valid sensor signals if fault checks do not detect continuation of fault conditions.

8.1.3. Fault Confirmation

The fault confirmation of the ZSSC4165D-01 is defined as follows:

- Fault confirmation is an up-and-down event counter that allows confirmation of a failure event.
- Fault confirmation is only processed for fault checks assigned to the Temporary DM.
- Fault confirmation is a low-pass filter that delays the activation and deactivation of the Temporary DM.
- In the event of a fault detection, faults are re-checked before entering Temporary DM.
- In the case of Temporary DM, detected fault conditions that no longer exist are re-checked before returning from Temporary DM to NOM.

8.2 Fault Messaging

8.2.1. Overview

The SENT interface offers three different options for fault messaging:

- Fault codes in the SENT FC data channels (for example, the channel used for pressure)
- Two status bits in the SENT status nibble
- SENT SDM Channel status word

8.2.2. SENT Fast Channel Fault Codes

For the 12-bit SENT Fast Channel, the output value interval [4089, 4095] is reserved for fault codes. This is according to the SENT standard. In addition, the value 0 is used for signal initialization (no valid data available).

In the ZSSC4165D-01, the SENT Fast Channel fault codes are selectable, and a dedicated fault code must be assigned to every supervised fault. A fault prioritization is available, and in the event of simultaneous detection of multiple faults, the fault code of the highest prioritized fault is transmitted.

8.2.3. SENT Status Bits

According to the SENT standard, the SENT status nibble contains two bits for status information. The assignment of the status bits to the individual detectable faults is configurable.

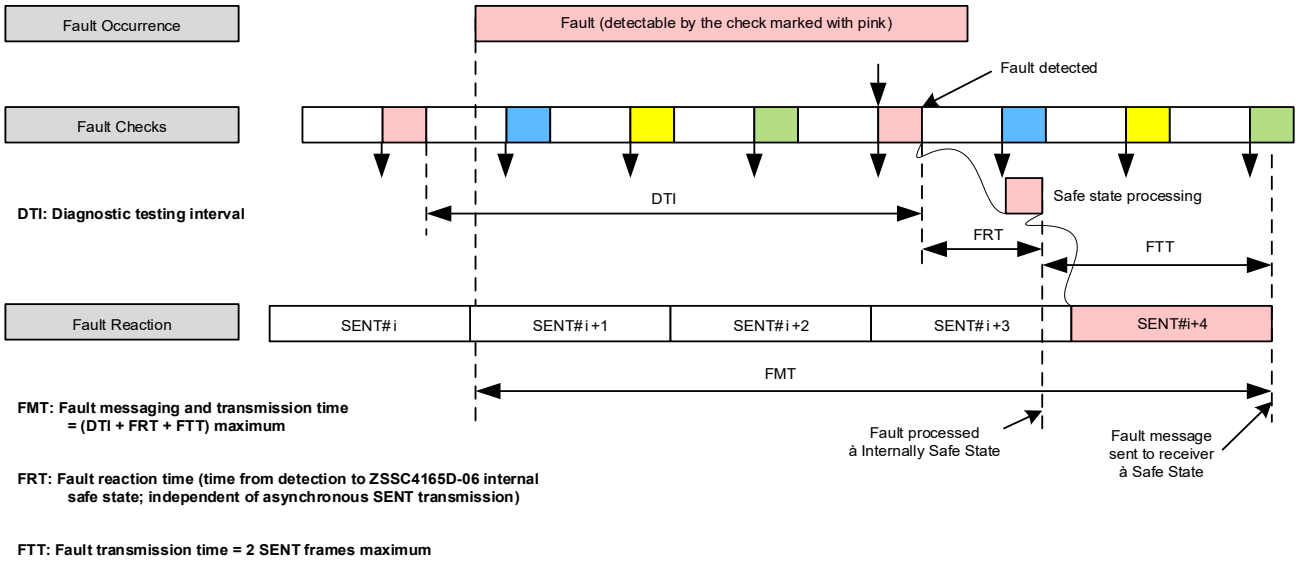
8.2.4. SENT SDM Channel Status Codes

The SENT standard defines a SMD Channel status word assigned to the SDM identifier #01.

In the ZSSC4165D-01, the SENT SMD Channel status codes are freely programmable, and a dedicated fault code must be assigned to every supervised fault. A fault prioritization is available, and in the event of simultaneous detection of multiple faults, the status code of the highest prioritized fault is transmitted.

8.2.5. Timing Definitions

The timing for the fault messaging is defined in Figure 7. See Table 4 for the fault messaging time (FMT) specifications. Refer to the *Configuration Description Report* regarding the timing for the diagnostic testing interval (DTI). This document is available on request from Renesas.



Note: In this figure, the different colors indicate the different fault checks processed in the cycle.

Figure 7. Fault Messaging Timing Diagram

9. Fault Checks

9.1 Overview

The ZSSC4165D-01 implements a diagnostic mechanism architecture that can support end-user applications requirements in regard to random failure diagnostic capabilities. These fault checks are supported by three types of monitors:

- Hardware Monitors – are implemented in the hardware and firmware of the ZSSC4165D-01
- Application Monitors – are defined by the ZSSC4165D-01 configuration and mainly check values for a certain range
- Transmission Monitors – are not implemented by the ZSSC4165D-01 but by the receiver of the conditioned signal data (ECU)

Table 10, Table 12, and Table 13 list the monitors for the supported fault checks.

9.2 Hardware Fault Checks

Table 10. Hardware Monitors

No.	Fault Check	Messaging Time	Active	DM Type
DS_094	V_{DDA} under-voltage check (VDDAPOR); power-on reset	< 200µs	Always on	Static
DS_095	Digital supply under-voltage check (VDDDBOD); brownout detection	< 200µs	Always on	Static
DS_096	Oscillator fail check (OSCFAIL)	< 200µs	Always on	Static
DS_097	ROM CRC check (ROMCRC)	< FMT	Always on	Static
DS_098	NVM CRC check (NVMCRC)	tSTARTUP	Always on	Static
DS_099	RAM CRC check (RAMCRC)	< FMT	Always on	Static
DS_100	RAM parity check (RAMPRTY)	< FMT	Always on	Static
DS_101	Windowed watchdog (WWDG)	< 2 ∗ OUR	Always on	Static
DS_102	Initialization phase check (INITCRC)	tSTARTUP	Always on [a]	Static
DS_103	Measurement cycle check (MCYCCRC) including • AFE input multiplexer check (AFEMUX) • Register data check (REGCRC)	< FMT	Always on [a]	Static

No.	Fault Check	Messaging Time	Active	DM Type
DS_104	Conditioning cycle check (CCYCCRC)	< FMT	Always on [a]	Static

[a] Must be ensured in customer production line by sending the *RunCycCrcCalc* command to the ZSSC4165D-01.

9.3 Application Monitors

The ZSSC4165D-01 provides several fault checks mainly based on the monitoring of a physical value; see Table 12 for a list of the application monitors. A fault is detected if the measurement value exceeds or falls below a given threshold. For every measurement, there is a specific transfer characteristic from the monitored physical value to the measurement value. The reverse function maps a threshold to a specific physical value. Because of the part-dependent measurement tolerance, a defined threshold spreads out over a certain range determined by a lower and an upper value. A fault is securely detected if the physical value falls below the lower value (A) coming from the lower threshold, or if it exceeds the upper value (D) coming from the upper threshold. Otherwise it is ensured that no fault is messaged if the physical value is in the range between the upper value (B) coming from the lower threshold and the lower value (C) coming from the upper threshold. See Figure 8 for an illustration of the thresholds and Table 11 for the definitions of A, B, C, and D.

Table 11. Fault Check Threshold Definition

Threshold	Description
A	If the physical value is below this measured value, the fault is securely detected and messaged.
B	If the physical value is above this measured value (and below the C value), a non-fault state is securely detected.
C	If the physical value is below this measured value (and above the B value), a non-fault state is securely detected.
D	If the physical value is above this measured value, the fault is securely detected and messaged.

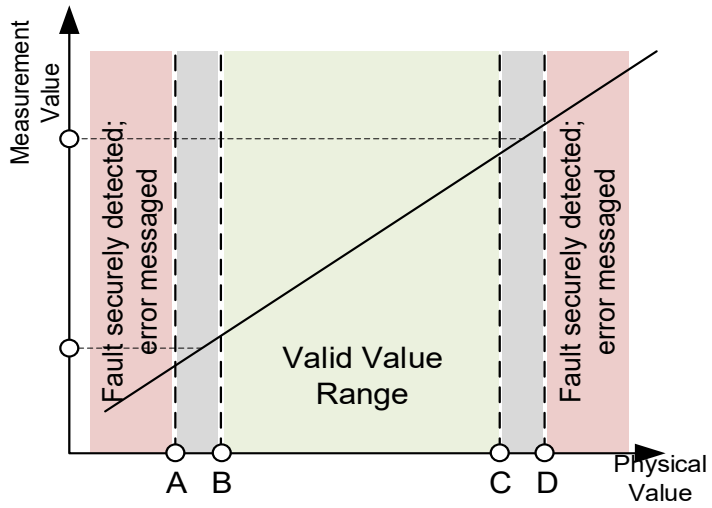


Figure 8. Fault Check Thresholds

Note that there are several application monitors. Some have thresholds that are predefined by Renesas. Others can have custom thresholds. All monitors require a correctly programmed and calibrated configuration to ensure the correct fault check operation.

Table 12. Application Monitors

No.	Group [a]	Block [b]	Monitor	Thresholds				Unit
				A	B	C	D	
DS_172	0	Hardware	ICSM	Custom				–
DS_173	1	Supply Monitor	VDDEOV	-		5.5	5.7	V
DS_174	2	Supply Monitor	VDDEUV	4.3	4.5	-		V
DS_175	3	Bridge2 Measurement	ADCOFFSRNG					
DS_110	3	Bridge1 Measurement	ADCOFFSRNG					
DS_111	3	AFE Gain Monitor	AFEGAIN					

No.	Group [a]	Block [b]	Monitor	Thresholds				Unit
				A	B	C	D	
DS_116	4	Chip-Temp Measurement	TSI					
DS_176	5	Chip-Temp Linearization	TSIRNG	Custom		Custom		
DS_114	6	Bridge1 Short Check	BRSS[c]	50	1650	–		Ω
DS_178	7	Bridge1 CSAT	CSAT	–				–
DS_179	7	Bridge1 Measurement	BRSRAW	See 9.3.1				
DS_113	7	Bridge1 Connection Check	BRSC[c]	–	–	8.5	295	kΩ
DS_180	8	Bridge2 Short Check	BRSS[c]	50	1650	–		Ω
DS_181	9	Bridge2 CSAT	CSAT	–				–
DS_182	9	Bridge2 Measurement	BRSRAW	See 9.3.1				
DS_183	9	Bridge2 Connection Check	BRSC[c]	–	–	8.5	295	kΩ
DS_184	10	Diode1 Measurement	TSEC	Custom		Custom		
DS_185	10	Diode1 Linearization	TSERNG	Custom		Custom		
DS_187	11	Diode2 Measurement	TSEC	Custom		Custom		
DS_188	11	Diode2 Linearization	TSERNG	Custom		Custom		
DS_118	13	Bridge1 Linearization	BRSRNG	Custom		Custom		–
DS_190	14	Bridge2 Linearization	BRSRNG	Custom		Custom		–
DS_191	15	Bridge2 DiffTrans	DRNG	Custom		Custom		–
DS_124	15	Computational Saturation Monitor	CSAT	–				–

[a] For each monitor group, a separate error code on the output interface can be defined. All monitors within a group will have the same error code assigned.

[b] See the Functional Description for more information.

[c] The connection- and short-check thresholds are independent of the bridge resistance

9.3.1. BRSRAW (Bridge1 Measurement and Bridge2 Measurement Monitors)

The limits of the ADC raw data check BRSRAW must be adjusted depending on the selected ADC resolution for the full-bridge measurement. The ADC raw data measurement register range is $[0,2^{15})$. If the resolution is higher than 15 bit, the digital zooming is activated and the range of the ADC results is different.

Table 13. BRSRAW Thresholds

ADC Resolution [bits]	ADC Result Range	Lower Limit	Upper Limit
14	$[0,2^{15})$	$0.04 \times (2^{15}-1)$	$0.96 \times (2^{15}-1)$
15			
16	$[-2^{15},2^{15})$	-32767	32766
17			
18			

9.3.2. BRSC (Bridge1 Connection Check and Bridge2 Connection Check)

The limits for the BRSC monitor cannot be changed. The sensor connection check is sensitive to bridge common mode variation. It triggers the Temporary Diagnostic Mode if the Common Mode changes more than ±15% referenced to the bridge supply voltage. This behavior is not a failure and is given by system design. The application design must account for this behavior on the module development level.

10. Application Circuit and External Components

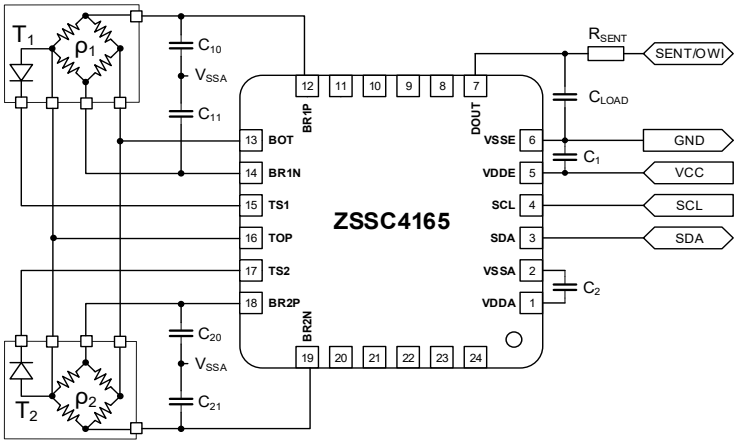
Specification	Circuit Diagram
DP_043	 Application features: • 5V module is powered by the application's electronic control unit (ECU). • Sensor module with 3-pin connector provides main sensor signal and media or ambient temperature measurement data via SENT output. • Temperature signal for pressure signal correction can be derived either from the on-chip PTAT or from an external diode (connected to TS1 or TS2). • End-of-line calibration uses one-wire communication via the DOUT pin.

Figure 9. Application Circuit Example

Table 14. Dimensioning of External Components for the Application Example

Note: The component values are examples and must be adapted to the requirements of the application, in particular to the EMC requirements.

Specification	Component	Symbol	Conditions	Min	Typical	Max	Unit
DP_044	Capacitor	C1	$V_{MAX} \geq 32V$	47 – 20%	100 ± 20%		nF
	Capacitor	C2	$V_{MAX} \geq 10V$	47 - 20%	100 ± 20%	470 + 20%	nF
	Capacitor	C_{LOAD}	$V_{MAX} \geq 32V$	2.2 – 20%	2.2	2.2 + 20%	nF
	Resistor	R_{SENT}				50	Ω
	Capacitor	C_{10}, C_{11}, C_{20}, C_{21}				10 + 20%	nF

11. ESD Protection and EMC Specification

11.1 ESD Protection

All pins have an ESD protection of up to 2kV according to the Human Body Model (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7). The VDDE, VSSE, and DOUT pins have an additional ESD protection of up to 4kV (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7).

The levels of ESD protection are tested with devices in a 4 × 4 mm 24-QFN package during the product qualification.

11.2 Electromagnetic Emission

The wired emission of the externally connected pins of the ZSSC4165D-01 is measured according to the following standard: *IEC 61967_4:2002 + A1:2006*.

Measurements must be performed with the application circuit described in Figure 9. SENT transmission uses a tick time of 9µs.

For the off-board pins, the spectral power measured with the 150Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 Code H10kN*. For the VSSE pin, the spectral power measured with the 1Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN*.

11.3 Conducted Susceptibility (DPI)

The conducted susceptibility of externally connected pins of the device is measured according to the *IEC 62132-4 standard*.

Measurements must be performed with the application circuit described in Figure 9. The sensor bridge is replaced by a 3-resistor string connected to TOP, BR1P, BR1N, and BOT. SENT transmission uses a tick time of 9µs.

Table 15 gives the specifications for the DPI tests. RES refers to the coupling impedance. CAP refers to the injection capacitance.

Table 15. Conducted Susceptibility (DPI) Tests

Requirement	Test	Frequency Range	Power [dBm]	Load Pins	Protocol	Error Band[a]	Comment
DS_169	DPI, direct coupled	1MHz to 10MHz	20dBm	VDDE, DOUT	SENT	±1%	RES = 50Ω CAP= 4.7nF
DS_170	DPI, direct coupled	>10MHz	30dBm	VDDE, DOUT	SENT	±1%	RES = 50Ω CAP = 4.7nF

[a] Error band regarding main signal (SENT FC1).

12. Reliability and RoHS Conformity

The ZSSC4165D-01 is qualified according to the AEC-Q100 standard, operating temperature grade 0.

The ZSSC4165D-01 complies with the RoHS directive and does not contain hazardous substances. The complete RoHS declaration update can be downloaded https://www.renesas.com/eu/en/document/cer/green-products-rohs-material-declaration-certificate.

12.1 Calculation of Power Dissipation and Junction Temperature

Calculation examples for self-heating (maximum thermal resistor in 24-QFN package is $R_{th\_JA\_QFN24}$ = 32K/W):

- Normal Operation:
  - Maximum supply current at 5.5V is 10mA
  - Minimum SENT load resistance of 10kΩ
  - Maximum power dissipation is given by Equation 5.

$$P_{max} = 5.5V \times 10mA + 5.5V \times \frac{5.5V}{10k\Omega} = 58mW \quad \textbf{Equation 5}$$

  - Temperature difference is given by Equation 6.

$$T_J - T_{AMB} = 32\frac{K}{W} * 58mW = 1.9K \quad \textbf{Equation 6}$$

→ With the conditions above, the maximum junction temperature T_J is about 2K greater than the ambient temperature T_{AMB}.

- Over-Voltage Conditions (18V):
  - Maximum power dissipation is $P_{max,OV}$ = 300mW; output is switched off.
  - Temperature difference is given by Equation 7.

$$T_J - T_{AMB} = 32\frac{K}{W} * 300mW = 9.6K \quad \textbf{Equation 7}$$

→ With the conditions above, the maximum junction temperature T_J is about 10K greater than the ambient temperature T_{AMB}.

13. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

For the 24-QFN package

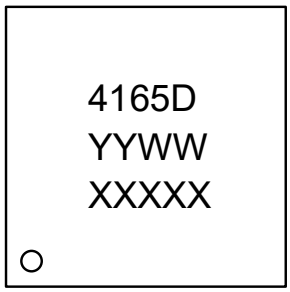
Package Outline Drawing Package Code: NLG24S2 24-VFQFPN 4.0 x 4.0 x 0.85 mm Body, 0.5mm Pitch

For the 16-TSSOP package:

ENG16 Package Outline Drawing 5.0 x 4.4 mm Body, 0.65mm Pitch TSSOP

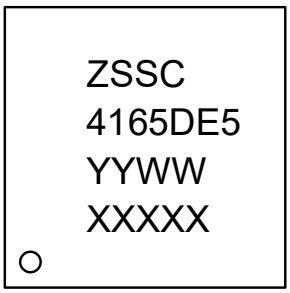
14. Marking Diagram

14.1 QFN24 Marking



1. “4165D” is the truncated part number.
2. “YYWW” is the last digits of the year and week that the part was assembled.
3. “XXXXX” is the last digits of the lot number.

14.2 TSSOP16 Marking



Line 1: “ZSSC” is the first part of the product family.

Line 2: “4165DE5” is the truncated part number, with special remark on DE5 for TSSOP package.

Line 3: “YYWW” is the last digits of the year and week that the part was assembled.

4. Line 4: “XXXXX” is the last digits of the lot number.

15. Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front-End
ASIL	Automotive Safety Integrity Level
BOD	Brownout Detection
BR	Bridge Sensor
CM	Command Mode
CMC	Calibration Microcontroller; optimized microcontroller architecture for Renesas signal conditioners
CMV	Common Mode Voltage
CSAT	Computational Saturation (an overflow of the 16-bit unsigned integer mathematics)
DM	Diagnostic Mode
DNL	Differential Nonlinearity
DTI	Diagnostic Testing Interval; the rate of fault check processing
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FMT	Fault Messaging Time; latency from the fault event to the completion of the transmission of the fault message
FS	Full Scale
FTT	Fault Transmission Time
HBM	Human Body Model
I/O	Input/Output
I2C	Inter-Integrated Circuit; serial two-wire data bus
INL	Integral Nonlinearity
LSB	Least Significant Bit
LSN	Least Significant Nibble
MSB	Most Significant Bit
MSN	Most Significant Nibble
MUX	Multiplexer
MTP	Multiple-Time Programmable
n.a.	Not Applicable
NOM	Normal Operation Mode
NVM	Nonvolatile Memory
ORNG	Over-Range Monitor
OTP	One-Time Programmable
OWI	One-Wire Interface
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
POR	Power-On Reset
PTAT	Proportional-to-Absolute Temperature
PTC	Positive Temperature Coefficient
PWR	Power Management and Protection Unit
QFN	Quad-Flat No-Leads – ZSSC4165D package
RAM	Volatile Memory for Configuration and Conditioning Coefficients
RISC	Reduced Instruction Set Computing
ROM	Read-Only Memory

Term	Description
SCCM	Sensor Check and Common Mode Adjustment Unit
SSC	Sensor Short Check (diagnostic task) or Sensor Signal Conditioner
TSI	Internal Temperature Sensor
TSSOP	Thin Shrink Small Outline – ZSSC4165 package
TQE	Extended Temperature Range Identifier
URNG	Under-Range Monitor
ZACwire™	Renesas-specific one-wire interface (OWI)

16. Ordering Information

Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
ZSSC4165DE1B	Dual bridge input, SENT output, internal and/or external temperature measurement, tested wafer	na	Wafer Boxes	-40°C to 150°C
ZSSC4165DE1C	Dual bridge input, SENT output, internal and/or external temperature measurement, tested die sawn on frame	na	Frame Boxes	-40°C to 150°C
ZSSC4165DE1D-ES	Dual bridge input, SENT output, internal and/or external temperature measurement, tested die in waffle pack	na	Waffle Pack	-40°C to 150°C
ZSSC4165DE4R	Dual bridge input, SENT output, internal and/or external temperature measurement, 4 × 4 mm 24-QFN, wettable flanks	MSL1	13” Reel	-40°C to 150°C
ZSSC4165DE5R	Dual bridge input, SENT output, internal and/or external temperature measurement, 4.4mm x 5.0mm 16-TSSOP with exposed pad (ENG16)	MSL1	13” Reel	-40°C to 150°C
ZSSC4165DE5T	Dual bridge input, SENT output, internal and/or external temperature measurement, 4.4mm x 5.0mm 16-TSSOP with exposed pad (ENG16)	MSL1	Tube	-40°C to 150°C
ZSSC4160EVKV1P5	ZSSC4160 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, 10 Samples.			

Contact Renesas for additional options.

17. Revision History

Date	Description
Apr 23.26	• Updated QFN-20L package recommendation (see “Pin Assignments”) • Removed “not applicable” from BR2P/BR2N pin descriptions (see “Pin Descriptions”) • Split programming time into 2x parameters (see “Interface Characteristics and Nonvolatile Memory”: DS_068) • Completed other minor changes
Jan.21.25	• DS_065: decreased the max limit to 125 • DS_066: Parameter changed
May.20.22	ZSSC4165DE4W removed
Aug.3.21	• Explanation for output update rate and output response time • New ordering codes for bare dies and TSSOP16 package • Correcting calculation of power dissipation
Aug.24.20	Initial release.