ZSSC4165D-05

Automotive Resistive Sensor Signal Conditioner with SENT Output

Description

The ZSSC4165D-05 is member of Renesas' family of CMOS integrated circuits for highly accurate amplification and sensor-specific correction of differential bridge sensor element signals. Featuring a maximum analog pre-amplification up to 200, the ZSSC4165D-05 is configurable to nearly all resistive bridges. This datasheet specifies one certain configuration – 4165_0500_05.

Digital compensation of offset, sensitivity, temperature drift, and nonlinearity are accomplished via a 16-bit RISC microcontroller. Calibration coefficients and configuration data are stored in the ZSSC4165D-05 nonvolatile memory (NVM), which is reliable in automotive applications.

The ZSSC4165D-05 supports internal PTAT as temperature reference.

Measured values are provided via a digital SENT interface. The SENT interface enables transmission of sensor data via its Fast Channel as well as transmission of supplementary data via its Serial Data Message (SDM) Channel (also referred to as the "slow" channel) using only one output pin. End-of-line calibration is also supported through this output pin via a One-Wire Interface (OWI). The ZSSC4165D-05 and the calibration equipment communicate digitally, so the noise sensitivity is greatly reduced. Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The ZSSC4165D-05 is optimized for automotive environments by overvoltage and reverse polarity protection circuitry, excellent electromagnetic compatibility, and multiple diagnostic features.

Typical Applications

- Fluid brake pressure sensing (PV)
- Hydraulic pressure sensing
  (e.g., steering systems with hydraulic steering support)
- Pneumatic pressure sensing
  (e.g., air brake systems; pneumatic shock absorbers)

Available Support

- Evaluation kit
- Application notes
- Calculation tools

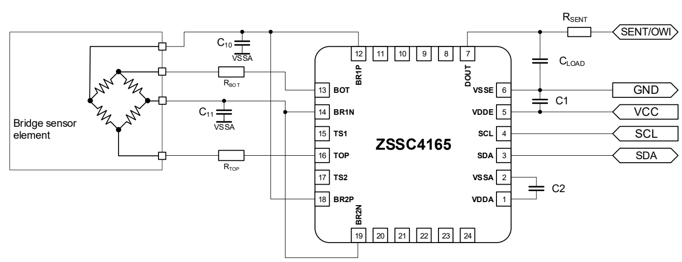
Features

- One differential full bridge sensor element measurement
- One single ended half bridge measurement derived from one of the full bridge signals on a separate input pin.
- One internal chip temperature measurement
- Digital compensation for offset, gain, and higher order nonlinearity as well as temperature coefficients of the differential and half bridge sensor element input signal
- Operating temperature range: -40°C to 150°C
- Accuracy: ±0.50% FS at -40°C to 150°C
- NVM memory for configuration, calibration data, and configurable measurement and conditioning functionality
- SENT output based on SAE J2716 Revision 3.0 standard using Fast and Serial Data Message Channels
- Supports output of one or more sensor signals and product identification via a single SENT interface connection
- One-pass, end-of-line calibration algorithm minimizes production costs
- No external trimming or components required
- Qualified according to AEC-Q100 Grade 0
- Support for the user´s ASIL B applications as HW qualified (ISO26262 Part 8-13) QM part (ISO 26262 Part9-6)

Physical Characteristics

- Supply voltage: 4.75V to 5.25V
- Over-voltage and reverse polarity protection up to ±18V
- Bridge sensor element input span: 1 to 800 mV/V
- Output resolution: 12-bit via SENT interface
- Package: 24-QFN (4 × 4 mm; wettable flanks)

ZSSC4165D-05 Basic Circuit



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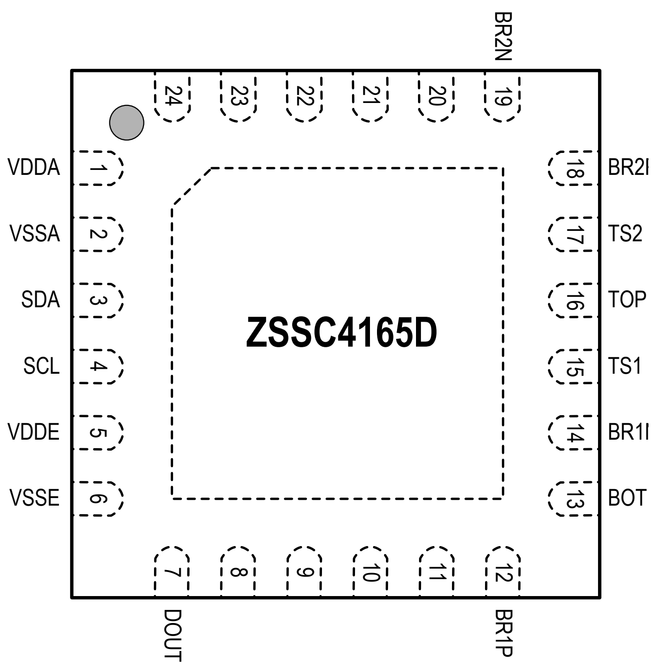
1. Pin Assignments

The ZSSC4165D-05 is available in a 24-QFN (4 x 4 mm; wettable flanks) RoHS-conformant package.

Note: The backside of the 24-QFN package (exposed pad; see section 13) is electrically connected to VSSA.

Recommendation: Solder the QFN exposed pad to the PCB, even if electrically redundant, to ensure adequate thermal performance and to reduce mechanical stress and solder joint failure risk.

Figure 1. 24-QFN Pin Assignments – Top View



2. Pin Descriptions

Table 1. Pin Descriptions

24-QFN Pin #	Pin Name	Type	Description
1	VDDA	Supply	Internal supply
2	VSSA	Supply	Internal ground
3	SDA [a], [b]	I/O	I²C data input/output with internal pull-up
4	SCL [a], [b]	Input	I²C clock, with internal pull-up
5	VDDE	Supply	External supply
6	VSSE	Supply	External ground
7	DOUT	I/O	SENT output and One-Wire Interface (OWI) input/output
8 to 11	–		n.c.
12	BR1P	Input	Positive bridge sensor input
13	BOT	Supply	Negative bridge supply voltage

24-QFN Pin #	Pin Name	Type	Description
14	BR1N	Input	Negative bridge sensor input
15	TS1	Input	not used
16	TOP	Supply	Positive bridge supply voltage
17	TS2	Input	not used
18	BR2P	Input	Positive bridge sensor input 2
19	BR2N	Input	Negative bridge sensor input 2
20 to 24	–	–	n.c.
-	EPAD [c]	Supply	Internal ground; connected to VSSA

[a] Internal pull-up

[b] No connection required

[c] Ground – can be shorted externally to VSSA (pin 2).

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the ZSSC4165D-05 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability. In addition, extended exposure to stresses above the operating conditions given in section 4 might affect device reliability.

See section 7.2.1 for information about overvoltage protection, reverse polarity, and short-circuit protection.

Table 2. Absolute Maximum Ratings

No.	Symbol	Parameter	Conditions	Min	Max	Unit
DS_177	V_{VDDE_MAX}	Supply voltage		-18	18	V
DS_178	V_{DOUT_MAX}	Voltage at the DOUT pin		-18	18	V
DS_179	V_{DIFF_MAX}	Pin voltage difference	Voltage between any two of these pins: VDDE, OUT and VSSE	-18	18	V
DS_180	V_{VDDA_MAX}	Analog supply voltage	On-chip controlled voltage; do not supply externally	-0.3	6	V
DS_181	V_{PIN_MAX}	Voltage at all other pins	Maximum voltage is V_{VDDA} + 0.3V	-0.3	6	V
DS_182	T_{J_MAX}	Junction temperature	Note: See section 7.2.1 regarding overvoltage protection	-40	160	°C
DS_183	T_{STOR_MAX}	Storage temperature		-55	155	°C

4. Operating Conditions

The operating conditions below specify the conditions that the application circuit must provide to the device during operation for proper function. Unless otherwise stated, the parameter limits in this section are applied as test conditions for the electrical parameters specified in section 5.

Table 3. Recommended Operating Conditions

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_009	V_{VDDE}	Supply voltage	VDDE to VSSE	4.75	5	5.25	V
DS_010	V_{VDDE_EXTD}	Extended supply voltage [a]	VDDE to VSSE; derated accuracy as specified with DS_059.	4.5	5	5.5	V
DS_011	V_{VDDE_OP}	Operating supply voltage [a]	VDDE to VSSE; derated accuracy and derated SENT pulse shaping outside of normal supply range V_{VDDE}. Note for a supply greater than 5.5V: Above the ZSSC4165D-05 overvoltage limitation threshold, the output potential is clipped at this threshold.	4		6	V
DS_012	T_{AMB}	Ambient temperature [a], [c]	Temperature Range	-40		150	°C
Informational [d]	$R_{th\_JA\_QFN24}$	Thermal resistance 24-QFN [a]	According to JESD 51		32		K/W
DS_185	R_{BR}	Bridge sensor resistance [a], [e]	One sensor bridge at pins BR1P and BR1N or BR2P and BR2N	1		10	kΩ

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] Temperature stress over lifetime is restricted to the Temperature Profile described in section 12 or to similar stress caused by equivalent temperature profiles. Use the calculation sheet *Temperature Profile Calculation Sheet* for temperature stress calculation.

[c] Assuming application conditions according to Test Board Design as per JESD51-7 and natural convection Test Conditions as per JESD51-2.

[d] Package-related parameter.

[e] Symmetric behavior and identical electrical properties (especially the low-pass characteristic) of the differential bridge sensor inputs are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins can generate a failure in signal operation.

5. Electrical Characteristics

All parameter values are valid under the operating conditions specified in section 4 (unless otherwise stated). All parameters are valid for the ambient temperature range T_{AMB} and for the supply voltage range V_{VDDE} = 4.75 to 5.25 V. Unless otherwise defined, the parameters are related to the ZSSC4165D-05 itself. All voltages are referenced to VSSA pin.

The following parameters are specified based on a ZSSC4165D-05 main channel configuration setup using a PGA gain of 100 and assuming a resulting ADC input range usage of ≥ 50%FS. Further preconditions are an ADC resolution of 14 bits, a 2-step A/D conversion scheme using an MSB-to-LSB ratio of 8/6 bit, an oscillator frequency of 8MHz, and an ADC clock frequency of 1MHz (1st step) / 2MHz (2nd step).

Table 4. Electrical Parameters

Note: See important table notes at the end of this table.

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
5.1 Supply Current and System Operating Conditions							
DS_015	I_S	Supply current	Excluding sensor supply current and excluding output current at DOUT pin; oscillator adjusted to f_{OSC} = 8MHz		8	10	mA
DS_016	P_{OV}	Overvoltage power consumption [a]	5.5V < V_{VDDE} < 18V; excluding sensor and output load			300	mW
DS_017	$V_{OV\_LIM\_TH}$	Overvoltage limitation threshold [a]	V_{VDDA} is limited if V_{VDDE} exceeds the threshold $V_{OV\_LIM\_TH}$.	5.55		18	V
DS_018	$V_{OV\_OFF\_TH}$	Overvoltage switch-off threshold [a]	The ZSSC4165D-05 is set to the reset state with limited current consumption if V_{VDDE} exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.	7		12	V
DS_019	$t_{OV\_OFF\_DLY}$	Overvoltage switch-off delay [a]	The ZSSC4165D-05 is set to the reset state with limited current consumption if V_{VDDE} exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$.		10	25	ms
DS_020	$I_{S\_OV\_OFF}$	Supply current limitation in the event of overvoltage switch-off [a]	Overvoltage switch-off is activated if the supply voltage exceeds the threshold $V_{OV\_OFF\_TH}$ for a time longer than $t_{OV\_OFF\_DLY}$. V_{VDDE} < 18V; excluding sensor and output load			10	mA
DS_184	V_{VDDA}	Analog supply voltage	V_{VDDA} is limited if V_{VDDE} exceeds the threshold $V_{OV\_LIM\_TH}$.	0.9		1.0	V_{VDDE}
DS_021	V_{SENS}	Bridge sensor supply voltage	$V_{SENS} = V_{TOP} - V_{BOT}$ at R_{BR} ≥ 1kΩ where V_{TOP} is the voltage at the TOP pin and V_{BOT} is the voltage at BOT pin.	0.9		1.0	V_{VDDA}

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_022	V_{POR_OFF}	Power-on reset off-threshold	V_{VDDA} measured referenced to VSSA; POR is active until V_{VDDA} exceeds this threshold.	3.3		3.8	V
DS_023	V_{POR_ON}	Power-on reset on-threshold	V_{VDDA} measured referenced to VSSA; POR is activated if V_{VDDA} falls below this threshold.	3.0		3.6	V
DS_024	V_{POR_HYST}	Power-on reset hysteresis [a]	V_{POR_ON} - V_{POR_OFF}		0.4		V
DS_025	f_{OSC}	Oscillator frequency	Calibrated oscillator frequency.	7.6	8	8.6	MHz
DS_026	TC_{OSC}	Oscillator frequency temperature coefficient [a]		-200		200	ppm/K
5.2 Analog Front-End Characteristics							
DS_027	V_{IN_SPAN}	Differential input span	Analog gain: 1 to 200	1		800	mV/V
DS_028	$V_{IN\_RNG\_1}$	Input voltage range	Analog gain = 1 Corresponds to V_{ADC_IN}	0.05		0.95	V_{SENS}
DS_029	$V_{IN\_RNG\_2}$		Analog gain = 2 to 200	0.3		0.65	V_{SENS}
DS_030	C_{IN}	Capacitance at input [a]	Capacitance at pins BR1P and BR1N to VSSA; Requirement for timing parameters	0		1.2	nF
5.3 A/D Conversion Refer to section 7.1.1.4.							
DS_032	r_{ADC}	ADC resolution [a]	Fixed resolution selection for each measured signal	11		14	Bit
DS_033	V_{ADC_IN}	ADC input range [a]	Differential input signal range depending on analog gain a_{PGA} and ADC range shift rs_{ADC}: $V_{ADC\_IN} = V_{IN} \times a_{PGA} + rs_{ADC} \times V_{SENS}$	0.05		0.95	V_{SENS}
			Restriction for analog gain > 100	0.1		0.9	V_{SENS}
DS_034	DNL_{ADC}	DNL [a]				0.95	LSB
DS_035	INL_{ADC}	INL	Best fit		3	8	LSB_{14}
5.4 Temperature Measurement							
DS_036	ST_{TSI}	Internal temperature PTAT sensitivity	Raw values, without conditioning calculation; analog gain = 12.6	20			LSB_{14}/K
5.5 Sensor Diagnostic Tasks							
DS_043	R_{BRSC_TH}	Sensor connection loss detection threshold	Fault check BRSC: Sensor pin to ZSSC4165D-05 pin connection; without capacitive load at bridge input pins	20		100	kΩ

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_044	r_{BRSC_TH}	Sensor bridge resistor short and open check threshold [a]	Fault check BRSCMRNG: Ratio of sensor bridge branch resistances. Deviation can be caused by shorts or opens of single bridge resistors or by resistor aging.		2		
DS_045	I_{LEAK_TH}	Input leakage detection threshold [a]	Based on common mode voltage measurement. BRSCMRNG check must be calibrated in conjunction with the sensor bridge. Detectable leakage current depends on the bridge sensor resistance R_{BR} and on the applied analog gain a_{PGA} (refer to Table 6). Limits must be adapted to the required safety target.		10		µA
5.6 System Response							
DP_036	$t_{STARTUP}$	Startup time [a]	Time to first valid output after power-on; V_{VDDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz			10	ms
DP_037	OUR	Output update rate [a],[d]	ZSSC4165D-05 internal output update, asynchronous to SENT transmission			1.5	ms
DP_012	ORT	Output response time [a],[d]	100% input step, t_{TICK} = 3µs, SENT pause = on, minimum			5	ms
DP_038	FMT	Fault messaging time [a],[d]	t_{TICK} = 3µs, SENT pause pulse enabled, and the SENT frame length is set to the minimum, One fault confirmation			20[e]	ms
DP_039	FMDT	Fault message disappear time [a],[d]	t_{TICK} = 3µs, SENT pause pulse enabled, and the SENT frame length is set to the minimum, One fault confirmation			30	ms
5.7 System Accuracy							
DS_058	RE	Ratiometricity error	Maximum error for V_{VDDE} from 5V to 4.75V or to 5.25V Ratiometricity error is already contained in overall failure (DS_059).			500	ppm

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_059	F_{ALL_BR}	Overall failure Deviation from ideal line including INL, gain, offset, and temperature impacts; excluding sensor-caused effects	Differential sensor readout V_{VDDE} = 4.75V to 5.25V			0.5	%FS
	$F_{ALL\_BR\_EXTD}$ [a]		Differential sensor readout V_{VDDE_EXTD} = 4.5V to 5.5V			1.0	%FS
	F_{ALL_HBR} [a]		Single-ended sensor readout V_{VDDE} = 4.75V to 5.25V			1.0	%FS
	$F_{ALL\_HBR\_EXTD}$ [a]		Single-ended sensor readout V_{VDDE_EXTD} = 4.5V to 5.5V			1.5	%FS
	$F_{ALL\_DERATED}$ [a]		In the operating supply voltage range V_{VDDE_OP}			5	%FS

5.8 Nonvolatile Memory

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DS_065	T_{AMB_NVM}	Ambient temperature for NVM programming [a]		-40		125	°C
DS_066	N_{NVM_PAGE}	NVM page count [a]	Pages available for writing.	22			
DS_067	t_{NVM_RET}	Data retention [a]	Temperature profile [b]	15			years
DS_068.1	$t_{NVM\_WRI\_DIFF}$	Programming time without soaking [a]	Per programmed data word in differential mode			1.7	ms
DS_068.2	$t_{NVM\_WRI\_RED}$		Per programmed data word in redundant mode			3.3	

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] The temperature sensor range is the calibration target for the SENT output of the SDM temperature channels. This target can be adjusted.

[c] Compliant to SENT – Rev. 4.0. Sent – Rev. 3.0 specifies maximum jitter of 50ns at tick time = 3µs and maximum jitter of 250ns at tick time = 10µs.

[d] Time values are given based on a system clock frequency of 8MHz.

[e] Except three Fault Checks which have an FMT <22ms, see Table 16(DS_124, DS_126, and DS_127)

6. Interface Characteristics

Table 5. Interface Characteristics and Nonvolatile Memory

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
6.1 SENT Output Refer to *SAE J2716 SENT Specification Rev. 3.0 (Jan. 2010)* for detailed specifications for SENT Physical and Software Layer.							
DS_048	t_{TICK}	Tick time [a]	Adjustment step = 1µs	3		90	µs
DS_049	t_{TICK_JITTER}	Tick time jitter [a], [c]	Valid for tick time ≤ 10µs, 6-sigma value			300	ns
DS_050	n_{SDM}	Number of SDMs	Absolute count of different messages	0		32	
DS_051	n_{SDM_CYC}	Number of SDM in SDM cycle	Message count in SDM cycle, including use of different priority levels.	0		64	
DS_052	n_{SDM_PRIO}	SDM transmission priority levels		1		3	
DS_053	t_{PAUSE}	Pause length	Fixed frame length.	12		768	t_{TICK}
DS_054	t_{FRAME}	Frame length	Pause pulse disabled, 6 data nibble, and variable frame length.	154		270	t_{TICK}
			Pause pulse enabled, 6 data nibble, and fixed frame length.	282		922	t_{TICK}
6.2 ZACwire™ One-Wire Interface – only for production purpose One-wire communication at the DOUT pin.							
DS_060	t_{PWRUP}	Power-on time [a]	Time to ready for communication after power-on; V_{VDDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz			3.0	ms
DS_061	$t_{OWI\_STARTWIN}$	Start window [a]	OWI enabled latest 5ms after power-on; V_{VDDE} slew rate > 0.1V/µs; f_{OSC} = 8MHz		250		ms
DS_062	$V_{OWI\_IN\_H}$	OWI voltage level HIGH [a]	Master to slave	0.80			V_{VDDE}
DS_063	$V_{OWI\_IN\_L}$	OWI voltage level LOW [a]	Master to slave			0.20	V_{VDDE}
DS_064	$V_{OWI\_OUT\_L}$	Slave output level LOW	Open drain, I_{OL} < 4mA			0.1	V_{VDDE}

[a] No measurement in volume production; parameter is guaranteed by design and/or quality observation.

[b] Over lifetime and valid for the dice. Note that the package can cause additional restrictions. Use the calculation sheet *Renesas Temperature Profile Calculation Sheet* for temperature stress calculation.

7. Circuit Description

7.1 General Operation Description

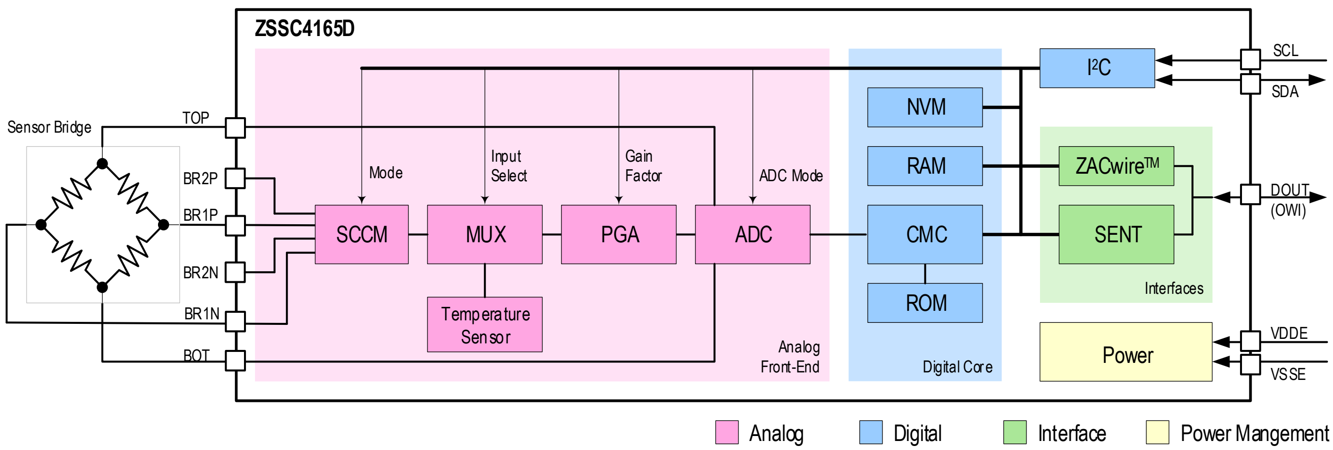
The ZSSC4165D-05 is a sensor signal conditioner for readout of resistive bridge sensor elements. This bridge sensor elements signal is pre-amplified and converted to a digital signal by the analog-to-digital-converter (ADC). Then the digital conversion results are offset compensated and gain adjusted. Temperature coefficients and nonlinearity of the bridge sensing element are compensated, if necessary. Nonlinearity of external temperature sensing elements are compensated in terms of nonlinearity. Then all calculated conditioning results can be output using the SENT protocol.

The ZSSC4165D-05 can measure a differential full bridge signal and a single ended half bridge signal from independent pins. All input pins are routed to the same multiplexer (MUX) for processing.

Signal conditioning processes the following tasks:

- Measurement of the voltage signal of the connected resistive sensing element
- Measurement of internal temperature
- Conditioning calculation for all sensor signals
- SENT output of the conditioning result

Figure 2. Block Diagram



SCCM	Sensor Check and Common Mode Adjustment Unit
MUX	Multiplexer
PGA	Programmable Gain Amplifier
ADC	Analog-to-Digital Converter
CMC	Calibration Microcontroller
ROM	Read-Only Memory for Correction Formula and Algorithm
NVM	Nonvolatile Memory for Configuration and Conditioning Coefficients
RAM	Volatile Memory for Configuration and Conditioning Coefficients
SENT	SENT Controller and SENT Physical Layer Output Stage
ZACwire™	Digital One-Wire Interface
I²C	I²C Digital Interface
PWR	Power Management and Protection Unit

7.1.1 Analog Front-End

The analog front-end (AFE) consists of the multiplexer (MUX), the programmable gain amplifier (PGA), and the analog-to-digital converter (ADC). The internal offset of the analog front-end is eliminated by an auto-zero compensation.

7.1.1.1 SCCM

The sensor check and common mode block (SCCM) implements the self-diagnostic features for the analog front-end. The SCCM provides the sensor connection checks (short and open circuit) as well as several other diagnostic functions.

7.1.1.2 Input Multiplexer

The input multiplexer (MUX) selects one of the various inputs and connects it to the signal path utilizing a single ADC. It allows a very flexible signal routing between the sensors and the ZSSC4165D-05.

7.1.1.3 Programmable Gain Amplifier

The sensor signal can be amplified by the on-chip programmable amplifier (PGA) using a gain between 2 and 200. Alternatively the PGA can be bypassed and the sensor signal is applied directly to the ADC. The gain is adjustable for bridge measurement task individually in order to provide an ADC input signal span of greater than 50% FS.

Table 6 shows the adjustable gains of the PGA, the corresponding signal spans, and the common mode range limits.

Table 6. Adjustable PGA Gains and Resulting Sensor Signal Spans and Common Mode Ranges

Nominal PGA Gain a_{PGA}	Maximum Input Span V_{IN_SPAN} [mV/V]	Input Common Mode Range V_{IN_CM} [% V_{VDDA}]
PGA bypassed	800	5 to 95
2.08	385	30 to 65
3.15	254	30 to 65
4.31	186	30 to 65
6.25	128	30 to 65
8.31	96	30 to 65
12.6	63	30 to 65
17.3	46	30 to 65
25.0	32	30 to 65
33.2	24	30 to 65
50.4	16	30 to 65
69.0	12	30 to 65
100.0	8	30 to 65
138.0	6	30 to 65
200.0	4	30 to 65

Recommendation: To achieve the best stability and linearity performance of the AFE, operate the PGA in a differential output voltage range within 10% to 90% of the ratiometric reference voltage $V_{REF} = V_{SENS} = (V_{TOP} – V_{BOT})$. The gain must be selected to guarantee this constraint for the entire operating temperature range of the application and for the specified sensor bridge tolerances.

7.1.1.4 Analog-to-Digital Converter

The analog-to-digital converter is implemented using the full-differential switched-capacitor technique. The conversion is largely insensitive to short-term and long-term instabilities of the clock frequency. The ADC provides adjustability of the A/D conversion input voltage range shift.

7.1.2 Signal Conditioning

7.1.2.1 Internal Temperature Sensor Signal Conditioning

The internal temperature sensor signal conditioning uses ROM resident formulas and temperature sensor specific coefficient stored inside NVM. Calculation is processed every time that a new measurement result value is available from the analog-to-digital conversion. The conditioning calculation provides compensation of offset and gain, and of the nonlinearity. Signal conditioning will map temperature sensor element input data to standardized SENT output format.

The conditioning coefficients for each compensation calculation are stored as signed 16-bit values (sint16, two's complement) in the NVM during the calibration process. The weights w_{tsi_i} are unsigned 4-bit values (uint4).

7.1.2.2 Full Bridge and Half Bridge Sensor Signal Conditioning

The full-bridge and the half-bridge sensor element signal conditioning uses ROM resident formulas and temperature sensor specific coefficient stored inside NVM. Calculation is processed every time that a new measurement result value is available from the analog-to-digital conversion. The conditioning calculation provides compensation of the temperature dependent offset and gain and of the nonlinearity.

The conditioning coefficients are stored as signed 16-bit values (sint16, two's complement) while the weights are stored as unsigned 4-bit values (uint4) in the NVM during the calibration process.

All intermediate results and the final conditioning results for the full-bridge or the half-bridge sensor are stored as signed 16-bit values (sint16, two's complement) in the RAM Output Memory. These values can be low-pass filtered and can be assigned to SENT Fast output channels.

7.1.2.3 Conditioning Cycle

The conditioning cycle is the sequence of equations and supervision functions processed during the Normal Operation Mode (NOM). It uses raw measurement results from measurement cycle and delivers conditioned output data for SENT output function.

7.1.3 Output Interfaces

ZSSC4165D-05 provides two different digital interfaces for the output of data and status messages:

- The SENT controller and physical layer for SENT transmission complies with the *SAE J2716 SENT Specification Jan. 2010 (Rev. 3.0)* and enables readout of conditioned sensor signal data during NOM.
- The ZACwire™ interface for one-wire communication supports sensor configuration and calibration process, and readout of conditioned sensor signal data during NOM.

7.1.3.1 SENT Output

The SENT interface is one of the main application output interfaces. The configuration of the SENT frame format and the assignment of sensor signals and fault messages to the SENT output channels are configurable.

In addition to other protocols, the SENT interface supports the application specific SENT protocols Single Sensor (P, P/t), Single Pressure Secure Sensor (P/S, P/S/t) and Pressure-Pressure Sensor (P1/P2, P1/P2/t).

7.1.3.1.1 SENT Fast Channel Modes and Frame Format

The ZSSC4165D-05 SENT interface supports various frame configurations:

- SENT Fast Channel Mode: one or two Fast data channels.
- SENT Transmission Mode: fixed SENT frame length and adjustable pause pulse, or SENT transmission without pause pulse.

DP_045	The 4165_0500_05 configuration provides the following different Fast data channel modes: ▪ 12-bit FC1 and 12-bit FC2 (6 nibbles) (H.1) ▪ 12-bit FC1, 8-bit counter and 4-bit zero (6 nibbles) (H.5)

The SENT frame transmission is not synchronized to the ZSSC4165D-05 internal output data update. The internal output data update is determined by the ADC resolution for the sensor signal measurements. The output data update time and the SENT frame length are generally different. Depending on the SENT frame length used, it is possible that individual data is either sent twice or it is skipped and not sent at all.

After power-on the initial output values of the SENT Fast data channels are 0 until the first valid output data is available from the measurement and conditioning cycle.

7.1.3.1.2 SENT SDM Channel Modes

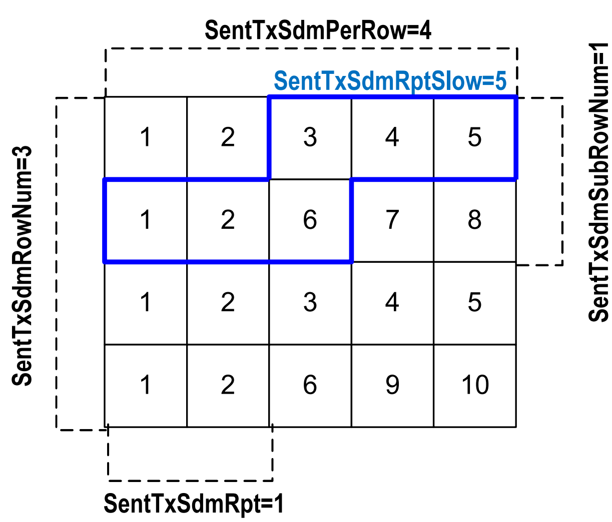
The ZSSC4165D-05 SENT interface supports up to 32 different serial data messages (SDM) transmitted in the SDM data channels. The SDM format, the number of SDMs, and the transmission priority are configurable:

- Enhanced SDM format with up to 32 SDMs
- Mode with no SDM available (SDM bits in the status nibble are set to "0")
- Configurable SDM IDs
- Three priority levels, configurable number of SDMs per priority level

  Example:

Priority Level	SDM ID			
1	*1*	*2*		
2	*3*	*4*	*5*	*6*
3	*7*	*8*	*9*	*10*

Configuration via field	Value
SentTxSdmRpt	*1*
SentTxSdmRowNum	*3*
SentTxSdmPerRow	*4*
SentTxSdmRptSlow	*5*
SentTxSdmSubRowNum	*1*



7.1.3.1.3 SENT Output Operation Modes

The ZSSC4165D-05 provides SENT output of the conditioned sensor element measurement results at the DOUT pin. This pin is also connected to the ZACwire™ interface for "End of Line" communication using a one-wire communication protocol (OWI).

There are four different modes of starting the OWI communication in combination with the SENT output:

SENT_TX_INIT:

- SENT transmission starts immediately after the initialization phase.
- During the initialization, the DOUT pin is set to the output idle state.
- SENT data channels are set to "0" until the first valid values are available.
- OWI Rx is enabled in parallel to the SENT output for a time window.
- OWI communication can be started by transmitting the command for starting Command Mode (CM) during this time window. The communication master must overwrite the output potential at the DOUT pin for transmitting the first command (DOUT pin drive capability is current limited).

SENT_TX_FIRST_CYC:

- SENT transmission starts after the first measurement and conditioning cycle.
- During the initialization and the first cycle, the DOUT pin is set to the output idle state.
- SENT data channels start transmission with valid values.
- OWI Rx is enabled in parallel to the SENT output for a time window.
- OWI communication can be started by transmitting the command for starting CM during this time window. The communication master must overwrite the output potential at the DOUT pin for transmitting the first command (DOUT pin drive capability is current limited).

SENT_TX_STRT_WINDOW:

- SENT transmission starts only after a time window; the DOUT pin is set to the output idle state.
- DOUT is weakly pulled to VDDA (pull-up current: ~2.5µA). OWI Rx is enabled for a specified time window.
- OWI communication can be started by transmitting the command for starting CM during this time window. The communication master must overwrite the output potential at the DOUT pin for transmitting the first command (DOUT pin drive capability is current limited).

OWI:

- SENT transmission is disabled. OWI Rx/Tx is enabled without time limitation. OWI communication can be started by transmitting the command for starting CM.

All fault checks are processed in the initialization phase before calculating the first conditioned sensor element signal. In the event of a detected failure and when no fault filtering is activated, the transmission starts with transmitting a fault code instead of transmitting invalid sensor data (different from initialization value "0") via the SENT interface in all SENT modes.

The output idle state of the ZSSC4165D-05 is defined as follows:

- The DOUT pin is switched to high impedance; DOUT is weakly pulled to VDDA (pull-up current: ~5 µA).
- The final resulting potential at the output is defined by the (pull-up) load resistor at the SENT communication line.

Table 7. SENT Output Operation Modes and Initialization Behavior

No.	Parameter	Value	Unit
DS_079	Number of SENT output operation modes (SENT_TX_INIT, SENT_TX_FIRST_CYC, SENT_TX_STRT_WINDOW, OWI)	4	–

7.1.3.1.4 SENT Pulse Shaping

The ZSSC4165D-05 provides several fixed adjustment options to optimize the rise and fall times depending on the SENT tick time. This helps to get optimal EMC performance regarding electromagnetic emission.

7.1.3.2 OWI Interface

The ZSSC4162D includes a serial digital interface that is able to support a ZACwire™ interface. After power on OWI communication can be started in a limited time window ($t_{OWI\_STARTWIN}$) or without time limitation in case that SENT output mode was set to OWI. Refer details on SENT output modes in section SENT Output Operation Modes.

The interface will allow access to:

- Conditioned bridge sensor element data
- Conditioned internal temperature sensor data
- IC Failure Status Summation Register
- IC Status Register

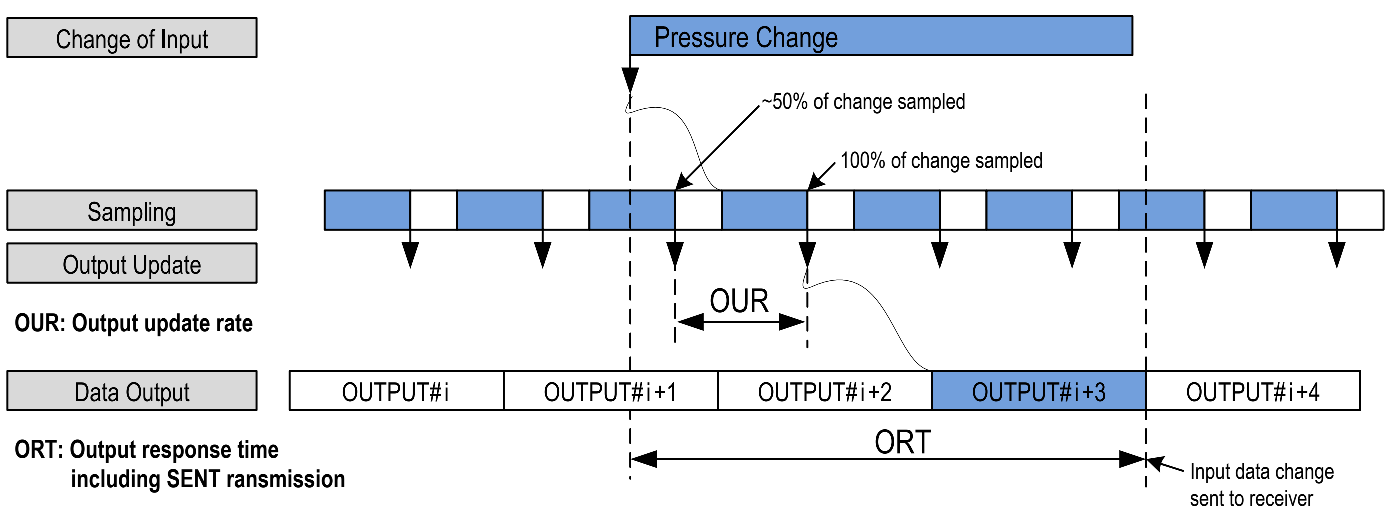
7.1.3.3 Timing Definitions

The timing for the update of the SENT output is defined in Figure 3. The relevant timing parameters are listed in Table 8.

Table 8. Timing Parameter

Symbol	Parameter	Description
OUR	Output update rate	Internal update rate of the main signal data
ORT	Output response time	Latency from the main signal event to the completion of the SENT, OWI, or I2C transmission of this signal event

Figure 3. Output Update Timing Diagram



7.1.4 NVM OEM Data Memory

The ZSSC4165D-05 provides a NVM memory area for the storage of OEM data, which is physically part of the NVM memory module (OTP; one-time programmable) but is delimited from the configuration and calibration data by dedicated commands for read and write access. Data protection and multiple-time programming data management must be implemented by the OEM.

Table 9. NVM OEM Data Memory

No.	Parameter	Value	Unit
DS_081	NVM OEM data memory (OTP)	8	16-bit words
DS_082	NVM OEM data memory (OTP) with dedicated command set	24	16-bit words

7.2 Signal Path

The ZSSC4165D-05 signal path consists of the analog front-end (AFE), the digital signal processing unit, the SENT Controller, and the SENT physical interface (SENT PHY). In addition, this is supported by a serial digital one-wire interface (ZACwire™) interface for production and calibration purpose.

DP_040	The resistive bridge sensor element signal is input via the BR1P and BR1N pins and is handled as a fully differential signal. Both signal lines have a dynamic range symmetrical to the common mode potential (analog ground; equal to $V_{VDDA}/2$) so that it is possible to process positive and negative differential input signals. These differential signals are pre-amplified by the programmable gain amplifier (PGA) and are converted to digital values by the A/D converter (ADC). In addition, the measurement of a half-bridge sensor signal is available by one of the BR2P or BR2N pins referenced to an on-chip reference half-bridge and using the same signal path.

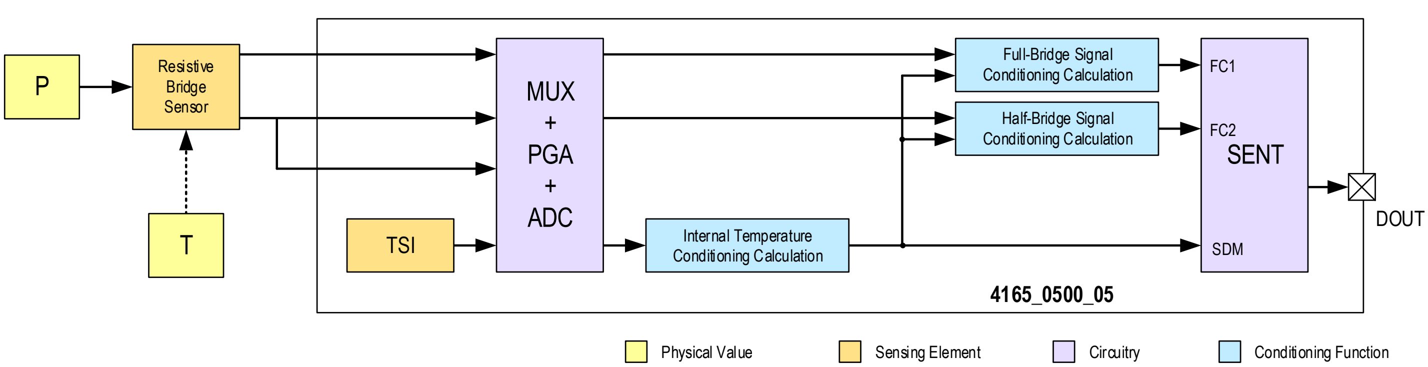
A multiplexer (MUX) selects and transmits the signals from either the bridge sensor or the selected temperature sensor to the analog-to-digital converter (ADC) in a defined sequence. The temperature sensor is an internal proportional-to-absolute-temperature (PTAT).

The digital signal correction is processed in the calibration microcontroller (CMC) using ROM-resident correction formulas and sensor-specific coefficients stored in the NVM. The configuration data and the conditioning coefficients are programmed into the NVM during the calibration process by digital one-wire communication via the DOUT pin.

During the calibration process, raw measurement values can be requested via the digital interfaces.

ZSSC4165D-05 provides SENT transmission according to the *SAE J2716 SENT Specification Rev. 3.0 (Jan. 2010)*. Several SENT output modes are available. These modes include assignment of the various sensor signals to the SENT Fast and Serial Data Message (SDM) communication channels as well as the configuration of the SENT frame itself.

Figure 4. Main Signal Path (Example P1/P2/t Sensor)



7.2.1 Full Bridge Sensor Measurement

The ZSSC4165D-05 measures a differential sensor signal (BR1P to BR1N); i.e., a bridge or voltage source type signal. The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal to ($V_{TOP} – V_{BOT}$).

Following parameters are adjustable:

- Gain – from 2.1 to 200
- Range Shift – 1/16, 1/8, 1/4 and ½
- Input Polarity - BR1P/BR1N or BR1N/BR1P

Following properties are fixed (not adjustable):

- Measurement resolution: 14 Bits

7.2.2 Half-Bridge Sensor Measurement

The ZSSC4165D-05 supports the measurement of a half-bridge sensor signal referenced to an internal reference potential of nominal (V_{TOP} - V_{BOT})/2. The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal to (V_{TOP} - V_{BOT}). The signal input pin is selectable between BR2P and BR2N.

Following parameters are adjustable:

- V_{TOP}-V_{BOT} Reference voltage – from 2.09% to 97.91%
- Gain – from 2.1 to 200
- Range Shift – 1/16, 1/8, 1/4 and 1/2
- Input Pin – BR2P or BR2N

Following properties are fixed (not adjustable):

- Measurement resolution: 13 Bits

7.2.3 Internal Temperature Measurement

The ZSSC4165D-05 supports temperature measurement by chip internal PTAT sensor.

Figure 5. Overvoltage and Short Circuit Protection

The ZSSC4165D-05 is designed for a 5V supply provided by an electronic control unit (ECU).

The ZSSC4165D-05 and the connected sensor elements are protected from overvoltage and reverse polarity damage by an internal supply voltage limiter. The SENT output pin DOUT is protected regarding short circuit, over-voltage, and reverse polarity. These functions are described in Table 10 and are valid for operation of the ZSSC4165D-05 in the application circuit shown in section 10 within the specifications of absolute maximum ratings given in section 3.

Note: The specified junction temperature range T_J (Table 2) is in force not only for operation but also for all protection cases listed in Table 10. In the event of an over-voltage, the device might have increased power dissipation. Depending on the sensor elements and the output load, this may lead to a violation of the maximum junction temperature.

Table 10. Overvoltage, Reverse Polarity, and Short Circuit Protection

No.	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Overvoltage and Reverse Polarity Protection							
DS_085	V_{VDDE_OV1}	Maximum voltage at VDDE to VSSE	DOUT is connected to VSSE or VDDE (connection resistance value = 0 to ∞)	0		18	V
DS_086	V_{VDDE_OV2}	Maximum voltage at VDDE to DOUT	VSSE is connected to DOUT or VDDE[a] (connection resistance value = 0 to ∞)	0		18	V
DS_087	V_{DOUT_OV1}	Maximum voltage at DOUT to VSSE	VDDE is connected to DOUT or VSSE (connection resistance value = 0 to ∞)	0		18	V
DS_088	V_{DOUT_OV2}	Maximum voltage at DOUT to VDDE	VSSE is connected to DOUT[a] or VDDE (connection resistance value = 0 to ∞)	0		18	V
DS_089	V_{VSSE_OV1}	Maximum voltage at VSSE to VDDE[a]	DOUT is connected to VSSE or VDDE (connection resistance value = 0 to ∞)	0		18	V
DS_090	V_{VSSE_OV2}	Maximum voltage at VSSE to DOUT[a]	VDDE is connected to DOUT or VSSE (connection resistance value = 0 to ∞)	0		18	V
Short Circuit Protection							
DS_091	$I_{VDDA\_SHRT\_VSSA}$	Current limitation in the event of a VDDA to VSSA short circuit				60	mA
DS_092	$I_{DOUT\_SHRT\_VSSE}$	Current limitation in the event of a DOUT to VSSE short circuit	Output is activated, output current limitation has been adjusted	-10		-2	mA
DS_093	$I_{DOUT\_SHRT\_VDDE}$	Current limitation in the event of a DOUT to VDDE short circuit	Output is activated, output current limitation has been adjusted	2		10	mA

[a] reverse polarity condition

8. Fault-Safe Operation

8.1 Fault-Safe Operation Modes

Fault checks verify the operation of the ZSSC4165D-05 and of the connected sensing elements at power-on and during Normal Operation Mode (NOM). If a fault is detected, the Diagnostic Mode (DM) is activated and the fault status is provided via one of the two methods described below depending on the diagnostic mode.

ZSSC4165D-05 differentiates between two DMs with different behavior:

Static Diagnostic Mode

- Measurement and conditioning cycle are interrupted.
- SENT transmission is stopped, and the output pin DOUT is either driven to a HIGH output level or is switched to high impedance.
- The ZACwire™ interface for one-wire communication (OWI) is enabled; both RAM output pages are readable.
  The command *StrtCmdMd* must be sent to switch to Command Mode for further command processing.
- If enabled, the ZSSC4165D-05 is reset, i.e. the ZSSC4165D-05 is restarted including a reset of all status registers.
- The ZSSC4165D-05 can be restarted by a power-off/power-on sequence.

Temporary Diagnostic Mode

- Measurement and conditioning cycle are continuously processed.
- Fault checks are continuously processed including fault filtering (see below).
- SENT transmission is continued; at least one of following the fault messaging options is activated: the fault code is transmitted in the SENT Fast Channel; fault bit(s) are set in the SENT status nibble; the fault code is transmitted in the SDM Channel (SENT fault messaging and fault codes are configurable).
- The ZACwire™ interface for one-wire communication is enabled. The command *StrtCmdMd* must be sent to switch to Command Mode for further command processing (SENT output must be overwritten by the OWI master).
- The ZSSC4165D-05 returns to Normal Operation Mode including SENT transmission of valid sensor signal if fault checks do not detect continuation of fault conditions.

The **Fault Confirmation** of the ZSSC4165D-05 is defined as follows:

- Fault confirmation is only processed for fault checks assigned to the Temporary DM.
- Fault confirmation is a low-pass filter that delays the activation and deactivation of the Temporary DM.
- In the event of a fault detection, faults are re-checked before entering Temporary DM.
- In the case of Temporary DM, detected fault conditions that no longer exist are re-checked before returning from Temporary DM to NOM.
- Fault confirmation is an up-and-down event counter that allows confirmation of a failure event.

8.2 Fault Messaging

8.2.1 Overview

The SENT interface offers three different options for fault messaging:

- Fault codes in the data channels (the Fast Channels as well as the SDM Channels; e.g., the channel used for temperature)
- Two status bits in the SENT status nibble
- SDM Channel status word

8.2.2 Timing Definitions

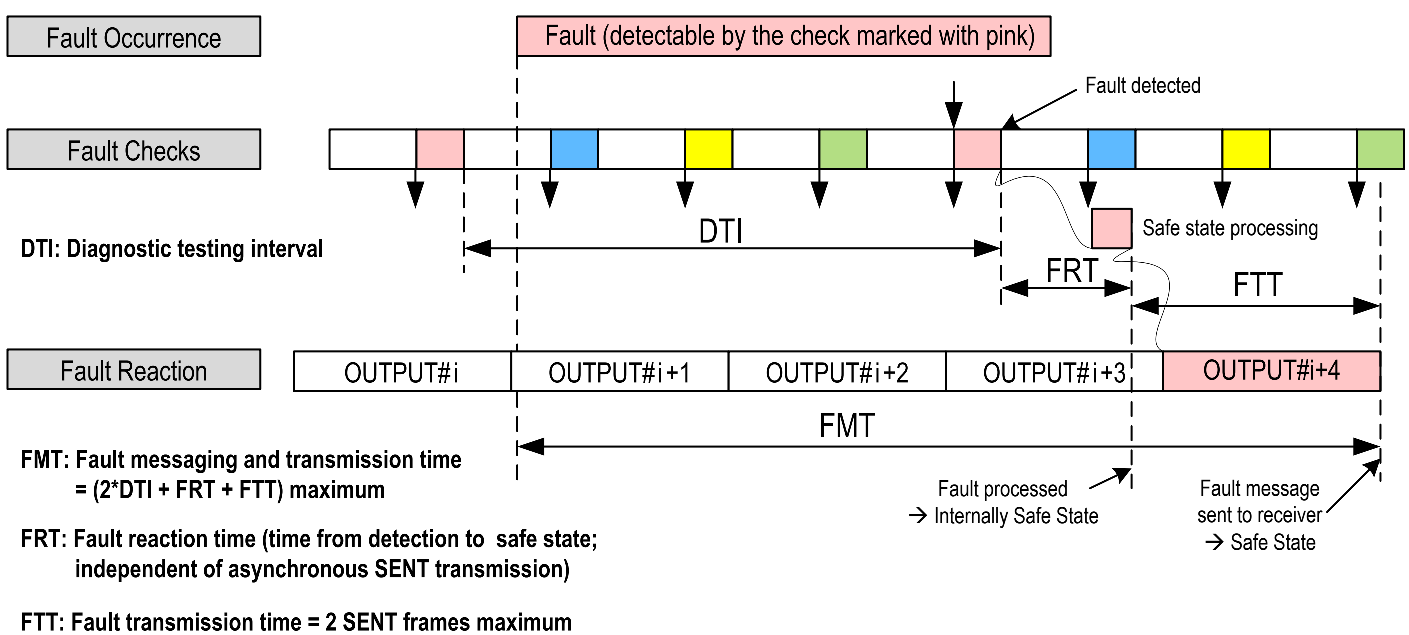
The timing for the fault messaging is defined in Figure 6. The relevant timing parameters are listed in Table 11Table 8.

Table 11. Timing Parameter

Symbol	Parameter	Description
OUR	Output update rate	Update rate of the main signal data
ORT	Output response time	Latency from the main signal event to the completion of the SENT, OWI, or I2C transmission of this signal event
DTI	Diagnostic testing interval	Rate of fault check processing
FMT	Fault messaging time	Latency from the fault event to the completion of the SENT, OWI, or I2C transmission of the fault message

Figure 6. Fault Messaging Timing Diagram

Note: In this figure, the different colors indicate the different fault checks processed in the cycle.



8.2.3 SENT Fast Channel Fault Codes

For the 12-bit SENT Fast Channel, the output value interval [4089, 4095] is reserved for fault codes. This is according to the SENT standard. In addition, the value 0 is used to signal initialization (no valid data available).

In the ZSSC4165D-05, the SENT Fast Channel fault codes are adjustable, and a dedicated fault code must be assigned to every supervised fault. A fault prioritization is available, and in the event of simultaneous detection of multiple faults, the fault code of the highest prioritized fault is transmitted.

8.2.4 SENT Status Bits

According to the SENT standard, the SENT status nibble contains two bits for status information. The assignment of the status bits to the individual detectable faults is configurable.

8.2.5 SENT SDM Channel Status Codes

The SENT standard defines a SMD Channel status word assigned to the SDM identifier #01.

In the ZSSC4165D-05, the SENT SMD Channel status codes are freely programmable, and a dedicated fault code must be assigned to every supervised fault. A fault prioritization is available, and in the event of simultaneous detection of multiple faults, the status code of the highest prioritized fault is transmitted.

9. Fault Checks

9.1 Overview

The ZSSC41650500_05 implements a diagnostic mechanism architecture that can support end-user applications up to ASIL B requirements in regard to random failure diagnostic capabilities. Table 12 lists the available fault checks.

Table 12. Fault Checks Overview

Note: See important notes at the end of this table.

No.	Identifier	Fault Check
4165_0500_05 Self-Supervision Fault Checks		
DS_094	VDDAPOR	Analog supply voltage V_{VDDA} under-voltage check; power-on reset (POR)
DS_095	VDDDBOD	Digital supply under-voltage check; brownout detection (BOD)
DS_096	OSCFAIL	Oscillator-fail check based on a second oscillator/timer; reset after oscillator restart
DS_097	ROMCRC	ROM content CRC check
DS_098	NVMCRC	NVM content CRC check
DS_099	RAMCRC	RAM content CRC check
DS_100	RAMPRTY	RAM content parity check
DS_101	WWDG	Windowed watchdog; microcontroller and measurement and conditioning cycle active check
DS_102	INITCRC	Measurement and conditioning initialization check; processing, order, and configuration
DS_103	MCYCCRC	Measurement cycle operation check; processing, order, and configuration
	AFEMUX	AFE input multiplexer operation check
	REGCRC	Configuration register content CRC check
DS_104	CCYCCRC	Conditioning cycle operation check; processing, order, and configuration
DS_105	SENTDATA	SENT data consistency check
DS_106	SENTPHY [a]	SENT transmission monitoring
DS_107	CHIPP	Chipping check
DS_108	COMP	Computational check; microcontroller conditioning calculation, code processing, and peripheral bus access check
DS_109	VDDDRNG	Digital supply voltage range check; digital core and memory supply
DS_110	ADCOFFSRNG	ADC offset range check; ADC operation check
DS_111	AFEGAIN	AFE gain check
DS_112	VDDARNG	Analog supply voltage V_{VDDA} range check; front-end and sensor supply

No.	Identifier	Fault Check
Sensing Element Fault Checks		
DS_113	BRSC	Bridge sensor connection check
DS_114	BRSS	Bridge sensor short check
DS_115	BRSCMRNG	Bridge sensor common mode range check and sensor input leakage check
DS_116	TSI	Internal temperature sensor operation check
Environment and Operating Condition Fault Checks		
DS_118	BRSRNGH	Bridge sensor conditioning result range check: upper limit
DS_119	BRSRNGL	Bridge sensor conditioning result range check: lower limit
Informational [b]	HBRSRNG	Half-bridge sensor range check
DS_120	TSIRNG	Internal temperature sensor range check (over-temperature/under-temperature)
DS_122	VDDEUV	Supply voltage V_{VDDE} under-voltage check
DS_123	VDDEOV	Supply voltage V_{VDDE} over-voltage check
DS_124	CSAT	Conditioning calculation saturation check

[a] SENTPHY is not applicable for SENT tick times less than 3µs.

[b] HBRSRNG is available for SENT Fast Channel P2 transmission of the half-bridge sensor signal.

9.2 Fault Checks for ZSSC4165D-05 Self-Supervision

The ZSSC4165D-05 provides several fault checks which supervise the ZSSC4165D-05 hardware itself.

Table 13. ZSSC4165D-05 Hardware Fault Checks

Note: See important notes at the end of this table.

Requirement	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [a]
DS_094	V_{VDDA} under-voltage check (VDDAPOR); power-on reset	< 200µs	–	Always on	Static	1
DS_095	Digital supply under-voltage check (VDDDBOD); brownout detection	< 200µs	–	Always on	Static	1
DS_096	Oscillator fail check (OSCFAIL)	< 200µs	–	Always on	Static	1
DS_097	ROM CRC check (ROMCRC)	< FMT	–	Always on	Static	1
DS_098	NVM CRC check (NVMCRC)	$t_{STARTUP}$	Page-wise 16-bit CRC	Always on	Static	1
DS_099	RAM CRC check (RAMCRC)	< FMT	Page-wise 16-bit CRC	Always on	Static	1
DS_100	RAM parity check (RAMPRTY)	< FMT	–	Always on	Static	1
DS_101	Windowed watchdog (WWDG)	< 2 × OUR	–	Always on	Static	1

Requirement	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [a]
DS_102	Initialization phase check (INITCRC)	$t_{STARTUP}$	16-bit CRC	Enable/ Disable	Static	1
DS_103	Measurement cycle check (MCYCCRC) including ▪ AFE input multiplexer check (AFEMUX) ▪ Register data check (REGCRC)	< FMT	16-bit CRC	Enable/ Disable	Static	1
DS_104	Conditioning cycle check (CCYCCRC)	< FMT	16-bit CRC	Enable/ Disable	Static	1
DS_105	SENT data consistency check (SENTDATA)	t_{FRAME}	–	Enable/ Disable	Static	1

[a] "Enable/Disable" indicates that the user can enable or disable the check.

[b] Prioritization describes the default fault messaging order ("1" means highest priority).

Table 14. 4165_0500_05 Operation and Cycle Fault Checks

Requirement	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [a]
DS_106	SENT transmission monitoring (SENTPHY)	< FMT	–	Enable/ Disable	Temporary	2
DS_107	Chipping check (CHIPP)	< FMT	–	Enable/ Disable	Temporary	2
DS_108	Computational check (COMP) including microcontroller arithmetic, code processing, and bus access	< FMT	–	Enable/ Disable	Temporary	2
DS_109	Digital supply voltage check (VDDDRNG)	< FMT	Lower limit	Enable/ Disable	Temporary	4
DS_110	ADC offset check (ADCOFFSRNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	3
DS_111	AFE gain check (AFEGAIN)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	5
DS_112	Analog supply voltage check (VDDARNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	15
DS_171	Bridge measurement raw data check (H/BRSRAW)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	

[a] "Enable/Disable" indicates that the user can enable or disable the check.

[b] Prioritization describes the default fault messaging order ("1" means highest priority).

9.3 Fault Checks for Sensing Element Supervision

The4165_0500_05 provides several fault checks that supervise the sensing elements.

Table 15. Sensing Element Fault Checks

Requirement	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [a]
DS_113	Full - Bridge sensor connection check (BRSC)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	7
DS_128	Half - Bridge sensor connection check (HBRSC)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	6
DS_114	Bridge sensor short check (BRSS)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	8
DS_115	Bridge sensor common mode range check (BRSCMRNG) including sensor input leakage check	< FMT	Lower/upper limit	Enable/ Disable	Temporary	9
DS_116	Internal temperature sensor operation check (TSI)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	10

[a] "Enable/Disable" indicates that the user can enable or disable the check.

[b] Prioritization describes the default fault messaging order ("1" means highest priority).

9.4 Fault Checks for Environment and Operating Condition Supervision

The 4165_0500_05 provides several fault checks that supervise the environment and operating conditions.

Table 16. Environment and Operating Condition Fault Checks

Requirement	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [a]
DS_118	Bridge sensor range check upper limit (BRSRNGH)	< FMT	Upper limit	Enable/ Disable	Temporary	13
DS_119	Bridge sensor range check lower limit (BRSRNGL)	< FMT	Lower limit	Enable/ Disable	Temporary	13
DS_129	Half-Bridge sensor range check (HBRSRNGH)	< FMT	Upper limit	Enable/ Disable	Temporary	12
DS_130	Half-Bridge sensor range check (HBRSRNGL)	< FMT	Lower limit	Enable/ Disable	Temporary	12
DS_120	Internal temperature sensor range check (TSIRNG)	< FMT	Lower/upper limit	Enable/ Disable	Temporary	10
DS_122	Supply V_{VDDE} under-voltage check (VDDEUV)	< FMT	Lower limit	Enable/ Disable	Temporary	15

Requirement	Fault Check	Messaging Time	Adjustable	Active [a]	DM Type	Priority [a]
DS_123	Supply V_{VDDE} overvoltage check (VDDEOV)	< FMT	Upper limit	Enable/ Disable	Temporary	14
DS_124	Saturation check for all signal conditioning except Half-Bridge signal and on-chip temperature signal (CSAT)	< 22 ms	-	Enable/ Disable	Temporary	16
DS_125	Saturation check for on-chip temperature signal conditioning (CSAT)	< FMT	-	Enable/ Disable	Temporary	10
DS_126	Saturation check for common mode signal conditioning (CSAT)	< 22 ms	-	Enable/ Disable	Temporary	9
DS_127	Saturation check for half-bridge signal conditioning only (CSAT)	< 22 ms	-	Enable/ Disable	Temporary	6

[a] "Enable/Disable" indicates that the user can enable or disable the check.

[b] Prioritization describes the default fault messaging order ("1" means highest priority).

Table 17. SENT Transmission Fault Checks

Note: SENT transmission fault checks must be implemented on the SENT receiver.

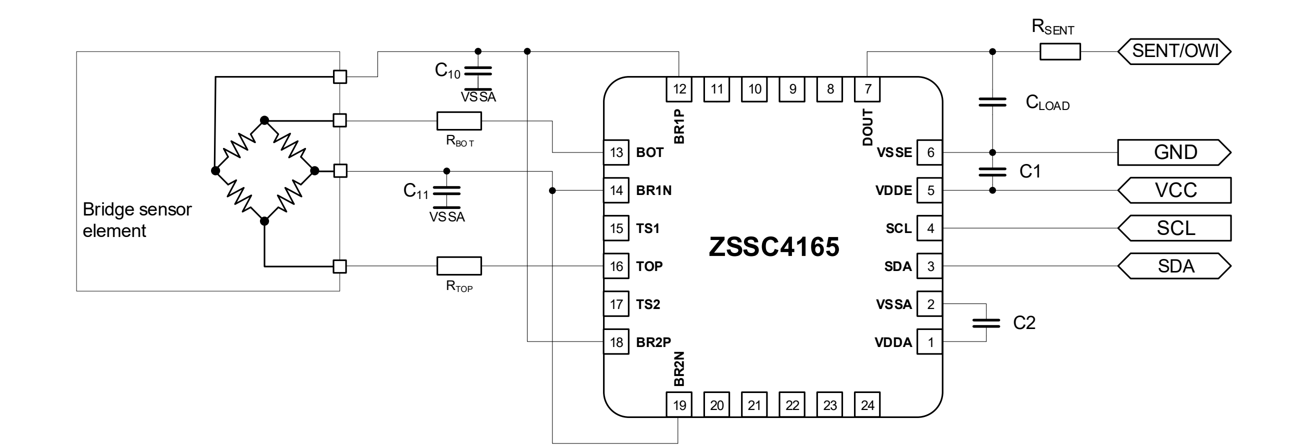
Fault Check	Messaging Time	Adjustable	Notes	Priority [a]
SENT CRC (SENTCRC)	t_{FRAME}	n.a.	SENT-receiver	n.a.
SENT tick time (SENTTICK)	t_{FRAME}	n.a.	SENT-receiver	n.a.
SENT timeout (SENTIMEOUT)	t_{FRAME}	n.a.	SENT-receiver	n.a.
SENT sync time (SENTSYNC)	t_{FRAME}	n.a.	SENT-receiver	n.a.
SENT idle state (SENTIDLE)	t_{FRAME}	n.a.	SENT-receiver	n.a.

[a] Prioritization describes the default fault messaging order ("1" means highest priority).

10. Application Circuit and External Components

Figure 7. Application Circuit Example with combined full / half bridge with half bridge on input channel 2

DP_043



Note: The pin BR1P must be connected to pin BR2P or BR2N. The pin BR1N must be connected to pin BR2N or BR2P.

Table 18. Dimensioning of External Components for the Application Example

DP_044	Component	Symbol	Conditions	Min	Typical	Max	Unit
	Capacitor	C1 [a]	$V_{MAX} \geq 32V$, SMD MLCC type		100 ± 20%	tbd	nF
	Capacitor	C2 [a]	$V_{MAX} \geq 10V$, SMD MLCC type		100 ± 20%	470 + 20%	nF
	Capacitor	C_{LOAD}	$V_{MAX} \geq 32V$, SMD MLCC type		2.2 ± 20%	tbd	nF
	Resistor	R_{SENT}				47+5%	Ω
	Capacitor	C_{10}, C_{11}	$V_{MAX} \geq 10V$, SMD MLCC type			1.2	nF
	Resistor	R_{TOP}, R_{BOT}	Resistance of R_{TOP} must be equal to R_{BOT}	0	0	$\frac{10k - R_{BR}}{2}$	Ω

[a] Device is mandatory for meeting Electrical Characteristics described in section 5.

Note: The component values are examples and must be adapted to the requirements of the application, in particular to the EMC requirements.

11. ESD Protection and EMC Specification

11.1 ESD Protection

All pins have an ESD protection of <=2000V according to the Human Body Model (HBM with 1.5kOhm/100pF, based on MIL883, Method 3015.7). The VDDE, VSSE and DOUT pins have an additional ESD protection of <=4000V (HBM with 1.5kOhm/100pF, based on MIL883, Method 3015.7).

The levels of ESD protection are tested with devices in a 4 × 4 mm 24-QFN package during the product qualification.

11.2 Electromagnetic Emission

The wired emission of the externally connected pins of the ZSSC4165D-05 is measured according to the following standard: *IEC 61967_4:2002 + A1:2006.*

Measurements must be performed with the application circuit described in Figure 7; SENT transmission uses a tick time of 9µs.

For the off-board pins, the spectral power measured with the 150Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN*. For the VSSE pin, the spectral power measured with the 1Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN.*

11.3 Conducted Susceptibility (DPI)

The conducted susceptibility of externally connected pins of the device is measured according to the IEC 62132-4 standard:

Measurements must be performed with the application circuit described in Figure 7; the sensor bridge element is replaced by a 3-resistor string connected to TOP, BR1P, BR1N, and BOT; SENT transmission uses a tick time of 9µs.

Table 19 gives the specifications for the DPI tests. RES refers to the coupling impedance. CAP refers to the injection capacitance.

Table 19. Conducted Susceptibility (DPI) Tests

No.	Test	Frequency Range	Power [dBm]	Load Pins	Protocol	Error Band [a]	Comment
DS_169	DPI, direct coupled	1MHz to 10MHz	20dBm	VDDE, DOUT	SENT	±1%	RES = 50Ω CAP= 4.7nF
DS_170	DPI, direct coupled	>10MHz	30dBm	VDDE, DOUT	SENT	±1%	RES = 50Ω CAP = 4.7nF

[a] Error band regarding main signal (SENT FC1).

12. Reliability and RoHS Conformity

The ZSSC4165D-05 is qualified according to the AEC-Q100 standard, operating temperature grade 0. A fit rate < 5 FIT (junction temperature = 55°C, confidence level = 60%, activation energy = 0.7eV) is estimated.

A typical fit rate for TSMC's CV018BCD technology, which is used for the ZSSC4165D-05, is < 1 FIT (temperature = 55°C, confidence level = 60%, activation energy = 0.7eV).

The reliability calculation is based on an average operating junction temperature of 90.5°C over an operating lifetime of 15000 hours, in normal operating conditions, and according to the ambient temperature profile listed in Table 20.

Table 20. Ambient Temperature Profile (Example)

	Operating Ambient Temperature [°C]	Relative Time [%] Based on a 15000h Operating Lifetime	Absolute Time [h]
DP_041	-40	2	300
	-20	8	1200
	0	15	2250
	25	25	3750
	55	25	3750
	85	17	2550
	125	6	900
	150	2	300

- Overvoltage Conditions (18V):

  Maximum power dissipation is $P_{max,OV}$ = 300mW, output is switched off.

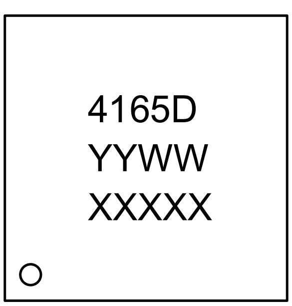
  Temperature difference: $T_J - T_{AMB}$ = 32K/W × 300mW = 9.6K→ With these conditions, the maximum junction temperature T_J is ~10K greater than the ambient temperature T_{AMB}.

The ZSSC4165D-05 complies with the RoHS directive and does not contain hazardous substances. The complete RoHS declaration update can be downloaded at https://www.renesas.com/eu/en/about/corporate-responsibility-citizenship.

13. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

14. Marking Diagram



1. "4165" is the truncated part number.
2. "YYWW" is the last digits of the year and week that the part was assembled.
3. "XXXXX" is the last digits of the lot number.

15. Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front-End
ASIL	Automotive Safety Integrity Level
BOD	Brownout Detection
BR	Bridge Sensor
CM	Command Mode
CMC	Calibration Microcontroller; optimized microcontroller architecture for Renesas signal conditioners
CMV	Common Mode Voltage
DM	Diagnostic Mode
DNL	Differential Nonlinearity
ECU	Electronic Control Unit
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FC	Fast Channel; transmitted in SENT frame
FMT	Fault Messaging Time
FS	Full Scale
HBM	Human Body Model
I/O	Input/Output
I²C	Inter-Integrated Circuit; serial two-wire data bus
INL	Integral Nonlinearity
LSB	Least Significant Bit
LSN	Least Significant Nibble
MSB	Most Significant Bit
MSN	Most Significant Nibble
MUX	Multiplexer
MTP	Multiple-Time Programmable
n.a.	Not Applicable
NOM	Normal Operation Mode
NVM	Nonvolatile memory
OTP	One-Time Programmable

Term	Description
OWI	One-Wire Interface
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
POR	Power-On Reset
PTAT	Proportional to Absolute Temperature
PWR	Power Management and Protection Unit
QFN	Quad-Flat No-Leads – ZSSC4165D-05 package
RAM	Volatile Memory for Configuration and Conditioning Coefficients
RISC	Reduced Instruction Set Computing
ROM	Read-Only Memory
RTD	Resistance Temperature Device
SCCM	Sensor Check and Common Mode Adjustment Unit
SDM	Serial Data Message; transmitted in the slow channel of SENT protocol
SENT	Single Edge Nibble Transmission; communication protocol for automotive applications defined by SAE International.
SSC	Sensor Short Check—diagnostic task or Sensor Signal Conditioner
TSI	Internal Temperature Sensor
TQE	Extended Temperature Range Identifier
ZACwire™	Renesas specific one-wire interface

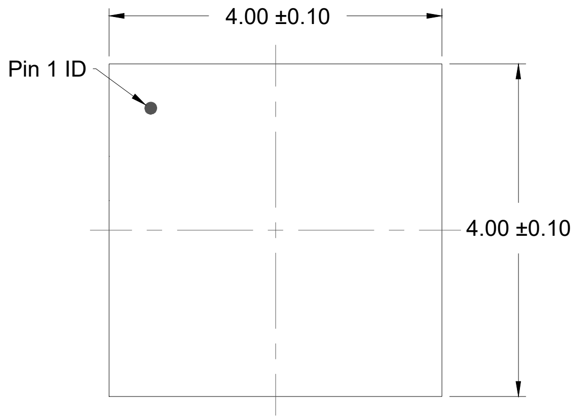
16. Ordering Information

Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
ZSSC4165DE4R	Single bridge input, SENT output, internal and/or external temperature measurement, 4 × 4 mm 24-QFN, wettable flanks (NLG24P5)	MSL1	13” Reel	-40°C to 150°C
ZSSC4165DE4W	Single bridge input, SENT output, internal and/or external temperature measurement, 4 × 4 mm 24-QFN, wettable flanks (NLG24P5)	MSL1	7” Reel	-40°C to 150°C
ZSSC4160EVKV1P5	ZSSC4160D SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, 10 Samples.			

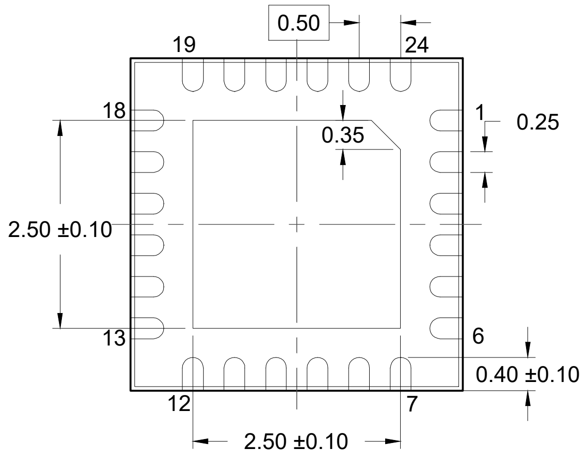
Contact Renesas for additional options.

17. Revision History

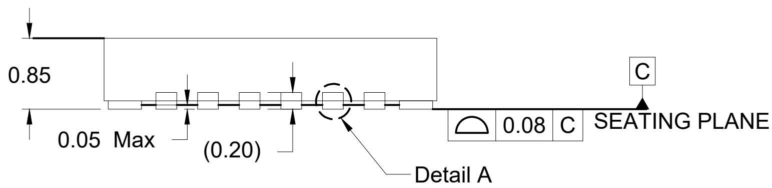
Revision Date	Description of Change
Apr 23, 2026	• Updated QFN-20L package recommendation (see “Pin Assignments”) • Split programming time into 2x parameters (see “Nonvolatile Memory”: DS_068) • Updated the package outline drawings; however, no technical changes were made (see links in “Ordering Information”) • Completed other minor changes
January 21, 2025	DS_065: decreased the max limit to 125 DS_066: Parameter changed
May 3, 2021	DS_092 and DS_093 corrected (from 5-15mA to 2-10mA) Adding Footnote on DP_038 Ordering Codes corrected (revision D added) Rebranding to Renesas template
April 18, 2018	“Preliminary” state removed
March 6, 2018	Update of parameter descriptions
February 9, 2018	Change DP_038
January 22, 2018	Add Requirement IDs
December 22, 2017	Initial draft version of datasheet created



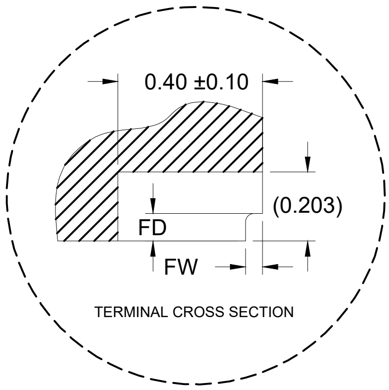
TOP VIEW



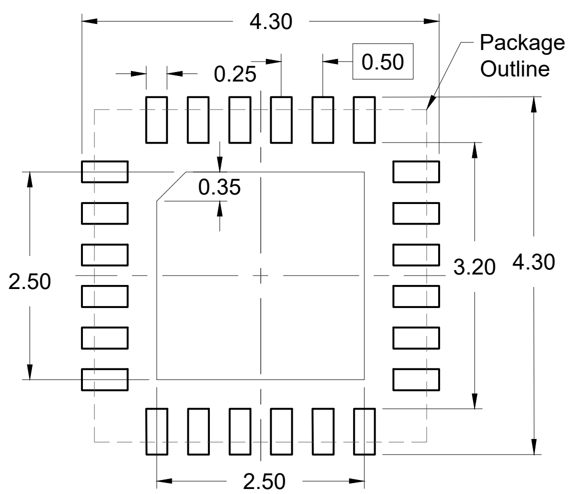
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

Table 1: Dimensions of wettable flank (DETAIL A)

Symbol	Unit (mm)	
	MIN	MAX
FD	0.100	-
FW	0.010	0.075

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Wettable flank (step cut).

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