RC4640/RC4650 Device Errata

Notes

Supplemental Information

This Device Errata affects all revisions of RC4640/RC4650 silicon

Revision History

July 7 1999: First version of errata for RC4640/RC4650

Descriptions and Workarounds

Item #1 - NMI behaviour

Issue: If a non-maskable interrupt (NMI*) occurs while the CPU is processing an exception, the NMI detection logic will fail if the pipeline cancelling logic and the NMI edge detection logic occur in the same Pipeline Clock (internal clock) cycle. The NMI IS NOT recognized again until it is de-asserted and then re-asserted to form the edge.

Workaround: Use the following sequence to assert NMI*

1. Assert NMI* for one system clock cycle
2. Deassert NMI* for one system clock cycle
3. Assert NMI*

The double assertion of the NMI* signal will result in only one NMI cycle. If the CPU recognizes the first NMI* assertion, the deassertion and re-assertion of the signal will be transparent to the CPU. If the 1st assertion of NMI* is not recognized due to the presence of an exception as described above, the 2nd assertion of the signal will be recognized.

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