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# RENESAS TECHNICAL UPDATE

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| Product Category | IIBU/ClockMatrix | | Document No. | | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | 8A3xxxx Firmware Version v4.8.8 - Errata Notice | | Information Category | Technical Notification | | |
| Applicable Product | 8A3xxxx, ClockMatrix | Lot No. | Reference Document | | | |

Devices Affected

8A3xxxx devices running firmware version 4.8.8 loaded from internal ROM, or loaded into RAM from an EEPROM or by a host processor. Consult Renesas for information about later firmware versions that may eliminate these issues.

## Issue BRMBXR-3256 Description

A DPLL configured as a GPIO_Slave will use hitless reference switching when it is triggered by GPIO to switch from Master to Slave. This behavior can cause a phase difference between the output of the master and the slave timing devices.

### Work-Around

There are two options:

1. After a DPLL is triggered to switch from Master mode to Slave mode by a GPIO, use the DPLL_HS_TIE_RESET control bit to reset the hitless switching time interval error and align the DPLL output with its input reference.

2. Change from Master mode to Slave mode using the DPLL_REF_MODE control register.

## Issue BRMBXR-3301 Description

PWM receivers configured for an external channel cannot receive all 128 bytes of payload if the carrier frequency is lower than 50kHz.

### Work-Around

Ensure the carrier frequency is ≥ 50kHz.

## Issue BRMBXR-3302 Description

If the OTP or EEPROM configuration has OUT_SYNC_DISABLE bit set to “1” then the output clock might not become active for a random interval of up to 8 seconds after power on reset. This issue does not happen after a warm reset.

### Work-Around

Set the OUT_SYNC_DISABLE bit to “0” in OTP and EEPROM configurations.

## Issue BRMBXR-3308 Description

DPLL_0 will not switch from disabled mode to write phase mode using the PLL_MODE bit field unless DPLL_0 is reset after changing the setting of the PLL_MODE bit field.

### Work-Around

There is no work-around for this issue.

## Issue BRMBXR-3403 Description

The fine phase measurement algorithm may affect the decimator value of the DPLL when the FILTER_STATUS_UPDATE_EN bit is set.

### Work-Around

There is no work-around for this issue.

## Issue BRMBXR-3416 Description

When a channel is in Phase Measurement mode and the frequency of the channel FOD is set to zero Hz; if a new reference input is selected, valid phase measurement data will not be available for 10s.

### Work-Around

There is no work-around for this issue.

## Issue BRMBXR-3427 Description

For every DPLL except the System DPLL:

If:

- The host makes any of the four configuration changes listed below to a DPLL.
- And, an already qualified reference has been selected for the DPLL.

Then:

- There is a chance that the DPLL feedback divider will not be properly aligned with the DPLL master divider. This situation will cause a constant phase offset between the DPLL input reference and the DPLL output clocks. The constant phase offset can exceed the Input - Output Alignment Variation ($t_{ALIGN}$) datasheet limits.

The following are the applicable DPLL configuration changes:

1. DPLL_n.DPLL_MODE (trigger register) is written, after either of the following changes:
    a. GLOBAL_SYNC_EN is changed from 0 to 1.
    b. Source of the feedback clock for the DPLL is changed.
2. DPLL_CTRL_n.DPLL_FOD_FREQ register is written.
3. DPLL_CTRL_n.DPLL_MASTER_DIV register is written.
4. DPLL_CTRL_n.DPLL_DCD_FILTER_CNFG is register is written.

This issue will not occur if the DPLL configuration changes are due to configurations loaded from EEPROM or OTP.

### Work-Around

After the host executes one of the four configuration changes listed above, the host should:

1. Wait at least 10ms.
2. Trigger the input module for the currently selected reference by writing to INPUT_n.IN_MODE.

This work-around will cause the DPLL to properly align the feedback divider and the master divider and the DPLL will meet the Input - Output Alignment Variation ($t_{ALIGN}$) datasheet limits.

## Issue BRMBXR-3431 Description

If two consecutive DPLL restart events occur within 1ms then subsequent reference switching instructions may not be accepted by the DPLL state machine.

### Work-Around

Ensure consecutive DPLL restart events do not occur within less than 1ms.

## Issue BRMBXR-3523 Description

Satellite channels do not align properly when they are in phase measurement mode.

### Work-Around

There is no work-around for this issue.

## Issue BRMBXR-3235 Description

The outputs of a channel in phase measurement mode are affected when new inputs are selected for phase measurement.

### Work-Around

There is no work-around for this issue.

## Issue BRMBXR-3553 Description

When a channel is configured as a “satellite channel”, it is controlled by an internal automatic alignment algorithm that maintains alignment between the satellite channel and its source channel. On rare occasions, the automatic alignment algorithm can apply an unintended and small FFO to a satellite channel for up to 35 minutes.

### Work-Around

There is no work-around for this issue.

## Issue BRMBXR-3555 Description

When a DISQUAL_TIMER bit field is set to 1.25ms the reference monitor may generate false alarms.

### Work-Around

Ensure the DISQUAL_TIMER bit fields are not set to 1.25ms.

## Issue BRMBXR-3599 Description

For coarse phase measurement mode, the phase measurement values are provided to the user in both the DPLLx_FILTER_STATUS field and the DPLLx_PHASE_STATUS field.

### Work-Around

There is no work-around for this issue.

## Issue BRMBXR-3636 Description

The DPLL phase pull-in procedure does not pull-in the phase offset when DPLL_PHASE_PULL_IN_OFFSET is 1ns and the DPLL_PHASE_PULL_IN_SLOPE_LIMIT is 1ppb.

### Work-Around

There is no work-around for this issue.

## Issue BRMBXR-3644 Description

When tod_frame_access_en = 1, if TOD frames are not discarded by the user, then over the course of many hours, TOD frames can accumulate in the receive FIFO.

### Work-Around

There is no work-around for this issue.

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