PowerPro Device Errata

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1. PowerPro Device Errata and Design Notes

This document describes all the errata of the PowerPro (CA91L750-100IL) device. It also details design notes for the PowerPro device.

1.1 Errata Listing

Table 1 provides a summary list of the PowerPro device errata.

Table 1: Summary of Device Errata.

Errata	Description
1	"Incorrect SDRAM Burst Accesses When BMGT is Set in the SD_Bx_CTRL Registers" on page 3
2	"Incorrect Configuration Master Cycles During HRESET Assertion" This errata is no longer applicable for the PowerPro production device.
3	"Incorrect PB_OFFSET During HRESET" on page 4
4	"PowerPro Incompatibility During Snooped Transactions" on page 4
5	"Incorrect Negation of PB_ARTRY" on page 4
6	"Incorrect Interleaving of SDRAM and FLASH/ROM Accesses" on page 5
7	"Incorrect Latching of Power-up Options During HRESET_" on page 6

1.1.1 Errata Descriptions

The following sections describe the PowerPro device errata.

1.1.1.1 Incorrect SDRAM Burst Accesses When BMGT is Set in the SD_Bx_CTRL Registers

When BMGT is turned on in the PowerPro (changed from the reset value of zero to one) and a burst read or write is issued, the PowerPro will assert an auto precharge (which closes the row) command on each of the four beats of the burst. The PowerPro should only issue an auto precharge command on the last beat of the burst. The first beat of the burst will complete but all the other subsequent beats will be incorrect. The wrong data will be read back and/or data will be written to the wrong location.

Work around

This issue occurs when bank management is enabled. Ensure that the BMGT field in the SD_Bx_CTL registers is set to zero.

1.1.1.2 Incorrect PB_OFFSET During HRESET

During Power-on reset, if the PowerPro is configured as a PowerPC configuration master, it will configure its register base address (PB_REG_ADDR) to a user defined location. On any subsequent assertion of HRESET_, the base address of the PowerPro will be reset to its default address.

The configuration master cycle will fail to reload the user defined register base address value into the PB_REG_ADDR register. The PowerPro will no longer respond to register accesses to its previously set base address.

Work around

The base address of the PowerPro's PB_REG_ADDR must remain its default value to avoid this issue.

1.1.1.3 PowerPro Incompatibility During Snooped Transactions

The following description is applicable to an application with multiple PowerPC processors which share a global region of memory that is controlled by the PowerPro device.

Description

A PowerPC processor performs a global burst write (GBL pin is asserted) access to a memory region residing behind the PowerPro memory controller. During a third party PB_ARTRY_ assertion, the PowerPro asserts TA for one clock cycle and keeps it asserted a second clock cycle after PB_ARTRY_ negation. This second TA assertion without an associated data phase causes PowerPC bus activity to cease.

Work around

Disable snooping (GBL assertion) for the memory regions controlled by the PowerPro memory controller. System designers must ensure memory coherency is maintained through software control.

1.1.1.4 Incorrect Negation of PB_ARTRY

Description

When Processor Bus Address Retry (PB_ARTRY) is enabled in PowerPro and PowerPro asserts the PB_ARTRY_ signal during a 60x transaction, PowerPro does not drive the PB_ARTRY_ signal to its inactive state. The PowerPro relies on external pull-up circuitry to bring this signal to its inactive state.

This design requirement is a violation of the 60x specification. The specification states that the PB_ARTRY_ signal must negate by going to high impedance for a minimum of one-half processor cycle then be driven negated for one bus cycle before returning to high impedance.

Work around

External logic must be implemented on the PB_ARTRY_ signal of the PowerPro device when PB_ARTRY is enabled to meet 60x bus specification requirements.

1.1.1.5 Incorrect Interleaving of SDRAM and FLASH/ROM Accesses

Description

When SDRAM and FLASH/ROM devices share the PowerPro's SDRAM address bus and if a FLASH/ROM access occurs less than one clock after an SDRAM initialization, the FLASH/ROM and SDRAM accesses will simultaneously attempt to use the SDRAM address bus and the FLASH/ROM access will return incorrect data.

Hardware work around

When designing an application using PowerPro ensure that FLASH/ROM devices do not share the PowerPro's SDRAM address bus. If the hardware work around is not used, then the software work around must be enabled.

Software work around

When enabling the SDRAM interface, with the SDRAM Enable bit in the SDRAM Timing register (see the *PowerPro User Manual* for more register information), encapsulate the register access with the “sync” and “isync” commands from the processor (if available). These commands make sure that only one instruction is completed at a time by the processor.

1.1.1.6 Incorrect Latching of Power-up Options During HRESET_

Description

Whenever HRESET_ is asserted, and PB_A[7] is low, and PowerPro is configured as the configuration master, PowerPro latches its power-up options from PB_D[0:31]. This enables PowerPro to operate as either a configuration master or a configuration slave in systems that require this functionality.

However, there is a potential issue with PowerPro latching power-up options in this manner. Because some 60x masters do not tri-state their PB_A bus on the same clock cycle as the assertion of HRESET_, if PB_A[7] is driven low at the same time the HRESET_ signal is asserted, and PB_A[7] persists as a low signal, PowerPro will latch in its power-up options from PB_D[0:31]. When this occurs, PowerPro latches in the values that are present on PB_D[0:31] at the time that PB_A[7] is low. This causes incorrect values to be loaded into the power-up option registers.

Hardware work around

When designing an application using PowerPro, ensure when the HRESET_ signal is low the PB_A[7] signal is high.

Work around

When using PowerPro in configuration master mode, make sure that PORESET_ is generated if HRESET_ is generated. The minimum pulse requirement for PORESET_ is five PB clock cycles. In configuration slave mode, HRESET_ must be tied high and PORESET_ must only be used as the reset input.

1.2 Design Note Descriptions

The following section describes the PowerPro design notes. These notes are created to help design systems using PowerPro.

1.2.1 Specific Behavior of EE_DATA[0:7] When Used as Interrupts

Description

PowerPro toggles the EE_DATA[0:7] lines when an access to one of its FLASH/ROM banks occur. If the PowerPro's EE_DATA[0:7] lines are used as interrupt inputs, and FLASH/ROM accesses occur, these lines incorrectly toggle and cause spurious and incorrect interrupt flags to be set within the PowerPro's interrupt status registers.

Work around

The GPIO enable register, which controls the EE_DATA line's GPIO functionality, must be enabled and the signal direction set so that the EE_DATA lines are inputs. The interrupt enable, control, and polarity registers must be programmed as well for proper GPIO operation (see the *PowerPro User Manual* for register programming information).

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