SLG46620-EV Errata Note

Abstract

This document contains the known errata for SLG46620-EV and the recommended workarounds.

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Package(s)	20-pin STQFN: 2 mm x 3 mm x 0.55 mm, 0.4 mm pitch

2. Errata Summary

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3. Errata Details

3.1 ACMP IN- Leakage Current when Powered Down

3.1.1. Effect

ACMPs

3.1.2. Technical Description

There is a leakage current from the EXT Vref pin when ACMP uses EXT Vref and the ACMP is powered down.

3.1.3. Workaround

Currently there is no workaround. The only alternative is to turn off the IN- external Vref source.

3.2 ACMP Output Glitch due to Ring OSC Operation

3.2.1. Effect

W/S Control, ACMP

3.2.2. Technical Description

The output of the ACMP incorrectly goes low even when IN+ is greater than IN- if the RING OSC is active when the WS signal rises.

Channel 1 – ACMP out

Channel 2 – WS_OUT

3.2.3. Workaround

Avoid using the RING OSC with the WS Controller, or add a filtering block on the ACMP output to filter out the glitch.

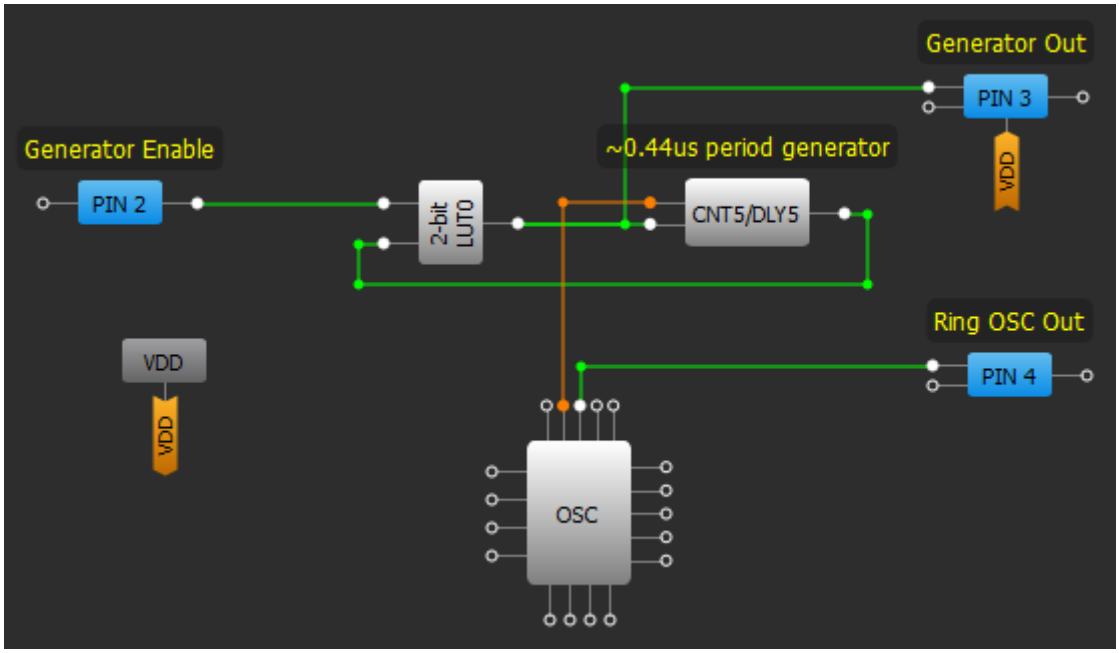
3.3 Long Ring OSC Settling Time

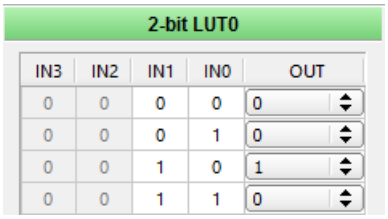
3.3.1. Effect

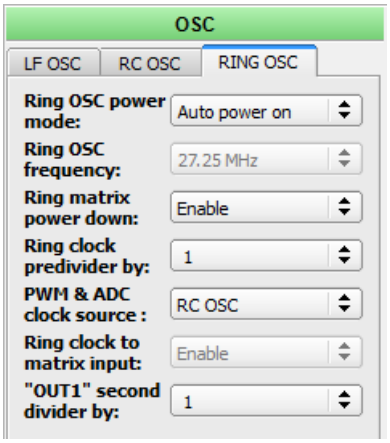
Ring OSC, Delay, Counter

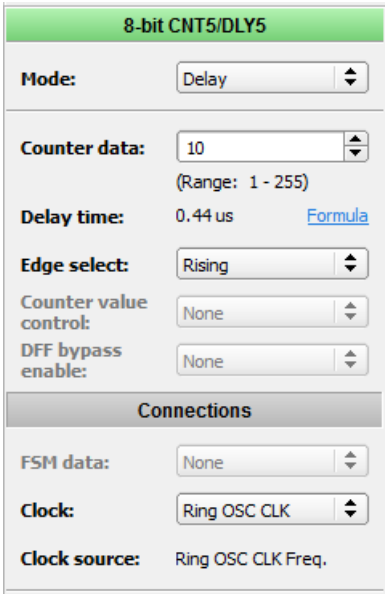
3.3.2. Technical Description

The Ring OSC has a longer settling time when configured as Auto Power On in the designs that have very short Ring OSC disable time. An example of this issue is shown in the following configuration:

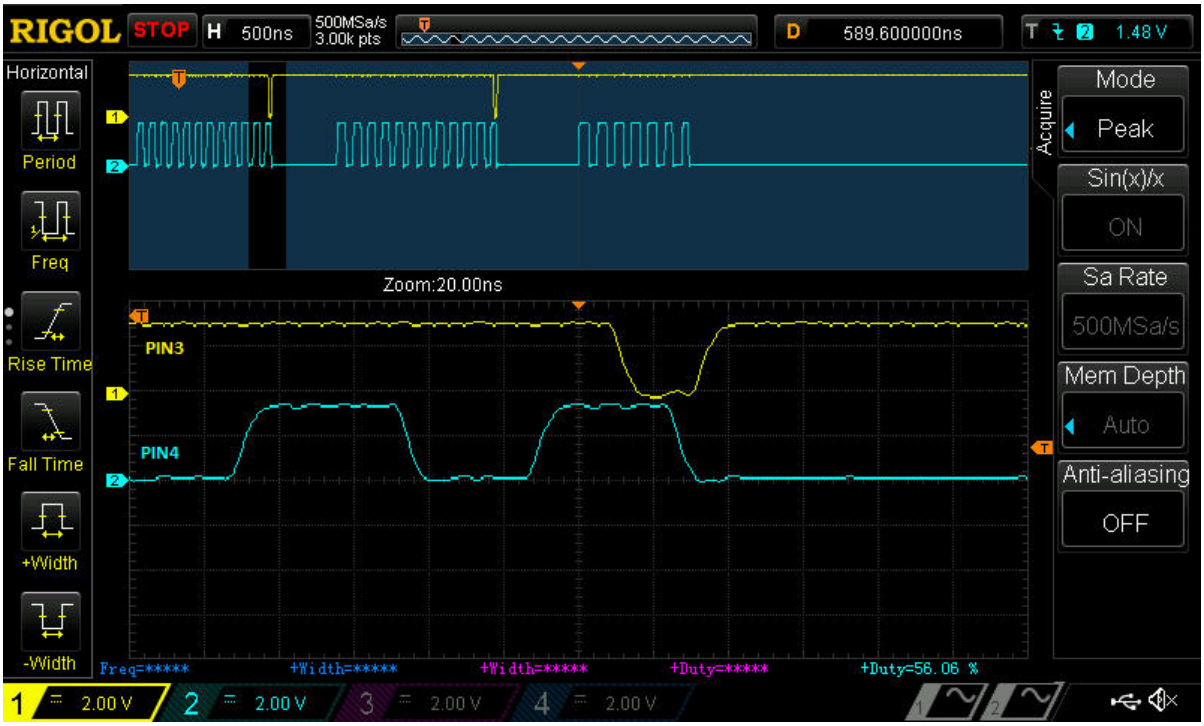








The configuration shown above generates a periodical signal with a frequency defined by the Delay cell and started by a high signal on PIN2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). See waveform below.

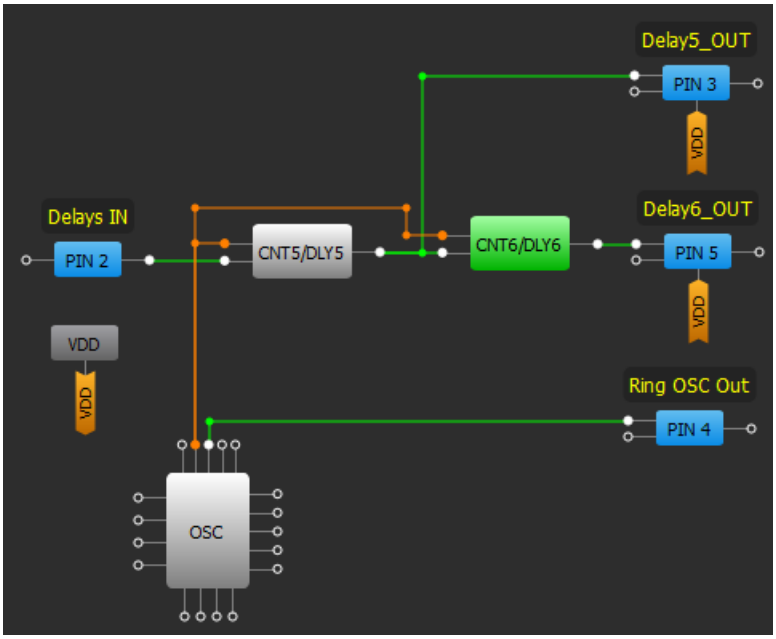


Channel 1 – 2-bit LUT0 output; Channel 2 – Ring OSC output

Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

A similar situation can occur while using two connected delays (all edge detect types except for a pair “Rising edge DLY – Falling edge DLY”).

In the following example, Delay5 and Delay6 are configured in the same way. However, Delay5 time is 11.4us instead of expected 0.4us (Delay5 time).



3.3.3. Workaround

- Set Ring OSC power mode to “Force Power On”
- or, Set Turn on by register option in BG (Band Gap) block as “Enable”

3.4 PGA has an Offset when Loaded

3.4.1. Effect

PGA, Vref

3.4.2. Technical Description

The PGA block has an offset when its output through the VREF is loaded. For reference, the table below shows the load vs PGA 4x gain.

Load, mA	Gain (ideal = 4x)
0	3.87
1	3.84
5	3.78
10	3.71
20	3.5
40	3
80	2.2
160	1.4

When the load current is higher than 10 mA the output offset is large and may influence the design operation significantly.

3.4.3. Workaround

Use an external buffer to support high load.

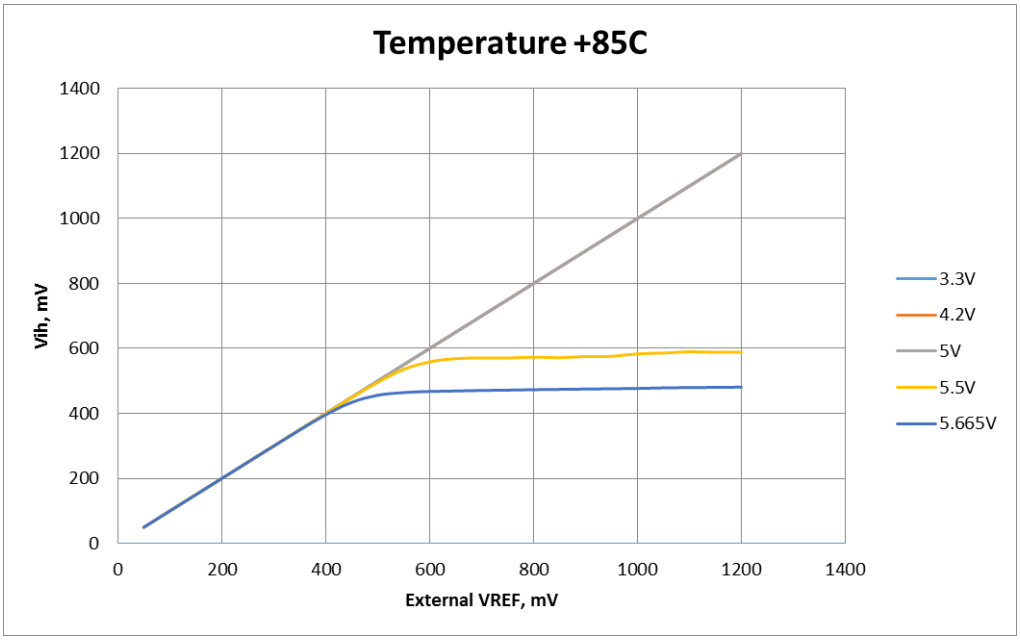
3.5 ACMP Output is Inaccurate when Using External Vref at High VDD and Temperature

3.5.1. Effect

ACMP

3.5.2. Technical Description

When using external Vref source, the ACMP comparison may happen at wrong threshold if the external Vref voltage is higher than a particular value (please see figure below) at high VDD values (> 5V) and high temperature.



3.5.3. Workaround

Avoid using ACMPs in such conditions.

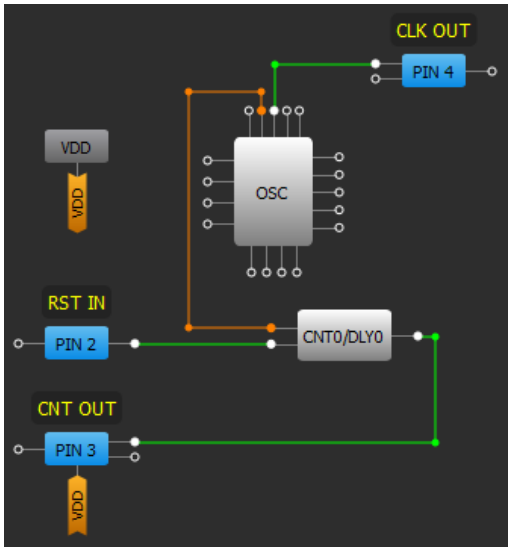
3.6 Incorrect Counter Operation after the Reset

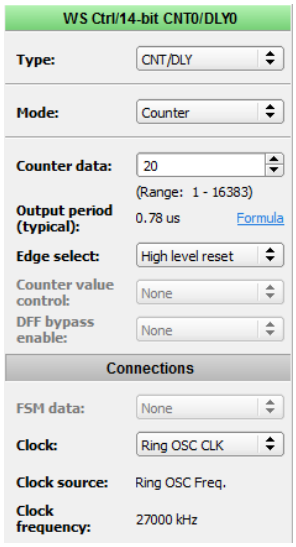
3.6.1. Effect

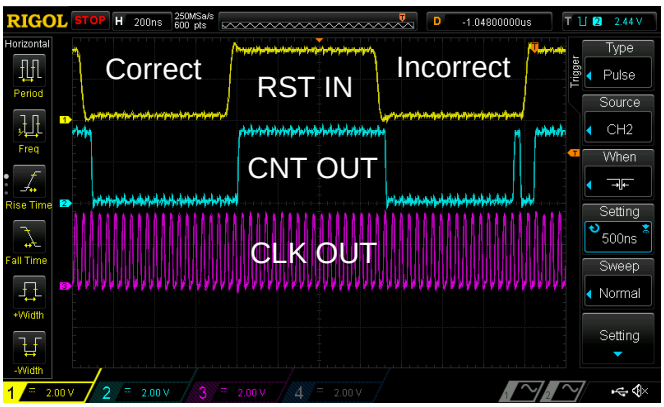
Counter

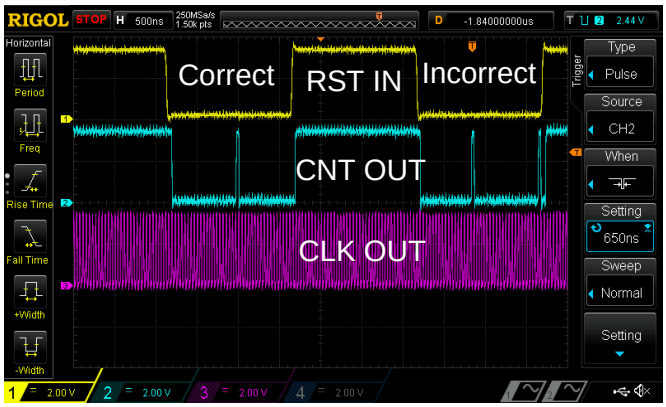
3.6.2. Technical Description

If the Counter Reset occurs at a time very close to a rising edge of the clock signal during clock signal generation (for example OSC operation), there is a possibility that the Counter Data of the Counter is reset incorrectly and the counter end signal (HIGH pulse) may appear faster than expected. This phenomena appears more frequently the higher the clock frequency is.



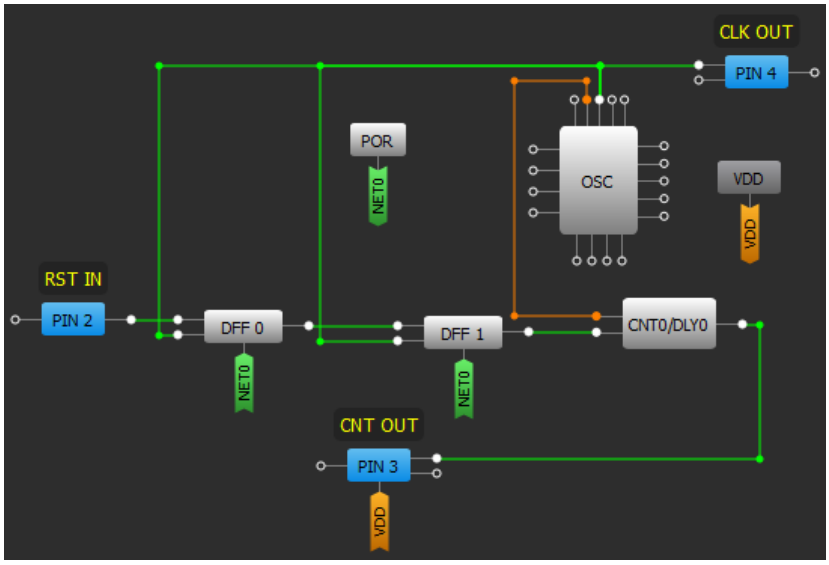






3.6.3. Workaround

Synchronize RESET input of the Counter with its CLK using 2 DFF cells as shown in the image below.



3.7 DCMP OUT+ Output Glitch

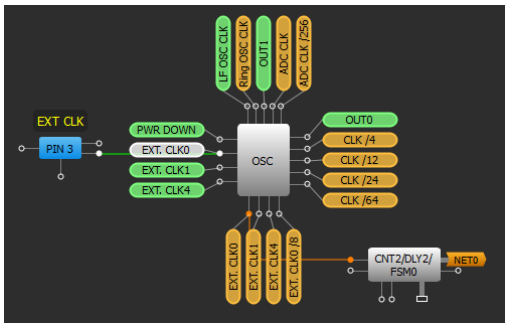
3.7.1. Effect

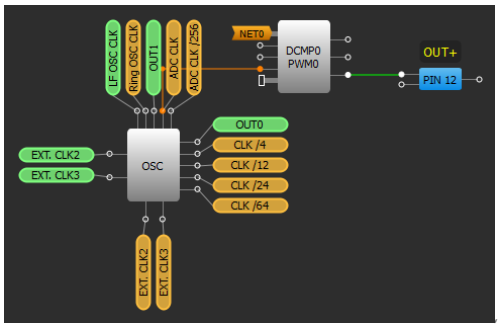
DCMPs

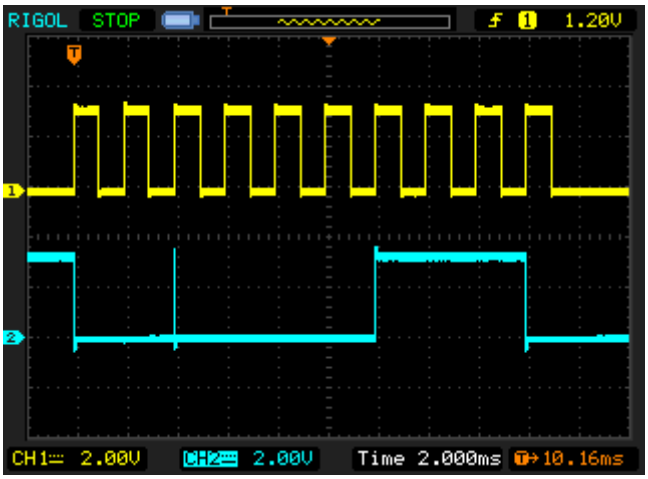
3.7.2. Technical Description

DCMP's OUT+ output may have a glitch when the input data is changed. This issue appears more frequently the higher DCMP clock is.

For example, DCMP IN+ sources from FSM0 and IN- from Register0. DCMP is clocked from the Ring OSC.

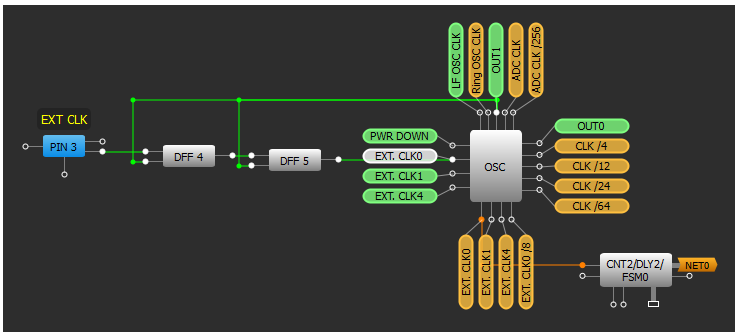


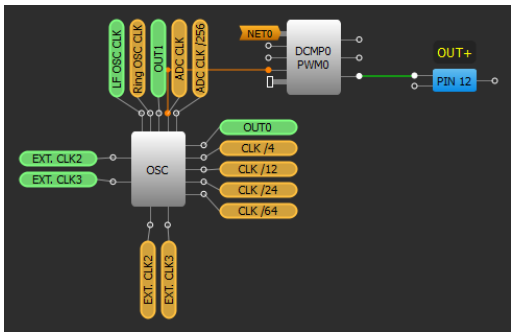




3.7.3. Workaround

Synchronize the data source clock with the DCMP clock source using 2 DFF cells as shown in the images below.





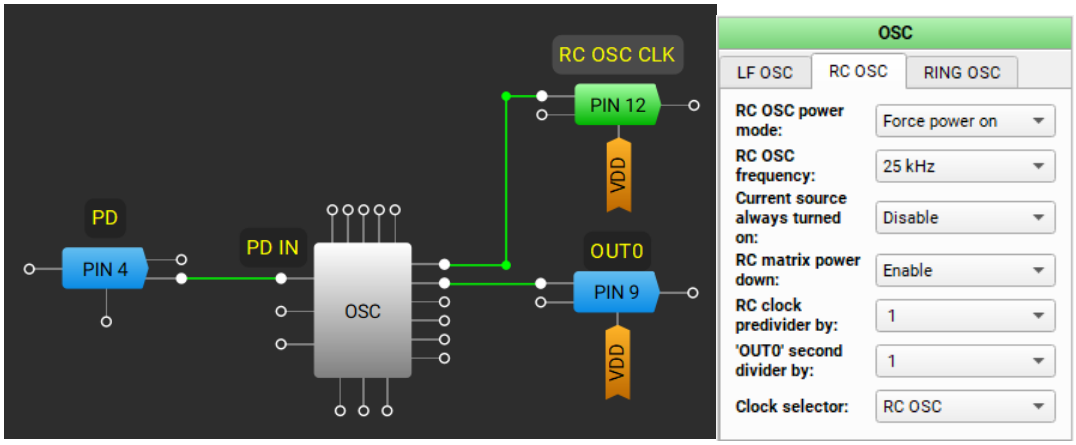
3.8 OSC Long Start-Up Time

3.8.1. Effect

When a short pulse is applied to the PWR DOWN input, the oscillator exhibits a long start-up time.

3.8.2. Conditions

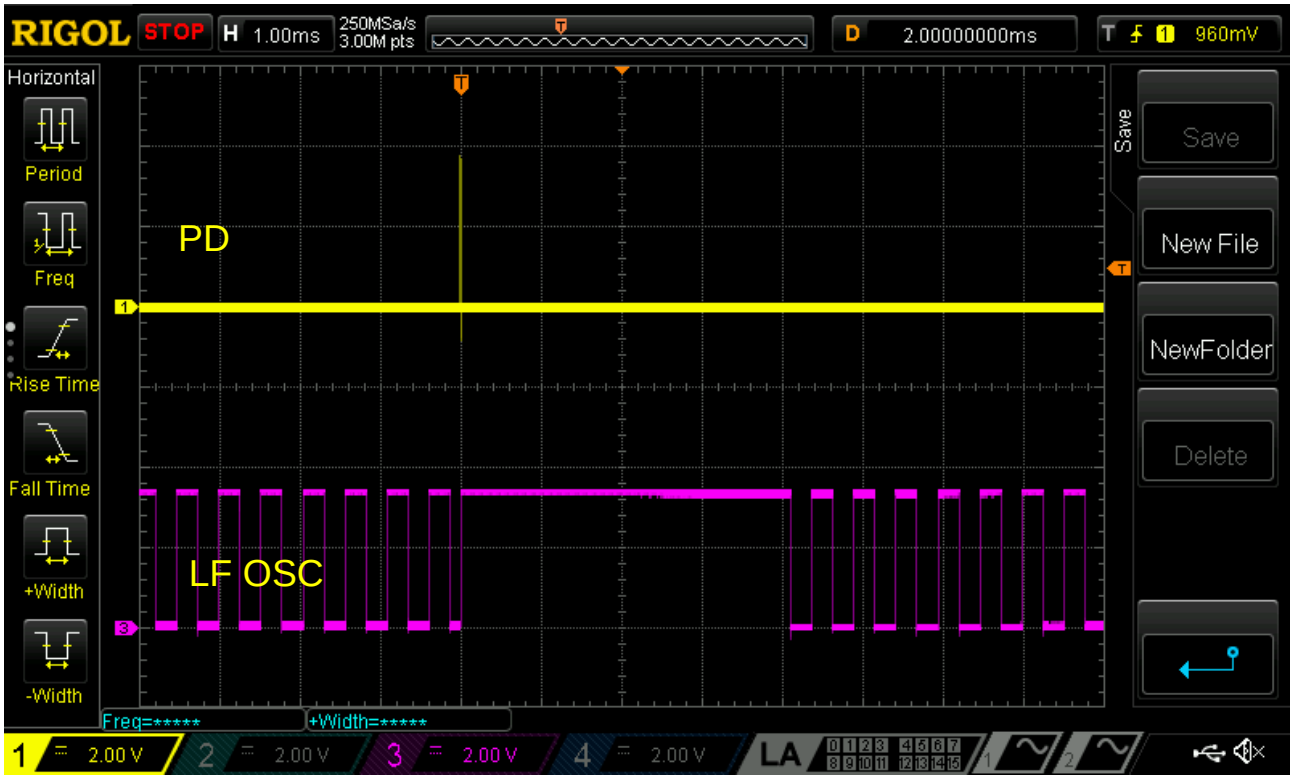
When a short pulse of less than ~40 ns is applied to the PWR DOWN input.



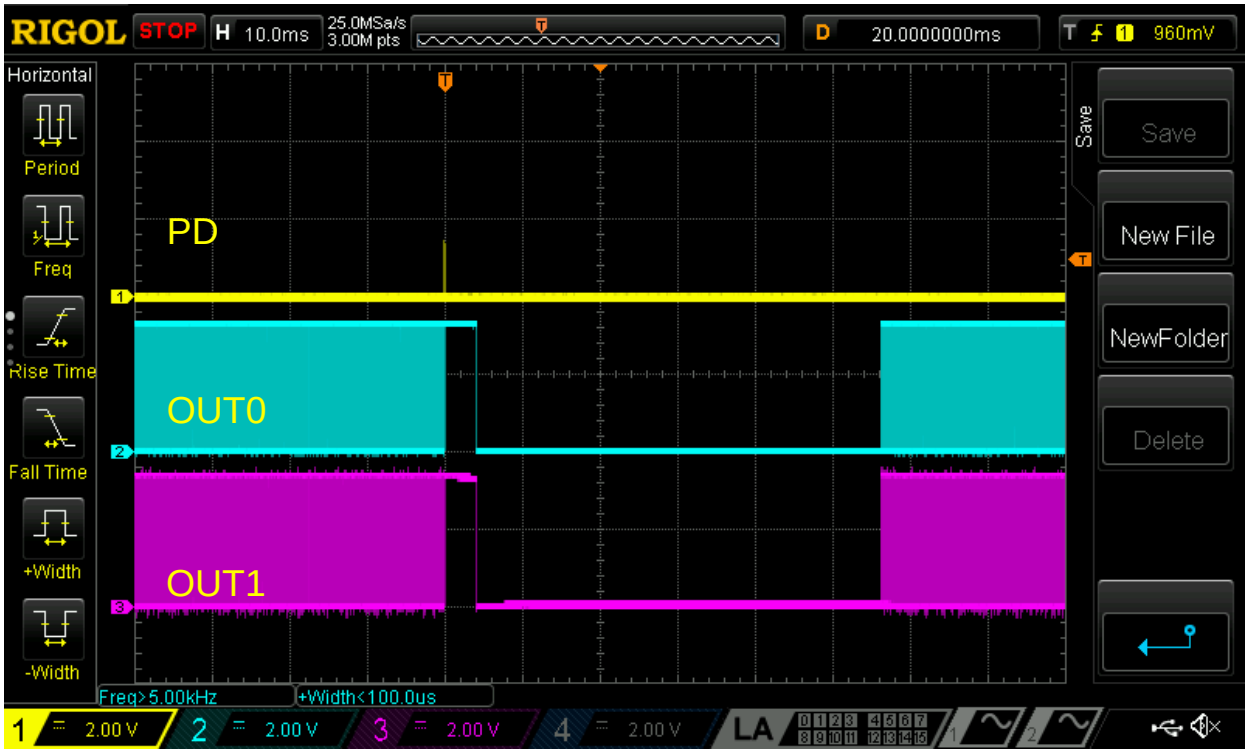
3.8.3. Technical Description

If a pulse with a duration of less than ~40 ns is applied to the PWR DOWN input of the oscillator, the oscillator outputs remain stuck for milliseconds, as shown in Figure 16 and Figure 17. The issue is observed for all available oscillators.

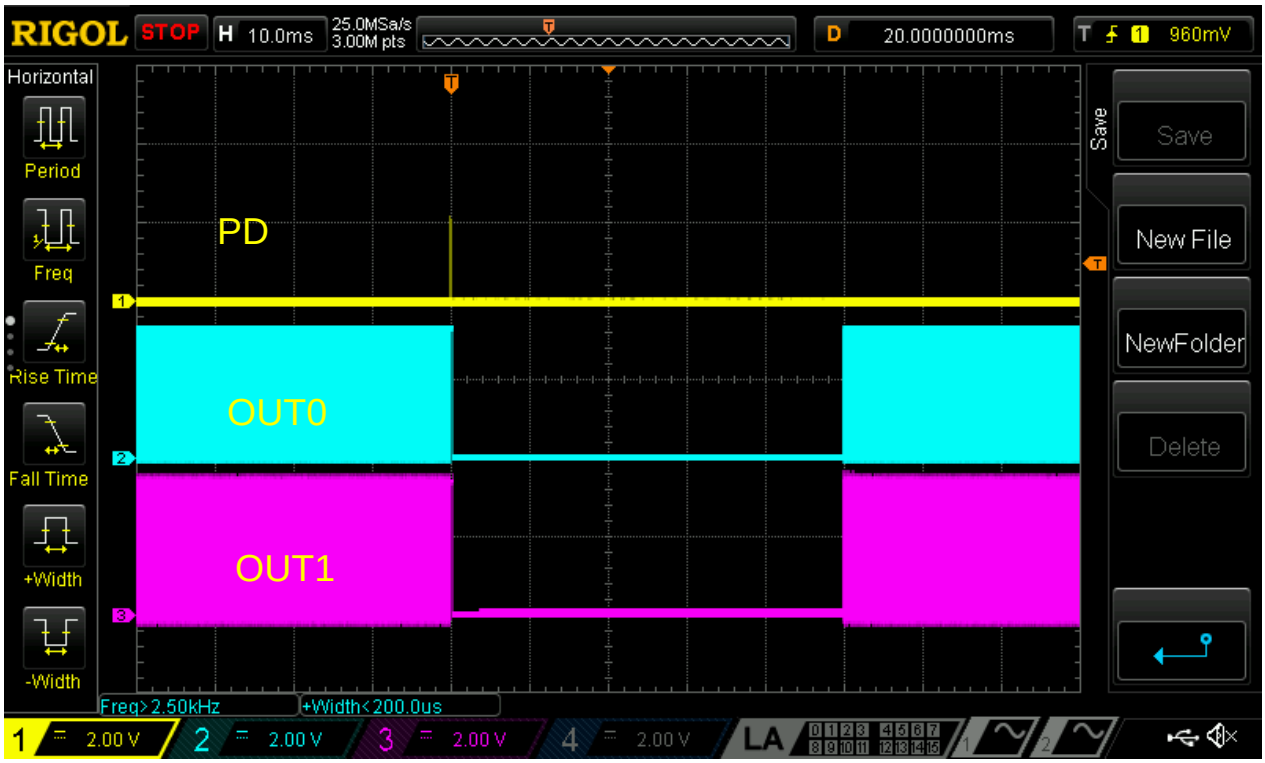
1.9 kHz OSC long start-up



25 kHz OSC Long Start-Up



2 MHz OSC Long Start-Up



3.8.4. Workaround

Avoid applying glitches to the PWR DOWN input of an OSC.

4. Revision History

Revision	Date	Description
1.01	Dec 20, 2024	Added issue #8
1.00	Jun 12, 2024	Initial release.