

## SLG46880-E Errata Note

## Abstract

This document contains the known errata for SLG46880-E and the recommended workarounds.

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## 1. Information

Package(s)	32-pin STQFN: 4.0 mm x 4.0 mm x 0.55 mm, 0.4 mm pitch
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## 2. Errata Summary

Issue #	Issue Title
1	<a href="#">Incorrect I<sup>2</sup>C Reads of the 8-bit Counter Registers</a>
2	<a href="#">Noise Coupling from Vref0 to Low-Power Bandgap</a>
3	<a href="#">Unstable Vref Output Buffer</a>
4	<a href="#">Incorrect Data Write</a>

## 3. Errata Details

### 3.1 Incorrect I<sup>2</sup>C Reads of the 8-bit Counter Registers

#### 3.1.1. Effect

CNT2/DLY2 and CNT4/DLY4

#### 3.1.2. Conditions

I<sup>2</sup>C latch signal and the clock input occur at about the same time.

#### 3.1.3. Technical Description

Asynchronous interaction between the CNT/DLY clock input and the I<sup>2</sup>C latch signal (generated by an I<sup>2</sup>C read command of the CNT/DLY block's count value) can result in an incorrect I<sup>2</sup>C data read. The CNT/DLY block will count accurately, but the count value transferred into the block's I<sup>2</sup>C read register might be loaded incompletely if the I<sup>2</sup>C latch signal and the clock input occur at about the same time.

The example data capture below shows ten periodic I<sup>2</sup>C reads of CNT2/DLY2 configured to count down at about 16 clocks per read. The sixth read sample erroneously shows a value greater than that of the fifth. The seventh sample reads as if the previous I<sup>2</sup>C error never occurred - the difference from the fifth sample (176) to the seventh (143) is 33 clocks or 16 clocks + 17 clocks as expected.

Channel 1 (yellow/top line) – PIN#2 (CNT2/DLY2 Out)

Channel 2 (light blue/2nd line) – PIN#1 (I<sup>2</sup>C Read Triggers)

Channel 3 (magenta/3rd line) – PIN#8 (I<sup>2</sup>C SCL)

Channel 3 (dark blue/4th line) – PIN#9 (I<sup>2</sup>C SDA)

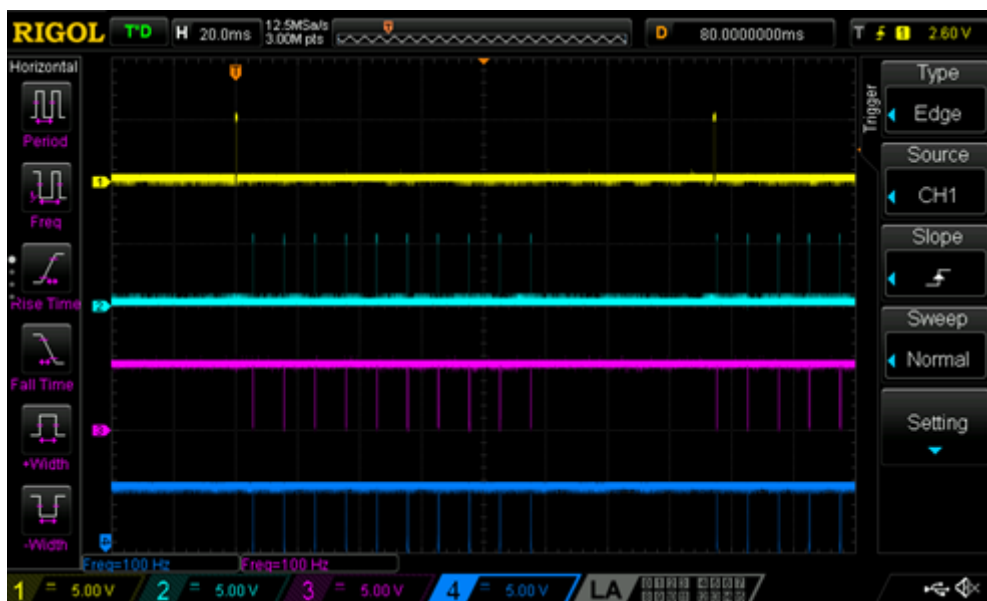


Figure 1. Example Data

#### 3.1.4. Workaround

If the possibility of incorrect I<sup>2</sup>C data reads can't be accommodated for by external software checks, one can guarantee proper operation by stopping the CNT/DLY block's clock during I<sup>2</sup>C reads through one of the following methods: by disabling the oscillator block, by reconfiguring the CNT/DLY block's clock source, or by gating an external clock using a LUT (Look Up Table) in the signal matrix. After disabling the CNT/DLY block's clock, the count registers can be read without error. Please note that this workaround will add the I<sup>2</sup>C read and processing time to the counter's overall clock period.

The best workaround depends on the resource constraints of the application. If the oscillator block doesn't clock other logic elements within the design, a matrix output can be used to manually power down the oscillators for the I<sup>2</sup>C read. When the CNT/DLY block's clock source is routed internally from the oscillator block, I<sup>2</sup>C commands can temporarily reconfigure the CNT/DLY block's clock source registers to select "Ext. CLK. (From Matrix)." This action will disable the clock by connecting it to ground. If the CNT/DLY block is clocked from the signal matrix, LUT can be used to gate the clock during an I<sup>2</sup>C read.

### 3.2 Noise Coupling from Vref0 to Low-Power Bandgap

#### 3.2.1. Effect

All ACMPs

#### 3.2.2. Conditions

Manual powering up the high-speed ACMPs via the "PWR UP" connector.

#### 3.2.3. Technical Description

There is some noise coupling from the Vrefs of high-speed ACMPs to the low-power bandgap (BG) while the high-speed ACMPs Vref is turning on and off.

#### 3.2.4. Workaround

There is no issue with manually powering up the low-speed ACMPs. If you are manually powering up the high-speed ACMPs via the "PWR UP" connector, you should add a 1 ms delay to the output of all of the ACMPs used in the design.

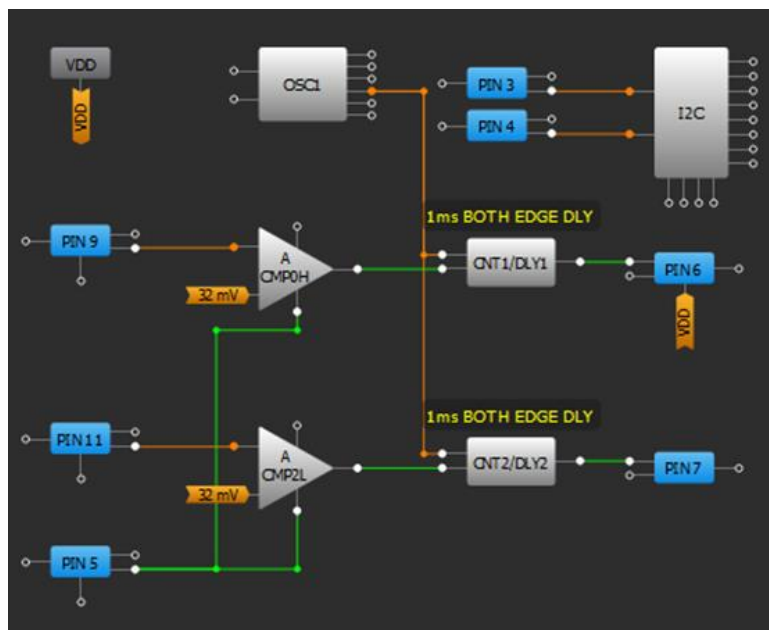


Figure 2. Testing Design

### 3.3 Unstable Vref Output Buffer

#### 3.3.1. Effect

Both Vref Output

#### 3.3.2. Conditions

$V_{DD} = 2.5 \text{ V}$ ,  $V_{ref \text{ Out}} = (0.5 \times V_{DD}) \pm 0.4 \text{ V}$ .

### 3.3.3. Technical Description

For systems where  $V_{DD} = 2.5\text{ V}$ , the Vref output buffer will be unstable if the output voltage is around  $0.5 \times V_{DD}$ .

### 3.3.4. Workaround

For a system where  $V_{DD} = 2.5\text{ V}$ , bypass the buffer if the output voltage of the Vref buffer is within  $(0.5 \times V_{DD}) \pm 0.4$ . Check the Vref section of the device datasheet to see which registers need to be modified.

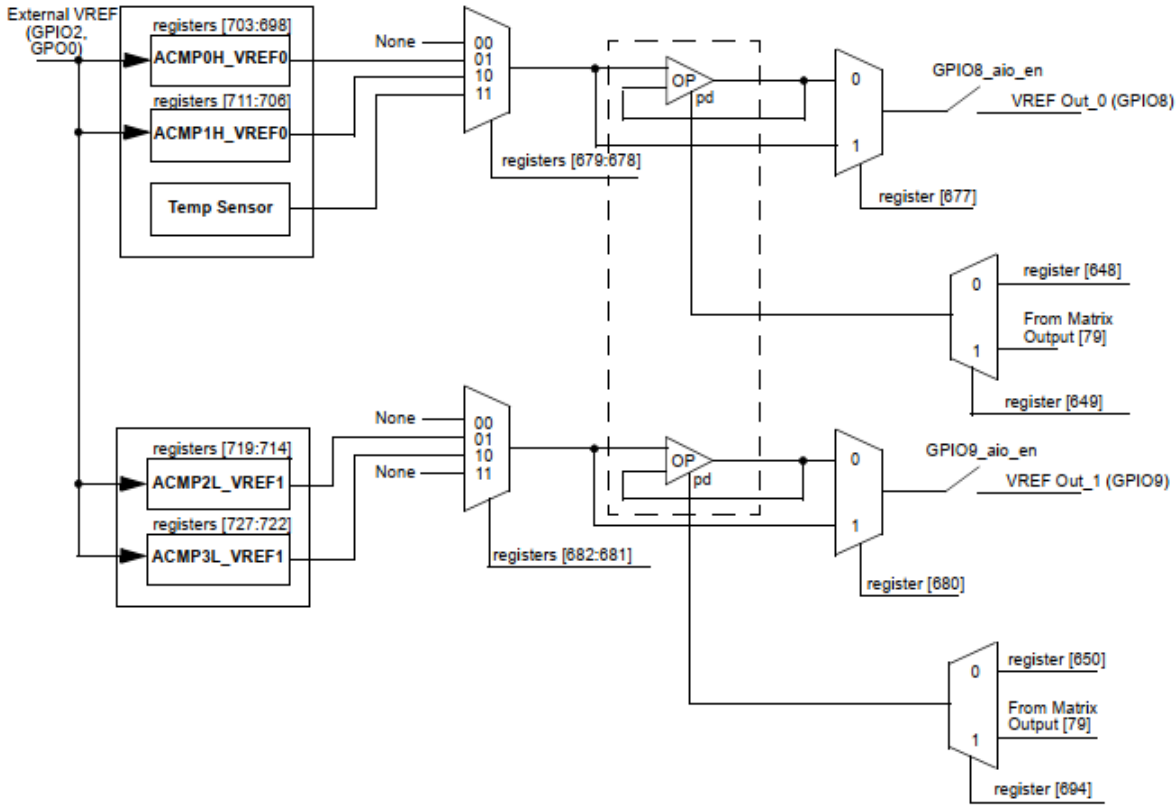


Figure 3. Testing Design

## 3.4 Incorrect Data Write

### 3.4.1. Effect

I<sup>2</sup>C

### 3.4.2. Conditions

Any.

### 3.4.3. Technical Description

When performing a masked I<sup>2</sup>C write, unchanged bits in the 8-bit I<sup>2</sup>C bus may be coupled to the changed bits due to the large coupling capacitor between the I<sup>2</sup>C bus bits, leading to incorrect data being written.

### 3.4.4. Workaround

There is no workaround, but this will be fixed in the next silicon revision.

## 4. Revision History

Revision	Date	Description
1.00	Oct 28, 2025	Initial release.

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