SLG47011-E Errata Note

Abstract

This document contains the known errata for SLG47011-E and the recommended workarounds.

Contents

1. Information

Package(s)	16-pin STQFN: 2.0 mm x 2.0 mm x 0.55 mm, 0.4 mm pitch

2. Errata Summary

Issue #	Issue Title
1	Analog Comparator Output Noise with Slow Rise Input Signal
2	Analog Comparator Output Noise with High-Frequency on the Digital Input/Output

3. Errata Details

3.1 Analog Comparator Output Noise with Slow Rise Input Signal

3.1.1. Effect

Noise at the comparator output under certain conditions.

3.1.2. Conditions

Slow rise input signal with V_{DD} > 3.3 V.

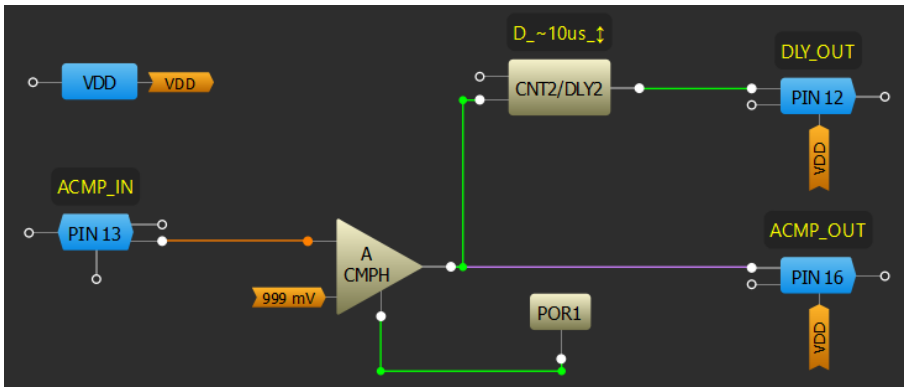

Figure 1. Test Design

3.1.3. Technical Description

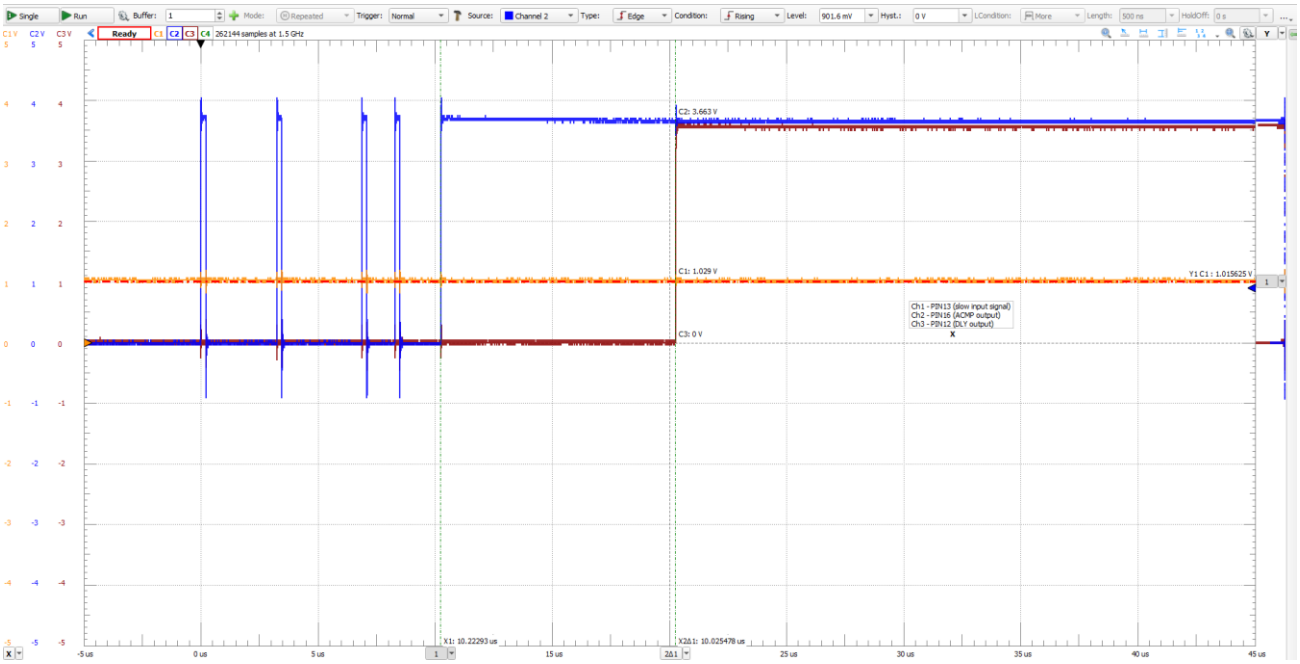

Figure 2. ACMP Output Noise (Ch1 – Slow Input Signal, Ch2 – ACMP Output, Ch3 – DLY Output)

When chip V_{DD} level is more than 3.3 V with ACMP hysteresis 27 mV or 54 mV noise can be seen at the output on some reference levels. As shown in Figure 2.

3.1.4. Workaround

Any one of the following prevents the issue:

- Add both edge delay to ACMP output with delay time more than 10 µs.
- Use hysteresis 162 mV.
- Use V_{DD} < 3.3 V.

3.2 Analog Comparator Output Noise with High-Frequency on the Digital Input/Output

3.2.1. Effect

Noise at the comparator output under certain conditions

3.2.2. Conditions

Frequency > 100 kHz on the digital input/output.

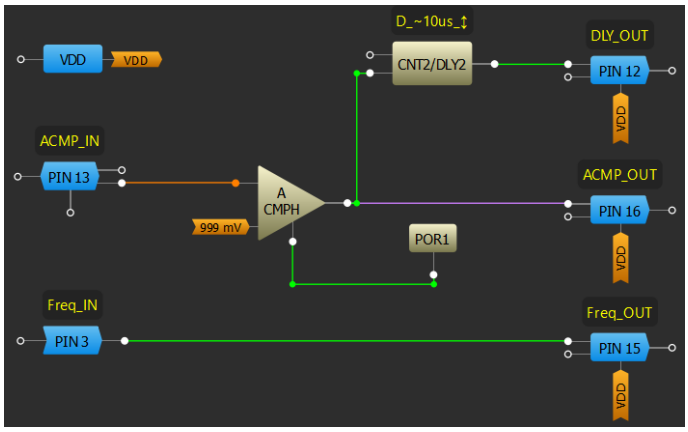

Figure 3. Test Design

3.2.3. Technical Description

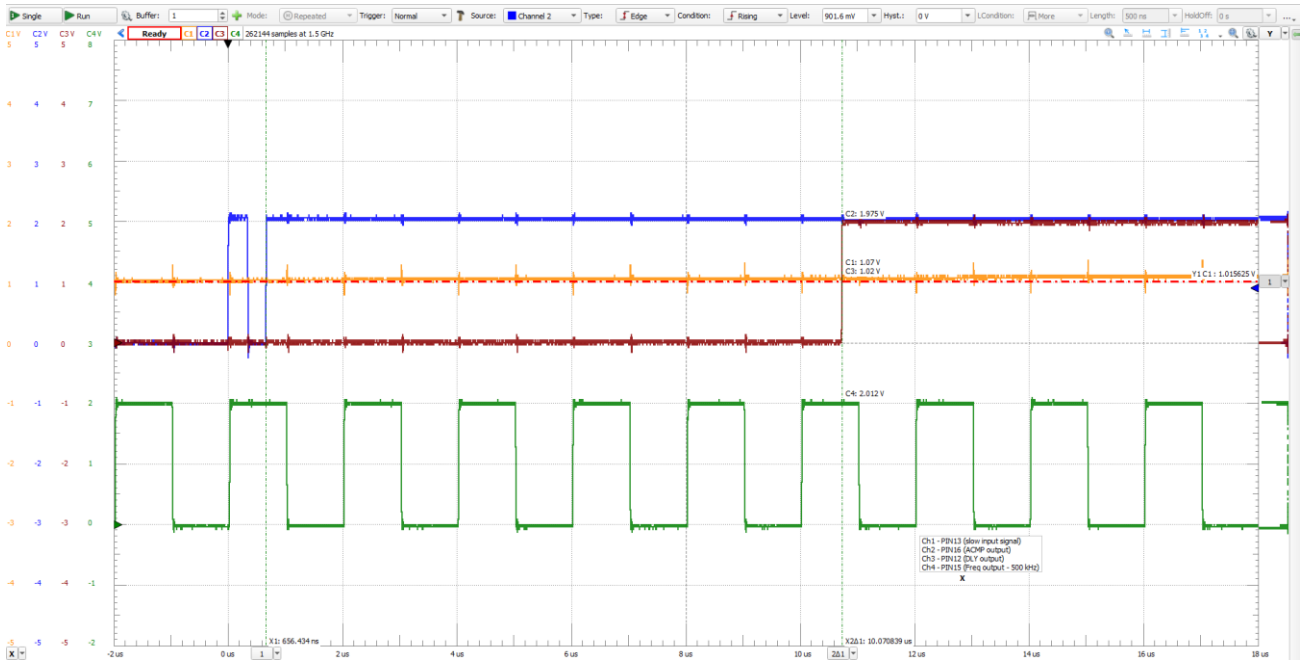

Figure 4. ACMP Output Noise (Ch1 – Slow Input Signal, Ch2 – ACMP Output, Ch3 – DLY Output)

If there is a frequency on the GPIO above 100 kHz, noise may occur at the output of the comparator as shown in Figure 4. This behavior is observed over the entire VDD range. Also, this behavior is not affected by the hysteresis setting.

3.2.4. Workaround

Any one of the following prevents the issue:

- Add both edge delay cells to ACMP output with delay time more than 10 µs.

4. Revision History

Revision	Date	Description
1.00	Jul 24, 2025	Initial release

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