Analog IP

Analog-PLL For Frequency Multiplying

Key Features

- Including Loop-filter
- VCO operating range : 580 -1250 MHz
- Output frequency range : 72.5 –1250 MHz
- Input frequency range : 9.6 -100MHz
- Multiplying (Output freq. / PFD freq.) : 40 -120
- Divider -7bit feedback divider (N divider) -3bit input divider (M divider)
- Selectable feedback loop for skew adjust
- Power-down Mode is supported
- Multiple outputs with post-divider
- SSC Input is available (recommend triangle profile)
- Power-on sequence is constraint-free
- STBY sequence is constraint-free

Technology

Process：TSMC 40LP

Operating Condition

Parameter		Min	Max	Unit
Operating Voltage（VDDAI)		1.04	1.26	V
Operating Voltage（VDD)		1.04	1.26	V
Junction Temperature		-40	125	℃
Input Clock	Duty	30	70	%
	Rise/Fall time	-	0.2	ns

**This IP is contract design IP. Please contact for detail.*

CTPD-24-140
R06PF0107EJ0100

2024.9