Analog IP

Analog-PLL For Frequency Multiplying

Key Features

- Including Loop-filter
- VCO operating range : 2000MHz - 4096 MHz
- Output frequency range : 1000MHz - 2048 MHz
- Input frequency range : 12.5MHz - 200 MHz
- Multiplying (Output freq. / PFD freq.) : 40 - 120
- Divider
  7bit feedback divider and 3bit input divider
- Power-down Mode
- Multiple outputs with post-divider
- Power-on sequence is constraint-free
- STBY sequence is constraint-free

Technology

Process：TSMC 16nm FF+

Operating Condition

Parameter		Min	Max	Unit
Operating Voltage（AVDD)		1.62	1.98	V
Operating Voltage（VDD)		0.745	0.88	V
Junction Temperature		-40	125	℃
Input Clock	Duty	27	70	%
	Rise/Fall time	-	0.2	ns

CTPD-24-130
R06PF0099EJ0100

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