Analog IP

Analog-PLL For Skew adjust

Overview

This core is Analog PLL with Skew adjust. This core can adjust the output clock delay using the external delay.

Technology

Process: TSMC T22ULP

Features

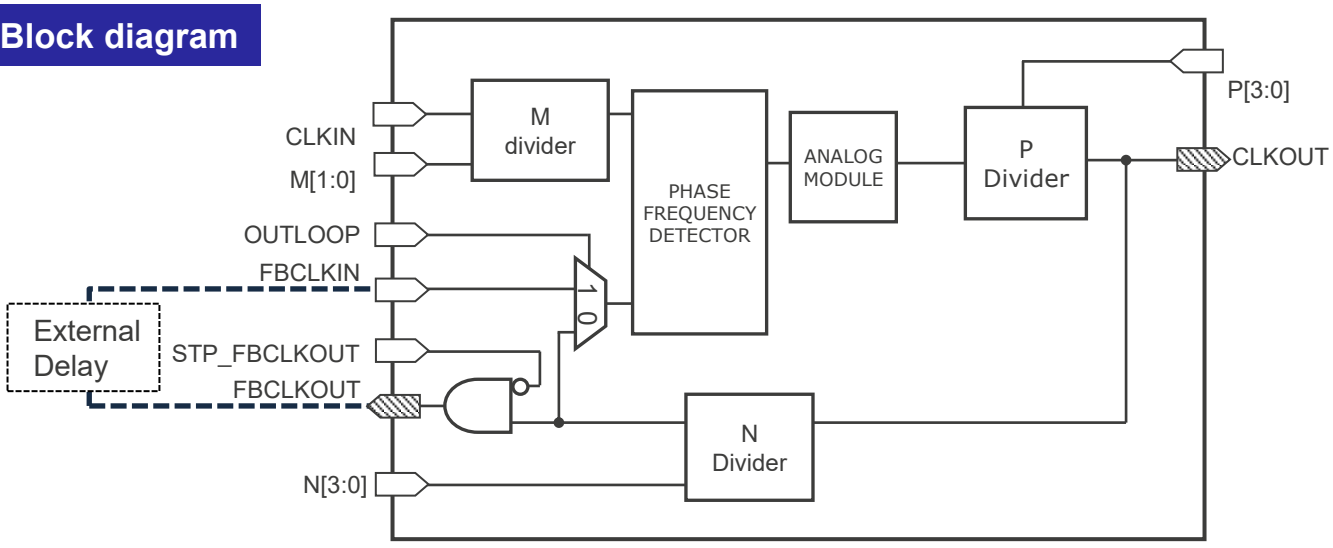
- Including Loop-filter
- VCO operating range : 560 - 1190 MHz
- Output frequency (CLKOUT): 40 - 1190 MHz
- Input frequency (CLKIN) : 10 - 170 MHz
- PFD comparison frequency : 10 - 85 MHz
- Multiplying CLKOUT / PFD : 14, 28 and 56
- Divider
  - 4bit feedback divider (N divider)
  - 2bit input divider (M divider)
  - 4bit output divider (P divider)
- Selectable feedback loop by OUTLOOP
- Power-down Mode

Parameter		Min	Max	Unit
Operating Voltage at transistor	AVDD	1.60	1.98	V
	VDD	0.81	0.99	V
Junction Temperature		-40	125	℃
Input Clock	Period Jitter	-150	150	ps
	Duty	30	70	%
	Rise/Fall time *1	-	0.2	ns

*1 : 10%-90% of VDD in LSI

- SSC Input is not available
- Power-on sequence is constraint-free
- STBY sequence is constraint-free

Block diagram



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