Interface IP

Configurable PCI Express 4.0 Link Controller

Overview

The Renesas PCIe 4.0 Dual Mode Link Controller IP is compliant with the “PCI Express (PCIe) 4.0 Base Specification”. This IP supports the major functions required as PCIe link IP for embedded systems. The system interface of this IP is based on the “AMBA® AXI Protocol specification v1.0” ARM IHI 0022B and the “PHY Interface For the PCI Express, SATA, and USB3.1 Architectures (PIPE) 4.4.1 Specification”. This IP has many configurable parameters for each products. This IP is written in Verilog RTL.

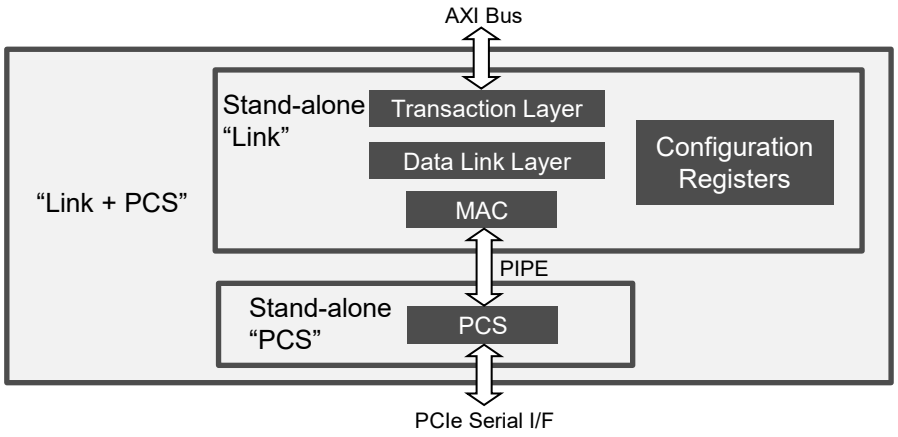
Key Features

General

- Compliant with “PCI Express™ Base Specification, Rev. 4.0 Version 1.0”
- Compliant with “PHY Interface For the PCI Express, SATA, and USB3.1 Architectures”
- Compliant with “AMBA® AXI Protocol Specification v1.0”

PCI Express

- Possible macro type :
  - “Link + PCS”
  - Stand-alone “Link”
  - Stand-alone “PCS”



- Dual mode (Root Complex / Endpoint) Applications, Type0/1 Configuration Register
- Data Rate 2.5 GT/s, 5.0 GT/s, 8.0 GT/s and 16.0 GT/s
- Number of lanes x1, x2 and x4
- Number of outstanding requests 1 to 8
- Number of functions for Endpoint 1 or 2
- Clock Power Management supported
- Power Management (PCI-PM and ASPM supported)
- Error handling/logging (AER supported)
- Lane reversal and Polarity inversion
- Max Payload Size 128 / 256 bytes
- SRIS / SRNS supported

AXI I/F

- With / without AXI I/F (selectable)
- Data bus bit width: 64bits or 128bits
- Supports little endian
- Provides master interface and slave interface
- Supports DMA transfer function up to 8 channels
  - 2-way DMA Control selectable, Register base control / Descriptor table base control

Note : This IP has many selectable or configurable parameters according to customer's requirements for various functions and performance. Please contact us for the settings of this link IP’s parameters.

CTPD-25-017
R06PF0123EJ0100