IP License

RX (Renesas Extreme) Core

Industry-Leading Performance, Power Efficient 32-bit CPU

The proven RX CPU is now available.
Our RX Core IP, widely adopted in high-quality industrial and consumer applications, makes your design easy from FPGA prototyping to SoC development.

All the development suite you need is supported.

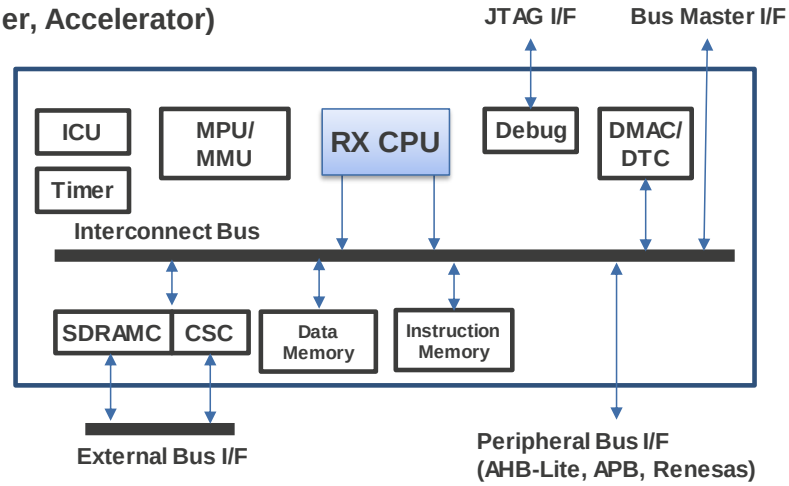
- RX CPU Subsystem including basic peripherals, interconnect bus and memory interfaces
- Comprehensive Development Environment and Partner Ecosystem of RX family

CPU Subsystem

- **RX CPU Core**
  includes FPU
- **MPU/MMU**
- **Cache**
- **Memory Interface**
  Instruction, Data memories
- **Debug Function**
- **Bus System**
  High-speed Interconnect Bus
  Peripheral Bus
  External Bus Interface
  (SDRAMC)
- **Peripherals**
  Timer
  Interrupt Controller
  Data Transfer Function
  (DMAC/DTC)

Block Diagram

Type C (Microcontroller, Accelerator)



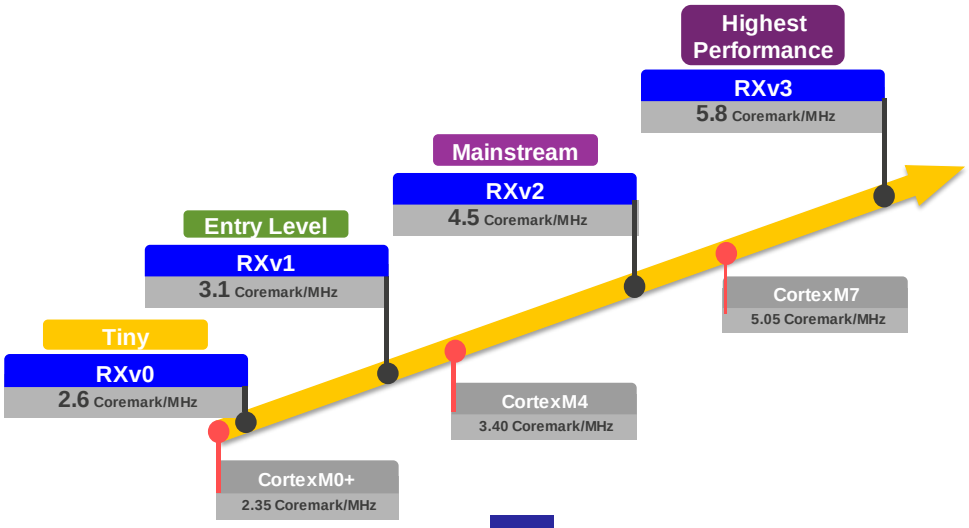
RENESAS
BIG IDEAS FOR EVERY SPACE

RX CPU Sub System Portfolio

	Type C Microcontroller, Accelerator Instruction Memory	Type S Microprocessor Cache
RXv3 Highest Performance 5-stage, enhanced superscalar pipeline DSP/Single-precision FPU Single-Cycle register saves Double-precision FPU	◆ **RXv3-CM** Dual-core microcontroller ◆ **RXv3-C** High performance microcontroller	◆ **RXv3-SM** Multicore microprocessor ◆ **RXv3-S** High performance microprocessor
RXv2 Mainstream 5-stage, superscalar pipeline DSP/Single-precision FPU	◆ **RXv2-CM** Dual-core microcontroller ◆ **RXv2-C** Mainstream microcontroller	◆ **RXv2-S** Mainstream microprocessor
RXv1 Entry Level 5-stage, single issue pipeline DSP/Single-precision FPU	◆ **RXv1-C** Entry-level microcontroller	
RXv0 Tiny 3-stage, single issue pipeline DSP/Single-precision FPU	◆ **RXv0-C** Tiny microcontroller	

RX CPU Core

- **Unified Architecture Covering the Small to Large Applications**
- **Superior Computing Performance and Power Efficiency**
  - Compact code size by adopting a variable-length instruction set
  - Optimized pipeline architecture for industry-leading performance
  - Energy-saving cache design to boost energy efficiency
- **Unrivaled Digital Signal Processing Performance**
  - Integrated DSP and FPU as all the core's basic configuration
  - Double-precision FPU for easy porting of high precision control models
  - DSP/FPU operations and memory accesses simultaneously for high data supply capability
- **Fastest Interrupt Response**
  - Single-cycle register saves for minimizing the interrupt handling overhead



Contact **ip-promotion@lm.renesas.com**

URL https://www.renesas.com/jp/ja/products/ip-products.html

This document has the information under development or consideration.
Therefore, it may be changed in the future.