Interface IP

PCI Express 5.0 Link Controller

Overview

This IP is a Renesas-developed Controller IP for PCI Express® (PCIe®) 5.0. This IP is from AMBA® AXI interface to PIPE 5 interface. It has a Data Link Layer. It also has a Transaction Layer each for the Root Complex and Endpoint, and Type 0/1 Configuration Registers. It also has a DMA controller function.
This IP is written in Verilog RTL.

Key Features

AMBA® AXI interface

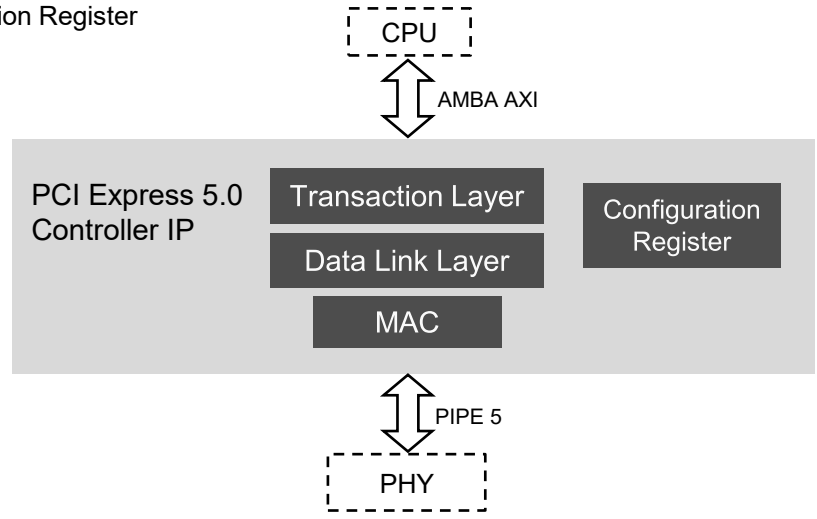
- Conforming to AMBA® AXI Protocol v1.0 Specification ARM IHI 0022B
- Interface: Master/Slave
- Endian: Little
- Bus Width: 128 bits
- DMAC functions are provided

PCIe specification

- Conforming to PCI Express Base Specification 5.0
- Supports
  PCIe1: 2.5[GT/s]
  PCIe2: 5.0[GT/s]
  PCIe3: 8.0[GT/s])
  PCIe4: 16.0[GT/s])
  PCIe5: 32[GT/s]
- Root Complex / Endpoint Applications, Type0/1 Configuration Register
- Multiple lane implementations x1
- Lane reversal and Polarity inversion
- Maximum data payload size is 4096 bytes, Maximum read request size is 4096 bytes
- Number of outstanding requests1

PIPE interface

- Supports PIPE 5.2
- Fixed Data-Path:32bit
  PCIe1: 62.5[MHz]
  PCIe2: 125[MHz]
  PCIe3: 250[MHz]
  PCIe4: 500[MHz]
  PCIe5: 1[GHz]
- Message Bus I/F support
- LPC interface support



CTP-25-018
R06PF0046EJ0101