Interface IP

USB2.0 PHY for TSMC 40nm LP Single-Port Transceiver

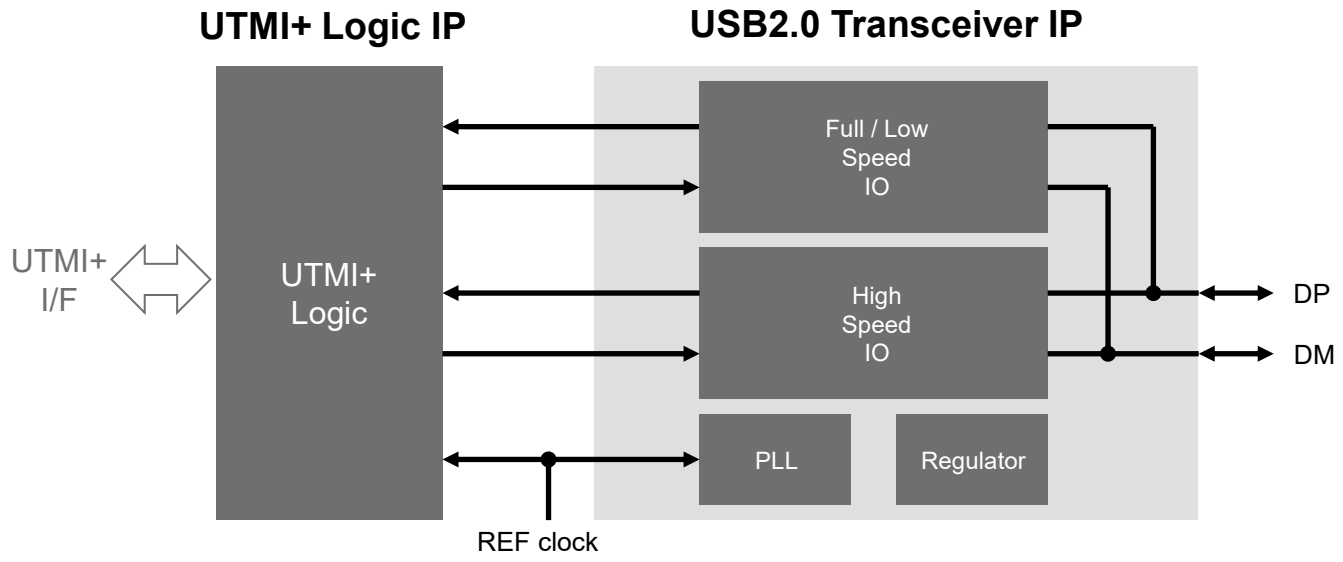
Overview

The Renesas USB2.0 Transceiver is useful analog 1port transceiver hard macro for UTMI+ (USB2.0 Transceiver Macro cell Interface +) Level3 of TSMC 40nm LP process. This macro can be configured to operate as a USB2.0 peripheral or USB2.0 host controller.

Key Features

- Renesas USB2.0 Transceiver can be used for analog transceiver of following interface .
  - Universal Serial Bus Specification Revision 2.0
  - Battery Charging Specification Revision 1.2
- Technology is TSMC 40nm LP 1p7M/1p8M .
- Supply voltage can be applied 1.1V for core voltage and 3.3V for IO voltage.
- USB transfer mode is high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) modes.
- A terminal resistance, pull-up resistor, and pull-down resistor are included.
- Input reference clock is 48MHz, 24MHz, 20MHz and 12MHz.

Block Diagram



**This IP is contract design IP. Please contact for detail.*

*Before purchasing or using any Renesas Electronics products listed herein, please refer to the latest product manual and/or data sheet in advance.

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