ISL91212AEVAL1Z

The ISL91212AEVAL1Z platform allows quick evaluation of the high performance features of the ISL91212A multi-output PMIC, which has three controllers capable of configuring its power stages for 2+1+1 channel outputs. Each channel can deliver up to 5A continuous output current per phase. The ISL91212A uses the Renesas proprietary R5 modulator technology to maintain accurate voltage regulation, while providing excellent efficiency and transient response. It also supports the standard I^2C communication protocol, ideal for systems using a single-cell battery.

Specifications

The board is designed to operate at the following operating conditions:

- Input voltage rating from 2.5V to 5.5V
- Programmable output voltage range of 0.3V to 2V
- 2+1+1 configuration with 5A maximum load current/phase
- 2MHz switching frequency
- DVS slew rate of 2.5mV/µs
- Power-up/ Power-down sequence: Buck1-3 power up/power down at the same time
- Operating temperature range: -40°C to +85°C
- V_{OUT1} = 1.0V, V_{OUT2} = 1.8V, and V_{OUT3} = 1.2V, for DVS0

Features

- Small, compact design
- Supports I^2C bus communication protocol
- Adjustable V_{OUT} and independent DVS control for both channels
- Real-time fault protection and monitor (OC, UV, OV, OT)
- Six layer board design optimized for thermal performance and efficiency
- Connectors, test points, and jumpers for easy measurements
- Built-in load transient circuits for each output channel

Contents

The ISL91212AEVAL1Z evaluation board shipment contains:

- ISL91212AEVAL1Z evaluation board
- Evaluation software
- Renesas mini USB I^2C dongle with USB cable (ISLUSBMINIEVAL1Z)
- All applicable documentation

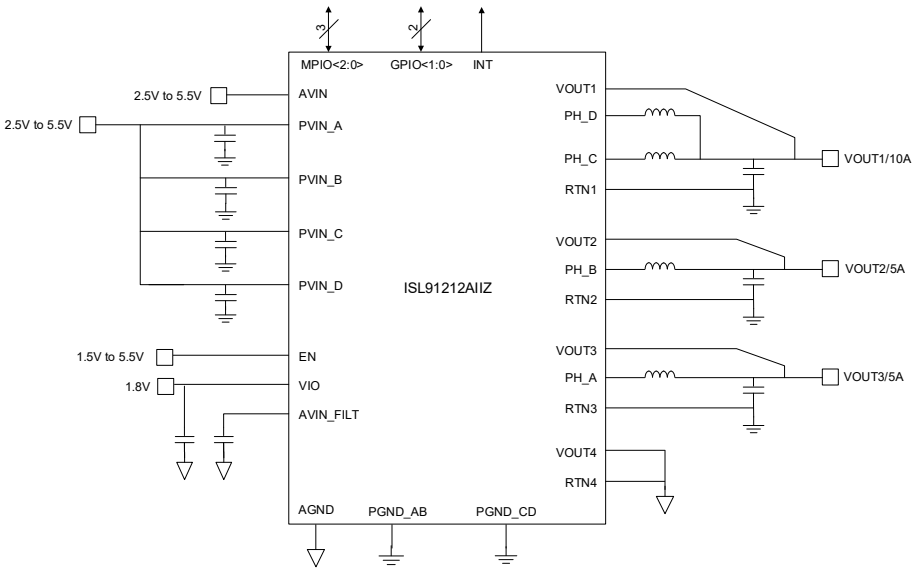

Figure 1. ISL91212A 2+1+1 Block Diagram

Contents

1. Functional Description

The ISL91212AEVAL1Z evaluation board provides a simple platform to demonstrate the feature-rich ISL91212A PMIC. With DVS0 configuration, it has a 1.0V, 1.8V, and 1.2V output (default) on each of its output channels after start-up, and the I^2C can program each output voltage. The evaluation board has been functionally optimized for best performance, working harmoniously with the factory default tuning on the ISL91212A. The input power and load connections are provided through multi-pin connectors for high current operations.

The ISL91212AEVAL1Z is shown in Figure 11. The evaluation board's key test points and jumpers are listed in Table 1. The ISL91212A's internal registers can be accessed by the I^2C through the on-board header J_{66} (I^2C).

Table 1. Description of Important Test Points and Jumpers

Test Point	Description
J_6(+), J_7(-)	Header for connecting V_{IN} supply
J_{35}(+), J_{38}(-)	Buck1 header for connecting external load
J_{37}(+), J_{58}(-)	Buck2 header for connecting external load
J_{57}(+), J_{36}(-)	Buck3 header for connecting external load
J_3	V_{IN} Kelvin connection for efficiency measurements
J_{65}	Buck1 V_{OUT} Kelvin connection for efficiency measurements
J_{63}	Buck2 V_{OUT} Kelvin connection for efficiency measurements
J_{64}	Buck3 V_{OUT} Kelvin connection for efficiency measurements
TP_1	VCC_6V supply for VIO LDO and load transient circuits
J_{60}	Buck1 driver input for load transient circuit
J_{61}	Buck2 driver input for load transient circuit
J_{62}	Buck3 driver input for load transient circuit
J_{52}	Load transient current sense, 1A/10mV
J_{55}	Load transient current sense, 1A/10mV
J_{59}	Load transient current sense, 1A/10mV
J_{66}	Header for connecting to I^2C interface
J_{42}	Header for connecting to I^2C interface

The evaluation software GUI window for the ISL91212A is shown in Figure 10. The schematic of the ISL91212AEVAL1Z is shown in Figure 15 through Figure 18. The PCB layout images for all layers are shown in Figure 19 through Figure 26. The bill of materials of the ISL91212AEVAL1Z is shown in the Bill of Materials.

1.1 Recommended Equipment

- 0V to 10V power supply with at least 10A current sourcing capability (VIN SUPPLY BIAS)
- 0V to 10V power supply with at least 1A current sourcing capability (VCC_6V SUPPLY BIAS)
- Electronic loads capable of sinking current up to 10A
- Digital multimeter
- 500MHz quad oscilloscope
- Dual edge slew rate controllable signal generator
- Differential probe (for load transient current measurement)

1.2 Operating Range

The V_{IN} range is 2.5V to 5.5V. The adjustable V_{OUT} range is 0.3V to 2.0V. The I_{OUT} range of the board is 0A to 5A per phase. The operating ambient temperature range is -40°C to +85°C.

1.3 Quick Start Guide

The ISL91212AEVAL1Z default output voltages for V_{OUT1}, V_{OUT2}, and V_{OUT3} are set at 1.0V, 1.8V, and 1.2V, respectively, for DVS0. All board jumpers should be left open at power up. All the settings and features are loaded through the one-time programmable memory inside the IC, after the minimum bias conditions are met. See Buck Output Voltage Configuration and Setting Up the ISL91212AEVAL1Z for further details with selecting output voltages and steps to setup and power the board.

1.3.1 Buck Output Voltage Configuration

ISL91212A has four independently programmable voltage settings to control the output voltage for a given buck output: DVS0, DVS1, DVS2, and DVS3. The ISL91212AEVAL1Z evaluation board has several options to achieve dynamic voltage scaling (DVS). For additional information on DVS and output voltage control methods, refer to the *ISL91212A Datasheet*.

The default PMIC device on the ISL91212AEVAL1Z board uses IO_PINMODE = 0x6, where the MPIO0/1/2 pins are used to select the respective Buck's output voltage.

Caution: The input state of the MPIO pins is not defined on the ISL91212AEVAL1Z EVB hardware – MPIO0/2 are floating, MPIO1 is pulled high, which can result in undesired output voltage selection at power up. Before power up, pull MPIO0/1/2 pins to GND to ensure a defined low logic state. This can be done by connecting a jumper wire from the respective test point to ground. The mapping of MPIOx pin logic to DVS selection per buck rail (VOUTX) is shown in Table 2

Table 2. DVS Logic

MPIO0	MPIO1	MPIO2	Buck1(V_{OUT1})	Buck2(V_{OUT2})	Buck3(V_{OUT3})
Low	Low	Low	DVS0: 1.0V	DVS0: 1.8V	DVS0: 1.2V
High	Low	Low	DVS1: 0.95V	DVS0: 1.8V	DVS0: 1.2V
Low	High	Low	DVS2: 0.9V	DVS0: 1.8V	DVS0: 1.2V
High	High	Low	DVS3: 0.9V	DVS0: 1.8V	DVS0: 1.2V
Low	Low	High	DVS0: 1.0V	DVS1: 1.5V	DVS0: 1.2V
High	Low	High	DVS1: 0.95V	DVS1: 1.5V	DVS0: 1.2V
Low	High	High	DVS2: 0.9V	DVS1: 1.5V	DVS0: 1.2V
High	High	High	DVS3: 0.9V	DVS1: 1.5V	DVS0: 1.2V

1.3.2 Setting Up the ISL91212AEVAL1Z

1. Place scope probes on the V_{OUT} test point and other test points of interest. Pull MPIO0 (TP13), MPIO1 (TP14) and MPIO2 (TP15) to GND. The V_{OUT1},V_{OUT2} and V_{OUT3} default outputs are set at DVS0.
2. Connect a power supply to J_6 and J_7 (VIN SUPPLY), with a voltage setting between 2.5V and 5.5V. This will bias the PVIN and AVIN pins, but not initiate the startup sequence. The quiescent current should be less than 1mA.
3. Connect a second power supply to TP_1 (VCC_6V), with the voltage set to 6V. This will bias the VIO and Chip Enable pin as well as the on-board load transient circuits. The ISL91212A will boot up its internal reference, load the default register settings, and then initiate a power-on sequence. The three outputs should turn on in Pulse Skipping mode if there are no external loads present. V_{OUT1} defaults to 1.0V, V_{OUT2} defaults to 1.8V, and V_{OUT3} defaults to 1.2V.

4. During the startup sequence, the three outputs should turn on at the same time with a 1.4ms delay from the Chip Enable pin going high.
5. To initiate a shutdown sequence, toggle switch SW1 to DISABLE position to short EN to GND. The ISL91212AEVAL1Z turns off all the buck regulators at the same time.

1.3.3 Enabling I²C Communication

The ISL91212A supports I²C communication by default. A USB to I²C communication dongle (ISLUSBMINIEVAL1Z) is included with each ISL91212AEVAL1Z evaluation board, and the Renesas Graphical User Interface (GUI) supports this tool across all operating systems.

To communicate with ISL91212A using I²C, connect the Renesas USB to I²C dongle to J_{66}.

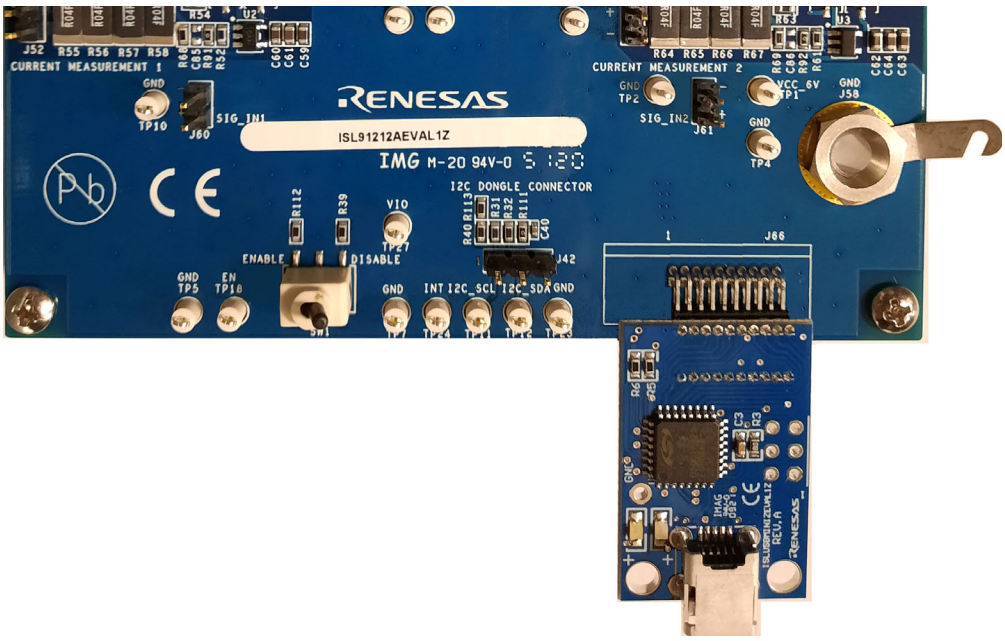

Figure 2. Communication Dongle Connection

1.3.4 Measuring Efficiency

1. Connect a power supply at J_6 (VIN supply), with the voltage setting between 2.5 and 5.5V. Set its current limit high enough to support the maximum load current with additional headroom. If the power supply supports remote sense lines, use a Kelvin connection on J_3. Otherwise, connect a multimeter at J_3.
2. Apply 6V to TP_1 (VCC_6V) to initiate the startup sequence. All three outputs turn on. Disable the other two outputs using the **Enable/Disable** switch in the GUI to get an accurate single channel measurement.
3. Turn on the electronic load at VOUTx. The connection should be made at J_{35} (V_{OUT1}) or J_{37} (V_{OUT2}) or J_{57} (V_{OUT3}). Ensure the load current does not exceed 5A per phase, and use the correct wire size when attaching the electronic load.
4. Measure the output voltage with a multimeter. The voltage should regulate within the limits specified in the *ISL91212A Datasheet*.
5. To determine efficiency:
   a. Measure input and output voltages at the Kelvin sense test points (S+ and S-), which are located at J_3 (VIN SENSE) and J_{65} (BUCK1 SENSE), or J_{63} (BUCK2 SENSE) or J_{64} (BUCK3 SENSE) headers.
   b. Measure the input and output currents from the VIN power supply and the electronic load.
   c. Calculate efficiency based on these measurements. For detailed setup information, see Figure 13.

1.3.5 Measuring Load Transients

1. Complete the setup procedure (see Setting Up the ISL91212AEVAL1Z). The ISL91212AEVAL1Z should already be powered up with 2.5V to 5.5V at J_6 (VIN supply) and 6V at TP_1 (VCC_6V).
2. Connect a slew rate controllable signal generator to the transient load circuit input, J_{60} (TRANSIENT 1 PULSE GEN), J_{61} (TRANSIENT 2 PULSE GEN), or J_{62} (TRANSIENT 3 PULSE GEN).
3. Program the signal generator to pulse mode, set the frequency to 100Hz, ON duration to 200µs, and signal amplitude from 0V to 2V. The load transient circuit starts to turn on when the input is ~2.6V. When in doubt, connect the signal generator output to an oscilloscope set to 1MΩ termination. The slew rate of the pulse, both rising and falling, should be conservatively slow, for example, 1µs.
4. Connect a differential probe to monitor load current across the sense resistors J_{52} (ISENSE1), J_{55} (ISENSE2), or J_{59} (ISENSE3). The load current can be accurately converted to a voltage at 1A/10mV. Ensure the vertical scale of the oscilloscope is set properly to display the full amplitude of the load profile.
5. Connect a second differential probe at the V_{OUT} sense points connected to the V_{OUT} decoupling capacitors J_{15} (BUCK1 SENSE), J_{18} (BUCK2 SENSE), or J_{56} (BUCK3 SENSE).
6. Set the oscilloscope to measure the rise and fall times and maximum level of the load current. Slowly increase the signal generator amplitude and slew rate until the required load profile is achieved. For detailed setup information, see Figure 14.

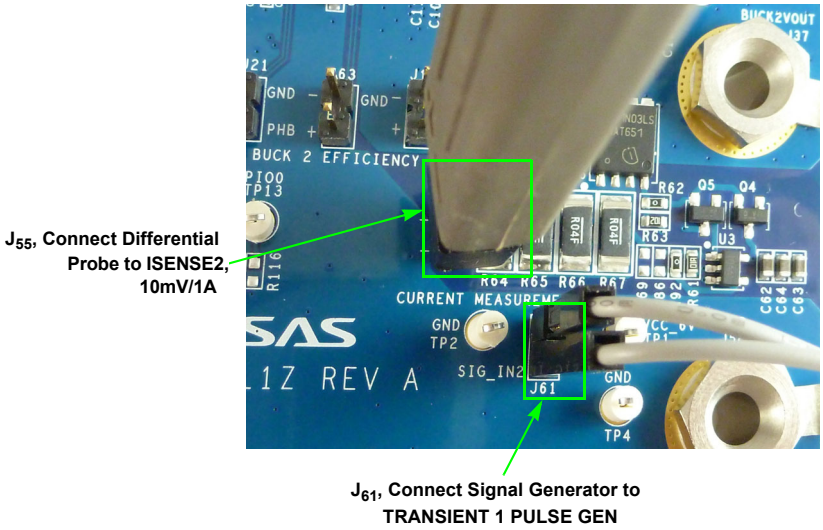

Figure 3. BUCK2 Transient Load Connection Example

1.4 Installing and Using the Evaluation Software

1. Download the Multiphase PMIC I2C Control Tool from the ISL91212A product page, double-click **AutoRun.exe**. Follow the instructions to install the *Multiphase PMIC I2C Control Tool* evaluation software.
2. Attach the USB-I^{2}C interface (ISLUSBMINIEVAL1Z) dongle to the computer using the supplied USB cable.
3. Attach the USB-I^{2}C interface dongle to J_{66} on the ISL91212AEVAL1Z evaluation board.
4. Follow the instructions in Setting Up the ISL91212AEVAL1Z, connect the power supplies, DC load, and other test equipment to the ISL91212AEVAL1Z.
5. Apply power to the ISL91212AEVAL1Z.
6. Navigate to the Start menu and select **Programs** > **Renesas** > **Multiphase PMIC I2C Control Tool**.

7. Select ISL91212 from the **Select Product** drop-down menu in the GUI.

Figure 4. Product Selection Menu and I2C Communication OK Indicator

8. Click the **Connect** button on the GUI to establish a connection between the GUI and the dongle. The LED light on the dongle turns on.
   a. The software shows a green check mark next to **I2C Communication** if a connection is detected.

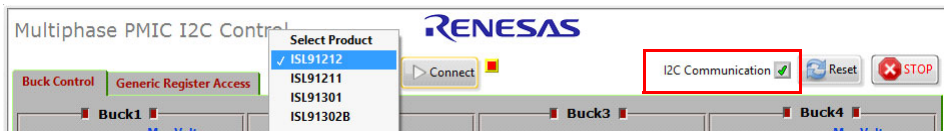

Figure 5. I2C Communication OK Indicator

   b. The software shows a red X next to **I2C Communication** if a connection is not detected. Click **Reset** to reconnect the dongle.

9. After the evaluation software establishes a connection to the USB-I^{2}C interface dongle, the software loads a blank startup script by default. It reads all the pertinent register values to show on screen.
10. Buck1, Buck2, and Buck3 are all enabled. The default DVS0 values are 1.0V for Buck 1, 1.8V for Buck2, and 1.2V for Buck3.
    a. If no fault conditions occurred during board power-up, all the fault indicators (UV, OV, OC) are clear.
    b. If fault conditions occurred during board power-up, the fault indicators are red.
11. To change the output voltage, enter the required value in voltages in the DVS0 control. Four default DVS values are loaded as part of the ISL91212A one-time programmable memory space. The user can select any of them and activate a DVS command by clicking on the DVS pointer when corresponding BUCKx_DVSCTRL bit is 0.

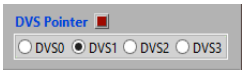

Figure 6. DVS Pointer Selection

12. Changing the **Max Voltage** controls changes the internal feedback divider between ratios of 1x, 0.8x, and 0.6x. This changes the maximum output voltage the ISL91212A can support, with a maximum of 2V through factory OTP. The smallest DVS resolution the IC and the software can support is no less than the maximum voltage divided by 1024.
13. After the evaluation software is up and running without hiccup, it polls all the registers at 2s intervals by default. Disable this feature by clearing the **Continuous Read** option.

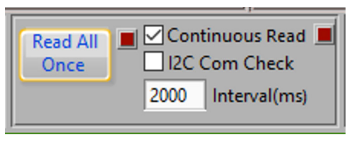

Figure 7. Continuous Read and Manual Read All Options

14. The fault indicators self-clear when the software reads the register through Continuous Read or the fault is removed. Three additional replica fault indicators (UV, OV, and OC) latch the faults so they clear only after clicking **Push to Clear** if a spurious fault condition occurs.

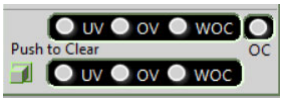

Figure 8. Fault Indicators

15. Select the **Generic Register Access** tab to write into or read from a specific register.
16. Select the register name from the drop-down menu to update the **Register Address** box with the address of the selected register.
17. To write data, enter the data to be written in the **Data In** field, then click **Write**.
18. To read data that has been written, click **Read**. The read value appears in the **Data Out** field.

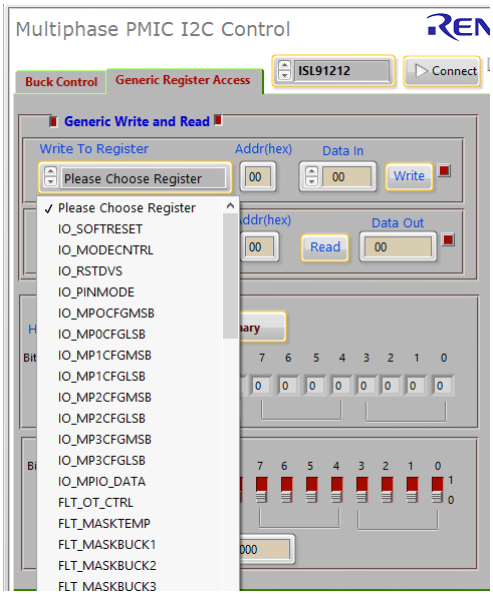

Figure 9. Generic Register Access

Note: The default switching frequency of the ISL91212A is set to 2MHz and the slew rates for both DVS and power-up/down are set to 2.5mV/µs. These settings and many other features are programmable only through an OTP request or a startup script, and are not supported by the evaluation software. For more information, contact your local Renesas sales representative.

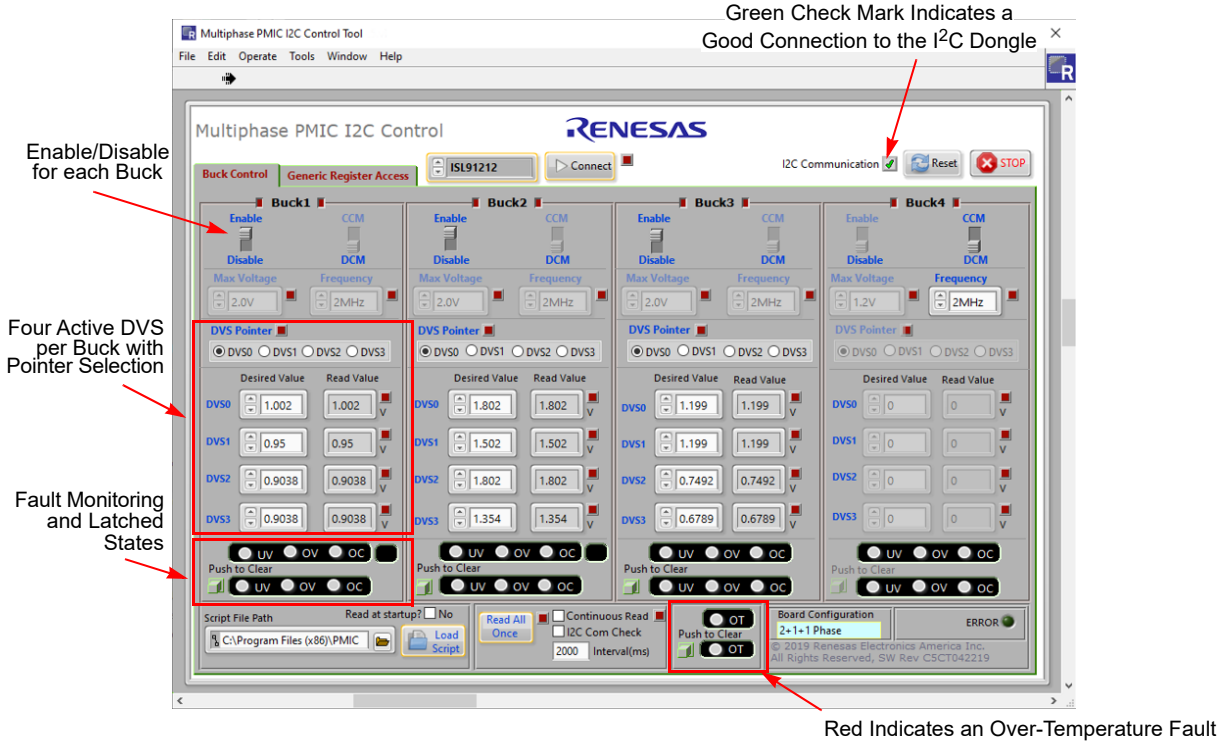

Figure 10. ISL91212A Evaluation Software Window

2. PCB Layout Guidelines

The ISL91212AEVAL1Z board is a 6-layer FR4 board. The main components are the ISL91212A and its passive filter components, test points, and connectors. The Buck inductor is located close to each phase node of the ISL91212A, and Buck output filter capacitors are populated at the output of each inductor. PVIN is distributed using a power plane on an inner layer with the Buck input filter capacitor placed in close proximity to the PVIN and PGND balls of the power stage. The AVIN filter capacitor is placed next to the ISL91212A, referenced to a quiet ground plane.

The PCB layout is a critical design step in ensuring the designed converter works under optimum conditions. For the ISL91212A, the power loop is composed of the inductor, output capacitors, phase node, and PGND pins. Keep this loop as short as possible. The connecting traces among them should be direct, short, and wide. To minimize the noise coupling, keep remote sense signals away from phase node traces, and do not route them under the inductor in an adjacent layer. Place the input capacitor as close as possible to the PVIN and PGND pins, and there should be a large unbroken ground plane that should connect all the decoupling capacitors together.

Heat is dissipated mainly through the GND and PHASE plane vias under the IC. To maximize thermal performance, use as much copper area as possible connecting to these vias. In addition, a solid ground plane is helpful for better EMI performance.

2.1 Key Layout Strategies

- Place input capacitors as close as possible to their respective PVIN and PGND pins to minimize parasitic loop inductance.
- Route phase nodes with short, wide traces and avoid any sensitive nodes.
- Route the remote sense lines directly to the load using small, low inductance capacitors at the load for bypassing.
- Place output capacitors close to the inductors with a low impedance path to the PGND pins.
- Prevent digital and phase nodes from intersecting the VIN_FILT, VOUT, and RTN lines.
- Create a PGND plane on the second layer of the PCB below the power components and bumps carrying high switching currents.

2.2 Evaluation Board

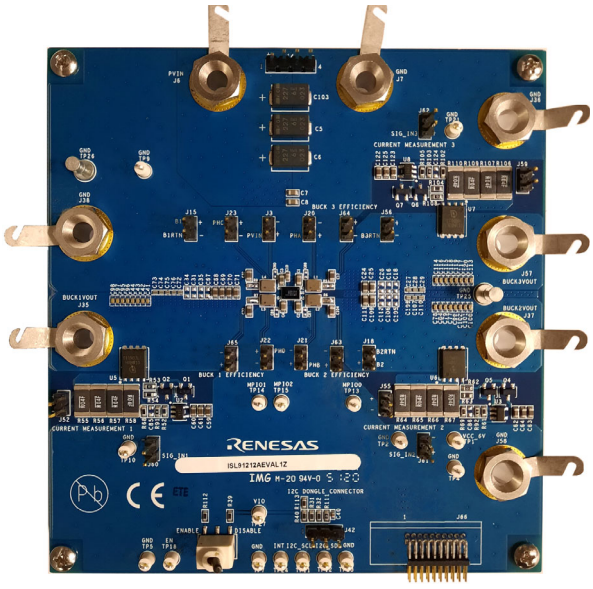

Figure 11. ISL91212AEVAL1Z Top View

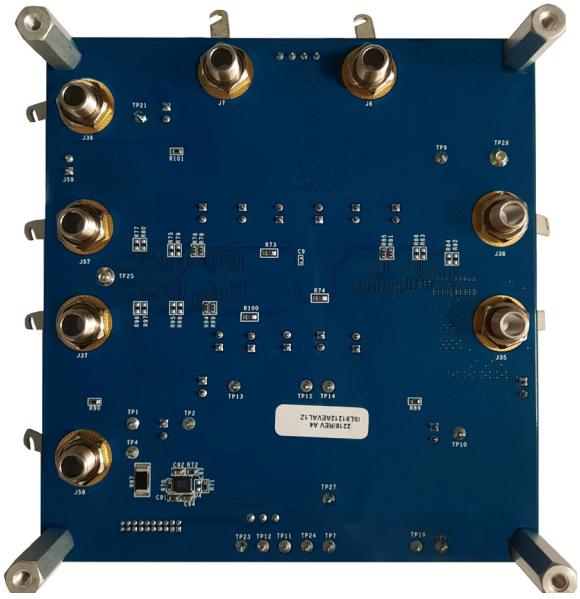

Figure 12. ISL91212AEVAL1Z Bottom View

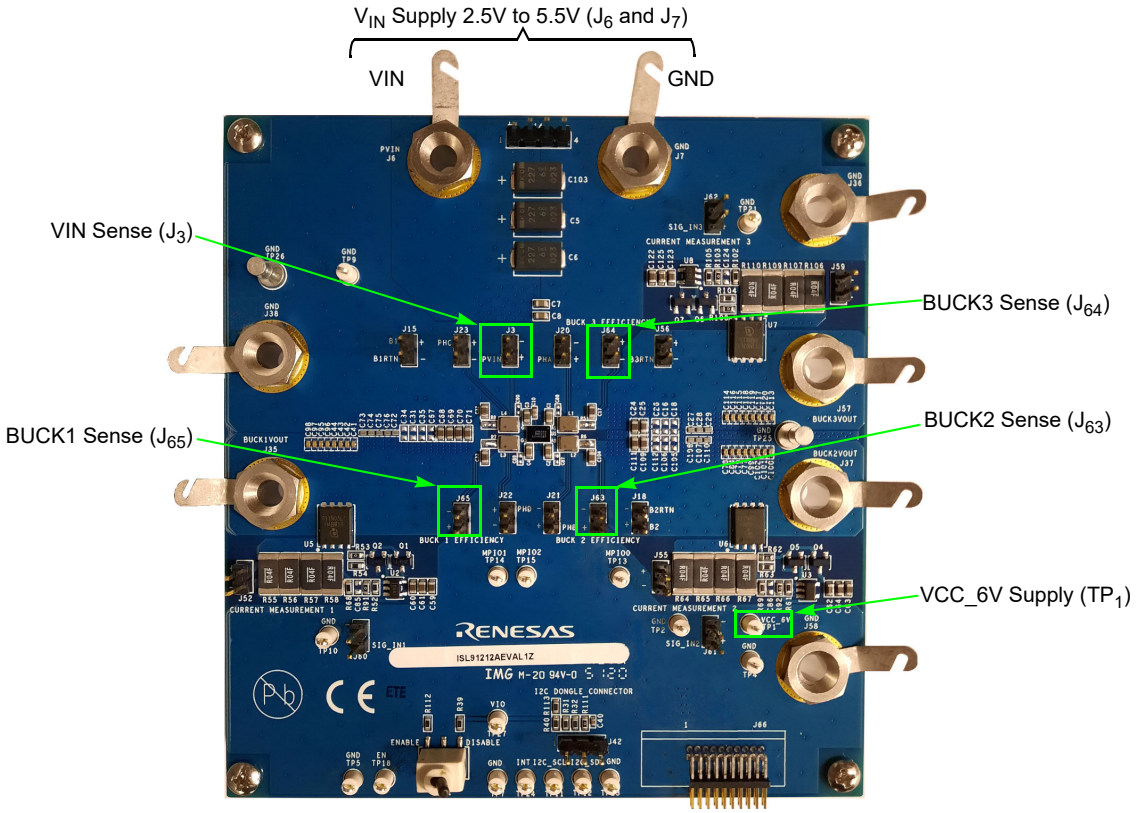

Figure 13. ISL91212AEVAL1Z Efficiency Measurement Connections

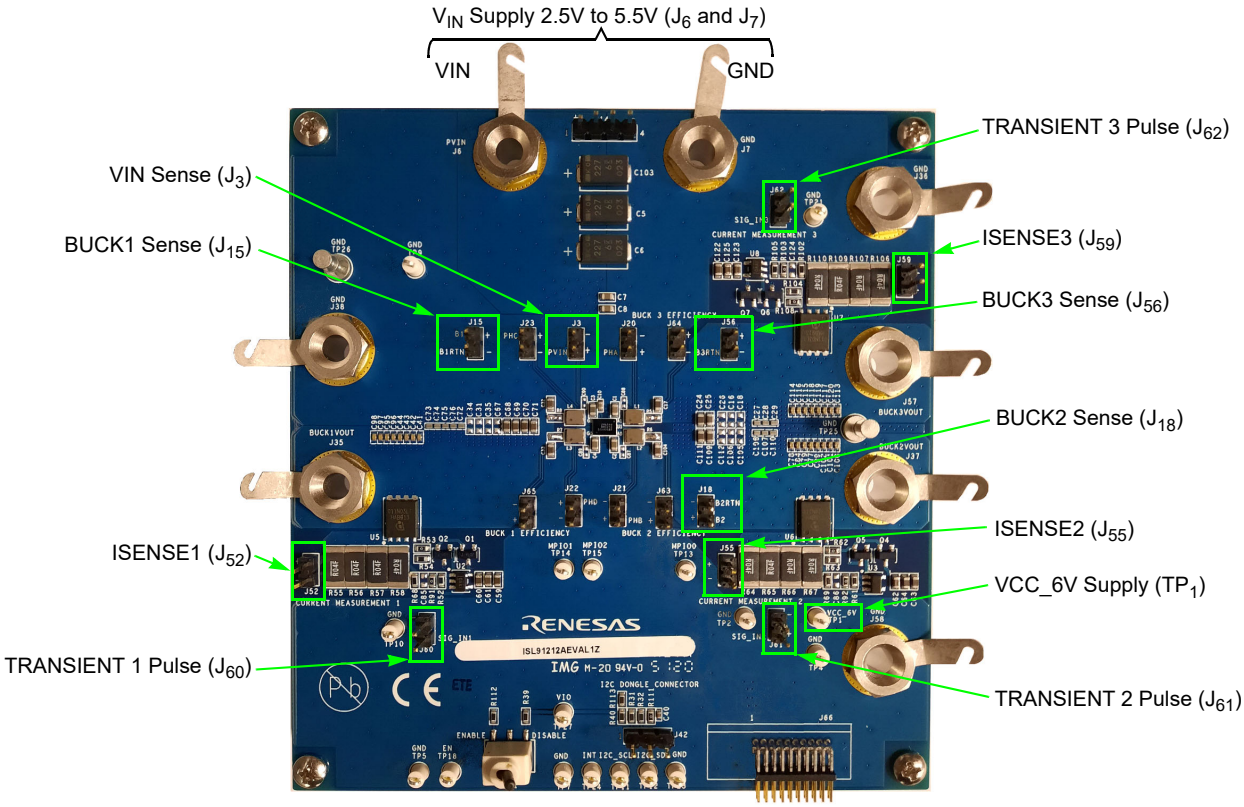

Figure 14. ISL91212AEVAL1Z Load Transient Measurement Connections

2.3 Schematics

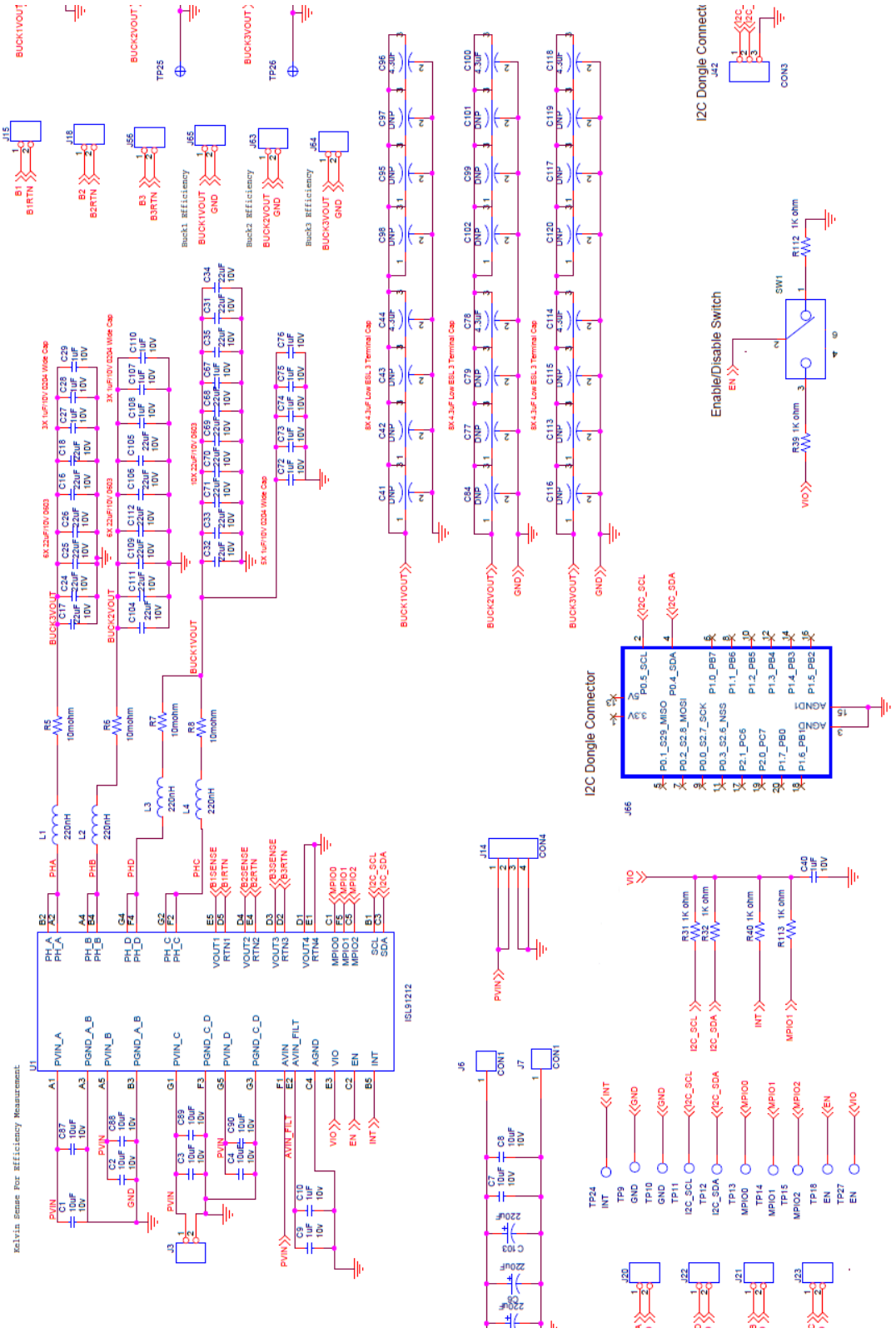

Figure 15. ISL91212AEVAL1Z Schematic - Page 1[1]

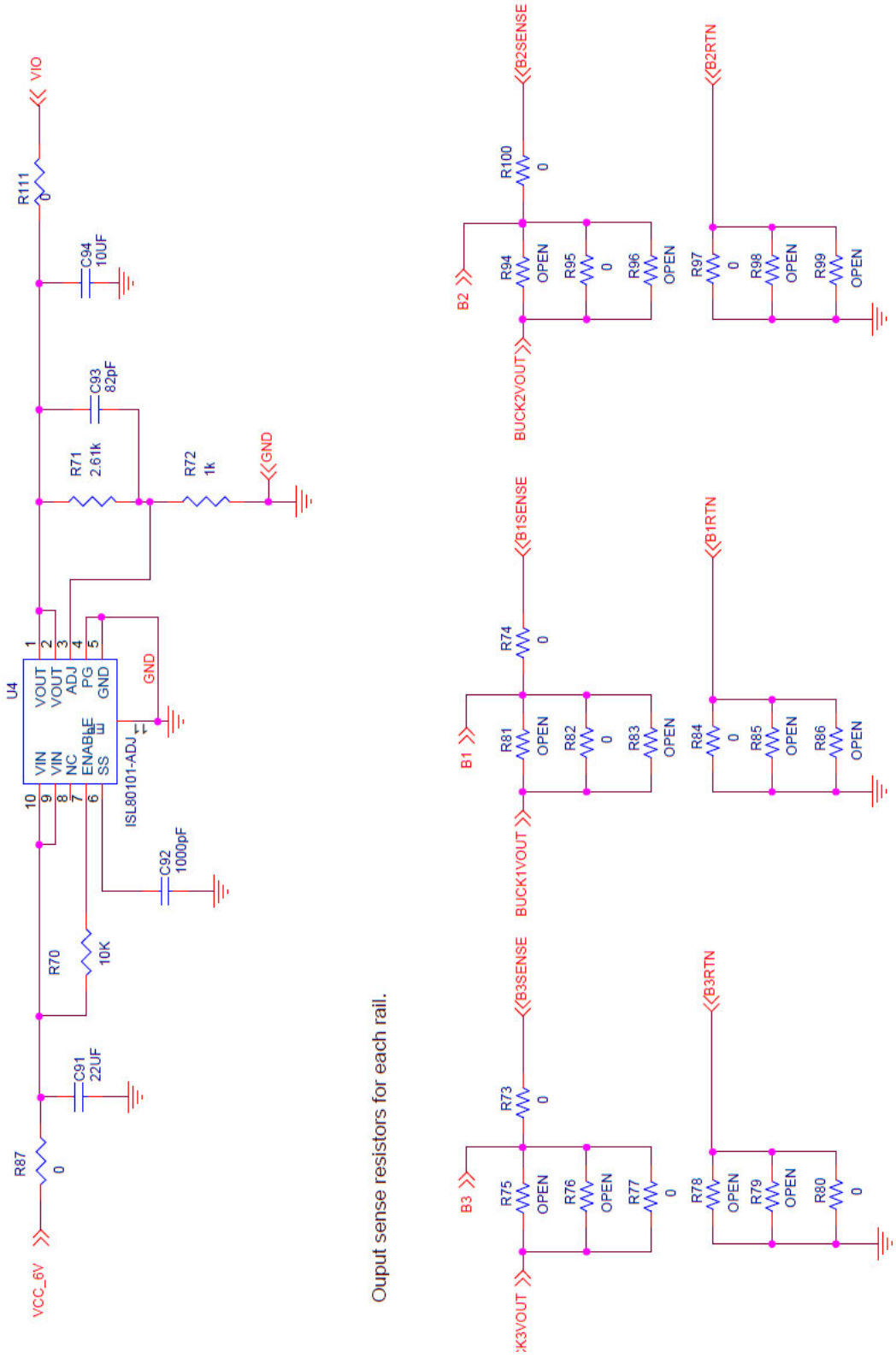

Figure 16. ISL91212AEVAL1Z Schematic - Page 2

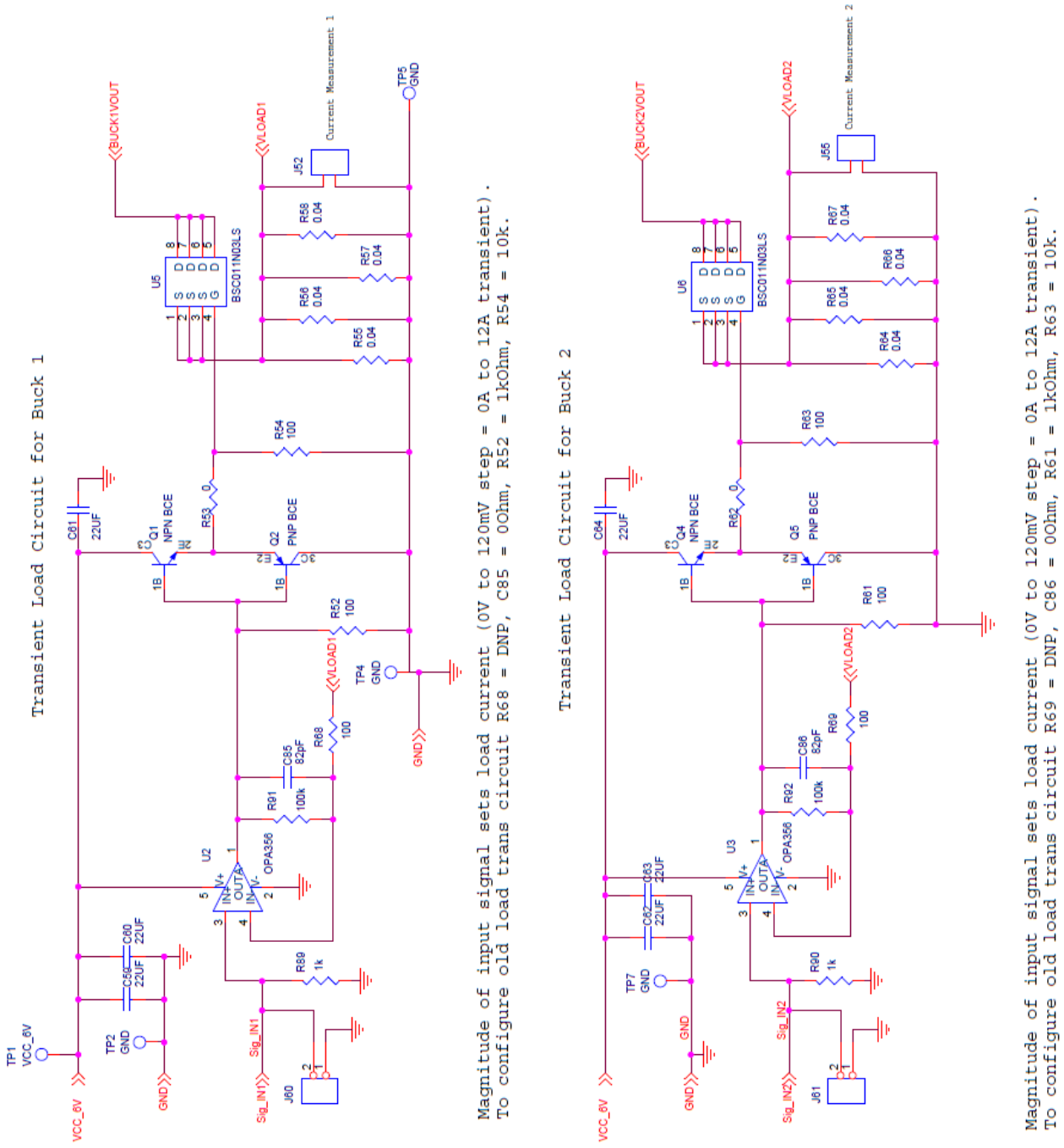

Figure 17. ISL91212AEVAL1Z Schematic - Page 3

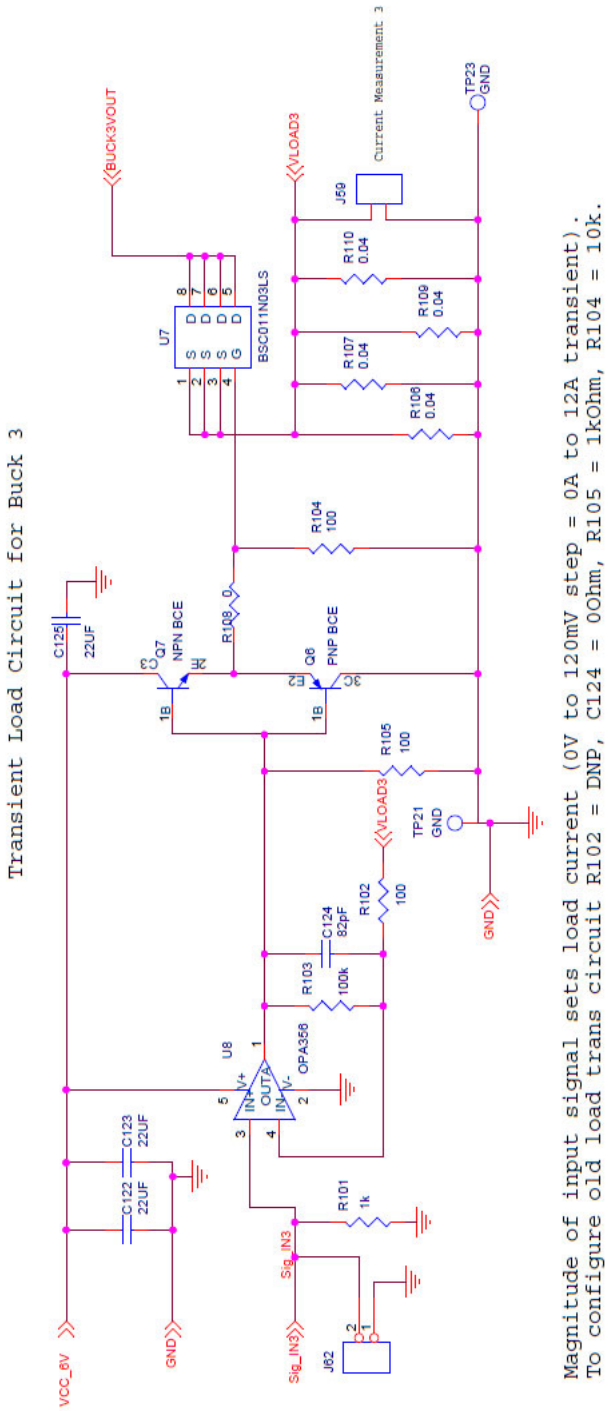

Figure 18. ISL91212AEVAL1Z Schematic - Page 4

1. For the component values in the schematics, see Bill of Materials.

2.4 Bill of Materials

Qty	Reference Designator[1]		Description	Manufacturer	Manufacturer Part Number
	Top Components	Bottom Components			
1	-	C92	1000pF, 50V, X7R, 0603	Taiyo Yuden	HMK107B7102KA-T
1	C40	-	1µF, 10V, X5R, 0402	Taiyo Yuden	LMK105BJ105KV-F
24	C41, C42, C43, C44, C98, C95, C97, C96, C84, C77, C79, C78, C102, C99, C101, C100, C116, C113, C115, C114, C120, C117, C119, C118	-	4.3µF Multi-Terminal, 4V, X5R, 0402	Murata	LLD154R60G435ME01
7	C1, C2, C3, C4, C7, C8	C94	10µF, 10V, X5R, 0603	Taiyo Yuden	LMK107BBJ106MAHT
1	C10	-	10µF, 10V, X5R, 0402	Samsung Electronics	CL05A106MP5NUNC
22	C17, C24, C25, C104, C111, C109, C32, C33, C71, C70, C69, C68, C60, C61, C62, C64, C123, C125, C59, C63, C122	C91	22µF, 10V, X5R, 0603	TDK	C1608X5R1A226M080AC
11	C27, C28, C29, C107, C108, C110, C72, C73, C74, C75, C76	-	1uF, 6.3V, X5R, 0204	Taiyo Yuden	JWK105BJ105MP-F
3	C5, C6, C103	-	220µF, 6.3V, Polymer Tant, D Case	KEMET	T520D227M006ATE040
16	R53, R62, R108, R91, R92, R103, R111	R73, R74, R78, R76, R85, R81, R99, R94, R100	0Ω, 1/10W, 0603	YAGEO	RC0603JR-070RL
1	-	R87	RES SMD 0.0Ω JUMPER 3/4W 2010	Stackpole	RMCF2010ZT0R00
12	R55, R56, R57, R58, R64, R65, R66, R67, R106, R107, R109, R110	-	0.04Ω, 1%, 1W, 2010	YAGEO	PE2512FKE070R04L
4	R5, R6, R7, R8	-	Jumper, Solder short	Any	Any
6	R52, R54, R61, R63, R104, R105	-	100Ω, 1%, 1/10W, 0603	YAGEO	RC0603FR-07100RL
10	R31, R32, R39, R40, R112, R113	R72, R89, R90, R101	1.0kΩ, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF1001V
1	-	R71	2.61kΩ, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF2611V
1	-	R70	10kΩ, 1%, 1/10W, 0603	YAGEO	RC0603FR-0710KL
3	R68, R69, R102	-	100Ω, 1%, 1/10W, 0603	Panasonic	ERJ-3EKF1000V
4	L1, L2, L3, L4	-	0.22µH, 12mΩ, 6.6Asat, 2520 Inductor	Cyntec	HMQR25201T-R22MSR
3	Q1, Q4, Q7	-	TRANS NPN 40V 0.2A SOT-23	Fairchild	MMBT3904
3	Q2, Q5, Q6	-	TRANS PNP 40V 0.2A SOT-23	Fairchild	MMBT3906

Qty	Reference Designator[1]		Description	Manufacturer	Manufacturer Part Number
	Top Components	Bottom Components			
8	J6, J7, J35, J36, J37, J38, J57, J58	-	CONN BANANA JACK THREADED 12AWG	Cinch Connectivity	108-0740-102
17	TP1, TP2, TP4, TP5, TP7, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP18, TP21, TP23, TP24, TP27	-	TEST POINT PC MINI .040"D WHITE	Keystone	5002
17	J3, J15, J18, J20, J21, J22, J23, J52, J55, J56, J59, J60, J61, J62, J65, J63, J64	-	2 Pin Header, 100 mil spacing	FCI	77311-118-02LF
1	J42	-	3 Pin Header, 100 mil spacing	Wurth	61300311121
1	J66	-	Right angle connector	Harwin Inc.	M50-3901042
2	TP25, TP26	-	Turret Binding Post	Keystone	1514-2
1	U1	-	ISL91212AIIZ, 0.5mm Pitch WLCSP	Renesas	ISL91212
3	U2, U3, U8	-	IC OPAMP VFB 200MHZ RRO SOT23-5	Texas Instruments	OPA356AIDBVR
1	-	U4	IC REG LDO ADJ 1A 10DFN	Renesas	ISL80101IRAJZ
3	U5, U6, U7	-	MOSFET N-CH 30V 100A 8TDSON	Infineon	BSC011N03LSATMA1
1	J14	-	4 Pin Header, 100 mil spacing	Wurth	61300411121
1	SW1	-	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-NONE-ON, ROHS	ITT INDUSTRIES/ C&K DIVISION	GT11MSCBE
0	C85, C86, C124, C93	-	82pF, NP0, 0603, DNP	Taiyo Yuden	QVS107CG820JCHT
0	C87, C88, C89, C90	C9	Capacitor, 0402, DNP	any	any
0	C26, C16, C18, C112, C106, C105, C67, C35, C31, C34	-	22µF, 10V, X5R, 0603, DNP	any	any
0	-	R75, R77, R79, R80, R82, R83, R84, R86, R95, R96, R97, R98,	Resistor, 0603, DNP	any	any

1. Components highlighted in red are DNP.

2.5 Board Layout

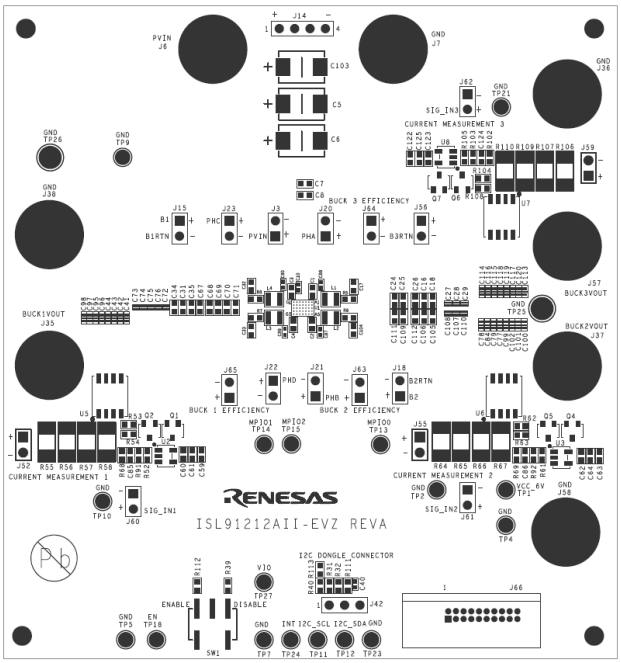

Figure 19. Top Silkscreen Layer

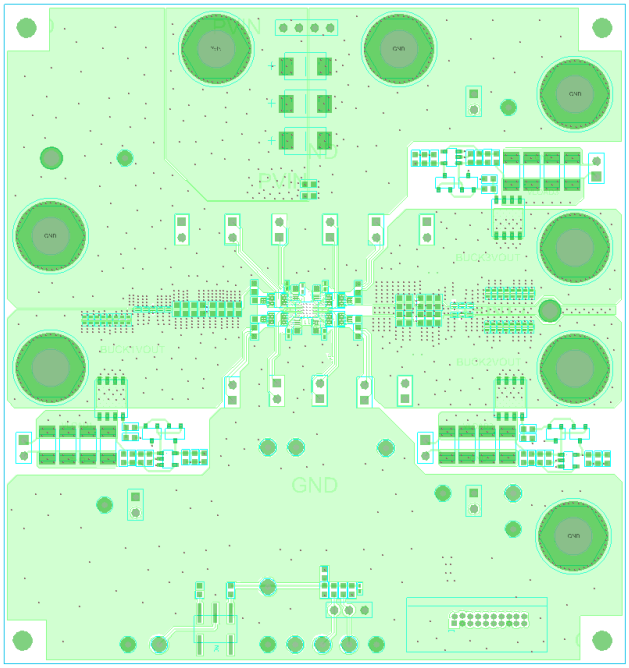

Figure 20. Top Layer

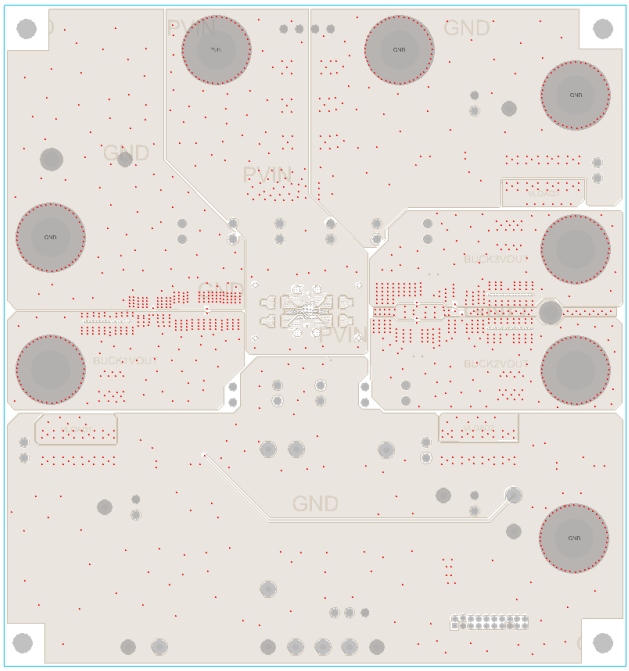

Figure 21. Layer 2 (PVIN Plane)

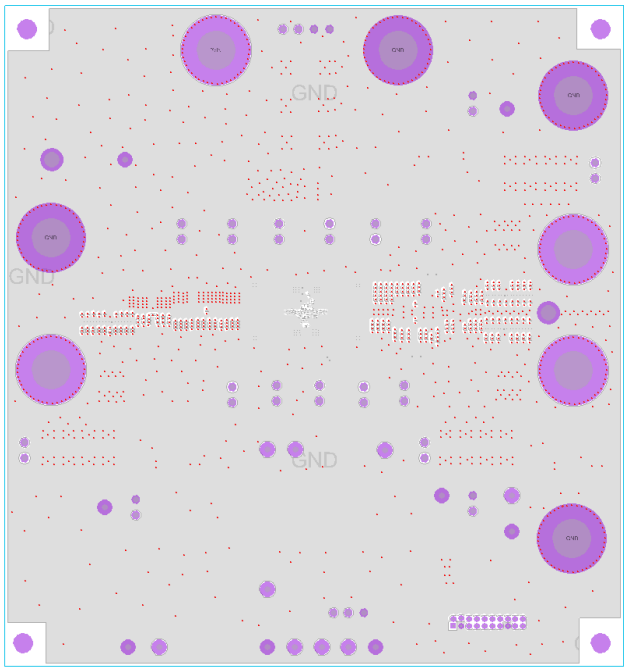

Figure 22. Layer 3 (GND Plane)

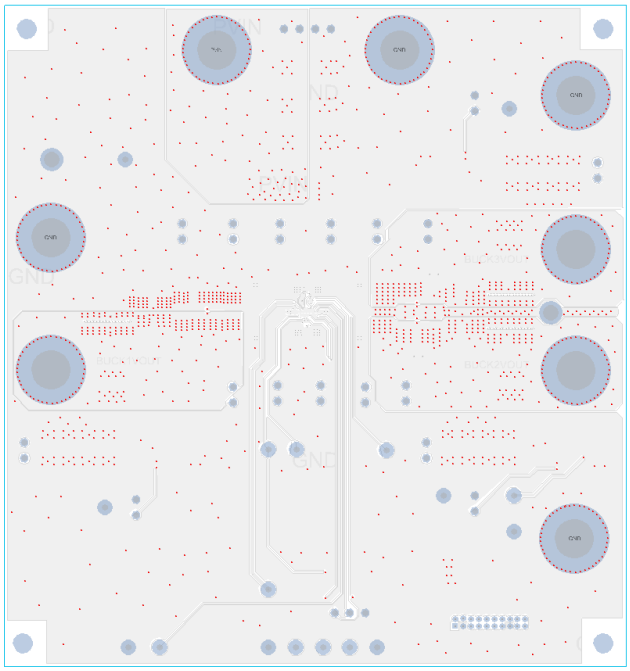

Figure 23. Layer 4 (IO Communications)

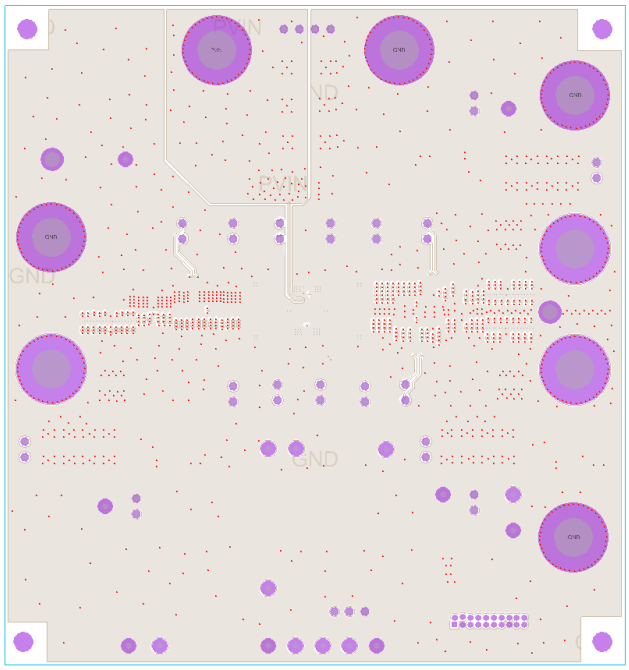

Figure 24. Layer 5 (GND Plane)

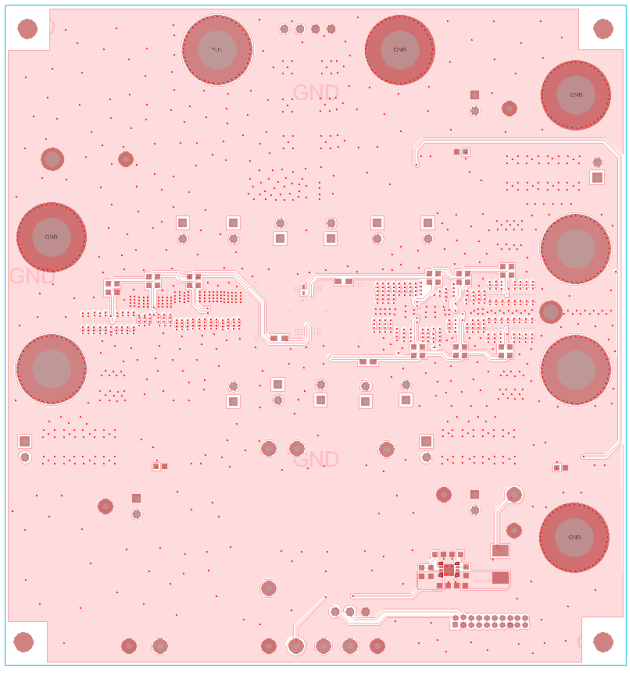

Figure 25. Bottom Layer (Remote Sense Lines)

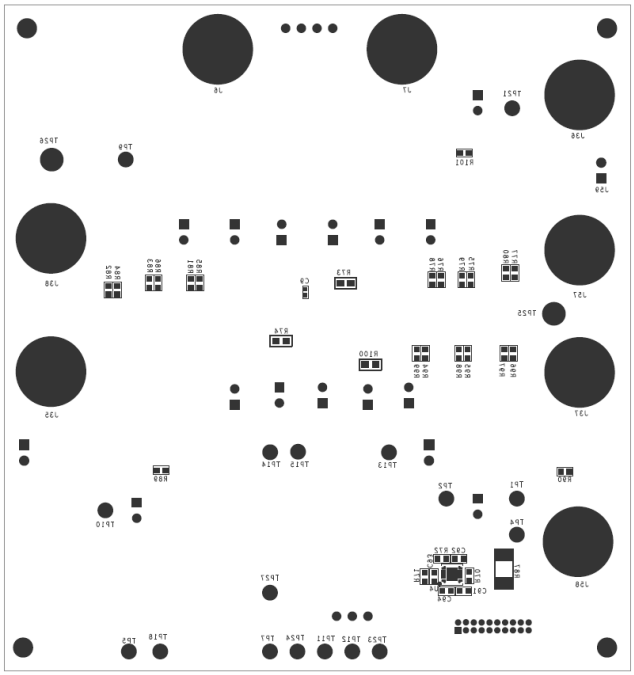

Figure 26. Bottom Silk Screen Layer

3. Typical Performance Curves

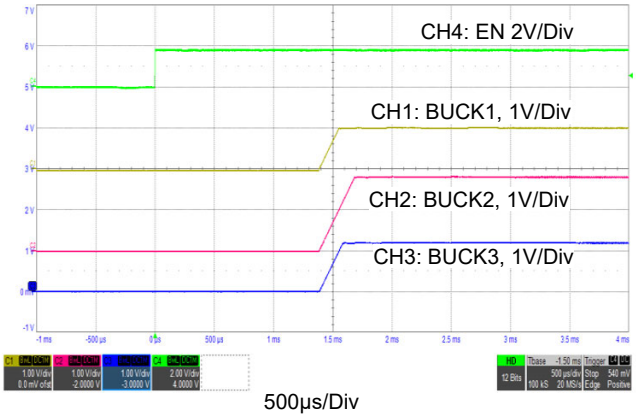

Figure 27. Startup by EN, V_{OUT1} = 1.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V

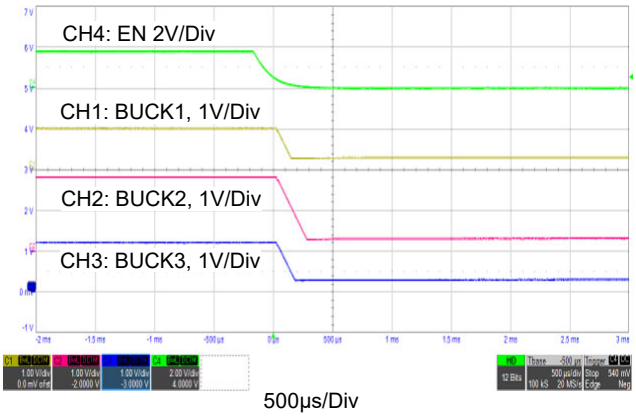

Figure 28. Shutdown by EN, V_{OUT1} = 1.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V

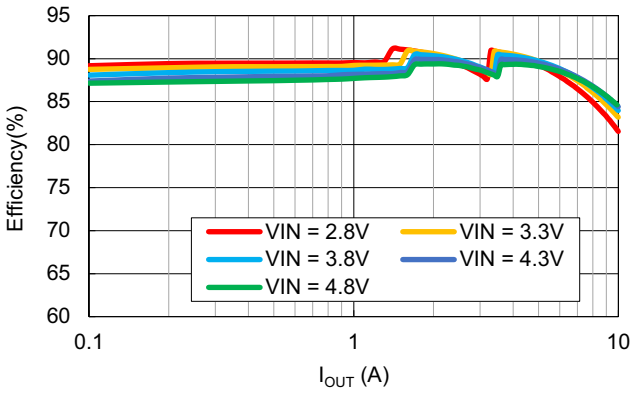

Figure 29. Dual-Phase Efficiency (V_{OUT} = 1V), Continuous Load Sweep (0.1A to 10A), f_{sw} = 2MHz

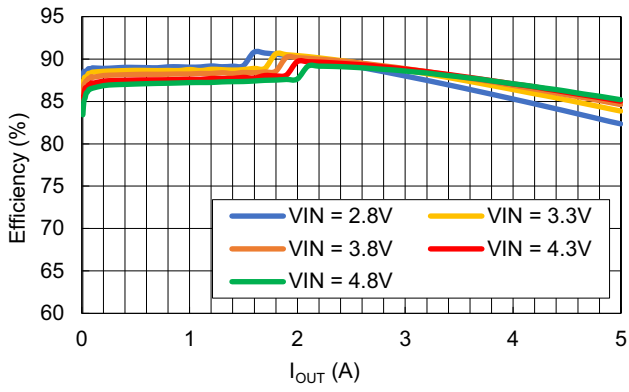

Figure 30. Single-Phase Efficiency (V_{OUT} = 1V), Continuous Load Sweep (0.01A to 5A), f_{sw} = 2MHz

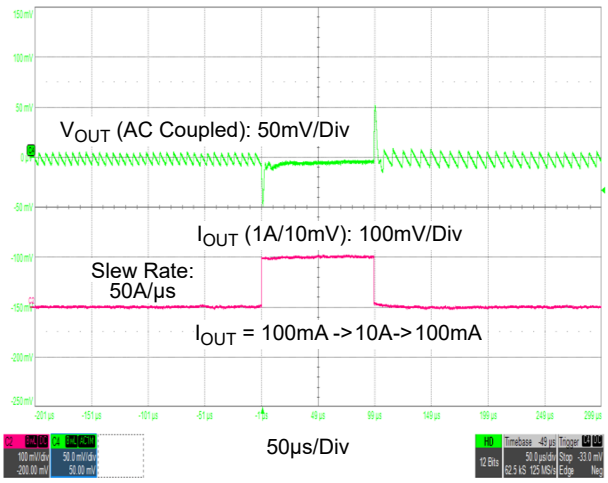

Figure 31. Dual-Phase Load Transient (10A/200ns) V_{IN} = 3.8V, V_{OUT} = 1V, f_{SW} = 2MHz, Load Step Slew Rate = 50A/µs, 0.1A to 10A

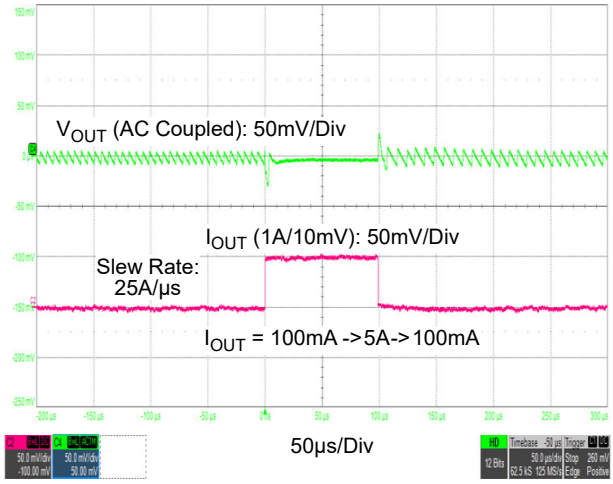

Figure 32. Single-Phase Load Transient (5A/200ns) V_{IN} = 3.8V, V_{OUT} = 1V, f_{SW} = 2MHz, Load Step Slew Rate = 25A/µs, 0.1A to 5A

4. Ordering Information

Part Number	Description
ISL91212AEVAL1Z	ISL91212A evaluation board

5. Revision History

Rev.	Date	Description
1.00	Jun 28, 2023	Applied new template. Updated Table 1. Updated the Quick Start Guide section. Added the Buck Output Voltage Configuration section. Updated the Setting Up the ISL91212AEVAL1Z section. Updated the Measuring Efficiency section. Updated Figures 1, 2, 3, 10-27, 30, and 31. Updated the Installing and Using the Evaluation Software section. Updated the PCB Layout Guidelines section. Added note to schematics. Updated Bill of Materials
0.00	Oct 8, 2018	Initial release

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