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1. Introduction

The P9242-R Wireless Power Receiver (Tx) is an integrated circuit (IC) consisting of multiple high-power blocks and noise-sensitive circuits controlled by a microprocessor. When implementing the application circuit on a printed circuit board (PCB), there are often tradeoffs associated with managing the critical current paths. In order to optimize the design, components should be placed on the circuit board based on circuit function to guarantee best performance. The thermal management of the P9242-R is also important to the product's performance and should be optimized when designing the PCB. The following guidance should be used in order to place the components in order of priority based on operation.

There are three main categories of circuitry:

- Power circuits
- Sensitive circuits
- Non-sensitive circuits

1.1 Key Points for Optimal Layout

- Route the power connections wide and on the same side of the PCB as the P9242-R (≥ 100mils).
- Use the layer under the P9242-R side of the board as a solid ground plane.
- Connect the exposed thermal pad (EP) in the center of the P9242-R to all other layers with an array of 4x5 10 mil vias.
- Avoid unnecessary layer transitions of the AC power connections (LC node, LC tank driving FETs, and GND).
- Place the P9242-R as close as possible to the center of the board. Avoid placing it along the PCB edge.
- Connect as much copper as possible to every pin of the P9242-R, including pins that do not carry high current.
- Use low ESR resonance capacitors (Cs/Cd) to decrease losses in the LC and AC1 current path (C0G preferred).
- Place components in the following order:
    - POWER CIRCUITS – NON H BRIDGE POWER STAGE:
        - CIN, CBOOST: Place all IC pin input voltage capacitors and boost capacitors close to their related pins (VIN, LDO33, LDO18, VDDIO, BST_BRG1, BST_BRG2, DRV_VIN, VBRG_IN:).
        - Buck Regulator L, Cout: Place the inductor as close as possible to the switch node pin to reduce the switching noise of that node. Place the buck regulator inductance and output capacitance such that they form the smallest possible current loop to minimize EMI transmissions.
    - SENSITIVE CIRCUITS – VOLTAGE AND CURRENT MEASUREMENT:
        - Current Sense: Place the bridge input current sense resistor directly in the current path to the tank FET drivers. Place the filtering components close to the sense resistor and tightly together.
        - Current Demodulation: Place the current demodulation circuit components tightly together and close to their related IC pins (ISNS_OUT, IDEMI).
        - Voltage Demodulation: Place the voltage demodulation circuit components tightly together and close to their related IC pin (VDEM1).
        - Q Measurement: This circuit lowers the voltage to the LC tank during Q measurement (for FOD detection purposes). The circuit consists of the resistor divider R45, R33 which reduce the Vin and Q6. Q6 shorts out the Vin-to-LC-tank resistor during normal operation. Place the R45, the top of the resistor divider, directly above the FET it is connected to (Q2). Place R33 directly below the FET. Make these traces wide and short to avoid corrupting the Q measurement.
    - POWER CIRCUITS – H BRIDGE POWER STAGE:
        - H Bridge: Place H bridge FETs (Q1, Q4) and LC tank capacitance (C20, C23, C24, C25) close to each other, to form a small current loop, to avoid EMI emissions.
        - H Bridge Cin: Place the V_BRG FET-H-Bridge capacitors such that the traces are short. This is the large DC and AC current path.
    - SENSITIVE CIRCUITS – FET GATE DRIVER COMPONENTS:
        - Gate driver circuit: Place the Low Side FET Gate and High Side Gate Rs close to their respective pins (GH_BRG1, 2, GL_BRG1, 2). and connect the Output RC Snubbers directly onto their respective the H Bridge switch nodes.
        - Gate driver traces: Running under the H Bridge switch nodes should be avoided. Run these traces under the relatively quiet VBRG node instead. Place a ground layer between these traces and the top signal level. Surround these traces with the ground plane to provide a tight loop AC signal return path to avoid EMI noise.

2. Tx Power Circuits

The main power circuit of the P9242-R device includes the current sense resistor, the four FETs of the H bridge resonant tank driver, and the resonant tank. Secondary power circuits are the VCC5V, LDO33, and LDO18 regulators.

Figure 1. Schematic with Main Power Path (Orange) and Main (Noisy) AC Power Loops (Red)

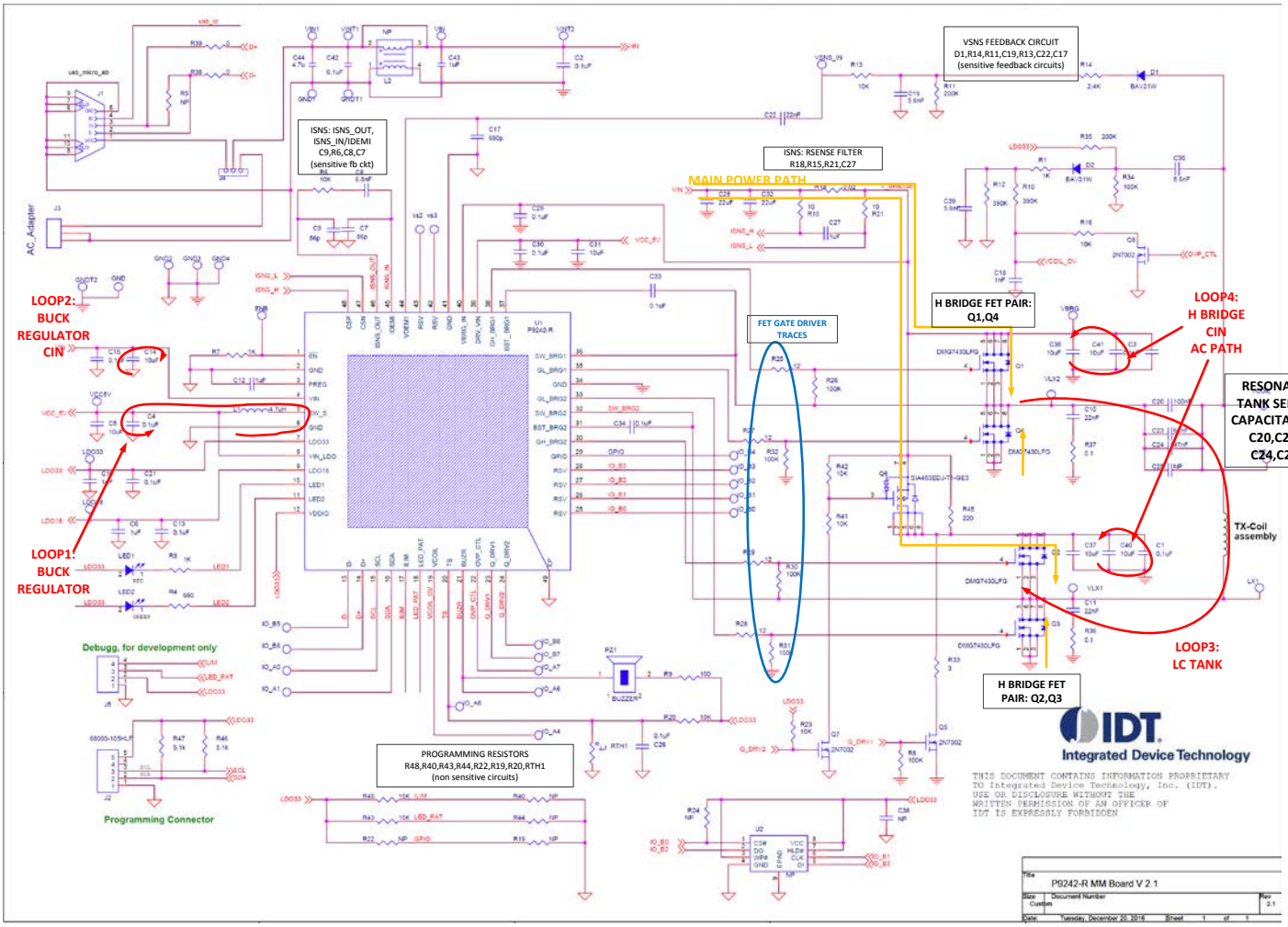
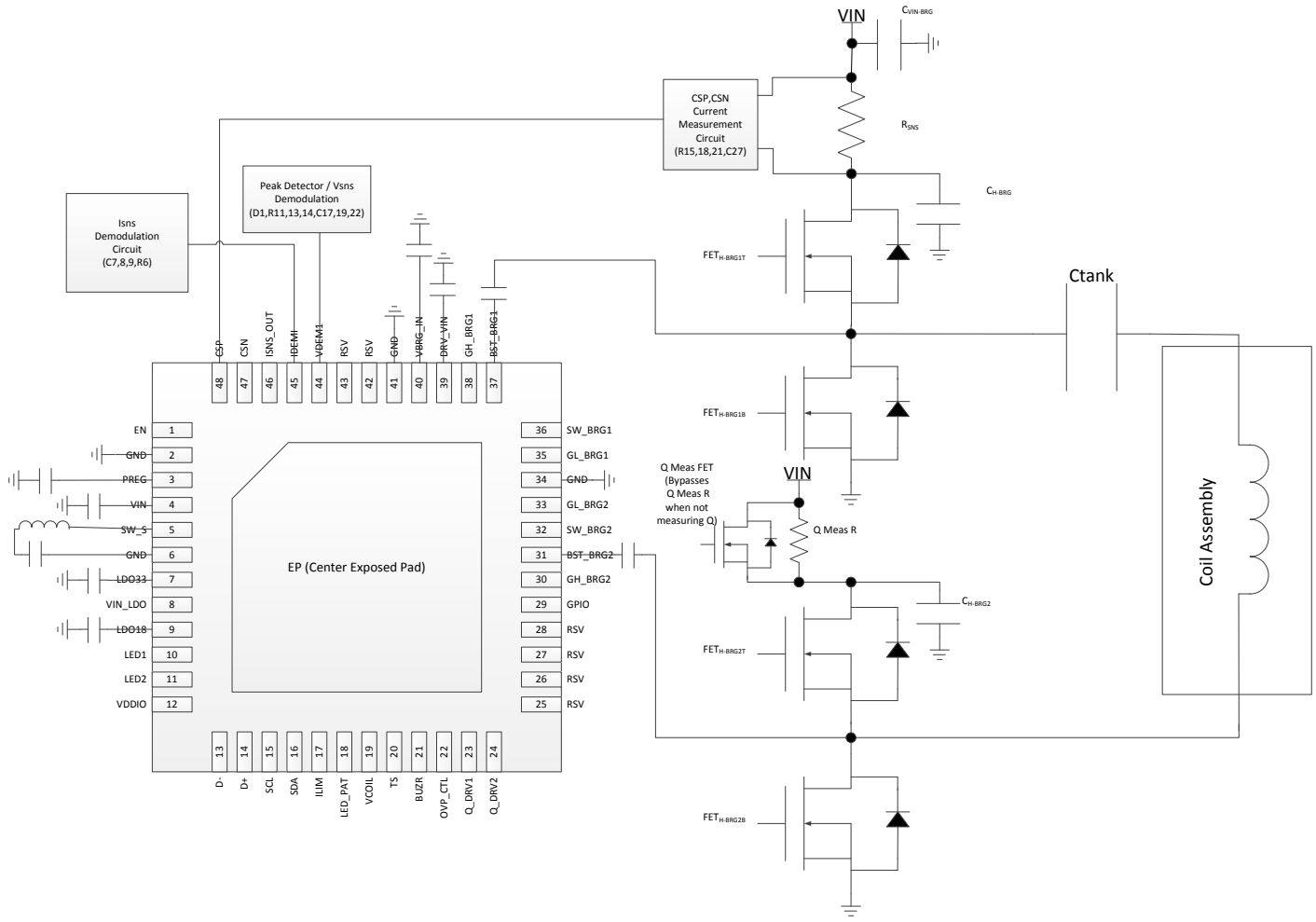
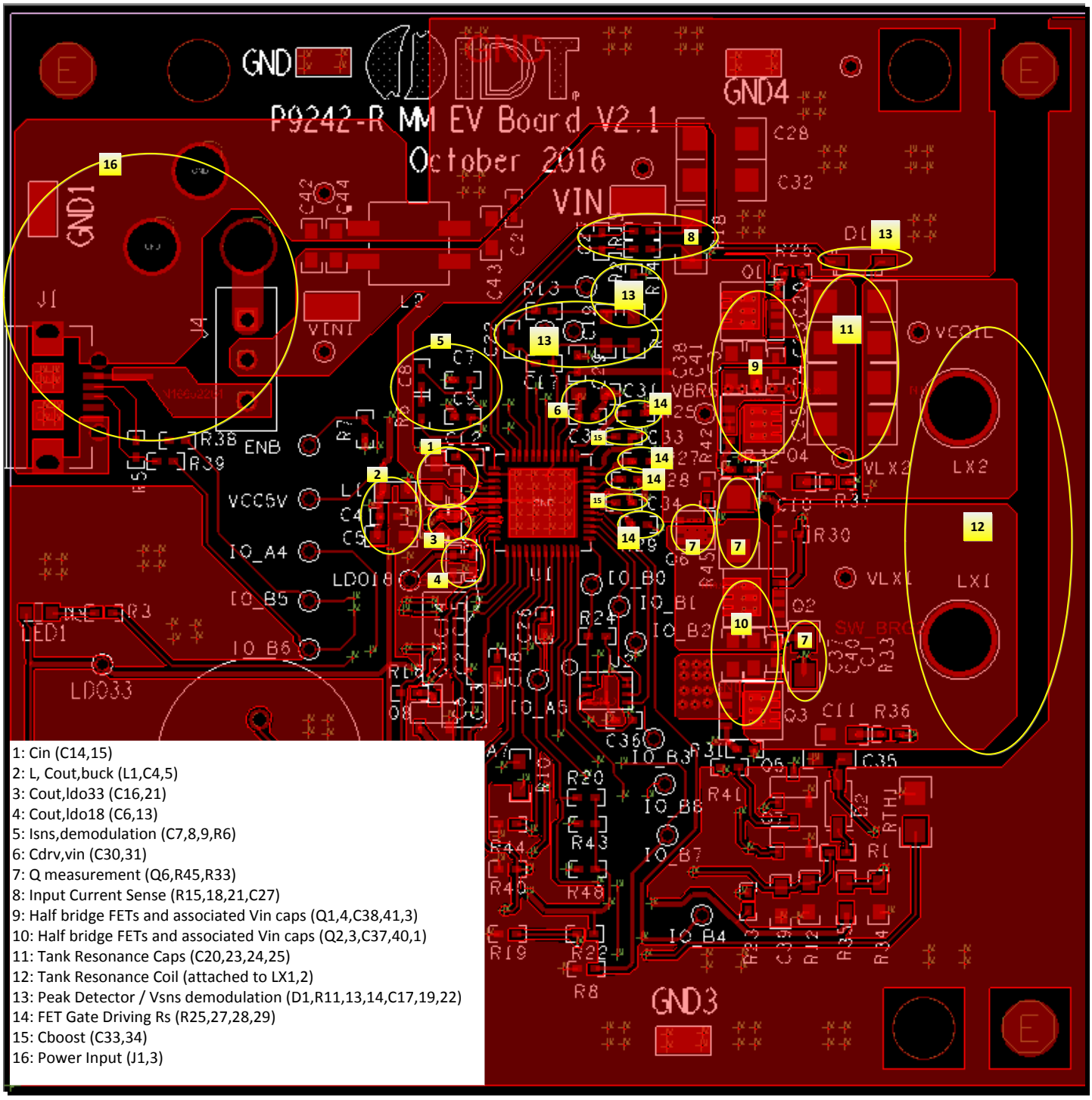


Figure 2. Recommended Orientation for the P9242-R and Generic Placement Guide for Select Critical Components



Recommendation: Once the final shape of the production or development PCB has been determined and the connection points for the power transfer coil (L_{TX}) have been chosen, place the P9242-R on the board as close to the center of the PCB as possible, taking into consideration the mechanical requirements of the system under design. Its orientation should be determined based on the ability to route connections and place the required components in the following order of priority. First place the input and boost capacitors as close to their respective pins in this order of priority: VIN, LDO33, LDO18, BST_BRG1, BST_BRG2, DRV_VIN, and VBRG_IN. The main power current path the connection from VIN through the sense resistor (R_{SNS}), through 1 of the two half bridge power FETs ($FET_{H\text{-}BRG1T,1B}$), through the tank capacitor (Ctank), through the Tx coil (Coil Assembly) and out through 1 of the other half bridge power FETs ($FET_{H\text{-}BRG2T,2B}$). The above figure represents the optimal orientation of the P9242-R relative to the other main components. Not all necessary connections are shown in this figure. For a complete diagram of the recommended connections, see the schematic in Section 5. Trace widths are not to scale.

Figure 3. Actual Placement for the P9242-R EVK. Select Critical Components are Circled in Yellow

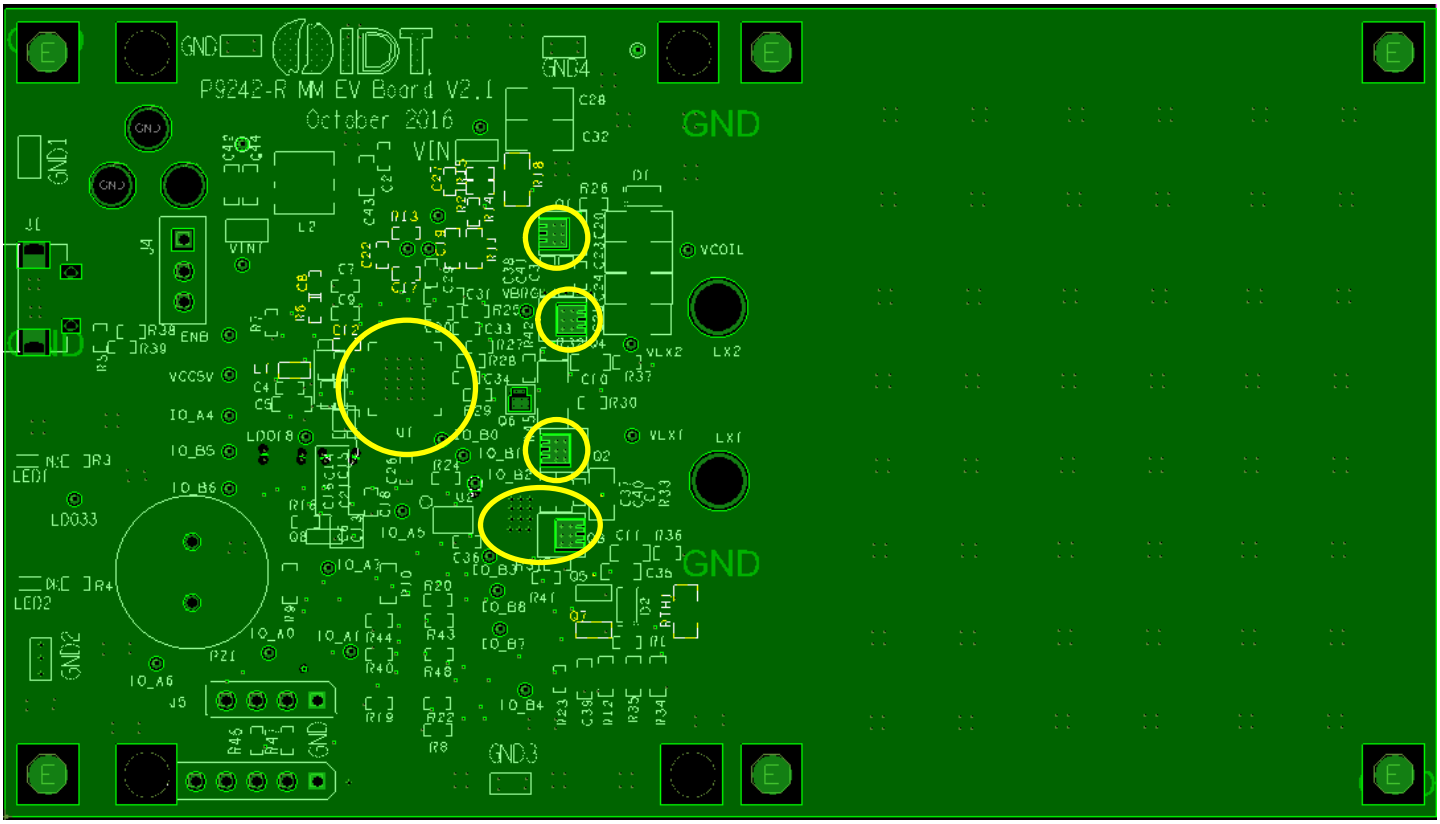


There are many things to take note of on this top layer with respect to creating an optimal layout (notes refer to the listing embedded in Figure 3):

Closeness of Cin and Cboost caps to their respective pins (notes 1,6,15)
Tight (small) AC loops of FETs in relation to the LC tank (notes 9-12)
Tight loops of the FETs in relation to the H bridge Cin capacitors (notes 9,10)
Closeness of current and voltage demodulation to the IC (notes 5,13)

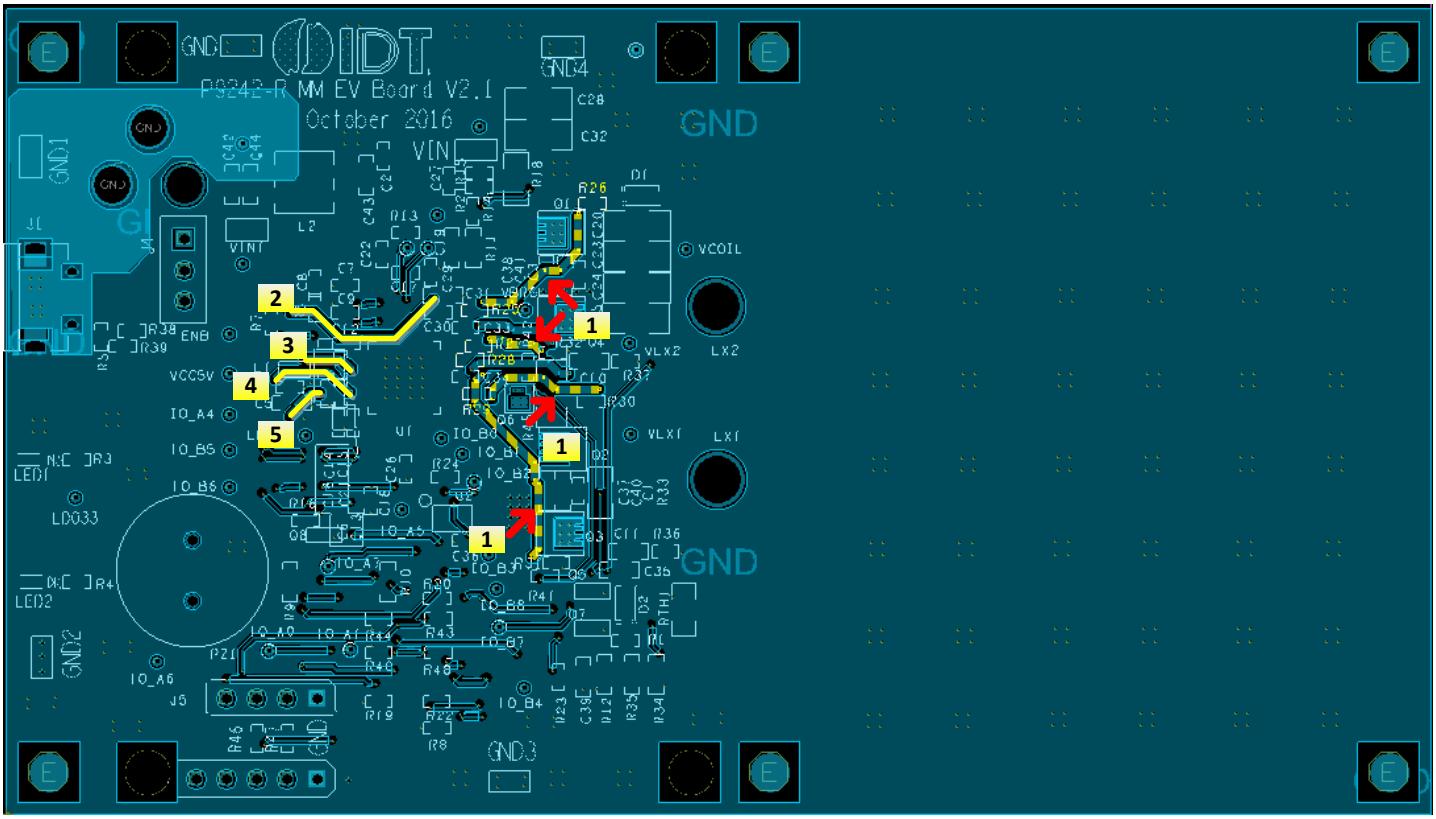
Closeness of H bridge FET gate driver resistors to the IC (note 14)
Tight loop of LC of 5V switching regulator for low loop inductance/noise (note 2)
Closeness of L to its respective switching node for minimum noise (note 2)
The H bridge FETs produce the most heat. Therefore, FET GND pads are connected to GND with the maximum number of 10mil vias for the best thermal performance.

Figure 4. P9242-R Physical Layout from P9242-R-EVK Evaluation Board (2nd Layer (L1)), Solid GND Plane with Minimal Connections, Direct Contact to GND Plane 10mil Vias for Thermal Transfer



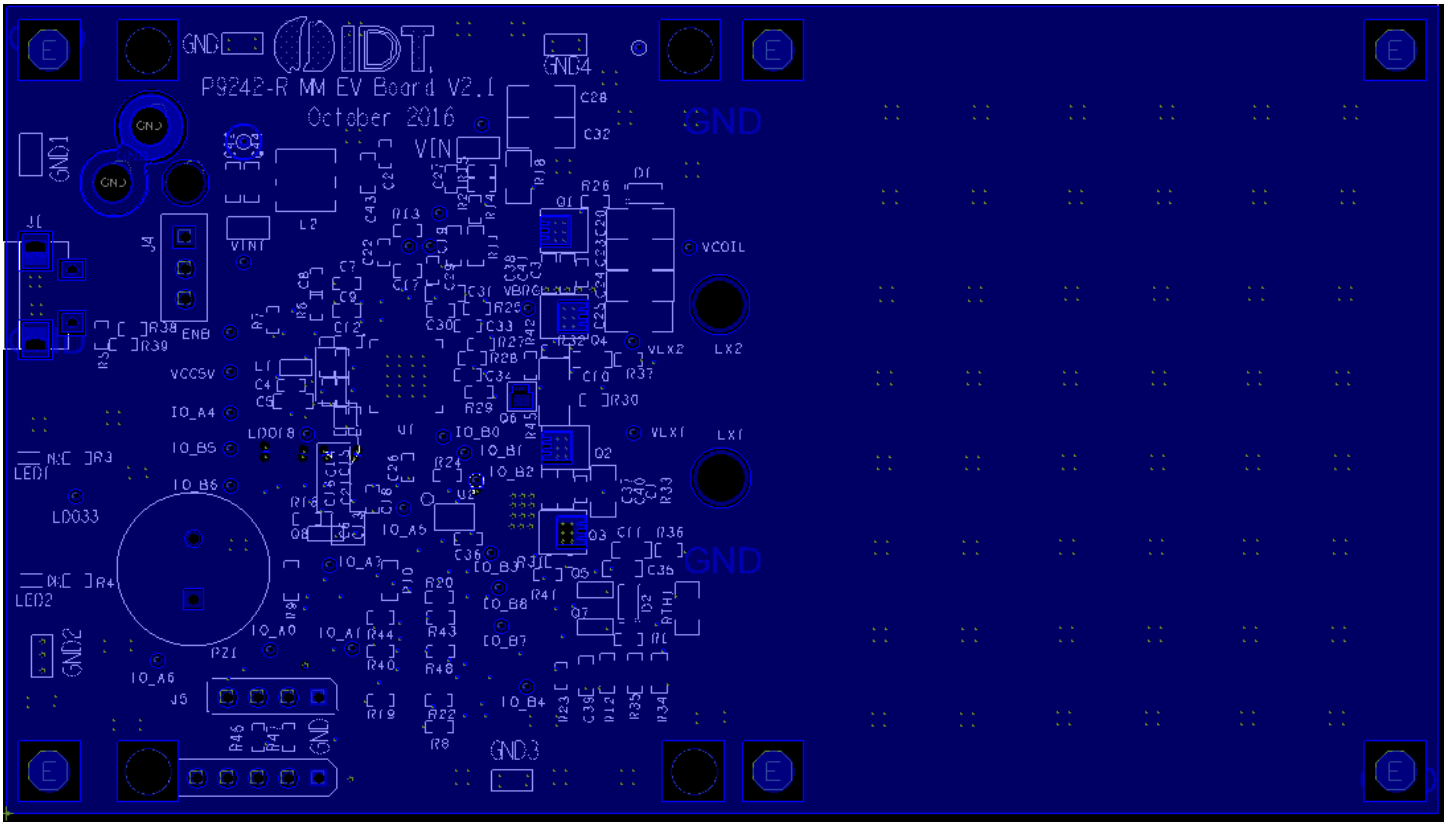
Note: The ground layer (L1) is between the top layer signal plane and layer 3 (second middle layer - L2) gate drive signal layer below.

Figure 5. P9242-R Physical Layout from P9242-R-EVK Evaluation Board of 3rd Layer (L2), Gate Driver Traces under Vin, GND Planes (Quiet Planes), Thick Power Traces, and Ground Plane with Minimal Traces especially around the P9242-R



Note: Routing of the FET gate driver lines away from switching nodes as much as possible (note 1). The traces are routed under the Vin and GND planes (electrically quite areas). Also note the thick 30mil traces for the supply voltages (5V-note 2,4; LDO33-note 5) and for the step down switching regulator's switch node (note 3). These thick traces prevent voltage drops when delivering the power, increasing reliability and efficiency.

Figure 6. P9242-R Physical Layout from Demo PCB of Bottom Layer, GND Plane with Minimal Traces for Maximum Thermal Transfer



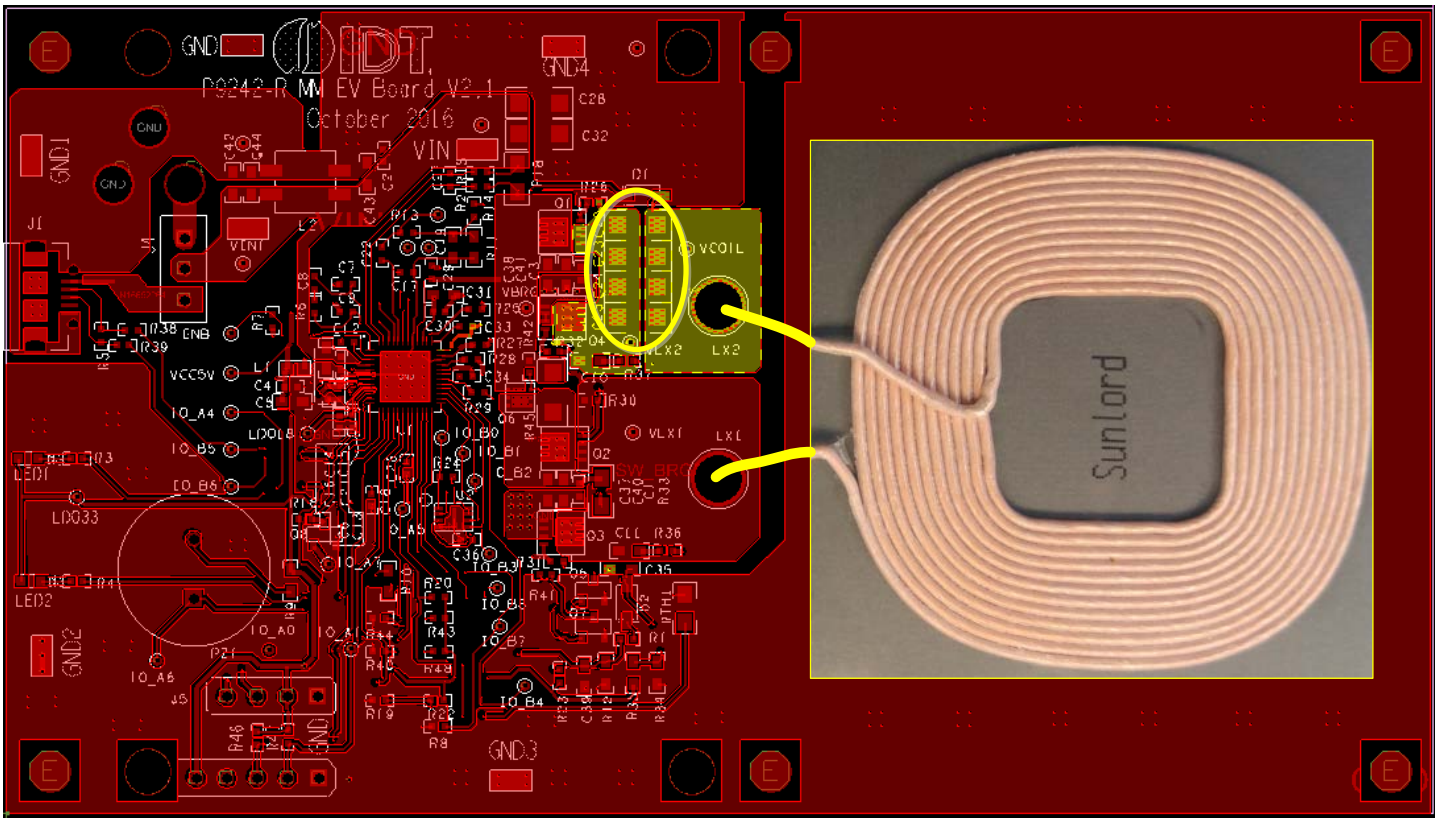
The outer layers of the PCB will be the most effective at transferring heat from the board to the ambient air or other objects. Spreading the heat into internal layers is also effective for lowering the operating temperature. Internal layers are able to effectively spread heat horizontally when they are not interrupted by traces and through-holes along their surface. An ideal layout will result in the entire PCB being close to the same temperature; however, in order to obtain this result, all board layers should have planes that are fairly continuous and in direct contact with the P9242-R thermal vias.

A single internal layer should be selected for routing the majority of the inner row/column pins to the rest of the PCB. The third layer is preferred for this purpose. The required nodes for connecting heat spreading planes are GND, the Vin sources to the H bridge (V_BRIDGE, drain of Q2), and the switch nodes (VLX1, VLX2). The other connections will spread heat due to natural thermodynamics, but the listed nodes contact the primary heat sources of the P9242-R.

2.1 Resonance Capacitors

Next, the resonance components should be placed. The C20, C23, C24, C25, and C9 capacitors should have wide copper planes connected to them and be in-line from the P9242-R to the Tx coil. C0G capacitors will offer the highest performance and are recommended. X7R and X5R can be substituted, but low-ESR components should be used. Since all the load current and the current required to transmit energy to the receiver flows through the resonance capacitors, the heat developed within the resonance capacitors (Class II only) should be given opportunity to spread into large copper planes.

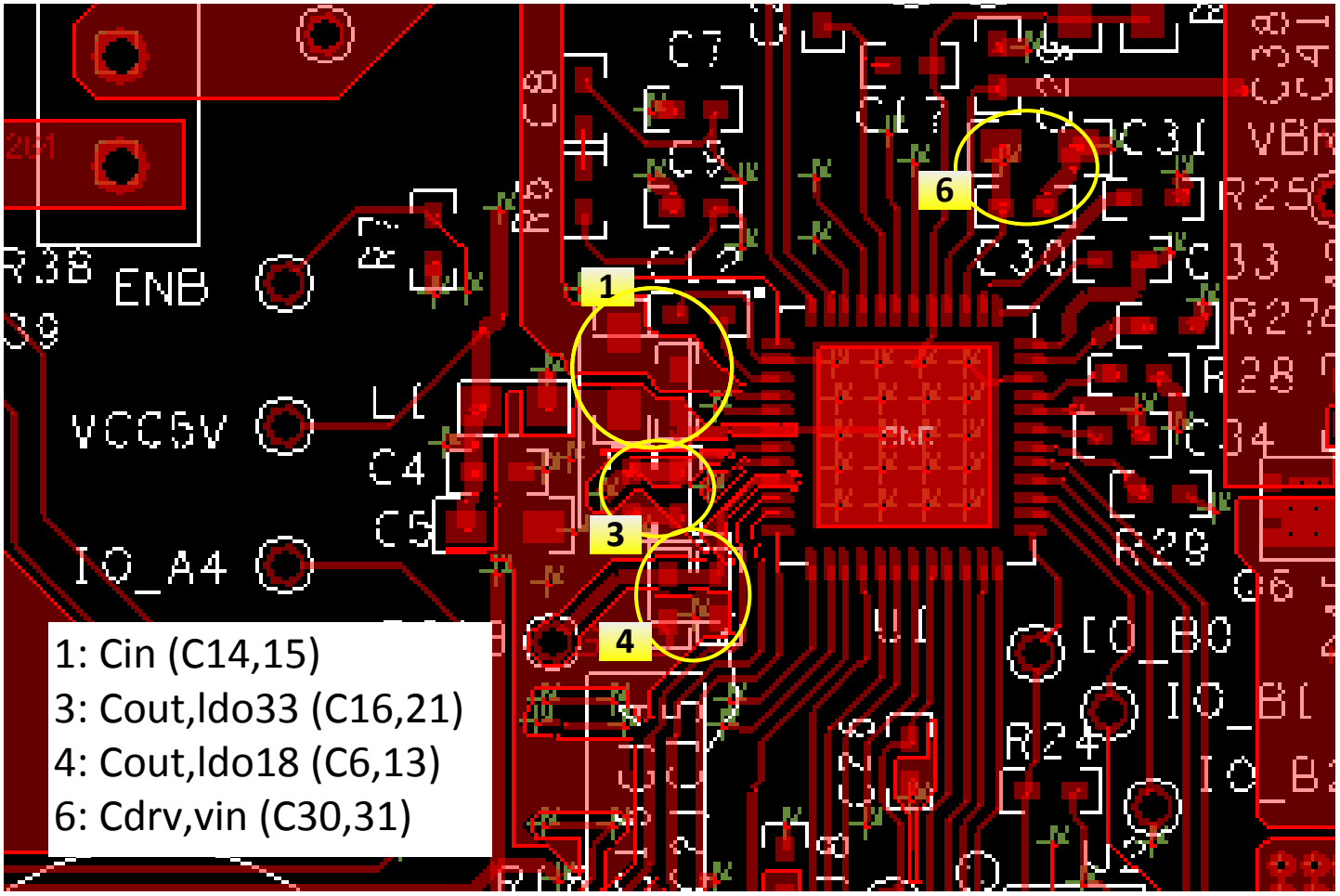
Figure 7. Resonance Capacitors



2.2 VCC5V VIN, VCC5V, LDO33, LDO18, VBRG_IN, and DRV_VIN Pin Capacitors

The VCC5V node, VIN, LDO33, LDO18, VBRG_IN, and DRV_VIN pin capacitors (C5, C4, C15, C14, C16, C21, C6, C13, C29, C30, C31) are used to stabilize internal voltage supplies used for normal operation. These capacitors must be located close to the P9242-R. A 10µF decoupling capacitor is recommended to be placed as close as possible to GND from the VIN, VCC5V, and DRV_VIN nodes. A 1µF decoupling capacitor is recommended for LDO33 and LDO18 regulated output pins. A 0.1µF capacitor is also recommended in parallel with aforementioned decoupling capacitor. This will reduce the ESR of the decoupling which will reduce noise at the pin. VBRG_IN requires a 0.1µF capacitor only.

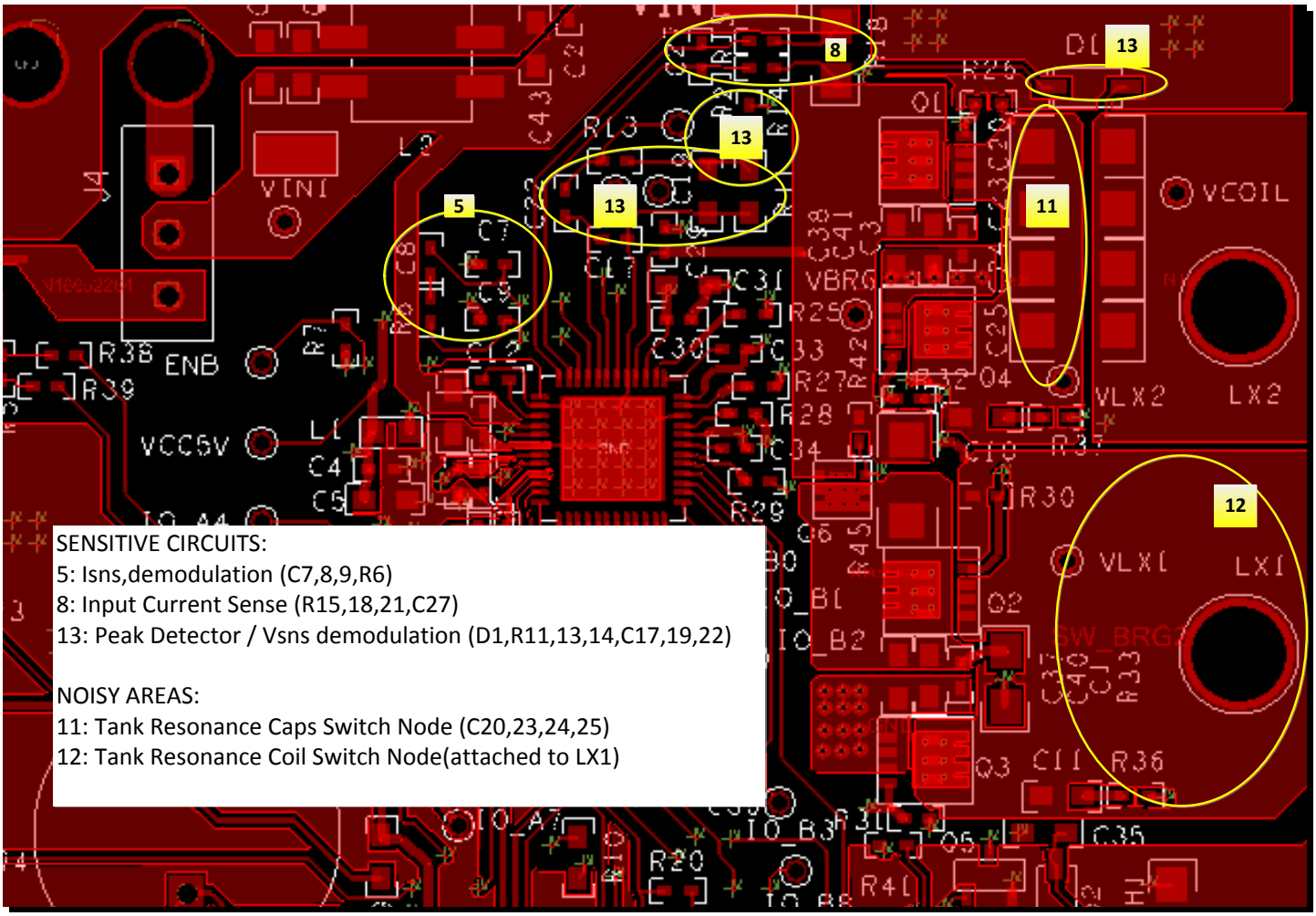
Figure 8. VIN, VCC5V, LDO33, LDO18, VBRG_IN, and DRV_VIN Pin Capacitors Placed Close to P9242-R with 0.1µF Placed Closest



2.3 Sensitive Circuits

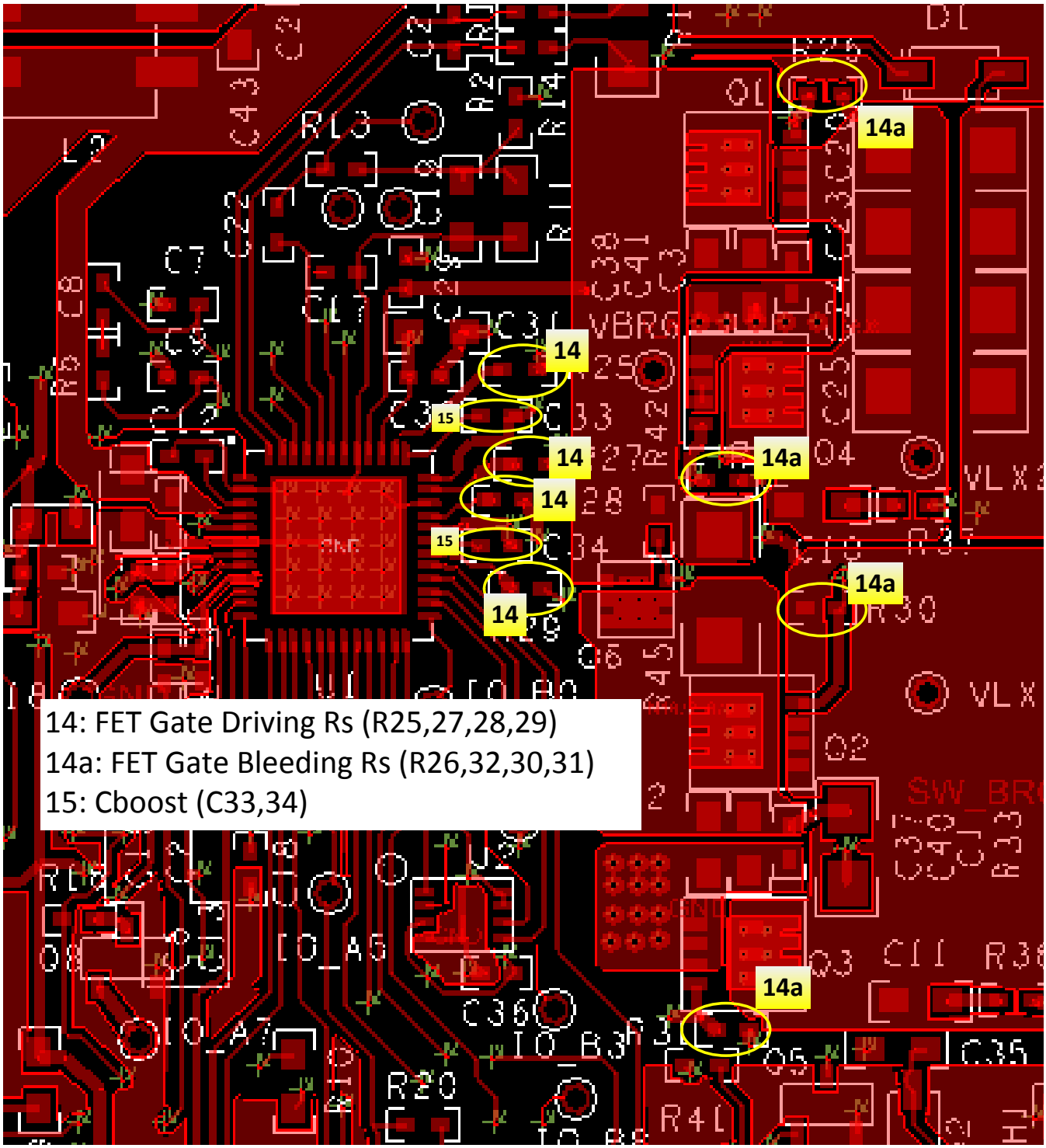
The term “sensitive circuits” refers to noise-sensitive circuits that should be referenced to GND in the “quiet” ground area. AC coupling, the thermistor bypass capacitors, and other capacitors are for decoupling noise. The resonance nodes generate the highest harmonic noise, which must be filtered with decoupling capacitor. Place the current sense circuitry, the voltage demodulation circuitry, and the current demodulation circuitry, in quiet ground areas away from the resonance nodes.

Figure 9. P9242-R Typical GND Noise Areas and Sensitive Circuit Placement



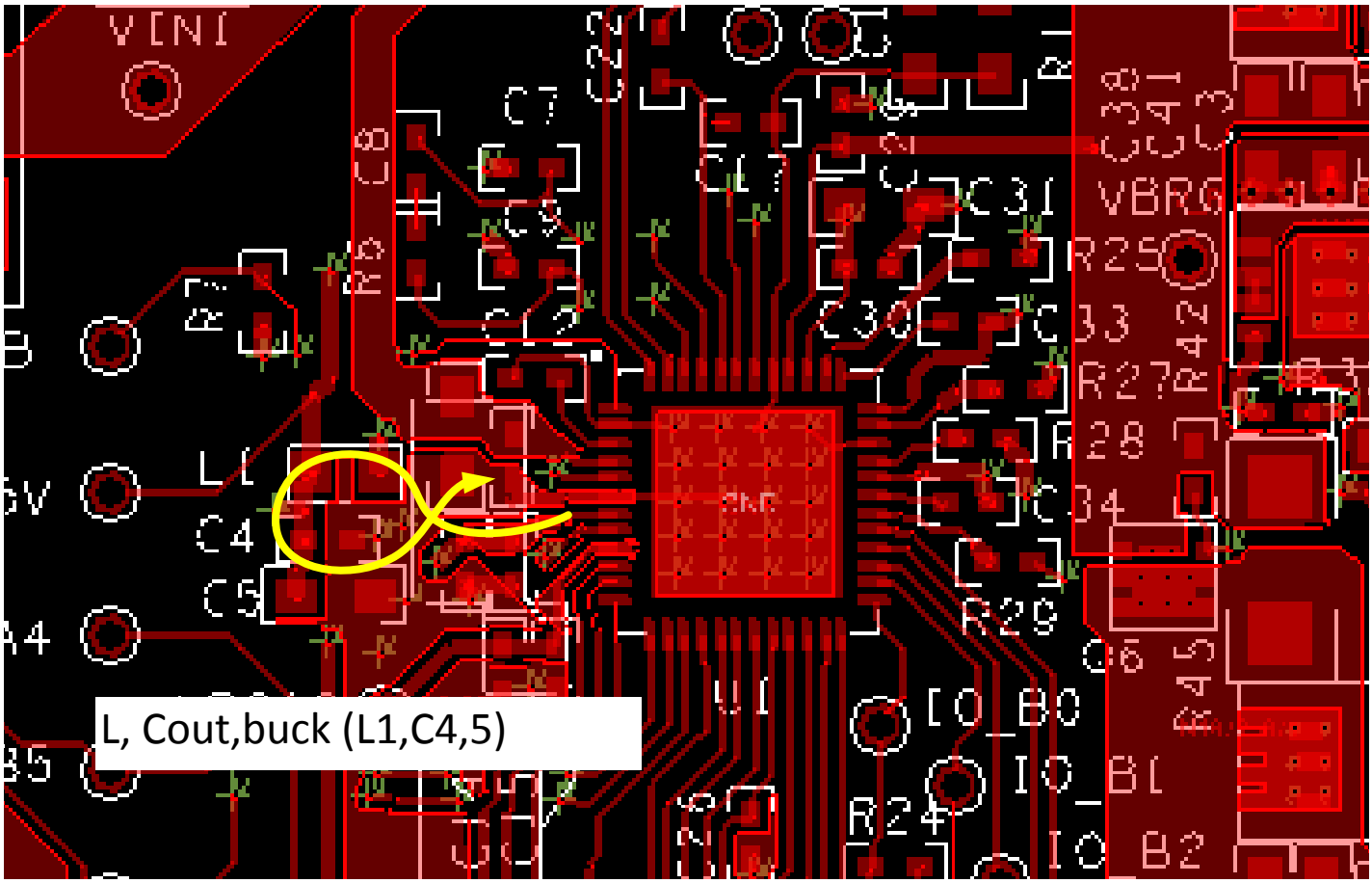
2.4 Boost Capacitors and Gate Drive Lines

Place the boost capacitors (C33, C34) close to their respective pins for maximum transfer of the capacitive energies. Place the gate driver resistors (R25, R27, R29, R28) close to their respective pins. This limits the switching noise generated. Place the FET gate bleed resistors (R26, R32, R30, R31) close to their respective FET gate pad/pin.



2.5 5V Step Down Switching Regulator

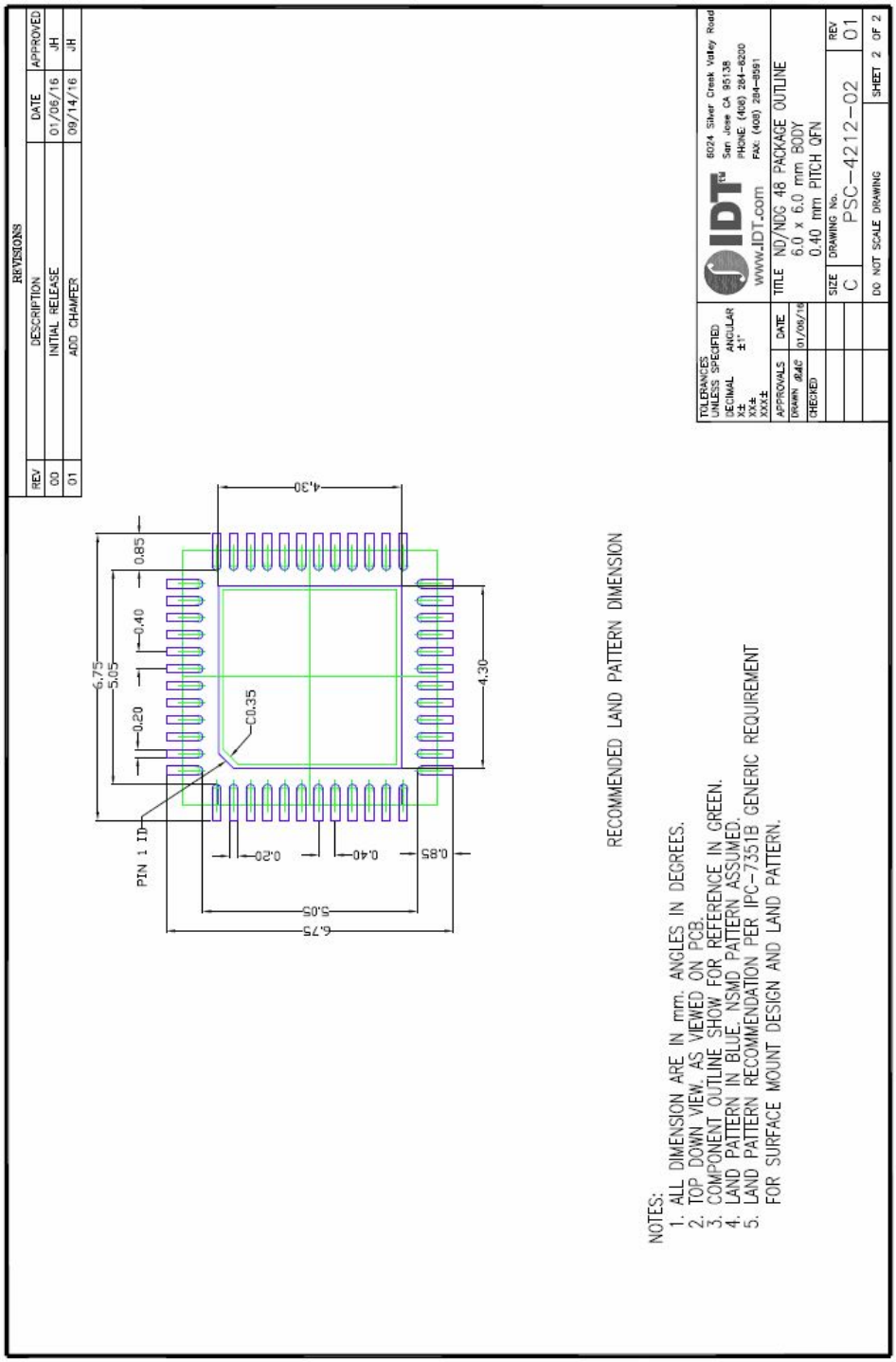
Keep the switch node small by moving the inductor close to the switch node. This is only after placing all Cin capacitors as close to their respective pins as possible. Make the L, Cout loop small to limit the loop inductance and related noise. Place the Cout such that the ground end of the capacitor is close to the nearest ground pin (pin 6).



3. PCB Footprint Design

The P9242-R package is a fine-pitch 48-VFQFN device.

Figure 10. P9242-R Recommended PCB Land Pattern Drawing



4. Audible Noise Suppression

Wireless power receiver solutions have been observed to produce audible noise. If sound is detected, there are several steps that can be taken to reduce or eliminate the noise. The first priority should be identifying the source (i.e., the rectifier capacitors, the Tx coil ferrite, communication capacitors). Typically, the rectifier capacitors are the components that generate the audible noise. The reason the noise is present and associated with the rectifier capacitors is due to the WPC communication signals being generated in the audible frequency range and the use of small-form factor ceramic capacitors. The noise occurs due to the piezoelectric effect of ceramic capacitors. The capacitors constrict and expand while providing the communication pulses, and this noise is amplified as it flexes the PCB.

The primary solution to this issue is to use low-acoustic noise capacitors. Alternatively, higher voltage rated components can have superior piezoelectric properties that can reduce the audible noise. Additionally, placing the capacitors on both sides of the PCB (directly above and below each other) counters the piezoelectric forces applied to the PCB (cancels the force by each capacitor). Another method is to add slots through the PCB on both outer sides of the capacitors or directly under each capacitor. One additional approach is to place additional lower capacitance value components in parallel to reduce the mechanical force of the piezoelectric effect per component.

For any additional questions, contact IDT technical support (see last page for contact information).

5. Schematics, Bill of Materials (BOM), and Board Layout

Figure 11. Application Schematics

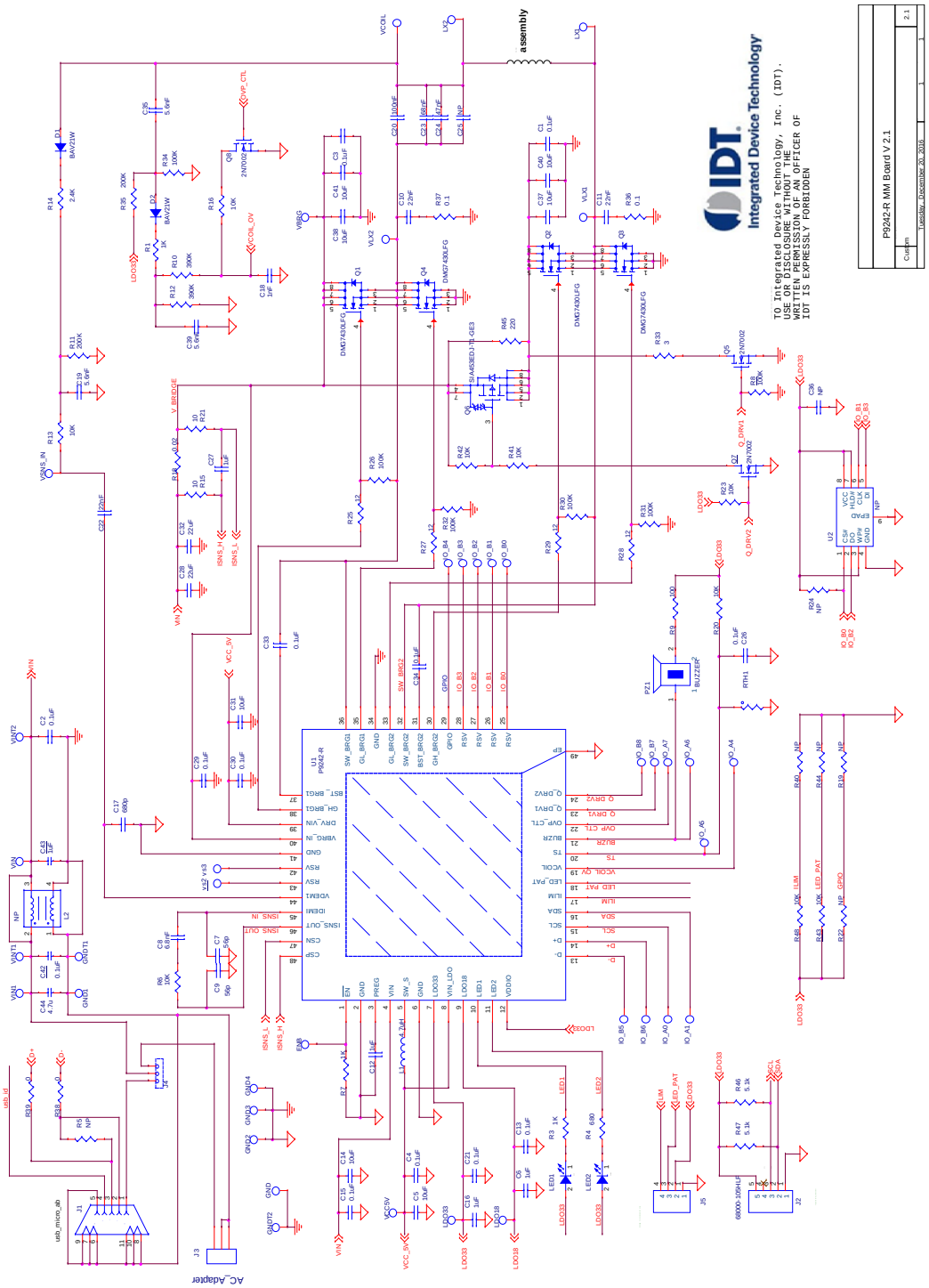


Table 1. Application Board Bill of Materials (BOM)

Item	Quantity	Reference	Value	Description	Part Number	PCB Footprint
1	12	C1,C2,C3,C4,C13,C15,C21,C26,C29,C30,C33,C34	0.1uF	CAP CER 0.1UF 25V 10% X7R 0402	C1005X7R1E104K050BB	402
2	7	C5,C14,C31,C37,C38,C40,C41	10uF	CAP CER 10UF 25V 20% X5R 0603	C1608X5R1E106M080AC	603
3	4	C6,C12,C16,C27	1uF	CAP CER 1UF 25V 20% X5R 0402	C1005X5R1E105M050BC	402
4	2	C7,C9	56p	CAP CER 56PF 50V NP0 0402	CL05C560JB5NNNC	402
5	1	C8	6.8nF	CAP CER 6800PF 25V X7R 0402	GRM155R71E682KA01D	402
6	2	C10,C11	22nF	0.022µF 50V Ceramic Capacitor X7R 0603	GCM188R71H223KA37D	603
7	1	C17	680p	CAP CER 680PF 50V X7R 0402	CL05B681KB5NNNC	402
8	1	C18	1nF	CAP CER 1000pF ±10% 50V X7R 0402	GRM155R71H102KA01D	402
9	3	C19,C35,C39	5.6nF	5600pF 100V Ceramic Capacitor C0G, NP0 0603	C1608C0G2A562J080AC	603
10	1	C20	100nF	CAP CER 0.1UF 100V C0G 1206	C3216C0G2A104K160AC	1206
11	1	C22	22nF	CAP CER 0.022UF 50V 10% X7R 0402	GRM155R71H223KA12D	402
12	1	C23	68nF	CAP CER 0.068UF 100V NP0 1206	C3216C0G2A683K160AC	1206
13	1	C24	47nF	CAP CER 0.047UF 100V NP0 1206	C3216C0G2A473J115AC	1206
14	1	C25	NP	CAP CER 10000PF 100V C0G 1206	C3216C0G2A103J115AA	1206
15	2	C28,C32	22uF	CAP CER 22UF 25V 20% X5R 1206	GRM31CR61E226KE15L	1206
16	1	C36	NP	CAP CER 0.1UF 25V 10% X7R 0402	C1005X7R1E104K050BB	402
17	1	C42	0.1uF	0.10µF 50V Ceramic Capacitor X7R 0603	GRM188R71H104KA93D	603
18	1	C43	1uF	1µF 25V Ceramic Capacitor X5R 0603	GRM188R61E105KA12D	603
19	1	C44	4.7u	4.7µF 25V Ceramic Capacitor X5R 0603	GRM188R61E475KE11D	603
20	2	D1,D2	BAV21W	DIODE GEN PURP 80V 125MA DFN	BAV21W-7-F	sod123
21	30	VLX1,VINT1,IO_B1,IO_A1,GNDT1,vs2,VLX2,VINT2,IO_B2,GNDT2,vs3,IO_B3,IO_B4,IO_A4,VCC5V,IO_B5,IO_A5,IO_B6,IO_A6,IO_B7,IO_A7,IO_B8,LDO18,LDO33,VSNS_IN,VCOIL,VBRG,IO_B0,IO_A0,ENB	PTH_TP	30 GAUGE WIRE PAD	NP	TEST_PT30DPAD
22	7	VIN1,GND1,GND2,GND3,GND4,VIN,GND	TP	TEST POINT PC MINIATURE SMT	5015	test_pt_sm_135x70
23	1	J1	5P	CONN RCPT MCR USB AB SMD TH SHLL	ZX62D-AB-5P8	usb_micro_ab
24	1	J2	68000-105HLF	BERGSTIK II .100" SR STRAIGHT	68000-105HLF	sip5
25	1	J3	AC_Adapter	CONN POWER JACK 2.5X5.5MM HI CUR	PJ-002AH	CONN_POWER_JACK5_5MM
26	1	J4	TP	CONN HEADER 3POS .100" STR GOLD	901200763	sip3
27	1	J5	SIP con	4 Positions Header, Unshrouded Connector 0.100" (2.54mm) Through Hole Gold or Gold, GXT™	961104-6404-AR	sip-4
28	1	LED1	LED	LED RED CLEAR 0603 SMD	150060RS75000	0603_diode
29	1	LED2	LED	LED GREEN CLEAR 0603 SMD	150060GS75000	0603_diode
30	2	LX1,LX2	NP	Tx Coil assemble through hole	NA	TP_TXCoil
31	1	L1	4.7uH	FIXED IND 4.7UH 620MA 500 MOHM	CIG10W4R7MNC	L0603
32	1	L2	NP	Common mode EMI choke	ACM4520-901-2P-T-000	EMI_TDK_ACM4520L
33	1	PZ1	BUZZER	BUZZER PIEZO 4KHZ 12.2MM PC MNT	PS1240P02CT3	9235_buzzer
34	4	Q1,Q2,Q3,Q4	DMG7430LFG	MOSFET N-CH 30V 10.5A PWRDI3333	DMG7430LFG-7	powerdi3333_8ld_fet
35	3	Q5, Q7, Q8	2N7002	N-Channel 60-V (D-S) MOSFET	2N7002KT1G	SOT23_3
36	1	Q6	SIA453EDJ-T1-GE3	MOSFET P-CH 30V 24A PPAK SC-70-6	SIA453EDJ-T1-GE3	sc70_6ld_fet
37	1	RTH1	NP	NTC Thermistor 10k Bead	NTCLE203E3103JB0	805
38	3	R1,R3,R7	1K	RES SMD 1K OHM 5% 1/16W 0402	RC0402JR-071KL	402
39	1	R4	680	RES SMD 680 OHM 5% 1/16W 0402	RC0402JR-07680RL	402
40	1	R5	NP	RES SMD 0.0 OHM JUMPER 1/10W	RC0402JR-070RL	402
41	9	R6,R13,.R16,R20,R23,R41,R42,R43,R48	10K	RES SMD 10K OHM 1% 1/10W 0402	RC0402FR-0710KL	402
42	5	R8,R26,R30,R31,R32	100K	RES SMD 100K OHM 5% 1/10W 0402	ERJ-2GEJ104X	402
43	1	R24	NP	RES SMD 100K OHM 5% 1/10W 0402	ERJ-2GEJ104X	402
44	1	R9	100	RES SMD 100 OHM 5% 1/10W 0603	RC0603JR-07100RL	603
45	2	R10,R12	390K	RES SMD 390K OHM 5% 1/10W 0603	ERJ-3GEYJ394V	603
46	1	R14	2.4K	RES SMD 2.4K OHM 5% 1/10W 0402	ERJ-2GEJ242X	402
47	2	R11,R35	200K	RES SMD 200K OHM 1% 1/10W 0603	RC1608F204CS	603
48	2	R15,R21	10	RES SMD 10 OHM 1% 1/10W 0402	ERJ-2RKF10R0X	402
49	1	R18	0.02	RES SMD 0.02 OHM 1% 1/8W 0805	WSL0805R0200FEA	805
50	4	R19,R22,R40,R44	NP	RES SMD 10K OHM 1% 1/10W 0402	RC0402FR-0710KL	402
51	4	R25,R27,R28,R29	12	RES SMD 12 OHM 5% 1/10W 0402	ERJ-2GEJ120X	402
52	1	R33	3	RES SMD 3 OHM 1% 1/8W 0805	RC0805FR-073RL	805
53	1	R34	100K	RES SMD 100K OHM 1% 1/10W 0603	ERJ-3EKF1003V	603
54	2	R36,R37	0.1	RES SMD 0.1 OHM 5% 1/6W 0402	ERJ-2BSJR10X	402
55	2	R38,R39	0	RES SMD 0.0 OHM JUMPER 1/10W	RC0402JR-070RL	402
56	1	R45	220	RES SMD 220 OHM 1% 0.4W 0805	RC1206FR-07220RL	1206
57	2	R46,R47	5.1k	RES SMD 5.1K OHM 5% 1/16W 0402	MCR01MRTJ512	402
58	1	U1	P9242-R	Medium Power Transmitter	P9242-R	socketqfn_48_6x6_0p4
59	1	U2	NP	SPIFLASH 2M-BIT 4KB UNIFORM SECT	W25X20CLUXIG TR	uson_2x3_8LD

Figure 12. Silkscreen – Top of Board

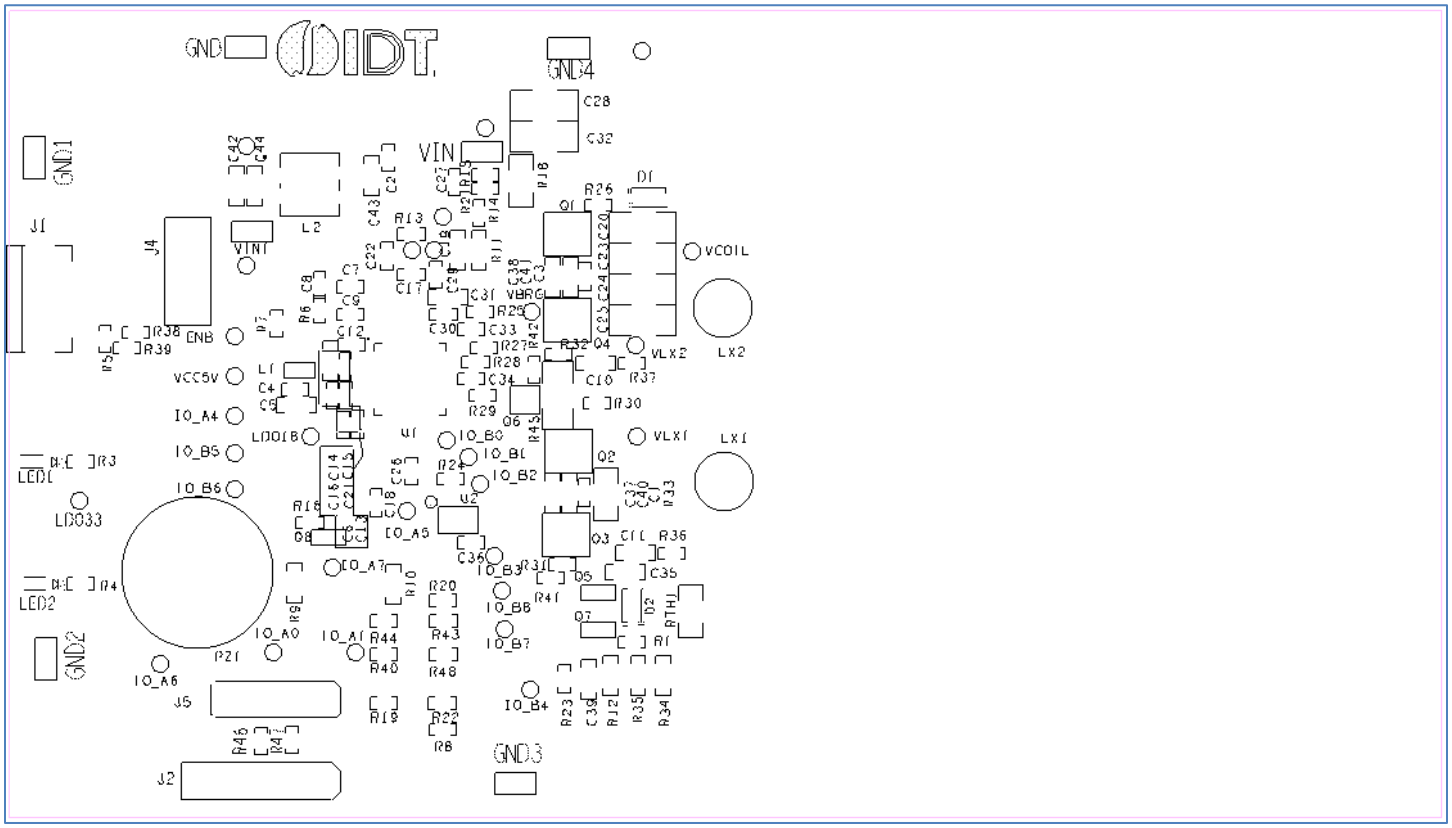


Figure 13. Copper – Top Layer

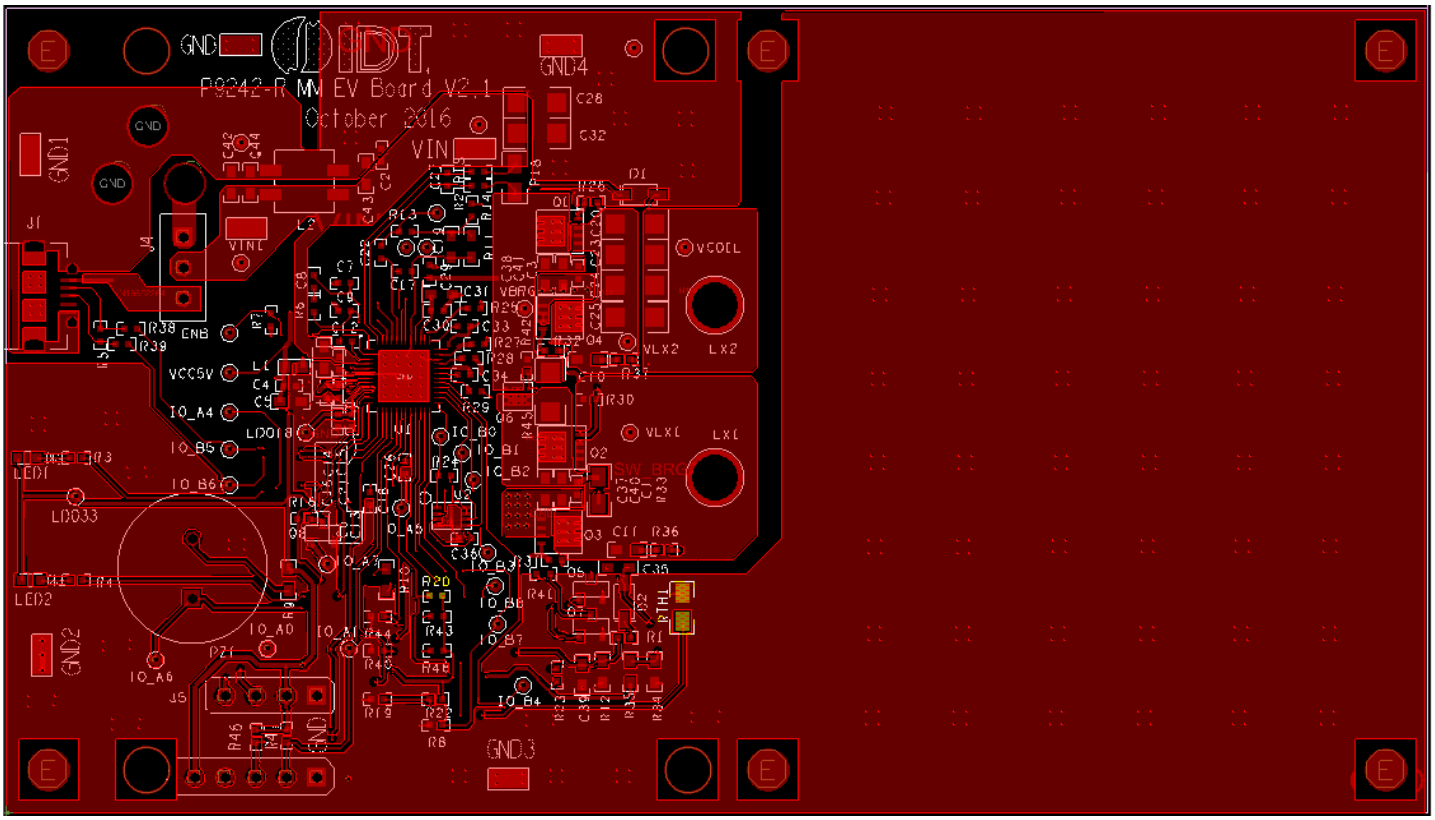


Figure 14. Copper L1 Layer

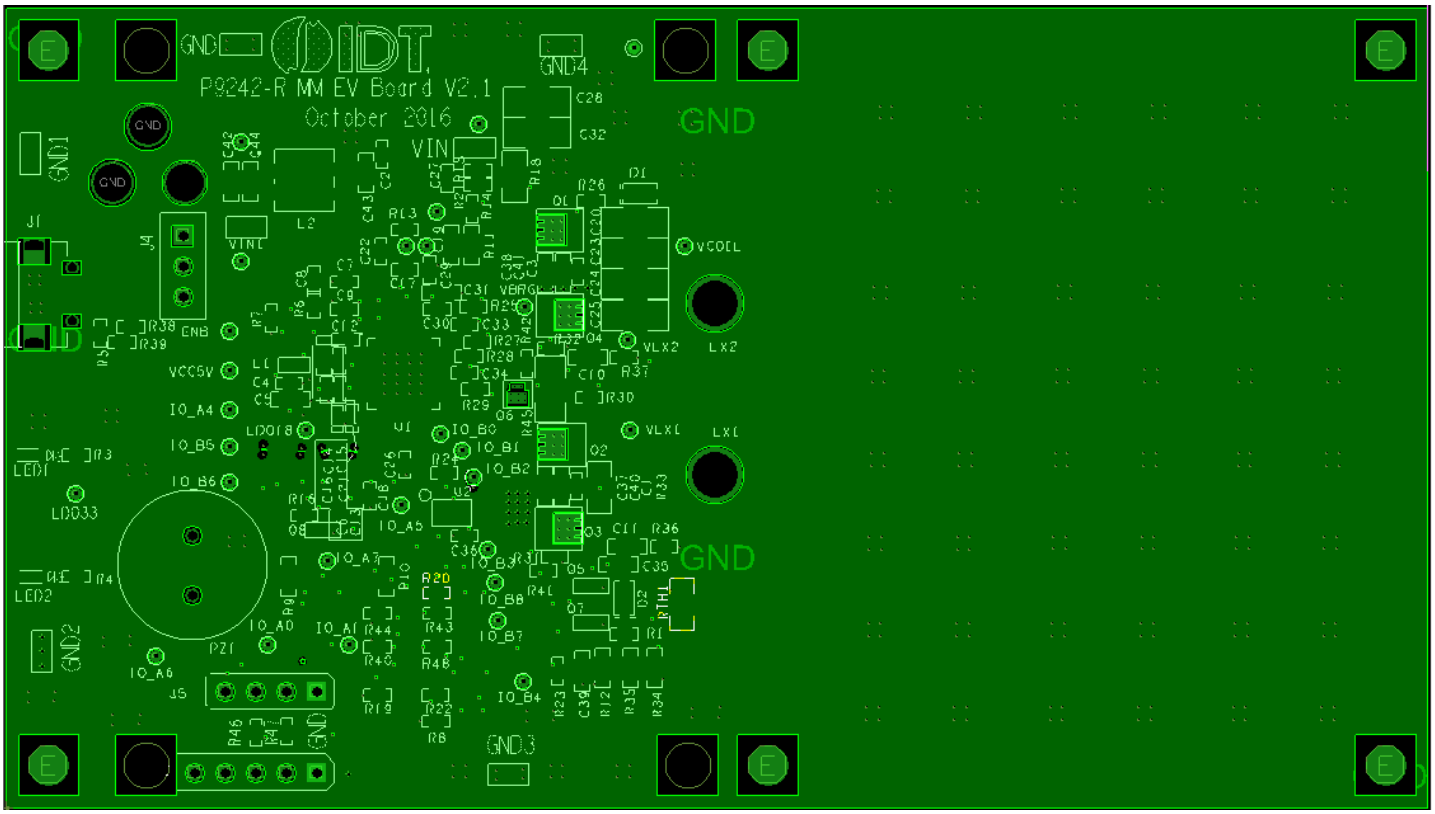


Figure 15. Copper L2 Layer

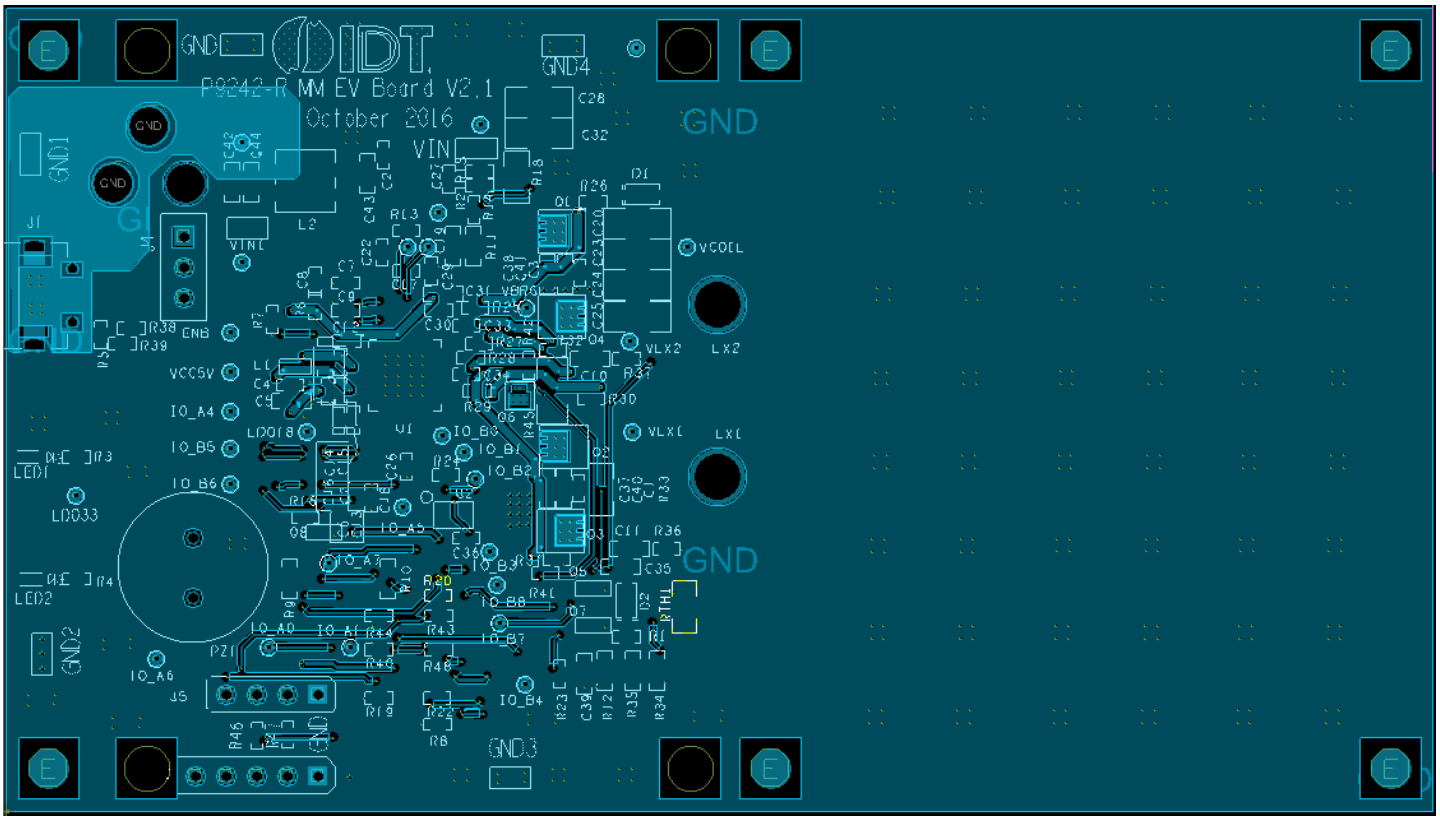
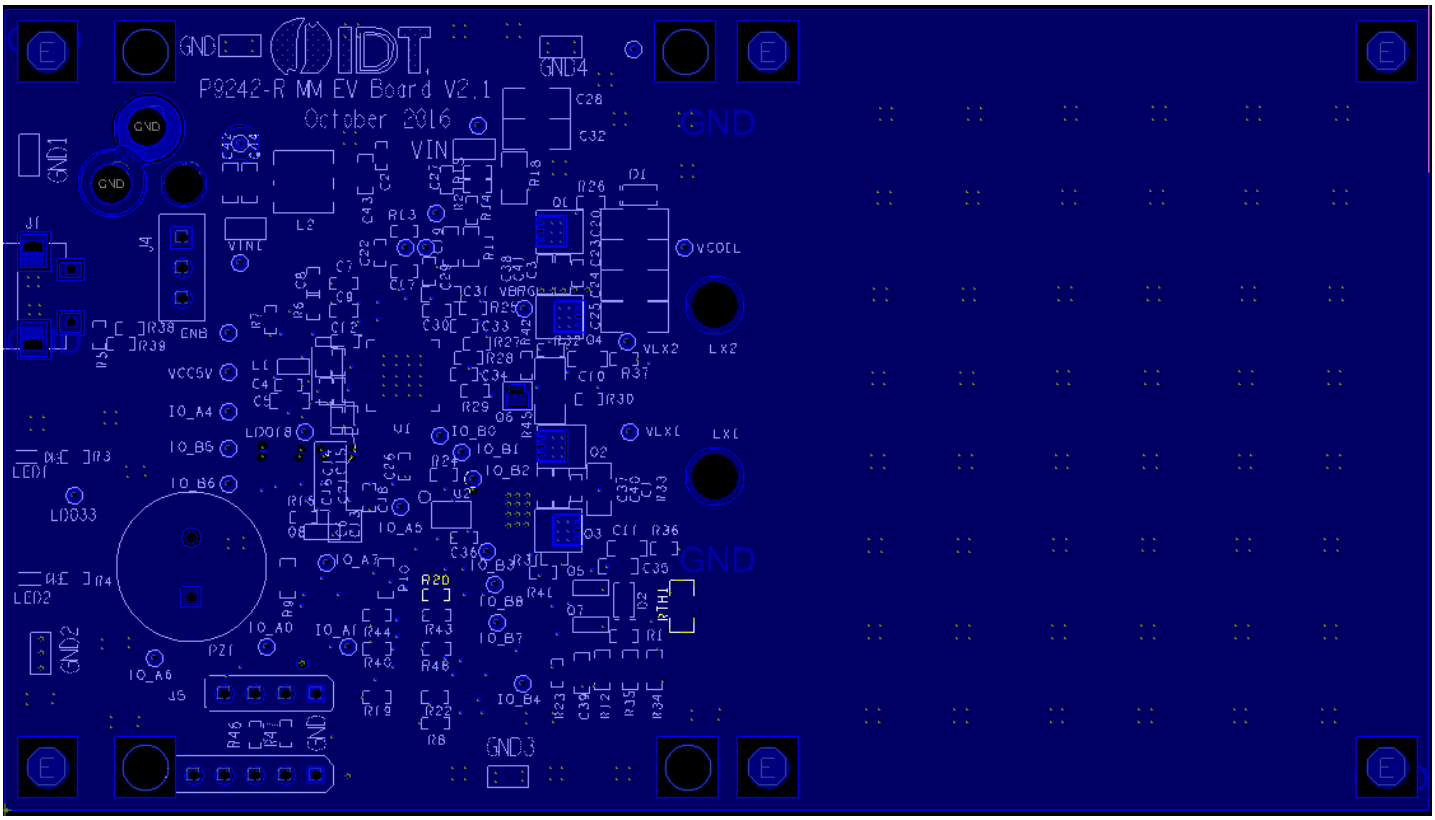


Figure 16. Copper Bottom



6. Revision History

Revision Date	Description of Change
December 22, 2016	Initial release of document.

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