R9A06G061 DC-PLC PCB Design Guide

Design Guide

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Summary

This document is a design guide for DC power line communication (hereinafter referred to as DC-PLC) using Renesas Electronics' PLC modem LSI R9A06G061 (CPX4). This document uses the CPX4 DC-PLC Evaluation Kit RTK0EE0009D01001BJ as an example and explains various cautions regarding the design of a DC-PLC board equipped with a PLC modem LSI (CPX4), Power Amp (ISL15102), and power supply ICs. There are two types of drive methods for the DC-PLC board: CPX4 direct drive (hereinafter referred to as CPX drive) and CPX4 + Power Amp drive (hereinafter referred to as PA drive), and the circuit configurations for each are listed. Note that the cautions explained in this document are general considerations for board design, and may not necessarily be appropriate depending on the size, installed components, and layout of your board.

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1. DC-PLC board configuration example

Figure 1-1 shows a configuration example of a DC-PLC board equipped with PLC modem LSI R9A06G061 (CPX4), Power Amp (ISL15102), and power supply ICs. The DC-PLC board has two types of drive methods: CPX drive that is directly driven by the CPX4 output, and PA drive that is driven by a Power Amp after the CPX4. PA drive has an output level 10dB higher than CPX drive, and is used when a large number of connected devices or communication distance is long. Power filter board is used to achieve stable DC-PLC when the impedance of the power supply or other systems on the DC power line is low.

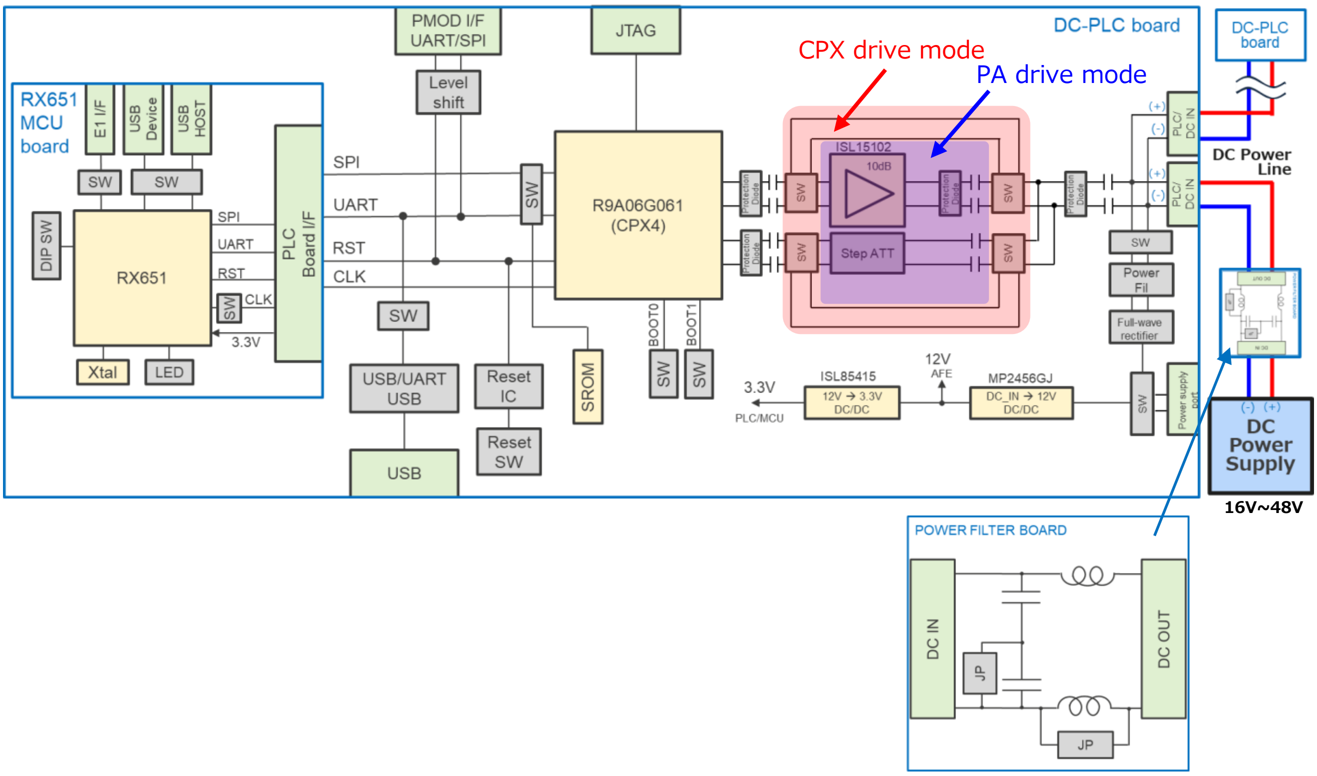


Figure 1-1 R9A06G061(CPX4) / ISL15102 applicable DC-PLC board configuration example

2. Cautions regarding peripheral circuits of R9A06G061

2.1 R9A06G061 Peripheral circuit

Add the R9A06G061's decoupling capacitance to each power supply terminal as shown in Figure 2-1, and place them near the power supply terminal. In particular, note that AVDD33R (1pin) and AVDD33T (36pin) affect the TX and RX characteristics.

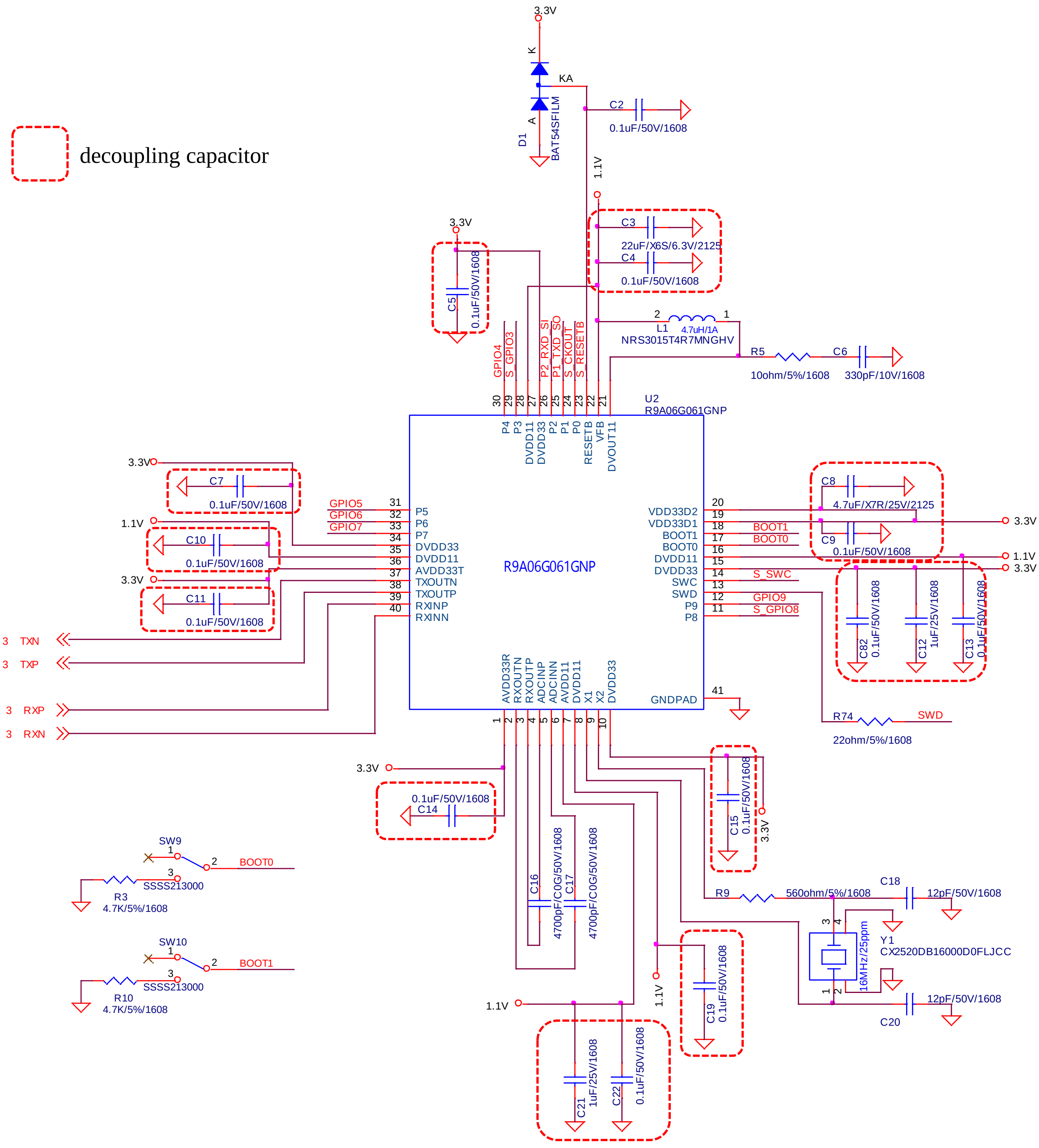


Figure 2-1 R9A06G061 Peripheral circuit

2.2 BOOT terminal setting

The BOOT0 and BOOT1 are terminals for setting the interface for downloading firmware for boot. Figure 2-2 shows the settings for the BOOT0 and BOOT1 terminals.

- Set to UART I/F BOOT : BOOT0, BOOT1=Open (High)
- Set to SPI I/F BOOT : BOOT0=Open (High), BOOT1=Connect to GND via 4.7kΩ or 5.1kΩ (Low)
- Set to SROM I/F BOOT : BOOT0=Connect to GND via 4.7kΩ or 5.1kΩ (Low), BOOT1=Open (High)
- TEST mode (Setting prohibited) : BOOT0, BOOT1=Connect to GND via 4.7kΩ or 5.1kΩ (Low)

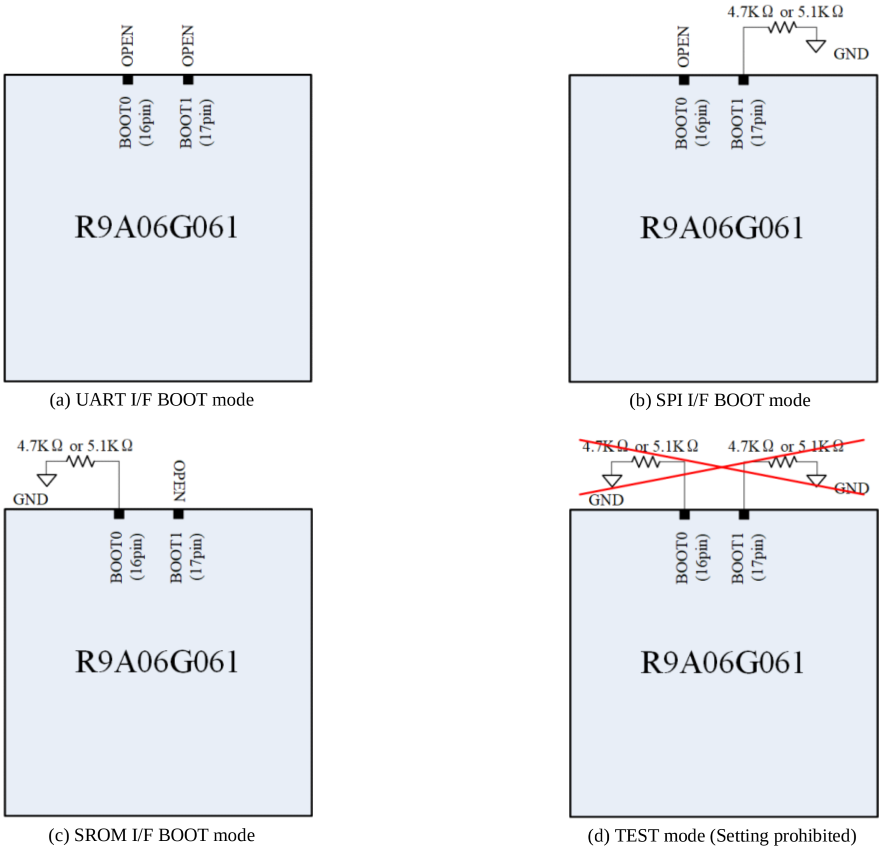


Figure 2-2 BOOT0, BOOT1 terminal settings

2.3 Reference clock setting

- Figure 2-3 shows a connection example of the crystal oscillator circuit.
- Capacitor loads C18 and C20 are required for the X1(8pin) and X2(9pin) terminals in order for the 16MHz crystal oscillator to oscillate stably. In addition, R9 is required to adjust the negative resistance.
- For the reference clock, the G3-PLC standard recommends that the frequency deviation of the system clock be within ± 25 ppm across the full temperature range used. Therefore, it is recommended to select the reference clock so that the frequency tolerance (deviation) and frequency stability (temperature characteristics) are within ± 25 ppm.
- Recommended specifications for the crystal resonator are frequency: 16MHz, load capacitance: 8pF, frequency tolerance: ±10ppm, frequency temperature characteristics: ±15ppm.
- Table 2-1 shows recommended crystal resonator devices and external circuit constants. Recommended devices: Daishinku DSX221SH (recommended specifications must be specified), NDK NX2520SA-16M-CHP-CSW-19 (please note that the external circuit constants are different from DSX221SH)
- Determine the final circuit constant in consideration of the specifications of the crystal oscillator to be used and the pattern capacitance of the PCB, and consult with the crystal oscillator manufacturer if necessary.
- R9A06G061 does not have a mode that uses an external clock.
- Place the crystal oscillator and its peripheral components connected to the R9A06G061 as close to the terminals as possible, and keep the wiring short. Also, place a GND under and around the crystal oscillator, and connect it to the GND solid pattern so that it does not become an isolated island pattern. Figure 2-4 shows an example of the placement of a crystal oscillator and its peripheral components.

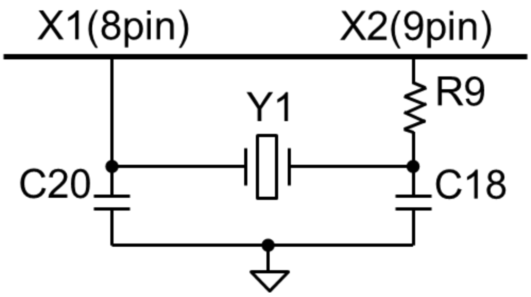


Figure 2-3 Crystal oscillator circuit connection example

Table 2-1 Recommended devices for crystal oscillator circuits and examples of external circuit constants

Part No. / Recommended crystal oscillator device	C18	C20	R9
Using Daishinku DSX221SH	12pF	12pF	560Ω
Using NDK NX2520SA-16M-CHP-CSW-19	15pF	12pF	2.2kΩ

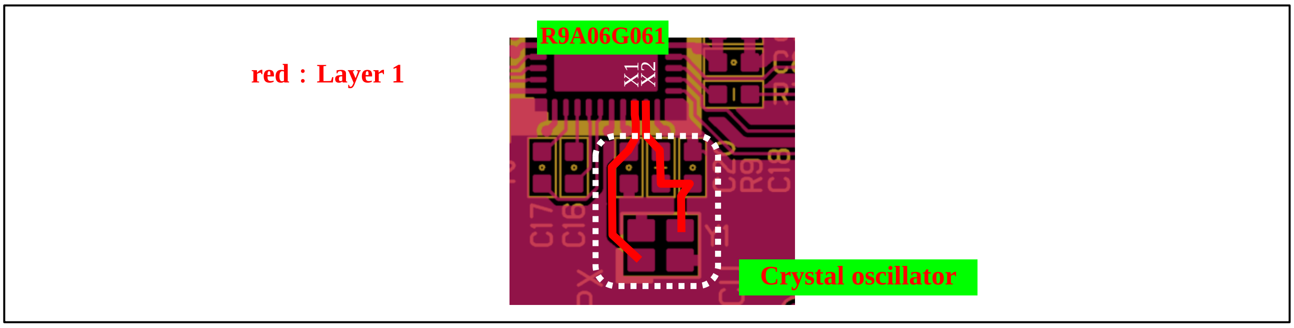


Figure 2-4 Example of placement of crystal oscillator and its peripheral components

2.4 RESETB terminal

- An example of an external circuit for the RESETB terminal is shown in Figure 2-5, and an example of the circuit constants is shown in Table 2-2.
- Place C2 near the RESETB terminal to prevent malfunction due to noise.
- If surge noise such as ESD is expected and there is a concern about the operating environment such as malfunction or terminal destruction, it is recommended to add D1 near the terminal. (In the circuit constant example in Table 2-2, STMicro's BAT54SFILM is used, but determine the specifications such as current capacitor according to the assumed noise.)
- It is recommended to connect to GND via Rx (pull-down resistor). This is to keep the R9A06G061 in the reset state (RESETB = low) to prevent malfunctions while preparing to download the R9A06G061 firmware after a power-on reset. For the resistance value of Rx, consider the impedance of the reset signal output and set the optimum value. (In the circuit constant example in Table 2-2, it is set assuming that there is a pull-up resistance of 50 kΩ or more.)

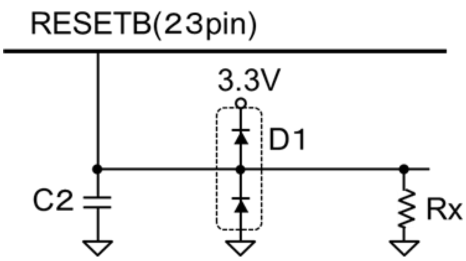


Figure 2-5 Example of an external circuit for the RESETB terminal

Table 2-2 Example of the circuit constants for the RESETB terminal

Component No.	C2	D1	Rx
Component value	0.1uF	BAT54SFILM (STMicro)	4.7kΩ or 5.1kΩ

2.5 DC-DC converter

- The built-in DC-DC converter of R9A06G061 generates a power supply voltage of 3.3V to 1.1V by the switching regulator method. This 1.1V is supplied to the 1.1V power supply of R9A06G061 through the PCB wiring.
- For the frequency stability of the DC-DC converter, C3 should be a total of 20uF~60uF.
- Figure 2-6 shows an example of an external circuit for a DC-DC converter, and Table 2-3 shows an example of its circuit constants.
- Figure 2-7 shows an example of connecting the decoupling capacitor of the power supply terminal of the DC-DC converter. As shown in Figure 2-7 (a), place the decoupling capacitor in the immediate vicinity of the power supply terminal.
- Place the R9A06G061's decoupling capacitance and the R9A06G061's built-in DC-DC external components near the R9A06G061's terminals, and make the wiring from DVOUT11 to VFB as short as possible, avoiding crossing with other signals. Figure 2-8 shows an example of the placement of external DC-DC converter components.

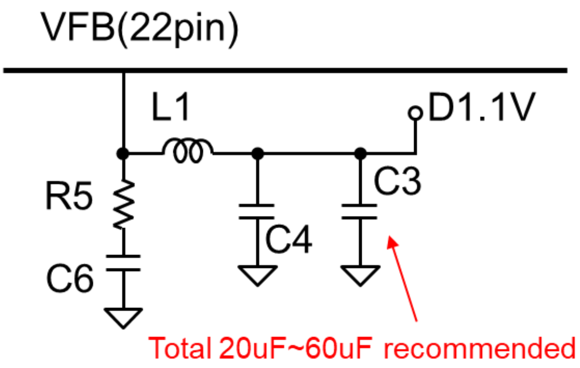
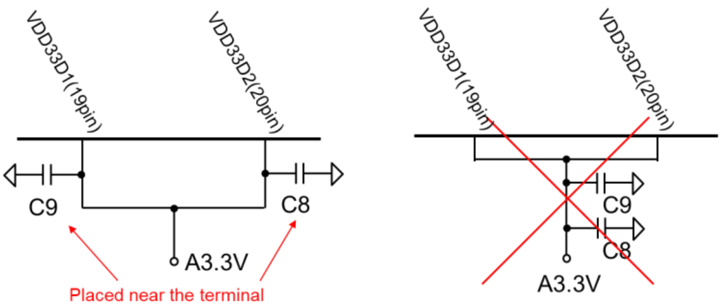


Figure 2-6 Example of an external circuit for a DC-DC converter

Table 2-3 Example of the circuit constants for a DC-DC converter

Component No.	R5	C6	C3	C4	L1
Component value	10Ω	330pF	22uF	0.1uF	4.7uH



(a) (b)

Figure 2-7 Example of connecting the decoupling capacitor of the power supply terminal of the DC-DC converter

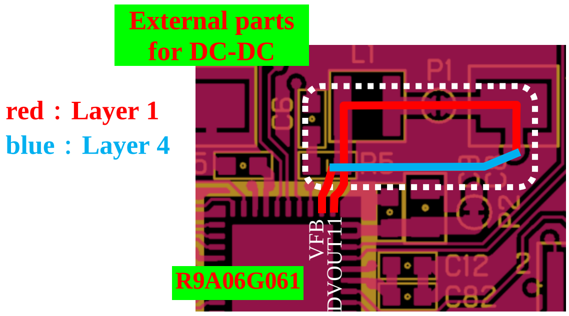


Figure 2-8 Placement of the external parts for R9A06G061 built-in DC-DC

2.6 LED setting

- Figure 2-9 shows an example of using the LED that shows the transmission / reception status of R9A06G061.
- In this example, it is assumed that LED1 indicates the state when the packet is sent and LED2 indicates the state when the packet is received. (The control of the LEDs is done based on the firmware that is downloaded during booting.) However, due to the limitation of the GPIO terminal of R9A06G061, the connection terminal to the LED becomes a terminal that can be used as both the BOOT0 terminal and the BOOT1 terminal.
- It is recommended to set the current flowing through the LED to about 1mA.
- For LEDs1 and R7, set R7 so that

$I_{LED1} = \frac{(3.3V - V_{F\_LED1})}{R7}$ makes I_{LED1} about 1mA.

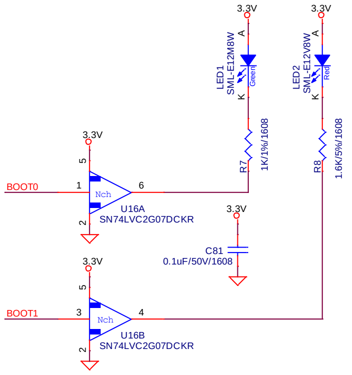


Figure 2-9 Example of using the LED that shows the TX/RX status of R9A06G061

3. Cautions regarding AFE circuit

The DC-PLC board has two types of drive methods: CPX drive that is directly driven by the CPX4 output, and PA drive that is driven by a Power Amp after the CPX4. Regarding the drive capacity of each drive method, CPX drive assumes a load impedance of 50Ω or more, and PA drive assumes a load impedance of 10Ω or more. PA drive has an output level 10dB higher than CPX drive, and is used when a large number of connected devices or communication distance is long. This chapter explains cautions when designing AFE circuits for CPX drive and PA drive.

3.1 Cautions on CPX drive AFE circuit

3.1.1 CPX drive configuration

- Figure 3-1 shows a connection example of a CPX drive AFE circuit.

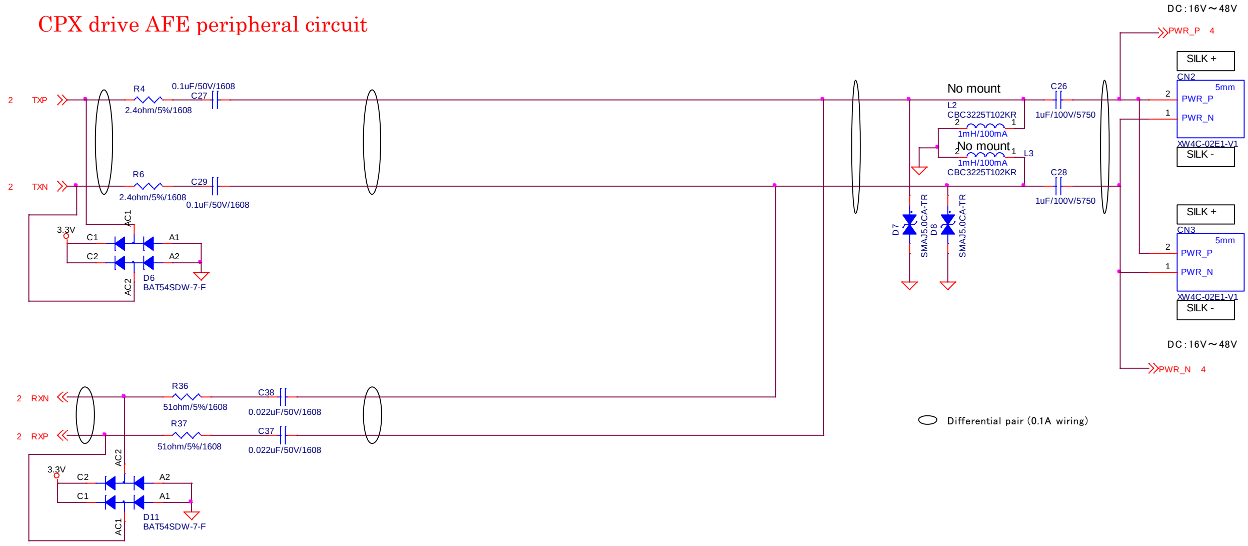


Figure 3-1 Connection example of CPX drive AFE peripheral circuit

3.1.2 CPX drive protection circuit

Figure 3-2 shows an example of connecting a protection circuit for CPX drive. Select a protection element considering the expected noise level.

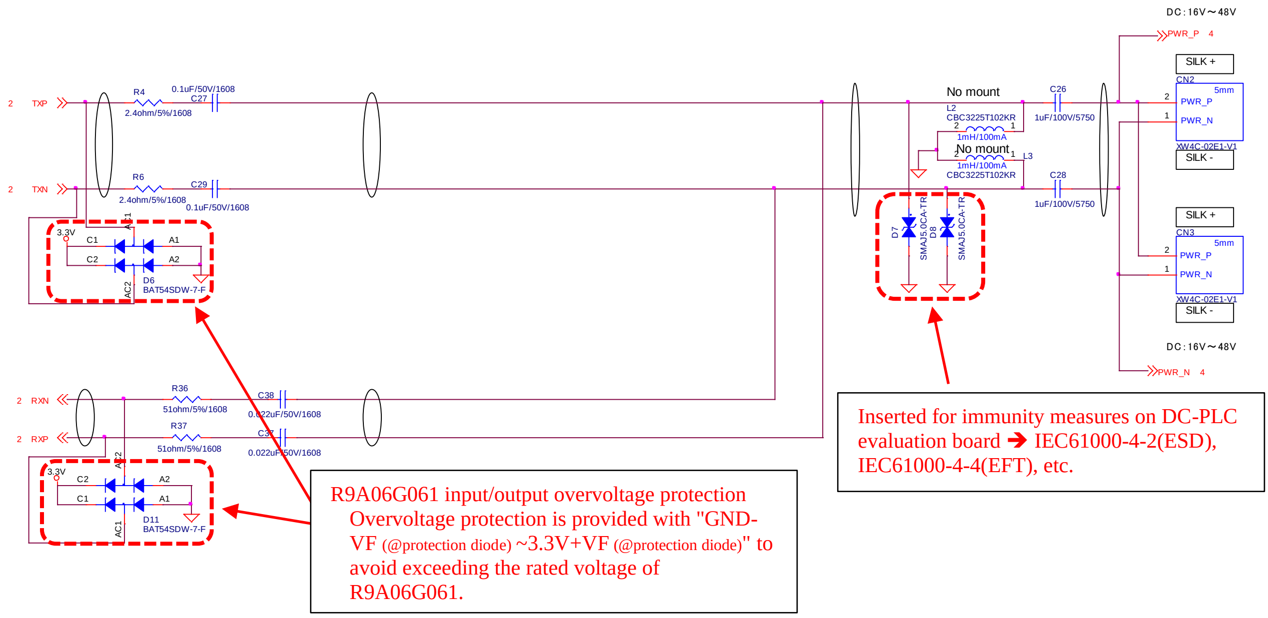


Figure 3-2 Connection example of CPX drive protection circuit

3.1.3 Cautions regarding PCB layout around for CPX drive AFE circuit

- Figure 3-3 shows cautions for the PCB layout of the CPX drive AFE circuit.
- Since the TX and RX signal lines of the R9A06G061-DC IN/PLC signal terminal are differential signals, please arrange and wire the components with equal length wiring, as short as possible, and with balance in mind. However, if there is a risk of interference with the power circuit, give priority to increasing the distance (at least 3 cm) between the RX signal line and the power circuit. (See Figure 3-3)
- On the power supply layer (3rd layer), avoid crossing the power supply patterns and use GND patterns as much as possible in areas that overlap with the TX and RX signal lines and its components. (Figure 5-4 shows an example of the GND pattern of the power layer)

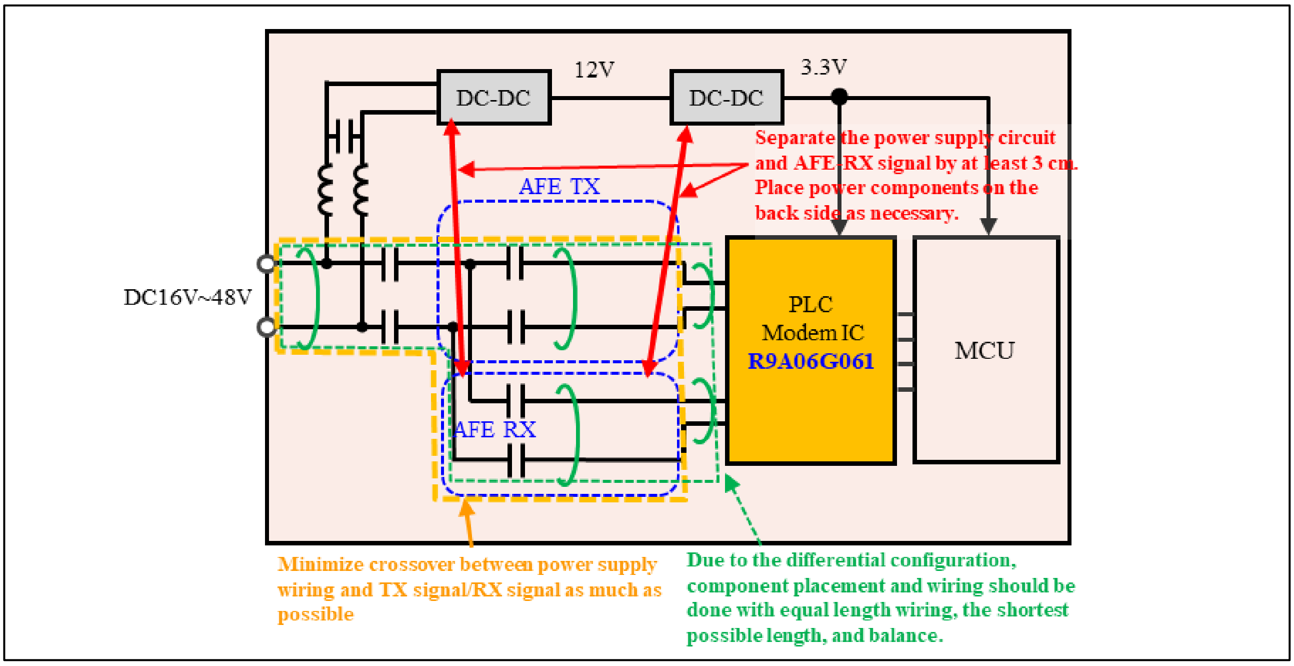


Figure 3-3 Cautions on PCB layout of CPX drive AFE circuit

3.2 Cautions for PA drive AFE circuit

3.2.1 PA drive configuration

- Figure 3-4 shows a connection example of a PA drive AFE circuit configuration.
- Place decoupling capacitors near the emitter followers of ISL15102's VS+ (11pin, 21pin) and RX circuits. (In particular, VS+ (21pin) of ISL15102 is the PA output power supply, so place 1uF and 100uF near the terminal)

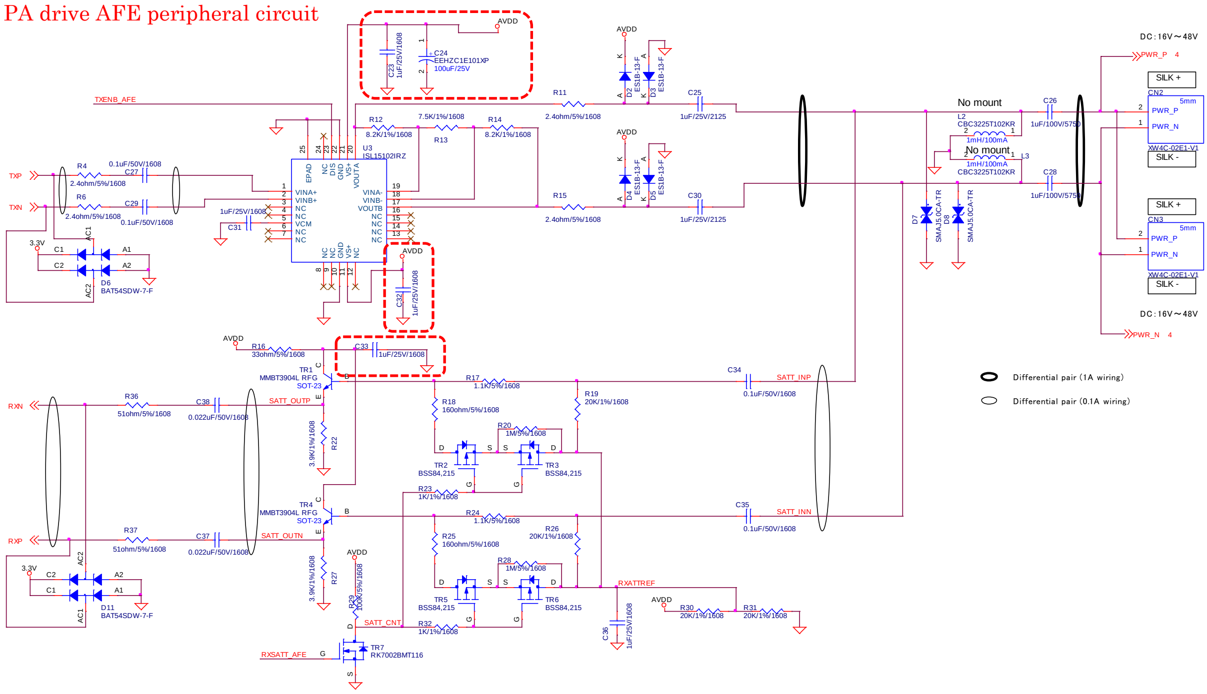
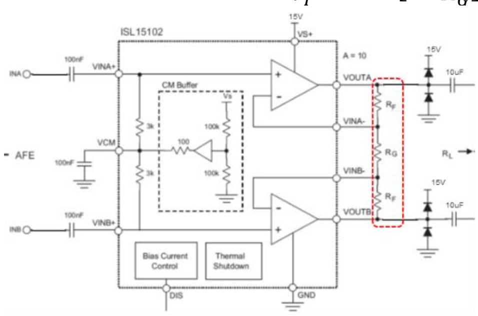


Figure 3-4 Connection example of PA drive AFE peripheral circuit

3.2.2 Setting the feedback resistor RF of PA(ISL15102)

- As a tendency of the frequency characteristics of ISL15102 described in the data sheet of ISL15102, when the feedback resistance RF of ISL15102 shown in the red circle in Figure 3-5(a) becomes smaller, the peak near 70MHz of the frequency characteristic shown in Figure 3-5(b) becomes large.
- In order to avoid the influence of this peak around 70MHz, by checking the RF oscillation stability and the influence on out-of-band noise, it has been confirmed that the oscillation amplitude is almost constant when RF = 8.2kΩ or more, and the out-of-band noise is the lowest when RF = 8.2kΩ.
- From this result, From this result, as shown in Figure 3-6, set the optimum value of RF(=R12=R14) to 8.2kΩ, RG to 7.5kΩ so that the voltage gain of ISL15102 is 10dB. The formula for the voltage gain of the ISL15102 is shown below.

ISL15102 voltage gain ⋯ $\frac{V_O}{V_I} = 1 + \left[2 \cdot \frac{R_F}{R_G}\right]$



(a) ISL15102 block diagram

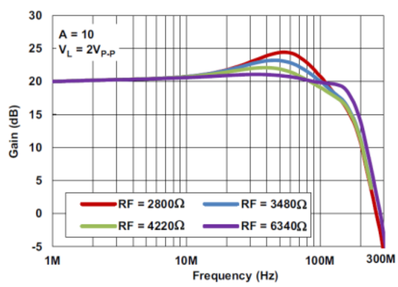


Figure 8. Small Signal Frequency Response vs R_F

(b) ISL15102 frequency characteristics vs RF

Figure 3-5 Catalog data of ISL15102

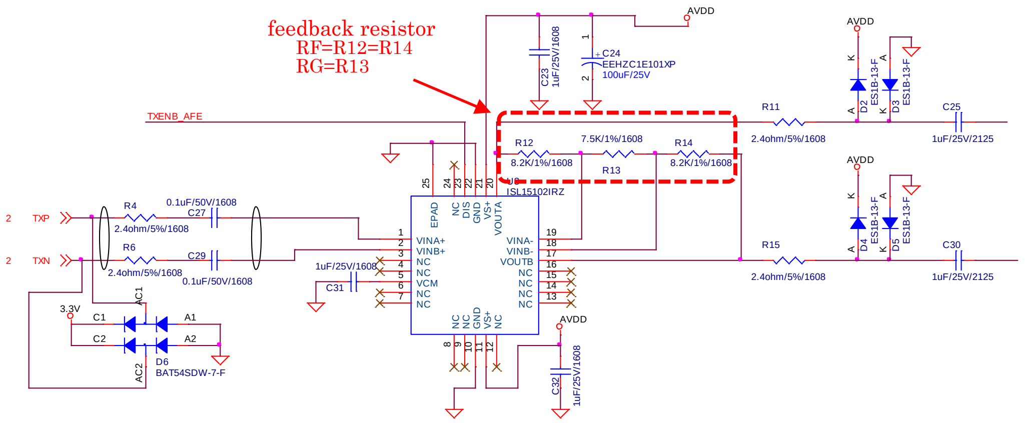


Figure 3-6 Setting the feedback resistor RF of ISL15102

3.2.3 Step attenuator circuit

This section describes the step attenuator (SATT) used in the PA drive AFE-RX.

- The function of SATT is to attenuate the received signal so that when a large amplitude signal or interference wave that exceeds the input level of the R9A06G061 is input, the receiving circuit can demodulate without becoming saturated. If the received signal is smaller than the specified amplitude, the received signal is passed through without attenuation.
- If the receiving circuit is saturated, unnecessary harmonics will be generated and it will be difficult to distinguish it from the received signal, so please insert a SATT circuit in the receiving circuit to prevent the receiving circuit from becoming saturated.
- Figure 3-7 shows how to control SATT.
  (1) Using the received preamble data, the level detection function of the digital baseband circuit of R9A06G061 determines whether the signal strength of the ADC output exceeds the signal level that saturates the receiving circuit.
  (2) If the received level exceeds the level that saturates the receiving circuit, the received signal is attenuated by switching the RXSATT signal from 0 to 1 and the SATT gain from 0dB to -18dB. Figure 3-8 shows an example of a SATT circuit mounted on a DC-PLC board.
- When the RXSATT signal is low level, the gain of the SATT circuit is 0dB, and when the RXSATT signal is high level, the gain of the SATT circuit is -18dB.
- The resistors that determine the gain of the SATT circuit are R18 and R22 and are determined by the following formula.

$$G_{SATT} = 20\log\left(\frac{R22}{R18+R22}\right) = 20\log\left(\frac{160}{1100+160}\right) = -17.93[\mathrm{dB}]$$

- If you are considering inserting a fixed attenuator circuit (fixed ATT) instead of a SATT circuit, the following cautions are required and we do not recommend it.
  - When inserting a fixed ATT=-18dB, signals with large amplitudes can be attenuated and demodulated without saturating the receiving circuit, similar to when using a SATT circuit. However, the minimum receiving sensitivity is 18dB worse than when using the SATT circuit.
  - When inserting a fixed ATT=-6dB, the signal amplitude that can be received without saturating the receiving circuit is 1/4 (-12dB) compared to -18dB, so it is necessary to check the receivable signal level. Also, the minimum receiving sensitivity is 6dB worse than when using the SATT circuit.
  - When fixed ATT=0dB, the minimum receiving sensitivity is the same as when using a SATT circuit. However, signals with large amplitudes exceeding the input level of R9A06G061 will generate harmonics due to saturation, making it difficult to identify the received signal.

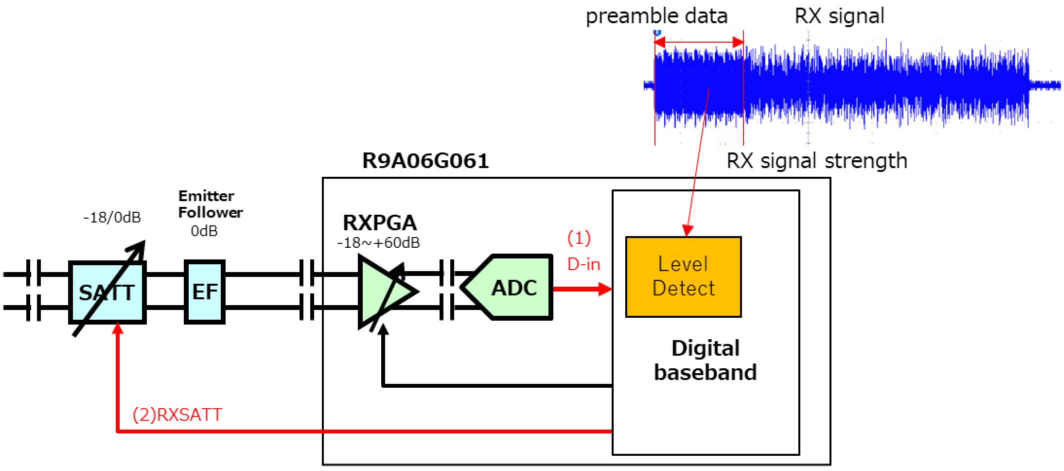


Figure 3-7 Step Attenuator (SATT) control method

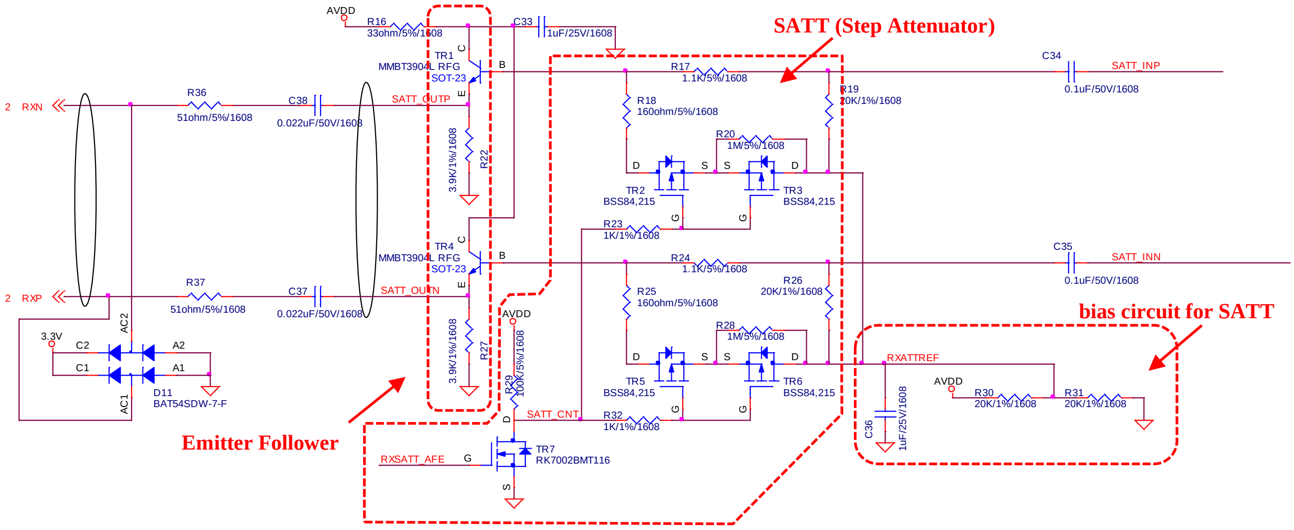


Figure 3-8 Step Attenuator (SATT) circuit example

3.2.4 PA drive protection circuit

Figure 3-9 shows an example of connecting a protection circuit for PA drive. Select a protection element considering the expected noise level.

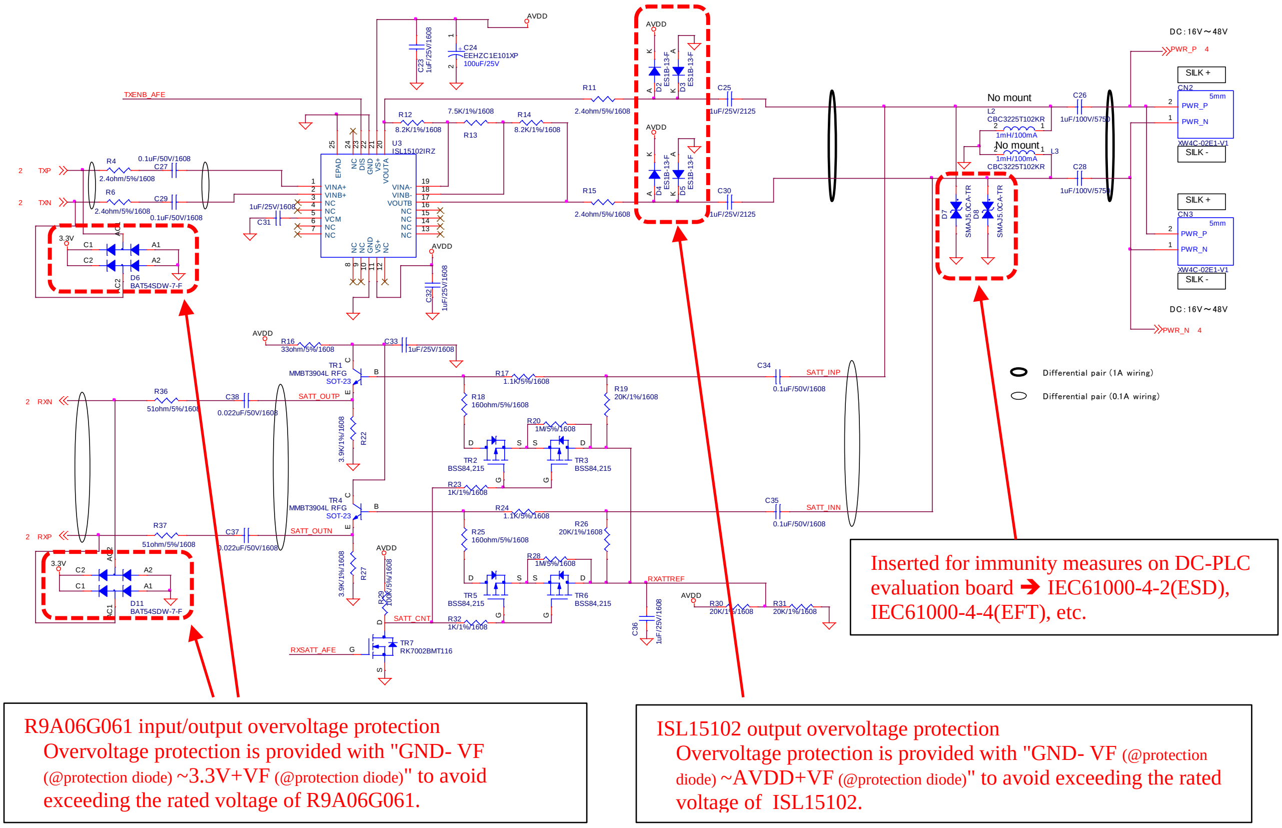


Figure 3-9 Connection example of PA drive protection circuit

3.2.5 Cautions on PCB layout of PA drive AFE circuit

- Figure 3-10 shows cautions for PCB layout of the PA drive AFE circuit.
- Place the decoupling capacitance near the terminals and shorten the wiring pattern for "ISL15102 VS+ (11pin, 21pin)" and "RX circuit emitter follower" of the PA drive AFE circuit. In particular, "VS+ (21pin) of ISL15102" is a PA output power supply, so please place 1uF and 100uF as close to the terminal as possible.
- The recommended output signal wiring width for AFE-TX (ISL15102) is 1 mm or more, considering that a current of about 1 A flows depending on the load.
- The TX signal lines between R9A06G061 - AFE TX(ISL15102) - DC IN/PLC signal terminals are differential signals, so arrange the components symmetrically, and wire them with the same length as much as possible and the shortest and symmetrical wiring in a well-balanced manner.
- The RX signal lines between DC IN/PLC signal terminals - AFE RX - R9A06G061 are differential signals, so arrange the components symmetrically, and wire them with the same length as much as possible and the shortest and symmetrical wiring in a well-balanced manner. However, if there is a risk of interference with the power circuit, give priority to increasing the distance (at least 3 cm) between the RX signal line and the power circuit. (Wiring route example is shown in Figure 3-11)
- It is assumed that the AVDD (12V) power supply pattern contains a lot of noise. Therefore, please avoid crossing the power supply pattern with the TX/RX signal line and its components as much as possible.
- On the power supply layer (3rd layer), use a GND pattern as much as possible in the area that overlaps with the TX/RX signal line and its components. (Figure 5-4 shows an example of the GND pattern of the power layer)

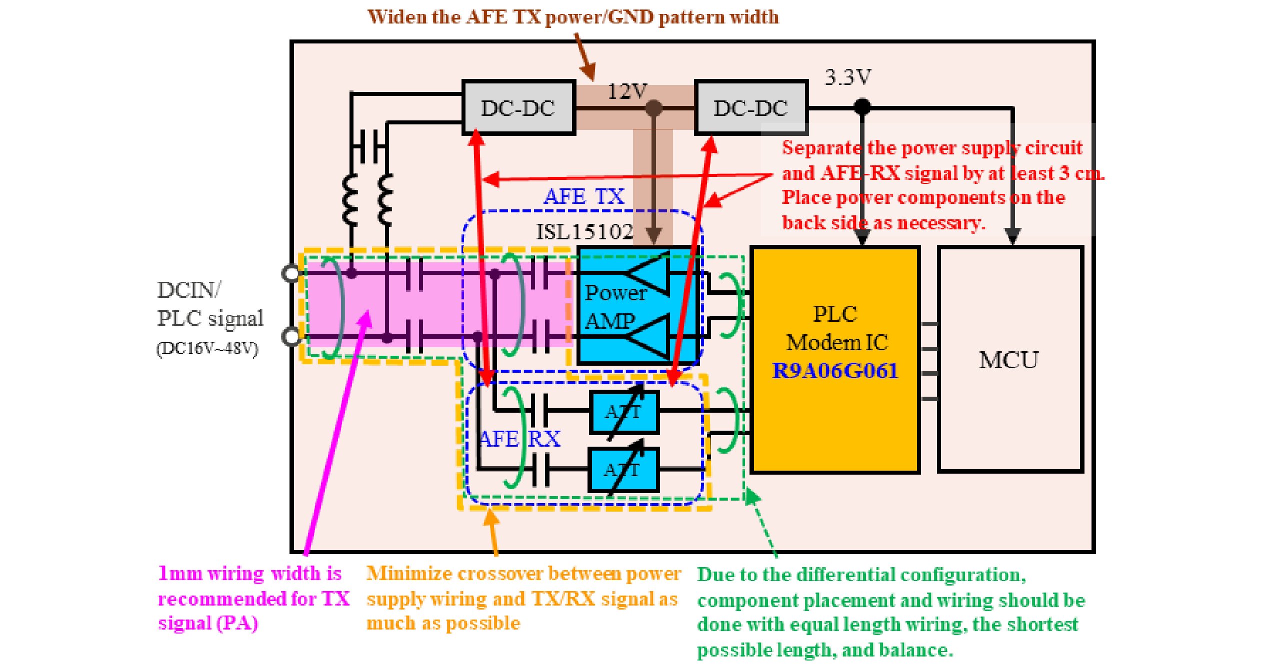


Figure 3-10 Cautions on PCB layout of PA drive AFE circuit

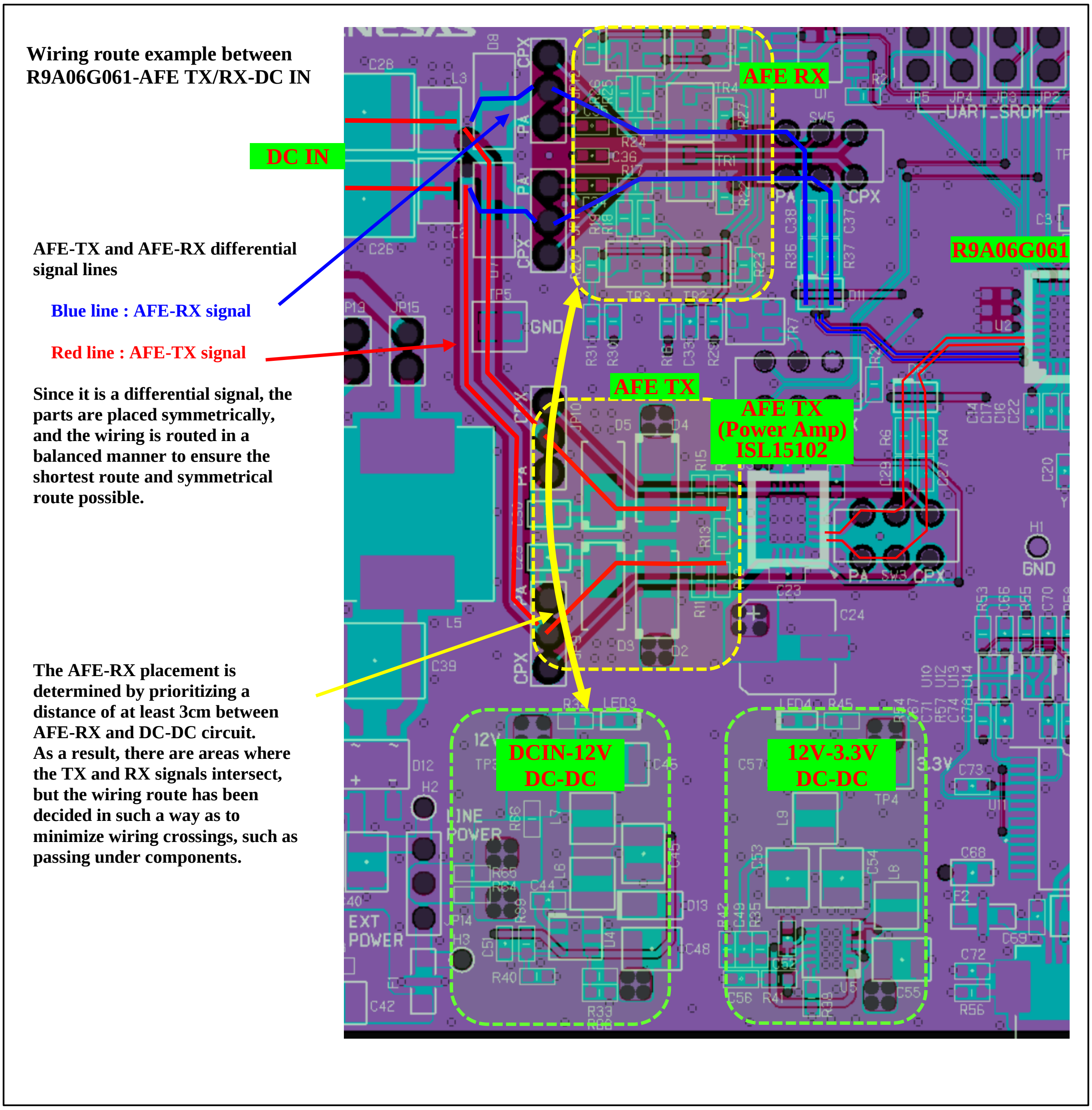


Figure 3-11 Wiring route example between R9A06G061-AFE TX/RX-DC IN

4. Cautions when designing DC-DC power supply circuits

4.1 Cautions when designing DC-DC power supply circuits

This section explains cautions when designing DC-DC power supply circuits by mounting DC-DC power supply ICs on a DC-PLC board.

- It is necessary to generate 3.3V to use R9A06G061 and 12V to use ISL15102 on the DC-PLC board.
- When using a DC-DC power supply circuit, operating switching noise may affect the PLC signal and circuit.
- To avoid affecting the signal band (35kHz-500kHz) of the NB-PLC, use a DC-DC power supply IC that can select a switching frequency of 1MHz or higher.
- For the switching operation of the DC-DC power supply circuit, use a DC-DC power supply IC that has a PWM (Pulse Width Modulation) fixed operation function. The operation method of PFM (Pulse Frequency Modulation) and PSM (Pulse Skipping Modulation) may operate within the signal band of NB-PLC (35kHz-500kHz), which may affect the characteristics of PLC.
- In order to suppress the influence on other power supply circuits and PLC circuits, it is recommended to insert an LC filter at the input section of the DC-DC power supply circuit in order to remove noise contained in the input power supply and reduce the effects of switching noise generated in the DC-DC power supply circuit. Figure 4-1 shows a circuit example of an input filter for a DC-DC power supply circuit, and Table 4-1 shows an example of its circuit constants.
- When generating the power supply voltage on the DC-PLC board from the supply voltage of the DC power line, the load impedance of the PLC must be high so that the load impedance of the DC-PLC is not affected by the input impedance of the DC-DC power circuit. there is. Therefore, it is recommended to insert an impedance upper circuit into the voltage supply path from the DC power line. (See section 4.2 for details)
- Figure 4-2 shows an example of DC-DC power supply circuits that generate 12V and 3.3V from DC supply voltage of 16V to 48V using MP2456GJ and ISL85415.

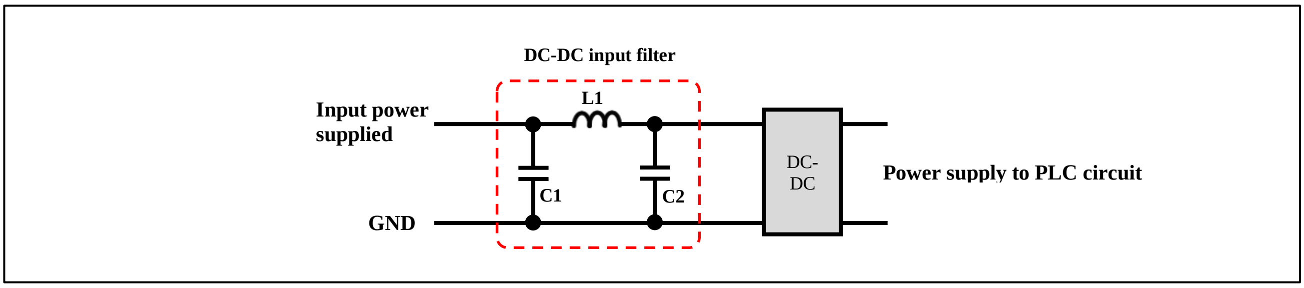


Figure 4-1 Example of input filter for DC-DC power supply circuit

Table 4-1 Example of circuit constants of input filter for DC-DC power supply circuit

	Circuit constant
L1	10uH
C1	10uF-22uF
C2 [1)]	10uF-22uF

Note 1) C2 can be omitted if the input capacitor of the DC-DC power supply circuit is 10uF or more.

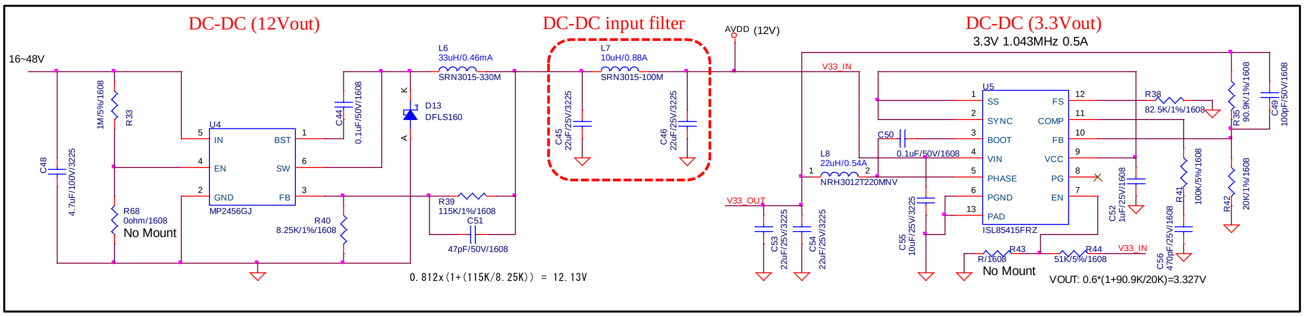


Figure 4-2 Example of DC-DC power supply circuits

4.2 Input circuit of DC power line ~ DC-DC power circuit

Figure 4-3 shows an example of the input circuit that connects the DC power line to the DC-DC power circuit on the DC-PLC board.

When generating the power supply voltage on the DC-PLC board from the supply voltage of the DC power line, it is recommended to insert an impedance upper circuit (L4, L5) for the purpose of increasing the load impedance of the DC-PLC so that the DC-PLC is not affected by the input impedance of the DC-DC power supply circuit. In addition, it is recommended to add C39 and insert a low-pass filter consisting of L4, L5, and C39 for the purpose of removing the PLC signal so that it does not affect the DC-DC power supply circuit side. Figure 4-4 shows an example of the characteristics of an impedance upper circuit.

The inductance values of L4 and L5 are determined by taking into account that the input impedance of the DC-PLC receiver is 1kΩ to 1.5kΩ. The impedance in the frequency band used is set to approximately double so that the impedance on the power circuit side does not affect the input impedance of the DC-PLC receiver.

In Figure 4-3, L4 and L5 are 2.7mH, so for example, the impedance Z_L at 150kHz is as follows.

$$Z_L = 2\pi f L = 2 \times 3.14 \times 150kHz \times 2.7mH = 2.54k\Omega$$

Note that the load impedance of the DC-PLC changes depending on the number of DC-PLC-equipped devices and other systems connected to the DC Power Line.
Therefore, it is necessary to determine the Z_L value after considering the assumed system and the driving capacity of the DC-PLC board and performing evaluation as necessary.
In addition, the cutoff frequency of the low-pass filter consisting of L4, L5 and C39 is 3.06kHz as shown in the following formula, which is a sufficiently low value compared to the NB-PLC signal band (35kHz-500kHz).

$$f_{cutoff} = 1/2\pi\sqrt{LC} = 1/(2 \times 3.14 \times \sqrt{(2.7mH \times 1uF)} = 3.06kHz$$

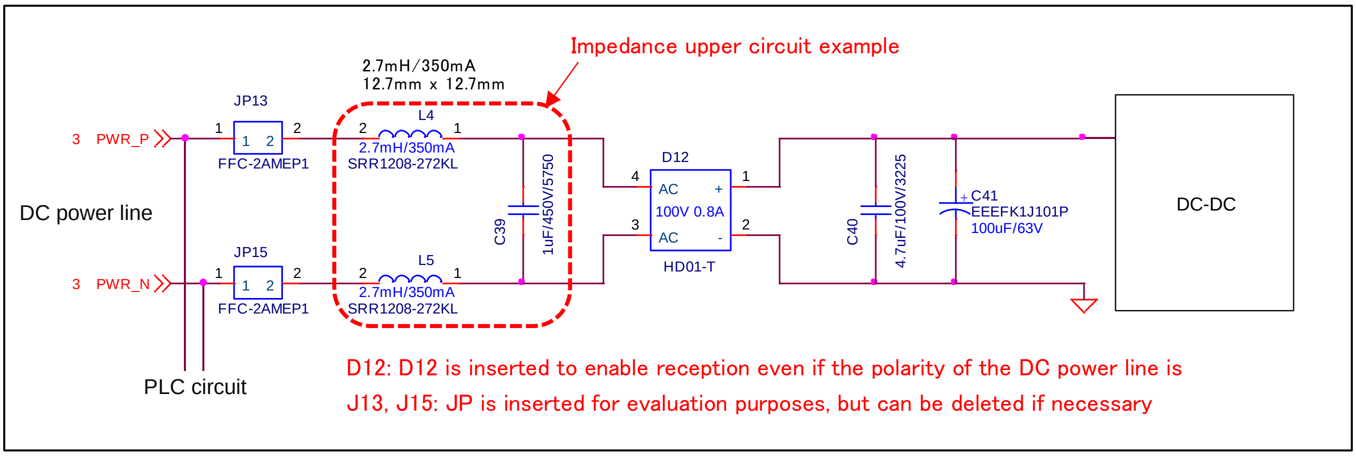
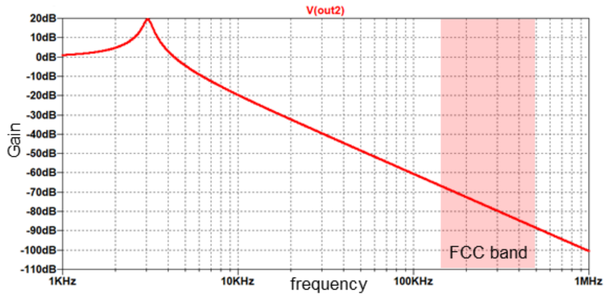
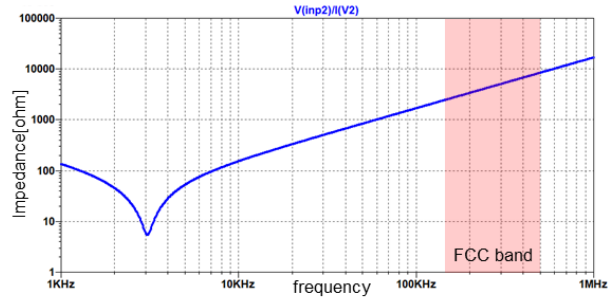


Figure 4-3 Input circuit example of DC power line ~ DC-DC power circuit



(a) Transfer characteristics of the impedance upper circuit in Fig.4-3



(b) Impedance characteristics of the impedance upper circuit in Fig.4-3

Figure 4-4 Characteristic example of impedance upper circuit in Fig.4-3

5. Cautions on PCB layout of GND and power supply of DC-PLC board

5.1 Cautions on GND Patterns

5.1.1 Cautions regarding GND reinforcement and heat dissipation design

- For DC-PLC board design, it is recommended to use a PCB substrate with 4 or more layers.
  - The 1st layer is used as the signal layers, fill the unused area with GND patterns for strengthen the GND, heat dissipation, and signal separation.
  - For the 2nd layer, it is important to use the GND layer for signal separation, strengthen the GND, noise shielding and heat dissipation.
  - The 3rd layer is used as the power supply layer, and it is recommended to place a GND pattern partially for noise shielding and heat dissipation.
  - The 4th layer is used as the signal layer and fill the unused area with GND patterns for strengthen the GND, heat dissipation, and signal separation.
- There is the exposed die pad (internally connected to GND) on the back side of R9A06G061 and ISL15102 for heat dissipation. Place GND pattern to connect the exposed die pad on 1st layer, 2nd layer, 3rd layer and 4th layer, and connect the GND pattern of each layer with via holes. Place via holes as much as possible on GND pattern (recommendation: hole diameter: 0.3mm, R9A06G061: more than 12 pcs, ISL15102: more than 9pcs). Figure 5-1 shows an example of the PCB layer structure and GND pattern of a DC-PLC board.
- In the 1st layer, connect the Exposed die pad of ISL15102 to the GND plane of the first layer as much as possible to improve heat dissipation. (An example is shown in Figure 5-2.)
- In the GND layer of the 2nd layer, connect the path to the GND supply terminal on the PCB smoothly with the Exposed die pad of R9A06G061 and ISL15102. (An example is shown in Figure 5-3.)
- In the power supply layer of the 3rd layer, place a GND pattern as much as possible in the via hole part connected to the exposed die pad of R9A06G061, ISL15102, and in the area that overlaps with the TX/RX signal wiring and its components. (An example of 3-layer connection is shown in Figure 5-4)
- In the 4th layer, the GND pattern is especially important for heat dissipation design. In order to further improve heat dissipation performance, widen the area of the GND pattern and connect the Exposed die pad of R9A06G061, ISL15102 to the GND pattern. Then, connect as smoothly as possible so that there are no obstacles in the path to the Exposed die pad of the ISL15102 and the GND supply terminal on the PCB. (An example is shown in Figure 5-5.) (Reason: Since large current flows in ISL15102 (Power amplifier for transmission) when transmitting at low load, heat dissipation will deteriorate if the connection between the Exposed die pad of ISL15102 and the GND pattern is not appropriate. Then, the thermal shutdown function of the ISL15102 may intermittently stop the output of the signal.)
- When checking PCB artwork, in the paste mask (paste data) used for component mounting, it is recommended to check if the appropriate pattern is placed on the exposed die pad part of R9A06G061 and ISL15102. (See Figure 5-6 for details.)
- Fill the unused area of 1st and 4th layer as the signal layer with GND patterns. However, if the GND pattern becomes a small island or fine antenna-shape, it is not necessary to fill it.

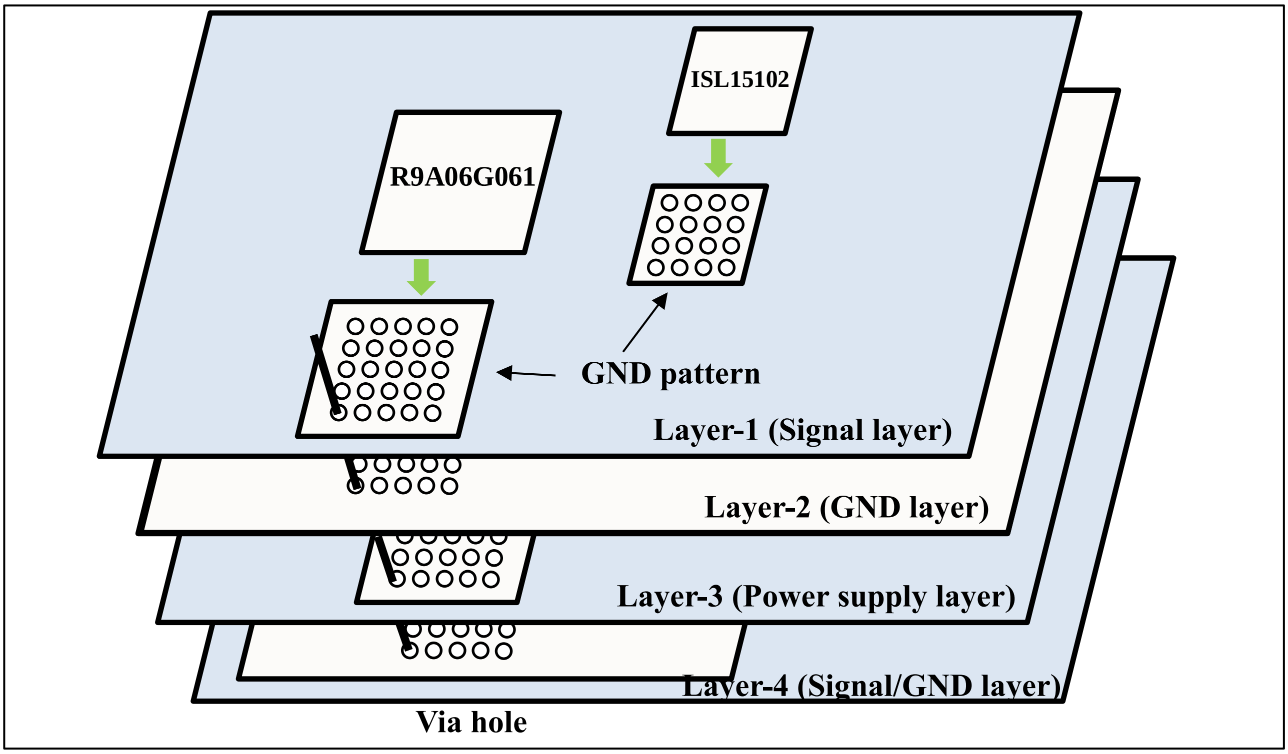
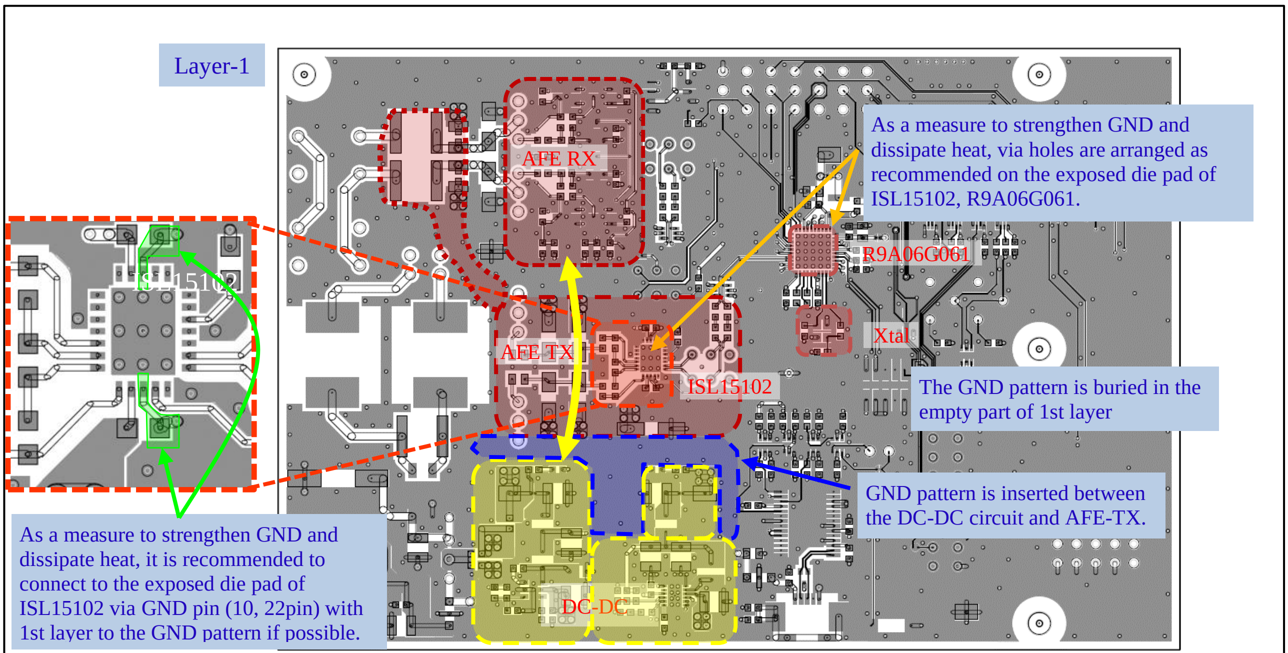
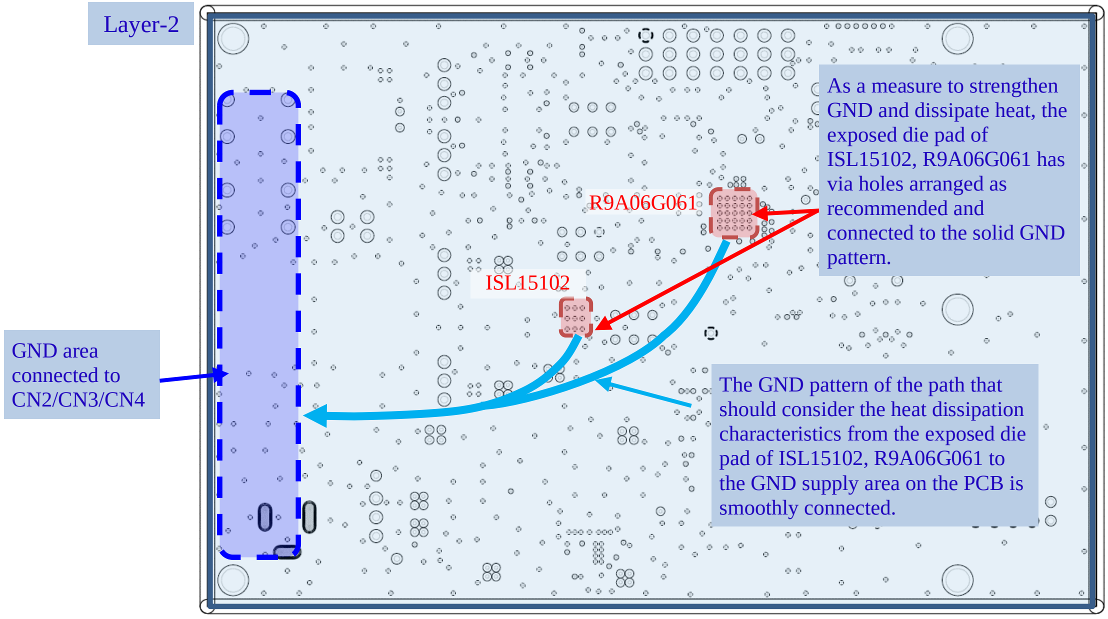


Figure 5-1 Example of PCB Substrate Configuration and GND pattern for the DC-PLC Board



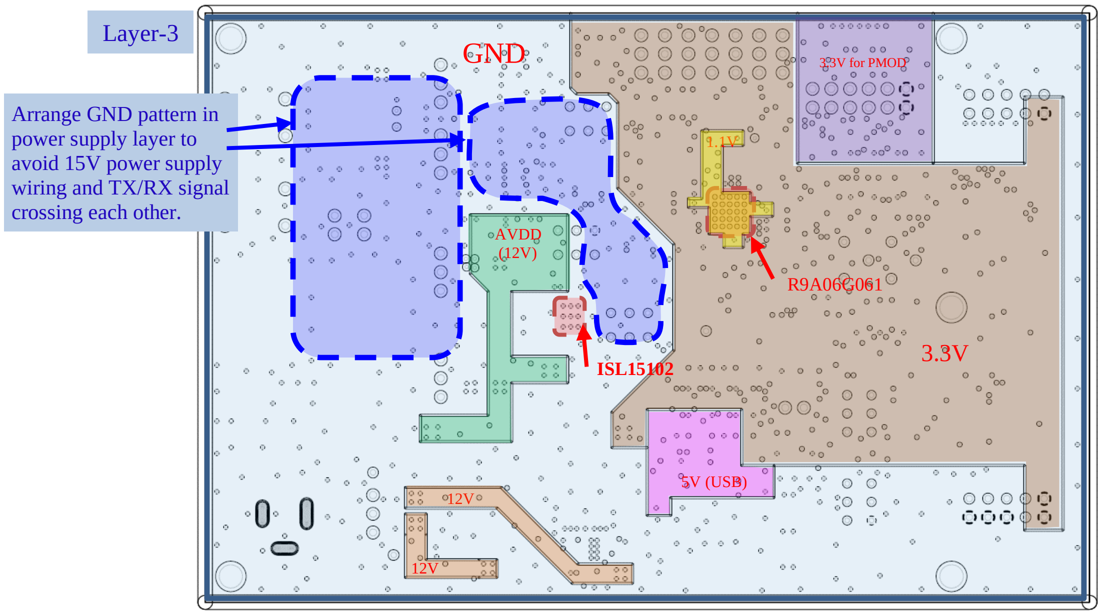
- The GND pattern is buried in the empty part of 1st layer
- As a measure to strengthen GND and dissipate heat, via holes are arranged as recommended on the exposed die pad of ISL15102, R9A06G061. It is recommended to connect to the exposed die pad of ISL15102 via GND pin (10, 22pin) with 1st layer to the GND pattern if possible.
- The distance between the DC-DC circuit and AFE-RX is maintained, and a GND pattern is inserted between the DC-DC circuit and AFE-TX.

Figure 5-2 Example of connection between exposed die pad of R9A06G061 and ISL15102 and GND pattern (1st Layer)



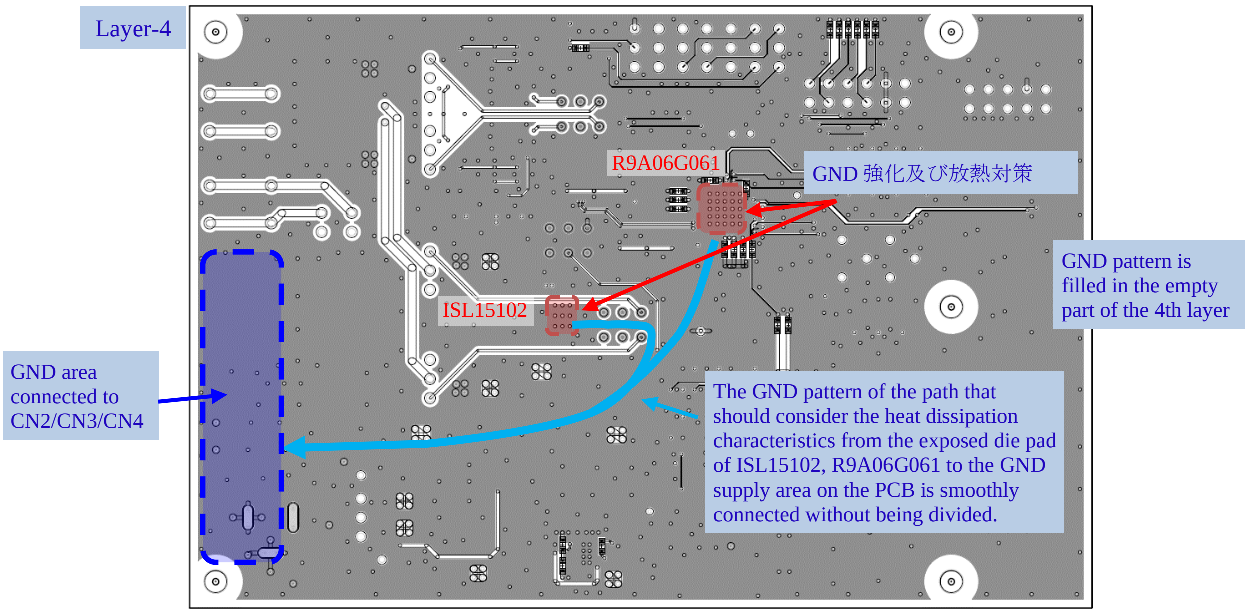
- As a measure to strengthen GND and dissipate heat, the exposed die pad of ISL15102, R9A06G061 has via holes arranged as recommended and connected to the solid GND pattern.
- The GND pattern of the path that should consider the heat dissipation characteristics from the exposed die pad of ISL15102, R9A06G061 to the GND supply area on the PCB is smoothly connected.

Figure 5-3 Example of connection between exposed die pad of R9A06G061 and ISL15102 and GND pattern (2nd Layer)



- The GND pattern is embedded in the part connected to the exposed die pad part of ISL15102 on 3rd layer. In this figure, the exposed die pad part of R9A06G061 is in the 1.1V region, but it is desirable to set it in the GND region if possible.
- In the wiring area of the TX / RX signal, a GND pattern is arranged to avoid crossing with the noisy 15V power supply pattern. (Blue part)

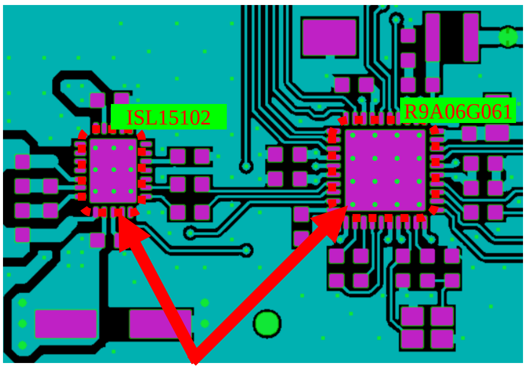
Figure 5-4 Example of connection between exposed die pad of R9A06G061 and ISL15102 and GND pattern (3rd Layer)



- GND pattern is filled in the empty part of the 4th layer.
- As a measure to strengthen GND and dissipate heat, the exposed die pad of ISL15102, R9A06G061 has via holes arranged as recommended and connected to the solid GND pattern.
- The GND pattern of the path that should consider the heat dissipation characteristics from the exposed die pad of ISL15102, R9A06G061 to the GND supply area on the PCB is smoothly connected without being divided.

Figure 5-5 Example of connection between exposed die pad of R9A06G061 and ISL15102 and GND pattern (4th Layer)

Cyan: 1st layer / Magenta: Top Paste Mask / Yellow green: via hole



Confirm that there is paste mask data in the exposed die pad part of R9A06G061 and ISL15102.

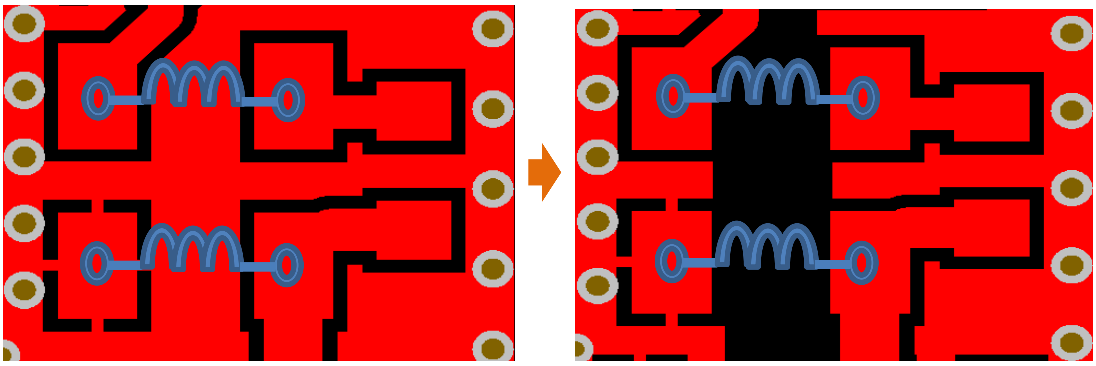
- When checking the PCB artwork, it is recommended to check if the appropriate patterns are placed on the exposed die pad part of R9A06G061 and ISL15102 in the paste mask (paste data) used for component mounting.
- If the paste mask does not have a pattern to connect to the exposed die pad of R9A06G061 and ISL15102, the operation will be unstable because R9A06G061 and ISL15102 will not be connected to GND. In addition, the heat dissipation of the ISL15102 deteriorates, and as a result, the output of the signal is intermittently stopped by the thermal shutdown function of the ISL15102.
- Mask to check: Paste mask extension GTP, GBP, etc. (The mask used for assembling parts))
    - GTP : Top Paste Mask
    - GBP : Bottom Paste Mask
- The Gerber file provided by the board vendor may not contain the paste mask data. In that case, request the paste mask data from the board vendor.

- There is a solder mask as mask data for PCB that can be easily mistaken for a paste mask (sometimes called resist data, etc.). Solder masks are used only when manufacturing boards, and paste masks are used when assembling parts.
- Solder mask extension GBS, GBS, etc. (mask used when manufacturing the board)
    - GTS: Top Solder Mask
    - GBS: Bottom Solder Mask

Figure 5-6 Example of checking the paste mask (paste data) used for component mounting

5.1.2 Cautions on other GND Pattern

- For the low voltage circuit domain GND, it is recommended to use the GND solid pattern instead of separating GND for the digital circuit and GND for the analog circuit.
- Do not place a GND pattern under the inductance as shown in Figure 5-7 to avoid noise influences on the GND pattern. (e.g. Inductors used in power supply circuits, power supply filters, etc.)



The GND pattern under the inductance must not locate it.

Figure 5-7 Cautions on GND patterns under the inductor

5.2 Cautions on the Power Supply Pattern

- It is recommended to configure the power supply layer with the PCB substrate configuration of the PLC board as shown in Figure 5-1.
- It is recommended to arrange 1.1V/3.3V/12V power regions used in the PLC board for the power supply layer, and arrange the GND pattern in the area where crossing with the power region should be avoided.
- Figure 5-4 show examples of the power supply layer.

6. Power Filter board design example

The Power Filter board is used to achieve stable DC-PLC when the impedance of the power supply on the DC Power Line or other systems is low. The Power Filter board provides the following two functions:

- Impedance upper : By inserting a Power Filter board, the load impedance is increased to prevent DC-PLC communication signal attenuation and improve communication quality.
- Low pass filter : To prevent the PLC signal from affecting the power supply or other systems on the DC Power Line, a low-pass filter suppresses the PLC signal, prevents noise from affecting the entire system, and maintains stable operation.

Figure 6-1 shows a circuit example of the Power Filter board, Figure 6-2 shows an example of the characteristics of the Power Filter board, and Figure 6-3 shows an example of how to use the Power Filter board. When calculating the impedance as the impedance upper in Figure 6-1, the inductance value of L201 and L202 is 1mH, so as an example, the impedance Z_L at 150kHz is as follows.

$$Z_L = 2\pi f L = 2 \times 3.14 \times 150kHz \times 1mH = 942\Omega$$

Note that the load impedance of the DC-PLC changes depending on the number of DC-PLC devices and other systems connected to the DC Power Line. Therefore, it is necessary to determine the ZL value after considering the assumed system and the driving capacity of the DC-PLC board and performing evaluation as necessary.

In addition, the cutoff frequency of the low-pass filter composed of L201 and C201 is 1.59kHz as shown in the following formula, which is a sufficiently low value compared to the NB-PLC signal band (35kHz-500kHz).

$$f_{cutoff} = 1/2\pi\sqrt{LC} = 1/(2 \times 3.14 \times \sqrt{(1mH \times 10uF)} = 1.59kHz$$

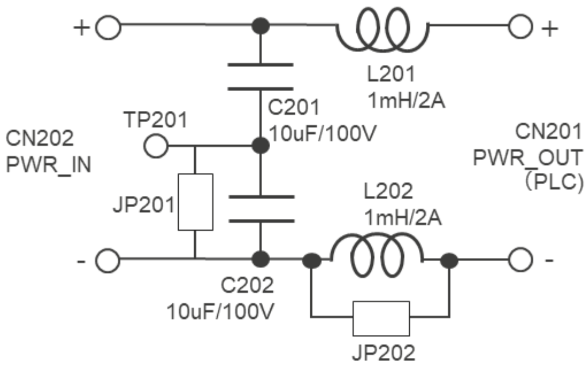
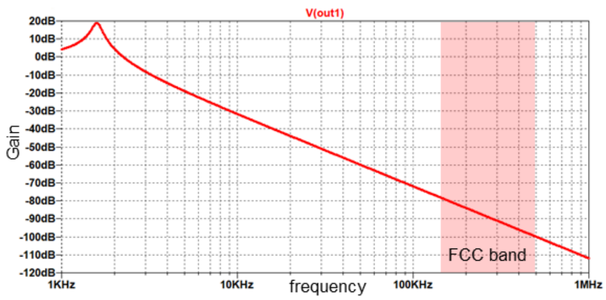
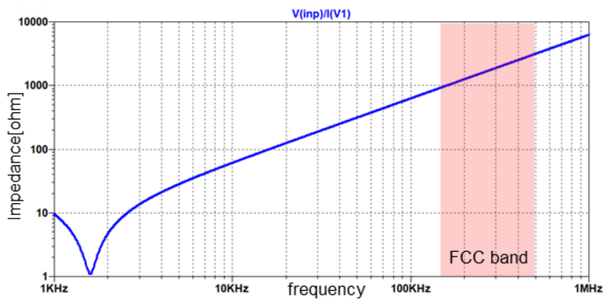


Figure 6-1 Power Filter board circuit example



(a) Transfer characteristics seen from the CN201 side



(b) Impedance characteristics seen from the CN201 side

Figure 6-2 Characteristic example of Power Filter board

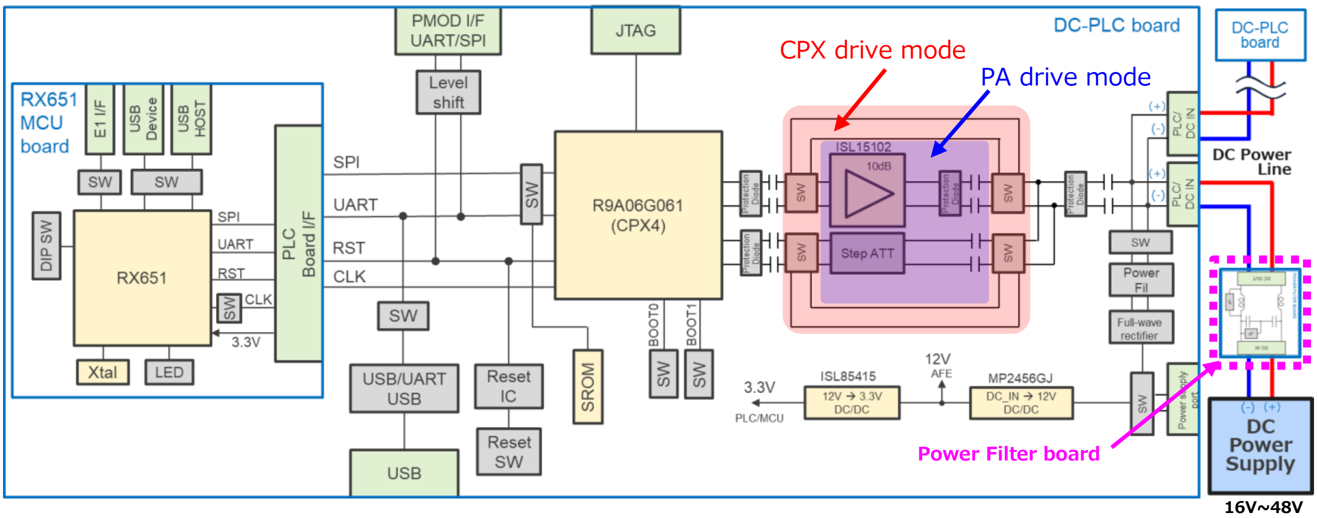


Figure 6-3 Example of using Power Filter board

7. Circuit design example

- This chapter provides a circuit design example of Renesas Electronics' DC-PLC evaluation kit RTK0EE0009D01001BJ for reference.
- If the contents of Chapters 2 to 4 differ from the circuit design examples in this chapter, please give priority to the contents of Chapters 2 to 4.
- Circuit design examples are shown in Section 7.1 (Figure 7-1-Figure 7-8), and Bill of materials examples are shown in Section 7.2 (Table 7-1-Table 7-5).

7.1 Example of circuit design

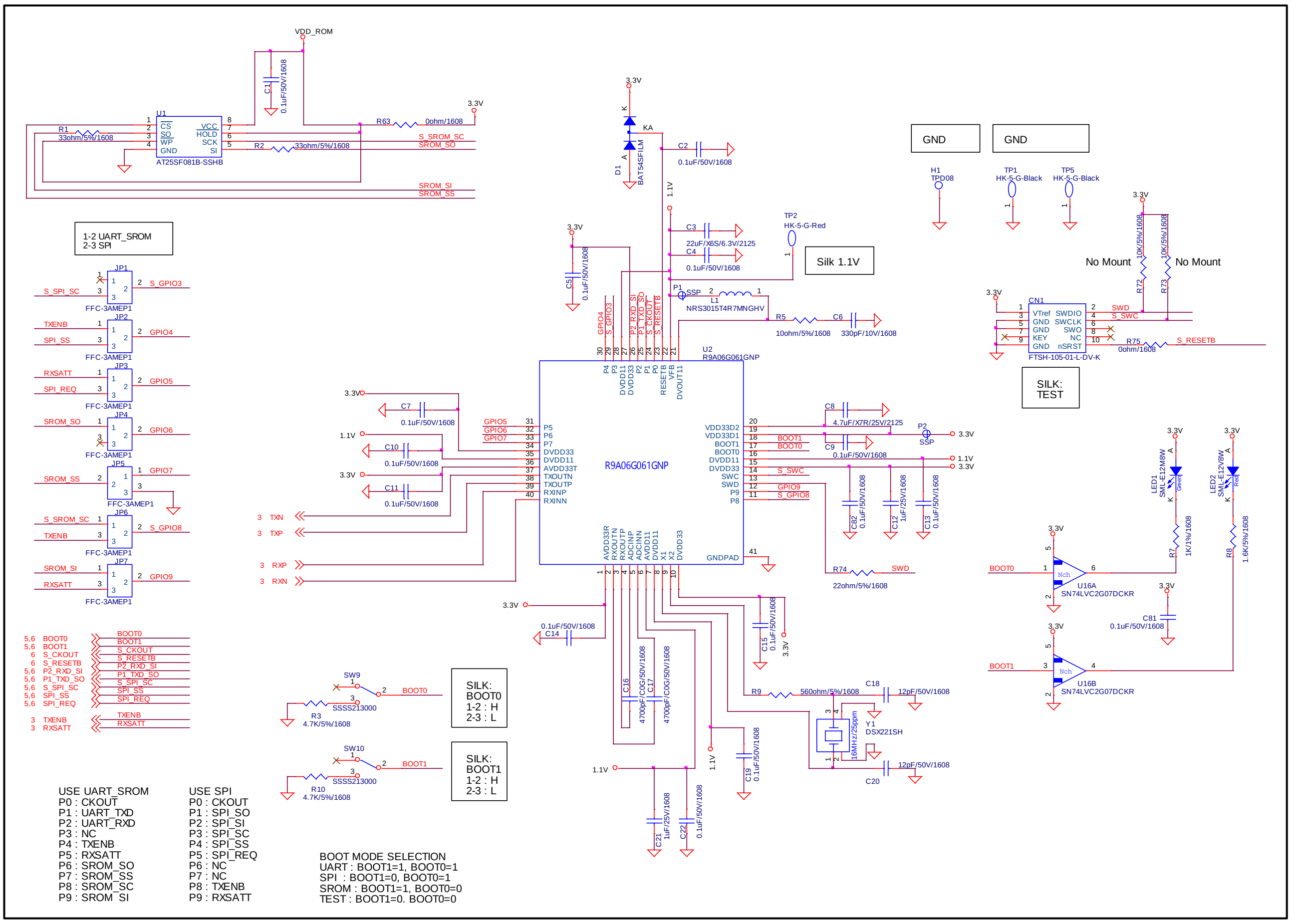


Figure 7-1 DC-PLC board (R9A06G061 peripheral circuit)

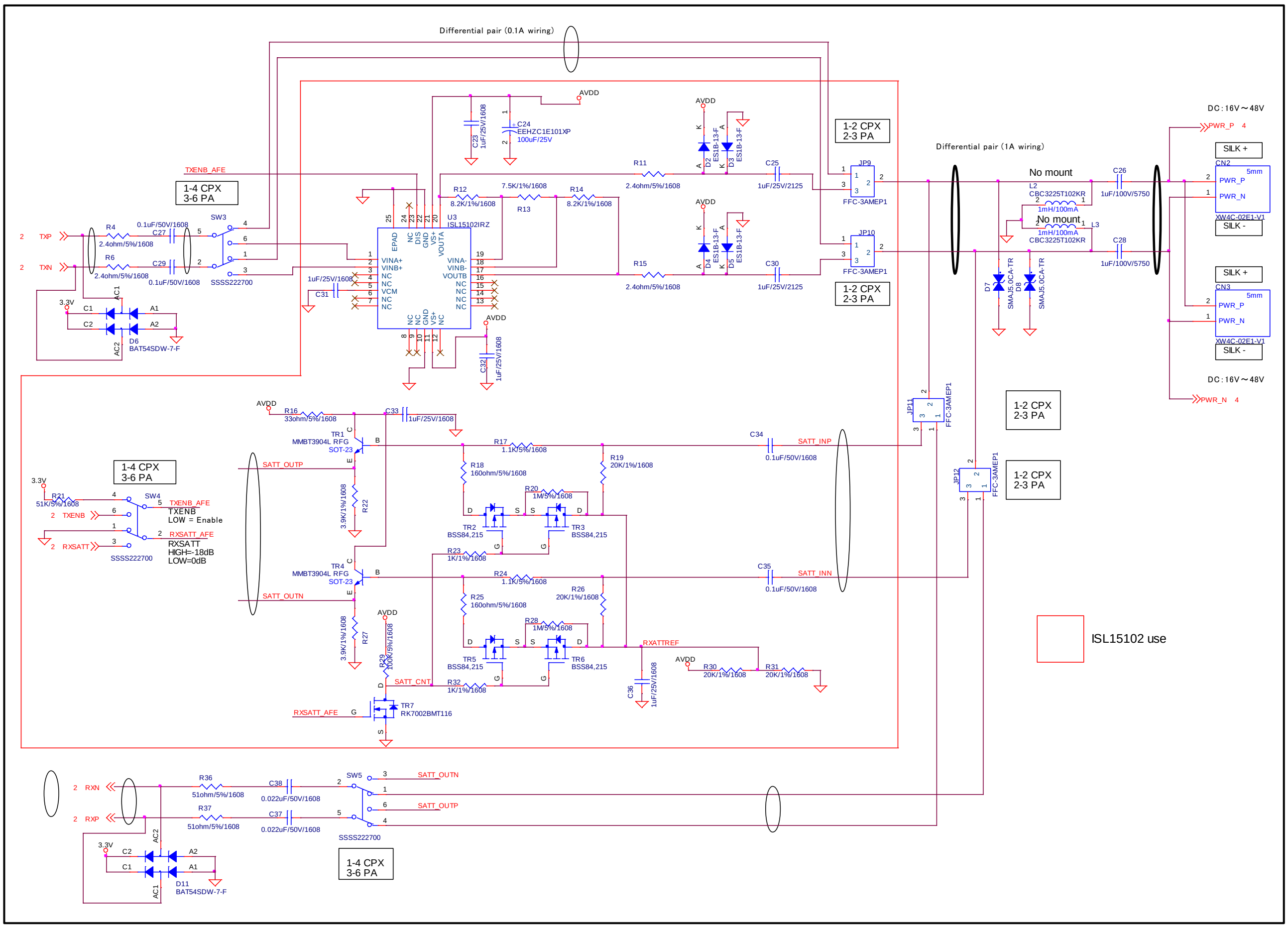


Figure 7-2 DC-PLC board (AFE peripheral circuit)

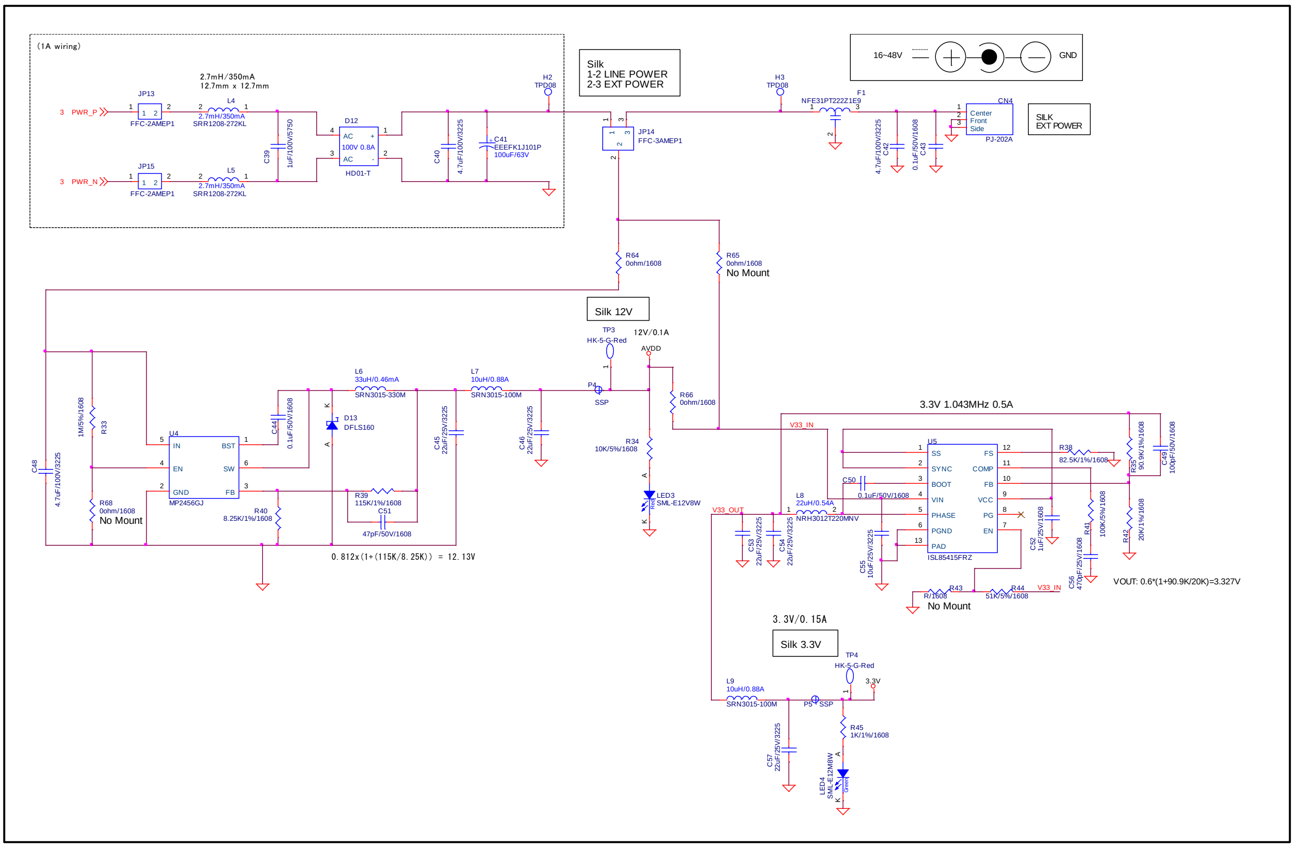


Figure 7-3 DC-PLC board (DC-DC power supply circuit)

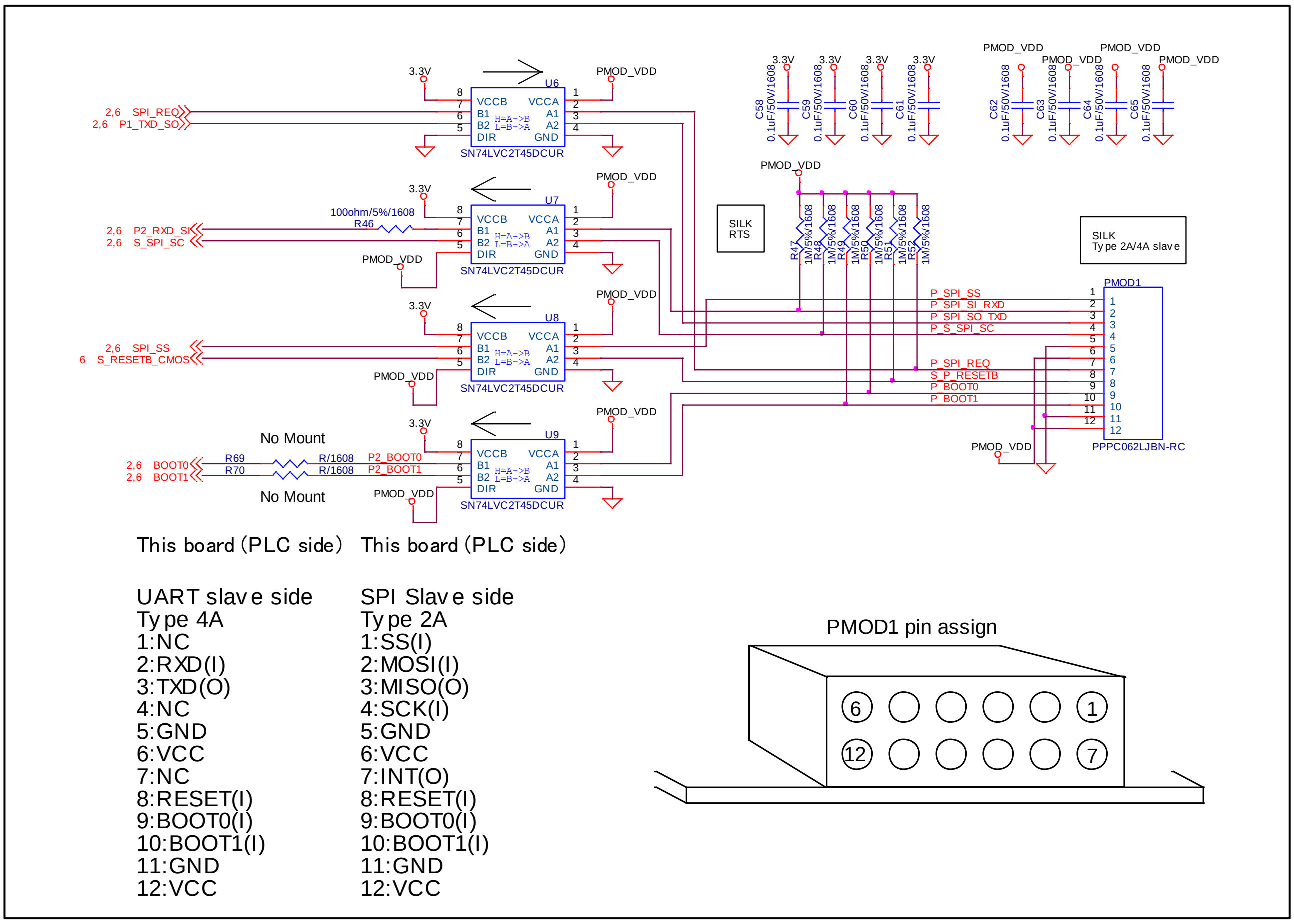


Figure 7-4 DC-PLC board (PMOD interface circuit)

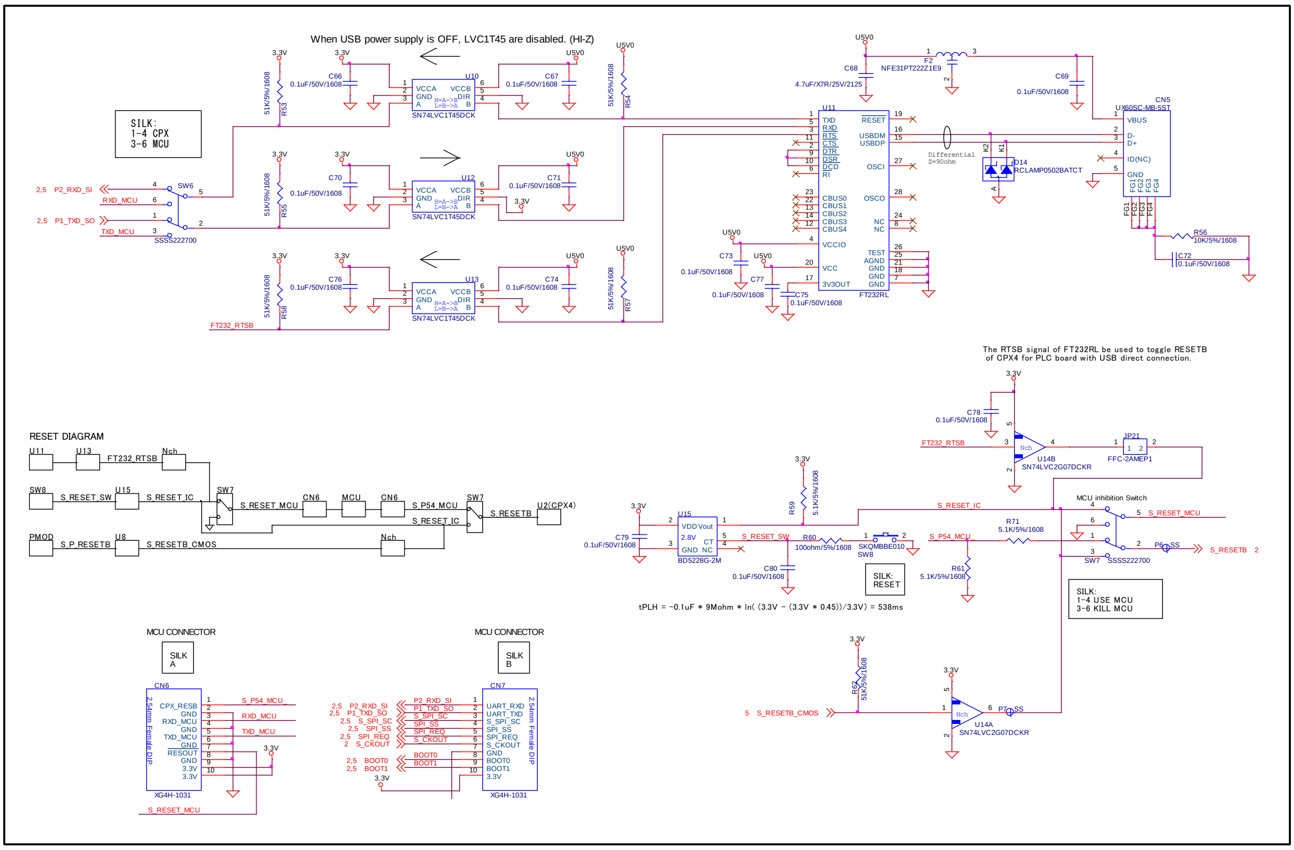


Figure 7-5 DC-PLC board (USB-serial circuit and RESET circuit)

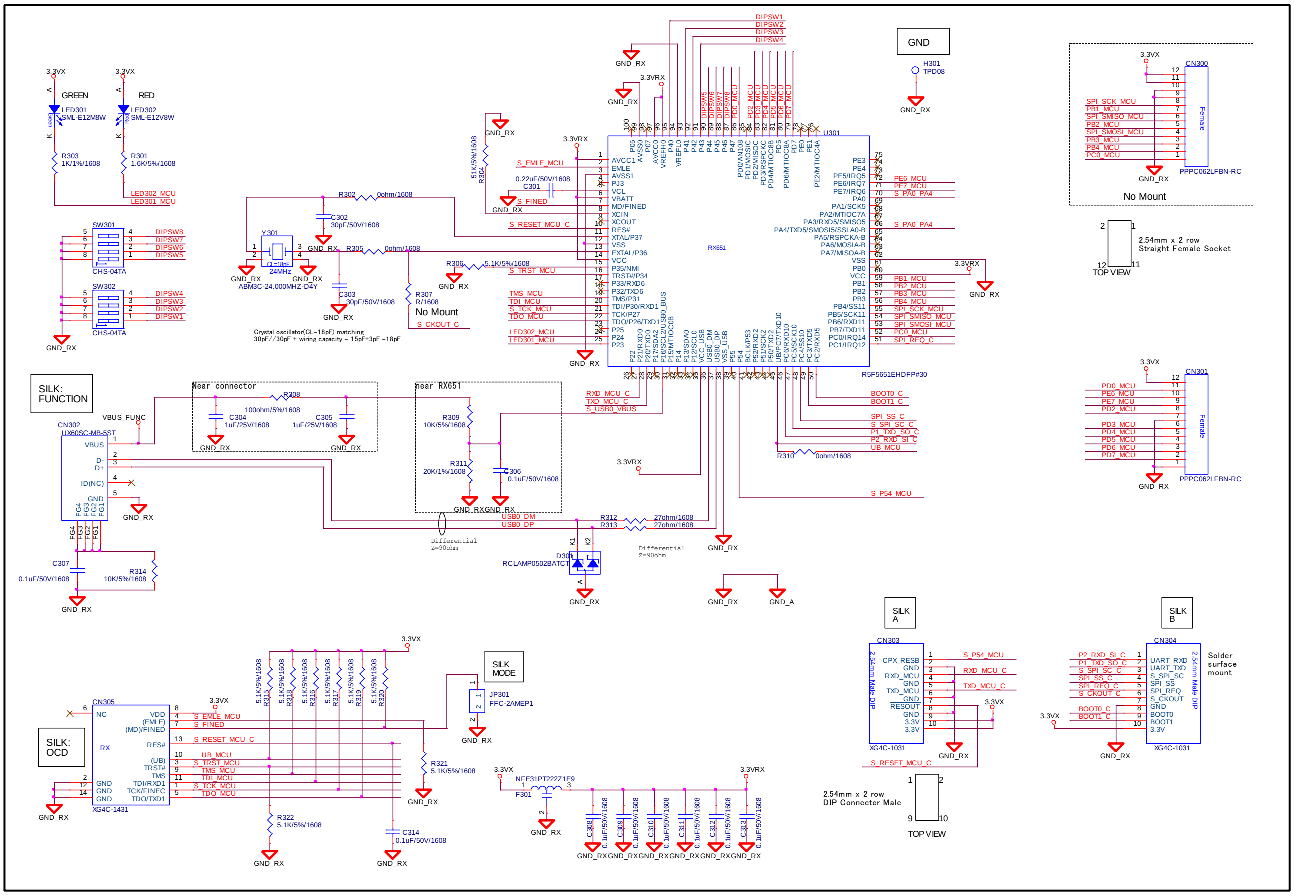


Figure 7-6 RX651 MCU board

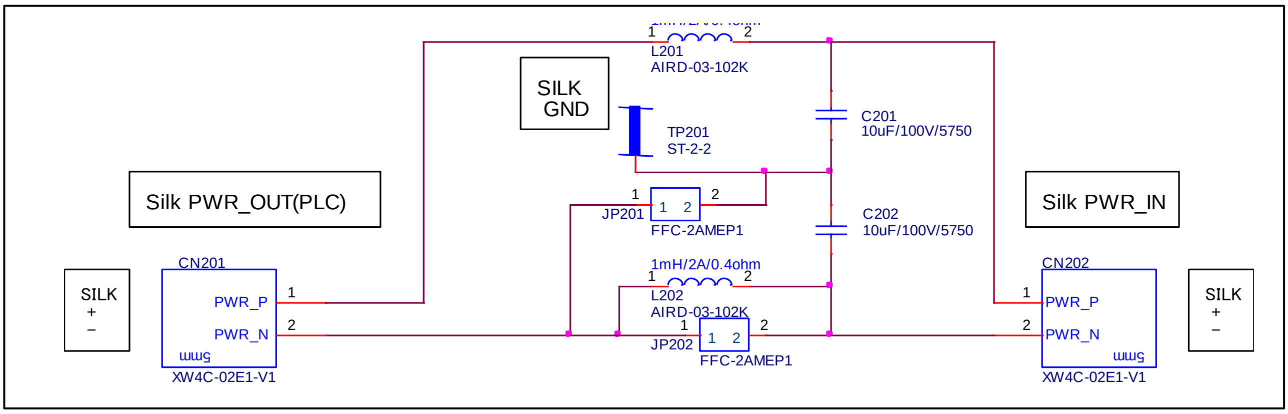


Figure 7-7 Power Filter board

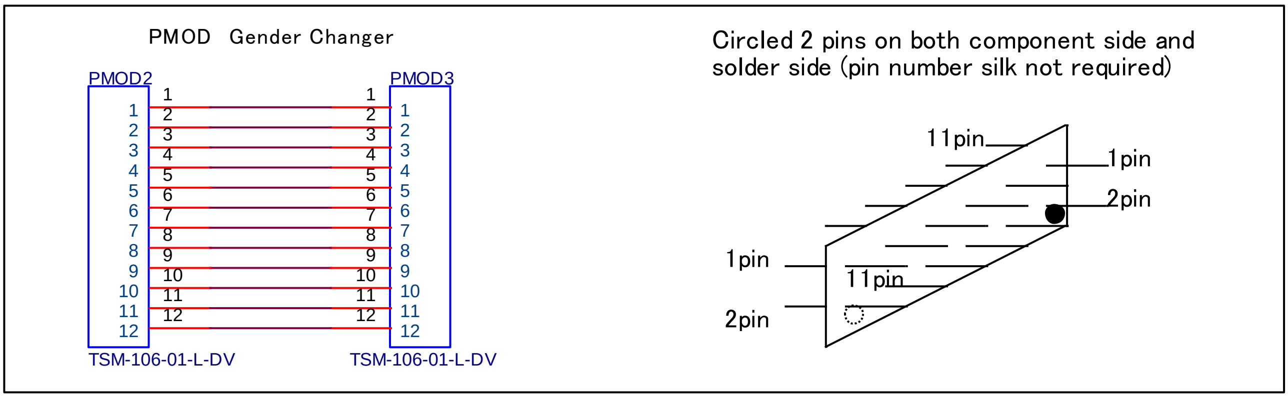


Figure 7-8 PMOD conversion board

7.2 Example of Bill of materials

Table 7-1 DC-PLC board (1/2)

Quantity	Reference	KIND	Parts Name	Manufacturer	Remark
1	CN1	CONNECTOR	FTSH-105-01-L-DV-K	SAMTEC	
2	CN2,CN3	CONNECTOR	XW4C-02E1-V1	OMRON	(2*) SPT2,5/2-V-5,0 (Phoenix Contact)
1	CN4	CONNECTOR	PJ-202A	CUI	
1	CN5	CONNECTOR	UX60SC-MB-5ST	HIROSE	
2	CN6,CN7	CONNECTOR	XG4H-1031	OMRON	
44	C1,C2,C4,C5,C7,C9,C10,C11,C13,C14,C15,C19,C22,C27,C29,C34,C35,C43,C44,C50,C58,C59,C60,C61,C62,C63,C64,C65,C66,C67,C69,C70,C71,C72,C73,C74,C75,C76,C77,C78,C79,C80,C81,C82	CERAMIC CAPACITOR	CC0603KRX7R9BB104	Yageo	(1*) 0.1uF/X7R/50V/1608
1	C3	CERAMIC CAPACITOR	C2012X6S0J226M085AC	TDK	(1*) 22uF/X6S/6.3V/2125
1	C6	CERAMIC CAPACITOR	C0603C331J3GACTU	KEMET	(1*) 330pF/C0G/10V/1608
2	C8,C68	CERAMIC CAPACITOR	TMK325B7226KMHP	Taiyo Yuden	(1*) 4.7uF/X7R/25V/2125
8	C12,C21,C23,C31,C32,C33,C36,C52	CERAMIC CAPACITOR	CGA3E1X7R1E105K080AC	TDK	(1*) 1uF/X7R/25V/1608
2	C16,C17	CERAMIC CAPACITOR	CGA3E2C0G1H472J	TDK	(1*) 4700pF/C0G/50V/1608
2	C18,C20	CERAMIC CAPACITOR	CGA3E2C0G1H120J080AA	TDK	(1*) 12pF/C0G/50V/1608
1	C24	ALUM CAP	EEHZC1E101XP	Panasonic	
2	C25,C30	CERAMIC CAPACITOR	CGA4J3X7R1E105M125AB	TDK	(1*) 1uF/X7R/25V/2125
3	C26,C28,C39	CERAMIC CAPACITOR	22201C105KAT2A	AVX	(1*) 1uF/X7R/100V/5750
2	C37,C38	CERAMIC CAPACITOR	C1608X7R1H223K	TDK	(1*) 0.022uF/X7R/50V/1608
3	C40,C42,C48	CERAMIC CAPACITOR	HMK325BJ475MN-TE	Taiyo Yuden	(1*) 4.7uF/X5R/100V/3225
1	C41	ALUM CAP	EEEFK1J101P	Panasonic	
5	C45,C46,C53,C54,C57	CERAMIC CAPACITOR	TMK325B7226KMHT	Taiyo Yuden	(1*) 22uF/X7R,X5R/25V/3225
1	C49	CERAMIC CAPACITOR	C1608C0G1H101J080AA	TDK	(1*) 100pF/C0G/50V/1608
1	C51	CERAMIC CAPACITOR	CGA3E2C0G1H470J080AA	TDK	(1*) 47pF/C0G/50V/1608
1	C55	CERAMIC CAPACITOR	GRM32DR71E106KA12L	MURATA	(1*) 10uF/X7R,X5R/25V/3225
1	C56	CERAMIC CAPACITOR	C0603C471J3GACAUTO	KEMET	(1*) 470pF/C0G/25V/1608
1	D1	DIODE	BAT54SFILM	STMicroelectronics	
4	D2,D3,D4,D5	DIODE	ES1B-13-F	Diodes Inc	
2	D6,D11	DIODE	BAT54SDW-7-F	Diodes Inc	(2*) BAT54SDWQ-7-F
2	D7,D8	DIODE	SMAJ5.0CA-TR	STMicroelectronics	Recommended by STMicroelectronics
1	D12	BRIDGE DIODE	HD01-T	Diodes Inc	
1	D13	DIODE	DFLS160	Diodes Inc	
1	D14	DIODE	RCLAMP0502BATCT	Semtech	
2	F1,F2	FILTER	NFE31PT222Z1E9	Murata	
12	JP1,JP2,JP3,JP4,JP5,JP6,JP7,JP9,JP10,JP11,JP12,JP14	CONNECTOR	FFC-3AMEP1	HONDA	(1*)
3	JP13,JP15,JP21	CONNECTOR	FFC-2AMEP1	HONDA	(1*)
2	LED1,LED4	LED	SML-E12M8W	Rohm	
2	LED2,LED3	LED	SML-E12V8W	Rohm	
1	L1	INDUCTOR	NRS3015T4R7MNGHV	Taiyo Yuden	(2*) VLS3015CX-4R7M(TDK)
2	L4,L5	INDUCTOR	SRR1208-272KL	Bourns Inc	
1	L6	INDUCTOR	SRN3015-330M	Bourns	(2*) VLS3015CX-330M (TDK)
2	L7,L9	INDUCTOR	SRN3015-100M	Bourns	(2*) VLS3015CX-100M (TDK)
1	L8	INDUCTOR	NRH3012T220MNV	Taiyo Yuden	(2*) LQH3NPN220MMEL (Murata)
1	PMOD1	CONNECTOR	PPPC062LJBN-RC	Sullins	
2	PMOD2,PMOD3	CONNECTOR	TSM-106-01-L-DV	SAMTEC	
3	R1,R2,R16	RESISTOR	RK73B1JTTD330J	KOA	(1*) 33ohm/5%/1608
2	R3,R10	RESISTOR	RK73B1JTTD472J	KOA	(1*) 4.7K/5%/1608
4	R4,R6,R11,R15	RESISTOR	RK73B1JTTD2R4J	KOA	(1*) 2.4ohm/5%/1608
1	R5	RESISTOR	RK73B1JTTD100J	KOA	(1*) 10ohm/5%/1608
4	R7,R23,R32,R45	RESISTOR	RK73H1JTTD1001F	KOA	(1*) 1K/1%/1608
1	R8	RESISTOR	RK73B1JTTD162J	KOA	(1*) 1.6K/5%/1608
1	R9	RESISTOR	RK73B1JTTD561J	KOA	(1*) 560ohm/5%/1608
2	R12,R14	RESISTOR	RK73H1JTTD8201F	KOA	(1*) 8.2K/1%/1608
1	R13	RESISTOR	RK73H1JTTD7501F	KOA	(1*) 7.5K/1%/1608
2	R17,R24	RESISTOR	RK73B1JTTD112J	KOA	(1*) 1.1K/5%/1608
2	R18,R25	RESISTOR	RK73B1JTTD161J	KOA	(1*) 160ohm/5%/1608
5	R19,R26,R30,R31,R42	RESISTOR	RK73H1JTTD2002F	KOA	(1*) 20K/1%/1608
9	R20,R28,R33,R47,R48,R49,R50,R51,R52	RESISTOR	RK73B1JTTD105J	KOA	(1*) 1M/5%/1608
8	R21,R44,R53,R54,R55,R57,R58,R62	RESISTOR	RK73B1JTTD513J	KOA	(1*) 51K/5%/1608
2	R22,R27	RESISTOR	RK73H1JTTD3901F	KOA	(1*) 3.9K/1%/1608
2	R41,R29	RESISTOR	RK73B1JTTD104J	KOA	(1*) 100K/5%/1608
2	R34,R56	RESISTOR	RK73B1JTTD103J	KOA	(1*) 10K/5%/1608
1	R35	RESISTOR	RK73H1JTTD9092F	KOA	(1*) 90.9K/1%/1608
2	R36,R37	RESISTOR	RK73B1JTTD510J	KOA	(1*) 51ohm/5%/1608
1	R38	RESISTOR	RK73H1JTTD8252F	KOA	(1*) 82.5K/1%/1608
1	R39	RESISTOR	RK73H1JTTD1153F	KOA	(1*) 115K/1%/1608
1	R40	RESISTOR	RK73H1JTTD8251F	KOA	(1*) 8.25K/1%/1608
2	R46,R60	RESISTOR	RK73B1JTTD101J	KOA	(1*) 100ohm/5%/1608
3	R59,R61,R71	RESISTOR	RK73B1JTTD512J	KOA	(1*) 5.1K/5%/1608
4	R63,R64,R66,R75,	RESISTOR	RK73Z1JTTD	KOA	(1*) 0ohm/1608
1	R74	RESISTOR	RK73B1JTTD220J	KOA	(1*) 22ohm/5%/1608
5	SW3,SW4,SW5,SW6,SW7	SWITCH	SSSS222700	ALPS	

(1*)Equivalent product can be changed
(2*)Alternative product

Table 7-2 DC-PLC board (2/2)

Quantity	Reference	KIND	Parts Name	Manufacturer	Remark
1	SW8	SWITCH	SKQMBBE010	ALPS	
2	SW9,SW10	SWITCH	SSSS213000	ALPS	
2	TP1,TP5	TEST PIN	HK-5-G-Black	MAC8	
3	TP2,TP3,TP4	TEST PIN	HK-5-G-Red	MAC8	
2	TR1,TR4	TRANSISTOR	MMBT3904L RFG	Taiwan Semiconductor	
4	TR2,TR3,TR5,TR6	TRANSISTOR	BSS84,215	Nexperia	
1	TR7	TRANSISTOR	RK7002BMT116	Rohm	
1	U1	IC	AT25SF081B-SSHB	Adesto	(2*) W25Q80DVSNIG(Winbond)
1	U2	IC	R9A06G061GNP	Renesas	
1	U3	IC	ISL15102IRZ	INTERSIL	
4	U6,U7,U8,U9	IC	SN74LVC2T45DCUR	TI	
3	U10,U12,U13	IC	SN74LVC1T45DCK	TI	
1	U11	IC	FT232RL	FTDI	
2	U14,U16	IC	SN74LVC2G07DCKR	TI	
1	U15	IC	BD5228G-TR	Rohm	(2*) BD5228G-2MTR(Rohm)
1	Y1	CRYSTAL	DSX221SH	Daishinku	Specify the specifications (16MHz,CL:8pF, Frequency tolerance:±10ppm, Frequency characteristics over temperature:±15ppm) (2*)(3*)NX2520SA-16M-CHP-CSW-19(NDK) (4*)

(2*)Alternative product
(3*) For NX2520SA-16M-CHP-CSW-19, it is necessary to change the constants of the external circuit (R9=2.2kΩ, C20=12pF, C18=15pF).
(4*) CX2520DB16000D0FLJCC (Kyocera) has been discontinued.

7.3 RX651 MCU board

Table 7-3 RX651 MCU board

Quantity	Reference	KIND	Parts Name	Manufacturer	Remark
1	CN301	CONNECTOR	PPPC062LFBN-RC	SULLINS	
1	CN302	CONNECTOR	UX60SC-MB-5ST(82)	HIROSE	
2	CN303,CN304	CONNECTOR	XG4C-1031	OMRON	
1	CN305	CONNECTOR	XG4C-1431	OMRON	
1	C301	CERAMIC CAPACITOR	GCM188R71H224KA64	MURATA	(1*) 0.22uF/X7R/50V/1608
2	C302,C303	CERAMIC CAPACITOR	C0603C300J5GACTU	KEMET	(1*) 30pF/C0G/50V/1608
2	C304,C305	CERAMIC CAPACITOR	CGA3E1X7R1E105K080AC	TDK	(1*) 1uF/X7R/25V/1608
9	C306,C307,C308,C309,C310,C311,C312,C313,C314	CERAMIC CAPACITOR	CC0603KRX7R9BB104	Yageo	(1*) 0.1uF/X7R/50V/1608
1	D301	DIODE	RCLAMP0502BATCT	Semtech	
1	F301	FILTER	NFE31PT222Z1E9	Murata	
1	JP301	CONNECTOR	FFC-2AMEP1	HONDA	(1*)
1	LED301	LED	SML-E12M8W	Rohm	
1	LED302	LED	SML-E12V8W	Rohm	
1	R301	RESISTOR	RK73B1JTTD162J	KOA	(1*) 1.6K/5%/1608
3	R302,R305,R310	RESISTOR	RK73Z1JTTD	KOA	(1*) 0ohm/1608
1	R303	RESISTOR	RK73H1JTTD1001F	KOA	(1*) 1K/1%/1608
1	R304	RESISTOR	RK73B1JTTD513J	KOA	(1*) 51K/5%/1608
9	R306,R315,R316,R317,R318,R319,R320,R321,R322	RESISTOR	RK73B1JTTD512J	KOA	(1*) 5.1K/5%/1608
1	R308	RESISTOR	RK73B1JTTD101J	KOA	(1*) 100ohm/5%/1608
2	R309,R314	RESISTOR	RK73B1JTTD103J	KOA	(1*) 10K/5%/1608
1	R311	RESISTOR	RK73H1JTTD2002F	KOA	(1*) 20K/1%/1608
2	R312,R313	RESISTOR	RK73B1JTTD270J	KOA	(1*) 27ohm/5%/1608
2	SW301,SW302	SWITCH	CHS-04TA	COPAL	
1	U301	IC	R5F5651EHDFP#30	Renesas	
1	Y301	CRYSTAL	ABM3C-24.000MHZ-D4Y	Abracon	

(1*)Equivalent product can be changed

7.4 Power Filter board

Table 7-4 Power Filter board

Quantity	Reference	KIND	Parts Name	Manufacturer	Remark
2	CN201,CN202	CONNECTOR	XW4C-02E1-V1	OMRON	(2*) SPT2,5/2-V-5,0 (Phoenix Contact)
2	C201,C202	CERAMIC CAPACITOR	22201C106MAT2A	AVX	(1*) 10uF/X7R,X5R/100V/5750
2	JP201,JP202	CONNECTOR	FFC-2AMEP1	HONDA	(1*)
2	L201,L202	INDUCTOR	AIRD-03-102K	Abracon	
1	TP201	TEST PIN	ST-2-2	MAC8	

(1*)Equivalent product can be changed
(2*)Alternative product

7.5 PMOD conversion board

Table 7-5 PMOD conversion board

Quantity	Reference	KIND	Parts Name	Manufacturer	Remark
2	PMOD2,PMOD3	CONNECTOR	TSM-106-01-L-DV	SAMTEC	

8. PCB Layout Design Example

This chapter uses the CPX4 DC-PLC evaluation kit RTK0EE0009D01001BJ as an example to show PCB layout example of DC-PLC board equipped with PLC modem LSI (CPX4), Power amplifier (ISL15102), and Power supply IC.

Figure 8-1 shows the CPX4 DC-PLC board configuration, Figure 8-2 shows an example of component placement, and Figure 8-3 to Figure 8-6 show examples of the layout of each layer. Please note that this PCB layout example may not be optimal depending on the PCB shape.

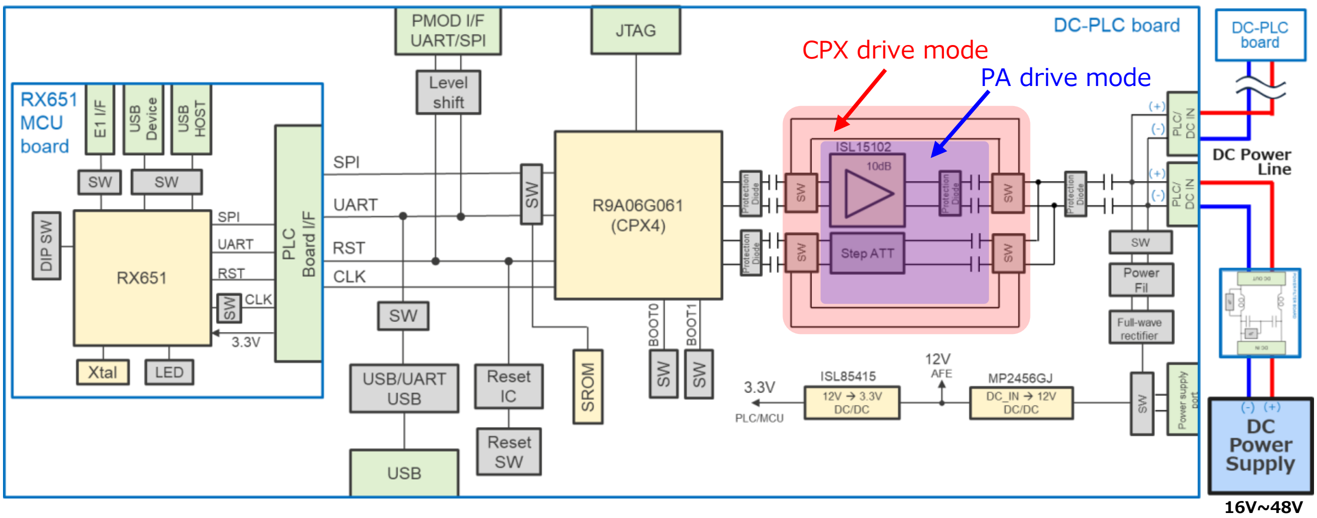


Figure 8-1 CPX4 DC-PLC board configuration

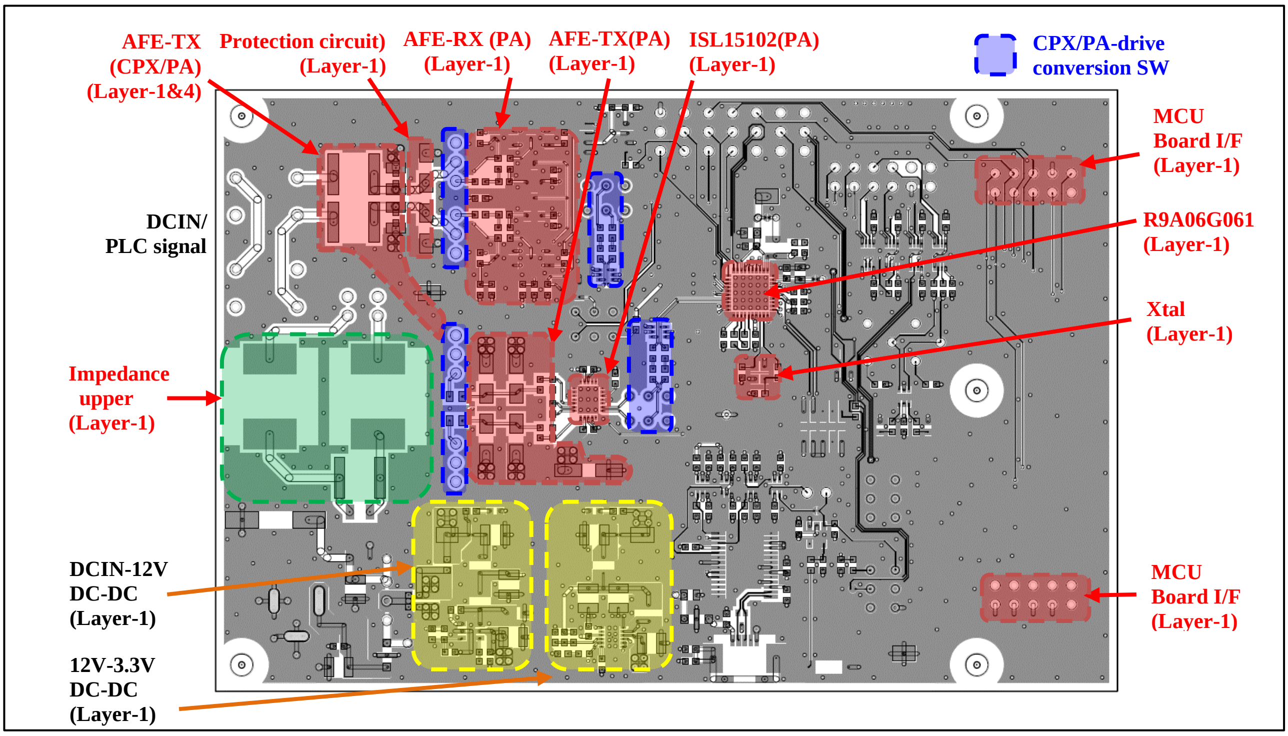


Figure 8-2 Example of parts arrangement of DC-PLC board

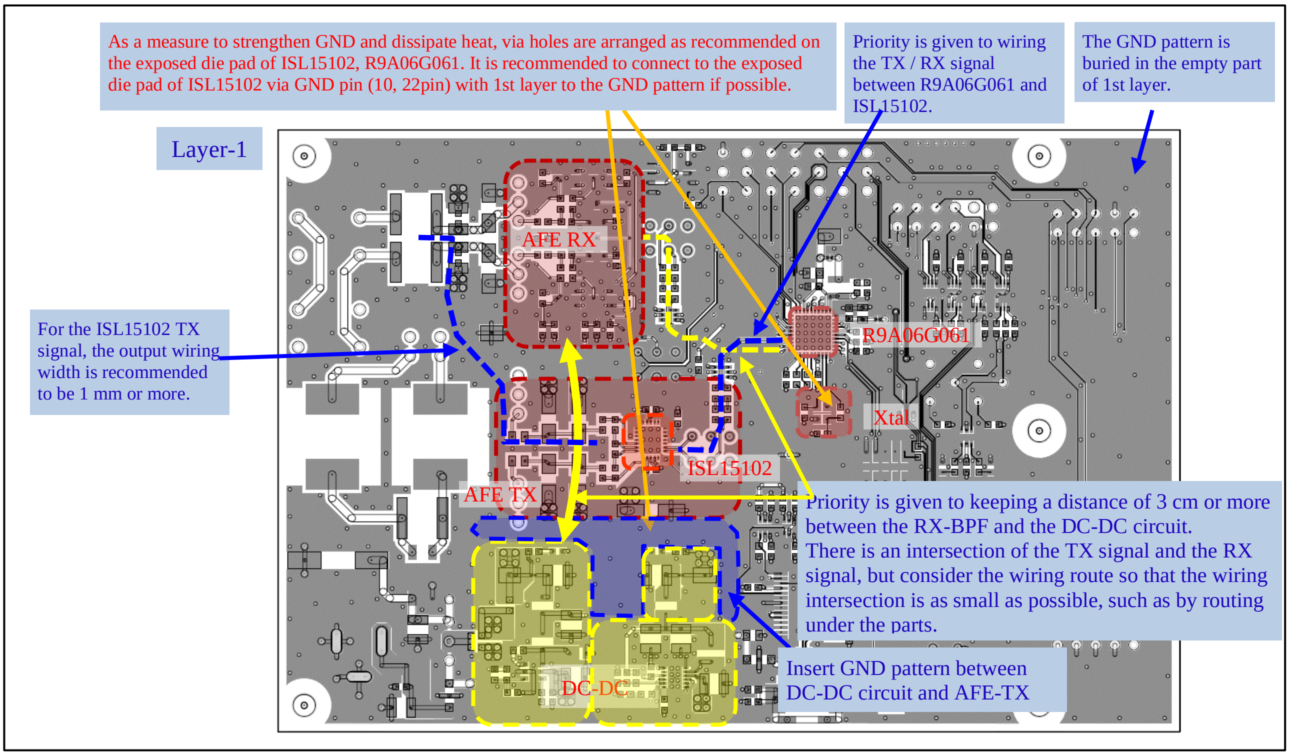


Figure 8-3 Layout example of the 1st layer of the DC-PLC board

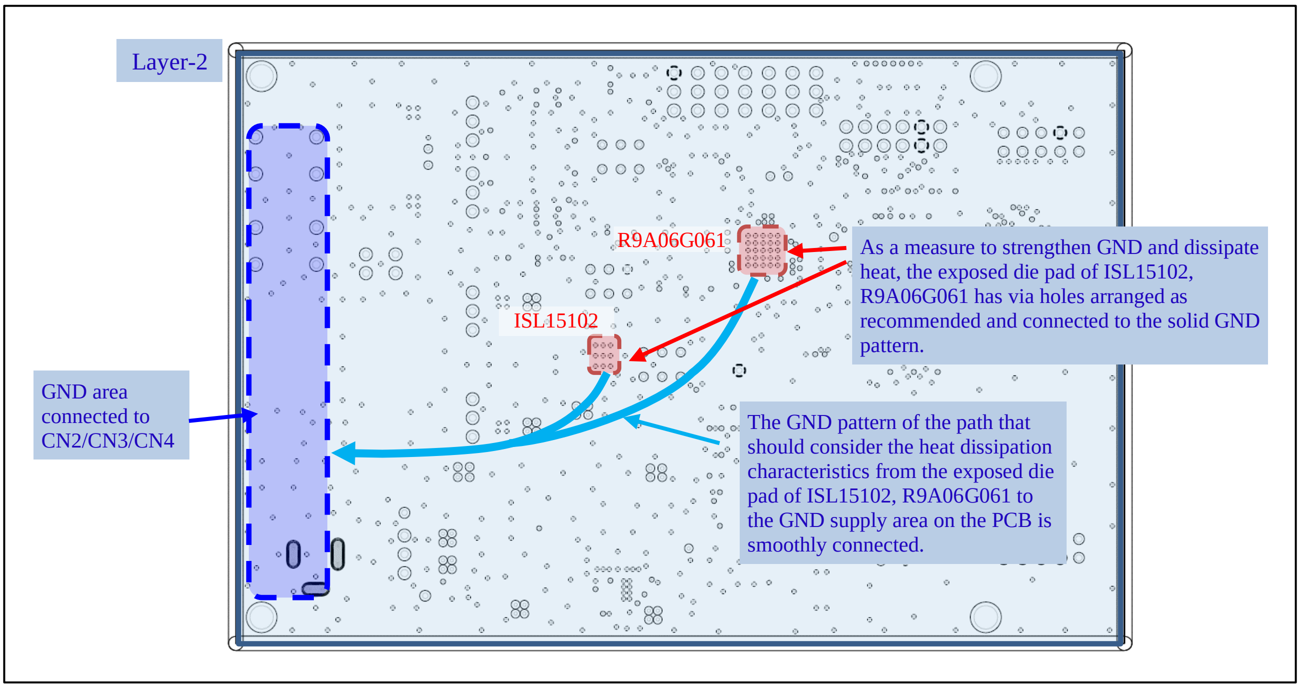


Figure 8-4 Layout example of the 2nd layer of the DC-PLC board

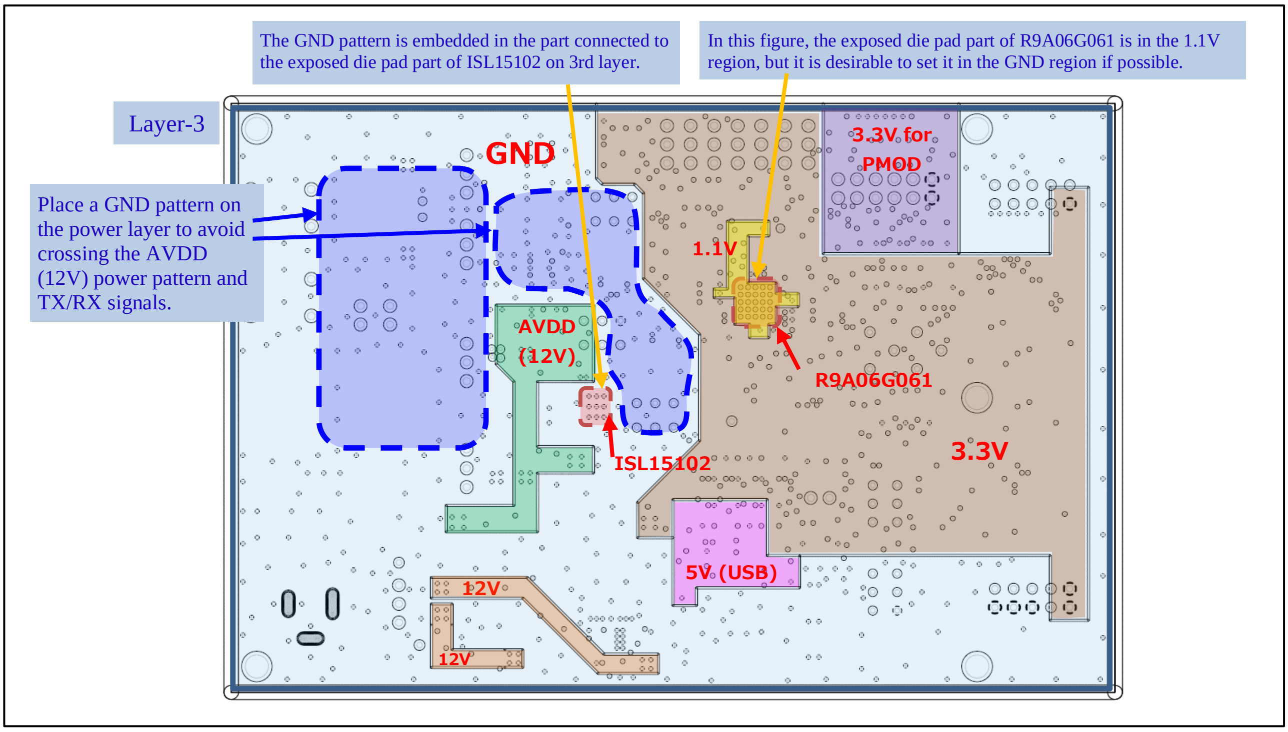


Figure 8-5 Layout example of the 3rd layer of the DC-PLC board

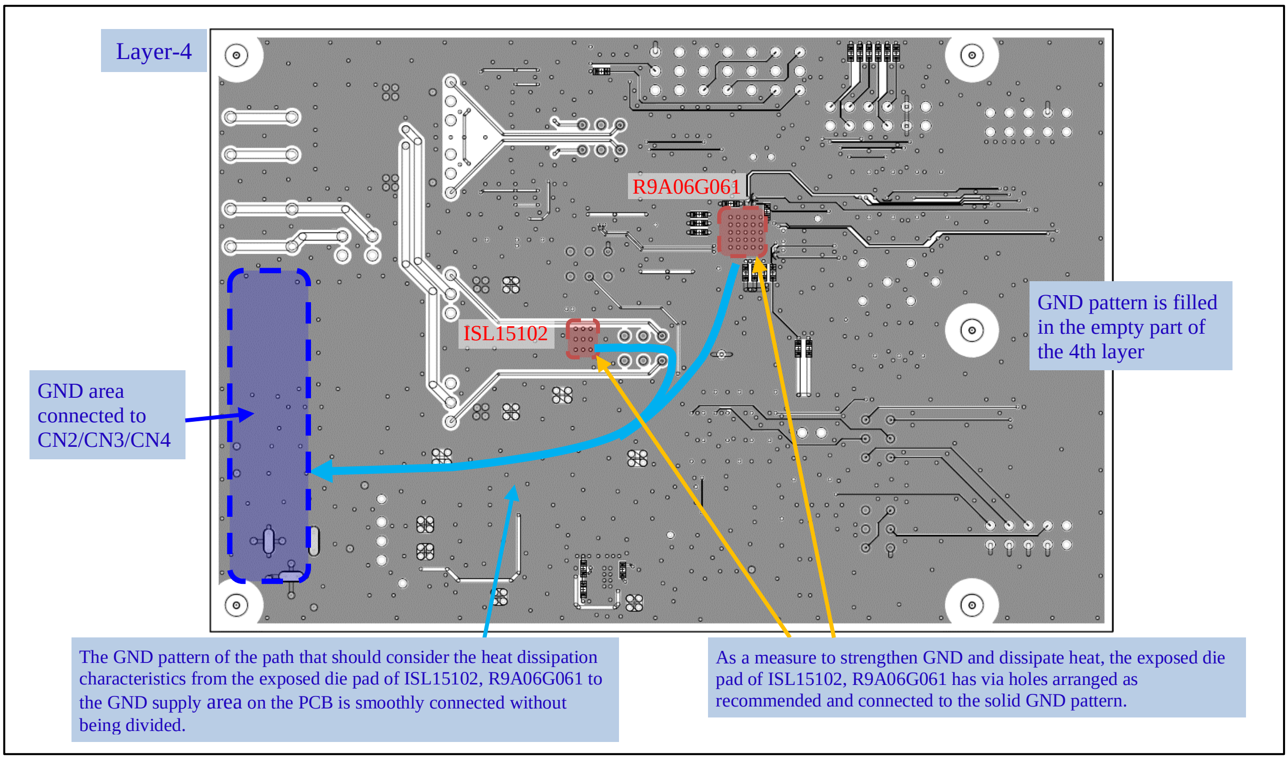


Figure 8-6 Layout example of the 4th layer of the DC-PLC board

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	2024.05.01		First Edition issued
1.10	July 01, 2024	30,31	Corrected errors in Table 7-1 and Table 7-3
1.20	March 01, 2025	7	Changed the recommended value of the external capacitance C2 and C3 of the DC-DC converter

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