RC32508A

This document describes the register organization and byte addresses of the RC32508A. Detailed register definitions can be located by following the links in the document.

Contents

1. Serial Interfaces

The RC32508A can be configured in two ways:

- From internal non-volatile memory using OTP user configurations
- From its slave serial interface and programmed by master device

The RC32508A supports two slave serial interfaces: I2C and SPI. The slave interface selection is determined by the ssi_enable (0x0026[1:0]) register field, which defaults to I2C mode. If OTP is not programmed, the device powers up in I2C 1-byte offset mode. These serial interfaces share the same pins so only one is available at a time.

An external master (I2C, SPI) can be used to access internal registers after the power-up and configuration load process is completed. Additionally, all of the device logic pins are sampled at the rising edge of the internal master reset signal and some of them may be used in setting the initial configuration.

1.1 1-Byte and 2-Byte Offset Mode

The RC32508A supports 1-byte and 2-byte offset mode for the slave serial interfaces, I2C and SPI. The user can choose to operate as 1-byte or 2-byte offset mode, and can be configured through register ssi_addr_size (0x0026[2]) register field which defaults as 1-byte offset mode. These offsets are used in conjunction with the page register to access registers internal to the device. Because the I2C protocol already includes a read/write bit with the Dev Addr, all bits of the 1-byte or 2-byte offset field can be used to address internal registers.

- The 1-byte offset mode – It also called page mode where part of the address offset is provided in each transaction and another part comes from an internal page register in each serial port. For an I2C 1-byte offset mode operation example, see Figure 1.
- The 2-Byte offset mode – Use two byte as the serial port providing the full offset address within each burst. For an I2C 2-byte offset mode operation example, see Figure 2.

1.2 I2C Slave

The I2C slave protocol complies with the *I2C Specification*, version UM10204 Rev.6, 4 April 2014. The SCL_SCLK and SDA_nCS pins are not 3.3V tolerant. The Dev Addr shown in the Figure 1 represents the I2C bus address that the device will respond to. This 7-bit value in the i2c_addr register field defaults to 0x09 if not programmed via the OTP load.

1.2.1 1-Byte Offset Mode

In 1-byte mode, the lower 8 bits of the register offset address originate from the Offset Addr byte and the upper 8 bits come from the page register. The page register can be accessed at any time using an offset byte value of 0xFD. Write to 0 for page0, 1 for page1, 2 for page2, and 3 for page3.

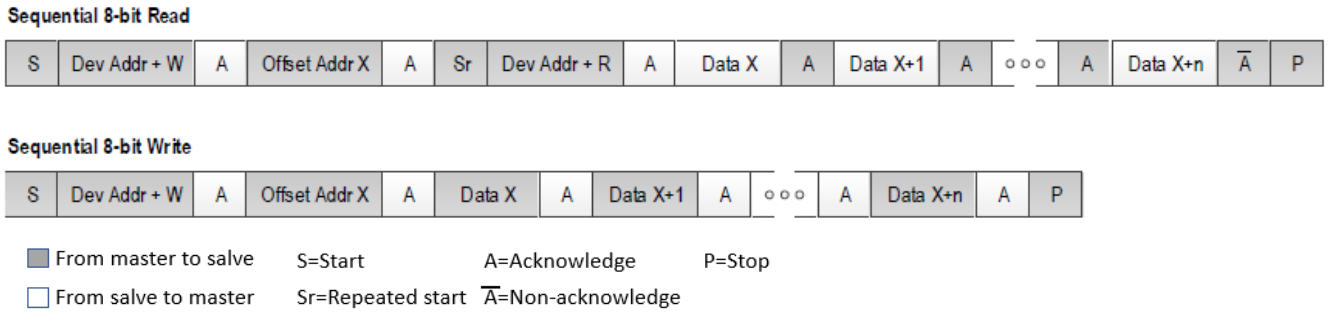


Figure 1. I2C 1-Byte Offset Mode Slave Sequencing

1.2.2 2-Byte Offset Mode

In 2-byte mode, the full 16-bit register address can be obtained from the Offset Addr bytes, so the page register does not need to be set up. The MSB offset address is the page number and the LSB address is the register address.

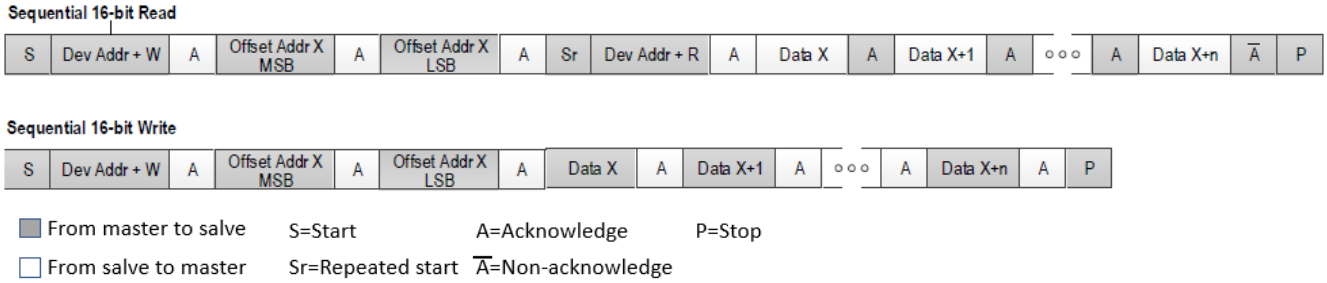


Figure 2. I2C 2-Byte Offset Mode Slave Sequencing

Note: All serial port configurations will take effect after the write cycle is completed.

1.3 SPI Slave

This device supports 3-wire SPI operation as a selectable protocol on the serial port. In 3-wire mode, the SDIO signal is used as a single, bidirectional data signal.

Figure 3 shows the sequencing of address and data on the serial port in 3-wire SPI mode. The R/W bit is high for read cycles and low for write cycles.

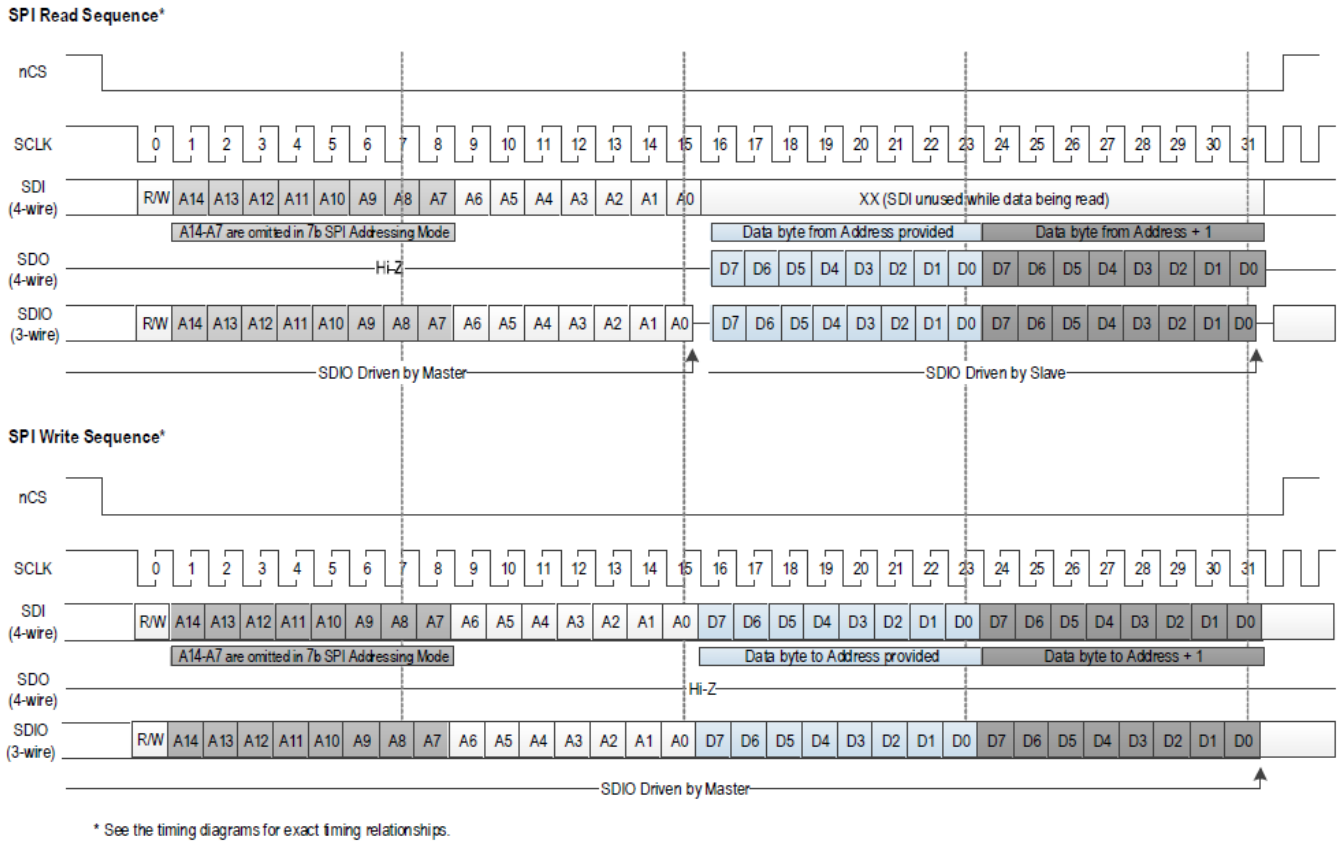


Figure 3. SPI Sequencing Diagram

SPI operation can be configured for the following settings through register fields: 1-byte or 2-byte offset addressing (ssi_addr_size).

In 1-byte operation, the 16-bit register address is formed by using the 7 bits of address supplied in the SPI access and taking the upper 9 bits from the page register. The page register is accessed using an Offset Address of 0xFD.

In 2-byte operation, the 16-bit register address is formed by using the 15 bits of address supplied in the SPI access and taking the upper 1-bit from the page register.

- Data sampling on falling or rising edge of SCLK (spi_clk_sel)
- Output (read) data positioning relative to active SCLK edge (spi_del_out)

Note: SPI burst mode operation is required to ensure data integrity of multi-byte registers. When accessing a multi-byte register, all data bytes must be written or read in a single SPI burst access. Bursts can be of greater length if desired but must not extend beyond the end of the register page. An internal address pointer is incremented automatically as each data byte is written or read.

The SPI interface operating at 10MHz supports a DCO update rate of approximately 200k updates per second.

2. Example of Programming Process

The RC32508A is comprised of a PLL0 and a PLL1. PLL0 has I^2C address of 0x9 and PLL1 has I^2C address of 0xD. By default, addressing mode is 1-byte mode for both devices. If addressing mode is unknown, perform the following steps to determine addressing mode.

Check I^2C 1-byte mode:

1. Program page register (address offset 0xFC) with value of 0x00000000.
2. Read 2 bytes from VENDOR_ID register (address offset 0x00).
   - If the value returned is 0x1033, then the device is in 1-byte mode.

Check I^2C 2-byte mode:

1. Program page register (address offset 0xFFFD) with value of 0x00000000.
2. Read 2 bytes from VENDOR_ID register (address offset 0x0000).
   - If the value returned is 0x1033, then the device is in 2-byte mode.

Addressing mode is controlled by ssi_addr_size register bit found in each PLL. The ssi_addr_size register bit must be programmed to the same value for both PLLs.

All RC32508A registers occupy address space from 0x000 to 0x1DF. In 1-byte mode, address offset from 0x00 to 0xFF have page register set to 0x00000000. The format for writing the page register is as follows:

Page 0

Write 0x9, 0xFC 0x00 0x00 0x00 0x00

RC32508A registers with address offset 0x100 to 0x1FF have page register set to 0x00000100. The format for writing the page register is as follows:

Page 1

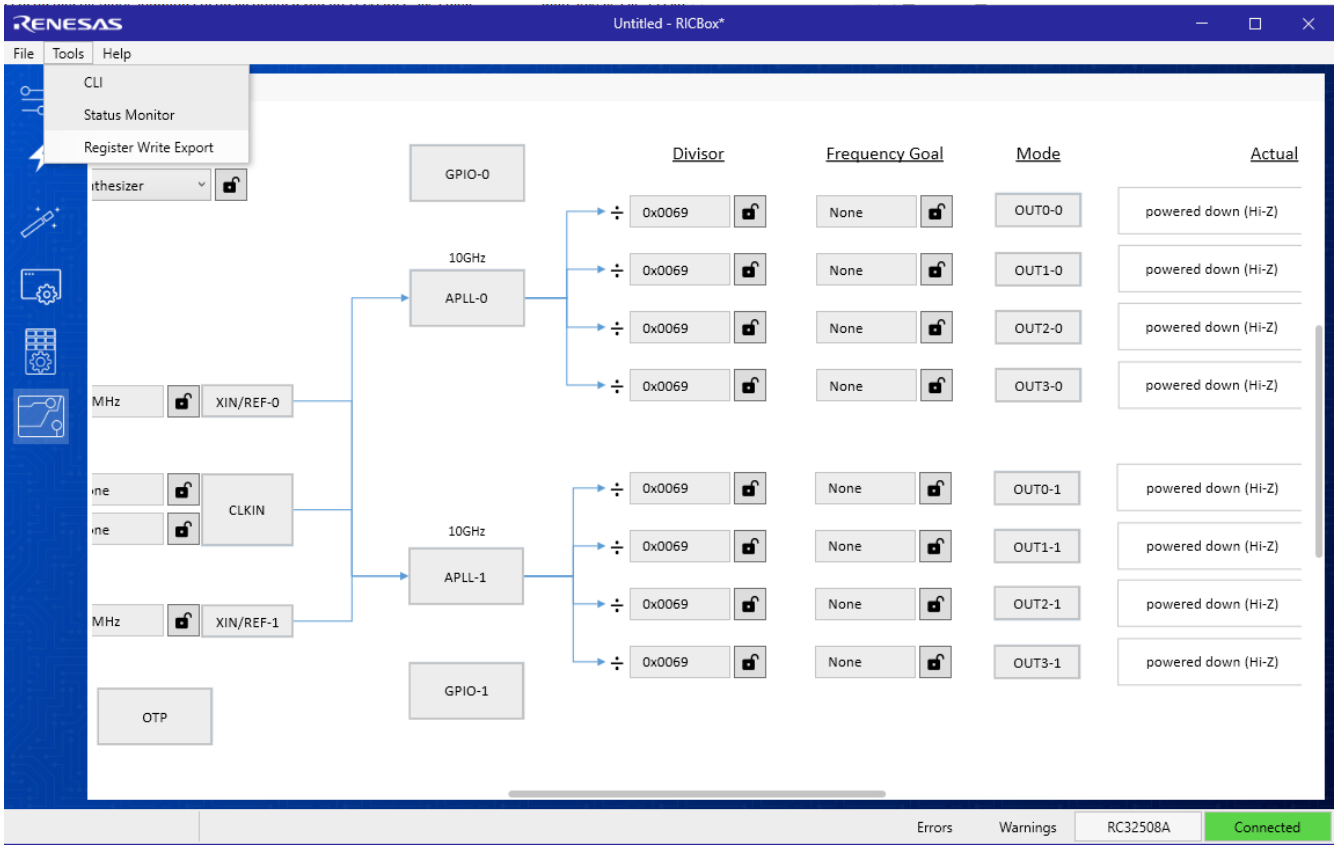
Write 0x9, 0xFC 0x00 0x01 0x00 0x00

In 2-byte mode, address offset from 0x0000 to 0xFFFF have page register set to 0x00000000. This also applies to SPI.

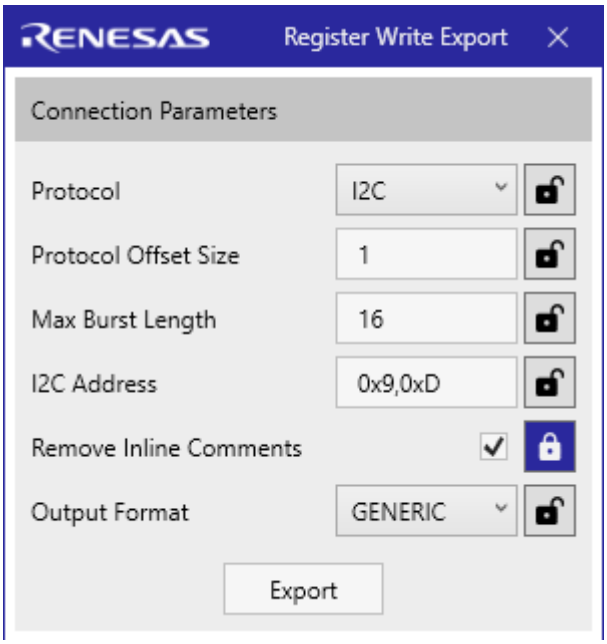
Complete the following steps to program the RC32508A:

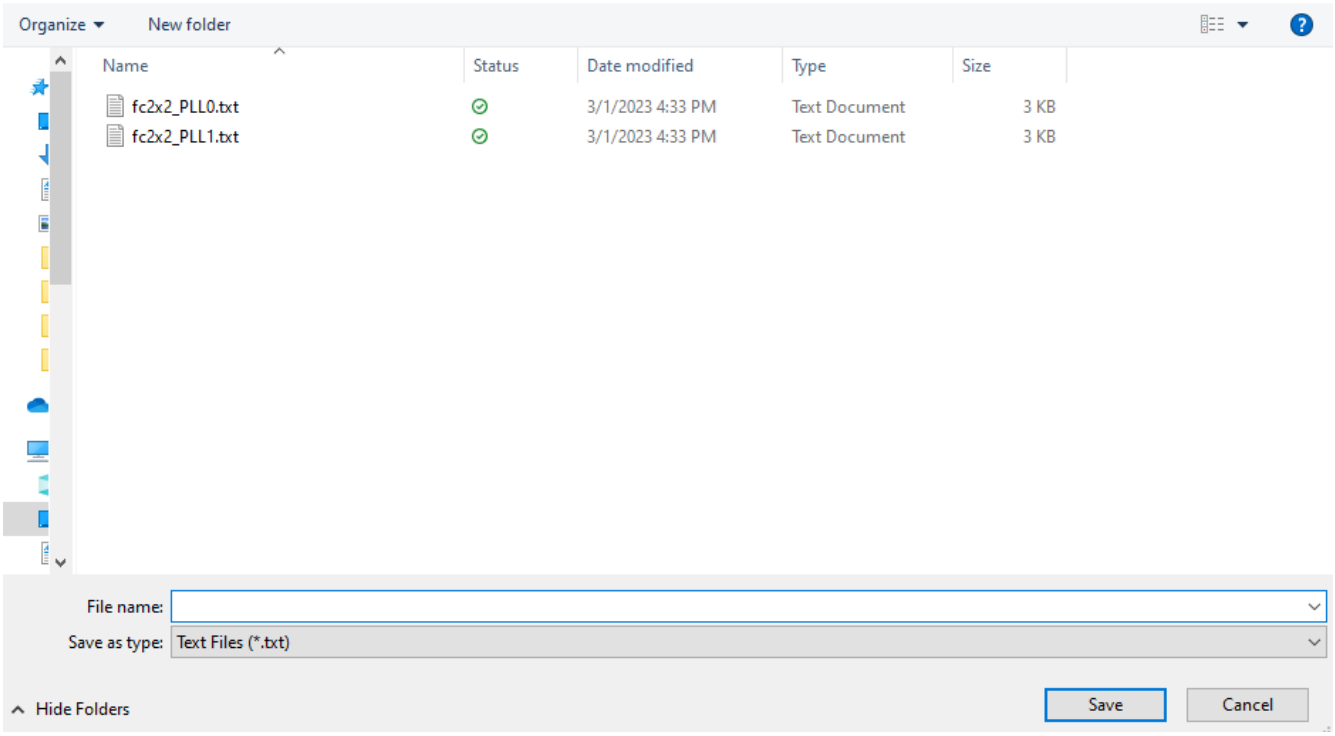
1. Program all PLL0 register values.
   a. Skip I2C_ADDR_CNFG and SSI_GLOBAL_CNFG
2. Perform a PLL0 VCO calibration.
   Note: This step applies only if the VCO frequency will change.
   a. PLL0. TOP.APLL.VCO_CAL_CNFG.vco_recal = 0 → 1 → 0
3. Perform a PLL0 divider sync up.
   a. PLL0.TOP.GLOBAL.DEV_RESET.divider_sync = 0 → 1 → 0
4. Program new PLL0 I2C_ADDR_CNFG and SSI_GLOBAL_CNFG values.
   a. This step is optional. If there is no change, then skip the step.
5. Repeat steps 1-4 for PLL1 register values.
6. If PLL0 and PLL1 VCO frequencies are the same then perform the following:
   a. Disable PLL1: vco_dis = 1
   b. Perform VCO recal on PLL0
   c. Perform Div Sycn on PLL0
   d. Read PLL0 vco_cap and vco_trim_val and save for later
   e. Disable PLL0: vco_dis = 1
   f. Enable PLL1: vco_dis = 0
   g. Perform VCO recal on PLL1
   h. Perform Div Sycn on PLL1
   i. Read PLL1 vco_cap and vco_trim_val and save for later
   j. Write PLL1 vco_cal_byp = 1
   k. Write PLL1 vco_sw_cap = saved value from read
   l. Write PLL1 vco_trim_wr_en = 1
   m. Write PLL1 vco_trim = saved value from read
   n. Enable PLL0: vco_dis = 0
   o. Write PLL0 vco_cal_byp = 1
   p. Write PLL0 vco_sw_cap = saved value from read
   q. Write PLL0 vco_trim_wr_en = 1
   r. Write PLL0 vco_trim = saved value read

7. Using the RICBox GUI for RC32508A, the register stream can be exported. Click Tools > Register Write Export.



8. Choose the protocol.
   - I2C
9. Choose the addressing mode.
   - 1 byte mode
10. Choose the maximum number of bytes to write.
    - 16 bytes
11. Choose the I2C addresses.
    - 0x9, 0xD
12. Remove inline comments.
    - Check to remove the extra comments for better readability.
13. Choose the output format.
    - GENERIC (txt) or Aardvark (xml)
14. Click on Export when ready to save.
    - A save dialog box will open (see screen on the following page).
    - Pick a location to save the two files. _PLL0/1 will automatically be added.




Organize
New folder
Name
Status
Date modified
Type
Size
fc2x2_PLL0.txt
3/1/2023 4:33 PM
Text Document
3 KB
fc2x2_PLL1.txt
3/1/2023 4:33 PM
Text Document
3 KB
File name:
Save as type:
Text Files (*.txt)
Hide Folders
Save
Cancel

3. Registers

It is highly recommended to use Renesas' RICbox GUI for creating a configuration file for RC32508A.

3.1 Register Block Offsets

Table 1. Register Block Offset

Block Offsets	Block Name	Register Block Address Table Links	Register Block Description
0x00	GLOBAL	Global Block Register Offsets	GLOBAL Registers
0x20	INT	Interrupt Block Register Offsets	INT Registers
0x30	LOSMON[0]	LOS Monitor Block Register Offsets	LOSMON Registers
0x40	LOSMON[1]	LOS Monitor Block Register Offsets	LOSMON Registers [1]
0x50	LOSMON[2]	LOS Monitor Block Register Offsets	LOSMON Registers [1]
0x60	ACTMON[0]	ACT Monitor Block Register Offsets	ACTMON Registers
0x80	ACTMON[1]	ACT Monitor Block Register Offsets	ACTMON Registers [1]
0xA0	DPLL	DPLL Block Register Offsets	DPLL Registers
0xE0	TDC	TDC Block Register Offsets	TDC Registers
0xF0	SYSDIV	System Clock Divider Block Register Offsets	SYSDIV Registers
0xF4	BIAS	Bias Block Register Offsets	BIAS Registers
0xF8	XO	Crystal Block Register Offsets	XO Registers
0x100	OUT[0]	Clock Output Block Register Offsets	OUT Registers
0x108	OUT[1]	Clock Output Block Register Offsets	OUT Registers [1]
0x110	OUT[2]	Clock Output Block Register Offsets	OUT Registers [1]
0x118	OUT[3]	Clock Output Block Register Offsets	OUT Registers [1]
0x120	REF[0]	Clock Reference Addresses	REF Registers
0x124	REF[1]	Clock Reference Addresses	REF Registers [1]
0x130	GPIO	GPIO Block Register Offsets	GPIO Registers
0x140	SSI	SSI Block Register Offsets	SSI Registers
0x150	APLL	APLL Block Register Offsets	APLL Registers
0x190	INP	Clock Input Block Register Offsets	INP Registers
0x1D0	Rsvd	Reserved	-

1. Register block functionality is the same, so the description is not duplicated.

3.2 Register Block Address Maps

3.2.1 Global Register Block Address Map

The Global Register block has a base address of 0x00. The addresses shown in Table 2 are offsets starting from this base address.

Table 2. Global Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	VENDOR_ID Register	Device vendor identification code. Address map for this block of registers: Global Block Register Offsets.
0x02	hword	DEVICE_ID Register	Device-specific identification code. Address map for this block of registers: Global Block Register Offsets.
0x04	hword	DEVICE_REV Register	Device revision identification information. Address map for this block of registers: Global Block Register Offsets.
0x06	hword	DEVICE_PGM Register	Identifies any factory OTP pre-programmed configuration. Address map for this block of registers: Global Block Register Offsets.
0x08	byte	DEVICE_CNFG Register	Device overall configuration settings. Address map for this block of registers: Global Block Register Offsets.
0x0A	byte	DEV_RESET Register	Device reset commands. Address map for this block of registers: Global Block Register Offsets.
0x0C	hword	SW_RESET Register	Software reset command. Address map for this block of registers: Global Block Register Offsets.
0x0E	hword	CLOCK_GATE Register	Clock gating control. Setting of any of the bits in this register stops the internal clocks to the indicated logic block(s). The Renesas Electronics Timing Commander Software automatically determines which logic can be disabled for a specific configuration. Contact Renesas Electronics if further details are needed.
0x10	byte	DEVICE_STS Register	Device status. Address map for this block of registers: Global Block Register Offsets.

3.2.2 Interrupt Register Block Address Map

The Interrupt block has a base address of 0x20. The addresses shown below are offsets starting from this base address.

Table 3. Interrupt Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	INT_EN Register	Interrupt Enable control. Address map for this block of registers: Interrupt Block Register Offsets.
0x02	hword	INT_STS Register	Interrupt Status. Address map for this block of registers: Interrupt Block Register Offsets.

3.2.3 Loss of Signal Monitor Register Block Address Map

The LOS Monitor 0 block has a base address of 0x30. The LOS Monitor 1 block has a base address of 0x40. The LOS Monitor 2 block has a base address of 0x50. The addresses shown below are offsets starting from this base address. Note that before reprogramming a Loss of Signal Monitor block, the corresponding losmon0_sw_rst, losmon1_sw_rst, or losmon2_sw_rst bit should be set. When programming is done, it should then be cleared.

Table 4. LOS Monitor Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	LOSMON_STS Register	LOS Monitor Status. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x01	byte	LOSMON_EVENT Register	LOS Monitor Event Status. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x02	byte	LOSMON_QUAL Register	LOS Monitor Qualify Counter Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x04	hword	LOSMON_WINDOW Register	LOS Monitor Window Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x08	word	LOSMON_THRESH Register	LOS Monitor Threshold Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.
0x0C	word	LOSMON_NOMINAL Register	LOS Monitor Nominal Number Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

3.2.4 Activity Monitor Register Block Address Map

The ACT Monitor 0 block has a base address of 0x60. The LOS Monitor 1 block has a base address of 0x80. The addresses shown below are offsets starting from this base address. Note that before reprogramming an Activity Monitor, the corresponding actmon0_sw_rst or actmon1_sw_rst bit should be set. Once programming is done, it should then be cleared.

Table 5. ACT Monitor Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	ACTMON_STS Register	Activity Monitor Status. Address map for this block of registers: ACT Monitor Block Register Offsets.
0x01	byte	ACTMON_EVENT Register	Activity Monitor Event Status. Address map for this block of registers: ACT Monitor Block Register Offsets.
0x04	word	ACTMON_WINDOW Register	Activity Monitor Window Configuration. Address map for this block of registers: ACT Monitor Block Register Offsets.
0x08	dword	ACTMON_THRESH Register	Activity Monitor Threshold Configuration. Address map for this block of registers: ACT Monitor Block Register Offsets.
0x10	word	ACTMON_NOMINAL Register	Activity Monitor Nominal Number Configuration. Address map for this block of registers: ACT Monitor Block Register Offsets.

3.2.5 DPLL Register Block Address Map

The Digital PLL block has a base address of 0xA0. The addresses shown below are offsets starting from this base address.

Table 6. DPLL Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	DPLL_REF_FB_CNFG Register	DPLL Ref and Fb Clock Configuration. Address map for this block of registers: DPLL Block Register Offsets.
0x01	byte	DPLL_MODE Register	Digital PLL mode control. Address map for this block of registers: DPLL Block Register Offsets.
0x02	byte	DPLL_DECIMATOR Register	Decimator configuration control. Address map for this block of registers: DPLL Block Register Offsets.
0x03	byte	DPLL_TRIM_OFFSET Register	DPLL Crystal trim offset. Address map for this block of registers: DPLL Block Register Offsets.
0x04	hword	DPLL_HOLDOVER_CNFG Register	Holdover Configuration. Address map for this block of registers: DPLL Block Register Offsets.
0x06	hword	DPLL_BANDWIDTH Register	DPLL Bandwidth configuration. Address map for this block of registers: DPLL Block Register Offsets.
0x08	hword	DPLL_DAMPING Register	DPLL Damping control. Address map for this block of registers: DPLL Block Register Offsets
0x0C	word	DPLL_PHASE_SLOPE_LIMIT Register	DPLL Phase Slope Limit control. Address map for this block of registers: DPLL Block Register Offsets
0x10	dword	DPLL_FB_DIV_NUM Register	DPLL Feedback Fraction Numerator value. Address map for this block of registers: DPLL Block Register Offsets.
0x18	dword	DPLL_FB_DIV_DEN Register	DPLL Feedback Fraction Denominator value. Address map for this block of registers: DPLL Block Register Offsets.
0x20	hword	DPLL_FB_DIV_INT Register	DPLL Feedback Integer value. Address map for this block of registers: DPLL Block Register Offsets.
0x22	hword	DPLL_FB_CORR Register	DPLL Feedback Correction Configuration. Address map for this block of registers: DPLL Block Register Offsets.
0x24	word	DPLL_PHASE_OFFSET Register	DPLL Phase Offset configuration. Address map for this block of registers: DPLL Block Register Offsets.
0x28	word	DPLL_WRITE_FREQ Register	DPLL Write Frequency command. Address map for this block of registers: DPLL Block Register Offsets.
0x2C	word	DPLL_LOCK Register	DPLL Lock Detection control. Address map for this block of registers: DPLL Block Register Offsets.
0x30	byte	DPLL_TDC_DELAY Register	DPLL TDC Delay Control. Address map for this block of registers: DPLL Block Register Offsets.
0x31	byte	DPLL_STS Register	DPLL Status. Address map for this block of registers: DPLL Block Register Offsets.
0x32	byte	DPLL_EVENT Register	DPLL Event status. Address map for this block of registers: DPLL Block Register Offsets.
0x33	byte	DPLL_LOL_CNT Register	DPLL Loss-of-Lock Event Counter. Address map for this block of registers: DPLL Block Register Offsets.
0x34	word	Reserved	Reserved
0x38	word	Reserved	Reserved
0x3C	byte	Reserved	Reserved

3.2.6 TDC Register Block Address Map

The TDC block has a base address of 0xE0. The addresses shown below are offsets starting from this base address.

Table 7. TDC Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	Reserved	Reserved
0x02	byte	TDC_REF_DIV_CNFG Register	TDC reference divider control. Address map for this block of registers: TDC Block Register Offsets.
0x03	byte	TDC_FB_SDM_CNFG Register	TDC internal APLL Feedback Divider SDM control. Address map for this block of registers: TDC Block Register Offsets.
0x04	byte	TDC_FB_DIV_INT Register	TDC internal APLL Feedback Divider Integer value. Address map for this block of registers: TDC Block Register Offsets.
0x06	hword	TDC_FB_DIV_FRAC Register	TDC internal APLL Feedback Divider Fraction value. Address map for this block of registers: TDC Block Register Offsets.
0x0A	byte	TDC_DAC_CNFG Register	TDC internal APLL Digital to Analog Converter (DAC) control. Address map for this block of registers: TDC Block Register Offsets.

3.2.7 System Clock Divider Register Block Address Map

The System Clock Divider block has a base address of 0xF0. The addresses shown below are offsets starting from this base address.

Table 8. System Clock Divider Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	SYS_DIV_INT Register	System Clock Divider Integer value. Address map for this block of registers: System Clock Divider Block Register Offsets.

3.2.8 Bias Register Block Address Map

The Bias block has a base address of 0xF4. The addresses shown below are offsets starting from this base address.

Table 9. Bias Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	Reserved	Reserved
0x02	hword	BIAS_STS Register	Bias circuit status. Address map for this block of registers: Bias Block Register Offsets.

3.2.9 Crystal Register Block Address Map

The Crystal block has a base address of 0xF8. The addresses shown below are offsets starting from this base address.

Table 10. Crystal Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	word	XO_CNFG Register	Crystal oscillator circuit control. Address map for this block of registers: Crystal Block Register Offsets.

3.2.10 Clock Output Register Block Address Map

The Clock Output 0 block has a base address of 0x100.
The Clock Output 1 block has a base address of 0x108.
The Clock Output 2 block has a base address of 0x110.
The Clock Output 3 block has a base address of 0x118.
The addresses shown below are offsets starting from this base address.

Table 11. Clock Output Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	OD_CNFG Register	Output Divider control. Address map for this block of registers: Clock Output Block Register Offsets.
0x02	byte	ODRV_EN Register	Output driver enable control. Address map for this block of registers: Clock Output Block Register Offsets.
0x03	byte	ODRV_MODE_CNFG Register	Output driver mode control. Address map for this block of registers: Clock Output Block Register Offsets.
0x04	byte	ODRV_AMP_CNFG Register	Output driver amplitude control. Address map for this block of registers: Clock Output Block Register Offsets.

3.2.11 Clock Reference Register Block Address Map

The Clock Reference Register block has a base address of 0x120. The addresses shown below are offsets starting from this base address.

Table 12. Clock Reference Addresses

Offset	Size	Register Name	Register Description
0x00	word	PREDIV_CNFG Register	Reference Clock Input Divider control. Address map for this block of registers: Clock Reference Addresses.

3.2.12 GPIO Register Block Address Map

The GPIO Register block has a base address of 0x130. The addresses shown below are offsets starting from this base address.

Table 13. GPIO Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	OE_CNFG Register	Configuration control for Output Enable input pin. Address map for this block of registers: GPIO Block Register Offsets.
0x01	byte	IO_CNFG Register	Miscellaneous Input/Output Configuration. Address map for this block of registers: GPIO Block Register Offsets.
0x02	hword	LOCK_CNFG Register	Lock output configuration control. Address map for this block of registers: GPIO Block Register Offsets.
0x04	hword	Reserved	-
0x06	byte	Reserved	Reserved
0x07	byte	STARTUP_STS Register	Start-up status. Address map for this block of registers: GPIO Block Register Offsets.
0x08	byte	GPIO_STS Register	GPIO status. Address map for this block of registers: GPIO Block Register Offsets.
0x0C	word	SCRATCH0 Register	Software Scratch Register 0. Address map for this block of registers: GPIO Block Register Offsets.

3.2.13 SSI Register Block Address Map

The SSI Register block has a base address of 0x140. The addresses shown below are offsets starting from this base address.

Table 14. SSI Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	byte	SPI_CNFG Register	SPI mode configuration. Address map for this block of registers: SSI Block Register Offsets.
0x01	byte	I2C_FLTR_CNFG Register	I^{2}C mode configuration. Address map for this block of registers: SSI Block Register Offsets.
0x02	byte	I2C_TIMING_CNFG Register	I^{2}C mode timing configuration. Address map for this block of registers: SSI Block Register Offsets.
0x03	byte	I2C_ADDR_CNFG Register	I^{2}C mode device address configuration. Address map for this block of registers: SSI Block Register Offsets.
0x04	byte	SSI_GLOBAL_CNFG Register	Slave Serial Interface Global configuration. Address map for this block of registers: SSI Block Register Offsets.

3.2.14 APLL Register Block Address Map

The Analog PLL block has a base address of 0x150. The addresses shown below are offsets starting from this base address.

Table 15. APLL Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	word	APLL_FB_DIV_FRAC Register	APLL Feedback Divider Fraction Numerator value. Address map for this block of registers: APLL Block Register Offsets.
0x04	hword	APLL_FB_DIV_INT Register	APLL Feedback Divider Integer value. Address map for this block of registers: APLL Block Register Offsets.
0x06	byte	APLL_FB_SDM_CNFG Register	APLL Feedback SDM control. Address map for this block of registers: APLL Block Register Offsets.
0x07	byte	APLL_CNFG Register	APLL Configuration control. Address map for this block of registers: APLL Block Register Offsets.
0x08	hword	Reserved	Reserved
0x0A	byte	LPF_CNFG Register	APLL Loop Filter Configuration. Address map for this block of registers: APLL Block Register Offsets.
0x0B	byte	LPF_3RD_CNFG Register	APLL Loop Filter 3rd Pole control. Address map for this block of registers: APLL Block Register Offsets.
0x0C	byte	Reserved	Reserved
0x0D	byte	Reserved	Reserved
0x0E	byte	Reserved	Reserved
0x0F	byte	Reserved	Reserved
0x10	byte	Reserved	Reserved
0x12	hword	Reserved	Reserved
0x14	hword	APLL_LOCK_CNFG Register	APLL Lock Detector control. Address map for this block of registers: APLL Block Register Offsets.
0x16	byte	APLL_LOCK_THRSH Register	APLL Precision Lock Detector Threshold control. Address map for this block of registers: APLL Block Register Offsets.
0x17	byte	VCO_CAL_STS Register	APLL VCO Calibration status. Address map for this block of registers: APLL Block Register Offsets.

Table 15. APLL Block Register Offsets (Cont.)

Offset	Size	Register Name	Register Description
0x18	byte	APLL_STS Register	APLL Lock status. Address map for this block of registers: APLL Block Register Offsets.
0x19	byte	APLL_EVENT Register	APLL Event status. Address map for this block of registers: APLL Block Register Offsets.
0x1A	byte	APLL_LOL_CNT Register	APLL Loss-of-Lock Event counter. Address map for this block of registers: APLL Block Register Offsets.

3.2.15 Clock Input Register Block Address Map

The Clock Input block has a base address of 0x190. The addresses shown below are offsets starting from this base address.

Table 16. Clock Input Block Register Offsets

Offset	Size	Register Name	Register Description
0x00	hword	REF_CLK_IN_CNFG Register	Reference Clock Input Pad configuration. Address map for this block of registers: Clock Input Block Register Offsets.

4. Register Descriptions

4.1 GLOBAL Registers

4.1.1 VENDOR_ID Register

Device vendor identification code. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default	Description
15:12	dev_id_type	RO	0x1	Device ID Block Type. A value of 0x1 indicates that this register is followed by a 16-bit Device ID register, a 16-bit Device Revision register, and a 16-bit Device Programming register.
11	reserved	RO	0x0	reserved.
10:0	vendor_id	RO	0x33	Vendor ID. Renesas Electronics JTAG ID.

4.1.2 DEVICE_ID Register

Device-specific identification code. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:0	device_id	RW	0x304A	Device ID.

4.1.3 DEVICE_REV Register

Device revision identification information. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:13	reserved	RO	0x0	Reserved
12:8	font_id	RO	0x2	Font ID. Font ID to distinguish die variants. Decode as follows: ▪ 0x0 = Font 0 (Font 0) ▪ 0x1 = Font 1 (Font 1) ▪ 0x2 = Font 2 (Font 2)
7:4	ana_rev	RO	0x3	Hardware analog revision. Decode as follows: ▪ 0x1 = First revision (TV) ▪ 0x2 = Second revision (RevA) ▪ 0x3 = Third revision (RevB)
3:0	dig_rev	RO	0x2	Hardware digital revision. Decode as follows: ▪ 0x1 = First revision (TV) ▪ 0x2 = Second revision (RevA/B)

4.1.4 DEVICE_PGM Register

Identifies any factory OTP pre-programmed configuration. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:0	dash_code	RW	0x0	Dash code. Decimal value assigned by Renesas Electronics to identify the user configuration loaded in OTP at the factory. This field is writeable and is configured from the OTP common configuration programmed at the factory. ▪ 0x0 = No user configurations are programmed at the factory

4.1.5 DEVICE_CNFG Register

Device overall configuration settings. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	digldo_cnf	RW	0x0	Digital LDO voltage select. Selects the digital LDO voltage level. This setting is intended for test purposes only. ▪ 0x0 = 1.25V ▪ 0x1 = 1.32V
6:4	xo_delay	RW	0x0	Crystal Startup Delay. Selects the wait time for the internal crystal oscillator circuit during the startup sequence. The default setting of 1ms should be sufficient for all crystals. This setting is intended for debug purposes only. ▪ 0x0 = 1 ms ▪ 0x1 = 2.5 ms ▪ 0x2 = 5 ms ▪ 0x3 = 7.5 ms ▪ 0x4 = 10 ms ▪ 0x5 = 0.5 ms ▪ 0x6 = 15 ms ▪ 0x7 = reserved
3:0	config_sel	RW	0x4	User Configuration Select. Controls the selection of the user configuration stored in OTP to read on start-up.

4.1.6 DEV_RESET Register

Device reset commands. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	reserved.
5	input_div_global_setb	RW	0x1	Input Dividers Common Set. When cleared, both input dividers get held in set mode (bit is active low). This allows to set and release both dividers at roughly the same time.
4	out_global_oe	RW	0x1	Output Global OE. This bit allows manual CSR control of the output OE.
3:2	reserved	RO	0x0	reserved.
1	divider_sync	RW	0x0	Divider synchronization. Writing this bit to 1 synchronizes the Output Dividers and the DPLL feedback divider (if the DPLL is enabled). The output clocks are squelched for approximately 10µs. *Note*: This bit must be written to 0 before it can be triggered again by writing it to 1.
0	apll_reinit	RW	0x0	APLL Reinitialization. Writing this bit to 1 restarts the startup sequence from the VCO calibration step, including divider synchronization. *Note*: This bit must be written to 0 before it can be triggered again by writing it to 1.

4.1.7 SW_RESET Register

Software reset command. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:12	reserved	RO	0x0	reserved.
11	reserved	RW	0x0	reserved
10:9	reserved	RO	0x0	reserved.
8	bias_cal_sw_rst	RW	0x0	Bias Cal Software reset. The bias calibration logic is held in reset while this bit is set to 1.
7	tdc_apll_dig_sw_rst	RW	0x0	TDC Software reset. The TDC logic is held in reset while this bit is set to 1.
6	dpll_sw_rst	RW	0x0	DPLL Software reset. The DPLL is held in reset while this bit is set to 1.
7:6	reserved	RO	0x0	reserved.
5	actmon1_sw_rst	RW	0x0	ACTMON1 Software reset. The Activity Monitor 1, which monitors the nCLKIN input, is held in reset while this bit is set to 1.
4	actmon0_sw_rst	RW	0x0	ACTMON0 Software reset. The Activity Monitor 0, which monitors the CLKIN input, is held in reset while this bit is set to 1.
3	losmon2_sw_rst	RW	0x0	LOSMON2 Software reset. The Loss-of-signal Monitor 2, which monitors the crystal input (XIN/REF), is held in reset while this bit is set to 1.
2	losmon1_sw_rst	RW	0x0	LOSMON1 Software reset. The Loss-of-signal Monitor 1, which monitors the nCLKIN input, is held in reset while this bit is set to 1.

Bit Field	Field Name	Type	Default Value	Description
1	losmon0_sw_rst	RW	0x0	LOSMON0 Software reset. The Loss-of-signal Monitor 0, which monitors the CLKIN input, is held in reset while this bit is set to 1.
0	otp_sw_rst	RW	0x0	OTP Software reset. The OTP logic is held in reset while this bit is set to 1.

4.1.8 CLOCK_GATE Register

Clock gating control. Setting of any of the bits in this register stops the internal clocks to the indicated logic block(s). The Renesas Electronics Timing Commander Software automatically determines which logic can be disabled for a specific configuration. Contact Renesas Electronics if further details are needed.

Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:12	reserved	RO	0x0	reserved.
11	dig_cg	RW	0x0	Digital Logic Clock Gate. All digital clocks that do not have separate clock gating control bits in this register are gated while this bit is set to 1. Because this gates the register bus clock, no further register access is possible through the serial port. The device must be power cycled to recover. This bit is intended for test purposes only (shut down all digital logic during analog characterization or debug).
10:9	reserved	RO	0x0	reserved.
8	reserved	RW	0x0	reserved
7	reserved	RO	0x0	reserved.
6	reserved	RW	0x0	reserved
5	actmon1_cg	RW	0x0	ACTMON1 Clock Gate. The Activity Monitor 1 is clock gated while this bit is set to 1.
4	actmon0_cg	RW	0x0	ACTMON0 Clock Gate. The Activity Monitor 0 is clock gated while this bit is set to 1.
3	losmon2_cg	RW	0x0	LOSMON2 Clock Gate. The Loss-of-signal Monitor 2 is clock gated while this bit is set to 1.
2	losmon1_cg	RW	0x0	LOSMON1 Clock Gate. The Loss-of-signal Monitor 1 is clock gated while this bit is set to 1.
1	losmon0_cg	RW	0x0	LOSMON0 Clock Gate. The Loss-of-signal Monitor 0 is clock gated while this bit is set to 1.
0	reserved	RW	0x0	reserved.

4.1.9 DEVICE_STS Register

Device status. Address map for this block of registers: Global Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:5	startup_seq_sts	RO	0x0	Startup Sequence Status. Status related to the startup sequence. This field is intended for debug purposes only. bit [0] = Bias calibration timeout (2ms) bit [1] = OTP load timeout (10ms) bit [2] = APLL lock timeout (2ms)
4	osc_fallback	RO	0x0	Power-on-Reset Ring Oscillator Fallback. Set to 1 if the system clock divider output does not begin toggling during the startup sequence and the reset controller muxes the ring oscillator clock onto the system clock instead.
3	device_ready	RO	0x0	Device Ready. Set to 1 when the OTP load completes during the startup sequence.
2	reserved	RO	0x0	reserved.
1:0	config_loaded	RO	0x0	User Configuration Loaded. Indicates the user configuration loaded from OTP on start-up. Note that the common configuration is always loaded in addition to any user configurations are loaded.

4.2 INT Registers

4.2.1 INT_EN Register

Interrupt Enable control. Address map for this block of registers: Interrupt Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15	device_int_en	RW	0x0	Device interrupt enable. Overall device interrupt enable. When this field is set to 1, the device interrupt is asserted while device_int_sts is 1.
14:12	reserved	RO	0x0	reserved.
11:9	reserved	RW	0x0	reserved.
8	act1_int_en	RW	0x0	nCLKIN Activity Monitor interrupt enable. When this field is set to 1, the act1_int_sts bit contributes to the device interrupt
7	act0_int_en	RW	0x0	CLKIN Activity Monitor interrupt enable. When this field is set to 1, the act0_int_sts bit contributes to the device interrupt.
6	los2_int_en	RW	0x0	XTAL Monitor Loss-of-Signal interrupt enable. When this field is set to 1, the los2_int_sts bit contributes to the device interrupt.
5	los1_int_en	RW	0x0	nCLKIN Monitor Loss-of-Signal interrupt enable. When this field is set to 1, the los1_int_sts bit contributes to the device interrupt
4	los0_int_en	RW	0x0	CLKIN Monitor Loss-of-Signal interrupt enable. When this field is set to 1, the los0_int_sts bit contributes to the device interrupt.

Bit Field	Field Name	Type	Default Value	Description
3	dpll_state_ch_int_en	RW	0x0	DPLL State Change interrupt enable. When this field is set to 1, the dpll_state_ch_int_sts bit contributes to the device interrupt.
2	dpll_holdover_int_en	RW	0x0	DPLL Holdover interrupt enable. When this field is set to 1, the dpll_holdover_int_sts bit contributes to the device interrupt.
1	dpll_lol_int_en	RW	0x0	DPLL Loss-of-Lock interrupt enable. When this field is set to 1, the dpll_lol_int_sts bit contributes to the device interrupt.
0	apll_lol_int_en	RW	0x0	APLL Loss-of-Lock interrupt enable. When this field is set to 1, the apll_lol_int_sts bit contributes to the device interrupt.

4.2.2 INT_STS Register

Interrupt Status. Address map for this block of registers: Interrupt Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15	device_int_sts	RO	0x0	Device interrupt status. Overall device interrupt status. This bit is the OR of all the other interrupt status bits in this register after masking by their respective interrupt enable bits in INT_EN Register. This bit is masked by device_int_en. The resulting signal is output on the LOCK pin when lock_sel selects the device interrupt.
14:9	reserved	RO	0x0	reserved.
8	act1_int_sts	RO	0x0	nCLKIN Activity Monitor interrupt status Mirrors the nCLKIN act_evt event bit
7	act0_int_sts	RO	0x0	CLKIN Activity Monitor interrupt status Mirrors the CLKIN act_evt event bit
6	los2_int_sts	RO	0x0	XTAL Monitor Loss-of-Signal interrupt status Mirrors the XIN/REF los_evt event bit
5	los1_int_sts	RO	0x0	nCLKIN Monitor Loss-of-Signal interrupt status Mirrors the nCLKIN los_evt event bit
4	los0_int_sts	RO	0x0	CLKIN Monitor Loss-of-Signal interrupt status Mirrors the CLKIN los_evt event bit
3	dpll_state_ch_int_sts	RO	0x0	DPLL State Change interrupt status Mirrors the dpll_state_ch event bit
2	dpll_holdover_int_sts	RO	0x0	DPLL Holdover interrupt status. Mirrors the dpll_holdover event bit.
1	dpll_lol_int_sts	RO	0x0	DPLL Loss-of-Lock interrupt status. Mirrors the dpll_lol event bit.
0	apll_lol_int_sts	RO	0x0	APLL Loss-of-Lock interrupt status. Mirrors the apll_lol event bit.

4.3 LOSMON Registers

Before reprogramming a Loss of Signal Monitor block, the corresponding losmon0_sw_rst, losmon1_sw_rst, or losmon2_sw_rst bit should be set. When programming is done, it should then be cleared.

4.3.1 LOSMON_STS Register

LOS Monitor Status. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:2	reserved	RO	0x0	reserved.
1	ref_invalid	RO	0x1	Reference Clock Invalid status. Indicates whether this reference clock is currently considered to be invalid. This occurs if the clock is disqualified by one or more of the Loss-of-Signal and Activity monitors or ref_disable is set to 1. ▪ 0x0 = Clock is valid ▪ 0x1 = Clock is invalid
0	los_sts	RO	0x1	Loss-of-Signal status. Current value of the LOS status from the clock monitor: ▪ 0x0 = Clock meets the monitoring criteria ▪ 0x1 = Loss-of-signal detected

4.3.2 LOSMON_EVENT Register

LOS Monitor Event Status. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:1	reserved	RO	0x0	reserved.
0	los_evt	RW1C	0x1	Loss-of-Signal Event status. Set while the clock monitor asserts LOS. This bit cannot be cleared by software while the LOS condition persists. This bit is set when the block comes out of reset and needs to be cleared after proper programming. ▪ 0x0 = Loss-of-signal not detected since the last time the bit was cleared ▪ 0x1 = Loss-of-signal detected since the last time the bit was cleared

4.3.3 LOSMON_QUAL Register

LOS Monitor Qualify Counter Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	los_good_times	RW	0x0	LOS Monitor Qualification Count If this number of consecutive accepted clock LOS monitoring windows occur without a rejected window, then the clock is qualified and los_sts is set to 0. A value of 0 is the same as using the value 1.
3:0	los_fail_times	RW	0x0	LOS Monitor Disqualification Count If this number of rejected clock LOS monitoring windows occur without qualifying the clock, then the clock is disqualified and los_sts is set to 1. A value of 0 is the same as using the value 1.

4.3.4 LOSMON_WINDOW Register

LOS Monitor Window Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:8	reserved	RO	0x0	reserved.
7:3	los_div_ratio	RW	0x0	LOS Monitor Divide Ratio This divide ratio must be set such that the monitored clock nominal frequency divided by los_div_ratio is less than 1/8 of the system clock frequency to achieve 25% accuracy. One period of the divided clock is the monitoring window duration. A value of 0 or 1 means divide by 1. The value 0x1F is not supported.
2	reserved	RO	0x0	reserved.
1	ref_disable	RW	0x0	Reference Clock Selection Disable Controls whether this reference clock may be selected as the DPLL reference clock. Not applicable for LOSMON2 (XTAL monitor). ▪ 0 = Reference clock may be selected, subject to qualification by the Loss-of-Signal, Activity and Frequency monitors, and prioritization according to ref_priority ▪ 1 = Reference clock cannot be selected, ref_invalid is 1.
0	los_fail_mask	RW	0x0	LOS Monitor Failure Mask Masks the LOS monitor status los_sts contribution to ref_invalid. ▪ 0 = los_sts contributes to ref_invalid ▪ 1 = los_sts does not contribute to ref_invalid

4.3.5 LOSMON_THRESH Register

LOS Monitor Threshold Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:29	reserved	RO	0x0	reserved.
28:16	los_acc_margin	RW	0x0	LOS Monitor Accept Threshold An accepted clock monitoring window occurs when the final monitor counter value is within los_nom_num ± los_acc_margin.
15:13	reserved	RO	0x0	reserved.
12:0	los_rej_margin	RW	0x0	LOS Monitor Reject Threshold A rejected clock monitoring window occurs when the final monitor counter value is outside of los_nom_num ± los_rej_margin.

4.3.6 LOSMON_NOMINAL Register

LOS Monitor Nominal Number Configuration. Address map for this block of registers: LOS Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:13	reserved	RO	0x0	reserved.
12:0	los_nom_num	RW	0x0	LOS Monitor Nominal Cycle Count Sets the expected number of system clock periods within one monitor window. Set to 0x0 to disable the LOS monitor. Disabling the monitor causes the los_sts to get asserted, therefore the los_fail_mask should also be set when this field is written to 0x0.

4.4 ACTMON Registers

Note that before reprogramming an Activity Monitor, the corresponding actmon0_sw_rst or actmon1_sw_rst bit should be set. When programming is done, it should then be cleared.

4.4.1 ACTMON_STS Register

Activity Monitor Status. Address map for this block of registers: ACT Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:1	reserved	RO	0x0	reserved.
0	act_sts	RO	0x1	Activity Monitor status. Current value of the qualification status from the activity monitor: ▪ 0x0 = Clock meets the monitoring criteria, clock qualified ▪ 0x1 = failure detected, clock disqualified

4.4.2 ACTMON_EVENT Register

Activity Monitor Event Status. Address map for this block of registers: ACT Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:1	reserved	RO	0x0	reserved.
0	act_evt	RW1C	0x1	Activity Monitor event status. Set while the activity monitor disqualifies the clock. This bit cannot be cleared by software while the disqualified condition persists. This bit is set when the block comes out of reset and needs to be cleared after proper programming. ▪ 0x0 = Activity monitor has not disqualified the clock since the last time the bit was cleared ▪ 0x1 = Activity monitor has disqualified the clock since the last time the bit was cleared

4.4.3 ACTMON_WINDOW Register

Activity Monitor Window Configuration. Address map for this block of registers: ACT Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:21	reserved	RO	0x0	reserved.
20	act_fail_mask	RW	0x0	Activity Monitor Failure Mask Masks the activity monitor status act_sts. ▪ 0 = Status is not masked ▪ 1 = Forces clock to be considered as qualified
19	reserved	RO	0x0	reserved.
18:0	act_div_ratio	RW	0x0	Activity Monitor Divide Ratio This divide ratio must be set such that the monitored clock nominal frequency divided by act_div_ratio is as close as possible to 100Hz, creating a 10ms monitoring window. A value of 0 means divide by 1. A value of 0x7FFFF is reserved.

4.4.4 ACTMON_THRESH Register

Activity Monitor Threshold Configuration. Address map for this block of registers: ACT Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
63:54	reserved	RO	0x0	reserved.
53:32	act_acc_margin	RW	0x0	Activity Monitor Accept Threshold An accepted clock monitoring window occurs when the final monitor counter value is within act_nom_num ± act_acc_margin. One accepted window qualifies the clock and act_sts is set to 0.
31:22	reserved	RO	0x0	reserved.
21:0	act_rej_margin	RW	0x0	Activity Monitor Reject Threshold A rejected clock monitoring window occurs when the final monitor counter value is outside of act_nom_num ± act_rej_margin. One rejected window disqualifies the clock and act_sts is set to 1.

4.4.5 ACTMON_NOMINAL Register

Activity Monitor Nominal Number Configuration. Address map for this block of registers: ACT Monitor Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:22	reserved	RO	0x0	reserved.
21:0	act_nom_num	RW	0x0	Activity Monitor Nominal Cycle Count Sets the expected number of clock periods of the ring oscillator frequency divided by 4 (nominally 216MHz) within one monitor window. Set to 0x0 to disable the activity monitor. Disabling the monitor causes the act_sts to get asserted, therefore the act_fail_mask should also be set when this field gets written to 0x0.

4.5 DPLL Registers

4.5.1 DPLL_REF_FB_CNFG Register

DPLL Ref and Fb Clock Configuration. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	dpll_ref_sel_mode	RW	0x0	DPLL reference clock selection mode ▪ 0x0 = manual mode, reference selection is based on the setting of dpll_ref_sel ▪ 0x2 = auto mode
5	reserved	RO	0x0	reserved.
4	dpll_ref_sel	RW	0x0	DPLL manual reference clock selection ▪ 0x0 = clkin0 ▪ 0x1 = clkin1
3:2	reserved	RO	0x0	reserved.
1	dpll_revertive_en	RW	0x0	DPLL revertive reference switch ▪ 0x0 = non-revertive ▪ 0x1 = revertive
0	dpll_hitless_en	RW	0x0	DPLL hitless reference switch ▪ 0x0 = hitless disabled ▪ 0x1 = hitless enabled

4.5.2 DPLL_MODE Register

Digital PLL mode control. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	bw_damp_sw	RW	0x1	Automatic bandwidth/damping switching. Enables the DPLL to switch to the Locking Loop Filter bandwidth and damping settings when the DPLL is in the Acquire state while locking. Refer to dpll_lock_timer. ▪ 0x0 = always use Normal Operation settings. ▪ 0x1 = use Locking settings when the DPLL is in the Acquire state.
6	los_to_freerun	RW	0x0	Reference Loss-of-Signal to Freerun. Controls whether the DPLL enters Freerun or Holdover mode when the current reference clock is invalid. ▪ 0x0 = Holdover. ▪ 0x1 = Freerun.
5:4	reserved	RW	0x0	reserved
3	filter_update_dis	RW	0x0	DPLL filter update disable. This bit must be set to 1 before reconfiguring any DPLL registers while the DPLL is enabled, and then must be cleared after the reconfiguration finishes. The exception is write_freq which may be controlled dynamically and automatically suppresses filter_update when written.
2	dpll_en	RW	0x0	DPLL Enable. Controls whether the DPLL is enabled. ▪ 0x0 = Synthesizer/DCO mode. DPLL (except loop filter and scaler blocks) is disabled (clock gated to reduce power) ▪ 0x1 = Jitter Attenuator mode. DPLL is enabled.

Bit Field	Field Name	Type	Default Value	Description
1:0	dpll_mode	RW	0x1	DPLL mode selection. Selects DPLL mode: ▪ 0x0 = Forces DPLL into Freerun state ▪ 0x1 = Places the DPLL in Normal (automatic) mode. This is the normal setting for Jitter Attenuator mode ▪ 0x2 = Forces DPLL into Holdover state. ▪ 0x3 = Places DPLL in Write Frequency mode. This is the normal setting in DCO mode.

4.5.3 DPLL_DECIMATOR Register

Decimator configuration control. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	reserved	RO	0x0	reserved.
6:4	dec_hitless_bw_shift	RW	0x3	Hitless Switch Decimator Bandwidth Shift to set the decimator bandwidth during a hitless reference switch or holdover-normal switch for measuring the phase offset. If dpll_histless_en is set to zero, this field is ignored.
3:0	dec_bw_shift	RW	0x6	Main Decimator Bandwidth. Shift to set the main decimator bandwidth. 0 puts the decimator in feed-through (infinite bandwidth).

4.5.4 DPLL_TRIM_OFFSET Register

DPLL Crystal trim offset. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:0	xtal_trim	RW	0x0	Crystal Trim Offset. Crystal fractional frequency offset compensation. This is an 8-bit 2's complement value. Resolution = 2^{-20} ≈ 1 ppm, Range = ±2^{-13} ≈ ±122 ppm.

4.5.5 DPLL_HOLDOVER_CNFG Register

Holdover Configuration. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:11	holdover_bw_shift	RW	0x7	Holdover Filter Bandwidth Shift. Coarse control of the holdover bandwidth. A value of zero disables the holdover filter (infinite bandwidth). The valid range is 0-20. Values larger than 20 are limited internally to 20.
10:8	holdover_bw_mult	RW	0x0	Holdover Filter Bandwidth Multiplier. Fine control of the holdover filter bandwidth. A value of zero disables the holdover filter (infinite bandwidth), which is also the default setting.

Bit Field	Field Name	Type	Default Value	Description
7:4	holdover_history	RW	0x0	Holdover history ▪ 0x0 = instantaneous ▪ 0x1 = 1 second ▪ 0x2 = 2 seconds ▪ 0x3 = 3 seconds ▪ ... ▪ 0x9 = 9 seconds ▪ 0xA = 10 seconds
3:0	dpll_lol_cnt_thresh	RW	0x0	DPLL Loss-of-Lock Counter Threshold. While the DPLL Loss-of-Lock counter (*dpll_lol_cnt*) exceeds this threshold, the *dpll_lol_lmt* bit is set.

4.5.6 DPLL_BANDWIDTH Register

DPLL Bandwidth configuration. Address map for this block of registers: DPLL Block Register Offsets.

Use Renesas Electronics's Timing Commander Software to provide appropriate settings. This section supports separate settings for fast-lock acquisition (Acquire) and regular locked operation (Normal Operation).

Bit Field	Field Name	Type	Default Value	Description
15:11	acquire_bw_shift	RW	0xE	Acquire Loop Filter Bandwidth Shift. Coarse control of the DPLL loop filter bandwidth in the Acquire state while locking to the input clock. Default bandwidth = 1023 Hz.
10:8	acquire_bw_mult	RW	0x0	Acquire Loop Filter Bandwidth Multiplier. Fine control of the DPLL loop filter bandwidth in the Acquire state while locking to the input clock. Default bandwidth = 1023 Hz.
7:3	normal_bw_shift	RW	0xB	Normal Operation Loop Filter Bandwidth Shift. Coarse control of the DPLL loop filter bandwidth in the Normal state when locked to the input clock. Default bandwidth = 127 Hz.
2:0	normal_bw_mult	RW	0x0	Normal Operation Loop Filter Bandwidth Multiplier. Fine control of the DPLL loop filter bandwidth in the Normal state when locked to the input clock. Default bandwidth = 127 Hz.

4.5.7 DPLL_DAMPING Register

DPLL Damping control. Address map for this block of registers: DPLL Block Register Offsets

Use Renesas Electronics's Timing Commander Software to provide appropriate settings. This section supports separate settings for fast-lock acquisition (Acquire) and regular locked operation (Normal Operation).

Bit Field	Field Name	Type	Default Value	Description
15:14	reserved	RO	0x0	reserved.
13:11	acquire_damping_shift	RW	0x5	Acquire Loop Filter Damping Shift. Coarse control of the DPLL loop filter damping in the Acquire state while locking to the input clock. Default damping causes 1.1 dB peaking in the frequency domain jitter transfer function.

Bit Field	Field Name	Type	Default Value	Description
10:8	acquire_damping_mult	RW	0x1	Acquire Loop Filter Damping Multiplier. Fine control of the DPLL loop filter damping in the Acquire state while locking to the input clock. Default damping causes 1.1 dB peaking in the frequency domain jitter transfer function.
7:6	reserved	RO	0x0	reserved.
5:3	normal_damping_shift	RW	0x0	Normal Operation Loop Filter Damping Shift. Coarse control of the DPLL loop filter damping in the Normal state when locked to the input clock. Default damping causes 0.1 dB peaking in the frequency domain jitter transfer function.
2:0	normal_damping_mult	RW	0x1	Normal Operation Loop Filter Damping Multiplier. Fine control of the DPLL loop filter damping in the Normal state when locked to the input clock. Default damping causes 0.1 dB peaking in the frequency domain jitter transfer function.

4.5.8 DPLL_PHASE_SLOPE_LIMIT Register

DPLL Phase Slope Limit control. Address map for this block of registers: DPLL Block Register Offsets

Bit Field	Field Name	Type	Default Value	Description
31:29	reserved	RO	0x0	reserved.
28:0	phase_slope_limit	RW	0x1FFFFFF	Phase Slope Limit. Control of the phase slope limit of the output clocks. This represents the maximum instant relative frequency change of the output clock. This is an unsigned unitless number although it is often expressed as µs/ or ns/s. Renesas recommends programming a value that is approx. 10% smaller than the required limit to leave some room for the integrator to adjust to frequency offsets. The resolution of 1 LSB is 2-35 = 2.91e-11 = 29. ps/s.

4.5.9 DPLL_FB_DIV_NUM Register

DPLL Feedback Fraction Numerator value. Address map for this block of registers: DPLL Block Register Offsets.

Use Renesas Electronics's Timing Commander Software to provide appropriate settings.

Bit Field	Field Name	Type	Default Value	Description
63:48	reserved	RO	0x0	reserved.
47:0	fb_div_num	RW	0x0	Feedback Divider Numerator. DPLL feedback divide numerator value. Refer to fb_div_int for details. This register is part of the atomic group consisting of DPLL_FB_DIV_NUM Register, DPLL_FB_DIV_DEN Register and DPLL_FB_DIV_INT Register. When the most significant byte (bits [47:40]) of fb_div_num or fb_div_den, is written, the value of both these fields, in addition to the one in fb_div_int is applied to the DPLL.

4.5.10 DPLL_FB_DIV_DEN Register

DPLL Feedback Fraction Denominator value. Address map for this block of registers: DPLL Block Register Offsets.

Use Renesas Electronics's Timing Commander Software to provide appropriate settings.

Bit Field	Field Name	Type	Default Value	Description
63:48	reserved	RO	0x0	reserved.
47:0	fb_div_den	RW	0x800000	Feedback Divider Denominator. DPLL feedback divide denominator value. Refer to fb_div_int for details. When the fb_div_num field is non-zero, the fraction has to be set such that the MSB of the fb_div_den is set (both fields should be shifted up by the same amount). This register is part of the atomic group consisting of DPLL_FB_DIV_NUM Register, DPLL_FB_DIV_DEN Register and DPLL_FB_DIV_INT Register. When the most significant byte (bits [47:40]) of fb_div_num or fb_div_den, is written, the value of both these fields, in addition to the one in fb_div_int is applied to the DPLL.

4.5.11 DPLL_FB_DIV_INT Register

DPLL Feedback Integer value. Address map for this block of registers: DPLL Block Register Offsets.

Use Renesas Electronics's Timing Commander Software to provide appropriate settings.

Bit Field	Field Name	Type	Default Value	Description
15:14	reserved	RO	0x0	reserved.
13:0	fb_div_int	RW	0x190	DPLL Feedback Clock Divider Integer. DPLL feedback divide integer value. The DPLL feedback clock frequency must be no more than 33 MHz, and must be equal to the frequency of the reference clock divided by id_ratio, or equal to the reference clock when the input divider is bypassed by id_byp_en. This register is part of the atomic group consisting of DPLL_FB_DIV_NUM Register, DPLL_FB_DIV_DEN Register and DPLL_FB_DIV_INT Register. When this field is changed from its previous value, the value of this field, in addition to the values from fb_div_num, fb_div_den get applied to the DPLL.

4.5.12 DPLL_FB_CORR Register

DPLL Feedback Correction Configuration. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	reserved.
9	fine_rev	RW	0x0	TDC Fine Timestamp Bit Reversal. Selects the bit ordering of the fine timestamp signals from the TDC analog to digital. This setting is intended for debug purposes only. ▪ 0x0 = Analog 30:0 maps to digital 30:0 ▪ 0x1 = Analog 0:30 maps to digital 30:0

Bit Field	Field Name	Type	Default Value	Description
8:7	pec_delay	RW	0x0	PEC Delay. Phase error correction delay. Intended for debug purposes only. ▪ 0x0 = sdm error no delay ▪ 0x1 = sdm error delay one cycle ▪ 0x2 = same as 0x0 ▪ 0x3 = same as 0x0
6:0	pec_corr_mult	RW	0x0	Feedback Correction Multiplier. Multiplier to get the FB SDM remainder bits on the same resolution as the TDC phase bits (resolution ≈18.7 ps if TDC APLL runs at 864MHz). Should be set as follows: pec_cor_mult = (Tvco/TDC_step) * (128/fb_div_den[47:41])

4.5.13 DPLL_PHASE_OFFSET Register

DPLL Phase Offset configuration. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:30	reserved	RO	0x0	reserved.
29:0	phase_offset	RW	0x0	Phase Offset. Manually sets the phase offset between the reference and feedback clocks. This is a 30-bit 2's complement value. The resolution is the TDC resolution / 8 (≈ 2.3 ps) and the range is ≈ ±1.26 ms. This allows all outputs to be adjusted in terms of their phase relationship to the input. All outputs move together using this precision setting. This field is not used when hitless switching is enabled. This register is atomic. When the most significant byte (bits [31:24]) is written, the new value is applied to the APLL.

4.5.14 DPLL_WRITE_FREQ Register

DPLL Write Frequency command. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:29	reserved	RO	0x0	reserved.
28:0	write_freq	RW	0x0	Write Frequency. Frequency control word for synthesizer/DCO mode. This is a 29-bit 2's complement value. The units are 2^{-40} * 1e6 [ppm]. This provides a maximum setting of ±244ppm. An update to this multi-byte register only takes effect when the most significant byte (bits [28:24]) are written, the new value is applied to the DPLL.

4.5.15 DPLL_LOCK Register

DPLL Lock Detection control. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:16	dpll_lock_timer	RW	0x00FF	DPLL lock timer. Specifies the time interval during which the absolute value of the phase detector error must remain below the DPLL lock threshold (dpll_lock_thresh) to declare lock. The DPLL switches from the Acquire state to the Normal state when the threshold has been met for half of this time interval. If enabled by bw_damp_sw, the loop filter bandwidth and damping settings revert at this time from the Acquire settings to the Normal settings. When the threshold has been met again for half of this time interval, the DPLL declares lock. The units are ms.
15:0	dpll_lock_thresh	RW	0x0155	DPLL lock threshold. Specifies the threshold that the absolute value of the phase detector error must remain below during the DPLL lock timer (dpll_lock_timer) to declare lock. The units are the 8 * TDC resolution (≈ 149 ps if TDC APLL runs at 864MHz).

4.5.16 DPLL_TDC_DELAY Register

DPLL TDC Delay Control. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:0	tdc_delay	RW	0x1F	TDC delay. Sets the TDC delay which goes to the DPLL, for debug purposes only.

4.5.17 DPLL_STS Register

DPLL Status. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	reserved	RO	0x0	reserved.
6:4	dpll_state_sts	RO	0x0	DPLL state machine's current state. Decode as follows: ▪ 0x0 = freerun ▪ 0x1 = normal/locked ▪ 0x2 = holdover ▪ 0x3 = write_frequency ▪ 0x4 = acquire ▪ 0x5 = hitless switch
3:2	reserved	RO	0x0	reserved.
1	dpll_ref_sel_sts	RO	0x0	DPLL reference clock selection status Indicates the reference clock selected by the DPLL. ▪ 0x0 = clkin0 ▪ 0x1 = clkin1

Bit Field	Field Name	Type	Default Value	Description
0	dpll_lock_sts	RO	0x0	DPLL lock status. Indicates the DPLL lock status: ▪ 0x0 = unlocked ▪ 0x1 = locked

4.5.18 DPLL_EVENT Register

DPLL Event status. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	reserved.
3	dpll_state_ch	RW1C	0x0	DPLL State Change event. Set to 1 when the DPLL state machine changes state.
2	dpll_holdover	RW1C	0x0	DPLL Holdover event. Set to 1 when the DPLL state machine enters the holdover state. When asserted, this bit remains asserted until cleared by a write of '1' to this bit position.
1	dpll_lol_lmt	RW1C	0x0	DPLL Loss-of-Lock Counter Threshold Exceeded status. Set while the DPLL Loss-of-Lock counter (*dpll_lol_cnt*) exceeds the threshold set in *dpll_lol_cnt_thresh*. This bit cannot be cleared by software while the condition persists. ▪ 0x0 = Loss-of-lock counter has not exceeded the threshold since the last time the bit was cleared ▪ 0x1 = Loss-of-lock counter exceeded the threshold since the last time the bit was cleared
0	dpll_lol	RW1C	0x0	DPLL Loss-of-lock event. Set to 1 when the DPLL lock status transitions from locked to unlocked. When asserted, this bit remains asserted until cleared by a write of '1' to this bit position.

4.5.19 DPLL_LOL_CNT Register

DPLL Loss-of-Lock Event Counter. Address map for this block of registers: DPLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	reserved.
3:0	dpll_lol_cnt	RW	0x0	DPLL Loss-of-Lock Counter. This counter increments each time the DPLL lock status de-asserts, and saturates at 0xF. It is cleared by writing it to 0x0, and may be preset by writing the desired value. Preset may be used either as a debug tool or to cause a threshold alarm to happen sooner because the alarm threshold is not configurable. This register can only be written if the block is not clock gated or held in reset (dpll_sw_rst).

4.6 TDC Registers

4.6.1 TDC_REF_DIV_CNFG Register

TDC reference divider control. Address map for this block of registers: TDC Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:3	reserved	RO	0x0	reserved.
2:0	tdc_ref_div_cnfg	RW	0x1	TDC Reference Divider Control. Controls the divide ratio of the TDC reference (either input or CLKIN input, selected by apll_ref_sel). This field should be programmed such that the reference to the TDC APLL is between 10MHz and 30MHz ▪ 0x0 = bypass divider. ▪ 0x1 = divide by2 ▪ 0x2 = divide by 4 ▪ 0x3 = divide by 8 ▪ 0x4 = divide by 16

4.6.2 TDC_FB_SDM_CNFG Register

TDC internal APLL Feedback Divider SDM control. Address map for this block of registers: TDC Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	tdc_fb_sdm_en	RW	0x1	TDC APLL Feedback SDM Enable. Enables the SDM controlling the TDC APLL feedback divider. ▪ 0x0 = SDM disabled, constant integer division by tdc_fb_div_int ▪ 0x1 = SDM enabled, MMD mode
6:2	reserved	RO	0x0	reserved.
1:0	tdc_fb_sdm_order	RW	0x1	TDC APLL Feedback SDM Order. Selects the order of the SDM controlling the feedback divider for the TDC APLL. ▪ 0x0 = Integer ▪ 0x1 = 1st order ▪ 0x2 = 2nd order ▪ 0x3 = reserved

4.6.3 TDC_FB_DIV_INT Register

TDC internal APLL Feedback Divider Integer value. Address map for this block of registers: TDC Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:0	tdc_fb_div_int	RW	0x23	TDC APLL Feedback Divider Integer. Integer portion of the TDC APLL feedback divider.

4.6.4 TDC_FB_DIV_FRAC Register

TDC internal APLL Feedback Divider Fraction value. Address map for this block of registers: TDC Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:0	tdc_fb_div_frac	RW	0x2800	TDC APLL Feedback Fraction. Fraction of the TDC APLL feedback divider. The fraction is calculated as follows: tdc_fb_div_frac/2^{16}.

4.6.5 TDC_DAC_CNFG Register

TDC internal APLL Digital to Analog Converter (DAC) control. Address map for this block of registers: TDC Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:5	reserved	RO	0x0	reserved.
4:0	tdc_dig_set	RW	0x4	TDC APLL Set value. Increases the baseline APLL DCO voltage. The step size is 1/32nd of the full range (nominally 37.5 mV). The dynamic control signal generated by the DAC SDM (0-16) is added to this value to create the DAC input. Values 0x11 to 0x1F are reserved. ▪ 0x0 = no increase ▪ 0x1 = 1/32 increase ▪ 0x2 = 2/32 increase ▪ 0x3 = 3/32 increase ▪ 0x4 = 4/32 increase ▪ 0x5 = 5/32 increase ▪ 0x6 = 6/32 increase ▪ 0x7 = 7/32 increase ▪ 0x8 = 8/32 increase ▪ 0x9 = 9/32 increase ▪ 0xA = 10/32 increase ▪ 0xB = 11/32 increase ▪ 0xC = 12/32 increase ▪ 0xD = 13/32 increase ▪ 0xE = 14/32 increase ▪ 0xF = 15/32 increase ▪ 0x10 = 16/32 increase

4.7 SYSDIV Registers

4.7.1 SYS_DIV_INT Register

System Clock Divider Integer value. Address map for this block of registers: System Clock Divider Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:5	reserved	RO	0x0	reserved.

Bit Field	Field Name	Type	Default Value	Description
4:0	sys_div_int	RW	0xC	System Clock Divide Integer. The system clock divide integer value must be set to produce a system frequency between 180MHz and 333MHz, divided down from the APLL VCO frequency divided by 4. The frequency picked has side effects on various calculations done in other blocks (LOSMON Registers). Normally expected to be between 210MHz and 240MHz. The minimum valid value for this field is10 and the maximum is 15.

4.8 BIAS Registers

4.8.1 BIAS_STS Register

Bias circuit status. Address map for this block of registers: Bias Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:9	reserved	RO	0x0	reserved.
8	bias_cal_in	RO	0x0	Bias Calibration comparator value. Raw bias_cal_in value.
7:5	cnf_bias_cal_eff	RO	0x0	Bias Calibration effective configuration value. Indicates the configuration value selected as sent to the bias control circuit. Valid when bias_cal_done is set to 1.
4:2	cnf_bias_cal	RO	0x0	Bias Calibration configuration value. Indicates the configuration value selected by the bias calibration logic. Valid when bias_cal_done is set to 1.
1	bias_cal_fail	RO	0x0	Bias Calibration failed. Indicates whether bias calibration completed successfully. Valid when bias_cal_done is set to 1. ▪ 0x0 = Bias calibration succeeded ▪ 0x1 = Bias calibration failed
0	bias_cal_done	RO	0x0	Bias Calibration done. Indicates whether bias calibration is running: ▪ 0x0 = Bias calibration is in progress ▪ 0x1 = Bias calibration is completed

4.9 XO Registers

4.9.1 XO_CNFG Register

Crystal oscillator circuit control. Address map for this block of registers: Crystal Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:19	Reserved	RO	0x0	reserved.
18:17	xo_cfg_res	RW	0x0	reserved. Not used.
16	en_ldo_xo	RW	0x1	XO LDO Enable. When set, enables the XO LDO.

Bit Field	Field Name	Type	Default Value	Description
15:14	en_gain	RW	0x1	XO gain boosting control. Selects the number of gain boosting amplifiers enabled during startup. ▪ 0x0 = Gain boosting amplifiers are disabled ▪ 0x1 = One parallel amplifier is enabled ▪ 0x2 = Two parallel amplifiers are enabled ▪ 0x3 = All three parallel amplifiers are enabled
13:8	en_cap_xout	RW	0x1F	XO additional tuning capacitance at XOUT terminal. Controls the internal tuning capacitance applied at the XOUT terminal. The capacitance rises monotonically n steps of 0.5pF from 0pF to 23.5pF as the control setting increases from 0x00 to the maximum of 0x2F. Values 0x30 to 0x3F are reserved.
7:6	Reserved	RW	0x0	reserved.
5:0	en_cap_xin	RW	0x1F	XO additional tuning capacitance at XIN/REF terminal. Controls the internal tuning capacitance applied at the XIN/REF terminal. The capacitance rises monotonically in steps of 0.5pF from 0pF to 23.5pF as the control setting increases from 0x00 to the maximum of 0x2F. Values 0x30 to 0x3F are reserved.

4.10 OUT Registers

4.10.1 OD_CNFG Register

Output Divider control. Address map for this block of registers: Clock Output Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15	en_ldo_od	RW	0x1	Output Divider LDO Enable. When set, enables the corresponding output divider LDO.
14	reserved	RO	0x0	reserved.
13:0	outdiv_ratio	RW	0x69	Output Divider ratio. Output divider ratio. The minimum divide value is 10 (decimal).

4.10.2 ODRV_EN Register

Output driver enable control. Address map for this block of registers: Clock Output Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	reserved.
3:2	out_dis_state	RW	0x0	Output Driver disabled state. Controls the state of OUTx/nOUTx when the output driver is disabled. ▪ 0x0 = Held Low/Low (except LVDS mode is held Low/High) ▪ 0x1 = Held Low/High ▪ 0x2 = Held Hi-Z/Hi-Z ▪ 0x3 = Normal operation (not held static). This is intended for debug purposes only.

Bit Field	Field Name	Type	Default Value	Description
1	out_dis	RW	0x0	Output Driver disable. Forces the Output Driver to be disabled. ▪ 0 = Output Driver is enabled if not disabled by other means ▪ 1 = Output Driver is disabled
0	out_pd	RW	0x0	Output Driver power down. Powers down the Output Driver. When powered down, OUTx/nOUTx are tri-stated and the output enable control is ignored. ▪ 0 = Output Driver is powered up and can be enabled/disabled ▪ 1 = Output Driver is powered down

4.10.3 ODRV_MODE_CNFG Register

Output driver mode control. Address map for this block of registers: Clock Output Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	out_cmos_mode	RW	0x1	Output Driver CMOS mode. Controls how OUTx and nOUTx are driven when CMOS mode is selected. ▪ 0x0 = OUTx, nOUTx are driven with the same phase ▪ 0x1 = OUTx, nOUTx are driven with the opposite phase ▪ 0x2 = Only OUTx is driven. nOUTx is held low. ▪ 0x3 = Only nOUTx is driven. OUTx is held low.
5:4	out_lvds_cm_voltage	RW	0x2	Output Driver LVDS common mode voltage control. Controls the common mode voltage of the output driver when LVDS mode is selected. ▪ 0x0 = 700mV ▪ 0x1 = 800mV ▪ 0x2 = 900mV ▪ 0x3 = 1000mV
3	out_hcsl_term_en	RW	0x1	Output Driver HCSL termination enable. Controls the internal HCSL termination. ▪ 0x0 = Internal HCSL termination is disabled. An external termination resistor to ground is required. ▪ 0x1 = Internal HCSL termination is enabled, providing an internal 50ohm resistor to ground.
2	en_out_bias	RW	0x1	Output Driver Bias Enable. When set, enables the output driver bias circuit.
1:0	out_mode	RW	0x0	Output Driver type. Selects the output driver type. ▪ 0x0 = HCSL ▪ 0x1 = reserved ▪ 0x2 = LVDS ▪ 0x3 = CMOS

4.10.4 ODRV_AMP_CNFG Register

Output driver amplitude control. Address map for this block of registers: Clock Output Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	out_cnf_hcsl_swing	RW	0xB	Output Driver HCSL amplitude control. Controls the amplitude of the output driver when CML mode is selected. Each value provides a 50mV increment. ▪ 0x0 = 200mV ▪ 0x1 = 250mV ▪ 0x2 = 300mV ▪ 0x3 = 350mV ▪ 0x4 = 400mV ▪ 0x5 = 450mV ▪ 0x6 = 500mV ▪ 0x7 = 550mV ▪ 0x8 = 600mV ▪ 0x9 = 650mV ▪ 0xA = 700mV ▪ 0xB = 750mV ▪ 0xC = 800mV ▪ 0xD = 850mV ▪ 0xE = 875mV ▪ 0xF = 900mV
3	out_cnf_lvds_amp	RW	0x0	Output Driver LVDS amplitude control. Controls the amplitude of the output driver when LVDS mode is selected. ▪ 0 = 350mV ▪ 1 = 400mV
2:0	reserved	RW	0x4	reserved.

4.11 REF Registers

4.11.1 PREDIV_CNFG Register

Reference Clock Input Divider control. Address map for this block of registers: Clock Reference Addresses.

Use the Renesas Electronics Timing Commander Software to provide correct settings.

Bit Field	Field Name	Type	Default Value	Description
31:25	reserved	RO	0x0	reserved.
24	ref_priority	RW	0x0	Reference Clock Priority Sets the clock's priority for DPLL reference switching. If multiple clocks are set to the same priority level, they are prioritized from the lowest numbered (clkin0) to the highest numbered (clkin3). ▪ 0x0 = first priority ▪ 0x1 = second priority
23	reserved	RO	0x0	reserved.
22	input_div_setb	RW	0x1	Input Divider Set When cleared, the corresponding input divider gets held in set mode (bit is active low).

Bit Field	Field Name	Type	Default Value	Description
21	enb_input_div	RW	0x0	Input Divider Enable When cleared, enables the corresponding input divider (active low).
20	id_byp_en	RW	0x1	Input Divider Bypass. Allows the input divider to be bypassed and the reference clock input is passed directly to the DPLL and clock monitor. Bypass must be disabled if the reference clock frequency is greater than 33MHz. ▪ 0 = divided reference clock is selected, divide ratio is id_ratio ▪ 1 = reference clock is selected, effective divide ratio is 1
19:0	id_ratio	RW	0x0	Input Divider ratio. Input divider ratio. The reference clock frequency divided by this value must be no more than 33 MHz, and must be equal to the DPLL feedback clock frequency. The minimum divide value is 2. To divide by 1 (when the input reference clock frequency is no more than 33MHz), bypass the divider by setting id_byp_en to 1.

4.12 GPIO Registers

4.12.1 OE_CNFG Register

Configuration control for Output Enable input pin. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	reserved.
5	oe_pd	RW	0x0	OE_nCS Pull-down Enable. Set to 1 to enable the internal pull-down resistor on the OE_nCS pin.
4	oe_pu	RW	0x1	OE_nCS Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the OE_nCS pin.
3	oe_pol	RW	0x0	OE Input Polarity. Controls the active polarity of the OE_nCS input pin when oe_sel is set to 0. ▪ 0x0 = Active high (1 = enable outputs, 0 = disable outputs) ▪ 0x1 = Active low (0 = enable outputs, 1 = disable outputs)
2:1	reserved	RO	0x0	reserved.
0	oe_sel	RW	0x0	OE Select. Selects whether the OE_nCS input pin can control the output enable of the clock output drivers: ▪ 0x0 = The OE_nCS input disables the clock output drivers when de-asserted. This setting is ignored in SPI mode. ▪ 0x1 = The OE_nCS input does not affect the clock output drivers.

4.12.2 IO_CNFG Register

Miscellaneous Input/Output Configuration. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	out_startup	RW	0x0	Output Disable on startup until PLL locks. Controls whether the clock output drivers are disabled until the APLL or DPLL locks during the startup sequence. ▪ 0x0 = Clock output drivers are disabled until APLL lock asserts ▪ 0x1 = Clock output drivers are disabled until DPLL lock asserts ▪ 0x2 = Clock output drivers are not disabled by APLL or DPLL lock status ▪ 0x3 = Reserved
5:4	pp_drv	RW	0x2	Push-Pull Drive Strength ▪ Applies to pads LOCK and SDA_SDIO (for 3-wire SPI only) when configured for push-pull mode. Drive strength increases as this setting increases.
3:2	od_drv	RW	0x3	Open-Drain Drive Strength ▪ Applies to pads LOCK when configured for open-drain mode. Drive strength increases as this setting increases.
1	sda_pu	RW	0x1	SDA Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the SDA_SDIO pin.
0	scl_pu	RW	0x1	SCL Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the SCL_SCLK pin.

4.12.3 LOCK_CNFG Register

Lock output configuration control. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:13	reserved	RO	0x0	reserved.
12	lock_od	RW	0x0	LOCK Open-drain enable. Set to 1 to configure the LOCK pin as an open-drain output. When lock_pol is set to 0, LOCK is driven low when the value to output is 0 and LOCK is open-drain when the value to output is 1. When lock_pol is set to 1, LOCK is driven low when the value to output is 1 and LOCK is open-drain when the value to output is 0.
11	lock_hiz	RW	0x0	LOCK Tristate Enable. Set to 1 to place the LOCK pin in a high-impedance state.
10	lock_pd	RW	0x0	LOCK Pull-down Enable. Set to 1 to enable the internal pull-down resistor on the LOCK pin. This should not be used when lock_od is set to 1.
9	lock_pu	RW	0x1	LOCK Pull-up Enable. Set to 1 to enable the internal pull-up resistor on the LOCK pin. Note that this internal pull-up is weak, so an external pull-up, tied to the V_{DDA} voltage rail is recommended when lock_od is set to 1.

Bit Field	Field Name	Type	Default Value	Description
8	lock_pol	RW	0x0	LOCK Output Polarity. Selects the polarity of the signal driven on the LOCK pin. When set to active high, the true value of the signal is driven. When set to active low, the inverse of the signal is driven. For example, when lock_sel selects APLL lock, and lock_pol is set to active high, LOCK drives high when the APLL is locked, and drives low when the APLL is unlocked. When lock_pol is set to active low, LOCK drives low when the APLL is locked, and drives high when the APLL is unlocked. This setting is ignored when lock_sel is set to 0x1F. ▪ 0x0 = Active high ▪ 0x1 = Active low
7:5	reserved	RO	0x0	reserved.
4:0	lock_sel	RW	0x0	LOCK Output Mode Select. Selects the status/clock to output on the LOCK pin: ▪ 0x0 = APLL lock (apll_lock_sts) ▪ 0x1 = DPLL lock (dpll_lock_sts) ▪ 0x2 = Reference #0 loss-of-signal (LOSMON0 los_sts) ▪ 0x3 = Reference #1 loss-of-signal (LOSMON1 los_sts) ▪ 0x4 = Crystal loss-of-signal (LOSMON2 los_sts) ▪ 0x5 = Reference #0 activity monitor status (ACTMON0 act_sts) ▪ 0x6 = Reference #1 activity monitor status (ACTMON1 act_sts) ▪ 0x7 = Reference #0 ref_invalid status ▪ 0x8 = Reference #1 ref_invalid status ▪ 0x9 = Device Interrupt (device_int_sts and device_int_en) ▪ 0xA = Device ready (startup sequence completed) ▪ 0x1D: Logic low ▪ 0x1E: Logic high ▪ Others: reserved

4.12.4 STARTUP_STS Register

Start-up status. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	bond_id	RO	0x0	Bond ID value. Value of bond id die pad.
6	reserved	RO	0x0	Reserved
5:0	gpio_at_startup	RO	0x0	GPIO startup value. Value of pins latched at startup. bit [0] = LOCK bit [1] = SDA_DSDIO bit [2] = SCL_SCLK bit [3] = OE_nCS bit [4] = Reserved bit [5] = Reserved

4.12.5 GPIO_STS Register

GPIO status. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:2	reserved	RO	0x0	reserved.
1	lock_o	RO	0x0	LOCK Output value. Reflects the value driven on the LOCK pin when lock_sel is set to 0x0 through 0x4. This bit reads as 0 when lock_sel is set to any other value.
0	oe_i	RO	0x0	OE Input value. Reflects the value input on the OE_nCS pin when oe_sel is set to 0. This bit reads as 0 when oe_sel is set to 1.

4.12.6 SCRATCH0 Register

Software Scratch Register 0. Address map for this block of registers: GPIO Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:0	scratch0	RW	0x0	Scratch register. This value can be stored in OTP on a per-configuration basis. It is not used by the device hardware for any purpose. Users can set this to any value.

4.13 SSI Registers

The acronym SSI refers to items that are generic to the Slave Serial Interface in any mode of operation. SPI or I^2C is used for features and functions that are specific to those operating modes.

4.13.1 SPI_CNFG Register

SPI mode configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	reserved	RO	0x0	reserved.
6:5	spi_dummy_size	RW	0x1	SPI dummy read byte count. Number of dummy bytes shifted out before the read data when spi_dummy_en is 1. ▪ 0x0 = reserved ▪ 0x1 = 1 byte ▪ 0x2 = 2 bytes ▪ 0x3 = 3 bytes
4	spi_dummy_en	RW	0x0	SPI dummy read byte enable. Enables insertion of dummy read bytes. ▪ 0x0 = Read data is immediately available (no dummy bytes) ▪ 0x1 = spi_dummy_size number of bytes are shifted out before the read data
3	spi_del_out	RW	0x0	SDO driving edge selection. Selects the clock edge that drives SDO. ▪ 0x0 = SDO is driven on opposite SCLK edge than the sampling edge ▪ 0x1 = SDO is delayed one half cycle of SCLK

Bit Field	Field Name	Type	Default Value	Description
2	reserved	RO	0x0	reserved.
1	spi_clk_sel	RW	0x0	SDI sampling edge selection. Selects the clock edge that samples SDI. ▪ 0x0 = SDI is sampled on rising SCLK edge ▪ 0x1 = SDI is sampled on falling SCLK edge
0	spi_3wire	RW	0x1	Select SPI 3-wire mode. Selects 3-wire or 4-wire mode. ▪ 0x0 = reserved ▪ 0x1 = 3-wire SPI. Data is received and transmitted on SDA_SDIO

4.13.2 I2C_FLTR_CNFG Register

I2C mode configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	reserved.
5:4	i2c_speed	RW	0x0	I2C speed selection. Selects the operating speed of the I2C interface. Only the output driver slew rate is affected by this setting (higher setting means higher drive strength). The I2C master must provide the appropriate SCL frequency and other timing requirements according to the selected speed. ▪ 0x0 = 1.8V Standard mode (100 kHz) or 3.3V Standard (100kHz) and Fast mode (400kHz) ▪ 0x1 = 1.8V Fast mode (400 kHz) ▪ 0x2 = reserved ▪ 0x3 = 1.8V and 3.3V Fast mode plus (1 MHz)
3:0	i2c_spike_fltr	RW	0x1	I2C digital spike filter duration. Controls the duration of the digital spike filters on the SCL and SDA inputs, specified in number of system clock cycles. 0 disables filtering.

4.13.3 I2C_TIMING_CNFG Register

I2C mode timing configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	i2c_sda_high_hold	RW	0x4	I2C/SMBus transmit one bit delay. Delays transmission of 1 value by 8x this number of system clock cycles.
3:0	i2c_sda_low_hold	RW	0x4	I2C/SMBus transmit zero bit delay. Delays transmission of 0 value by8x this number of system clock cycles.

4.13.4 I2C_ADDR_CNFG Register

I^{2}C mode device address configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	reserved	RO	0x0	reserved.
6:0	i2c_addr	RW	0x09	I2C device address. Sets I2C device address that the SSI acknowledges and accepts accesses on. Bits[1:0] are set by OTP only and can be overridden by pins.

4.13.5 SSI_GLOBAL_CNFG Register

Slave Serial Interface Global configuration. Address map for this block of registers: SSI Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:3	reserved	RO	0x0	reserved.
2	ssi_addr_size	RW	0x0	SSI address size. When 0 the SSI expects 1-byte CSR addresses; when 1 the SSI expects 2-byte CSR addresses. Upper address bits are taken from the SSI's page register to create a full 32-bit CSR address. ▪ 0x0 = 1-byte address ▪ 0x1 = 2-byte address
1:0	ssi_enable	RW	0x1	SSI mode. Selects the serial port mode: ▪ 0x0 = SSI is disabled ▪ 0x1 = SSI is in I2C mode ▪ 0x2 = SSI is in SPI mode ▪ 0x3 = Reserved

4.14 APLL Registers

4.14.1 APLL_FB_DIV_FRAC Register

APLL Feedback Divider Fraction Numerator value. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
31:27	reserved	RO	0x0	reserved.
26:0	apll_fb_div_frac	RW	0x0	APLL Feedback Divider Fraction Numerator. APLL feedback divider numerator value. The denominator is a fixed value of 2^{27}. This register is atomic. When the most significant byte (bits [31:24]) is written, the new value is applied to the APLL.

4.14.2 APLL_FB_DIV_INT Register

APLL Feedback Divider Integer value. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	reserved.
9:0	apll_fb_div_int	RW	0x6C	APLL Feedback Divider Integer. APLL feedback divider integer value. This register is atomic. When the most significant byte (bits [15:8]) is written, the new value is applied to the APLL.

4.14.3 APLL_FB_SDM_CNFG Register

APLL Feedback SDM control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:6	reserved	RO	0x0	reserved.
5	apll_fb_dither_en	RW	0x0	APLL Feedback SDM Dither Enable. Dither enable for the SDM controlling the APLL feedback divider. ▪ 0x0 = dither disabled ▪ 0x1 = dither enabled
4	apll_fb_dither_ns	RW	0x0	APLL Feedback SDM Dither Noise shaping. Dither noise shaping enable for the SDM controlling the APLL feedback divider. ▪ 0x0 = dither not shaped ▪ 0x1 = dither shaped
3:2	apll_fb_dither_gain	RW	0x0	APLL Feedback SDM Dither Gain. Gain control for the SDM controlling the APLL feedback divider. ▪ 0x0 = LSB ▪ 0x1 = 2*LSB ▪ 0x2 = 4*LSB ▪ 0x3 = 8*LSB
1:0	apll_fb_sdm_order	RW	0x3	APLL Feedback SDM Order. Selects the order of the SDM controlling the feedback divider for the APLL. ▪ 0x0 = Integer ▪ 0x1 = 1st order ▪ 0x2 = 2nd order ▪ 0x3 = 3rd order

4.14.4 APLL_CNFG Register

APLL Configuration control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
72	reserved	RO	0x0	reserved.
1	apll_ref_sel	RW	0x0	APLL Reference Selection Configuration. ▪ 0x0 = Selects XIN/REF ▪ 0x1 = Selects CLKIN

Bit Field	Field Name	Type	Default Value	Description
0	en_doubler	RW	0x1	Frequency doubler enable. Enables the frequency doubler. ▪ 0 = Disable ▪ 1 = Enable

4.14.5 LPF_CNFG Register

APLL Loop Filter Configuration. Address map for this block of registers: APLL Block Register Offsets.

Use the Renesas Electronics Timing Commander Software to provide optimal setting recommendations for a specific device configuration.

Bit Field	Field Name	Type	Default Value	Description
7	apll_vco_filter_byp	RW	0x0	VCO current source filter bypass. ▪ 0 = Filter active ▪ 1 = Filter bypassed
6:4	cnf_LPF_cp	RW	0x7	Loop filter pole capacitor setting. ▪ 0x0 = 33.3pF ▪ 0x1 = 36pF ▪ 0x2 = 38.7pF ▪ 0x3 = 41.4pF ▪ 0x4 = 44.1pF ▪ 0x5 = 46.8pF ▪ 0x6 = 49.5pF ▪ 0x7 = 52.2pF
3:0	cnf_LPF_res	RW	0x6	Loop filter resistor setting. ▪ 0x0 = 0Ohm ▪ 0x1 = 400Ohm ▪ 0x2 = 800Ohm ▪ 0x3 = 1.2kOhm ▪ 0x4 = 1.6kOhm ▪ 0x5 = 2kOhm ▪ 0x6 = 2.4kOhm ▪ 0x7 = 2.8kOhm ▪ 0x8 = 3.2kOhm ▪ 0x9 = 3.6kOhm ▪ 0xA = 4kOhm ▪ 0xB = 4.4kOhm ▪ 0xC = 4.8kOhm ▪ 0xD = 5.2kOhm ▪ 0xE = 5.6kOhm ▪ 0xF = 6kOhm

4.14.6 LPF_3RD_CNFG Register

APLL Loop Filter 3rd Pole control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	byp_p3	RW	0x0	Bypass 3rd pole. This bit can only be set to 1 when operating with an integer feedback divider. ▪ 0 = 3rd pole active ▪ 1 = 3rd pole bypassed
6:4	cnf_LPF_R3	RW	0x3	Loop filter 3rd pole resistor setting. ▪ 0x0 = 0Ohm ▪ 0x1 = 800Ohm ▪ 0x2 = 1.6kOhm ▪ 0x3 = 2.4kOhm ▪ 0x4 = 3.2kOhm ▪ 0x5 = 4kOhm ▪ 0x6 = 4.8kOhm ▪ 0x7 = 5.6kOhm
3	reserved	RO	0x0	reserved.
2:0	cnf_LPF_C3	RW	0x7	Loop filter 3rd pole capacitor setting. ▪ 0x0 = 2pF ▪ 0x1 = 3pF ▪ 0x2 = 4pF ▪ 0x3 = 5pF ▪ 0x4 = 6pF ▪ 0x5 = 7pF ▪ 0x6 = 8pF ▪ 0x7 = 9pF

4.14.7 APLL_LOCK_CNFG Register

APLL Lock Detector control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	reserved.
9	use_raw_lock	RW	0x0	APLL Lock Status Select to Pin. When set, the raw selected lock (precision or original) is sent to the GPIO status pin (LOCK)
8	apll_precision_lock_en	RW	0x1	APLL Precision Lock Detector Enable. When set, enables the lock detector using the ranges controlled by apll_th_refl and apll_th_refh.
7:6	apll_lock_timer	RW	0x2	APLL Lock Timer. Controls the digital debounce interval for the lock indication for the APLL. This duration is a function of the system clock cycles. ▪ 0x0 = 0us ▪ 0x1 = 570 cycles of the system clock ▪ 0x2 = 5700 cycles of the system clock ▪ 0x3 = 57000 cycles of the system clock.

Bit Field	Field Name	Type	Default Value	Description
5	sel_1time_lock	RW	0x0	One time lock select. Controls whether lock detection occurs once or continuously. ▪ 0x0 = Real-time lock. ▪ 0x1 = One-time lock. When the lock signal asserts, it remains asserted even if the APLL loses lock.
4	lck_detect_cal_byp	RW	0x0	Lock detect during calibration enable. Selects when the lock detector is enabled. ▪ 0x0 = Lock detector is enabled after VCO calibration completes ▪ 0x1 = Lock detector is enabled during and after VCO calibration
3	lck_byp	RW	0x0	Lock detector disable. ▪ 0x0 = Lock detector is enabled according to lck_detect_cal_byp and sel_1time_lock ▪ 0x1 = Lock detector is disabled and the lock signal is asserted
2:0	lck_detect_ref_sel	RW	0x0	Analog Lock Detect RC filter resistor Selects the filter resistor. C=5pF. ▪ 0x0 = 7.5kΩ ▪ 0x1 = 15kΩ ▪ 0x2 = 23kΩ ▪ 0x3 = 30kΩ ▪ 0x4 = 37.5kΩ ▪ 0x5 = 45kΩ ▪ 0x6 = 53kΩ ▪ 0x7 = 60kΩ

4.14.8 APLL_LOCK_THRSH Register

APLL Precision Lock Detector Threshold control. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	apll_th_refh	RW	0x8	APLL Precision Lock High Threshold. Controls the high threshold voltage of the precision lock detector. The threshold is approximately 750mV + 20mV * apll_th_refh. The default is around 900mV.
3:0	apll_th_refl	RW	0x8	APLL Precision Lock Low Threshold. Controls the low threshold voltage of the precision lock detector. The threshold is approximately 50mV + 18mV * apll_th_refl. The default is around 200mV.

4.14.9 VCO_CAL_STS Register

APLL VCO Calibration status. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7	vco_cal_fail	RO	0x0	VCO Calibration failed. Indicates whether VCO calibration completed successfully. Valid when vco_cal_done is set to 1. ▪ 0x0 = VCO calibration succeeded ▪ 0x1 = VCO calibration failed
6	vco_cal_done	RO	0x0	VCO Calibration done. Indicates whether VCO calibration is running: ▪ 0x0 = VCO calibration is in progress ▪ 0x1 = VCO calibration is completed
5:0	vco_cap	RO	0x0	VCO Calibration frequency band. Indicates the frequency band selected by the VCO calibration logic. Valid when vco_cal_done is set to 1.

4.14.10 APLL_STS Register

APLL Lock status. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:3	reserved	RO	0x0	reserved.
2	apll_rail_high_sts	RO	0x0	APLL rail high real-time status. When high, indicates that the APLL is railed high.
1	apll_rail_low_sts	RO	0x0	APLL rail low real-time status. When high, indicates that the APLL is railed low.
0	apll_lock_sts	RO	0x0	APLL lock real-time status. Indicates if the APLL is locked to its reference. ▪ 0x0 = unlocked ▪ 0x1 = locked

4.14.11 APLL_EVENT Register

APLL Event status. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:3	reserved	RO	0x0	reserved.
2	apll_rail_high_evt	RW1C	0x0	APLL Rail High event. Set to 1 when the APLL lock detects a rail high status. When asserted, this bit remains asserted until cleared by a write of 1 to this bit position.
1	apll_rail_low_evt	RW1C	0x0	APLL Rail Low event. Set to 1 when the APLL lock detects a rail low status. When asserted, this bit remains asserted until cleared by a write of 1 to this bit position.
0	apll_lol	RW1C	0x0	APLL Loss-of-lock event. Set to 1 when the APLL lock status transitions from locked to unlocked. When asserted, this bit remains asserted until cleared by a write of 1 to this bit position.

4.14.12 APLL_LOL_CNT Register

APLL Loss-of-Lock Event counter. Address map for this block of registers: APLL Block Register Offsets.

Bit Field	Field Name	Type	Default Value	Description
7:4	reserved	RO	0x0	reserved.
3:0	apll_lol_cnt	RW	0x0	APLL Loss-of-Lock Counter. This counter increments each time the APLL lock status de-asserts, and saturates at 0xF. It is cleared by writing it to 0x0, and can be preset by writing the desired value. Preset can be used either as a debug tool or to cause a threshold alarm to happen sooner because the alarm threshold is not configurable.

4.15 INP Registers

4.15.1 REF_CLK_IN_CNFG Register

Reference Clock Input Pad configuration. Address map for this block of registers: Clock Input Block Register Offsets.

Use the Renesas Electronics Timing Commander Software to provide correct settings.

Bit Field	Field Name	Type	Default Value	Description
15:10	reserved	RO	0x0	reserved.
9	en_LVDS	RW	0x0	Reference Clock LVDS Enable. Enables compatible termination when the reference clock input signal is LVDS. ▪ 0 = LVDS input termination is disabled ▪ 1 = LVDS input termination is enabled
8	en_HCSL	RW	0x0	Reference Clock HCSL Enable. Enables compatible termination when the reference clock input signal is HCSL. ▪ 0 = HCSL input termination is disabled ▪ 1 = HCSL input termination is enabled
7	en_ldo_ib	RW	0x1	Reference Clock Input Pad LDO enable. When set, enables the input buffer LDO.
6	en_selfbias_cmos	RW	0x0	Reference Clock Input Pad internal self-bias enable. When the single-ended reference clock input signal is AC-coupled external to the device, the internal DC bias voltage must be enabled. ▪ 0x0 = Internal self-bias is disabled (input signal is DC-coupled) ▪ 0x1 = Internal self-bias is enabled (input signal is AC-coupled)
5:4	en_term	RW	0x0	Unused. No defined function. Reserved for future use.
3	en_dc_bias	RW	0x0	Reference Clock Input Pad internal DC bias enable. When the differential reference clock input signal is AC-coupled external to the device, the internal DC bias voltage must be enabled. ▪ 0 = Internal DC bias is disabled (input signal is DC-coupled) ▪ 1 = Internal DC bias is enabled (input signal is AC-coupled)

Bit Field	Field Name	Type	Default Value	Description
2	en_inbuff	RW	0x0	Reference Clock Input Pad enable. The reference clock input pad must be enabled in Jitter Attenuator mode and should be left disabled in synthesizer/DCO mode. ▪ 0 = Input pad is disabled ▪ 1 = Input pad is enabled
1	CMOS_Sel	RW	0x0	Reference Clock Input Pad CMOS/differential select. Configures the reference clock input pad for a single-ended CMOS or differential input signal. ▪ 0 = Differential input is selected ▪ 1 = CMOS input is selected
0	P_N_Diff_Sel	RW	0x0	Reference Clock Input Pad PMOS/NMOS select. Configures the reference clock input pad according to the common mode voltage of the provided input signal. ▪ 0 = PMOS input pair is enabled (low common mode voltage) ▪ 1 = NMOS input pair is enabled (higher common mode voltage)

5. Revision History

Revision	Date	Description
1.01	Mar 31, 2023	Updated Example of Programming Process.
1.00	Oct 21, 2022	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.