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RENESAS

Design Manual

CMOS-N5 Series

CMOS Gate Array

Mega Macro Ver. 4.0

Document No. A14759EJ4V0DM00 (4th edition)
Date Published May 2006 NS CP(N)

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

Major Revisions in This Edition

Page	Description
p.15	Modification of **Table 1-2. Number of Pins Necessary for Testing Mega Macro**
p.61	Modification of **3.4 (3) Other timing**
p.69 in previous edition	Deletion of **3.5 (9) All input pins (except test input) and main clock**
p.91	**5.4 (3) Other timing** Addition of minimum value to "CP0 low delay time (to DAKB↑)"
p.95	Modification of **5.5 (6) Mode 2**
pp.103 and 111	Addition of description when related documents cannot be obtained
p.120 to 122	Modification of configuration in **7.2 NA16550A Initialization and Notes on Creating Pattern**
p.120	Addition of Note to **Figure 7-1. Initialization Pattern**
p.122	Addition of **7.2.3 Notes on creating pattern**
p.134	Modification of **7.5 (15) Timing of transmit READY in 16450 mode (DMA mode = 0)** Addition of **7.5 (16) Timing of transmit READY in FIFO mode (DMA mode = 0)** Modification of **7.5 (17) Timing of transmit READY in FIFO mode (DMA mode = 1)**

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

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INTRODUCTION

This manual explains how to design gate arrays using the mega macros (large-scale function blocks) of NEC Electronics' CMOS-N5 Series gate arrays.

Thoroughly read this manual for smooth LSI design.

Be sure to observe the points (general information, cautions, and limitations) described in this manual; otherwise, the quality and performance of the LSI may be degraded and the LSI may malfunction.

Lineup of Mega Macros

Mega Macro Name	Function	General-Purpose Models with Equivalent Functions
NA37A	Programmable DMA controller	μPD71037[Note]
NA51A	Serial control unit	μPD71051[Note]
NA54A	Programmable timer/counter	μPD71054[Note]
NA55A	Parallel interface unit	μPD71055[Note]
NA59A	Interrupt control unit	μPD71059[Note]
NA16550A	UART with FIFO	PC16550D

<R> **Note** Maintenance product

Because the gate placement and routing of each macro are predetermined, the internal timing specification of a macro is the same before and after placement and routing. However, the shape of the macro and the shape of the master, as well as the number of cells of the macro, must be taken into consideration when selecting the master on which the macro is to be mounted because the shape of the occupied cell area is fixed. In particular, when using two or more mega macros and when other hard macros (such as memory macros) are mounted, the combination of the shapes of the macros is complicated and mounting separate macros must be studied. In this case, consult NEC Electronics.

<R> Note that none of the macros listed above can be used in the specifications for power supply voltages of 3.0 V and 3.3 V.

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such. Contact NEC Electronics if the related documents cannot be obtained.

- CMOS-N5 Series Design Manual (A13826E)
- CMOS-N5 Series Block Library (A13872E)
- CMOS-N5 Series Memory Block Library (A14683E)
- CMOS-N5 Series Mega Macro Design Manual (This manual)
- Design For Test User's Manual (A14357E)
- μPD71059 User's Manual (U13042J)[Note]
- μPD71059 Data Sheet (U11932J)[Note]

Note Only Japanese version is available.

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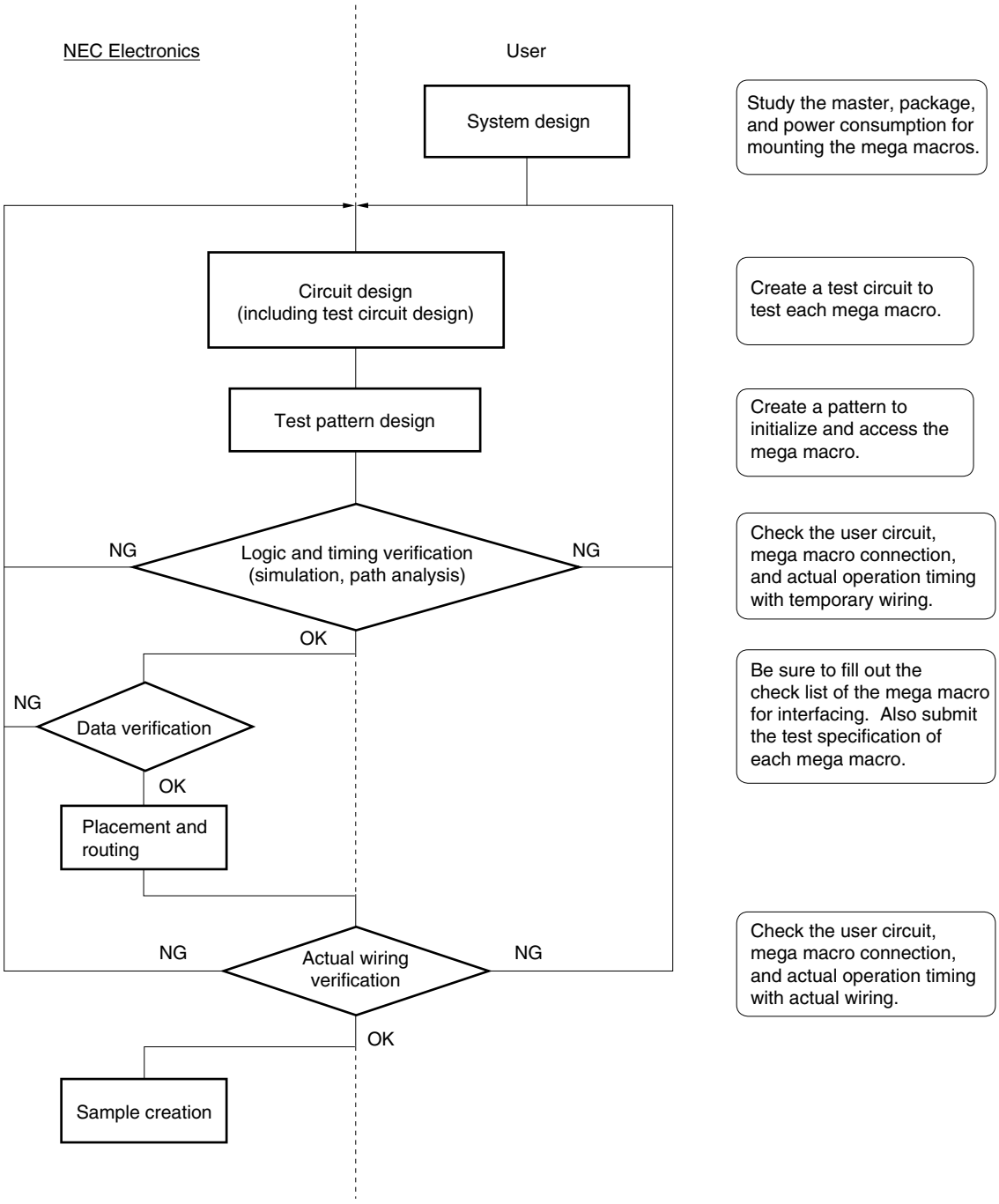
CHAPTER 1 COMMON INFORMATION

This chapter explains the points that always apply when designing a gate array using mega macros. Also refer to the related documents of each series.

1.1 Development Flow

Figure 1-1 Gate Array Development Flow When Mounting Mega Macros shows a development flowchart illustrating how mega macros are mounted on a gate array. The points to be noted when mounting mega macros are explained below.

Figure 1-1. Gate Array Development Flow When Mounting Mega Macros



1.2 System Design

The points to be considered when studying the specifications of the gate array on which mega macros are mounted are described in this section.

1.2.1 Selecting master

Because the shape of a mega macro is determined in advance, some mega macros cannot be used, depending on the master, and the number of cells and shape of the macro. Table 1-1 lists the masters that can be selected when each mega macro is mounted.

When mounting two or more mega macros or memory macros, a separate study is necessary. Consult NEC Electronics.

Table 1-1. Mega Macro Mountable Masters

Master Name	NA37A	NA51A	NA54A	NA55A	NA59A	NA16550A
μPD65880	×	×	×	√	×	×
μPD65881	×	√	×	√	√	×
μPD65882	√	√	√	√	√	√
μPD65883	√	√	√	√	√	√
μPD65884	√	√	√	√	√	√
μPD65885	√	√	√	√	√	√
μPD65887	√	√	√	√	√	√
μPD65889	√	√	√	√	√	√
μPD65890	√	√	√	√	√	√
μPD65893	√	√	√	√	√	√

Remark √: Supported
×: Not supported

1.2.2 Number of pins

To enable NEC Electronics to confirm the operation of a mega macro, the user is requested to create a test circuit. Connect the pins of the test circuit so that the operation of the macro can be monitored from outside the gate array without inverting the logic of a number of pins of the macro and without going through a sequential circuit.

Test pins should therefore be assigned to the gate array. Table 1-2 shows the number of pins necessary for testing each mega macro. Take these values into consideration when studying the number of pins.

Table 1-2. Number of Pins Necessary for Testing Mega Macro

<R>

Mega Macro Name			NA37A	NA51A	NA54A	NA55A	NA59A	NA16550A
Necessary number of test pins	Input	Dedicated[Note 1]	1	1	1	1	1	1
		Multiplexed[Note 2, 4]	27	23	22	41	38	32
	Output	Multiplexed[Note 3, 4]	28	15	11	32	29	20

Notes 1. Be sure to provide a signal for selecting the test mode.

2. When clamping CSE, CSD, and TTHR, the number of pins can be reduced.

3. Be sure to output any pins you do not use.

4. Do not share the test pin of one macro.

1.2.3 Number of test patterns

The test circuit tests each mega macro. The number of patterns necessary for testing each macro is determined as shown in Table 1-3.

The maximum number of test patterns of a gate array is limited by the series. Because the number of test patterns of a mega macro is included in this maximum number, create a test pattern that satisfies the conditions indicated below. Note that the test pattern of each mega macro is prepared by NEC Electronics and used only when delivering the LSI, and is not submitted to the user.

"Maximum number of test patterns for each series"
$\geq \Sigma$ "Number of mega macro test patterns"[Note 1] + Σ "Number of user test patterns"[Note 2]

Notes 1. Including when two or more instances of the same mega macro are mounted
2. Including the initialization pattern of the mega macro

Table 1-3. Number of Test Patterns of Each Mega Macro (Per Macro)

Mega Macro Name	Number of Test Patterns
NA37A	7009
NA51A	12874
NA54A	3479
NA55A	3643
NA59A	7334
NA16550A	14889

1.2.4 Delay time

When roughly estimating the delay time, use the methods described below. To estimate the delay time more accurately, use a simulator or delay analysis tool.

(1) Input timing

Use the fanin of the input pins, the AC characteristics, and the block name of each mega macro to investigate the input timing.

(2) Output timing

Use the fanout of the output pins, the AC characteristics, and the block name of each mega macro to investigate the output timing.

For reference, expressions to estimate delay time are shown below.

<1> Delay time of input buffer and internal function block

$t_{PD} = t_{LD0} + (\Sigma\ F/O + I) \times t_1$ (ns)

<2> Delay time of internal bus

$t_{PD} = t_{LD0} + (\Sigma\ F/O + I + (N - 1) \times 0.96) \times t_1$ (ns)

t_{PD}: Propagation delay time (ns)
t_{LD0}: Basic delay time without load (ns)
F/O: Fanout value
I: Wiring capacitance connected to each output pin
(Refer to the **CMOS-N5 Series Design Manual (A13826E)**).
t_1: Delay coefficient of block output pin
N: Number of 3-state buffers connected to bus

1.2.5 Power consumption

The power consumption of each mega macro is calculated by using the operating frequency or read/write access cycle. The expressions to calculate the power consumption are shown below. These expressions are with V_{DD} = 5 V, T_A = 85°C.

(1) Power consumption of NA37A macro (P37)

Series	Expression
CMOS-N5	P37 = 7.1 × f (mW)

f: Clock frequency (input pin CLK, in MHz)

(2) Power consumption of NA51A macro (P51)

Series	Expression
CMOS-N5	P51 = 3.5 × f (mW)

f: Clock frequency (input pin CLK, in MHz)

(3) Power consumption of NA54A macro (P54)

Series	Expression
CMOS-N5	P54 = 2.0 × (f0 + f1 + f2) (mW)

f0: Counter 0 clock frequency (input pin CLK0, in MHz)

f1: Counter 1 clock frequency (input pin CLK1, in MHz)

f2: Counter 2 clock frequency (input pin CLK2, in MHz)

(4) Power consumption of NA55A macro (P55)

Series	Expression
CMOS-N5	P55 = 2.3 × 1/T (mW)

T: Read/write access cycle (μs)

(5) Power consumption of NA59A macro (P59)

Series	Expression
CMOS-N5	P59 = 3.1 × 1/T (mW)

T: Read/write access cycle (μs)

(6) Power consumption of NA16550A macro (P16550)

Series	Expression
CMOS-N5	P16550 = 11.3 × f (mW)

f: Clock frequency (input pin XIN, in MHz)

1.3 Circuit Design

Keep in mind the following two points when embedding a mega macro in a circuit. Details of circuit design are explained from **1.3.1** onwards.

(1) Processing of output pins of mega macro

A mega macro is provided with 3-state output control signals so that a bus can be configured. Therefore, because there is a possibility that the input signal of a cell may float inside the ASIC, provide a circuit that prevents floating when using 3-state output signals.

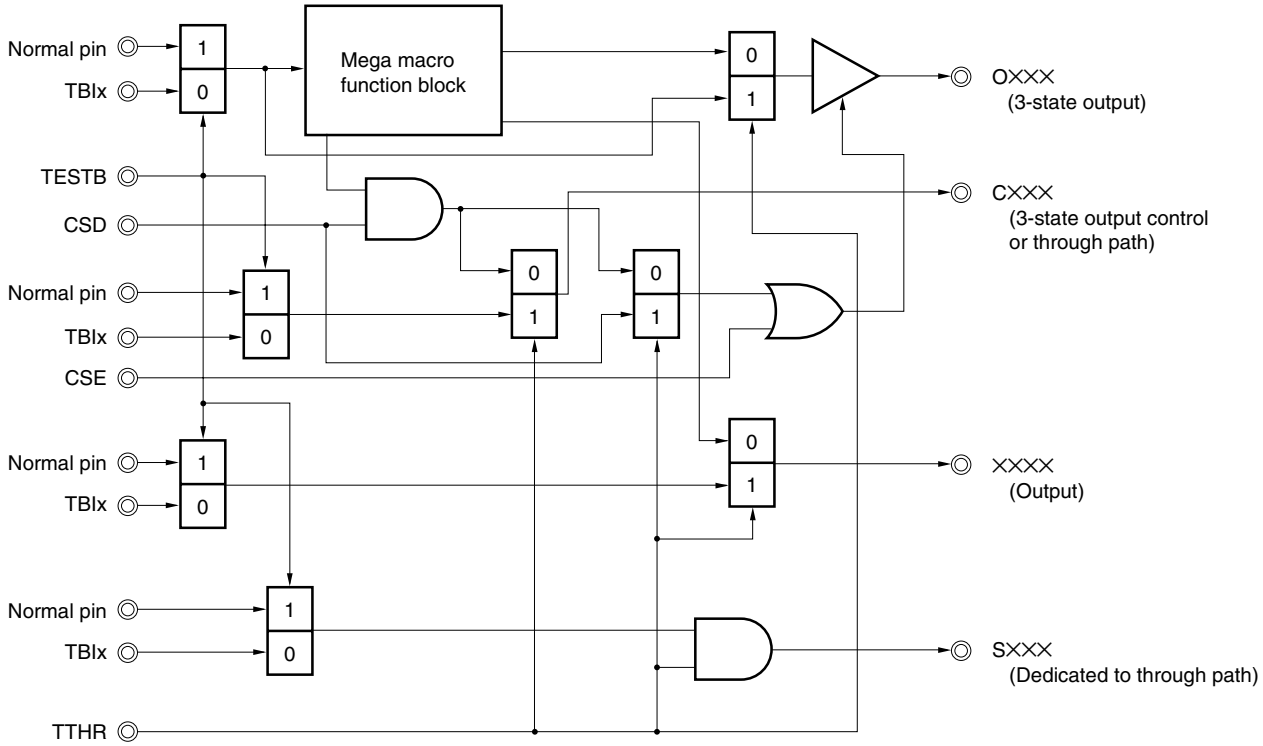
(2) Test circuit for each mega macro

Because the operation of each mega macro is tested using NEC Electronics' test pattern, be sure to design the test circuit so that the operation of each macro can be monitored from the external pins of the gate array without inverting the logic of the test pins of the macro and without going through a sequential circuit. Conduct a through path test if required by your application.

1.3.1 Internal configuration of mega macro

Figure 1-2 shows the internal configuration of the mega macro. The mega macro is provided with an output controller and a test circuit in the block that realizes the functions of the mega macro.

Figure 1-2. Internal Circuit Configuration of Mega Macro



1.3.2 Mode

The mega macro has several modes to facilitate application design and creating circuits. To control these modes, the following pins are provided:

- TESTB: Selects a test mode for each mega macro.
- TTHR: Selects a through path test mode.
- CSE: Forcibly enables the 3-state output pin of the mega macro. Fix the level of this pin by using F091.
- CSD: Controls the 3-state control pin of the mega macro.

(1) Operation mode of mega macro

The operation mode of the mega macro is selected by a combination of the TESTB and TTHR pins. Table 1-4 shows the truth table. Control the 3-state output pin separately.

Table 1-4. Operation Modes of Mega Macro

TTHR	TESTB	Normal Input Pin	Test Input Pin	Mode
0	0	Invalid	Valid	Mega macro test mode
0	1	Valid	Invalid	Normal operation
1	0	Invalid	Valid	Post-macro stage test mode (through path test)
1	1	Valid	Invalid	Pre-macro stage test mode (through path test)

- **Mega macro test mode**

  In this mode, the test input pins of the mega macro become valid and operate normally. The result of the normal operation is output from a function block of the mega macro to the output pins.

- **Normal operation**

  In this mode, the normal input pins of the mega macro become valid and operate normally. The result of the normal operation is output from a function block of the mega macro to the output pins.

- **Post-macro stage test mode (through path test)**

  In this mode, the test input pins of the mega macro become valid. The signals of the corresponding test input pins are output to the output pins as is.

- **Pre-macro stage test mode (through path test)**

  In this mode, the normal pins of the mega macro become valid. The signals of the corresponding normal input pins are output to the output pins as is.

(2) Output control mode of mega macro

Table 1-5. Output Control Truth Table of Mega Macro

TTHR	CSE	CSD	3-State Output Pin[Note 1]	3-State Control Pin	Other Output Pins	Output Pin Dedicated for Through Path[Note 2]
0	0	0	Hi-Z	0	Normal operation	0
0	0	1	Normal operation	Normal operation		
0	1	0	No Hi-Z output	0		
0	1	1		Normal operation		
1	0	0	Hi-Z	Through path	Through path	Through path
1	0	1	Through path			
1	1	×				

Notes 1. Control the output buffer by using the CSD pin when CSE = 0 for the through path test.

2. Some macros do not have a dedicated through path output pin.

Exercise care in controlling the 3-state output pin of the mega macro so that a high impedance is not input to the circuit in the stage succeeding the mega macro. If CSE is fixed to “L” when conducting a through path test, control the control signals so that the bus does not float or fight.

1.3.3 Connecting mega macro and user circuit

(1) Basic rule

<1> Connection to test each mega macro

Basically, externally connect all the output pins, except the test input and 3-state control pins of the mega macro, as the pins of the gate array.

<2> Adjusting fanout

Make sure that the fanout limit is not exceeded when connecting the input and output pins of the mega macro to the user circuit. For the fanin and fanout limits of the mega macro, refer to the description of each macro.

<3> Handling of unused pins

Fix the input pins not used by the mega macro to “H” or “L” level by using F091. The output pins not used by the mega macro are used to test each mega macro; therefore, connect all the pins, except the 3-state control pins, for testing.

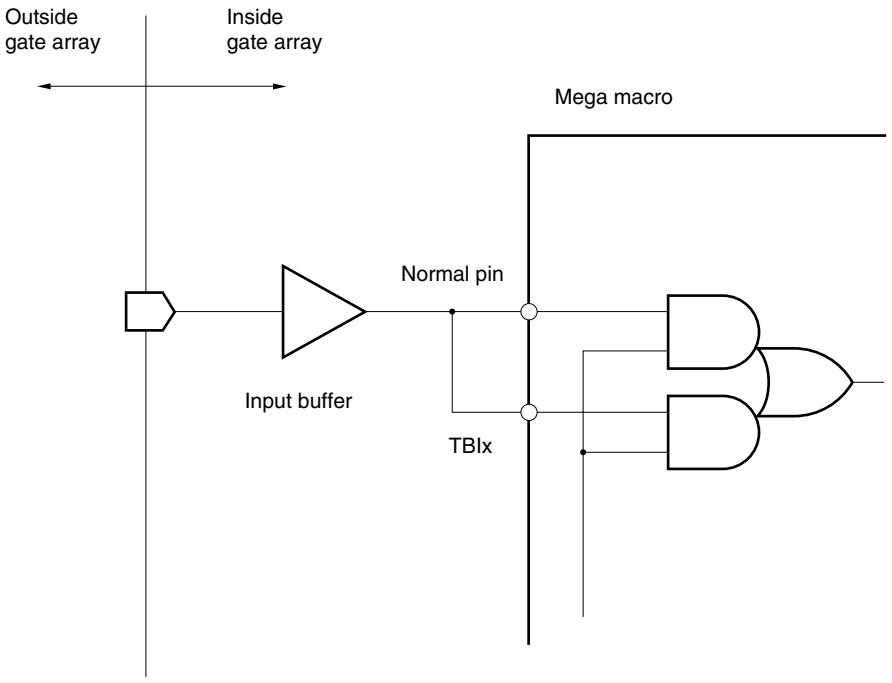
(2) Connection of mega macro and interface block

How to connect the pins of the mega macro to the pins of the gate array via an interface block is explained below.

<1> Input pins

Connect input pins to a normal pin and a test pin via an input buffer (this pin is shared between normal operation and testing each macro).

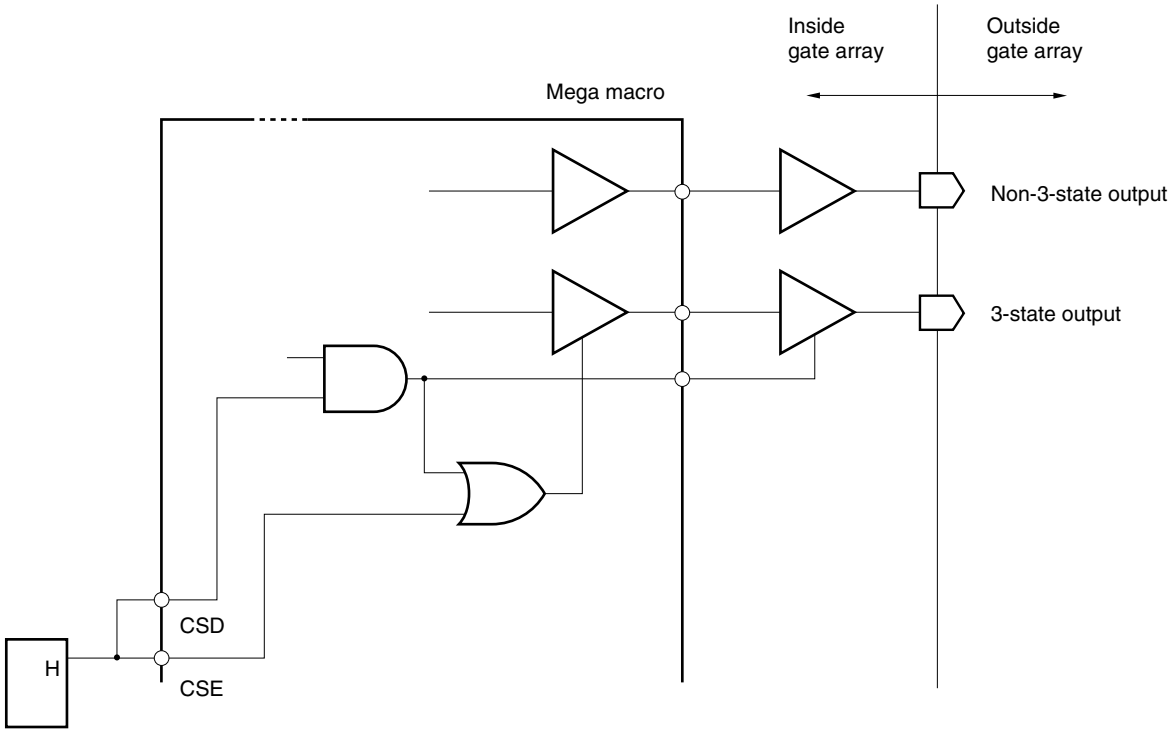
Figure 1-3. Connection with Input Pins



<2> Output pins

Connect the non-3-state output pins of the macro to output pins via an output buffer as is. Connect the 3-state output pins of the macro to the signal input of the 3-state buffer, and connect the 3-state control pins to the control signal input of the 3-state buffer. At this time, control CSE and CSD of the macro to make sure that the signal input of the 3-state buffer does not float.

Figure 1-4. Connection with Output Pins



<3> Bidirectional pins

Although it is possible to connect the input pin or output pin of the mega macro via a bidirectional buffer as a gate array pin, note the following points.

- **When connecting input pin to bidirectional pin**
  Be sure to set the input mode when a single test is conducted.
- **When connecting output pin to bidirectional pin**
  Be sure to set the output mode when a single test is conducted.

(3) Connection of mega macro and function cell

<1> Output and input pins other than 3-state pins

Connect these pins to function cells so that the fanout limitations are satisfied. In doing so, make sure that all the input pins and all the output pins except the 3-state control pins can be monitored from outside the gate array.

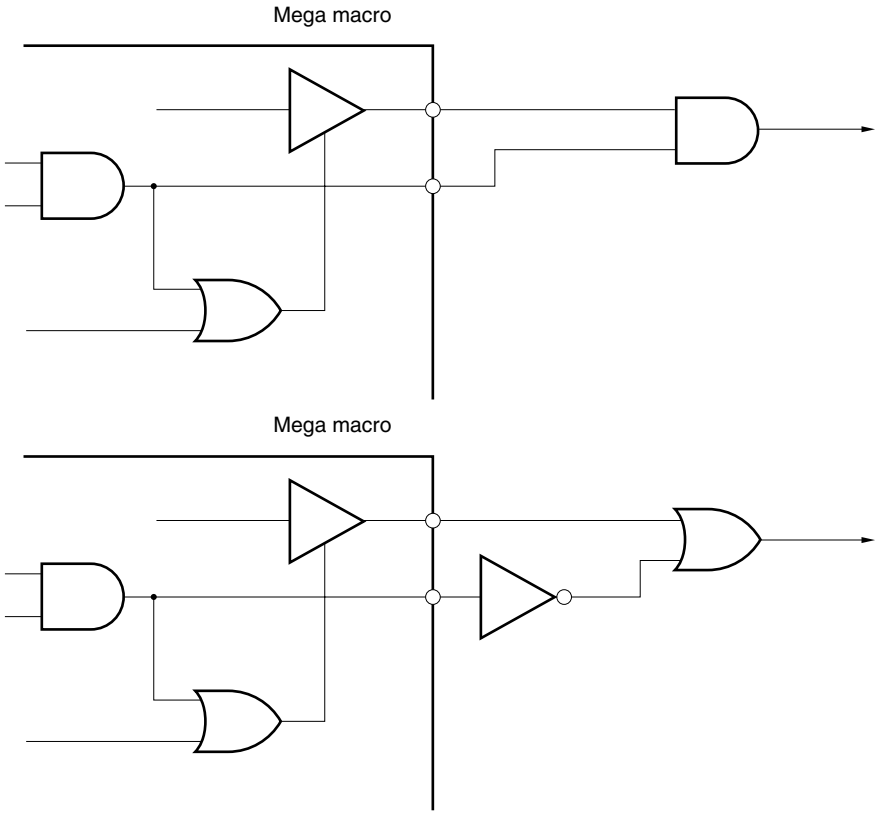
<2> 3-state output pins

Because high impedance may be output to the output pin of the macro, take countermeasures against high impedance in any of the following three ways:

- **By using an AND, NAND, OR, or NOR gate in the next stage**

  Connect an AND, NAND, OR, or NOR gate with three inputs or less, and input signals including the control signals. When making this connection, determine the logic so that the output value of the AND, NAND, OR, or NOR gate is determined regardless of the 3-state output of the macro when the control signal is inactive. Do not use any gate other than those above.

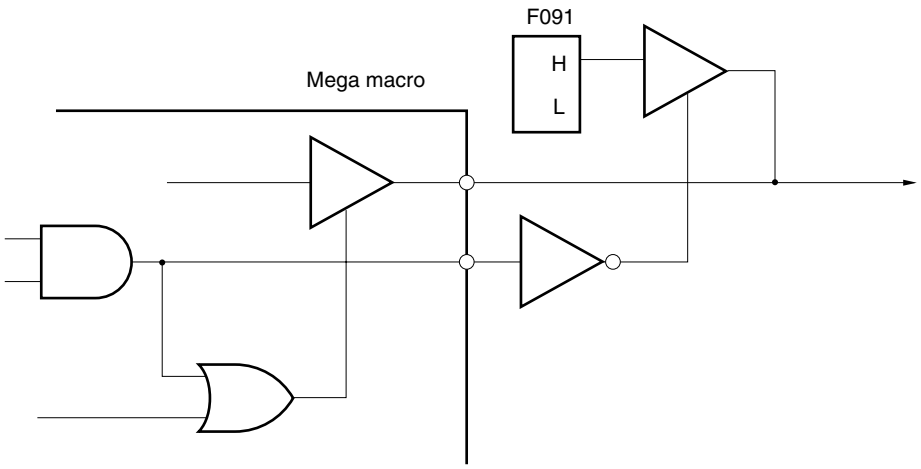
Figure 1-5. Examples of Using AND and OR Gates



- **Configure bus with F091**

  Assert the control signal of the 3-state block connected to F091 active when the 3-state output of the macro is inactive (high-impedance), by using F091 and a 3-state buffer as shown in Figure 1-6.

Figure 1-6. Example of Connecting Bus by Using F091



- **Fix CSE to "H"**

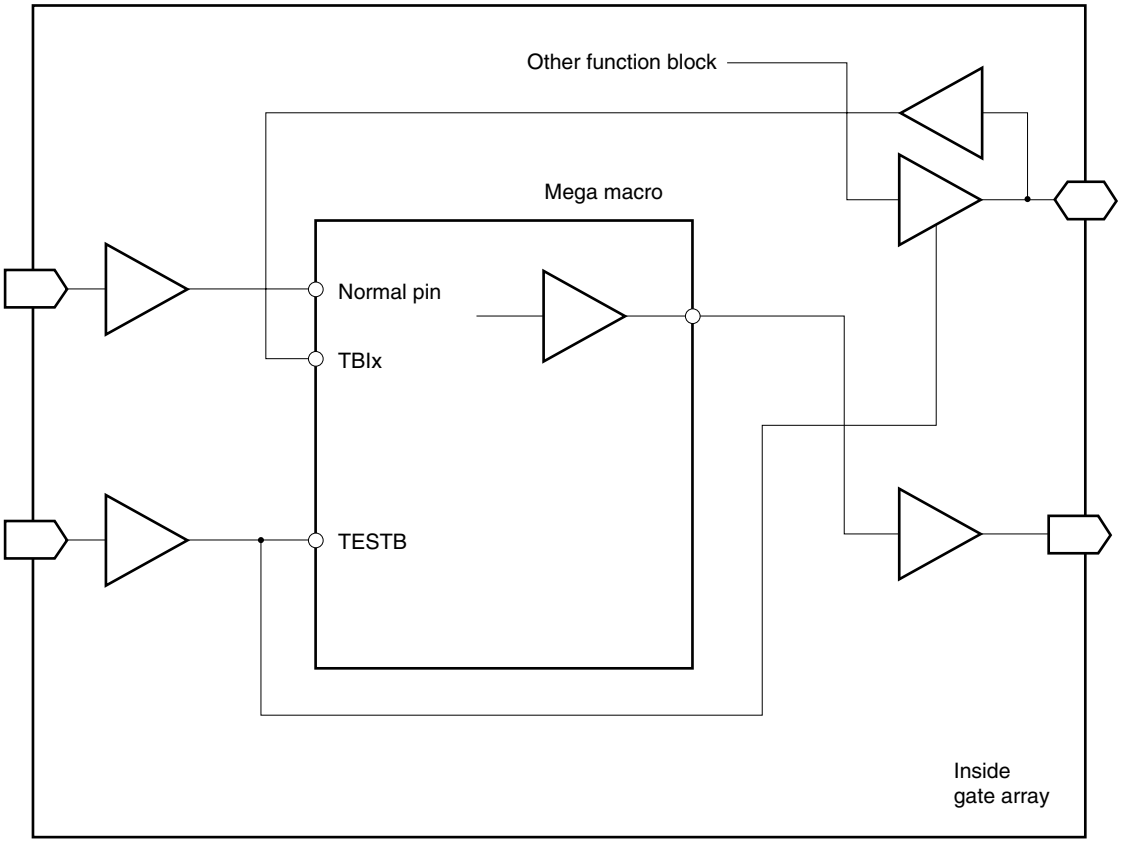
  If CSE is fixed to "H", a high impedance is not output to the output pin of the macro. Therefore, no special countermeasures against high impedance are necessary.

1.3.4 Assigning test signal

Although test pins are assigned to test each mega macro, a test signal and a normal signal are shared in most cases. To share a normal signal and a test signal, bear in mind the following three points:

- When pins are shared in the normal mode and test mode, use the control pins of the interface block so that a test signal can be accurately input or output in the test mode.
- Supply the clock signal of the mega macro from an input pin without sharing the pin with any other output signal, regardless of whether the pin is for normal input or test input.
- Note that normal pins using a GTL interface buffer, N-ch open-drain buffer, or CMOS 5 V withstand voltage output buffer cannot be used as test pins.

Figure 1-7. Example of Sharing Input Pin and Normal Output Pin of Mega Macro



1.3.5 Through path test

A through path test is used to test the user circuit connected to the mega macro. The signals input to the normal pins or test pins are output to the output pin of the macro, bypassing the macro function realization block.

By selecting a normal pin or test pin by using TESTB, the pre-macro-stage circuit and post-macro-stage circuit can be tested. To test the pre-macro-stage circuit, the output signals of the user circuit connected to the input pins of the mega macro are output to an output pin of the macro as is. To test the post-macro-stage, the signals input from the test pins of the mega macro are supplied to the user circuit via the output pins of the macro and tested.

Figure 1-8. Illustration of Normal Operation

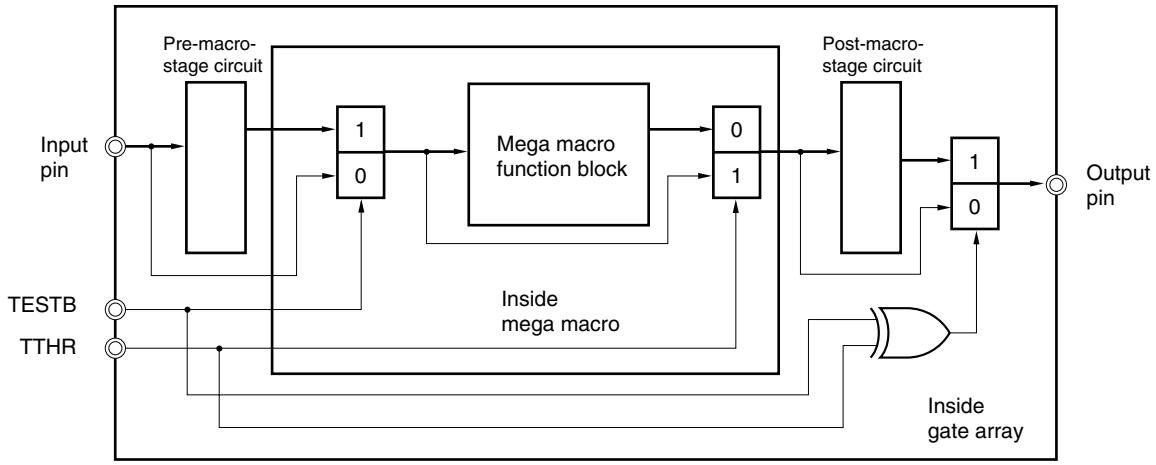


Figure 1-9. Illustration of Testing Each Mega Macro

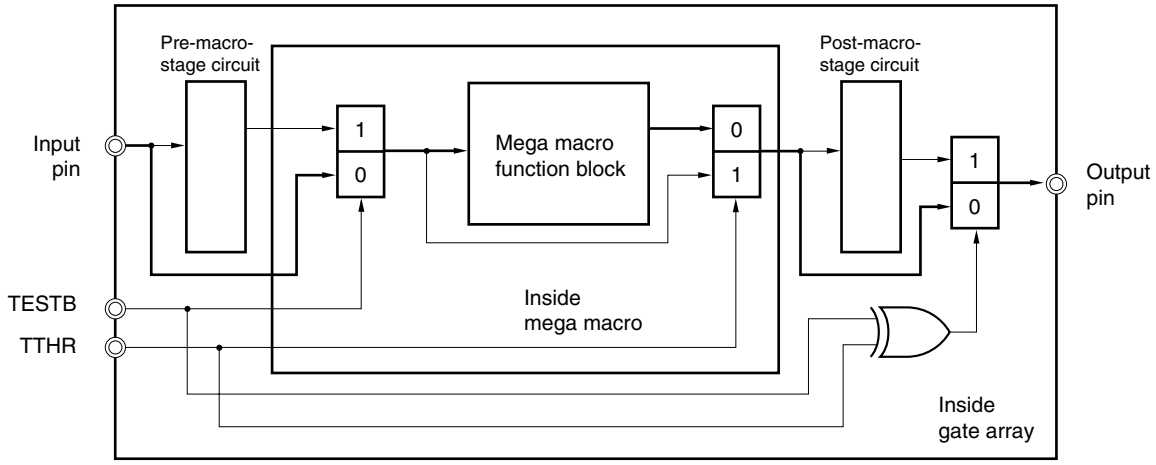


Figure 1-10. Illustration of Testing Pre-Macro-Stage Circuit (Through Path Test)

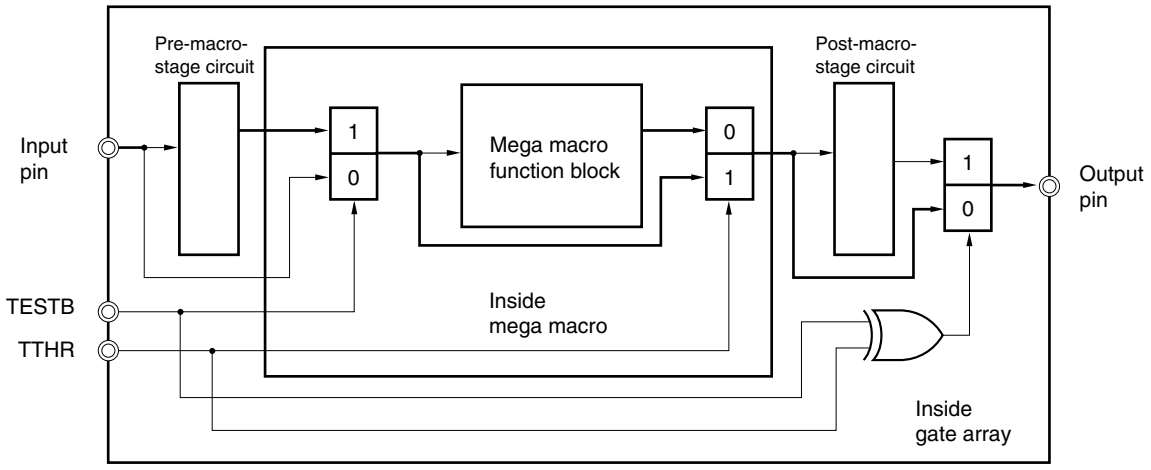
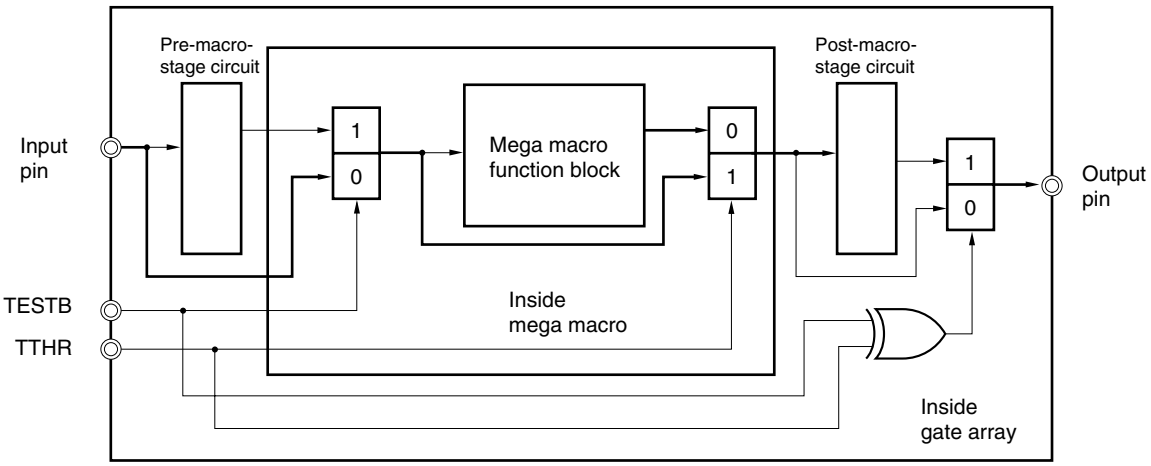


Figure 1-11. Illustration of Testing Post-Macro-Stage Circuit (Through Path Test)



1.3.6 Circuit example

An example of a circuit when mounting multiple mega macros is shown below.

Figure 1-12. Example of Circuit When Mounting Multiple Mega Macros

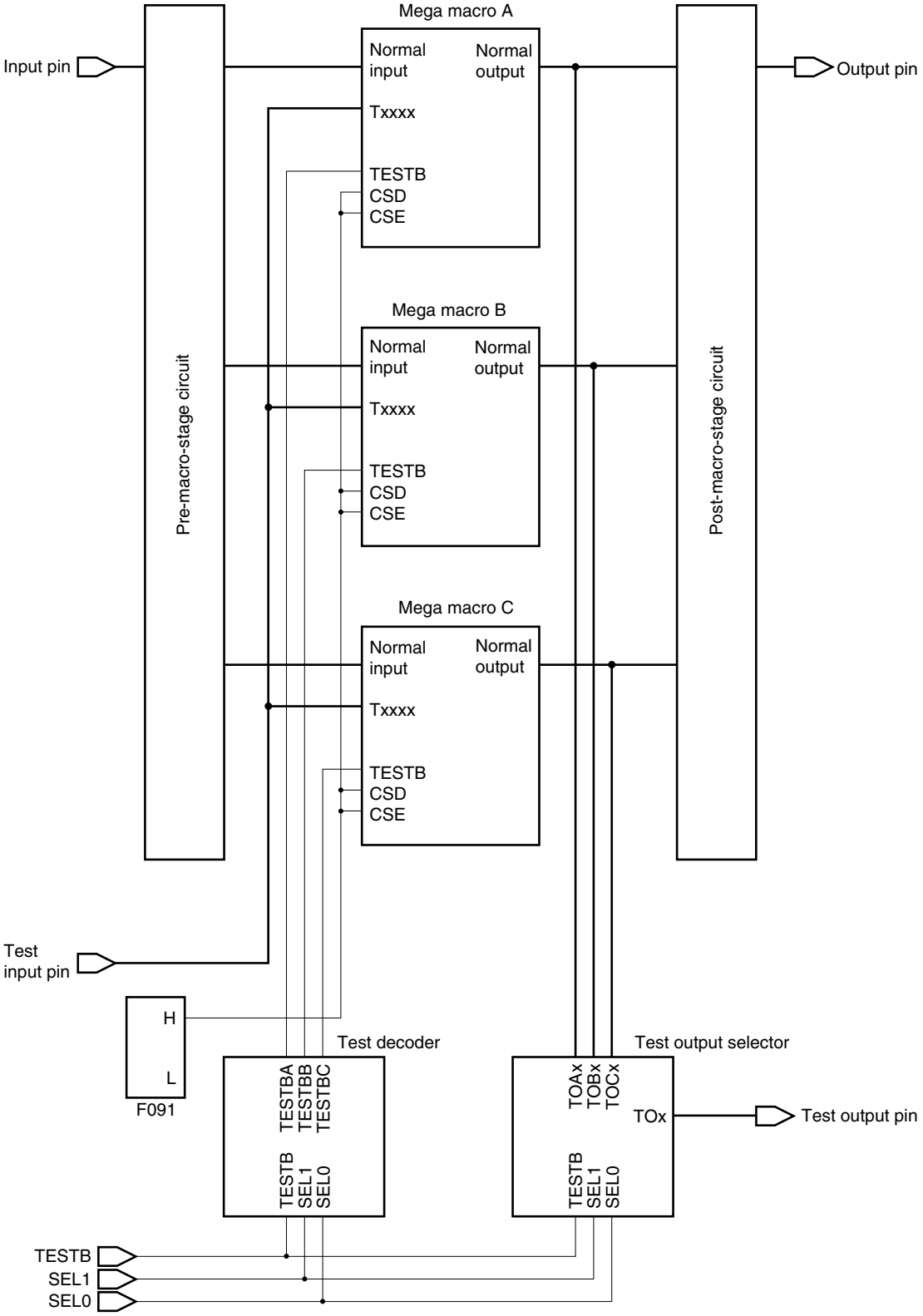


Table 1-6. Test Decoder Truth Table

Input			Output		
TESTB	SEL1	SEL0	TESTBA	TESTBB	TESTBC
1	X	X	1	1	1
0	0	0	0	1	1
0	0	1	1	0	1
0	1	0	1	1	0

X: “0” or “1”

Table 1-7. Test Output Selector Truth Table

Input						Output
TESTB	SEL1	SEL0	TOAx	TOBx	TOCx	TOx
1	X	X	X	X	X	X
0	0	0	TOAx	X	X	TOAx
0	0	1	X	TOBx	X	TOBx
0	1	0	X	X	TOCx	TOCx

X: “0” or “1”

During the mega macro test, create the circuit and initialization pattern so that only TESTB of the targeted mega macro is “0” and TESTB of other mega macros is “1”.

Take care to avoid floating because the mega macro outputs include 3-state outputs.

1.4 Notes on Creating Test Pattern

This section describes notes on creating a test pattern.

1.4.1 Notes on creating a mega macro initialization pattern

Because the internal circuit of the mega macro is not initialized unless an initialization pattern is used, be sure to add an initialization pattern for the mega macro at the beginning of the test pattern. Moreover, because the initialization pattern differs depending on the mega macro, initialize each macro by referring to the corresponding field of each macro.

Initialization may not be performed correctly because of the circuit configuration if a loop circuit exits between the mega macro and other user circuits. Therefore, also initialize any sequential circuit that constitutes a loop.

If the test pattern is divided, provide an initialization pattern for each test pattern.

1.4.2 Notes on creating a mega macro test setting pattern

The following six cautions must be observed to ensure normal operation of mega macro test patterns.

(1) Timing specification is prohibited

Do not specify RZ or modulation of NRZ.

(2) Initialization of a user logic other than a mega macro

Initialize so that a defined value is input to the mega macro normal pin from the user logic.

(3) Input of an undefined value (X) and Hi-Z to the gate array input pin is prohibited

Input a defined value to the gate array input pin.

(4) Expected values from pins other than the mega macro test output pin

Handle expected values from pins other than the mega macro test output pin as “don’t care”.
However, input the expected value to the output of the oscillation block.

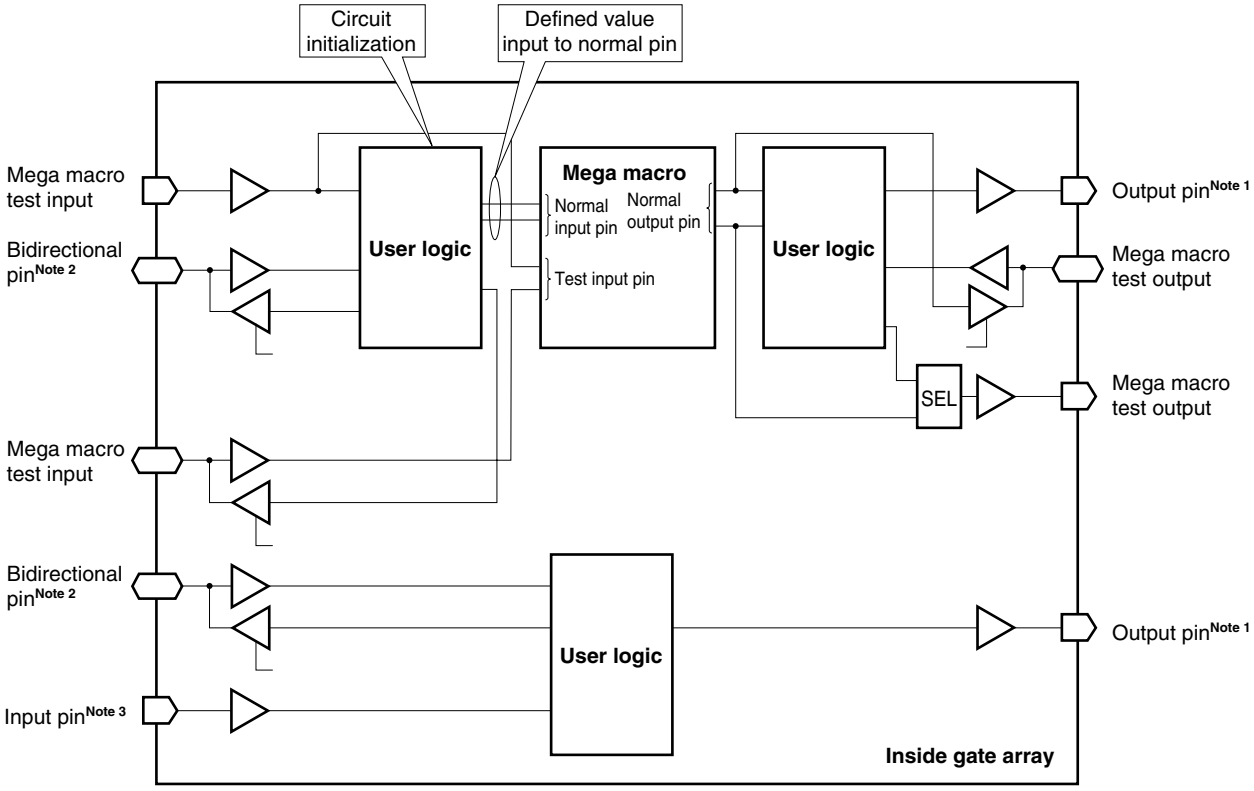
(5) Defining input mode for the input/output buffer

Define the direction of input/output, regardless of the output state of the mega macro test pin.

(6) Dealing with a mega macro that cannot be accessed directly

Settings to ensure that the mega macro is visible from outside the gate array should also be incorporated as a mega macro test setting pattern if the TESTB pin cannot be directly accessed externally or the unit does not have a decoder configuration.

Figure 1-13. Creating a Mega Macro Test Setting Pattern



Notes 1. don't care

2. Define input/output direction
Input: defined value input
Output: don't care

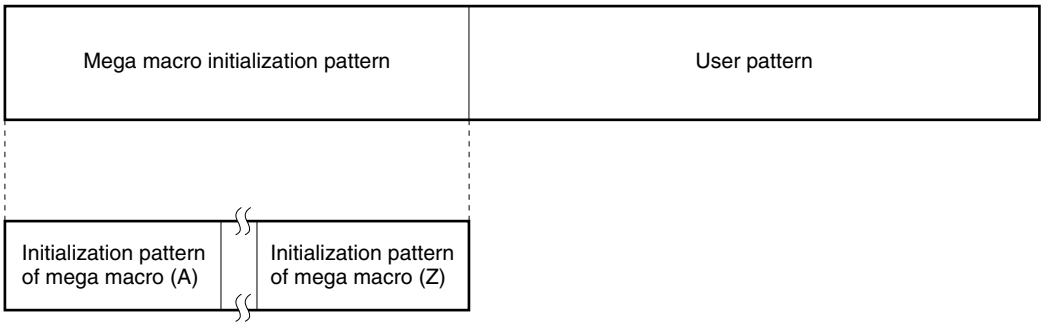
3. Defined value input

1.4.3 Limit of maximum number of test patterns

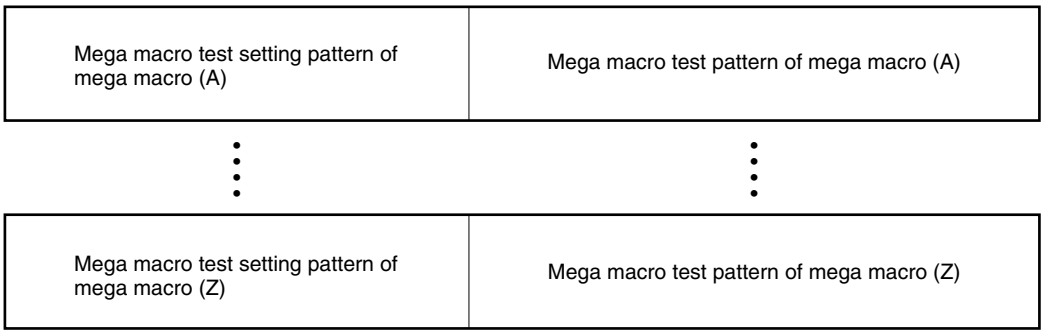
A test pattern is configured as shown in Figure 1-14. Make sure that the total number of these patterns does not exceed the maximum number of test patterns determined for each series.

Figure 1-14. Breakdown of Test Pattern

(a) Mega macro initialization pattern and user pattern



(b) Mega macro test setting pattern and mega macro test pattern



Remark Indicates configuration when multiple (A) to (Z) mega macros are used.

(1) Mega macro initialization pattern

Create a pattern for each mega macro mounted.

(2) User pattern

This is a test pattern for the circuit created by the user. Change the levels of all the I/O pins related to the functions used by the mega macro from “0” to “1” or from “1” to “0”.

(3) Mega macro test setting pattern

Create a pattern for each mega macro mounted.

(4) Mega macro test pattern

This pattern is used by NEC Electronics for delivery inspection and does not have to be created by the user. The test pattern length basically differs depending on the types of and the total number of macros used. For details, refer to **Table 1-3 Number of Test Patterns of Each Mega Macro (Per Macro)**.

1.4.4 Notes on clock input

Supply a clock signal[Note] from an input pin, not a bidirectional pin, regardless of whether the pin is a normal pin or test pin.

Note The “clock signal” means the signal described as “clock” in the Function column in **2.1**, **3.1**, **4.1**, and **5.1**.

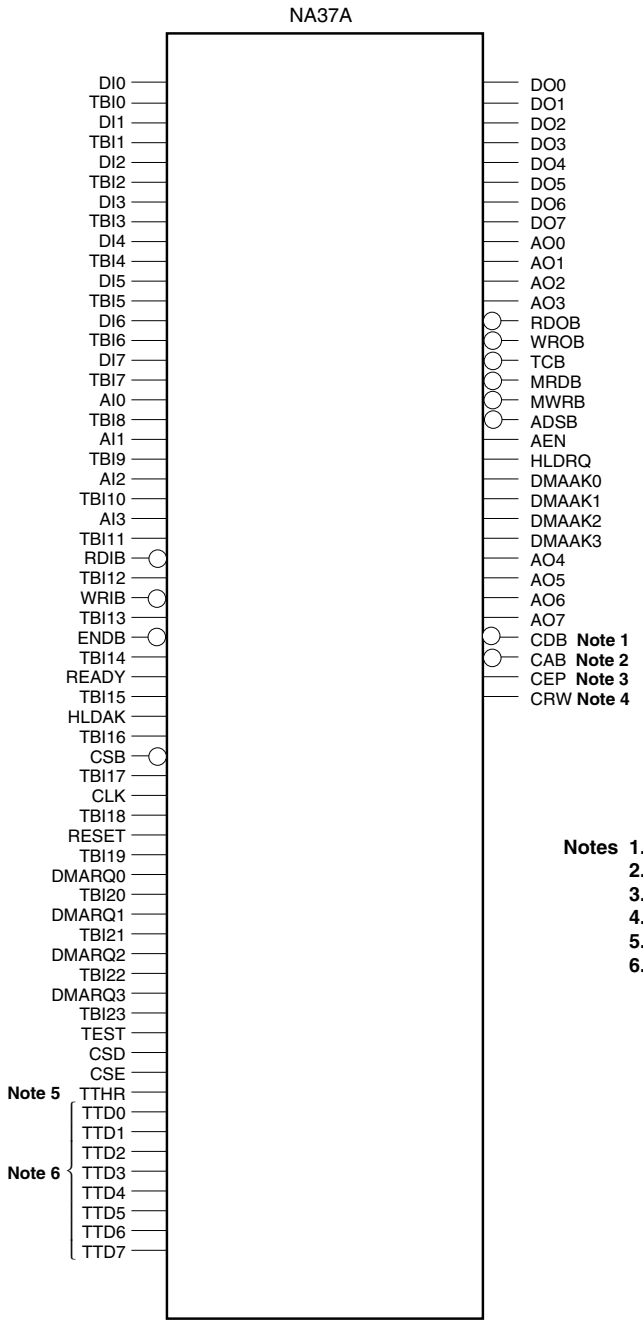
1.5 Other Points to Be Noted

(1) Each mega macro and its equivalent general-purpose product may partly differ from each other in terms of functions. Refer to the description of each mega macro.
(2) Note that an unexpected timing error may occur inside the mega macro when simulation is executed in the through path mode.
(3) For interfacing, create a mega macro test specification and submit it to NEC Electronics by referring to **A.1 Mega Macro Test Specification**.

CHAPTER 2 NA37A MACRO

This chapter explains the functions of the NA37A.

Block Type	Function
NA37A	Programmable DMA Controller



Features

- Compatible function with μPD71037
- Maximum operating frequency: 20 MHz

Caution

- Do not input spike to RDIB, WRIB, ENDB, CLK, and RESET.

Notes 1. Output control signal of DO7 to DO0
2. Output control signal of AO3 to AO0 and AO7 to AO4
3. Output control signal of TCB
4. Output control signal of RDOB, WROB, MRDB, and MWRB.
5. Through path/normal mode select pin
6. Through path dedicated input pin

Remark The input signal pins with “TBI” prefixed are test pins.

Number of cells used (configuration)	5460 (140 × 39)
Mega macro test pattern length	7009

2.1 NA37A Pins

Pin Name	I/O	Function	Test Pin	Fanin/ Fanout	Block Name
DI0	Input	Data bus input signal (LSB)	TBI0	1.5	L424
DI1	Input	Data bus input signal	TBI1	2.1	L424
DI2	Input	Data bus input signal	TBI2	2.2	L424
DI3	Input	Data bus input signal	TBI3	2.9	L424
DI4	Input	Data bus input signal	TBI4	2.1	L424
DI5	Input	Data bus input signal	TBI5	1.0	L424
DI6	Input	Data bus input signal	TBI6	1.6	L424
DI7	Input	Data bus input signal (MSB)	TBI7	2.9	L424
AI0	Input	Internal register address signal (LSB)	TBI8	1.4	L424
AI1	Input	Internal register address signal	TBI9	1.7	L424
AI2	Input	Internal register address signal	TBI10	1.4	L424
AI3	Input	Internal register address signal (MSB)	TBI11	1.2	L424
RDIB	Input	Internal register read signal	TBI12	1.5	L424
WRIB	Input	Internal register write signal	TBI13	1.2	L424
ENDB	Input	External End of Process signal	TBI14	1.3	L424
READY	Input	Memory read/write extended signal (WAIT cycle)	TBI15	1.8	L424
HLDAK	Input	Hold acknowledge signal from CPU	TBI16	1.7	L424
CSB	Input	Chip select signal	TBI17	1.6	L424
CLK	Input	System clock signal	TBI18	1.3	L424
RESET	Input	System reset signal	TBI19	2.7	L424
DMARQ0	Input	DMA request 0 for channel signal from peripheral circuit	TBI20	2.6	L424
DMARQ1	Input	DMA request 1 for channel signal from peripheral circuit	TBI21	2.2	L424
DMARQ2	Input	DMA request 2 for channel signal from peripheral circuit	TBI22	1.0	L424
DMARQ3	Input	DMA request 3 for channel signal from peripheral circuit	TBI23	2.3	L424
TEST	Input	Test/normal mode selection “H”: Normal mode “L”: Test mode	–	2.4	L101
CSD	Input	3-state output control “H”: No Hi-Z output “L”: Hi-Z output	–	1.3	F112
CSE	Input	3-state output control “H”: No Hi-Z output “L”: Hi-Z output	–	2.0	L111
TTHR	Input	Through path/normal mode select signal “H”: Through path mode “L”: Normal mode	–	4.3	F111
TTD0	Input	Through path dedicated input signal	–	1.8	L101
TTD1	Input	Through path dedicated input signal	–	2.3	L101

Pin Name	I/O	Function	Test Pin	Fanin/ Fanout	Block Name
TTD2	Input	Through path dedicated input signal	–	2.7	L101
TTD3	Input	Through path dedicated input signal	–	1.4	L101
TTD4	Input	Through path dedicated input signal	–	4.2	L424
TTD5	Input	Through path dedicated input signal	–	1.9	L424
TTD6	Input	Through path dedicated input signal	–	1.8	L424
TTD7	Input	Through path dedicated input signal	–	1.3	L424
DO0	Output	Data bus output signal (LSB)	–	31.0	F531
DO1	Output	Data bus output signal	–	30.0	F531
DO2	Output	Data bus output signal	–	31.0	F531
DO3	Output	Data bus output signal	–	29.0	F531
DO4	Output	Data bus output signal	–	30.0	F531
DO5	Output	Data bus output signal	–	31.0	F531
DO6	Output	Data bus output signal	–	30.0	F531
DO7	Output	Data bus output signal (MSB)	–	31.0	F531
AO0	Output	Address output signal (LSB)	–	27.0	F531
AO1	Output	Address output signal	–	27.0	F531
AO2	Output	Address output signal	–	26.0	F531
AO3	Output	Address output signal	–	27.0	F531
RDOB	Output	Peripheral circuit read signal	–	28.0	F531
WROB	Output	Peripheral circuit write signal	–	26.0	F531
TCB	Output	Internal End of Process signal	–	26.0	F531
MRDB	Output	Memory read signal	–	27.0	F531
MWRB	Output	Memory write signal	–	28.0	F531
ADSB	Output	Higher address strobe signal	–	30.0	L111
AEN	Output	Address enable signal	–	34.0	L101
HLDRQ	Output	Hold request signal	–	30.0	L111
DMAAK0	Output	DMA acknowledge 0 for channel to peripheral circuit	–	30.0	F111
DMAAK1	Output	DMA acknowledge 1 for channel to peripheral circuit	–	31.0	F111
DMAAK2	Output	DMA acknowledge 2 for channel to peripheral circuit	–	30.0	F111
DMAAK3	Output	DMA acknowledge 3 for channel to peripheral circuit	–	30.0	F111
AO4	Output	Address output signal	–	26.0	F531
AO5	Output	Address output signal	–	27.0	F531
AO6	Output	Address output signal	–	27.0	F531
AO7	Output	Address output signal (MSB)	–	26.0	F531
CDB	Output	Data bus control output signal “H”: No Hi-Z output “L”: Hi-Z output	–	31.0	L101

Pin Name	I/O	Function	Test Pin	Fanin/ Fanout	Block Name
CAB	Output	Address bus control output signal “H”: No Hi-Z output “L”: Hi-Z output	–	30.0	L101
CEP	Output	EOP control output siganl “H”: No Hi-Z output “L”: Hi-Z output	–	26.0	L101
CRW	Output	Read/write control signal “H”: No Hi-Z output “L”: Hi-Z output	–	29.0	L101
TBI0	Input	Test input	–	1.3	L424
TBI1	Input	Test input	–	2.1	L424
TBI2	Input	Test input	–	2.3	L424
TBI3	Input	Test input	–	3.0	L424
TBI4	Input	Test input	–	2.3	L424
TBI5	Input	Test input	–	1.1	L424
TBI6	Input	Test input	–	1.7	L424
TBI7	Input	Test input	–	2.9	L424
TBI8	Input	Test input	–	1.5	L424
TBI9	Input	Test input	–	1.9	L424
TBI10	Input	Test input	–	1.5	L424
TBI11	Input	Test input	–	1.3	L424
TBI12	Input	Test input	–	1.6	L424
TBI13	Input	Test input	–	1.3	L424
TBI14	Input	Test input	–	1.3	L424
TBI15	Input	Test input	–	1.9	L424
TBI16	Input	Test input	–	1.8	L424
TBI17	Input	Test input	–	1.5	L424
TBI18	Input	Test input	–	1.3	L424
TBI19	Input	Test input	–	1.8	L424
TBI20	Input	Test input	–	2.6	L424
TBI21	Input	Test input	–	2.3	L424
TBI22	Input	Test input	–	1.1	L424
TBI23	Input	Test input	–	2.4	L424

Remark Input: Input pin
Output: Output pin

Remarks 1. Txxx is a test input pin. A signal can be input from Txxx by making the TEST input low. Connect pins so that signals can be directly input to the mega macro from outside the gate array in test mode. "Directly" here means a circuit configuration where the input signal is not inverted or no sequential circuit such as a flip-flop is inserted between the pins.

TEST	Input Pin
1	I x x x[Note]
0	T x x x

Note Input a defined value of 0 or 1 to the test input pins in normal mode (it does not matter if 0 and 1 are mixed).

2. Functions of CSE input and CSD input

CSE input: Turns on (high or low level) all the 3-state outputs when "1" is input to this pin.

CSD input: Turns off (high-impedance: Hi-Z) of all the 3-state outputs when "0" is input to this pin while CSE = "0".

When "1" is input, the 3-state outputs are turned on/off by an internal control signal of the mega macro (normal operation).

CSE	CSD	Status of Output Pin	Status of 3-State Output Pin
0	0	Normal operation	Hi-Z
0	1	Normal operation	Normal operation
1	–	Normal operation	No Hi-Z output

3. When CSE = "0", the Hi-Z status of the 3-state output buffer can be checked by monitoring the output value of the corresponding output control signal.

"Hi-Z" Pin	Corresponding Output Control Signal and Output	
DO7 to DO0	CDB	0
AO3 to AO0, AO7 to AO4	CAB	0
TCB	CEP	0
RDOB WROB MRDB MWRB	CRW	0

When CSE = "1", the status of the buffer is not affected by the 3-state output control signal (the 3-state output does not go into a "Hi-Z" state).

4. CSE and CSD can be fixed by clamping. Fix CSD to 1 when clamping it.

Remarks 5. Operating status of output pin depending on combination of TTHR, CSE, and CSD

TTHR Pin	CSE Pin	CSD Pin	3-State Output Pin	3-State Control Pin	Other Pins
0	0	0	Hi-Z	0	Normal operation
		1	Normal operation	Normal operation	
	1	0	No Hi-Z output	0	
		1		Normal operation	
1	0	0	Hi-Z	Through path	Through path
		1	Through path		
	1	×			

6. I/O pin correspondence table in through path test

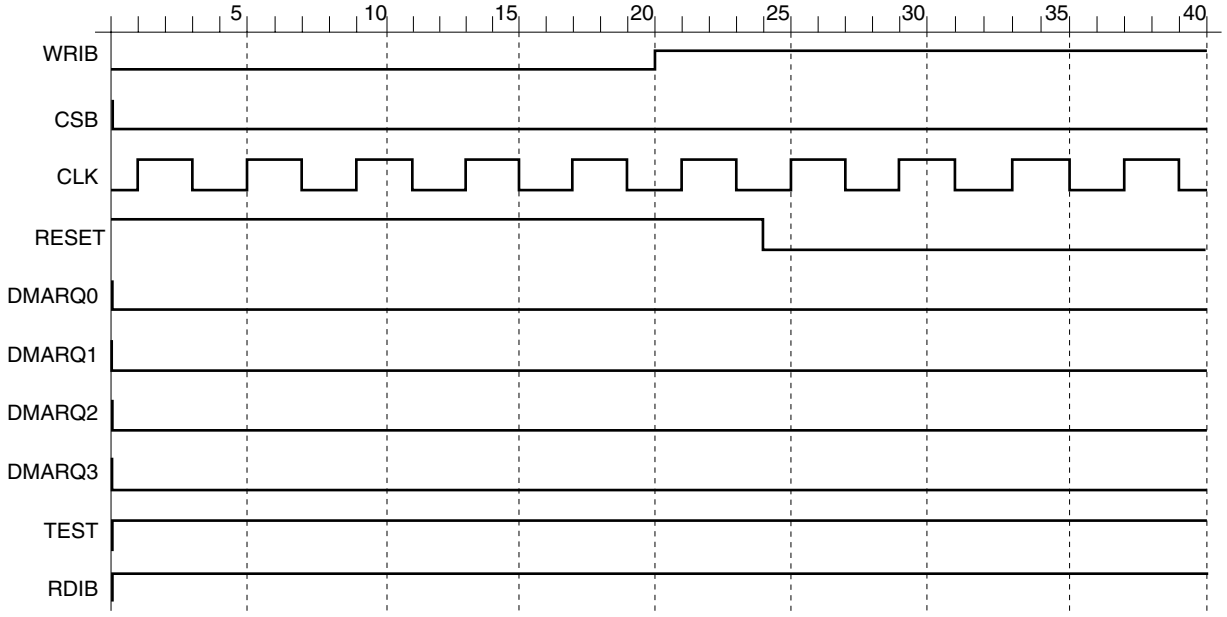
The input pins corresponding to the mega macro output pins when TTHR = “1” are as follows:

Output Pin	Through Path Corresponding Pin		Output Pin	Through Path Corresponding Pin		Output Pin	Through Path Corresponding Pin	
	TEST = 1	TEST = 0		TEST = 1	TEST = 0		TEST = 1	TEST = 0
DO0	DI0	TBI0	AO3	AI3	TBI11	DMAAK2	DMARQ2	TBI22
DO1	DI1	TBI1	RDOB	RDIB	TBI12	DMAAK3	DMARQ3	TBI23
DO2	DI2	TBI2	WROB	WRIB	TBI13	AO4	TTD0	
DO3	DI3	TBI3	TCB	ENDB	TBI14	AO5	TTD1	
DO4	DI4	TBI4	MRDB	READY	TBI15	AO6	TTD2	
DO5	DI5	TBI5	WMRB	HLDAK	TBI16	AO7	TTD3	
DO6	DI6	TBI6	ADSB	CSB	TBI17	CDB	TTD4	
DO7	DI7	TBI7	AEN	CLK	TBI18	CAB	TTD5	
AO0	AI0	TBI8	HLDRQ	RESET	TBI19	CEP	TTD6	
AO1	AI1	TBI9	DMAAK0	DMARQ0	TBI20	CRW	TTD7	
AO2	AI2	TBI10	DMAAK1	DMARQ1	TBI21			

When TTHR = “1” and CSE = “0”, all the 3-state pins are controlled by CSD (selection between through path and high impedance).

2.2 NA37A Initialization Pattern

The internal status of the mega macro is undefined on starting simulation. Therefore, input the following initialization pattern to determine the internal status when executing simulation.



Input “0” or “1” to the other input pins (normal input and test input).
Exercise care that “X” is not input.

- **Value of mega macro output pin after initialization pattern**

Output Pin	Status
DO7 to DO0	Hi-Z
AO3 to AO0	Hi-Z
RDOB	Hi-Z
WROB	Hi-Z
TCB	Hi-Z
MRDB	Hi-Z
MWRB	Hi-Z
ADSB	0
AEN	0
HLDRQ	0
DMAAK3 to DMAAK0	1
AO7 to AO4	Hi-Z
CDB	0
CAB	0
CEP	0
CRW	0

- **Value of internal register after initialization pattern**

Register Name	Register Value
Base address register	Undefined
Base word count register	Undefined
Current address register	Undefined
Current word count register	Undefined
Temporary address register	Undefined
Temporary word count register	Undefined
Status register	All 0
Command register	All 0
Temporary register	Undefined
Mode register	Undefined
Mask register	All channel set mask
Request register	All channel reset mask
First/last flip-flop	0

Cautions 1. DMA cannot be executed when the status of the base/count address register, base/current word count register, and mode register is undefined after the initialization pattern. Write valid values to the respective registers and then start DMA.

2. Configure the following input pins in a circuit that avoids spike input:
RDIB, WRIB, ENDB, CLK, and RESET

2.3 Delay Time

Refer to **1.2.4 Delay time**.

2.4 AC Characteristics (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

(1) DMA mode

(1/2)

Parameter	Symbol	MIN.	MAX.	Unit
AEN↑ delay time (to CLK↓ (S1))	t_{DAEH}		8	ns
AEN↓ delay time (to CLK↓ (SI))	t_{DAEL}		8	ns
Address lower byte float delay time (from CLK↑)	t_{FA}		8	ns
READ/WRITE float time (from CLK↑)	t_{FC}		8	ns
Address higher byte float delay time (from CLK↑)	t_{FD}		15	ns
Address lower byte hold time (from READ↑)	t_{HRA}	t_{CY} – 1		ns
Address higher byte hold time (from ADSB↓)	t_{HSTA}	5		ns
Address lower byte hold time (from WRITE↑)	t_{HWA}	t_{CY} – 1		ns
DACK valid delay time (to CLK↓)	t_{DKLDA}		10	ns
TCB↑ delay time (to CLK↑)	t_{DTCH}		3	ns
TCB↓ delay time (to CLK↑)	t_{DTCL}		8	ns
Address lower byte output delay time (to CLK↑)	t_{DA}		15	ns
Address higher byte setting time (to ADSTB↓)	t_{SAT}	t_{CY} – 5		ns
CLK↑ time	t_{KKH}	12.5		ns
CLK↓ time	t_{KKL}	12.5		ns
CLK cycle time	t_{CYK}	30		ns
READ/WRITE↓ delay time(to CLK↑)	t_{DCL}		5	ns
READ↑ delay time (to CLK↑ (S4))	t_{DKRH}		5	ns
WRITE↑ delay time (to CLK↑ (S4))	t_{DKWH}		5	ns
HRQ valid delay time (to CLK↑)	t_{DHQ}		8	ns
TCB↓ setting time (to CLK↓)	t_{SED}	10		ns
TCB pulse width	t_{EDEDL}	10		ns
Address lower byte output delay time (to CLK↑)	t_{KFA}		5	ns
READ/WRITE output delay time (to CLK↑)	t_{KFC}		5	ns
Address higher byte output delay time (to CLK↑)	t_{KFD}		5	ns
HLDA valid setting time(to CLK↑)	t_{SHA}	0	0	ns
Input data hold time (from MRDB↑)	t_{HMRID}	0	0	ns
Input data setting time (to MRDB↑)	t_{SIDMR}	15		ns
Output data hold time (from MWRB↑)	t_{HMWOD}	5		ns
Output data valid setting time (to MWRB↑)	t_{SODMW}	t_{CY} – 1		ns
DREQ setting time (to CLK↓ (SI, S1))	t_{SDQ}	5		ns
READY hold time (from CLK↓)	t_{HRY}	5		ns
READY setting (to CLK↓)	t_{SRY}	10		ns
ADSTB↑ delay time (to CLK↑)	t_{DSTH}		5	ns

(2/2)

Parameter	Symbol	MIN.	MAX.	Unit
ADSTB↓ delay time (to CLK↑)	t_{DSTL}		5	ns
CDB↑ delay time (to CLK↑)	t_{CDHD}		15	ns
CDB↓ delay time (to CLK↑)	t_{CDLD}		3	ns
CAB↑ delay time (to CLK↑)	t_{CAH}		8	ns
CAB↓ delay time (to CLK↑)	t_{CAL}		8	ns
CEP↑ delay time (to CLK↑)	t_{CEH}		8	ns
CEP↓ delay time (to CLK↑)	t_{CEL}		8	ns
CRW↑ delay time (to CLK↑)	t_{CRH}		8	ns
CRW↓ delay time (to CLK↑)	t_{CRL}		8	ns

(2) Inactive cycle

Parameter	Symbol	MIN.	MAX.	Unit
Address higher byte valid/CS↓ (to READ↓)	t_{SAIR}	0		ns
Address higher byte valid setting time (to WRITE↑)	t_{SAIW}	10		ns
CS↓ setting time (to WRITE↑)	t_{SCSIW}	10		ns
Input data setting time (to WRITE↑)	t_{SIDIW}	10		ns
Address higher byte/CS hold time (from READ↑)	t_{HIRA}	0		ns
Data access time (to READ↑)	t_{DIROD}		8	ns
Address higher byte float delay time (to READ↑)	t_{FIROD}	0	8	ns
V_{DD}↑ setting time (to RESET↓)	t_{SVDD}	500		ns
1st RDIB/WRIB (to RESET↓)	t_{SYIWR}	$2t_{CY}$		ns
RESET pulse width	t_{RESET}	50		ns
READ width	t_{IRIRL}	30		ns
Address lower byte hold time (to WRITE↑)	t_{HIWA}	5		ns
CS↑ hold time (to WRITE↑)	t_{HIWCS}	5		ns
Input data hold time (to WRITE↑)	t_{HIWID}	5		ns
WRITE width	t_{IWIWL}	25		ns
Read/write recovery time	t_{RVIWR}	50		ns
CDB↑ delay time (to RDIB↓)	t_{CDHR}		7	ns
CDB↓ delay time (to RDIB↑)	t_{CDLR}		7	ns

Remarks 1. The output load conditions of the propagation delay time are fanout = 1 and wiring length = 0 mm.

2. The actual WRIB or MWRB pulse width is $1t_{CYK}$ (ns) during normal write and $2t_{CYK}$ (ns) during extended write.

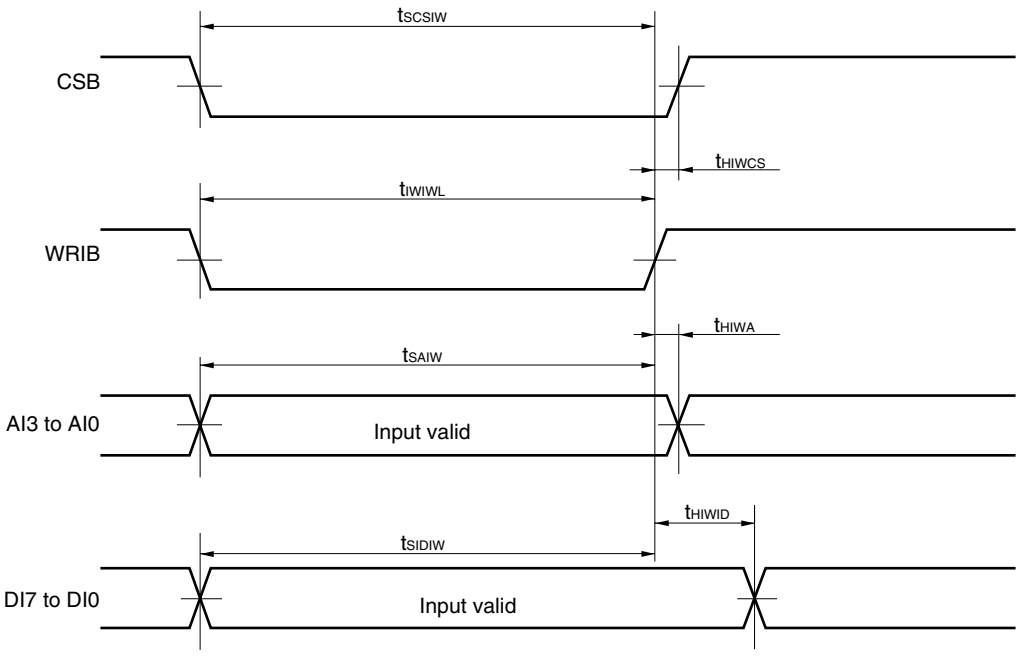
The actual RDIB or MRDB pulse width is $2t_{CYK}$ (ns) during normal read and $1t_{CYK}$ (ns) during compressed read.

3. Keep DREQ active until DACK is returned.

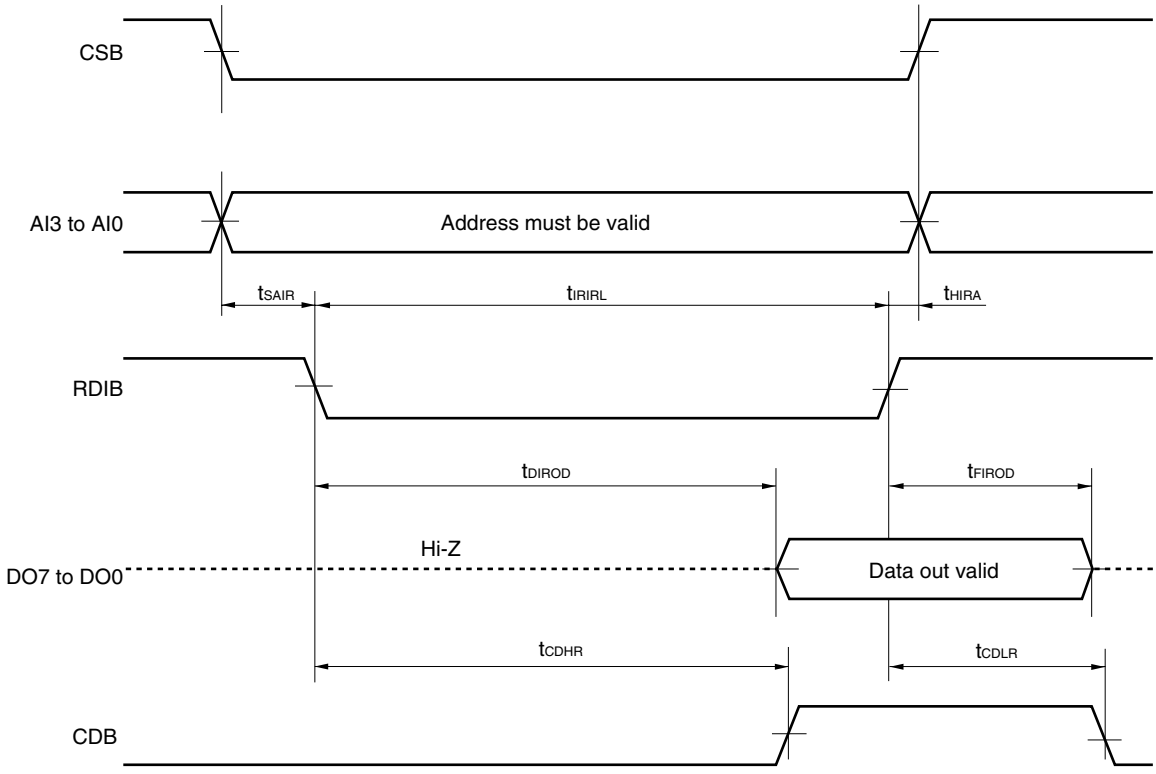
4. The DREQ and DACK signals may be active-high or active-low. In the timing chart, they are assumed to be active-high.

2.5 Timing Charts

(1) Inactive cycle write timing

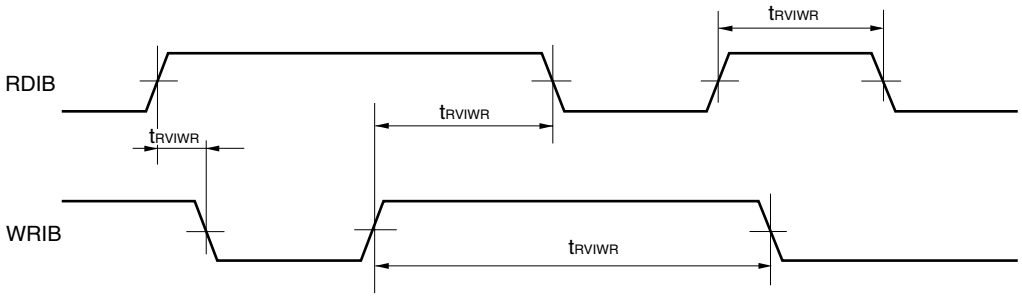


(2) Inactive cycle read timing

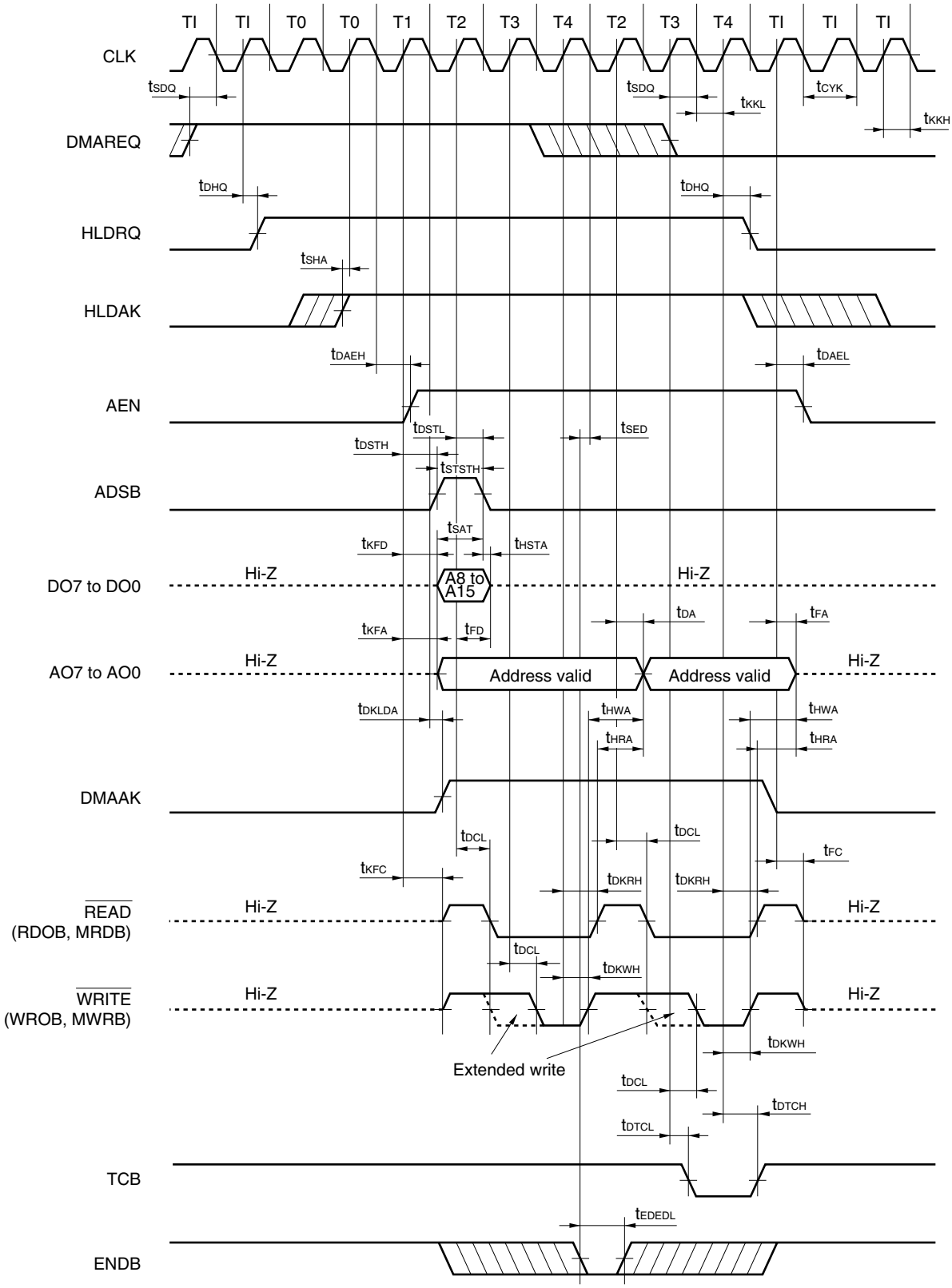


Remark The dotted line indicates a high-impedance state.

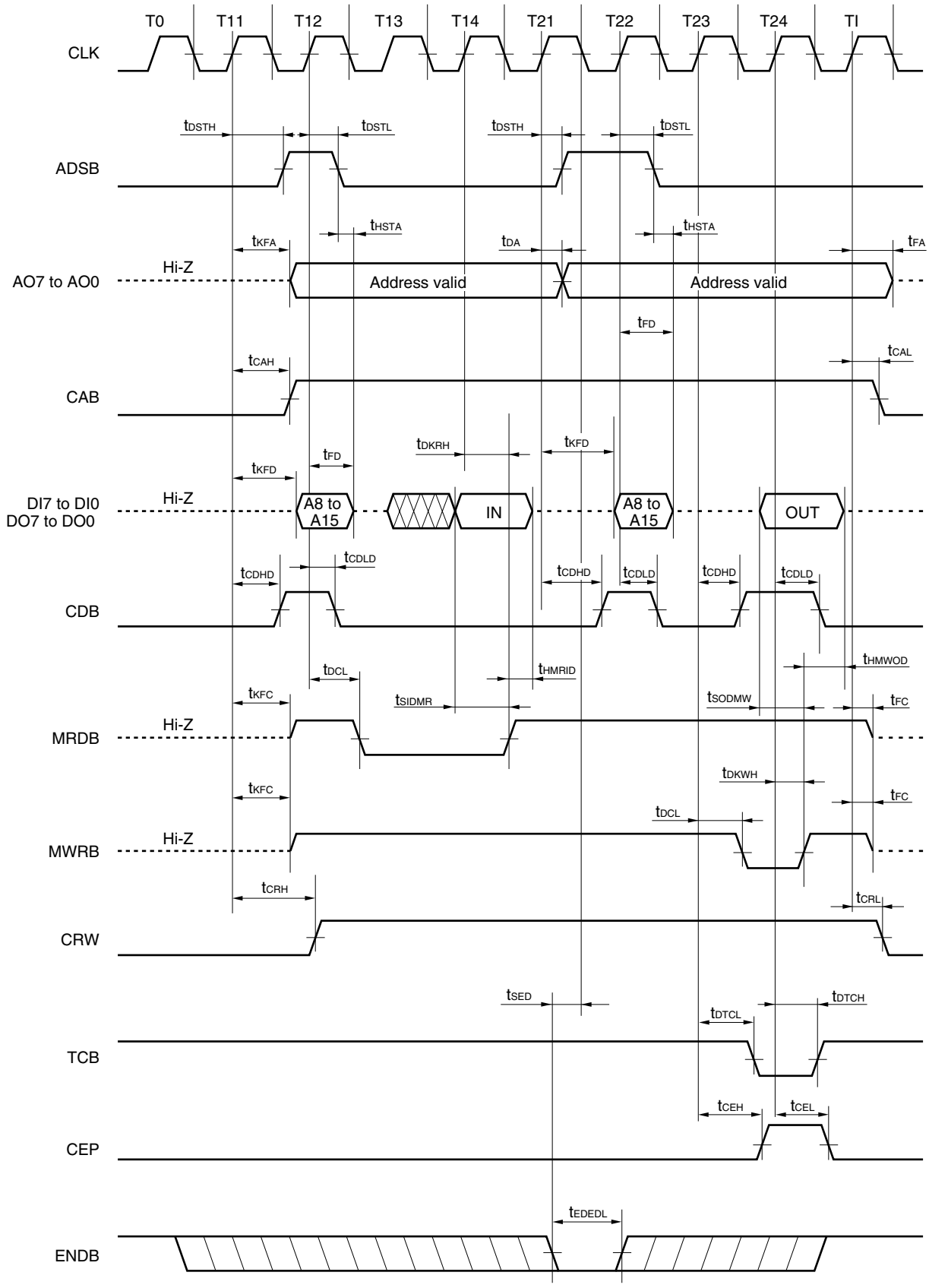
(3) Read/write recovery time



(4) I/O memory transfer timing

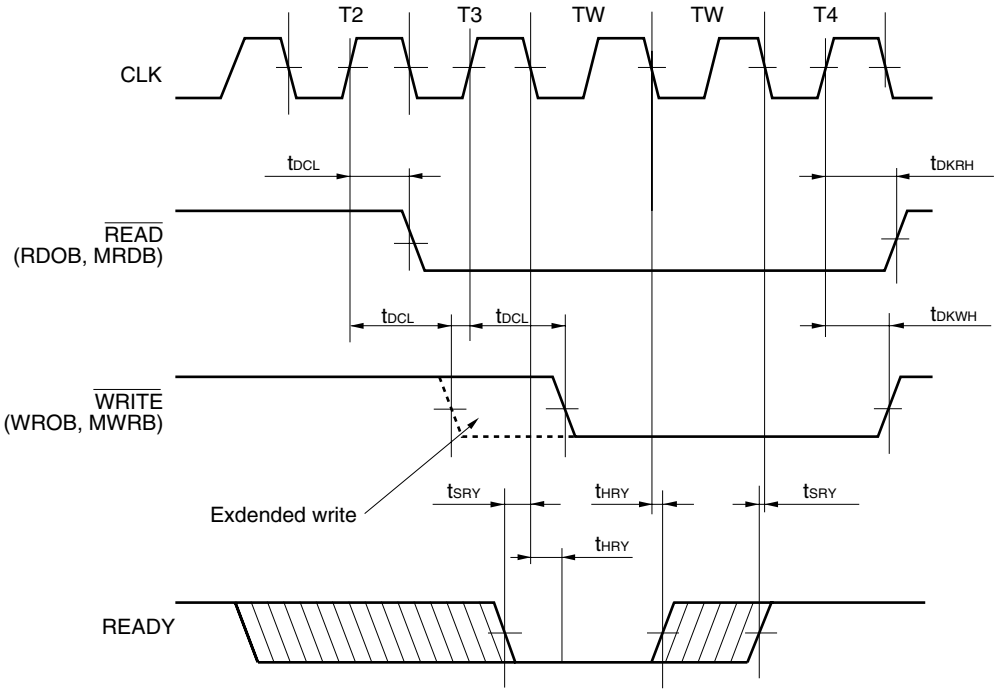


(5) Memory-to-memory transfer timing

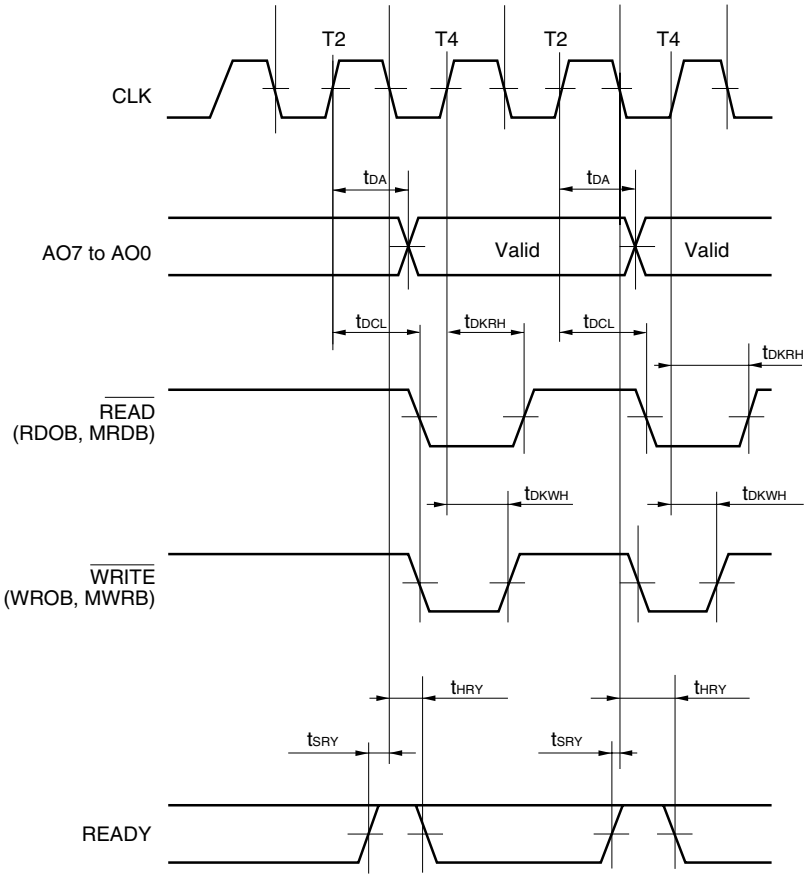


Remark The dotted line indicates a high-impedance state.

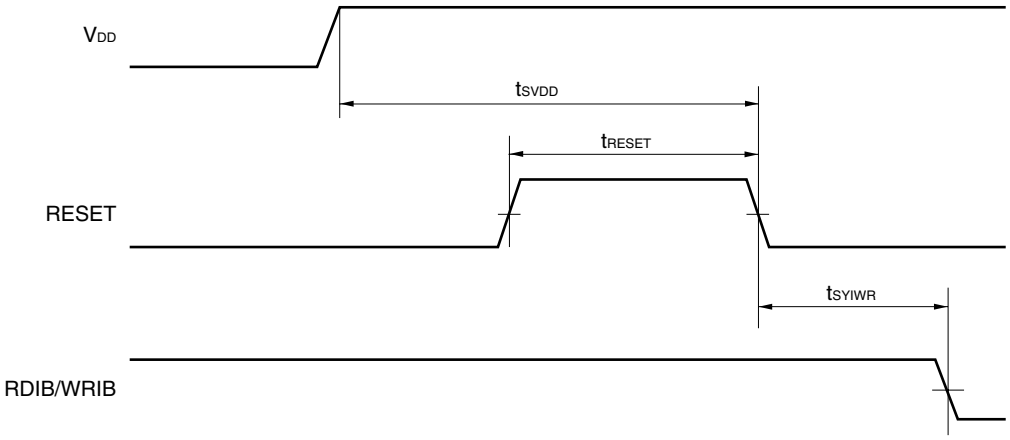
(6) Ready timing



(7) Compressed transfer timing



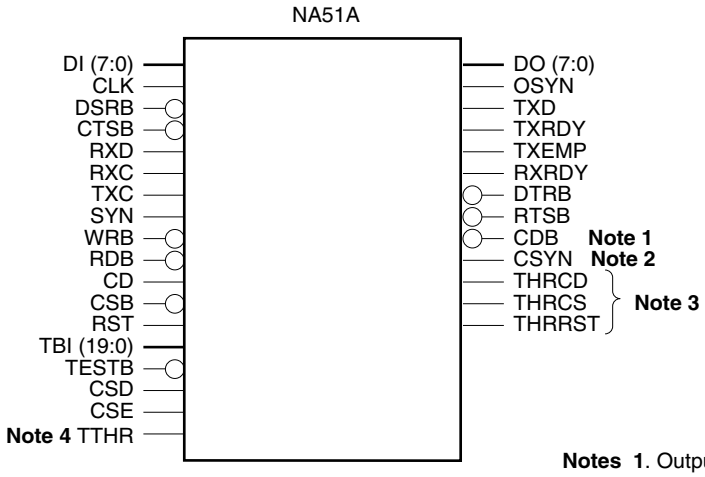
(8) Reset



CHAPTER 3 NA51A MACRO

This chapter explains the functions of the NA51A.

Block Type	Function
NA51A	Serial Control Unit (Universal synchronous/asynchronous receiver/transmitter)



Features

- Compatible functions with μPD71051
- Maximum operating frequency: 33 MHz
- Baud rate: DC-660 Kbps

Caution

- Do not input spike to CLK, RXC, TXC, WRB, RDB, and RST.

Notes 1. Output control signal of DO7 through DO0
2. Output control signal of OSYN
3. Through path output signals of CD, CSB, and RST in the pre- or post-mega-macro stage test
4. Through path/normal mode select pin

Remark The input signal pins with “TBI” prefixed are test pins.

Number of cells used (configuration)	2660 (95 × 28)
Mega macro test pattern length	12874

3.1 NA51A Pins

Pin Name	I/O	Function	Active Level	Test Pin	Fanin/ Fanout	Block Name
DI0	Input	Data bus input signal (LSB)		TBI0	1.8	L424
DI1	Input	Data bus input signal		TBI1	1.6	L424
DI2	Input	Data bus input signal		TBI2	1.2	L424
DI3	Input	Data bus input signal		TBI3	1.0	L424
DI4	Input	Data bus input signal		TBI4	1.0	L424
DI5	Input	Data bus input signal		TBI5	1.5	L424
DI6	Input	Data bus input signal		TBI6	1.4	L424
DI7	Input	Data bus input signal (MSB)		TBI7	1.4	L424
CLK	Input	System clock signal		TBI8	1.0	L424
DSRB	Input	General-purpose input pin (data set ready)	Low	TBI9	1.4	L424
CTSB	Input	Transmit control input pin (clear to send)	Low	TBI10	1.0	L424
RXD	Input	Serial data receive pin		TBI11	1.0	L424
RXC	Input	Receive clock signal		TBI12	1.0	L424
TXC	Input	Transmit clock signal		TBI13	1.0	L424
SYN	Input	Used to detect external synchronization in synchronization mode		TBI14	1.0	L424
WRB	Input	Write signal	Low	TBI15	1.0	L424
RDB	Input	Read signal	Low	TBI16	1.0	L424
CD	Input	“H”: Control word “L”: Character data		TBI17	1.8	L424
CSB	Input	Chip select signal	Low	TBI18	1.5	L424
RST	Input	System reset signal	High	TBI19	1.1	L424
TESTB	Input	Test/normal mode selection “H”: Normal mode “L”: Test mode		–	2.2	F112
CSD	Input	3-state output control		–	1.4	L111
CSE	Input	3-state output control		–	2.3	L111
TTHR	Input	Through path/normal mode select signal “H”: Through path mode “L”: Normal mode		–	2.4	L101
DO0	Output	Data bus output signal (LSB)		–	34.0	F531
DO1	Output	Data bus output signal		–	33.0	F531
DO2	Output	Data bus output signal		–	34.0	F531
DO3	Output	Data bus output signal		–	33.0	F531
DO4	Output	Data bus output signal		–	33.0	F531
DO5	Output	Data bus output signal		–	34.0	F531
DO6	Output	Data bus output signal		–	33.0	F531
DO7	Output	Data bus output signal (MSB)		–	34.0	F531

Pin Name	I/O	Function	Active Level	Test Pin	Fanin/ Fanout	Block Name
OSYN	Output	In synchronous mode: Internal synchronization detection signal In asynchronous mode: break signal		–	30.0	F532
TXD	Output	Serial data transmit pin		–	31.0	F111
TXRDY	Output	Signal indicating transmit data write enable		–	31.0	F111
TXEMP	Output	Signal indicating that the two transmit data buffers are empty		–	34.0	F111
RXRDY	Output	Signal indicating receive data read enable		–	30.0	F111
DTRB	Output	General-purpose output pin (data terminal ready)		–	34.0	F111
RTSB	Output	General-purpose output pin (request to send)		–	34.0	F111
CDB	Output	Enable signal of data bus		–	30.0	F111
CSYN	Output	Enable signal of OSYN		–	29.0	F111
THRCD	Output	Through path output pin		–	32.0	F312
THRCS	Output	Through path output pin		–	32.0	F312
THRRST	Output	Through path output pin		–	27.0	F312
TBI0	Input	Test input		–	1.9	L424
TBI1	Input	Test input		–	1.8	L424
TBI2	Input	Test input		–	1.3	L424
TBI3	Input	Test input		–	1.1	L424
TBI4	Input	Test input		–	1.1	L424
TBI5	Input	Test input		–	1.7	L424
TBI6	Input	Test input		–	1.5	L424
TBI7	Input	Test input		–	1.5	L424
TBI8	Input	Test input		–	1.1	L424
TBI9	Input	Test input		–	1.5	L424
TBI10	Input	Test input		–	1.1	L424
TBI11	Input	Test input		–	1.1	L424
TBI12	Input	Test input		–	1.1	L424
TBI13	Input	Test input		–	1.1	L424
TBI14	Input	Test input		–	1.1	L424
TBI15	Input	Test input		–	1.1	L424
TBI16	Input	Test input		–	1.1	L424
TBI17	Input	Test input		–	1.8	L424
TBI18	Input	Test input		–	1.5	L424
TBI19	Input	Test input		–	1.2	L424

Remark Input: Input pin
Output: Output pin

Remarks 1. TBIx is a test input pin. A signal can be input from TBIx by making the TESTB input low. Connect pins so that signals can be directly input to the mega macro from outside the gate array in test mode. "Directly" here means a circuit configuration where the input signal is not inverted or no sequential circuit such as a flip-flop is inserted between the pins.

TESTB	Input Pin
1	Normal pin[Note]
0	TBIx

Note Input a defined value of 0 or 1 to the test input pins in normal mode (it does not matter if 0 and 1 are mixed).

2. Functions of CSE input and CSD input

CSE input: Turns on (high or low level) all the 3-state outputs when "1" is input to this pin.

CSD input: Turns off (high-impedance: Hi-Z) of all the 3-state outputs when "0" is input to this pin while CSE = "0".

When "1" is input, the 3-state outputs are turned on/off by an internal control signal of the mega macro (normal operation).

CSE	CSD	Status of Output Pin	Status of 3-State Output Pin[Note]
0	0	Normal operation	Hi-Z
0	1	Normal operation	Normal operation
1	–	Normal operation	No Hi-Z output

Note 3-state pins are DO7 to DO0 and OSYN.

3. When CSE = "0", the Hi-Z status of the 3-state output buffer can be checked by monitoring the output value of the corresponding output control signal.

"Hi-Z" Pin	Corresponding Output Control Signal and Output	
DO7 to DO0	CDB	0
OSYN	CSYN	0

When CSE = "1", the status of the buffer is not affected by the 3-state output control signal (the 3-state output does not go into a "Hi-Z" state).

4. CSE and CSD can be fixed by clamping. Fix CSD to 1 when clamping it.

Remarks 5. Operating status of output pin depending on combination of TTHR, CSE, and CSD

TTHR Pin	CSE Pin	CSD Pin	3-State Output Pin (DOx)	3-State Control Pin (CDB(SD))	Other Pins	Through Path Dedicated Pin (Output THRxxx)
0	0	0	Hi-Z	0	Normal operation	0
		1	Normal operation	Normal operation		
	1	0	No Hi-Z output	0		
		1		Normal operation		
1	0	0	Hi-Z	Through path	Through path	Through path
		1	Through path			
	1	×				

6. I/O pin correspondence table in through path test

The input pins corresponding to the mega macro output pins when TTHR = “1” are as follows:

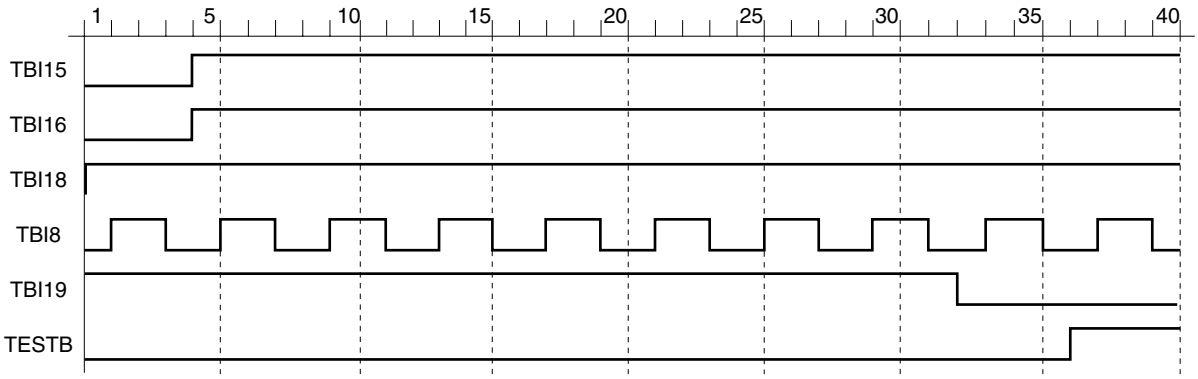
Output Pin	Through Path Corresponding Pin	
	TESTB = 1	TESTB = 0
DO0	DI0	TBI0
DO1	DI1	TBI1
DO2	DI2	TBI2
DO3	DI3	TBI3
DO4	DI4	TBI4
DO5	DI5	TBI5
DO6	DI6	TBI6
DO7	DI7	TBI7
OSYN	CLK	TBI8
TXD	DSRB	TBI9

Output Pin	Through Path Corresponding Pin	
	TESTB = 1	TESTB = 0
TXRDY	CTSB	TBI10
TXEMP	RXD	TBI11
RXRDY	RXC	TBI12
DTRB	TXC	TBI13
RTSB	SYN	TBI14
CDB	WRB	TBI15
CSYN	RDB	TBI16
THRCD	CD	TBI17
THRCS	CSB	TBI18
THRRST	RST	TBI19

When TTHR = “1” and CSE = “0”, all the 3-state pins are controlled by CSD (selection between through path and high impedance).

3.2 NA51A Initialization Pattern

The internal status of the mega macro is undefined on starting simulation. Therefore, input the following initialization pattern to determine the internal status when executing simulation.



Input “0” or “1” to the other input pins (normal input and test input).
Exercise care that “X” is not input.

- **Value of mega macro output pin after initialization pattern**

Pin Name	Status
DO7 to DO0	Hi-Z
OSYN	0
TXD	1
TXRDY	0
TXEMP	1
RXRDY	0
DTRB	1
RTSB	1
CDB	0
CSYN	1
THRCD	0
THRCS	0
THRRST	0

Cautions 1. NA51A is in the standby mode after the initialization pattern.
2. The clock is necessary during reset (the reset pulse width must be at least 6 clocks).
3. Configure the following input pins in a circuit that avoids spike input:
CLK, RXC, TXC, WRB, RDB, RST

3.3 Delay Time

Refer to **1.2.4 Delay time**.

3.4 AC Characteristics (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

(1) Read cycle

Parameter	Symbol	MIN.	MAX.	Unit
Address (CSB, CD) setup time (to RDB ↓)	t_{SAR}	0		ns
Address (CSB, CD) hold time (from RDB ↑)	t_{HRA}	0		ns
RDB pulse width	t_{RRL}	30		ns
Data delay time (to RDB ↓)	t_{DRD}	15	35	ns
Data float delay time (to RDB ↑)	t_{FRD}	15	35	ns
Port (DSRB, CTSB) setup time (to RDB ↓)	t_{SPR}	20		t_{CYK}
CDB high delay time (to RDB ↓)	t_{CDHR}	15	35	ns
CDB low delay time (to RDB ↑)	t_{CDLR}	15	35	ns

(2) Write cycle

Parameter		Symbol	MIN.	MAX.	Unit
Address (CSB, CD) setup time (to WRB ↓)		t_{SAW}	0		ns
Address (CSB, CD) hold time (from WRB ↑)		t_{HWA}	0		ns
WRB pulse width		t_{WWL}	30		ns
Data setup time (to WRB ↑)		t_{SDW}	1		ns
Data hold time (from WRB ↑)		t_{HWD}	0		ns
Port (DTRB, RTSB), TXEN delay time (to WRB ↑)		t_{DWP}		8	t_{CYK}
Write recovery time	When mode is specified	t_{RV}	6		t_{CYK}
	Asynchronous mode		12		t_{CYK}
	Synchronous mode		16		t_{CYK}

<R> **(3) Other timing**

Parameter		Symbol	MIN.	MAX.	Unit
Clock cycle		t_{CYK}	30		ns
Clock pulse high-level width		t_{KKH}	20		ns
Clock pulse low-level width		t_{KKL}	10		ns
TXD delay time (to TXCB ↓)		t_{DTKTD}	3	11	ns
Transmitter input clock pulse low-level width	1 × BR	t_{TKTKL}	12		t_{CYK}
	16 × BR, 64 × BR		1		t_{CYK}
Transmitter input clock pulse high-level width	1 × BR	t_{TKTKH}	15		t_{CYK}
	16 × BR, 64 × BR		3		t_{CYK}
Transmitter input clock frequency	1 × BR	f_{TK} Note 1	DC	660	kHz
	16 × BR		DC	4400	kHz
	64 × BR		DC	4400	kHz
Receiver input clock pulse low-level width	1 × BR	t_{RKRKL}	12		t_{CYK}
	16 × BR, 64 × BR		1		t_{CYK}
Receiver input clock pulse high-level width	1 × BR	t_{RKRKH}	15		t_{CYK}
	16 × BR, 64 × BR		3		t_{CYK}
Receiver input clock frequency	1 × BR	f_{RK} Note 1	DC	600	kHz
	16 × BR		DC	4400	kHz
	64 × BR		DC	4400	kHz
RXD setup time (to sampling pulse ↑)		t_{SRDSP} Note 2	1		μs
RXD hold time (from sampling pulse ↓)		t_{HSPRD} Note 2	1		μs
TXEM delay time		t_{DTXEP}		20	t_{CYK}
TXRD delay time (to TXRD ↑)		t_{DTXR}		8	t_{CYK}
TXRD delay time (to TXRD ↓)		t_{DWTXR}	5	17	ns
RXRD delay time (to RXRD ↑)		t_{DRXR}		26	t_{CYK}
RXRD delay time (to RXRD ↓)		t_{DRRXR}	2	7	ns
OSYN output delay time (internal synchronization)		t_{DRKSY}		26	t_{CYK}
SYN input setup time (external synchronization)		t_{SSYRK}	18		t_{CYK}
Reset pulse high-level width		t_{RST}	6		t_{CYK}

Notes 1. The frequency of TXC and RXC is limited in respect to CLK as follows:
1 × BR: f_{TK} or $f_{RK} \leq 1/30t_{CYK}$
16 × BR, 64 × BR: f_{TK} or $f_{RK} \leq 1/4.5t_{CYK}$

2. In the start-stop synchronization mode (16 × BR, 64 × BR), there is no problem if the bit width of the serial input of RXD matches the number of bits set and the transfer rate length.
Both t_{SRDSP} and t_{HSPRD} must be 3 × t_{CYK} or more in the start-stop synchronization mode (1 × BR).

Remarks 1. The system clock must be input during reset.

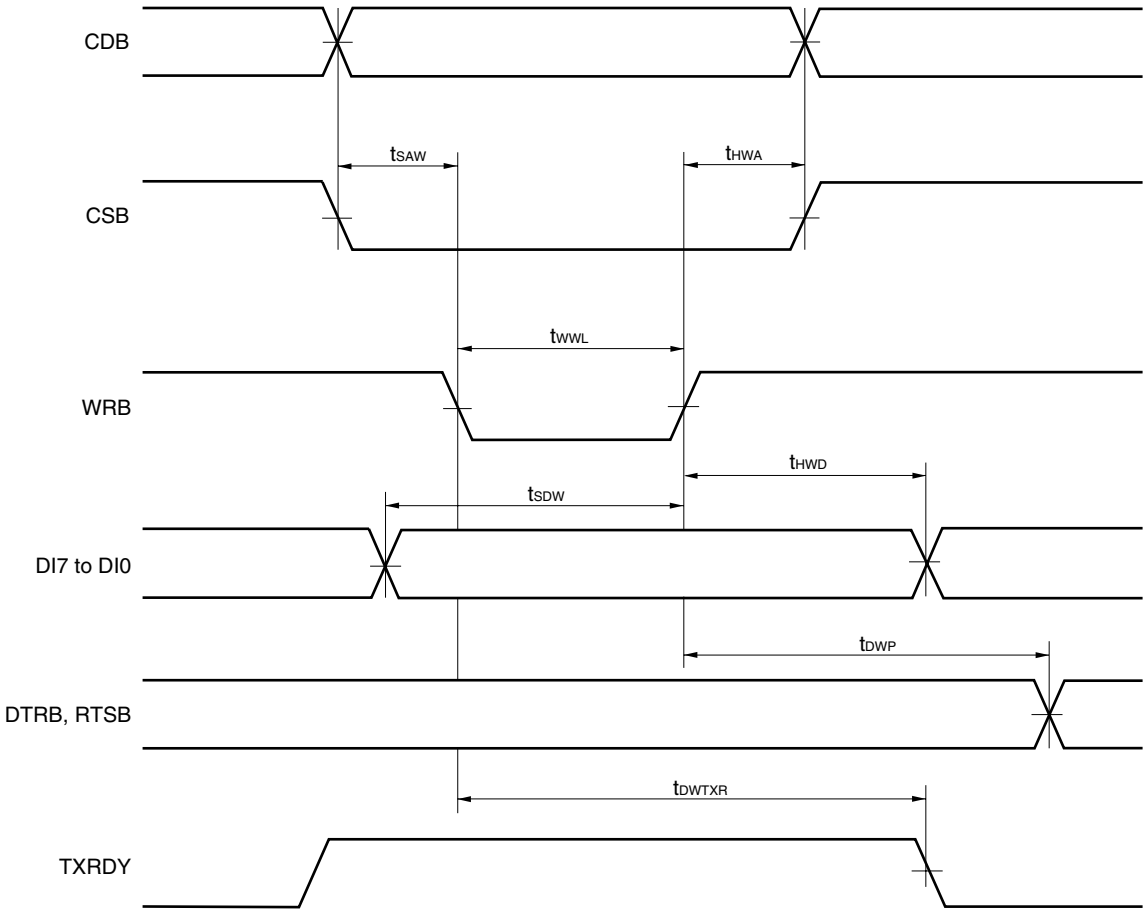
2. Updating the status is delayed by up to 28t_{CYK} after an event has influenced the status.

3. The output load conditions of the propagation delay time are fanout: 1, wiring length: 0 mm.

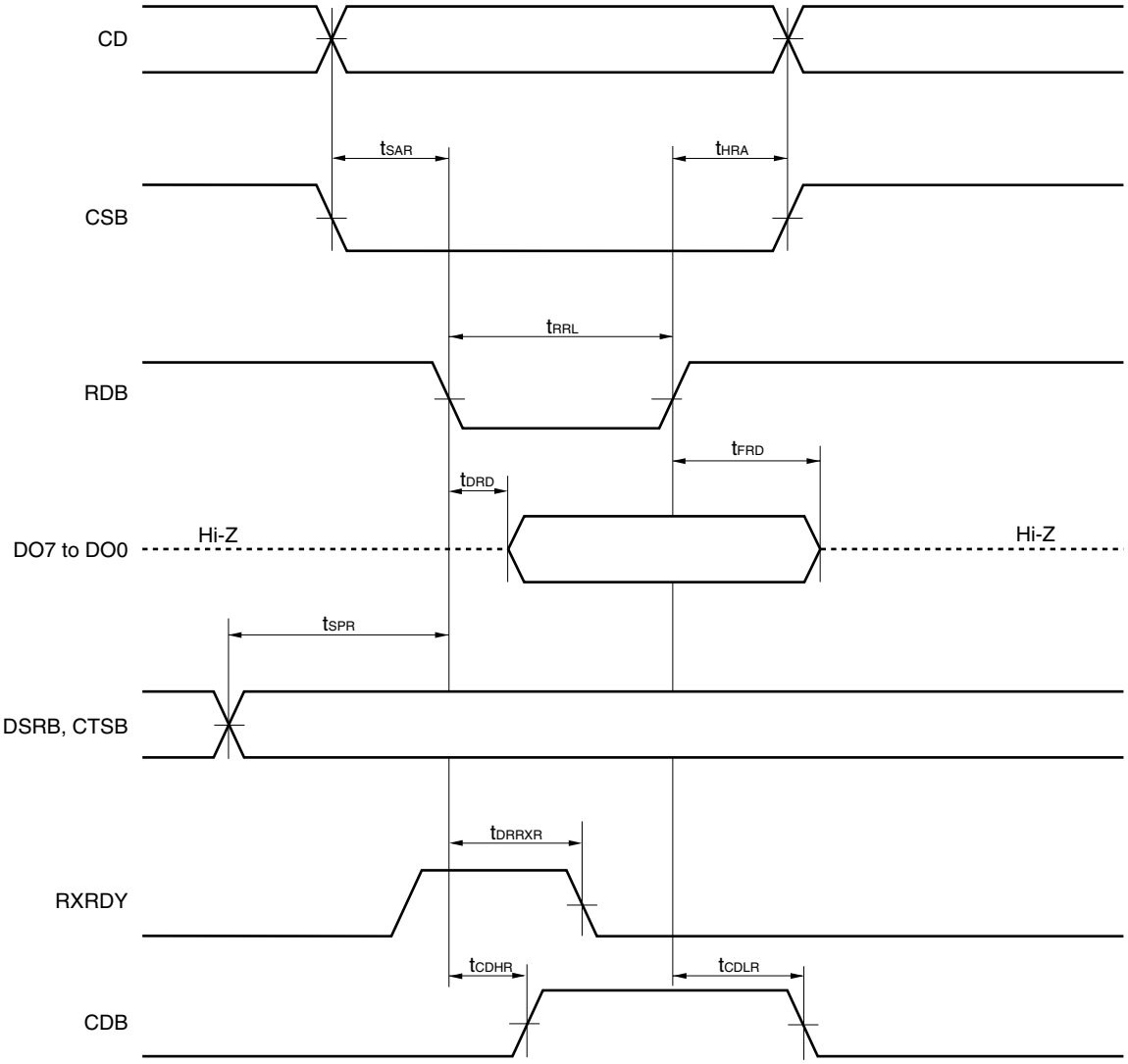
4. BR: Baud rate

3.5 Timing Charts

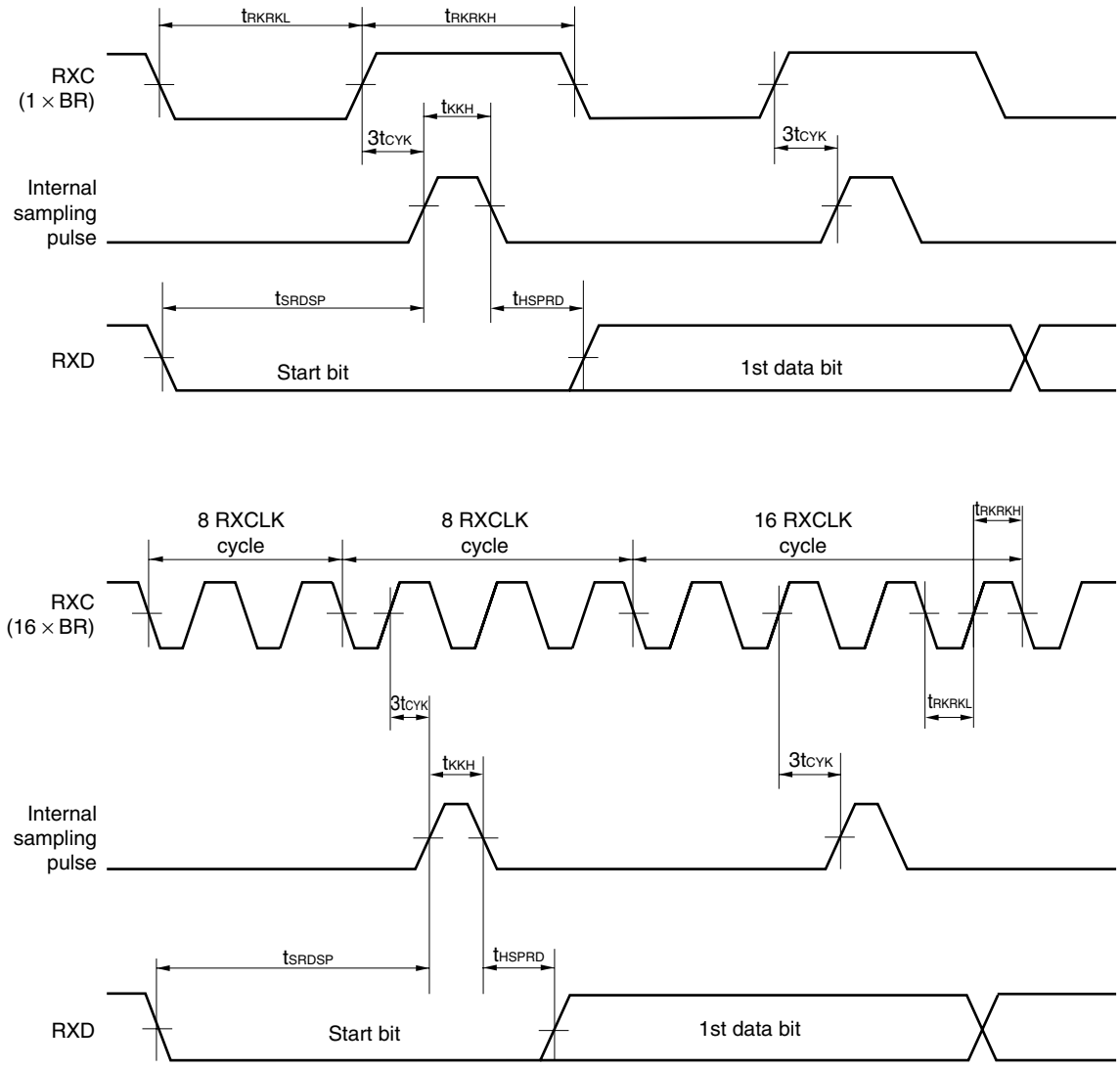
(1) Write data timing



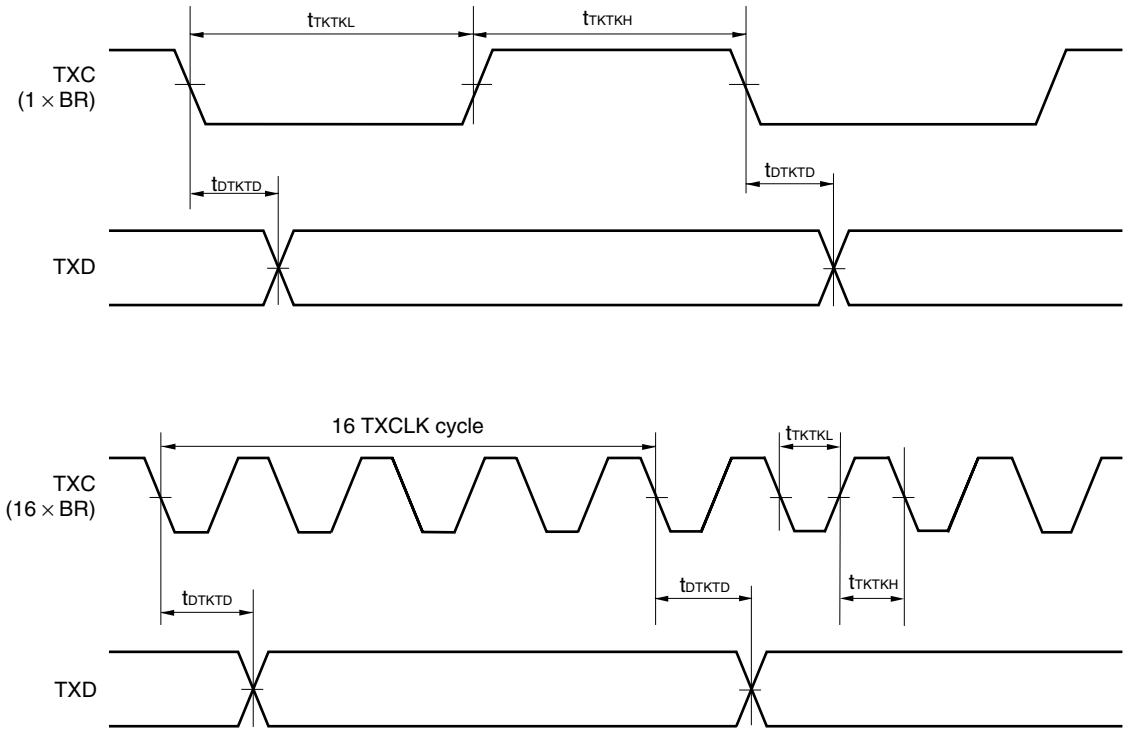
(2) Read data timing



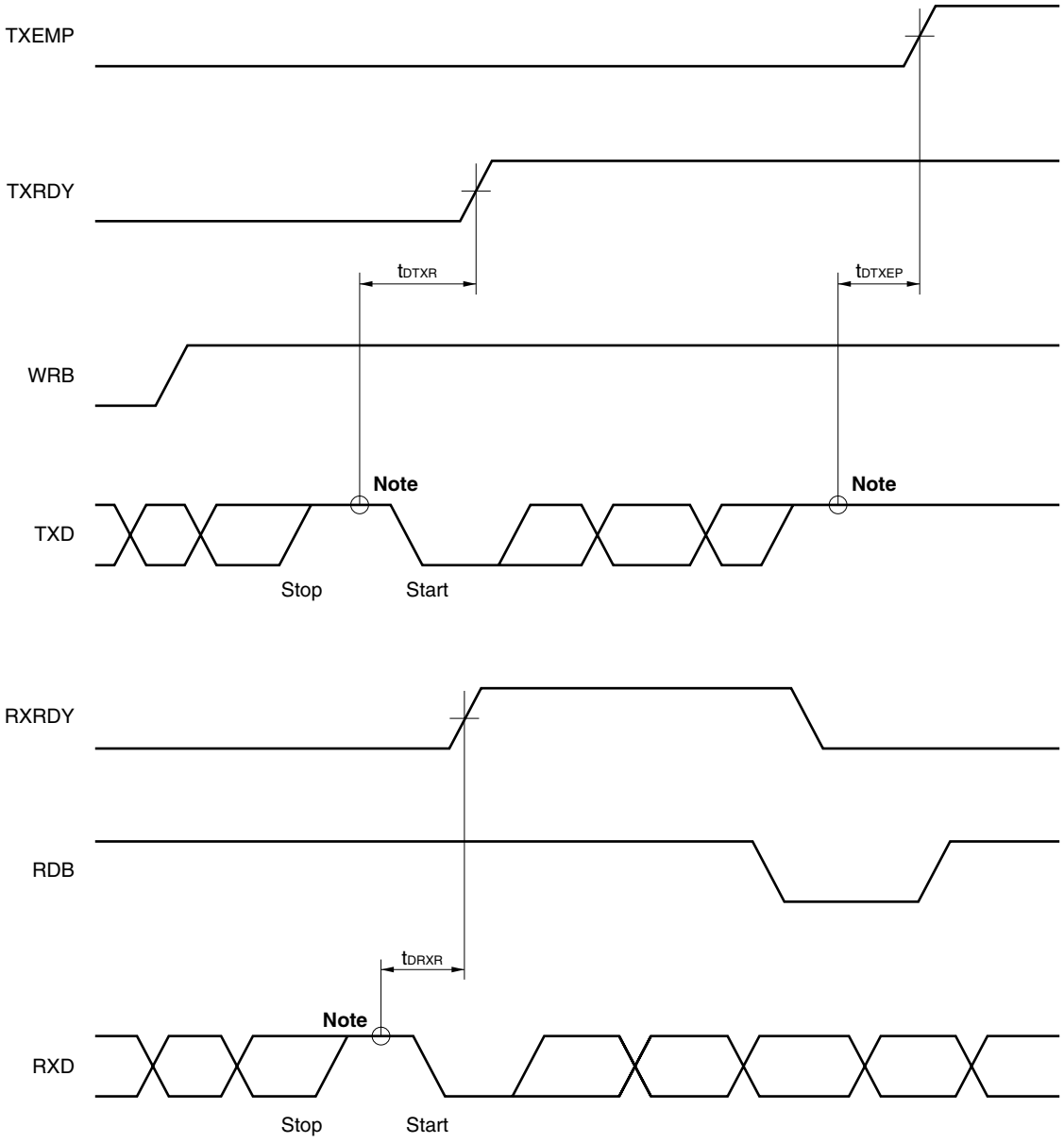
(3) Receiver clock and RXD



(4) Transmitter clock and TXD

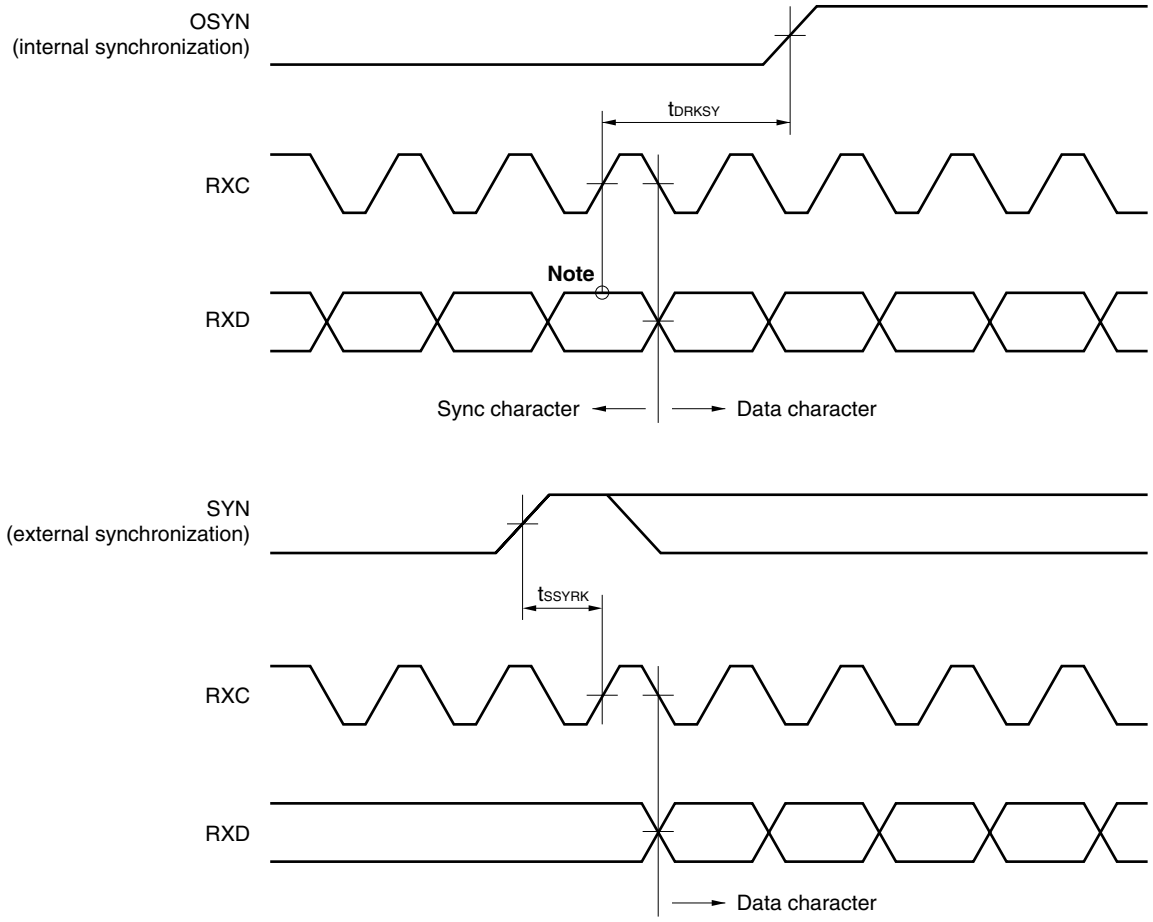


(5) Timing of flag



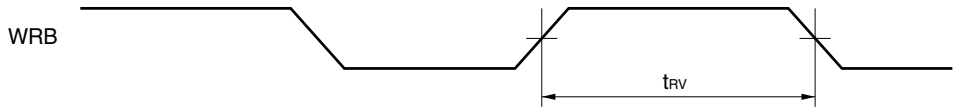
Note 1/2 bit.
Rising of the 8th clock if ×16 clock is used for sampling.
Rising of the 32nd clock if ×64 clock is used for sampling.

(6) Timing of RXD, SYN, and OSYN

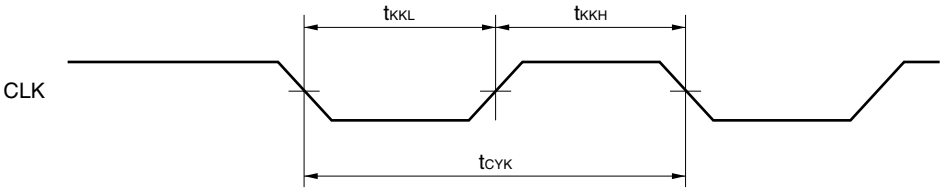


Note 1/2 bit.
Rising of the 8th clock if ×16 clock is used for sampling.
Rising of the 32nd clock if ×64 clock is used for sampling.

(7) Write recovery time



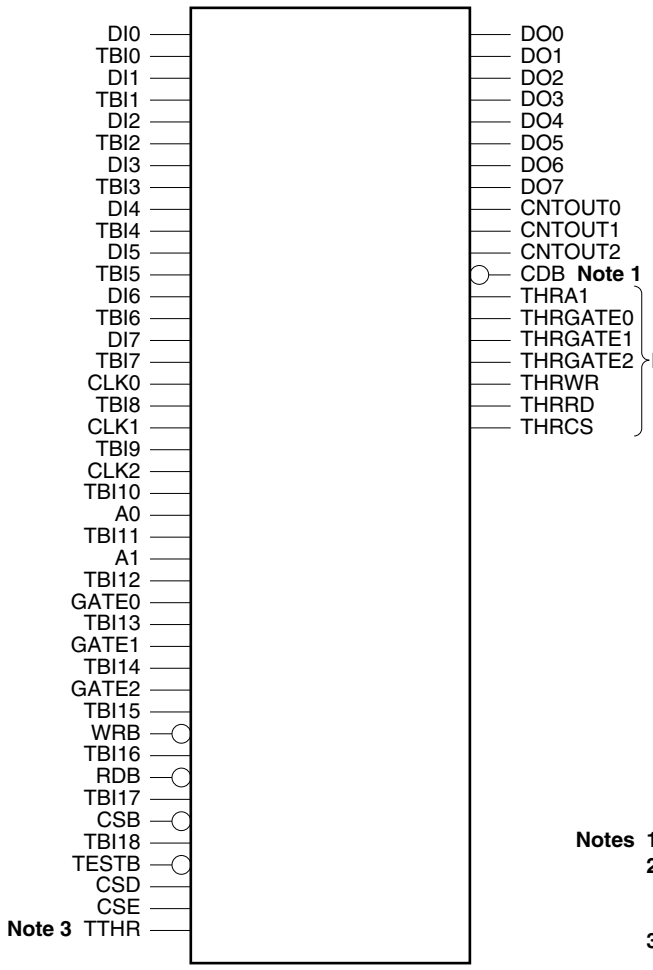
(8) Main clock



CHAPTER 4 NA54A MACRO

This chapter explains the functions of the NA54A.

Block Type	Function
NA54A	Programmable Timer/Counter



Features

- Compatible functions with μPD71054
- Maximum operating frequency: 33 MHz

Caution

- Do not input spike to CLK0, CLK1, CLK2, GATE0, GATE1, GATE2, WRB, and RDB.

Notes 1. Output control signal of DO7 through DO0
2. Through path output pins of A1, GATE0, GATE1, GATE2, WRB, RDB, and CSB in the pre- or post-mega-macro stage test
3. Through path/normal mode select pin

Remark The input signal pins with "TBI" prefixed are test pins.

Number of cells used (configuration)	4514 (122 × 37)
Mega macro test pattern length	3479

4.1 NA54A Pins

Pin Name	I/O	Function	Active Level	Test Pin	Fanin/ Fanout	Block Name
DI0	Input	Data bus input signal (LSB)		TBI0	1.3	L424
DI1	Input	Data bus input signal		TBI1	3.2	L424
DI2	Input	Data bus input signal		TBI2	2.7	L424
DI3	Input	Data bus input signal		TBI3	2.5	L424
DI4	Input	Data bus input signal		TBI4	1.1	L424
DI5	Input	Data bus input signal		TBI5	1.3	L424
DI6	Input	Data bus input signal		TBI6	2.4	L424
DI7	Input	Data bus input signal (MSB)		TBI7	1.5	L424
CLK0	Input	Clock of counter #0		TBI8	1.9	L424
CLK1	Input	Clock of counter #1		TBI9	1.3	L424
CLK2	Input	Clock of counter #2		TBI10	1.1	L424
A0	Input	Address (LSB)		TBI11	1.6	L424
A1	Input	Address (MSB)		TBI12	1.5	L424
GATE0	Input	Gate input of counter #0		TBI13	1.1	L424
GATE1	Input	Gate input of counter #1		TBI14	1.1	L424
GATE2	Input	Gate input of counter #2		TBI15	1.7	L424
WRB	Input	Write signal	Low	TBI16	1.5	L424
RDB	Input	Read signal	Low	TBI17	1.5	L424
CSB	Input	Chip select signal	Low	TBI18	1.0	L424
CSD	Input	3-state output control		–	2.8	L101
CSE	Input	3-state output control		–	3.7	L111
TTHR	Input	Through path/normal mode select signal “H”: Through path mode “L”: Normal mode		–	2.3	L111
TESTB	Input	Test/normal mode select signal “H”: Normal mode “L”: Test mode		–	3.1	F101
DO0	Output	Data bus output signal (LSB)		–	30.0	F532
DO1	Output	Data bus output signal		–	30.0	F532
DO2	Output	Data bus output signal		–	31.0	F532
DO3	Output	Data bus output signal		–	30.0	F532
DO4	Output	Data bus output signal		–	31.0	F532
DO5	Output	Data bus output signal		–	31.0	F532
DO6	Output	Data bus output signal		–	32.0	F532
DO7	Output	Data bus output signal (MSB)		–	33.0	F532
CNTOUT0	Output	Output of counter #0		–	31.0	F101
CNTOUT1	Output	Output of counter #1		–	33.0	F101

Pin Name	I/O	Function	Active Level	Test Pin	Fanin/ Fanout	Block Name
CNTOUT2	Output	Output of counter #2		–	33.0	F101
CDB	Output	Enable signal of data bus		–	32.0	F111
THRA1	Output	Through path output pin		–	29.0	F312
THRGATE0	Output	Through path output pin		–	27.0	F312
THRGATE1	Output	Through path output pin		–	25.0	F312
THRGATE2	Output	Through path output pin		–	28.0	F312
THRWR	Output	Through path output pin		–	28.0	F312
THRRD	Output	Through path output pin		–	29.0	F312
THRCS	Output	Through path output pin		–	28.0	F312
TBI0	Input	Test input		–	1.3	L424
TBI1	Input	Test input		–	4.4	L424
TBI2	Input	Test input		–	2.9	L424
TBI3	Input	Test input		–	2.5	L424
TBI4	Input	Test input		–	1.1	L424
TBI5	Input	Test input		–	1.4	L424
TBI6	Input	Test input		–	2.3	L424
TBI7	Input	Test input		–	1.5	L424
TBI8	Input	Test input		–	2.1	L424
TBI9	Input	Test input		–	1.3	L424
TBI10	Input	Test input		–	1.1	L424
TBI11	Input	Test input		–	1.5	L424
TBI12	Input	Test input		–	1.5	L424
TBI13	Input	Test input		–	1.1	L424
TBI14	Input	Test input		–	1.1	L424
TBI15	Input	Test input		–	1.8	L424
TBI16	Input	Test input		–	1.7	L424
TBI17	Input	Test input		–	1.5	L424
TBI18	Input	Test input		–	1.2	L424

Remark Input: Input pin
Output: Output pin

Remarks 1. TBIx is a test input pin. A signal can be input from TBIx by making the TESTB input low. Connect pins so that signals can be directly input to the mega macro from outside the gate array in test mode. "Directly" here means a circuit configuration where the input signal is not inverted or no sequential circuit such as a flip-flop is inserted between the pins.

TESTB	Input Pin
1	Normal pin[Note]
0	TBIx

Note Input a defined value of 0 or 1 to the test input pins in normal mode (it does not matter if 0 and 1 are mixed).

2. Functions of CSE input and CSD input

CSE input: Turns on (high or low level) all the 3-state outputs when "1" is input to this pin.

CSD input: Turns off (high-impedance: Hi-Z) of all the 3-state outputs when "0" is input to this pin while CSE = "0".

When "1" is input, the 3-state outputs are turned on/off by an internal control signal of the mega macro (normal operation).

CSE	CSD	Status of Output Pin	Status of 3-State Output Pin[Note]
0	0	Normal operation	Hi-Z
0	1	Normal operation	Normal operation
1	–	Normal operation	No Hi-Z output

Note 3-state pins are DO7 to DO0.

3. When CSE = "0", the Hi-Z status of the 3-state output buffer can be checked by monitoring the output value of the corresponding output control signal.

"Hi-Z" Pin	Corresponding Output Control Signal and Output	
DO7 to DO0	CDB	0

When CSE = "1", the status of the buffer is not affected by the 3-state output control signal (the 3-state output does not go into a "Hi-Z" state).

4. CSE and CSD can be fixed by clamping. Fix CSD to 1 when clamping it.

Remarks 5. Operating status of output pin depending on combination of TTHR, CSE, and CSD

TTHR Pin	CSE Pin	CSD Pin	3-State Output Pin (DOx)	3-State Control Pin (CDB(SD))	Other Pins	Through Path Dedicated Pin (Output THRxxx)
0	0	0	Hi-Z	0	Normal operation	0
		1	Normal operation	Normal operation		
	1	0	No Hi-Z output	0		
		1		Normal operation		
1	0	0	Hi-Z	Through path	Through path	Through path
		1	Through path			
	1	×				

6. I/O pin correspondence table in through path test

The input pins corresponding to the mega macro output pins when TTHR = “1” are as follows:

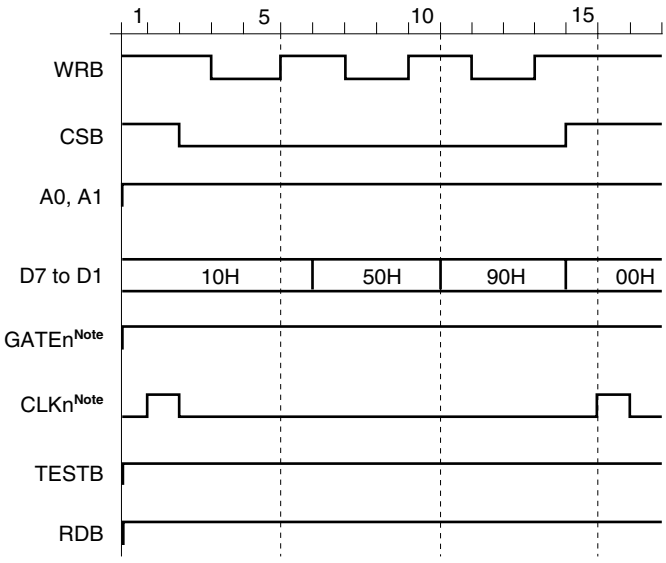
Output Pin	Through Path Corresponding Pin	
	TESTB = 1	TESTB = 0
DO0	DI0	TBI0
DO1	DI1	TBI1
DO2	DI2	TBI2
DO3	DI3	TBI3
DO4	DI4	TBI4
DO5	DI5	TBI5
DO6	DI6	TBI6
DO7	DI7	TBI7
CNTOUT0	CLK0	TBI8
CNTOUT1	CLK1	TBI9

Output Pin	Through Path Corresponding Pin	
	TESTB = 1	TESTB = 0
CNTOUT2	CLK2	TBI10
CDB	A0	TBI11
THRA1	A1	TBI12
THRGATE0	GATE0	TBI13
THRGATE1	GATE1	TBI14
THRGATE2	GATE2	TBI15
THRWR	WRB	TBI16
THRRD	RDB	TBI17
THRCS	CSB	TBI18

When TTHR = “1” and CSE = “0”, all the 3-state pins are controlled by CSD (selection between through path and high impedance).

4.2 NA54A Initialization Pattern

The internal status of the mega macro is undefined on starting simulation. Therefore, input the following initialization pattern to determine the internal status when executing simulation.



Example of initialization pattern

Mode setting is initialized.

[Example of setting counters #0 through #2 in mode 0]

Note n: 0, 1, or 2

Input “0” or “1” to the other input pins (normal input and test input).
Exercise care that “X” is not input.

- **Value of mega macro output pin after initialization pattern**

Mode	DO7 to DO0	CNTOUT2 to CNTOUT0	CDB	THRA1, THRGATE2 to THRGATE0, THRWR
0	Hi-Z	0	0	0
1	Hi-Z	1	0	0
2	Hi-Z	1	0	0
3	Hi-Z	1	0	0
4	Hi-Z	1	0	0
5	Hi-Z	1	0	0

Caution Configure the following input pins in a circuit that avoids spike input:
CLK0, CLK1, CLK2, GATE0, GATE1, GATE2, WRB, RDB
The values of CNTOUT2 to CNTOUT0 are output when the register of the corresponding counter is set. If the register is not set, the value is × (undefined).

4.3 Delay Time

Refer to **1.2.4 Delay time**.

4.4 AC Characteristics (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

(1) Read cycle

Parameter	Symbol	MIN.	MAX.	Unit
Address setup time (to RDB ↓)	t_{SAR}	5		ns
Address hold time (from RDB ↑)	t_{HRA}	0		ns
CSB setup time (to RDB ↓)	t_{SCR}	1		ns
Low-level RDB pulse width	t_{RRL}	30		ns
Data delay time (to RDB ↓)	t_{DRD}		35	ns
Data float delay time (to RDB ↑)	t_{FRD}	15	35	ns
Data delay time (to address)	t_{DAD}		40	ns
Read recovery time	t_{RV}	30		ns
CDB high delay time (to RDB ↓)	t_{CDHR}		35	ns
CDB low delay time (to RDB ↑)	t_{CDLR}		35	ns

(2) Write cycle

Parameter	Symbol	MIN.	MAX.	Unit
Address setup time (to WRB ↓)	t_{SAW}	0		ns
Address hold time (from WRB ↑)	t_{HWA}	0		ns
CSB setup time (to WRB ↓)	t_{SCW}	0		ns
Low-level WRB pulse width	t_{WWL}	30		ns
Data setup time (to WRB ↑)	t_{SDW}	10		ns
Data hold time (from WRB ↑)	t_{HWD}	0		ns
Write recovery time	t_{RV}	30		ns

(3) Clock, gate timing

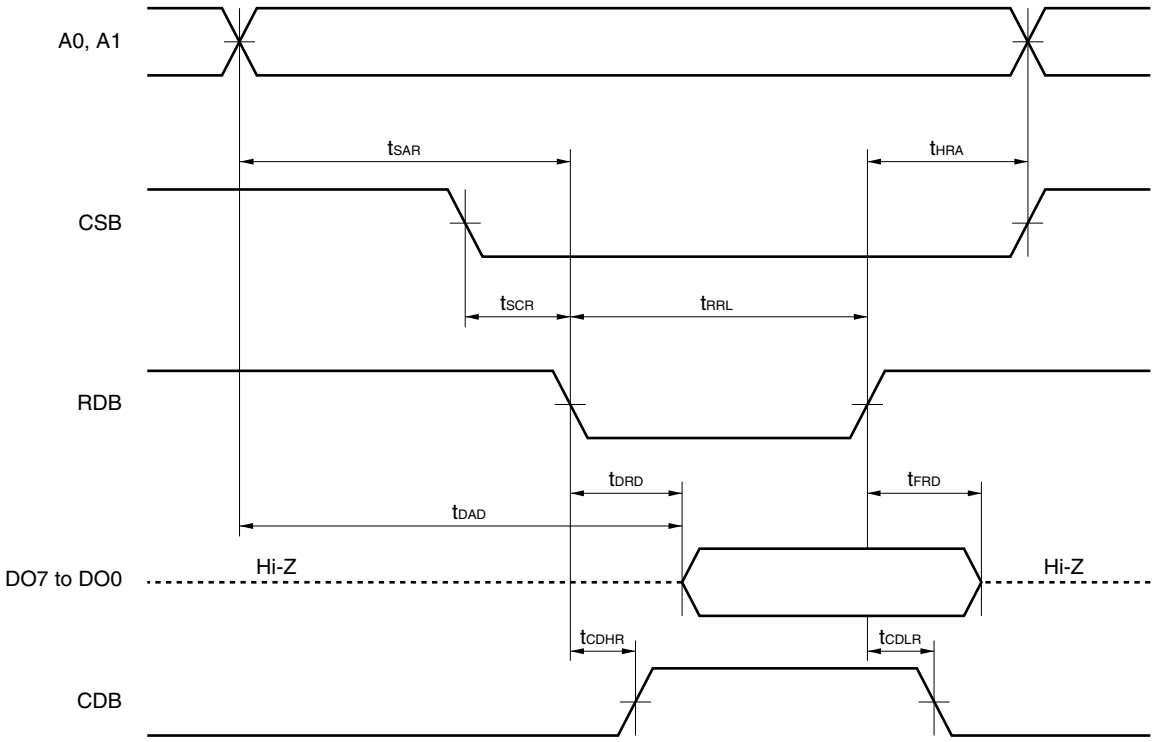
Parameter	Symbol	MIN.	MAX.	Unit
Clock cycle	t_{CYK}	30		ns
High-level clock pulse width	t_{KKH}	15		ns
Low-level clock pulse width	t_{KKL}	15		ns
High-level gate pulse width	t_{GGH}	10		ns
Low-level gate pulse width	t_{GGL}	10		ns
Gate setup time (to CLKn ↑)[Note]	t_{SGK}	20		ns
Gate hold time (from CLKn ↑)[Note]	t_{HKG}	0		ns
Clock delay time (to WRB ↑) (number of counts)	t_{DWK}	5		ns
Clock delay time (to WRB ↑) (latch command)	t_{SKW}	2		ns
Gate delay time (to WRB ↑)	t_{DWG}	0		ns
Output delay time (to GATEn ↓)[Note]	t_{DGO}		5	ns
Output delay time (to CLKn ↓)[Note]	t_{DKO}		10	ns
Output (initial OUT) delay time (to WRB ↑)	t_{DWO}		12	ns

Note n = 0, 1, or 2

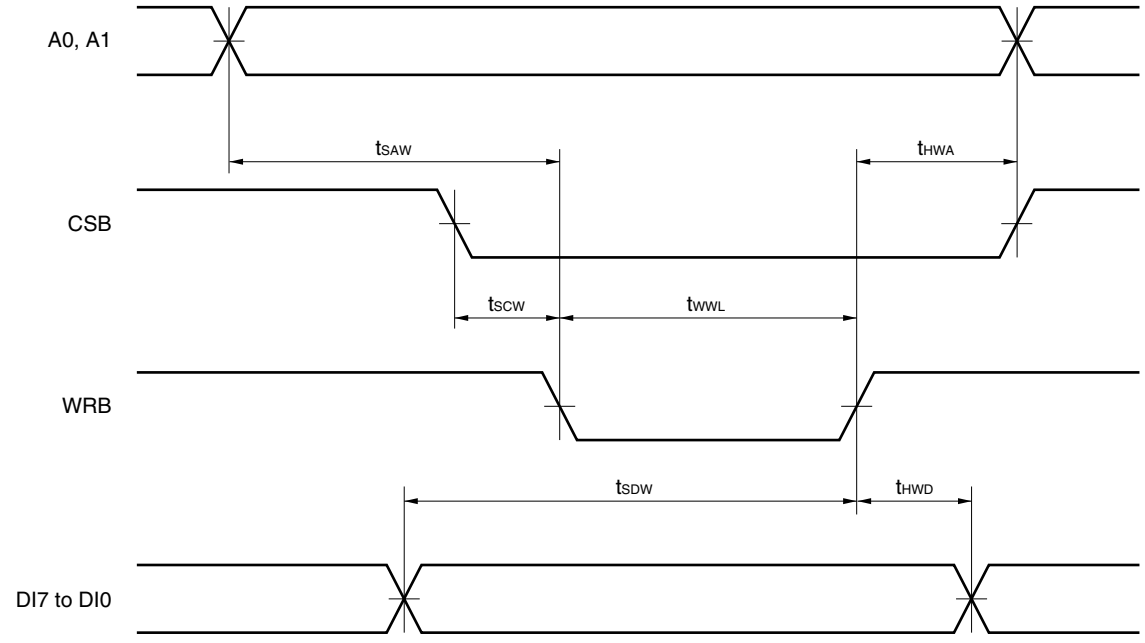
Remark The output load conditions of the propagation delay time are fanout: 1, wiring length: 0 mm.

4.5 Timing Charts

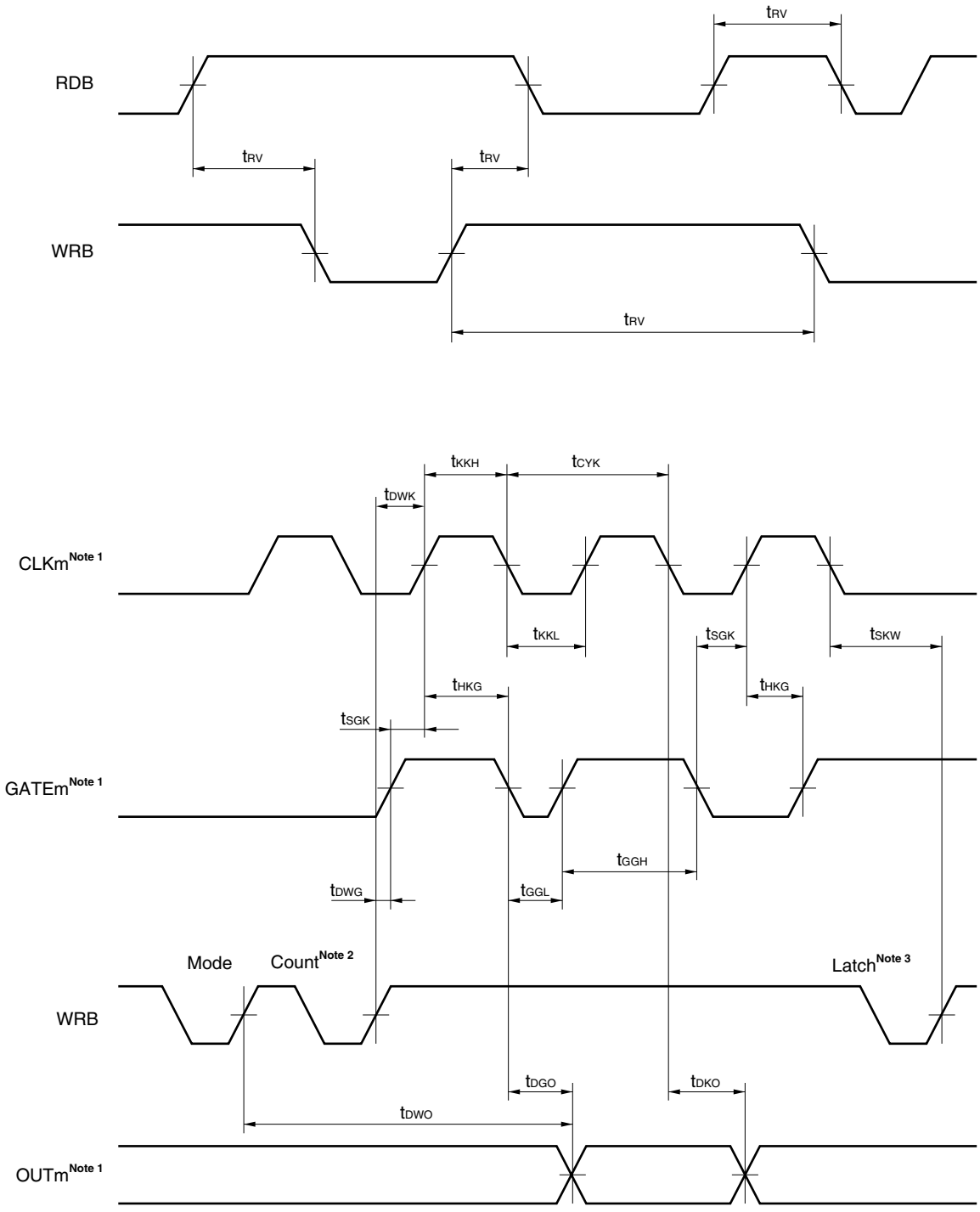
(1) Read cycle timing



(2) Write cycle timing



(3) Read/write recovery time



Notes 1. m = 0, 1, or 2

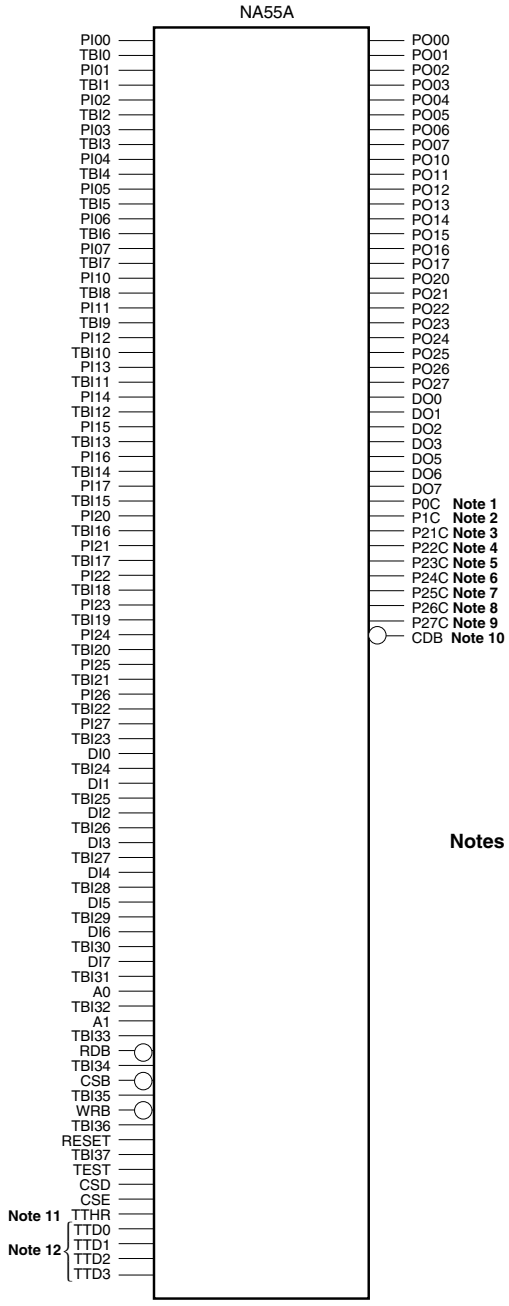
2. Writing of last byte of count number

3. Writing of count latch command or multiple latch command

CHAPTER 5 NA55A MACRO

This chapter explains the functions of the NA55A.

Block Type	Function
NA55A	Parallel Interface Unit



Features

- Compatible functions with μPD71055
- Maximum operating frequency: 20 MHz

Caution

- Do not input spike to WRB, RDB, and RESET.

Notes **1.** Output control signal of PO7 to PO0
2. Output control signal of PO17 to PO10
3. Output control signal of PO20 and PO21
4. Output control signal of PO22
5. Output control signal of PO23
6. Output control signal of PO24
7. Output control signal of PO25
8. Output control signal of PO26
9. Output control signal of PO27
10. Output control signal of DO7 to DO0
11. Through path/normal mode select pin
12. Through path mode dedicated input signal

Remark The input signal pins with “TBI” prefixed are test pins.

Number of cells used (configuration)	1764 (84 × 21)
Mega macro test pattern length	3643

5.1 NA55A Pins

Pin Name	I/O	Function	Test Pin	Fanin/ Fanout	Block Name
PI00	Input	Port 0 input (LSB)	TBI0	1.5	L424
PI01	Input	Port 0 input	TBI1	2.3	L424
PI02	Input	Port 0 input	TBI2	1.5	L424
PI03	Input	Port 0 input	TBI3	1.6	L424
PI04	Input	Port 0 input	TBI4	1.4	L424
PI05	Input	Port 0 input	TBI5	1.1	L424
PI06	Input	Port 0 input	TBI6	1.3	L424
PI07	Input	Port 0 input (MSB)	TBI7	1.4	L424
PI10	Input	Port 1 input (LSB)	TBI8	1.6	L424
PI11	Input	Port 1 input	TBI9	1.5	L424
PI12	Input	Port 1 input	TBI10	1.8	L424
PI13	Input	Port 1 input	TBI11	1.8	L424
PI14	Input	Port 1 input	TBI12	1.9	L424
PI15	Input	Port 1 input	TBI13	1.9	L424
PI16	Input	Port 1 input	TBI14	1.5	L424
PI17	Input	Port 1 input (MSB)	TBI15	1.7	L424
PI20	Input	Port 2 input (LSB)	TBI16	1.5	L424
PI21	Input	Port 2 input	TBI17	1.1	L424
PI22	Input	Port 2 input	TBI18	2.1	L424
PI23	Input	Port 2 input	TBI19	1.4	L424
PI24	Input	Port 2 input	TBI20	2.0	L424
PI25	Input	Port 2 input	TBI21	3.6	L424
PI26	Input	Port 2 input	TBI22	1.8	L424
PI27	Input	Port 2 input (MSB)	TBI23	3.5	L424
DI0	Input	Data bus input signal (LSB)	TBI24	1.5	L424
DI1	Input	Data bus input signal	TBI25	1.7	L424
DI2	Input	Data bus input signal	TBI26	1.5	L424
DI3	Input	Data bus input signal	TBI27	1.3	L424
DI4	Input	Data bus input signal	TBI28	1.5	L424
DI5	Input	Data bus input signal	TBI29	2.0	L424
DI6	Input	Data bus input signal	TBI30	1.2	L424
DI7	Input	Data bus input signal (MSB)	TBI31	1.8	L424
A0	Input	Address input	TBI32	1.6	L424
A1	Input	Address input	TBI33	1.5	L424
RDB	Input	Active “L” read signal	TBI34	1.5	L424
CSB	Input	Active “L” chip select signal	TBI35	1.4	L424
WRB	Input	Active “L” write signal	TBI36	1.4	L424
RESET	Input	System reset signal	TBI37	1.8	L424

Pin Name	I/O	Function	Test Pin	Fanin/ Fanout	Block Name
TEST	Input	Test/normal mode selection “H”: Normal mode “L”: Test mode	–	1.2	L111
CSD	Input	CSD = L PO27 to PO00 is forcibly output at Hi-Z	–	3.6	F153
CSE	Input	CSE = H PO27 to PO00 is not output at Hi-Z	–	1.7	F111
TTHR	Input	Through path/normal mode select signal “H”: Through path mode “L”: Normal mode	–	2.2	F112
TTD0	Input	Through path mode dedicated input pin	–	3.9	L111
TTD1	Input	Through path mode dedicated input pin	–	1.8	L111
TTD2	Input	Through path mode dedicated input pin	–	1.7	L111
TTD3	Input	Through path mode dedicated input pin	–	1.2	L111
PO00	Output	Port 0 output (LSB)	–	31.0	F531
PO01	Output	Port 0 output	–	32.0	F531
PO02	Output	Port 0 output	–	32.0	F531
PO03	Output	Port 0 output	–	32.0	F531
PO04	Output	Port 0 output	–	32.0	F531
PO05	Output	Port 0 output	–	32.0	F531
PO06	Output	Port 0 output	–	31.0	F531
PO07	Output	Port 0 output (MSB)	–	30.0	F531
PO10	Output	Port 1 output (LSB)	–	34.0	F531
PO11	Output	Port 1 output	–	33.0	F531
PO12	Output	Port 1 output	–	34.0	F531
PO13	Output	Port 1 output	–	34.0	F531
PO14	Output	Port 1 output	–	33.0	F531
PO15	Output	Port 1 output	–	34.0	F531
PO16	Output	Port 1 output	–	34.0	F531
PO17	Output	Port 1 output (MSB)	–	34.0	F531
PO20	Output	Port 2 output (LSB)	–	34.0	F531
PO21	Output	Port 2 output	–	34.0	F531
PO22	Output	Port 2 output	–	34.0	F531
PO23	Output	Port 2 output	–	34.0	F531
PO24	Output	Port 2 output	–	34.0	F531
PO25	Output	Port 2 output	–	32.0	F531
PO26	Output	Port 2 output	–	31.0	F531
PO27	Output	Port 2 output (MSB)	–	32.0	F531
DO0	Output	Data bus output signal (LSB)	–	33.0	F531
DO1	Output	Data bus output signal	–	32.0	F531
DO2	Output	Data bus output signal	–	33.0	F531
DO3	Output	Data bus output signal	–	33.0	F531
DO4	Output	Data bus output signal	–	33.0	F531

Pin Name	I/O	Function	Test Pin	Fanin/ Fanout	Block Name
DO5	Output	Data bus output signal	–	32.0	F531
DO6	Output	Data bus output signal	–	32.0	F531
DO7	Output	Data bus output signal (MSB)	–	33.0	F531
P0C	Output	PO07 to PO00 output control signal	–	33.0	F101
P1C	Output	PO17 to PO10 output control signal	–	34.0	F101
P21C	Output	PO20 and PO21 output control signal	–	34.0	F101
P22C	Output	PO22 output control signal	–	34.0	F101
P23C	Output	PO23 output control signal	–	30.0	F101
P24C	Output	PO24 output control signal	–	33.0	F101
P25C	Output	PO25 output control signal	–	33.0	F101
P26C	Output	PO26 output control signal	–	34.0	F101
P27C	Output	PO27 output control signal	–	33.0	F101
CDB	Output	DO7 to DO0 output control signal	–	31.0	F101
TBI0	Input	Test input	–	1.5	L424
TBI1	Input	Test input	–	2.4	L424
TBI2	Input	Test input	–	1.5	L424
TBI3	Input	Test input	–	1.6	L424
TBI4	Input	Test input	–	1.4	L424
TBI5	Input	Test input	–	1.1	L424
TBI6	Input	Test input	–	1.3	L424
TBI7	Input	Test input	–	1.4	L424
TBI8	Input	Test input	–	1.6	L424
TBI9	Input	Test input	–	2.1	L424
TBI10	Input	Test input	–	1.8	L424
TBI11	Input	Test input	–	1.9	L424
TBI12	Input	Test input	–	1.8	L424
TBI13	Input	Test input	–	1.9	L424
TBI14	Input	Test input	–	1.5	L424
TBI15	Input	Test input	–	1.7	L424
TBI16	Input	Test input	–	1.6	L424
TBI17	Input	Test input	–	1.2	L424
TBI18	Input	Test input	–	2.2	L424
TBI19	Input	Test input	–	1.5	L424
TBI20	Input	Test input	–	2.2	L424
TBI21	Input	Test input	–	3.7	L424
TBI22	Input	Test input	–	1.5	L424
TBI23	Input	Test input	–	3.5	L424
TBI24	Input	Test input	–	1.5	L424
TBI25	Input	Test input	–	1.7	L424
TBI26	Input	Test input	–	1.5	L424
TBI27	Input	Test input	–	1.3	L424

Pin Name	I/O	Function	Test Pin	Fanin/ Fanout	Block Name
TBI28	Input	Test input	–	1.4	L424
TBI29	Input	Test input	–	2.1	L424
TBI30	Input	Test input	–	1.2	L424
TBI31	Input	Test input	–	1.8	L424
TBI32	Input	Test input	–	1.6	L424
TBI33	Input	Test input	–	1.6	L424
TBI34	Input	Test input	–	1.6	L424
TBI35	Input	Test input	–	2.0	L424
TBI36	Input	Test input	–	1.5	L424
TBI37	Input	Test input	–	1.8	L424

Remarks 1. Txxx is a test input pin. A signal can be input from Txxx by making the TEST input low. Connect pins so that signals can be directly input to the mega macro from outside the gate array in test mode. "Directly" here means circuit configuration where the input signal is not inverted or no sequential circuit such as a flip-flop is inserted between the pins.

TEST	Input Pin
1	I x x x[Note]
0	T x x x

Note Input a defined value of 0 or 1 to the test input pins in normal mode (it does not matter if 0 and 1 are mixed).

2. Functions of CSE input and CSD input

CSE input: Turns on (high or low level) all the 3-state outputs when "1" is input to this pin.

CSD input: Turns off (high-impedance: Hi-Z) of all the 3-state outputs when "0" is input to this pin while CSE = "0".

When "1" is input, the 3-state outputs are turned on/off by an internal control signal of the mega macro (normal operation).

CSE	CSD	Status of Output Pin	Status of 3-State Output Pin[Note]
0	0	Normal operation	Hi-Z
0	1	Normal operation	Normal operation
1	–	Normal operation	No Hi-Z

Note 3-state pins are N01 to N32.

3. When CSE = "0", the Hi-Z status of the 3-state output buffer can be checked by monitoring the output value of the corresponding output control signal.

"Hi-Z" Pin	Corresponding Output Control Signal and Output	
PO07 to PO00	P0C	0
PO17 to PO10	P1C	0
PO20, PO21	P21C	0
PO22	P22C	0
PO23	P23C	0
PO24	P24C	0
PO25	P25C	0
PO26	P26C	0
PO27	P27C	0
DO7 to DO0	CDB	0

When CSE = "1", the status of the buffer is not affected by the 3-state output control signal (the 3-state output does not go into a "Hi-Z" state).

4. CSE and CSD can be fixed by clamping. Fix CSD to 1 when clamping it.

Remarks 5. Operating status of output pin depending on combination of TTHR, CSE, and CSD

TTHR Pin	CSE Pin	CSD Pin	3-State Output Pin	3-State Control Pin	Other Pins	Through Path Dedicated Pin
0	0	0	Hi-Z	0	Normal operation	0
		1	Normal operation	Normal operation		
	1	0	No Hi-Z output	0		
		1		Normal operation		
1	0	0	Hi-Z	Through path	Through path	Through path
		1	Through path			
	1	×				

6. I/O pin correspondence table in through path test

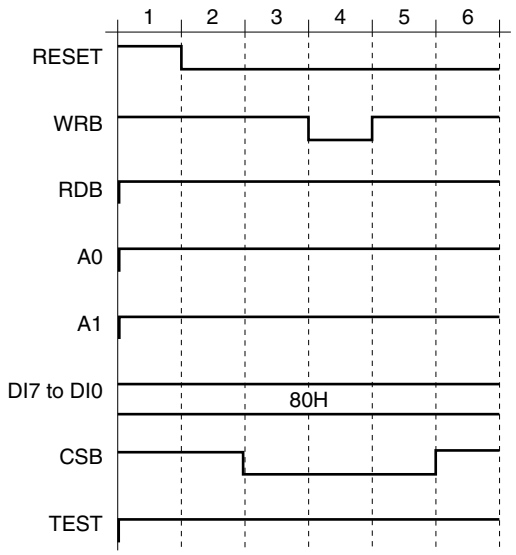
The input pins corresponding to the mega macro output pins when TTHR = “1” are as follows:

Output Pin	Through Path Corresponding Pin		Output Pin	Through Path Corresponding Pin		Output Pin	Through Path Corresponding Pin	
	TEST = 1	TEST = 0		TEST = 1	TEST = 0		TEST = 1	TEST = 0
PO00	PI00	TBI0	PO16	PI16	TBI14	DO4	DI4	TBI28
PO01	PI01	TBI1	PO17	PI17	TBI15	DO5	DI5	TBI29
PO02	PI02	TBI2	PO20	PI20	TBI16	DO6	DI6	TBI30
PO03	PI03	TBI3	PO21	PI21	TBI17	DO7	DI7	TBI31
PO04	PI04	TBI4	PO22	PI22	TBI18	P0C	A0	TBI32
PO05	PI05	TBI5	PO23	PI23	TBI19	P1C	A1	TBI33
PO06	PI06	TBI6	PO24	PI24	TBI20	P21C	RDB	TBI34
PO07	PI07	TBI7	PO25	PI25	TBI21	P22C	CSB	TBI35
PO10	PI10	TBI8	PO26	PI26	TBI22	P23C	WRB	TBI36
PO11	PI11	TBI9	PO27	PI27	TBI23	P24C	RESET	TBI37
PO12	PI12	TBI10	DO0	DI0	TBI24	P25C	TTD0	
PO13	PI13	TBI11	DO1	DI1	TBI25	P26C	TTD1	
PO14	PI14	TBI12	DO2	DI2	TBI26	P27C	TTD2	
PO15	PI15	TBI13	DO3	DI3	TBI27	CDB	TTD3	

When TTHR = “1” and CSE = “0”, all 3-state pins are controlled by CSD (selection between through path and high impedance).

5.2 NA55A Initialization Pattern

The internal status of the mega macro is undefined on starting simulation. Therefore, input the following initialization pattern to determine the internal status when executing simulation.



Example of initialization pattern

Be sure to set the mode select command after reset input for initialization.

Example of setting command to 80H after reset. The status of the output pin after initialization is indicated in the * column in Tables 5-1 and 5-2.

Input “0” or “1” to the other input pins (normal input and test input).

Be sure that X is not input.

Table 5-1. Status of Output Pin Immediately After Mode Select Command Setting (Group 0)

	Mode	Port 0	Port 2 (Higher)	PO07 to PO00	PO27	PO26	PO25	PO24	PO23[Note 1]
	0	Input	Input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	–
	0	Input	Output	Hi-Z	0	0	0	0	–
	0	Output	Input	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	–
*	0	Output	Output	0	0	0	0	0	–
	1	Input	Input	Hi-Z	Hi-Z	Hi-Z	Undefined or 1[Note 2]	Hi-Z	0
	1	Input	Output	Hi-Z	0	0	Undefined or 1[Note 2]	Hi-Z	0
	1	Output	Input	0	1	Hi-Z	Hi-Z	Hi-Z	0
	1	Output	Output	0	1	Hi-Z	0	0	0
	2	bidirection	Input	Hi-Z or 0[Note 3]	1	Hi-Z	Undefined or 1[Note 2]	Hi-Z	0
	2	bidirection	Output	Hi-Z or 0[Note 3]	1	Hi-Z	Undefined or 1[Note 2]	Hi-Z	0

Table 5-2. Status of Output Pin Immediately After Mode Select Command Setting (Group 1)

Mode	Port 1	Port 2 (Lower)	PO17 to PO10	PO23[Note 1]	PO22	PO21	PO20
0	Input	Input	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	Input	Output	Hi-Z	0	0	0	0
0	Output	Input	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
* 0	Output	Output	0	0	0	0	0
1	Input	Input	Hi-Z	Hi-Z	Hi-Z	Undefined or 1[Note 4]	0
1	Input	Output	Hi-Z	0	Hi-Z	Undefined or 1[Note 4]	0
1	Output	Input	0	Hi-Z	Hi-Z	1	0
1	Output	Output	0	1	Hi-Z	1	10

Notes 1. The operation of PO23 is as shown in Table 5-2 when group 0 is in mode 0, and as shown in Table 5-1 when group 0 is in mode 1 or mode 2.

2. Undefined when PI24 = 1, 1 when PI24 = 0

3. Hi-Z when PI26 = 1, 0 when PI26 = 0

4. Undefined when PI22 = 1, 1 when PI22 = 0

Remark DO7 to DO0 are always Hi-Z.

Cautions 1. Configure the following input pins in a circuit that avoids spike input: WRB, RDB, RESET.

2. When setting values as described in Note 2 of Table 5-1 or Note 4 of Table 5-2 for actual use, write the same command in succession.
When performing the second writing with PI24 = 0 (PI22 = 0), PO25 (PO21) is initialized.

3. When port 0 is set to mode 0 or mode 1 output for reading the port output value, connect the port 0 output of PO07 to PO00 to the port 0 input of PI07 to PI00 via the bus. Port 1 and port 2 are not required for the above connection.

5.3 Delay Time

Refer to **1.2.4 Delay time**.

5.4 AC Characteristics (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

(1) Read cycle

Parameter	Symbol	MIN.	MAX.	Unit
Address (CSB, A1, A0) setting time (to RDB↓)	t_{SAR}	0		ns
Address (CSB, A1, A0) hold time (from RDB↑)	t_{HRA}	0		ns
RDB pulse width	t_{RRL}	35		ns
Data delay time (to RDB↓)	t_{DRD}		35	ns
CDB high delay time (to RDB↓)	t_{CDHR}		35	ns
Data float delay time (to RDB↑)	t_{FRD}	10	35	ns
CDB low delay time (to RDB↑)	t_{CDLR}		30	ns
Read recovery time	t_{RV}	70		ns

(2) Write cycle

Parameter	Symbol	MIN.	MAX.	Unit
Address (CSB, A1, A0) setting time (to WRB↓)	t_{SAW}	0		ns
Address (CSB, A1, A0) hold time (to WRB↑)	t_{HWA}	0		ns
WRB pulse width	t_{WWL}	35		ns
Data setting time (to WRB↑)	t_{SDW}	10		ns
Data hold time (from WRB↑)	t_{HWD}	0		ns
Write recovery time	t_{RV}	70		ns

(3) Other timing

Parameter	Symbol	MIN.	MAX.	Unit
Port setting time (to RDB↓)	t_{SPR}	0		ns
Port hold time (from RDB↑)	t_{HRP}	0		ns
Port setting time (to STB↑)	t_{SPS}	0		ns
Port hold time (from STB↑)	t_{HSP}	10		ns
Port delay time (to WRB↑)	t_{DWP}		10	ns
STB pulse width	t_{SSL}	35		ns
DAKB pulse width	t_{DADAL}	35		ns
Port delay time (to DAKB↓)[Note 1]	t_{DDAP}		60	ns
CP0 high delay time (to DAKB↓)	t_{DCP0H}		60	ns
Port float time (to DAKB↑)[Note 1]	t_{FDAP}		60	ns
<R> CP0 low delay time (to DAKB↑)	t_{DCP0L}	16	60	ns
OBFB set delay time (to WRB↑)	t_{DWOB}		30	ns
OBFB clear delay time (to DAKB↓)	t_{DDAOB}		60	ns
IBF set delay time (to STB↓)	t_{DSIB}		30	ns
IBF clear delay time (to RDB↑)	t_{DRIB}		20	ns
INT set delay time (to DAKB↑)	t_{DDAI}		7	ns
INT clear delay time (to WRB↓)	t_{DWI}		30	ns
INT set delay time (to STB↑)	t_{DSI}		30	ns
INT clear delay time (to RDB↓)	t_{DRI}		20	ns
RESET pulse width	t_{RESET2}[Note 2]	70		ns

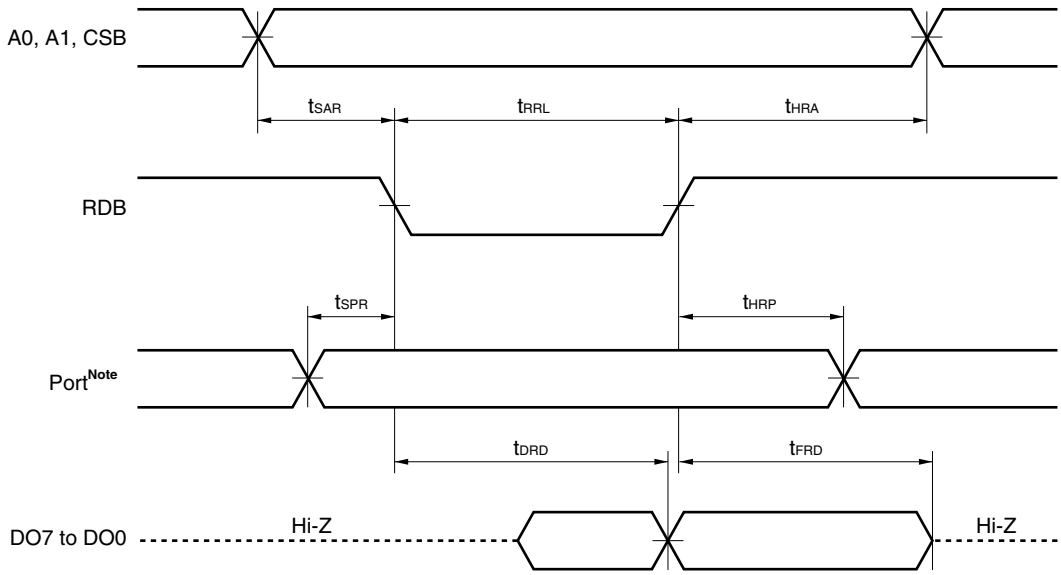
Notes 1. Mode 2

2. During operation

Remark The output load conditions of the propagation delay time are fanout = 1, wiring length = 0 mm.

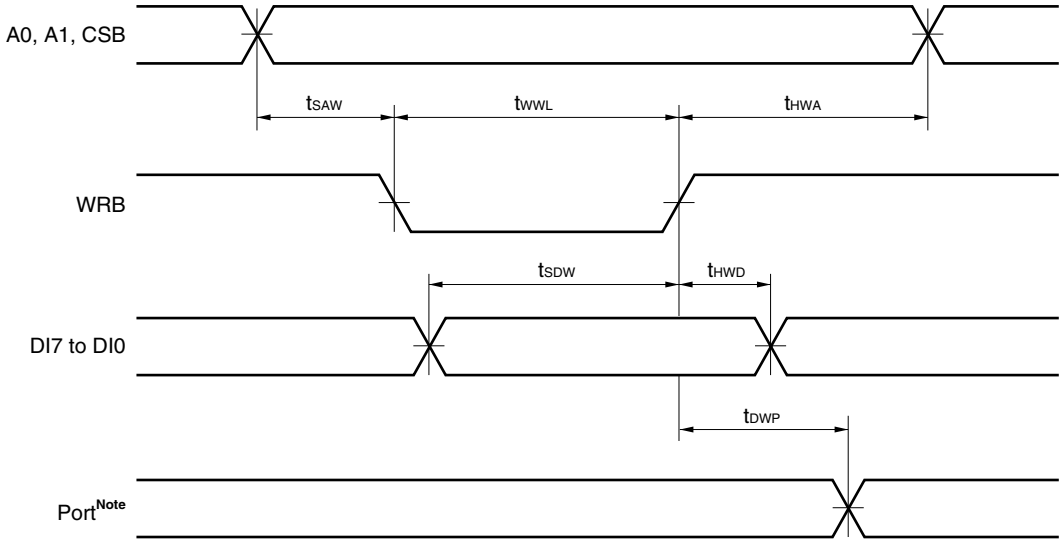
5.5 Timing Charts

(1) Mode 0: Input



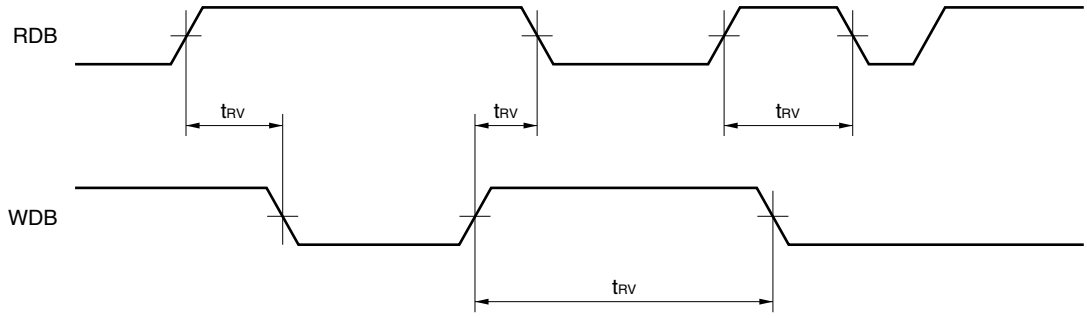
Note Ports are PI07 to PI00, PI17 to PI10, or PI27 to PI20.

(2) Mode 0: Output

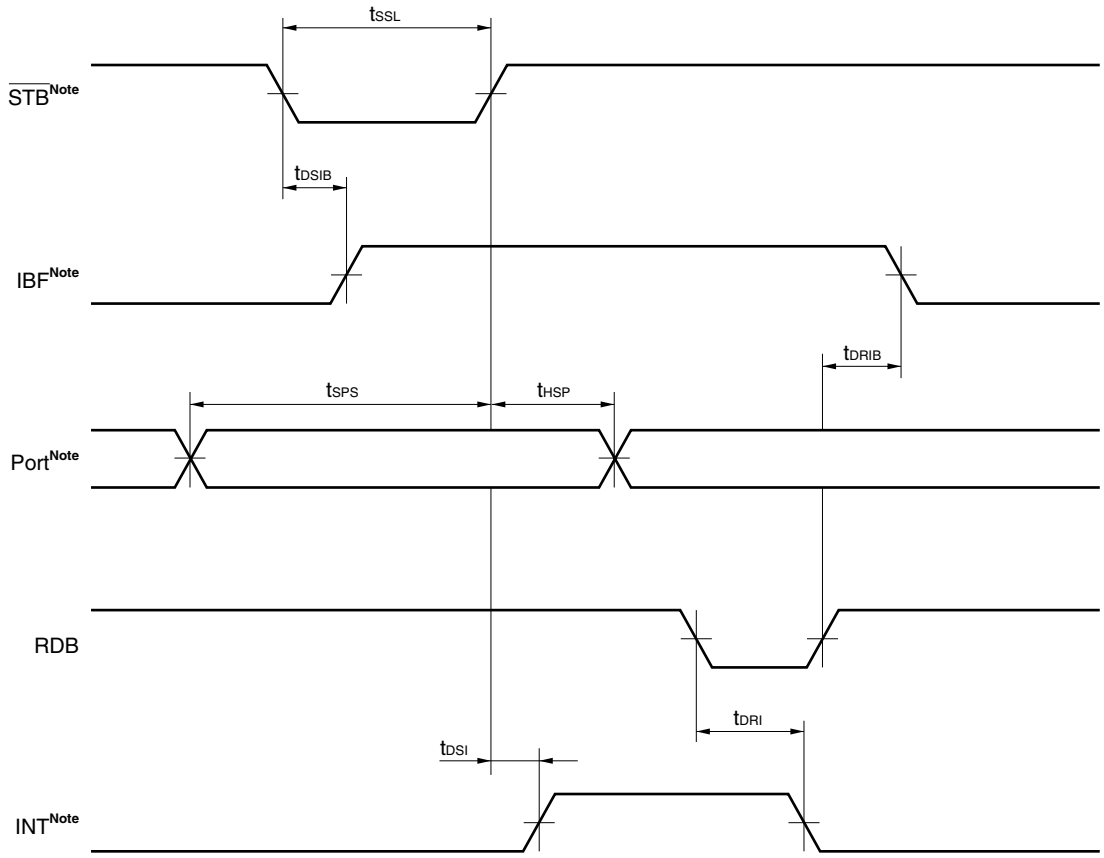


Note Ports are PO07 to PO00, PO17 to PO10, or PO27 to PO20.

(3) Recovery time

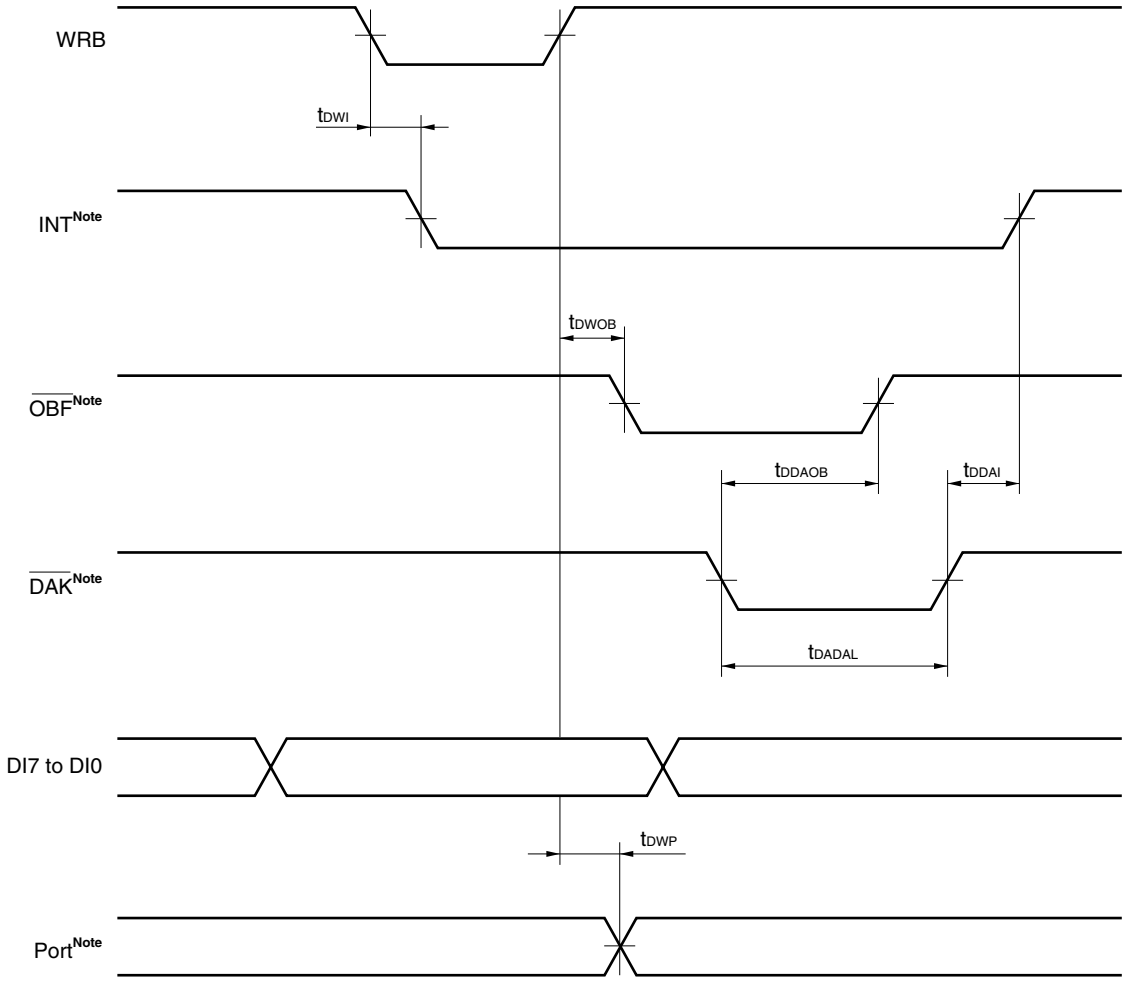


(4) Mode 1: Input



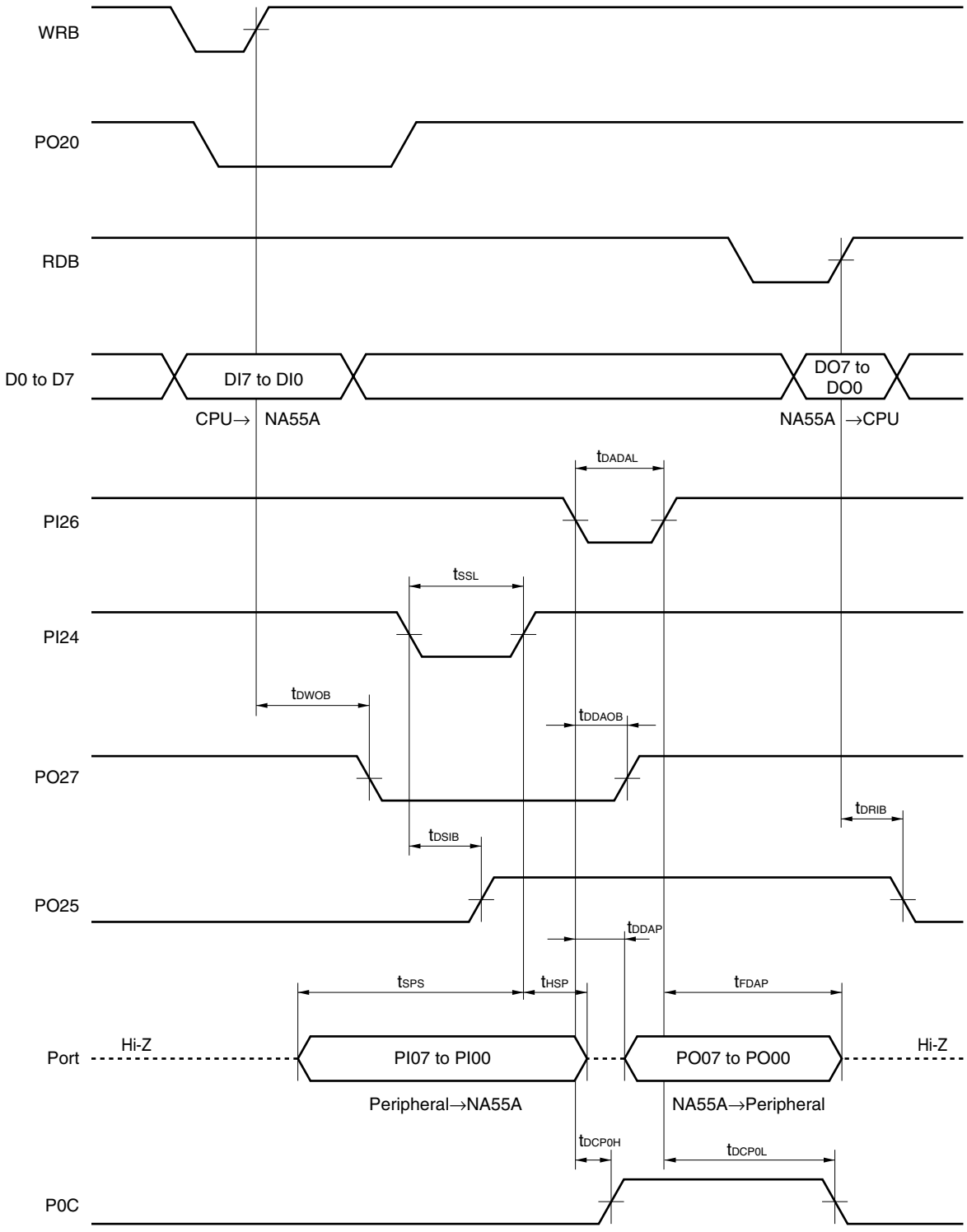
Note $\overline{\text{STB}}$ is PI22 or PI24.
IBF is PO21 or PO25.
Ports are PO07 to PO00 or PO17 to PO10.
INT is PO20 or PO23.

(5) Mode 1: Output



Remark INT is PO20 or PO23.
$\overline{\text{OBF}}$ is PO21 or PO27.
$\overline{\text{DAK}}$ is PI22 or PI26.
Ports are PO07 to PO00 or PO17 to PO10.

<R> **(6) Mode 2**

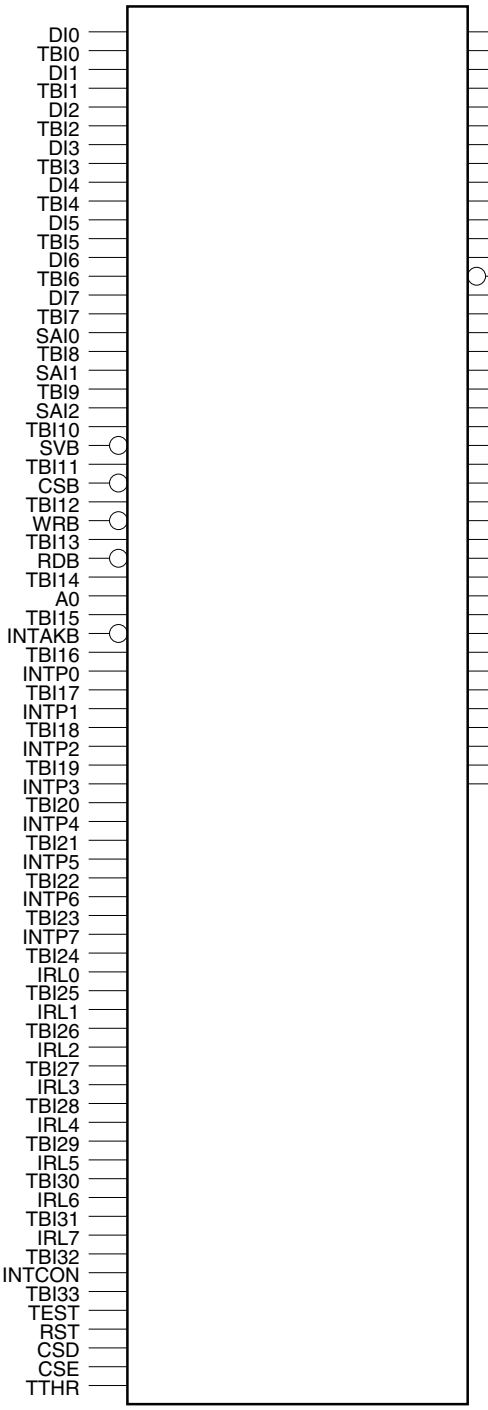

WRB
PO20
RDB
D0 to D7
DI7 to DI0
DO7 to DO0
CPU→ NA55A
NA55A →CPU
tDADAL
PI26
tSSL
PI24
tDWOB
tDDAOB
PO27
tDRIB
tDSIB
PO25
tDDAP
tSPS
tHSP
tFDAP
Port
Hi-Z
PI07 to PI00
PO07 to PO00
Hi-Z
Peripheral→NA55A
NA55A→Peripheral
tDCP0H
tDCP0L
P0C

CHAPTER 6 NA59A MACRO

This chapter explains the functions of the NA59A.

Block Type	Function
NA59A	Interrupt Control Unit

NA59A



Features

- Compatible functions with μPD71059 (some functions differ from the functions of μPD71059. For details, refer to **6.6 Differences Between NA59A and μPD71059**.)
- Maximum operating frequency: 33 MHz or equivalent

Caution

- Do not input spike to WRB, RDB, INTAKB, INTP7 through INTP0, and RST.

Notes 1. Output control signal of DO7 through DO0
2. Output control signal of SAO2 through SAO0
3. Output control signal of SVO
4. Through path dedicated output pins of CSB, WRB, RDB, A0, and INTP7 through INTP3 in the pre-/post-mega-macro stage test

Remark The input signal pins with "TBI" prefixed are test pins.

Number of cells used (configuration)	2349 (87 × 27)
Mega macro test pattern length	7334

6.1 NA59A Pins

Pin Name	I/O	Function	Active Level	Test Pin	Fanin/ Fanout	Block Name
DI0	Input	Data bus input signal (LSB)		TBI0	1.9	L424
DI1	Input	Data bus input signal		TBI1	1.1	L424
DI2	Input	Data bus input signal		TBI2	1.7	L424
DI3	Input	Data bus input signal		TBI3	2.6	L424
DI4	Input	Data bus input signal		TBI4	1.1	L424
DI5	Input	Data bus input signal		TBI5	1.5	L424
DI6	Input	Data bus input signal		TBI6	1.3	L424
DI7	Input	Data bus input signal (MSB)		TBI7	1.6	L424
SAI0	Input	Slave address (LSB)		TBI8	1.7	L424
SAI1	Input	Slave address		TBI9	1.3	L424
SAI2	Input	Slave address (MSB)		TBI10	1.7	L424
SVB	Input	Slave input signal	Low	TBI11	2.0	L424
CSB	Input	Chip select signal	Low	TBI12	1.4	L424
WRB	Input	Write signal	Low	TBI13	1.5	L424
RDB	Input	Read signal	Low	TBI14	1.7	L424
A0	Input	Specifies command/data when RD or WR		TBI15	1.1	L424
INTAKB	Input	Interrupt acknowledge signal	Low	TBI16	1.5	L424
INTP0	Input	Interrupt request input signal (bit 0)		TBI17	1.1	L424
INTP1	Input	Interrupt request input signal (bit 1)		TBI18	1.1	L424
INTP2	Input	Interrupt request input signal (bit 2)		TBI19	1.1	L424
INTP3	Input	Interrupt request input signal (bit 3)		TBI20	1.5	L424
INTP4	Input	Interrupt request input signal (bit 4)		TBI21	1.1	L424
INTP5	Input	Interrupt request input signal (bit 5)		TBI22	1.5	L424
INTP6	Input	Interrupt request input signal (bit 6)		TBI23	2.0	L424
INTP7	Input	Interrupt request input signal (bit 7)		TBI24	1.7	L424
IRL0	Input	Level edge select signal (bit 0) H = trig		TBI25	1.1	L424
IRL1	Input	Level edge select signal (bit 1) H = trig		TBI26	1.5	L424
IRL2	Input	Level edge select signal (bit 2) H = trig		TBI27	1.5	L424
IRL3	Input	Level edge select signal (bit 3) H = trig		TBI28	1.1	L424
IRL4	Input	Level edge select signal (bit 4) H = trig		TBI29	1.1	L424
IRL5	Input	Level edge select signal (bit 5) H = trig		TBI30	1.9	L424
IRL6	Input	Level edge select signal (bit 6) H = trig		TBI31	1.4	L424
IRL7	Input	Level edge select signal (bit 7) H = trig		TBI32	1.1	L424
INTCON	Input	INT output select		TBI33	1.7	L424
TEST	Input	Test/normal mode select signal “H”: Normal mode “L”: Test mode		–	2.7	L101
CSD	Input	3-state output control		–	5.0	F112
RST	Input	Fix the value of OSV, CSA, CSV	High	–	2.3	L212

Pin Name	I/O	Function	Active Level	Test Pin	Fanin/ Fanout	Block Name
CSE	Input	3-state output control		–	1.4	L111
TTHR	Input	Through path/normal mode select signal “H”: Through path mode “L”: Normal mode		–	2.5	F111
DO0	Output	Data bus output signal (LSB)		–	30.0	F531
DO1	Output	Data bus output signal		–	30.0	F531
DO2	Output	Data bus output signal		–	31.0	F531
DO3	Output	Data bus output signal		–	31.0	F531
DO4	Output	Data bus output signal		–	30.0	F531
DO5	Output	Data bus output signal		–	30.0	F531
DO6	Output	Data bus output signal		–	31.0	F531
DO7	Output	Data bus output signal (MSB)		–	31.0	F531
SAO0	Output	Slave address output signal (LSB)		–	32.0	F531
SAO1	Output	Slave address output signal		–	32.0	F531
SAO2	Output	Slave address output signal (MSB)		–	32.0	F531
SVO	Output	Slave output enable		–	30.0	F531
INTR	Output	Interrupt request signal		–	32.0	F101
CDB	Output	Output control signal of DO7 to DO0		–	33.0	F101
CSA	Output	Output control signal of SAO2 to SAO0		–	31.0	F111
CSV	Output	Output control signal of SVO		–	31.0	F111
ESLC0	Output	Interrupt reset output 0 (H = RESET)		–	34.0	F101
ESLC1	Output	Interrupt reset output 1 (H = RESET)		–	33.0	F101
ESLC2	Output	Interrupt reset output 2 (H = RESET)		–	33.0	F101
ESLC3	Output	Interrupt reset output 3 (H = RESET)		–	33.0	F101
ESLC4	Output	Interrupt reset output 4 (H = RESET)		–	33.0	F101
ESLC5	Output	Interrupt reset output 5 (H = RESET)		–	33.0	F101
ESLC6	Output	Interrupt reset output 6 (H = RESET)		–	33.0	F101
ESLC7	Output	Interrupt reset output 7 (H = RESET)		–	34.0	F101
INTO0	Output	Interrupt output 0 (H = interrupt)		–	33.0	F101
INTO1	Output	Interrupt output 1 (H = interrupt)		–	30.0	F101
INTO2	Output	Interrupt output 2 (H = interrupt)		–	33.0	F101
INTO3	Output	Interrupt output 3 (H = interrupt)		–	32.0	F101
INTO4	Output	Interrupt output 4 (H = interrupt)		–	33.0	F101
INTO5	Output	Interrupt output 5 (H = interrupt)		–	34.0	F101
INTO6	Output	Interrupt output 6 (H = interrupt)		–	34.0	F101
INTO7	Output	Interrupt output 7 (H = interrupt)		–	33.0	F101
THRCSB	Output	Through path output pin		–	30.0	F312
THRWRB	Output	Through path output pin		–	33.0	F312
THRRDB	Output	Through path output pin		–	31.0	F312
THRA0	Output	Through path output pin		–	32.0	F312
THRINTP3	Output	Through path output pin		–	32.0	F312

Pin Name	I/O	Function	Active Level	Test Pin	Fanin/ Fanout	Block Name
THRINTP4	Output	Through path output pin		–	33.0	F312
THRINTP5	Output	Through path output pin		–	34.0	F312
THRINTP6	Output	Through path output pin		–	33.0	F312
THRINTP7	Output	Through path output pin		–	32.0	F312
TBI0	Input	Test input			1.9	L424
TBI1	Input	Test input			1.1	L424
TBI2	Input	Test input			1.9	L424
TBI3	Input	Test input			2.7	L424
TBI4	Input	Test input			1.2	L424
TBI5	Input	Test input			1.6	L424
TBI6	Input	Test input			1.3	L424
TBI7	Input	Test input			1.6	L424
TBI8	Input	Test input			1.7	L424
TBI9	Input	Test input			1.3	L424
TBI10	Input	Test input			1.7	L424
TBI11	Input	Test input			2.1	L424
TBI12	Input	Test input			1.4	L424
TBI13	Input	Test input			1.5	L424
TBI14	Input	Test input			1.7	L424
TBI15	Input	Test input			1.1	L424
TBI16	Input	Test input			1.5	L424
TBI17	Input	Test input			1.1	L424
TBI18	Input	Test input			1.2	L424
TBI19	Input	Test input			1.3	L424
TBI20	Input	Test input			1.5	L424
TBI21	Input	Test input			1.1	L424
TBI22	Input	Test input			1.6	L424
TBI23	Input	Test input			1.9	L424
TBI24	Input	Test input			1.7	L424
TBI25	Input	Test input			1.1	L424
TBI26	Input	Test input			1.4	L424
TBI27	Input	Test input			1.5	L424
TBI28	Input	Test input			1.3	L424
TBI29	Input	Test input			1.1	L424
TBI30	Input	Test input			1.8	L424
TBI31	Input	Test input			1.3	L424
TBI32	Input	Test input			1.1	L424
TBI33	Input	Test input			1.6	L424

Remark Input: Input pin
Output: Output pin

Remarks 1. TBIx is a test input pin. A signal can be input from TBIx by making the TEST input low. Connect pins so that signals can be directly input to the mega macro from outside the gate array in test mode. "Directly" here means a circuit configuration where the input signal is not inverted or no sequential circuit such as a flip-flop is inserted between the pins.

TEST	Input Pin
1	Normal pin[Note]
0	TBIx

Note Input a defined value of 0 or 1 to the test input pins in normal mode (it does not matter if 0 and 1 are mixed).

2. Functions of CSE input and CSD input

CSE input: Turns on (high or low level) all the 3-state outputs when "1" is input to this pin.

CSD input: Turns off (high-impedance: Hi-Z) all the 3-state outputs when "0" is input to this pin while CSE = "0".

When "1" is input, the 3-state outputs are turned on/off by an internal control signal of the mega macro (normal operation).

CSE	CSD	Status of Output Pin	Status of 3-State Output Pin[Note]
0	0	Normal operation	Hi-Z
0	1	Normal operation	Normal operation
1	–	Normal operation	No Hi-Z output

Note 3-state pins are DO7 to DO0, SAO2 to SAO0, and SVO.

3. When CSE = "0", the Hi-Z status of the 3-state output buffer can be checked by monitoring the output value of the corresponding output control signal.

"Hi-Z" Pin	Corresponding Output Control Signal and Output	
DO7 to DO0	CDB	0
SAO2 to SAO0	CSA	0
SVO	CSV	0

When CSE = "1", the status of the buffer is not affected by the 3-state output control signal (the 3-state output does not go into a "Hi-Z" state).

4. CSE and CSD can be fixed by clamping. Fix CSD to 1 when clamping it.

Remarks 5. Operating status of output pin depending on combination of TTHR, CSE, and CSD

TTHR Pin	CSE Pin	CSD Pin	3-State Output Pin (DOx)	3-State Control Pin (CDB(SD))	Other Pins	Through Path Dedicated Pin (Output THRxxx)
0	0	0	Hi-Z	0	Normal operation	0
		1	Normal operation	Normal operation		
	1	0	No Hi-Z output	0		
		1		Normal operation		
1	0	0	Hi-Z	Through path	Through path	Through path
		1	Through path			
	1	×				

6. I/O pin correspondence table in through path test

The input pins corresponding to the mega macro output pins when TTHR = “1” are as follows:

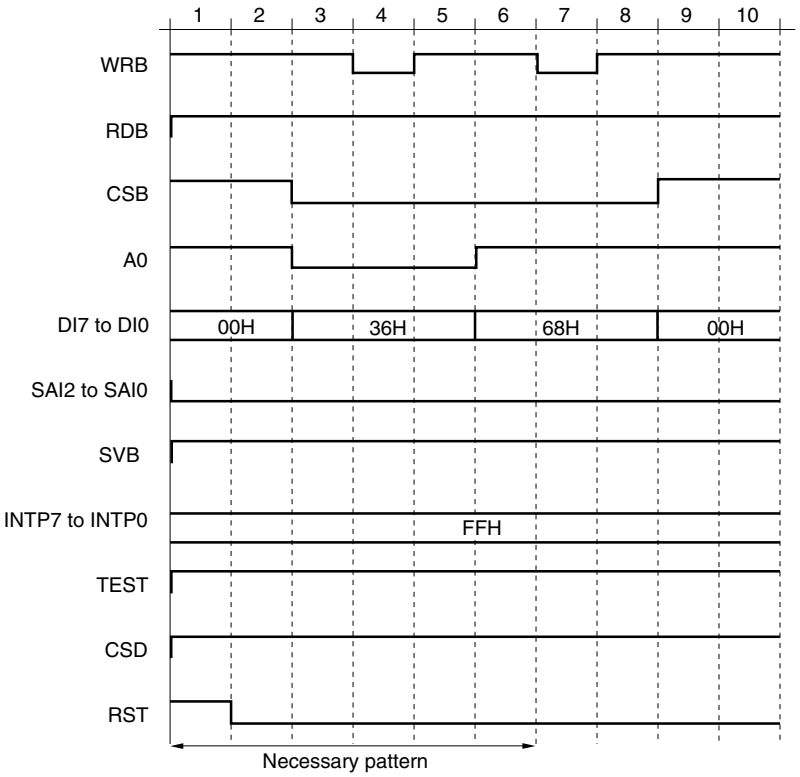
Output Pin	Through Path Corresponding Pin	
	TEST = 1	TEST = 0
DO0	DI0	TBI0
DO1	DI1	TBI1
DO2	DI2	TBI2
DO3	DI3	TBI3
DO4	DI4	TBI4
DO5	DI5	TBI5
DO6	DI6	TBI6
DO7	DI7	TBI7
SAO0	SAI0	TBI8
SAO1	SAI1	TBI9
SAO2	SAI2	TBI10
SVO	SVB	TBI11
INTR	INTAKB	TBI16

Output Pin	Through Path Corresponding Pin	
	TEST = 1	TEST = 0
CDB	INTP0	TBI17
CSA	INTP1	TBI18
CSV	INTP2	TBI19
THRCSB	CSB	TBI12
THRWRB	WRB	TBI13
THRRDB	RDB	TBI14
THRA0	A0	TBI15
THRINTP3	INTP3	TBI20
THRINTP4	INTP4	TBI21
THRINTP5	INTP5	TBI22
THRINTP6	INTP6	TBI23
THRINTP7	INTP7	TBI24

When TTHR = “1” and CSE = “0”, all the 3-state pins are controlled by CSD (selection between through path and high impedance).

6.2 NA59A Initialization Pattern

The internal status of the mega macro is undefined on starting simulation. Therefore, input the following initialization pattern to determine the internal status when executing simulation.



Example of initialization pattern

Be sure to input this pattern up to the second pattern for initialization. This initialization pattern sets the NA59A in the CALL mode, edge trigger mode, and single mode with an address gap of 4 bytes.
To use the vector mode or extended mode, set the third pattern and those that follow in the mode to be used.
For details of how to set the mode, refer to **Figures 4-2 Initialization Sequence** and **4-3 Initialization Word Format** in **4.1 Initialization Word** in the **μPD71059 Data Sheet (U11932J)** (Japanese version only) **Note**.

<R> **Note** Contact NEC Electronics if the related documents cannot be obtained.

Input “0” or “1” to the other input pins (normal input and test input).

Status of output pin after mode setting

Pin Name	Status
DO7 to DO0	Hi-Z
CDB	0
SAO2 to SAO0	0 (single mode and master mode) Hi-Z (slave mode)
CSA	1 (single mode and master mode) 0 (slave mode)
SVO	1 (buffer mode master) Hi-Z (buffer mode slave and non-buffer mode)
CSV	1 (buffer mode master) 0 (buffer mode slave and non-buffer mode)
INTR	0

Cautions 1. RST pin

The RST pin is peculiar to the NA59A. This pin makes the status of the NA59A the same as that of the standard model immediately after power application (when SVB = 1).

Be sure to input a signal of “1” to this pin for 10 ns or more immediately after power application, and input “0” to it after initialization.

By applying “1” to this pin, the output signals are determined as follows:

SVO ... Hi-Z

CSA ... 1

CSV ... 0

The other internal registers are not initialized.

2. Configure the following input pins in a circuit that avoids spike input:

WRB, RDB, INTAKB, INTP7 to INTP0, RST

6.3 Delay Time

Refer to **1.2.4 Delay time**.

6.4 AC Characteristics (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

(1) Read timing

Parameter	Symbol	MIN.	MAX.	Unit
Address setup time (to RDB ↓)[Note]	t_{SAR}	1		ns
Address hold time (from RDB ↑)[Note]	t_{HRA}	1		ns
Low-level RDB pulse width	t_{RRL}	30		ns
High-level RDB pulse width	t_{RRH}	30		ns
Data delay time (from CSB)	t_{DAD}		30	ns
Data delay time (from A0)	t_{DAD}		20	ns
Data delay time (from RDB ↓)	t_{DRD}		30	ns
CDB high delay time (from RDB ↓)	t_{CDHR}		25	ns
Data float time (from RDB ↑)	t_{FRD}	10	25	ns
CDB low delay time (from RDB ↑)	t_{CDLR}		25	ns
BUFR/W delay time (from RDB ↓)	t_{DRBL}		5	ns
BUFR/W delay time (from RDB ↑)	t_{DRBH}		5	ns

(2) Write timing

Parameter	Symbol	MIN.	MAX.	Unit
Address setup time (to WRB ↓)[Note]	t_{SAW}	1		ns
Address hold time (from WRB ↑)[Note]	t_{HWA}	1		ns
Low-level WRB pulse width	t_{WWL}	30		ns
High-level WRB pulse width	t_{WWH}	30		ns
Data setup time (to WRB ↑)	t_{SDW}	3		ns
Data hold time (from WRB ↑)	t_{HWD}	0		ns

Note “Address” means A0 and CSB.

(3) Interrupt timing

Parameter	Symbol	MIN.	MAX.	Unit
INTP pulse width[Note 1]	t_{IPIPL}	10		ns
SA setup time (2nd, 3rd INTAKB ↓) (slave)	t_{SSIA}	10		ns
Low-level INTAKB pulse width	t_{IAIAL}	30		ns
High-level INTAKB pulse width	t_{IAIAH}	30		ns
INT delay time (from INTP ↑)	t_{DIPI}		10	ns
SA delay time (from 1st INTAKB ↓) (master)	t_{DIAS}		10	ns
Data delay time (from INTAKB ↓)	t_{DIAD}		30	ns
CDB high delay time (from INTAKB ↓)	t_{CDHIA}		30	ns
Data float time (from INTAKB ↑)	t_{FIAD}	10	30	ns
CDB low delay time (from INTAKB ↑)	t_{CDLIA}		25	ns
Data delay time (from SA) (slave)	t_{DSD}		40	ns
BUFR/W delay time (from INTAKB ↓)	t_{DIABL}		5	ns
BUFR/W delay time (from INTAKB ↑)	t_{DIABH}		5	ns

(4) Other timing

Parameter	Symbol	MIN.	MAX.	Unit
Read/write recovery time[Note 2]	t_{RV1}	30		ns
INTAKB recovery time[Note 3]	t_{RV2}	30		ns
INTAKB/command recovery time[Note 4]	t_{RV3}	30		ns

Notes 1. Time necessary for clearing the input latch in the edge trigger mode

2. Time necessary for operation to change from read to write or from write to read

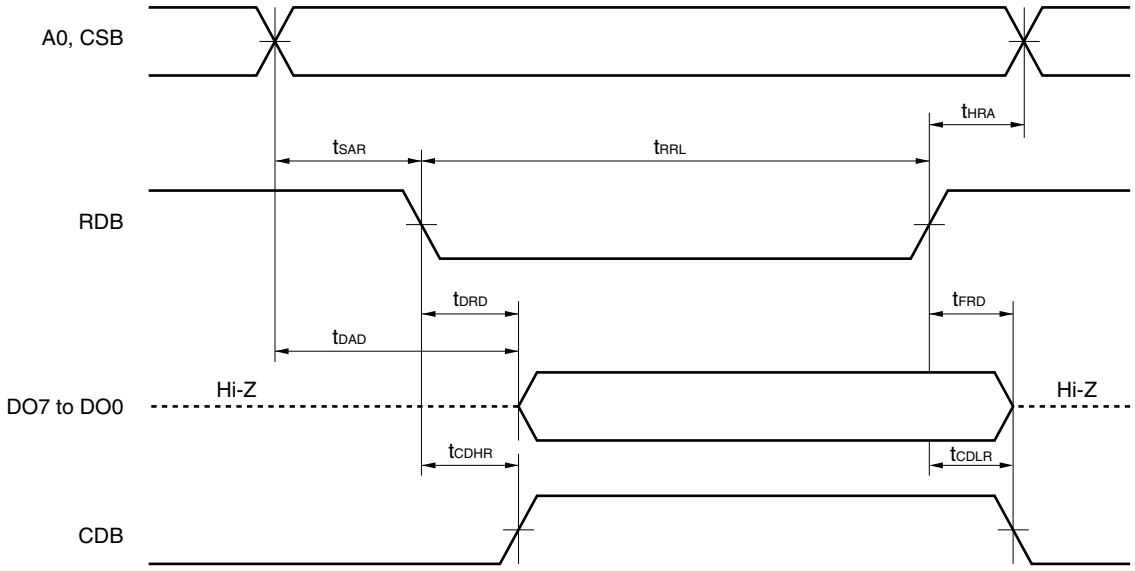
3. Time necessary to start the next INTAKB sequence from the last low pulse of an INTAKB sequence

4. Time necessary for operation to change from INTAKB to command (read/write) or from command to INTAKB

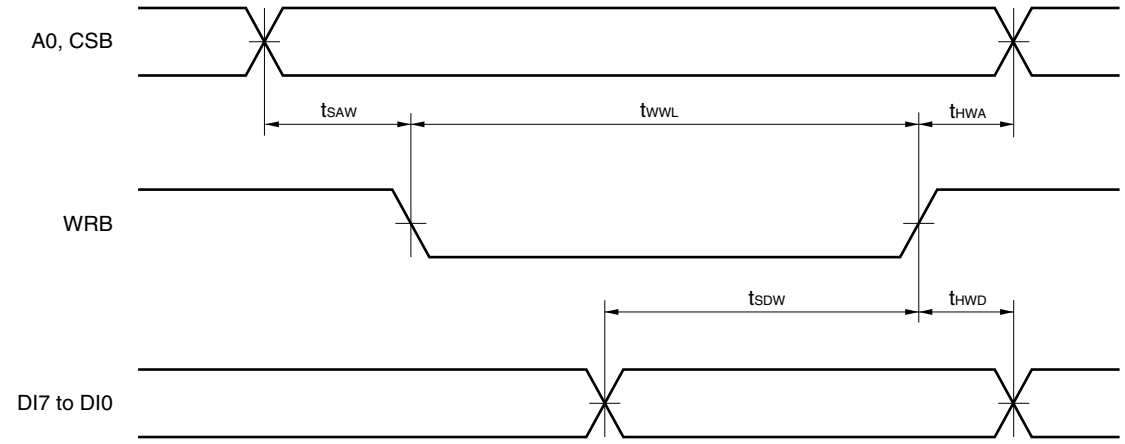
Remark The output load conditions of the propagation delay time are fanout: 1, wiring length: 0 mm.

6.5 Timing Charts

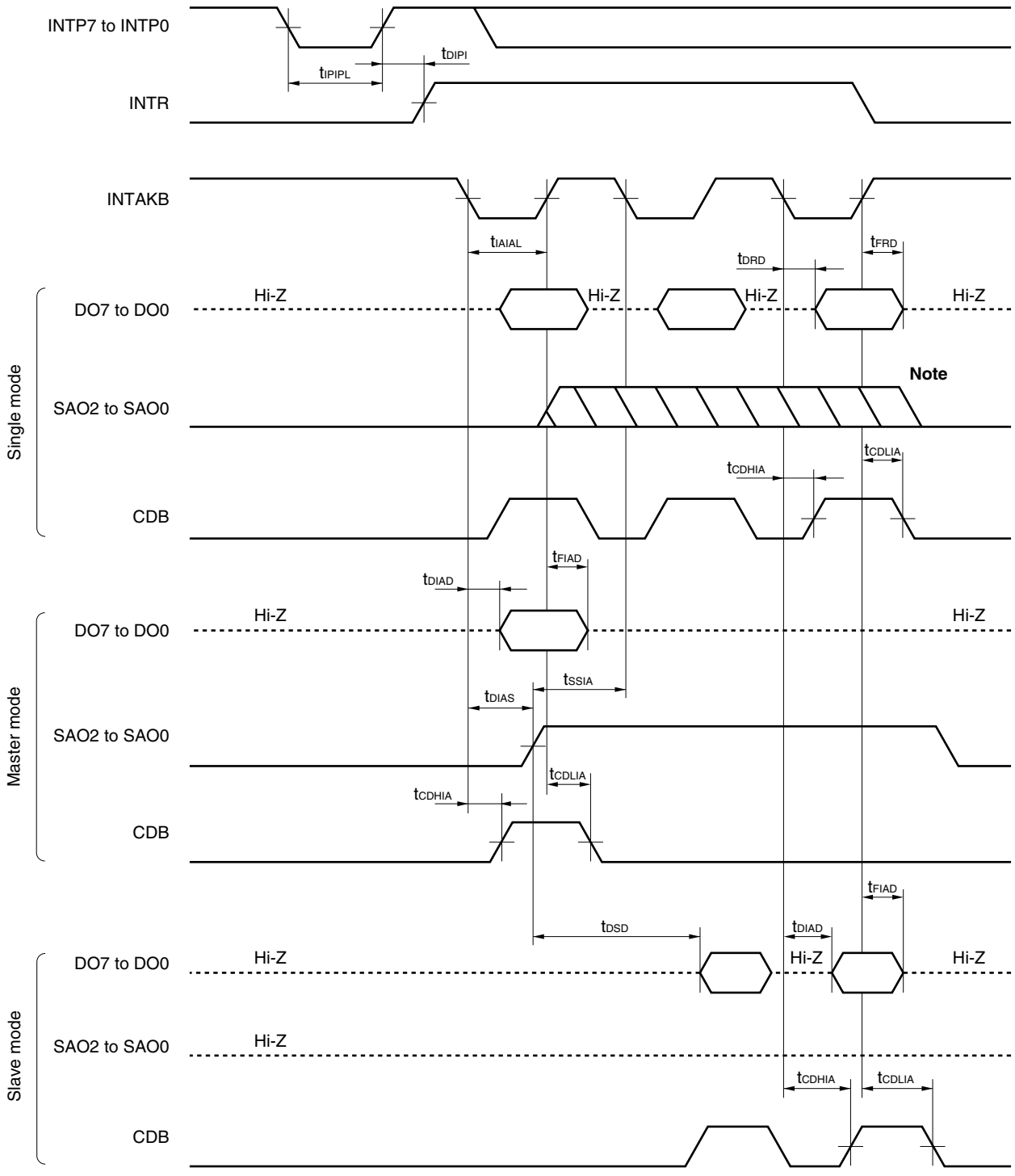
(1) Read cycle



(2) Write cycle

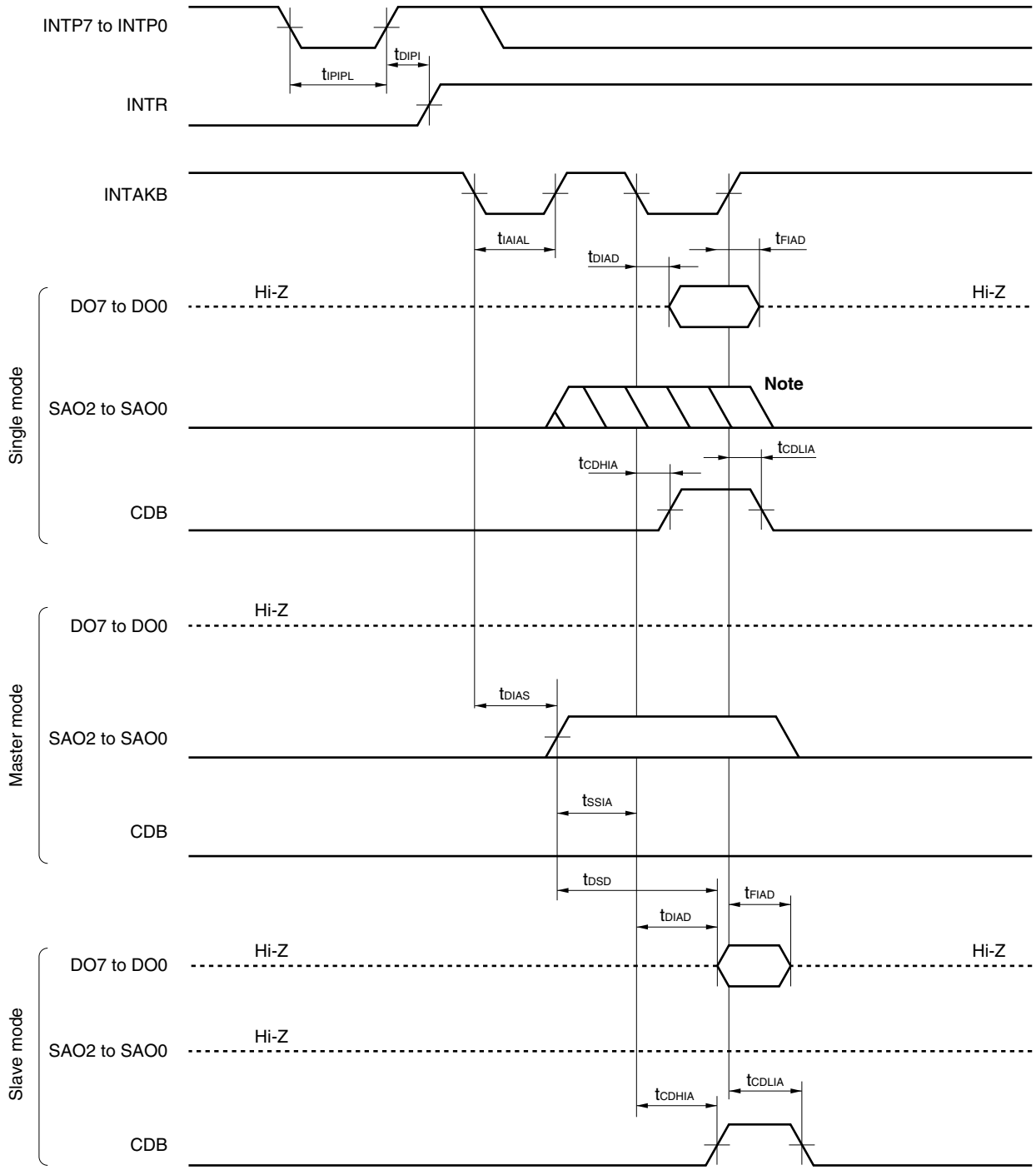


(3) INTAKB sequence (CALL mode) timing



Note SAO2 to SAO0 are output even in the single mode but are meaningless.

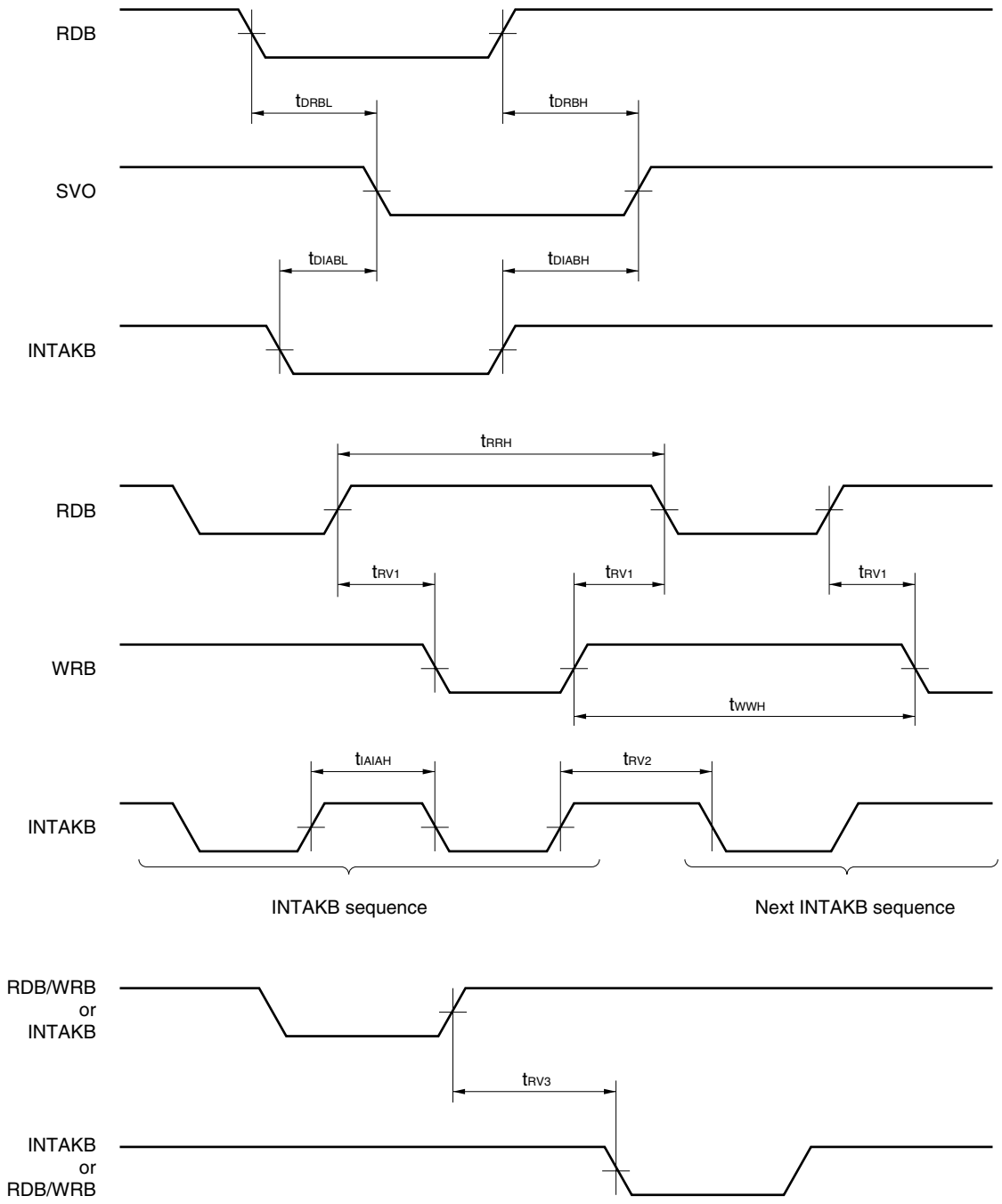
(4) INTAKB sequence (vector mode) timing



Note SAO2 to SAO0 are output even in the single mode but are meaningless.

Remark Keep INTP input high at least until the INTAKB pulse falls the first time.

(5) Other timing



6.6 Differences Between NA59A and μPD71059

- Level trigger or edge trigger of the interrupt request signal can be selected independently.
- Changes in the INTR signal can be prevented while it is high even if WRB goes low.
- Each interrupt request signal can be output independently.
- A reset signal can be issued independently in response to an interrupt request signal.
- Control pins for 3-state and output signals are added.
- Test pins are added (TBI33 to TBI0, TEST, and through path test pin).
- DC and AC characteristics, and pin capacitance

Note that because the macro operations of the NA59A other than above are almost the same as those of the μPD71059, refer to the **μPD71059 User's Manual (U13042J)** (Japanese version only) and **μPD71059 Data Sheet (U11932J)** (Japanese version only) for operation details. [Note]

<R> **Note** Contact NEC Electronics if the related documents cannot be obtained.

6.7 Notes on Designing Circuit

6.7.1 When using NA59A in same manner as μPD71059

(1) INTP7 to INTP0

The μPD71059 has internal pull-up resistors for INTP7 to INTP0, while the NA59A does not. To use the NA59A in the completely same manner as the μPD71059, connect a buffer with a pull-up resistor to INTP7 to INTP0 of the NA59A.

(2) IRL7 to IRL0, INTCON

Clamp all these pins to low level.

(3) INTO7 to INTO0, ESLC7 to ESLC0

Leave all these pins open. However, output these pins as test pins because they are used for the mega macro test in the same manner as the other pins.

(4) SAI2 to SAI0, SAO2 to SAO0, CSA

Use a bidirectional buffer and control the output by using CSA.

(5) SVB, SVO, CSV

Use a bidirectional buffer and control the output by using CSV.

6.7.2 Using IRL7 to IRL0

The μPD71059 can select an input trigger for INTP7 to INTP0 by using IW1, however, the same trigger must be selected for all these eight pins. The NA59A can set INTPx in the level trigger mode independently by making the corresponding IRLx high. When IRLx goes low, the corresponding INTPx is set in the edge trigger mode.

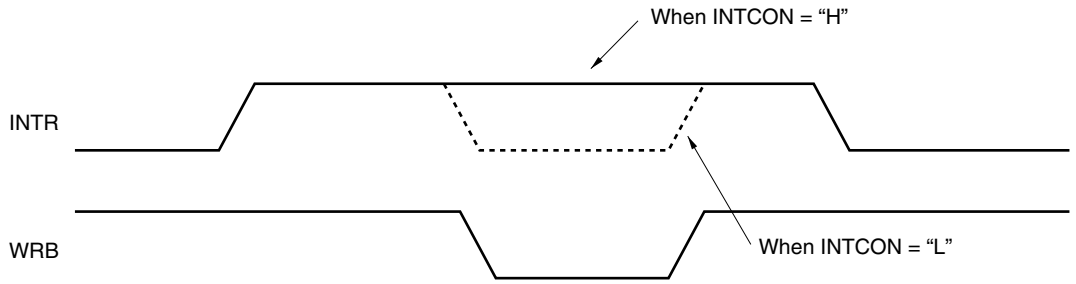
If D3 of IW1 is made high, all INTP7 to INTP0 are set in the level trigger mode, regardless of the level of IRL7 to IRL0.

Remark x: 0, 1, ..., 7

6.7.3 Using INTCON

If data is written to the μPD71059 while the INTR output is high, the INTR output goes low while WRB is low. With the NA59A, the INTR output can be kept high even while WRB is low, by making INTCON high in advance, even if data is written to the NA59A when the INTR output is high.

Figure 6-1. Relationship Between INTCON, INTR, and WRB



Caution If INTR is connected to INTP of the NA59A (or μPD71059) when it is set in the edge trigger mode, or to a CPU that is detecting an edge, missing the detection of an interrupt can be prevented. This is because INTR goes low while WRB is low when the FI command is issued or when a no-operation command is used to write data.
If INTCON is high, however, the above feature cannot be used; therefore, use the level trigger mode.

6.7.4 Using INTO7 to INTO0

INTO7 to INTO0 are output in response to the input signals INTP7 to INTP0 that serve as the source of the INTR output. INTP0 to INTP7 correspond to INTO0 to INTO7, respectively.

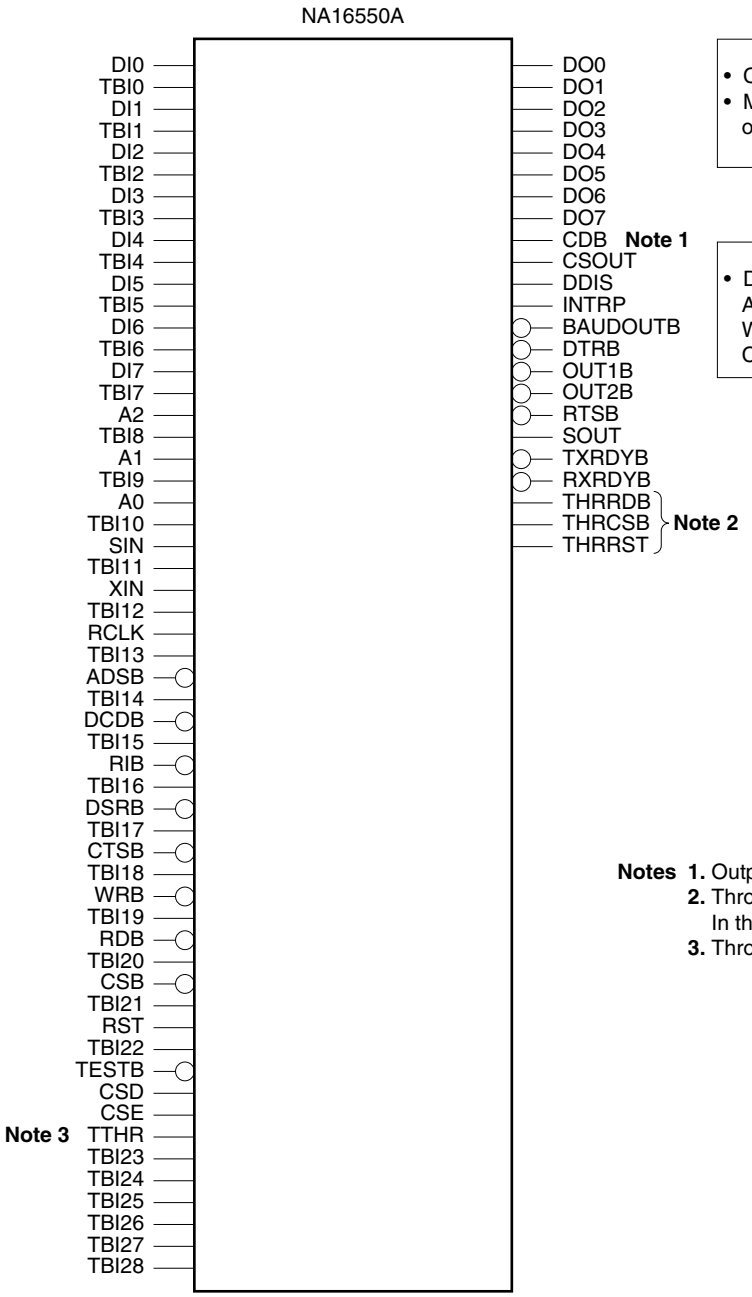
6.7.5 Using ESLC7 to ESLC0

These signals are asserted active (high) when ISR (in-service register) is cleared. They are output each time an interrupt signal that clears these signals is input.

CHAPTER 7 NA16550A MACRO

This chapter explains the functions of the NA16550A.

Block Type	Function
NA16550A	UART + FIFO



Features

- Compatible functions with PC16550D
- Maximum operating frequency: 33 MHz or equivalent

Caution

- Do not input spike to SIN, XIN, RCLK, ADSB, RIB, DCDB, DSRB, CTSB, WRB, RDB, CSB, RST, TESTB, CSD, CSE, TTHR, and TBI28 through TBI11.

Notes 1. Output control signal of DO7 through DO0
2. Through path output pins of RDB, CSB, and RST In the pre- or post-mega-macro stage test
3. Through path/normal mode select pin

Remark The input signal pins with “TBI” prefixed are test pins.

Number of cells used (configuration)	8528 (164 × 52)
Mega macro test pattern length	14889

7.1 NA16550A Pins

Pin Name[Note 1]	I/O	Function[Note 2]	Active Level	Test Pin[Note 1]	Fanin/ Fanout	Block Name
DI0	Input	Data bus input signal (LSB)		TBI0	1.3	L424
DI1	Input	Data bus input signal		TBI1	1.4	L424
DI2	Input	Data bus input signal		TBI2	1.6	L424
DI3	Input	Data bus input signal		TBI3	1.3	L424
DI4	Input	Data bus input signal		TBI4	2.1	L424
DI5	Input	Data bus input signal		TBI5	1.5	L424
DI6	Input	Data bus input signal		TBI6	1.5	L424
DI7	Input	Data bus input signal (MSB)		TBI7	1.1	L424
A2	Input	Address signal (used to access internal registers)		TBI8	1.6	L424
A1	Input	Address signal (used to access internal registers)		TBI9	2.0	L424
A0	Input	Address signal (used to access internal registers)		TBI10	1.1	L424
SIN	Input	Serial data input		TBI11	1.4	L111
XIN	Input	System clock input		TBI12	2.3	L111
RCLK	Input	Reference clock input for determining reception rate		TBI13	4.8	L111
ADSB	Input	Inputs strobe signal to latch address and chip select signals	Low	TBI14	1.7	L111
DCDB	Input	General-purpose input pin (Data Carrier Detect)	Low	TBI15	1.5	L111
RIB[Note 3]	Input	General-purpose input pin (Ring Indicator)	Low	TBI16	1.4	L111
DSRB	Input	General-purpose input pin (Data Set Ready)	Low	TBI17	1.6	L111
CTSB	Input	General-purpose input pin (Clear To Send)	Low	TBI18	1.3	L111
WRB	Input	Write signal	Low	TBI19	1.3	L111
RDB	Input	Read signal	Low	TBI20	1.1	L111
CSB	Input	Chip select signal	Low	TBI21	1.4	L111
RST	Input	Reset signal	High	TBI22	3.1	L111
TESTB	Input	Test/normal mode selection “H”: Normal mode “L”: Test mode		–	2.0	L101
CSD	Input	3-state output control		–	5.1	L101
CSE	Input	3-state output control		–	3.9	L101
TTHR	Input	Through path/normal mode select signal “H”: Through path mode “L”: Normal mode		–	3.2	L101

Pin Name	I/O	Function[Note 2]	Active Level	Test Pin	Fanin/ Fanout	Block Name
DO0	Output	Data bus output signal (LSB)		–	34.0	F531
DO1	Output	Data bus output signal		–	34.0	F531
DO2	Output	Data bus output signal		–	34.0	F531
DO3	Output	Data bus output signal		–	34.0	F531
DO4	Output	Data bus output signal		–	34.0	F531
DO5	Output	Data bus output signal		–	33.0	F531
DO6	Output	Data bus output signal		–	33.0	F531
DO7	Output	Data bus output signal (MSB)		–	33.0	F531
CDB	Output	Enable signal of data bus 0: High-impedance forced output 1: Normal 3-state operation		–	31.0	F101
CSOUT	Output	Signal indicating chip select status	High	–	30.0	F101
DDIS	Output	Driver Disable	Low	–	28.0	F101
INTRP	Output	Signal indicating interrupt status	High	–	32.0	F101
BAUDOUTB	Output	Output clock from baud rate generator		–	26.0	F101
DTRB	Output	General-purpose input pin (Data Terminal Ready)	Low	–	33.0	F101
OUT1B	Output	General-purpose input pin (Output1)	Low	–	31.0	F101
OUT2B	Output	General-purpose input pin (Output2)	Low	–	33.0	F101
RTSB	Output	General-purpose input pin (Request To Send)	Low	–	32.0	F101
SOUT	Output	Serial data output		–	34.0	F101
TXRDYB	Output	Transmission ready signal	Low	–	34.0	F101
RXRDYB	Output	Reception ready signal	Low	–	34.0	F101
THRRDB	Output	Through path output test pin (RDB signal)		–	34.0	F101
THRCSB	Output	Through path output test pin (CSB signal)		–	30.0	F101
THRRST	Output	Through path output test pin (RST signal)		–	34.0	F101
TBI0	Input	Test input		–	1.2	L424
TBI1	Input	Test input		–	1.6	L424
TBI2	Input	Test input		–	1.6	L424
TBI3	Input	Test input		–	1.2	L424
TBI4	Input	Test input		–	1.9	L424
TBI5	Input	Test input		–	1.8	L424
TBI6	Input	Test input		–	1.5	L424
TBI7	Input	Test input		–	1.2	L424
TBI8	Input	Test input		–	1.8	L424
TBI9	Input	Test input		–	1.9	L424
TBI10	Input	Test input		–	1.1	L424
TBI11	Input	Test input		–	1.2	L111
TBI12	Input	Test input		–	2.0	L111
TBI13	Input	Test input		–	4.7	L111
TBI14	Input	Test input		–	2.7	L111

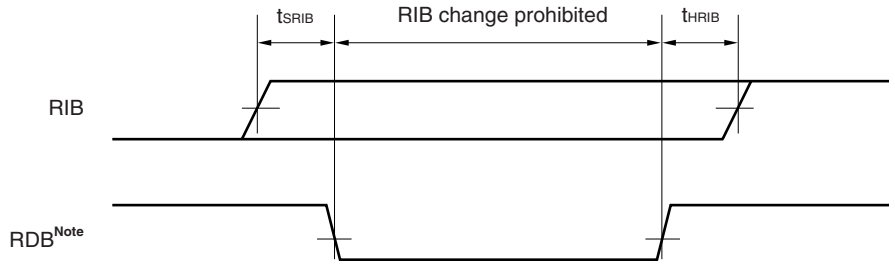
Pin Name	I/O	Function	Active Level	Test Pin	Fanin/ Fanout	Block Name
TBI15	Input	Test input		–	1.5	L111
TBI16	Input	Test input		–	1.6	L111
TBI17	Input	Test input		–	1.6	L111
TBI18	Input	Test input		–	1.3	L111
TBI19	Input	Test input		–	1.3	L111
TBI20	Input	Test input		–	1.5	L111
TBI21	Input	Test input		–	1.3	L111
TBI22	Input	Test input		–		
TBI23	Input	Test mode pin		–		
TBI24	Input	Test mode pin		–		
TBI25	Input	Test mode pin		–		
TBI26	Input	Test mode pin		–		
TBI27	Input	Test mode pin		–		
TBI28	Input	Test mode pin		–		

Notes 1. A (normal) pin and a test pin described in the same line have the same function.

2. Provide a clock pin (a pin described as “clock” in the Function column) using an input pin, not a bidirectional pin.

3. When not using the RIB pin, clamp it to “H” or “L”.
When using the RIB pin, satisfy the following timings:

Parameter	Symbol	MIN.	Unit
RIB rise setup time (to RDB↓)	t_{SRIB}	5.0	ns
RIB rise hold time (from RDB↑)	t_{HRIB}	5.0	ns



Note RDB is the timing at which the modem status register is read (MSR A = 6).

Remark Input: Input pin
Output: Output pin

Remarks 1. TBIx is a test input pin. A signal can be input from TBIx by making TESTB input low. Connect pins so that signals can be directly input to the mega macro from outside the gate array in test mode. "Directly" here means a circuit configuration where the input signal is not inverted or no sequential circuit such as a flip-flop is inserted between the pins.

TESTB	Input Pin
1	Normal pin[Note]
0	TBIx

Note Input a defined value of 0 or 1 to the test input pins in normal mode (it does not matter if 0 and 1 are mixed).

2. Functions of CSE input and CSD input

CSE input: Turned on (high or low level) all the 3-state outputs when "1" is input to this pin.

CSD input: Turned off (high-impedance: Hi-Z) all the 3-state outputs when "0" is input to this pin while CSE = "0".

When "1" is input, the 3-state outputs are turned on/off by an internal control signal of the mega macro (normal operation).

CSE	CSD	Status of Output Pin	Status of 3-State Output Pin[Note]
0	0	Normal operation	Hi-Z
0	1	Normal operation	Normal operation
1	–	Normal operation	No Hi-Z output

Note The 3-state pins are DO7 to DO0.

3. When CSE = "0", the Hi-Z status of the 3-state output buffer can be checked by monitoring the output value of the corresponding output control signal.

"Hi-Z" Pin	Corresponding Output Control Signal and Output	
DO7 to DO0	CDB	0

When CSE = "1", the status of the buffer is not affected by the 3-state output control signal (the 3-state output buffer does not go into a "Hi-Z" state).

4. CSE and CSD can be fixed by clamping. Fix CSD to 1 when clamping it.

Remarks 5. Operating status of output pin depending on combination of TTHR, CSE, and CSD

TTHR Pin	CSE Pin	CSD Pin	3-State Output Pin (DOx)	3-State Control Pin (CDB)	Other Pins	Through Path Dedicated Pin (Output THRxxx)
0	0	0	Hi-Z	0	Normal operation	0
		1	Normal operation	Normal operation		
	1	0	No Hi-Z output	0		
		1		Normal operation		
1	0	0	Hi-Z	Through path	Through path	Through path
		1	Through path			
	1	×				

6. I/O pin correspondence table in through path test

The input pins corresponding to the mega macro output pins when TTHR = “1” are as follows:

Output Pin	Through Path Corresponding Pin	
	TESTB = 1	TESTB = 0
DO0	DI0	TBI0
DO1	DI1	TBI1
DO2	DI2	TBI2
DO3	DI3	TBI3
DO4	DI4	TBI4
DO5	DI5	TBI5
DO6	DI6	TBI6
DO7	DI7	TBI7
CDB	A2	TBI8
CSOUT	A1	TBI9
DDIS	A0	TBI10
INTRP	SIN	TBI11

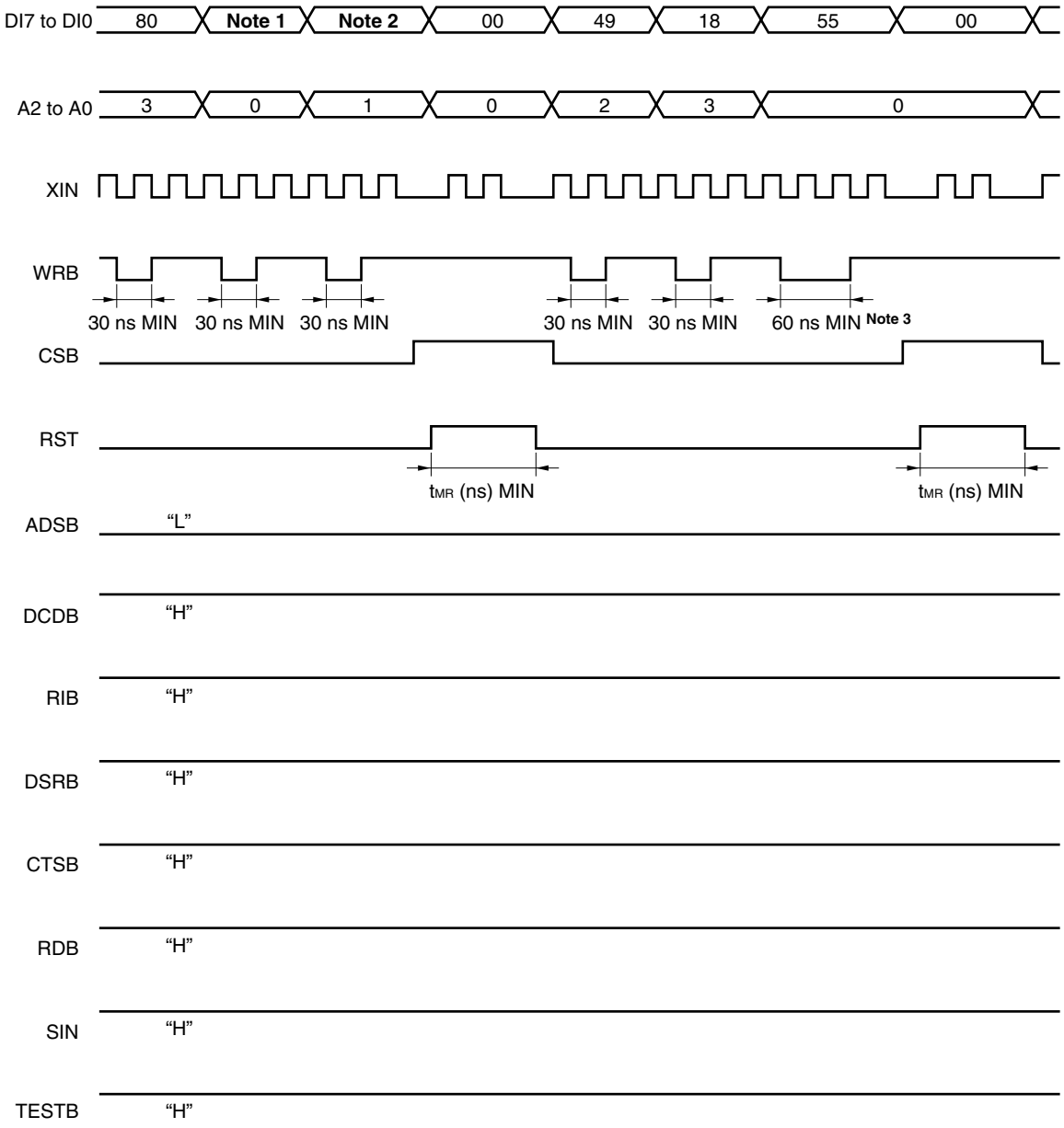
Output Pin	Through Path Corresponding Pin	
	TESTB = 1	TESTB = 0
BAUDOUTB	XIN	TBI12
DTRB	RCLK	TBI13
OUT1B	ADSB	TBI14
OUT2B	DCDB	TBI15
RTSB	RIB	TBI16
SOUT	DSRB	TBI17
TXRDYB	CTSB	TBI18
RXRDYB	WRB	TBI19
THRRDB	RDB	TBI20
THRCSB	CSB	TBI21
THRRST	RST	TBI22

When TTHR = “1” and CSE = “0”, all the 3-state pins are controlled by CSD (selection between through path and high-impedance status).

7.2 NA16550A Initialization and Notes on Creating Pattern

The NA16550A is initialized as follows:

Figure 7-1. Initialization Pattern



Notes 1. Lower byte of division ratio to be used.

2. Higher byte of division ratio to be used.

<R> **3.** Time necessary to determine the value of a loop circuit for simulation.

Cautions 1. Input "0" or "1" to the other input pins (normal input and test input pins). Make sure that "X" is not input to these pins.

2. Input the division ratio to Notes 1, 2, and be sure to reset after the division ratio is set.

7.2.1 Status of output pin after initialization

The status of the output pin is as follows after initialization:

Table 7-1. Status of Output Pin After Initialization

Output Pin Name	Pin Status
DO7 to DO0	When CSE = 0: Hi-Z When CSE = 1: Low level
CDB	Low level
CSOUT	Low level
DDIS	High level
INTRP	Low level
BAUDOUTB	Clock resulting from dividing frequency of reference clock (XIN) by the value specified at the baud rate generator divisor latch.
DTRB	High level
OUT1B	High level
OUT2B	High level
RTSB	High level
SOUT	High level
TXRDYB	Low level
RXRDYB	High level

7.2.2 Default value after reset

The default values of the registers and output signals (general-purpose output signals and serial data output signals) are as follows when the NA16550A has been reset.

Table 7-2. Default Values of Registers

Register	Default Value MSB LSB
IER	00000000
IIR	00000001
FCR	00000000
LCR	00000000
MCR	00000000
LSR	01100000
MSR	00000000

Table 7-3. Default Values of Output Signals (General-Purpose Output Signals and Serial Data Output Signals)

Output Signal Name	Default Value
SOUT	1
DTRB	1
OUT1B	1
OUT2B	1
RTSB	1

<R> **7.2.3 Notes on creating pattern**

Notes on creating a pattern are as follows.

<1> is a common limitation to simulation and actual devices.

<2> to <5> are limitations for simulation. <2> to <5> are not limitations for actual devices.

<1> Configure the following input pins in a circuit that avoids spike input.
SIN, XIN, RCLK, ADSB, DCDB, RIB, DSRB, CTSB, WRB, RDB, CSB, RST, TESTB, CSD, CSE, TTHR, TBI28 to TBI11

<2> Do not change the value of the divisor latch after initialization.

<3> Make sure that the change of XIN and the change of RST do not conflict.

<4> Make sure that the rising edges of XIN and WRB do not conflict (a pattern in which the falling edge of XIN is synchronized with the rising edge of WRB is recommended).

<5> Make sure that the change of SIN and the rising edge of RCLK do not conflict (a pattern in which the change of SIN is synchronized with the falling edge of RCLK is recommended).

7.3 Delay Time

Refer to **1.2.4 Delay time**.

7.4 AC Characteristics (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

(1) Read cycle and write cycle

Parameter		Symbol	MIN.	MAX.	Unit
Address strobe (ADSB) pulse width		t_{ADS}	10		ns
Address (A2, A1, A0) hold time (from ADSB ↑)		t_{AH}	2		ns
Address (A2, A1, A0) setup time (to RDB ↓)		t_{AR}	6		ns
Address (A2, A1, A0) setup time (to ADSB ↑)		t_{AS}	6		ns
Address (A2, A1, A0) setup time (to WRB ↓)		t_{AW}	6		ns
Chip select (CSB) hold time (from ADSB ↑)		t_{CH}	0		ns
Chip select (CSB) setup time (to ADSB ↑)		t_{CS}	5		ns
Chip select (CSB) setup time (to RDB ↓)		t_{CSR}	4		ns
Chip select (CSB) setup time (to WRB ↓)		t_{CSW}	4		ns
Data hold time (from WRB ↑)		t_{DH}	5		ns
Data setup time (to WRB ↓)		t_{DS}	3		ns
Data float delay time (from RDB ↑)		t_{HZ}		7	ns
Reset pulse high-level width		t_{MR}	200		ns
Address (A2, A1, A0) hold time (from RDB ↑)		t_{RA}	0		ns
Read cycle delay time		t_{RC1}	14		ns
Read cycle ADSB hold time		t_{RC2}	0		ns
Chip select (CSB) hold time (from RDB ↑)		t_{RCS}	0		ns
RDB active pulse width		t_{RD}	20		ns
DDIS delay time (from RDB)		t_{RDD}		5	ns
Data delay time (from RDB ↓)		t_{RVD}		10	ns
Address (A2, A1, A0) hold time (from WRB ↑)		t_{WA}	0		ns
Write cycle delay time		t_{WC1}	14		ns
Write cycle ADSB hold time		t_{WC2}	0		ns
Chip select (CSB) hold time (from WRB ↑)		t_{WCS}	0		ns
WRB active pulse width		t_{WR}	20		ns
Clock pulse high-level width		t_{XH}	12		ns
Clock pulse low-level width		t_{XL}	12		ns
Read cycle time	In 16450 mode	RC	40		ns
	When RXRDYB is not used		55		ns
	When RXRDYB is used		70		ns
Write cycle time	In 16450 mode	WC	30		ns
	When TXRDYB is not used		45		ns
	When TXRDYB is used		60		ns
Read/write recovery time	In 16450 mode	t_{RV}	25		ns
	When RXRDYB and TXRDYB are not used		40		ns
	When RXRDYB and TXRDYB are used		55		ns

(2) Baud rate generator

Parameter	Symbol	MIN.	MAX.	Unit
Transmission clock division ratio	N	1	$2^{16} - 1$	
Transmission clock rise delay time (from XIN)	t_{BHD}		7	ns
Transmission clock fall delay time (from XIN)	t_{BLD}		7	ns
Transmission clock pulse high-level width[Note]	t_{HW}	125		ns
Transmission clock pulse low-level width[Note]	t_{LW}	125		ns

Note f_X = 8.0 MHz, BAUDOUTB = XIN/2

(3) Receiver and transmitter

Parameter		Symbol	MIN.	MAX.	Unit
Interrupt clear time (from RDB ↑ (when LSR is read))		t_{RINT}		12	ns
Interrupt clear time (from RDB ↓ (when RBR is read))		t_{RINT}		12	ns
RXRDYB clear time (from RDB ↓ (RBR))	16450 mode	t_{RXI0}		15	ns
	FIFO mode	t_{RXI1}		35	ns
Sample clock delay time (from RCLK)		t_{SCD}		13	ns
Interrupt generation time (from valid data reception or reception error)		t_{SINT}		1	RCLK cycles[Note]
Interrupt clear time (from WRB ↓ (during THR write))		t_{HR}		8	ns
Interrupt clear time (from RDB ↑ (during IIR read))		t_{IR}		8	ns
Transmission start time		t_{IRS}	8	24	BAUDOUTB cycles
Interrupt generation time (from WRB ↑ (during THR write))		t_{SI}	16	24	BAUDOUTB cycles
Interrupt (THRE) generation time (from stop bit)		t_{STI}		8	BAUDOUTB cycles
TXRDYB generation time (vs. start bit)		t_{SXA}		8	BAUDOUTB cycles
TXRDYB clear time	16450 mode, FIFO mode (DMA = 0) (from WRB ↓ (during THR write))	t_{WXI0}		10	ns
	FIFO mode (DMA = 1) (from WRB ↑ (during THR write))	t_{WXI1}		50	ns

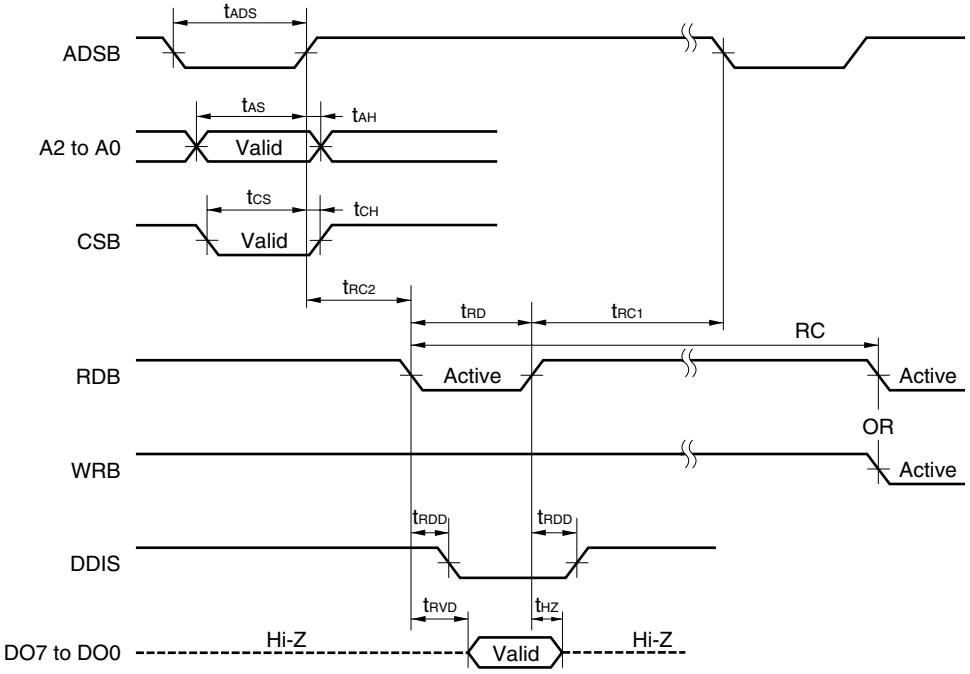
Note The high-level width of PRCLK is the same as t_{XH}, and the low-level width is the same as t_{XL}.
When FCR0 = 1, t_{SINT} = 3RCLK. When a timeout interrupt occurs, t_{SINT} = 8RCLK.

(4) Modem control

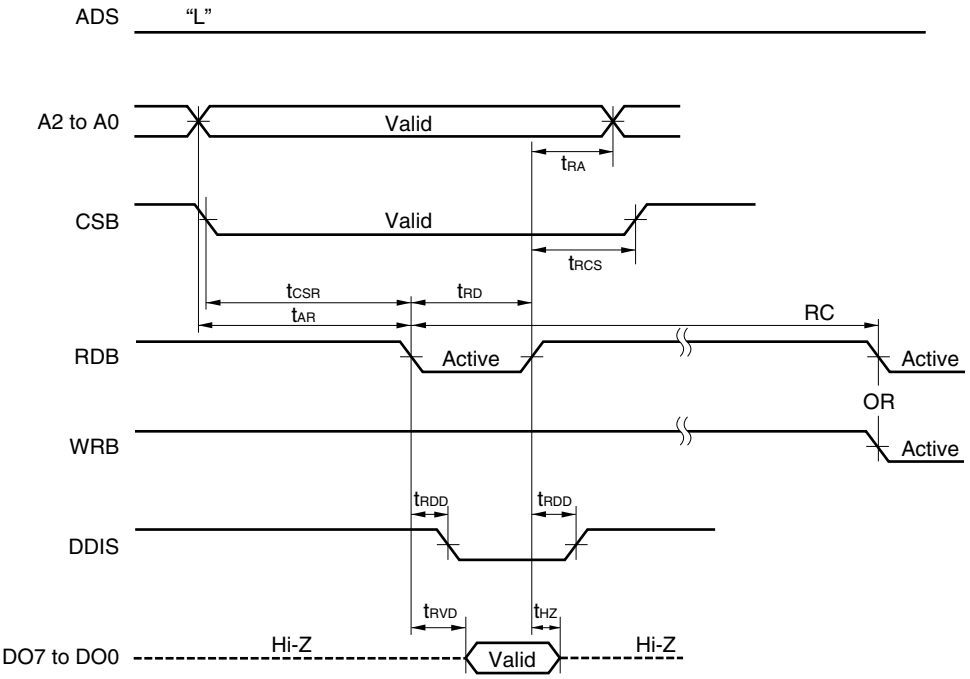
Parameter	Symbol	MIN.	MAX.	Unit
RTSB, DTRB, OUT1B, OUT2B delay time (from WRB ↑ (during MCR write))	t_{MDO}		8	ns
Interrupt clear time (from RDB ↓ (during MSR read))	t_{RIM}		15	ns
Interrupt generation time (from RIB ↑, CTSB, DSRB, DCDB)	t_{SIM}		15	ns

7.5 Timing Charts

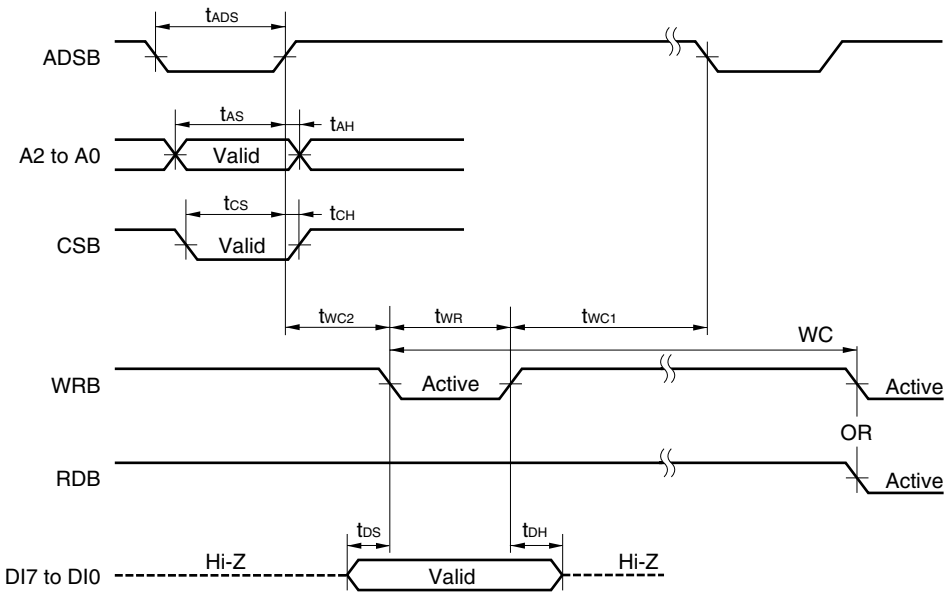
(1) Read cycle timing (when ADSB is used)



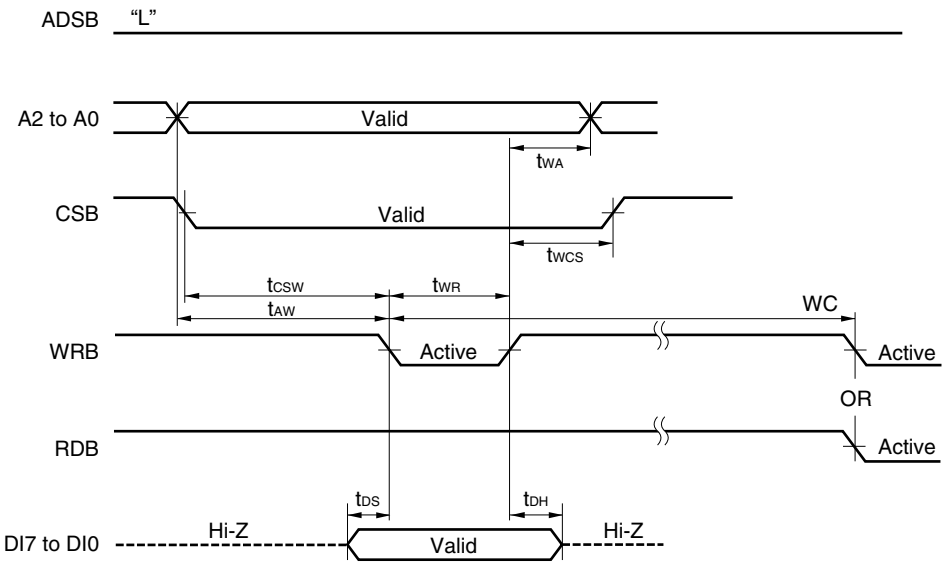
(2) Read cycle timing (when ADSB is clamped low)



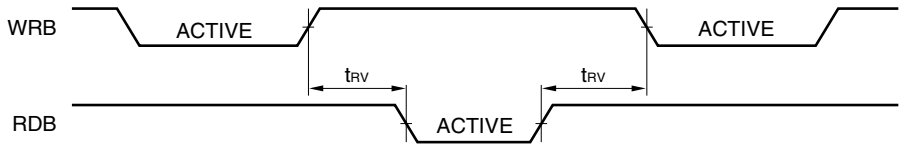
(3) Write cycle timing (when ADSB is used)



(4) Write cycle timing (when ADSB is clamped low)

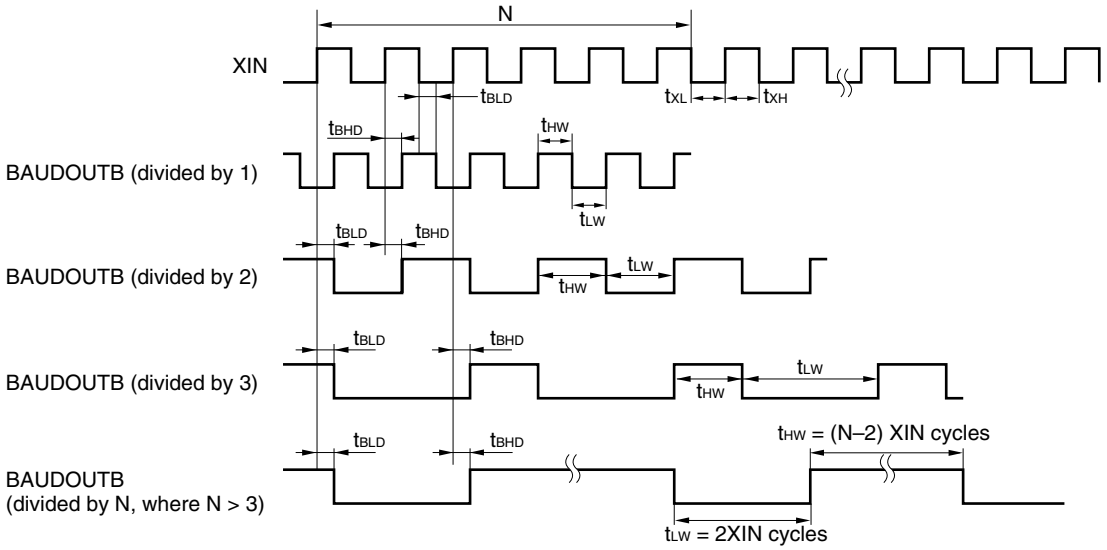


(5) Write and read recovery time

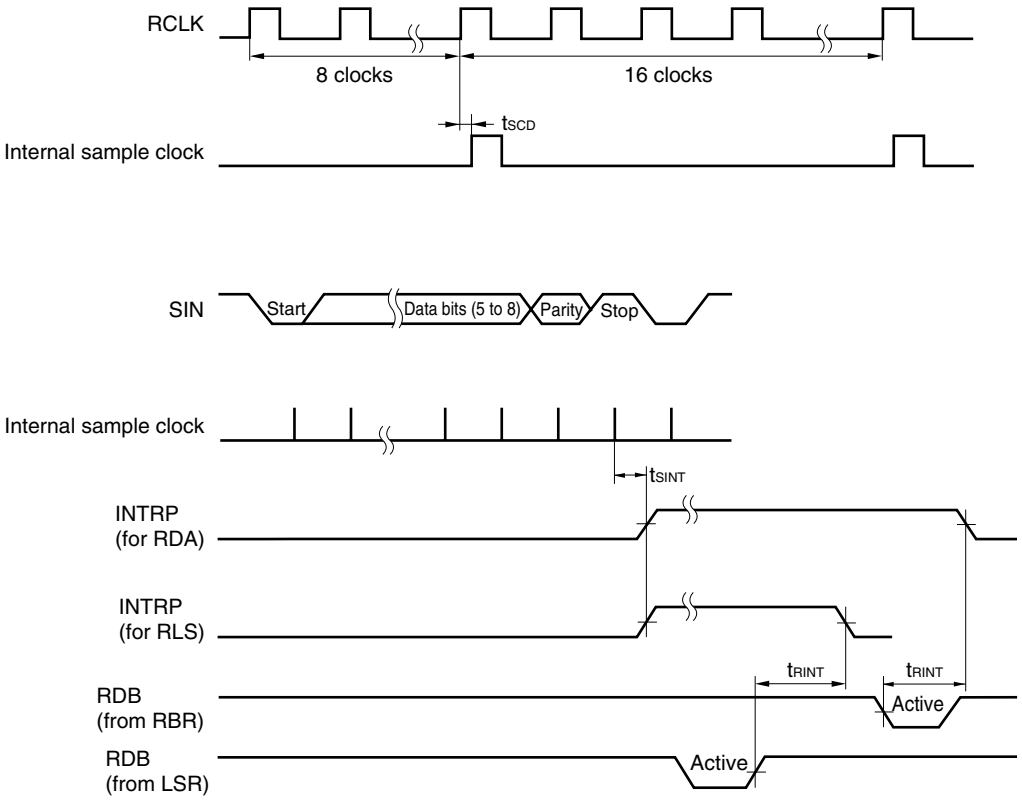


Remark When the RDB and WRB signals are simultaneously asserted active, an internal spike may be generated causing the device to malfunction. Therefore, do not assert the RDB and WRB signals active at the same time.

(6) Baud out timing



(7) Reception timing



Remarks 1. INTRP (for RDA) indicates the existence of receive data.
At this time, bit 0 of IER (ERBFI) is 1, and bits 1 to 3 of IIR are 010b.

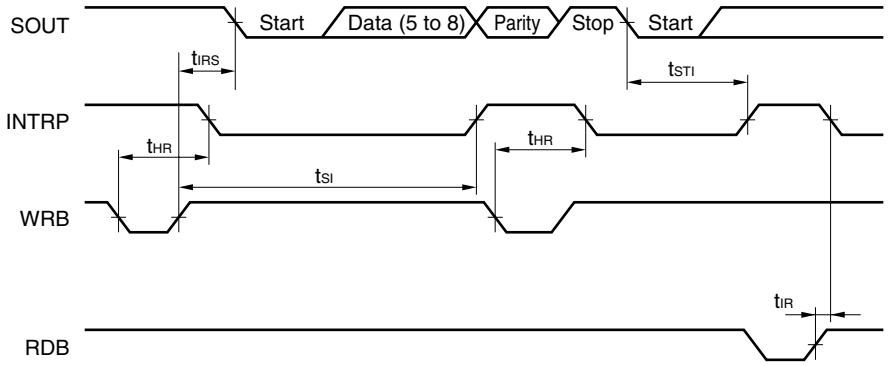
2. RDB (from RBR) reads RBR of A2 to A0 = 000b.

3. INTRP (for RLS) indicates a receive line status.
At this time, bit 2 (ERLSI) of IER is 1, and bits 1 to 3 of IIR are 011b.

4. RDB (from LSR) reads LSR of A2 to A0 = 101b.

For details of the read timing, refer to **(1) Read cycle timing (when ADSB is used)** and **(2) Read cycle timing (when ADSB is clamped low)**.

(8) Transmission timing



Remarks 1. INTRP indicates that the transmit buffer is empty.
At this time, bit 1 (ETBEI) of IER is 1, and bits 1 to 3 of IIR are 001b.

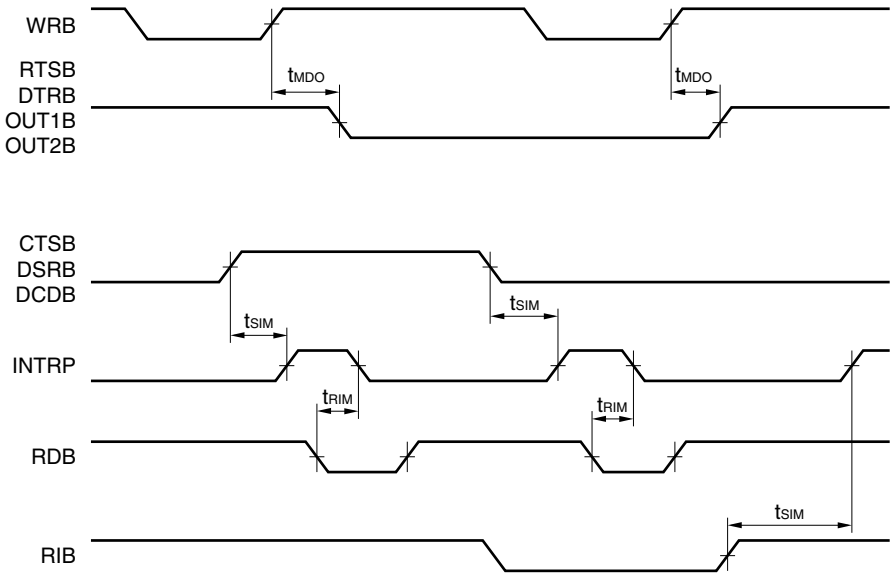
2. WRB writes THR of A2 to A0 = 000b.

3. RDB reads IIR of A2 to A0 = 010b.

For details of the read timing, refer to **(1) Read cycle timing (when ADSB is used)** and **(2) Read cycle timing (when ADSB is clamped low)**.

For details of the write timing, refer to **(3) Write cycle timing (when ADSB is used)** and **(4) Write cycle timing (when ADSB is clamped low)**.

(9) Modem control timing



Remarks 1. INTRP indicates the modem status.
At this time, bit 3 (EDSSI) of IER is 1, and bits 1 to 3 of IIR are 000b.

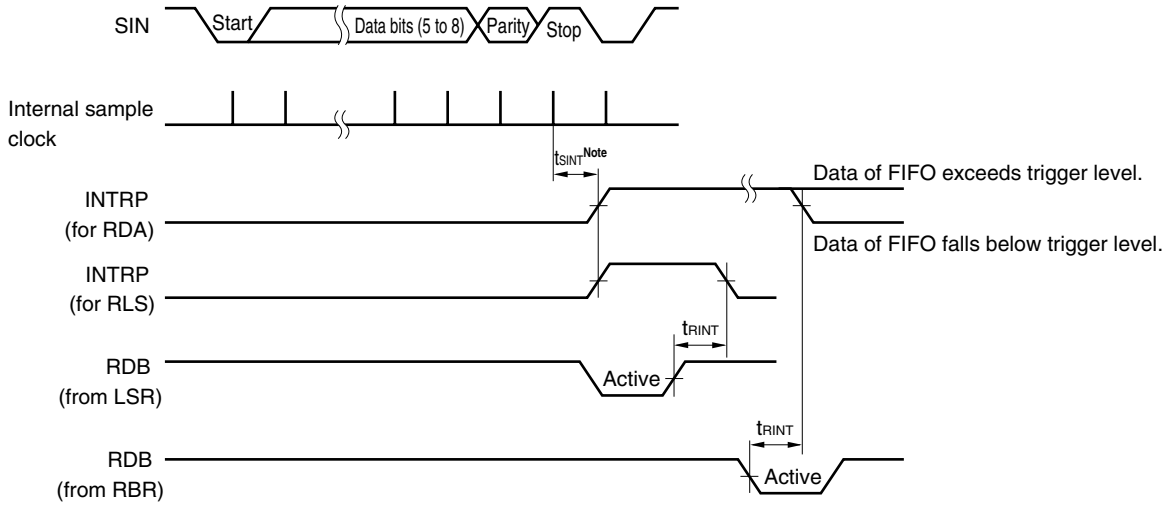
2. WRB writes MCR of A2 to A0 = 100b.

3. RDB reads MSR of A2 to A0= 110b.

For details of the read timing, refer to **(1) Read cycle timing (when ADSB is used)** and **(2) Read cycle timing (when ADSB is clamped low)**.

For details of the write timing, refer to **(3) Write cycle timing (when ADSB is used)** and **(4) Write cycle timing (when ADSB is clamped low)**.

(10) Timing of first byte of receive FIFO (when Data Ready is set)

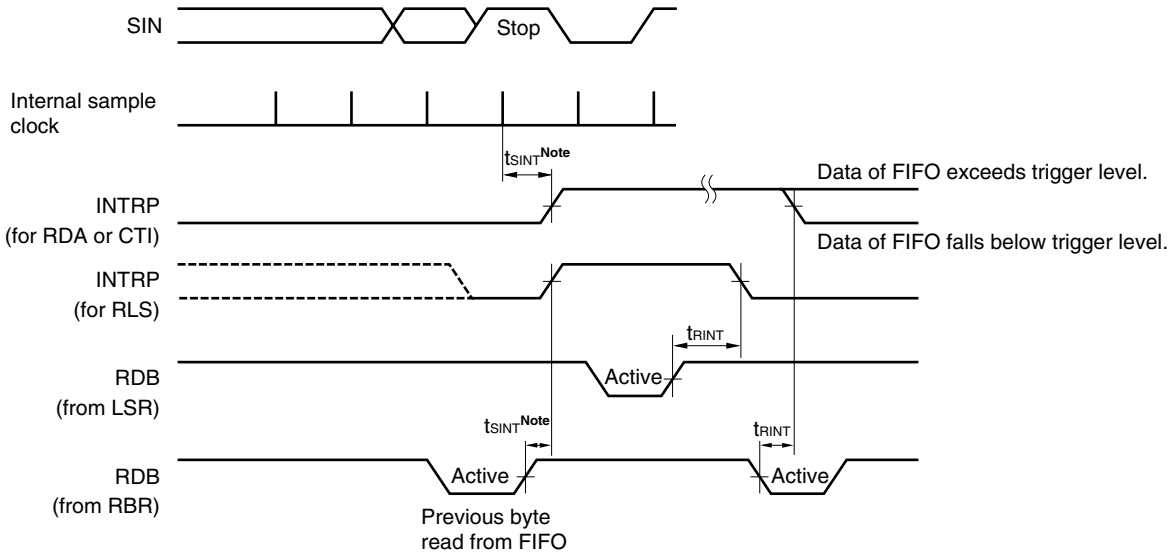


Note When FCR0 = 1, t_{SINT} = 3RCLK. If a timeout interrupt occurs, t_{SINT} = 8RCLK.

Remarks 1. INTRP (for RDA) indicates that the receive data has reached the trigger level of the FIFO.
At this time, bit 0 (ERBFI) of IER is 0, and bits 1 to 3 of IIR are 010b.
In the above figure, bits 6 and 7 of register FCR are cleared to 0.
INTRP is cleared depending on whether the receive data falls below the trigger level of the FIFO as a result of reading data.

2. INTRP (for RLS) indicates a receive line status.
At this time, bit 2 (ERLSI) of IER is 1, and bits 1 to 3 of IIR are 011b.

(11) Timing of byte other than first byte of receive FIFO (when Data Ready is already set)

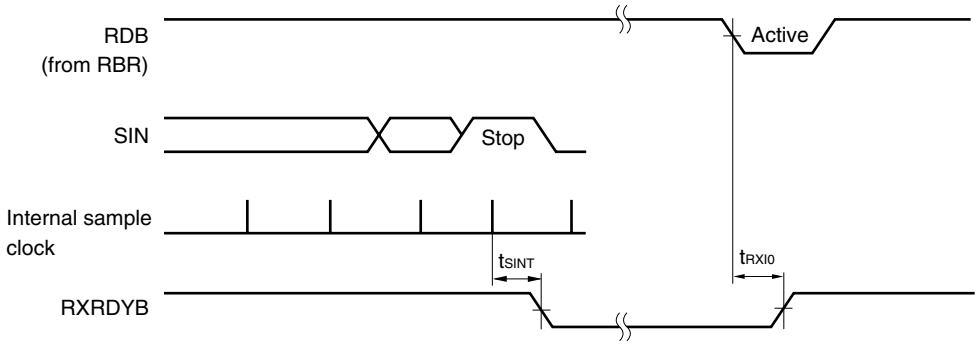


Note When FCR0 = 1, t_{SINT} = 3RCLK. If a timeout interrupt occurs, t_{SINT} = 8RCLK.

Remarks 1. INTRP (for RDA) occurs if the receive data exceeds the trigger level of the FIFO or if character time-out occurs.
At this time, bit 0 (ERBFI) of IER is 1, and bits 1 to 3 of IIR are 010b.
In the above figure, both bits 6 and 7 of register FCR are cleared to 0.
INTRP is cleared when the receive data falls below the trigger level of the FIFO as a result of reading data.

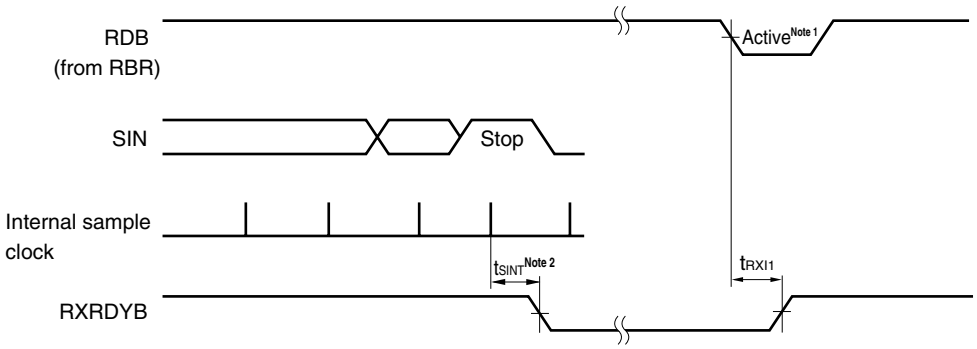
2. INTRP (for RLS) indicates a receive line status.
At this time, bit 2 (ERLSI) of IER is 1 and bits 1 to 3 of IIR are 011b.

(12) Timing of receive READY in 16450 mode



Remark The input signal of SIN is the first byte.

(13) Timing in receive READY in FIFO mode (DMA mode = 0)

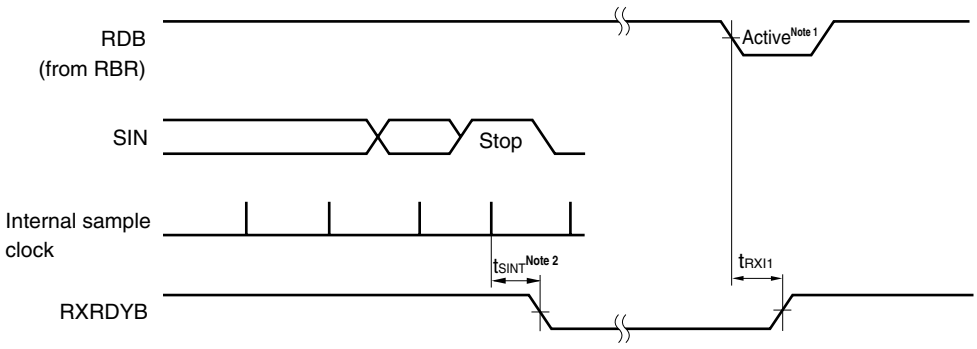


Notes 1. The last byte of the FIFO is read here.

2. When FCR0 = 1, t_{SINT} = 3RCLK.

Remark The input signal of SIN is the first byte that reaches the trigger level of the receive FIFO.

(14) Timing of receive READY in FIFO mode (DMA mode = 1)

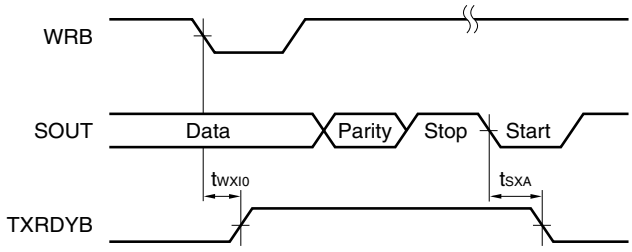


Notes 1. The last byte of the FIFO is read here.

2. When FCR0 = 1, t_{SINT} = 3RCLK. When a timeout interrupt occurs, t_{SINT} = 8RCLK.

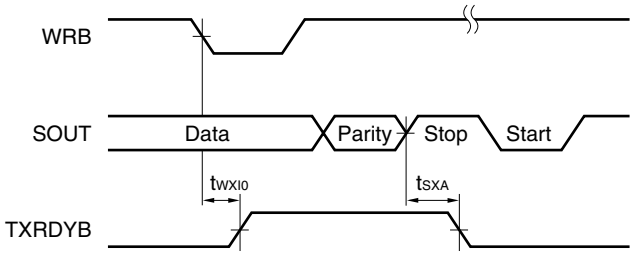
Remark The input signal of SIN is the first byte that reaches the trigger level of the receive FIFO.

<R> **(15) Timing of transmit READY in 16450 mode (DMA mode = 0)**



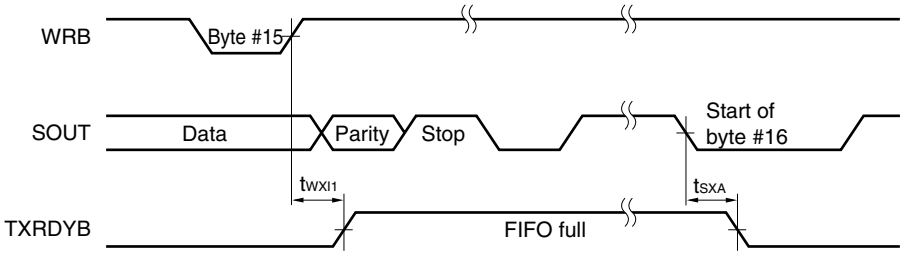
Remark WRB writes THR of A2 to A0= 000b.

<R> **(16) Timing of transmit READY in FIFO mode (DMA mode = 0)**



Remark WRB writes THR of A2 to A0= 000b.

<R> **(17) Timing of transmit READY in FIFO mode (DMA mode = 1)**

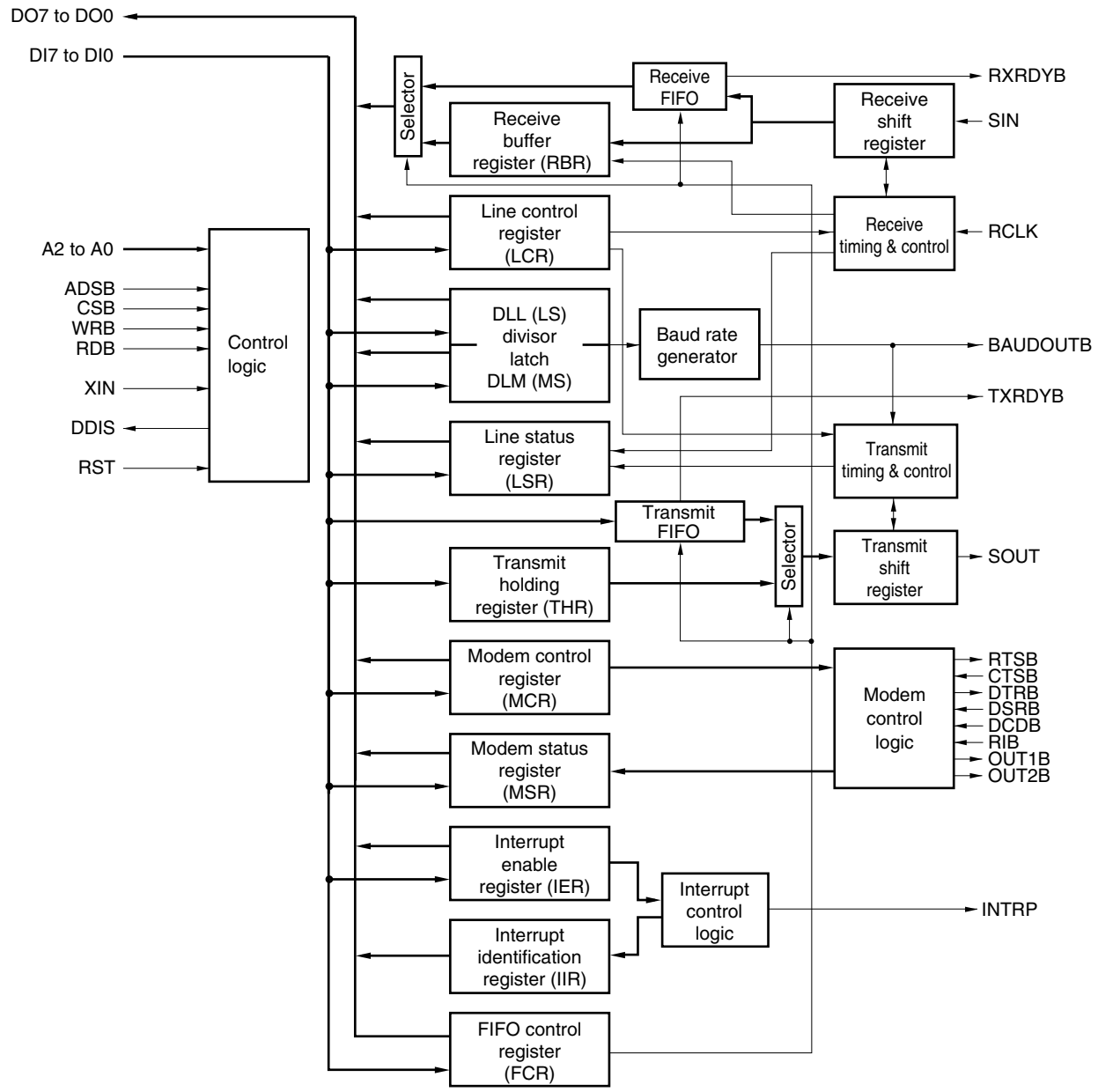


Remark WRB writes THR of A2 to A0 = 000b.

7.6 Block Diagram

The block diagram of this macro is shown below. In this block diagram, the circuits related to testing are omitted.

Figure 7-2. Block Diagram



7.7 Register List

Table 7-4. Register List (1/2)

		Register Address					
DLAB		DLAB = 0	DLAB = 0	DLAB = 0	DLAB = X	DLAB = X	DLAB = X
Address		A = 0	A = 0	A = 1	A = 2	A = 2	A = 3
Register name		Receive buffer register (read only)	Transmit holding register (write only)	Interrupt enable register	Interrupt ident. register (read only)	FIFO control register (write only)	Line control register
Register		RBR	THR	IER	IIR	FCR	LCR
Bit No.	0	Data bit 0[Note 1]	Data bit 0[Note 1]	Enable receive data available interrupt (ERBFI)	“0” if interrupt pending	FIFO enable	Word length select bit 0 (WLS0)
	1	Data bit 1	Data bit 1	Enable transmit holding register empty interrupt (ETBEI)	Interrupt ID bit (0)	RCVR FIFO reset	Word length select bit 1 (WLS1)
	2	Data bit 2	Data bit 2	Enable receive line status interrupt (ERLSI)	Interrupt ID bit (1)	XMIT FIFO reset	Number of stop bits (STB)
	3	Data bit 3	Data bit 3	Enable MODEM status interrupt (EDSSI)	Interrupt ID bit (2)[Note 2]	DMA mode select	Parity enable (PEN)
	4	Data bit 4	Data bit 4	0	0	Reserved	Even parity select (EPS)
	5	Data bit 5	Data bit 5	0	0	Reserved	Stick parity
	6	Data bit 6	Data bit 6	0	FIFOs enabled[Note 2]	RCVR trigger (LSB)	Set break
	7	Data bit 7	Data bit 7	0	FIFOs enabled[Note 2]	RCVR trigger (MSB)	Divisor latch access bit (DLAB)

Notes 1. Data bit 0 is LSB; the first bit when serial data is transmitted/received.

2. Always set to 0 in 16450 mode.

Remark X: don’t care.

Table 7-4. Register List (2/2)

		Register Address					
DLAB		DLAB = X	DLAB = X	DLAB = X	DLAB = X	DLAB = 1	DLAB = 1
Address		A = 4	A = 5	A = 6	A = 7	A = 0	A = 1
Register name		MODEM control register	Line status register	MODEM status register	Scratch register	Divisor latch (LS)	Divisor latch (MS)
Register		MCR	LSR	MSR	SCR	DLL	DLM
Bit No.	0	Data terminal ready (DTR)	Data ready (DR)	Delta clear to send (DCTS)	Bit 0	Bit 0	Bit 8
	1	Request to send (RTS)	Overrun error (OE)	Delta data set ready (DDSR)	Bit 1	Bit 1	Bit 9
	2	Out 1	Parity error (PE)	Trailing edge ring indicator (TERI)	Bit 2	Bit 2	Bit 10
	3	Out 2	Framing error (FE)	Delta data carrier detect (DDCD)	Bit 3	Bit 3	Bit 11
	4	Loop	Break interrupt (BI)	Clear to send (CTS)	Bit 4	Bit 4	Bit 12
	5	0	Transmitter holding register (THRE)	Delta set ready (DSR)	Bit 5	Bit 5	Bit 13
	6	0	Transmitter empty (TEMT)	Ring indicator (RI)	Bit 6	Bit 6	Bit 14
	7	0	Error in PCVR FIFO[Note]	Data carrier detect (DCD)	Bit 7	Bit 7	Bit 15

Note Always set to 0 in 16450 mode.

Remark X: don't care.

APPENDIX A TEST SPECIFICATIONS

A.1 Mega Macro Test Specification
A.2 NA37A Pin Reference Table
A.3 NA51A Pin Reference Table
A.4 NA54A Pin Reference Table
A.5 NA55A Pin Reference Table
A.6 NA59A Pin Reference Table
A.7 NA16550A Pin Reference Table

A.1 Mega Macro Test Specification

1. Part number μPD65 _ _ _ - _ _ _

2. Date of preparation 20 _ _ / _ _ / _ _
   Name of company of person in charge of preparation_____
   Telephone number of above person _____

3. Mega macro used
   NA37A × ___ pcs
   NA51A × ___ pcs
   NA54A × ___ pcs
   NA55A × ___ pcs
   NA59A × ___ pcs
   NA16550A × ___ pcs Total ___ pcs

4. Number of pins

Number of input pins	___
Number of output pins	___
Number of bidirectional pins	___
Total number of pins	___

5. Number of patterns

Number of user patterns		=	___ patterns
NA37A (7009 patterns)	× ___ pcs	=	___ patterns
NA51A (12874 patterns)	× ___ pcs	=	___ patterns
NA54A (3479 patterns)	× ___ pcs	=	___ patterns
NA55A (3643 patterns)	× ___ pcs	=	___ patterns
NA59A (7334 patterns)	× ___ pcs	=	___ patterns
NA16550A (14889 patterns)	× ___ pcs	=	___ patterns
Total			___ patterns

Fill out the “Pin reference table” on the following pages for each mega macro used and attach it to this specification.

A.2 NA37A Pin Reference Table

Instance name _____ (1/)

Mega Macro Test Input		Mega Macro Test Output	
Mega Macro Pin Name	External Pin Name	Mega Macro Pin Name	External Pin Name
TBI0		DO0	
TBI1		DO1	
TBI2		DO2	
TBI3		DO3	
TBI4		DO4	
TBI5		DO5	
TBI6		DO6	
TBI7		DO7	
TBI8		AO0	
TBI9		AO1	
TBI10		AO2	
TBI11		AO3	
TBI12		RDOB	
TBI13		WROB	
TBI14		TCB	
TBI15		MRDB	
TBI16		MWRB	
TBI17		ADSB	
TBI18		AEN	
TBI19		HLDRQ	
TBI20		DMAAK0	
TBI21		DMAAK1	
TBI22		DMAAK2	
TBI23		DMAAK3	
TEST[Note 1]		AO4	
CSD[Note 2]		AO5	
CSE[Note 2]		AO6	
TTHR		AO7	
Test Mode Setting Input		CDB	
External Pin Name	Input Value	CAB	
		CEP	
		CRW	

Notes 1. "TEST" can be replaced by the test mode setting input.
2. "CSD" and "CSE" can be fixed by clamping. However, write the input value.

Remark When connecting input pin to bidirectional pin: Be sure to set the **input mode** when testing the macro.
When connecting output pin to bidirectional pin: Be sure to set the **output mode** when testing the macro.

A.3 NA51A Pin Reference Table

Instance name _____ (1/)

Mega Macro Test Input		Mega Macro Test Output	
Mega Macro Pin Name	External Pin Name	Mega Macro Pin Name	External Pin Name
TBI0		DO0	
TBI1		DO1	
TBI2		DO2	
TBI3		DO3	
TBI4		DO4	
TBI5		DO5	
TBI6		DO6	
TBI7		DO7	
TBI8		OSYN	
TBI9		TXD	
TBI10		TXRDY	
TBI11		TXEMP	
TBI12		RXRDY	
TBI13		DTRB	
TBI14		RTSB	
TBI15		CDB	
TBI16		CSYN	
TBI17		Test Mode Setting Input	
TBI18		External Pin Name	Input Value
TBI19			
TESTB[Note 1]			
CSD[Note 2]			
CSE[Note 2]			
TTHR			

Notes 1. "TESTB" can be replaced by the test mode setting input.
2. "CSD" and "CSE" can be fixed by clamping. However, write the input value.

Remark When connecting input pin to bidirectional pin: Be sure to set the **input mode** when testing the macro.
When connecting output pin to bidirectional pin: Be sure to set the **output mode** when testing the macro.

A.4 NA54A Pin Reference Table

Instance name _____ (1/)

Mega Macro Test Input	
Mega Macro Pin Name	External Pin Name
TBI0	
TBI1	
TBI2	
TBI3	
TBI4	
TBI5	
TBI6	
TBI7	
TBI8	
TBI9	
TBI10	
TBI11	
TBI12	
TBI13	
TBI14	
TBI15	
TBI16	
TBI17	
TBI18	
TESTB[Note 1]	
CSD[Note 2]	
CSE[Note 2]	
TTHR	

Mega Macro Test Output	
Mega Macro Pin Name	External Pin Name
DO0	
DO1	
DO2	
DO3	
DO4	
DO5	
DO6	
DO7	
CNTOUT0	
CNTOUT1	
CNTOUT2	
CDB	

Test Mode Setting Input	
External Pin Name	Input Value

Notes 1. "TESTB" can be replaced by the test mode setting input.
2. "CSD" and "CSE" can be fixed by clamping. However, write the input value.

Remark When connecting input pin to bidirectional pin: Be sure to set the **input mode** when testing the macro.
When connecting output pin to bidirectional pin: Be sure to set the **output mode** when testing the macro.

A.5 NA55A Pin Reference Table

Instance name _____ (1/)

Mega Macro Test Input		Mega Macro Test Output	
Mega Macro Pin Name	External Pin Name	Mega Macro Pin Name	External Pin Name
TBI0		PO00	
TBI1		PO01	
TBI2		PO02	
TBI3		PO03	
TBI4		PO04	
TBI5		PO05	
TBI6		PO06	
TBI7		PO07	
TBI8		PO10	
TBI9		PO11	
TBI10		PO12	
TBI11		PO13	
TBI12		PO14	
TBI13		PO15	
TBI14		PO16	
TBI15		PO17	
TBI16		PO20	
TBI17		PO21	
TBI18		PO22	
TBI19		PO23	
TBI20		PO24	
TBI21		PO25	
TBI22		PO26	
TBI23		PO27	
TBI24		DO0	
TBI25		DO1	
TBI26		DO2	
TBI27		DO3	
TBI28		DO4	
TBI29		DO5	
TBI30		DO6	
TBI31		DO7	
TBI32		P0C	
TBI33		P1C	
TBI34		P21C	
TBI35		P22C	
TBI36		P23C	
TBI37		P24C	

Mega Macro Test Input		Mega Macro Test Output	
Mega Macro Pin Name	External Pin Name	Mega Macro Pin Name	External Pin Name
TEST[Note 1]		P25C	
CSD[Note 2]		P26C	
CSE[Note 2]		P27C	
TTHR		CDB	

Test Mode Setting Input	
External Pin Name	Input Value

Notes 1. “TEST” can be replaced by the test mode setting input.

2. “CSD” and “CSE” can be fixed by clamp. However, write the input value.

Remark When connecting input pin to bidirectional pin: Be sure to set the **input mode** when testing the macro.
When connecting output pin to bidirectional pin: Be sure to set the **output mode** when testing the macro.

A.6 NA59A Pin Reference Table

Instance name _____ (1/)

Mega Macro Test Input		Mega Macro Test Output	
Mega Macro Pin Name	External Pin Name	Mega Macro Pin Name	External Pin Name
TBI0		DO0	
TBI1		DO1	
TBI2		DO2	
TBI3		DO3	
TBI4		DO4	
TBI5		DO5	
TBI6		DO6	
TBI7		DO7	
TBI8		SAO0	
TBI9		SAO1	
TBI10		SAO2	
TBI11		SVO	
TBI12		INTR	
TBI13		CDB	
TBI14		CSA	
TBI15		CSV	
TBI16		ESLC0	
TBI17		ESLC1	
TBI18		ESLC2	
TBI19		ESLC3	
TBI20		ESLC4	
TBI21		ESLC5	
TBI22		ESLC6	
TBI23		ESLC7	
TBI24		INTO0	
TBI25		INTO1	
TBI26		INTO2	
TBI27		INTO3	
TBI28		INTO4	
TBI29		INTO5	
TBI30		INTO6	
TBI31		INTO7	
TBI32		Test Mode Setting Input	
TBI33		External Pin Name	Input Value
TEST[Note 1]			
RST			
CSD[Note 2]			
CSE[Note 2]			
TTHR			

Notes 1. “TEST” can be replaced by the test mode setting input.
2. “CSD” and “CSE” can be fixed by clamp. However, write the input value.

Remark When connecting input pin to bidirectional pin: Be sure to set the **input mode** when testing the macro.
When connecting output pin to bidirectional pin: Be sure to set the **output mode** when testing the macro.

A.7 NA16550A Pin Reference Table

Instance name _____ (1/)

Mega Macro Test Input		Mega Macro Test Output	
Mega Macro Pin Name	External Pin Name	Mega Macro Pin Name	External Pin Name
TBI0		DO0	
TBI1		DO1	
TBI2		DO2	
TBI3		DO3	
TBI4		DO4	
TBI5		DO5	
TBI6		DO6	
TBI7		DO7	
TBI8		CDB	
TBI9		CSOUT	
TBI10		DDIS	
TBI11		INTRP	
TBI12		BAUDOUTB	
TBI13		DTRB	
TBI14		OUT1B	
TBI15		OUT2B	
TBI16		RTSB	
TBI17		SOUT	
TBI18		TXRDYB	
TBI19		RXRDYB	
TBI20		Test Mode Setting Input	
TBI21		External Pin Name	Input Value
TBI22			
TBI23			
TBI24			
TBI25			
TBI26			
TBI27			
TBI28			
TESTB[Note 1]			
CSD[Note 2]			
CSE[Note 2]			
TTHR			

Notes 1. “TESTB” can be replaced by the test mode setting input.
2. “CSD” and “CSE” can be fixed by clamping. However, write the input value.

Remark When connecting input pin to bidirectional pin: Be sure to set the **input mode** when testing the macro.
When connecting output pin to bidirectional pin: Be sure to set the **output mode** when testing the macro.

For further information,
please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

Hanover Office
Podbielski Strasse 166 B
30177 Hanover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52180
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Limburglaan 5
5616 HR Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
TEL: 010-8235-1155
http://www.cn.necel.com/

NEC Electronics Shanghai Ltd.
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai P.R. China P.C:200120
Tel: 021-5888-5400
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
12/F., Cityplaza 4,
12 Taikoo Wan Road, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

Seoul Branch
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-2719-2377

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/