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April 1st, 2010
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RENESAS

User's Manual

PFESiP® EP-1 Evaluation Board

Ordering Information

Document No. A19352EJ1V0UM00 (1st edition)
Date published September 2008 NS

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

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PREFACE

Readers This manual is intended for users who understand the functions of the microcontroller function chip with an on-chip V850E2 CPU core (PFESiP/V850EP1) and wish to evaluate developing PFESiP EP-1 Series products using the chip.

Purpose This manual is a selection guide for selecting the options of the PFESiP EP-1 Evaluation Board.

How to Read This Manual It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, microcontrollers, SRAM, page ROM, and SDRAM.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Active low representation:	xxxZ (Z after pin or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ..... XXXX or XXXXB
	Decimal XXXX
	Hexadecimal ...XXXXH
Prefix indicating power of 2	
(address space, memory capacity):	K (kilo): $2^{10} = 1,024$
	M (mega): $2^{20} = 1,024^2$
	G (giga): $2^{30} = 1,024^3$
Data type:	Word … 32 bits
	Half-word … 16 bits
	Byte … 8 bits

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such. Furthermore, some related documents may be intended for individual customers, because the documents are prepared in the development/planning stage of each core.

Documents Related to PFESiP EP-1 Series

Document Name	Document No.
V850E2 Architecture User's Manual	U17135E
PFESiP EP-1 Series Design Manual	A19068E
PFESiP/V850EP1 Product Data User's Manual	A19069E
PFESiP/V850EP1 Hardware (CPU Functions) User's Manual	A19070E
PFESiP/V850EP1 Hardware (USB Functions) User's Manual	A19071E
PFESiP/V850EP1 USB Function Setting Example Application Note	A19349E

Documents Related to PFESiP EP-1 Evaluation Board

Document Name	Document No.
PFESiP EP-1 Evaluation Board Technical Information User's Manual	A19350E
PFESiP EP-1 Evaluation Board Ordering Information User's Manual	This manual
PFESiP EP-1 Evaluation Board FPGA Design Guide User's Manual	A19351E
PFESiP EP-1 Evaluation Board Lite Technical Information User's Manual	A19354E

Documents Related to Development Tools (User's Manuals)

Document Name			Document No.
RX850 Pro (Real-Time OS)	Ver.3.21	Basics	U18165E
	Ver.3.20	Installation	U17421E
	Ver.3.21	Technical	U18164E
	Ver.3.20	Task Debugger	U17422E
PM+ Ver.6.30 Project Manager			U18416E
QB-V850MINI On-chip Debug Emulator			U17638E
ID850QB Ver.3.20 Integrated Debugger	Operation		U17964E
RX850V4 Ver.4.22 Real-Time OS	Fanctionalities		U16643E
	Task Debugger		U16811E
AZ850V4 Ver.4.10 System Performance Analyzer			U17093J

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CHAPTER 1 INTRODUCTION

The PFESiP EP-1 Evaluation Board is a development evaluation board for assisting the development of PFESiP EP-1 Series products.

It can be used for the software development of the PFESiP EP-1 Series-dedicated microcontroller PFESiP/V850EP1 and for user logic development and verification using the on-board FPGA.

The PFESiP/V850EP1 has an on-chip high-performance 32-bit RISC-type CPU core (V850E2 (NBA85E2S) core).

The basic functions of PFESiP EP-1 Series products based on the PFESiP/V850EP1 can be evaluated using this board.

As the on-board FPGA, the Virtex®-4 Family LX Series made by Xilinx® is employed and the XC4VLX40 is mounted as standard. The FPGA size can be changed.

1.1 Overview of PFESiP EP-1 Evaluation Board

The PFESiP EP-1 Evaluation Board is a development evaluation board for assisting the development of PFESiP EP-1 Series products.

It can be used for the software development of the PFESiP EP-1 Series-dedicated microcontroller PFESiP/V850EP1 and for user logic development and verification using the on-board FPGA.

The functions of the embedded array (EA-9HD) that is provided with the user logic paired with the PFESiP/V850EP1 within the PFESiP EP-1 Series SiP can be used for developing and verifying the user logic by integrating the functions into the on-board FPGA (Virtex-4 Family LX Series made by Xilinx).

A more systematic evaluation can be performed by connecting the PFESiP EP-1 Evaluation Board to the user board using system expansion connectors. Furthermore, on-board memory required for a general system is also provided.

Note that the load capacitance of the PFESiP EP-1 Evaluation Board is not always equivalent, in contrast to the environment of actual SiP products, because the signals originally connected within the SiP are connected to the FPGA on-board.

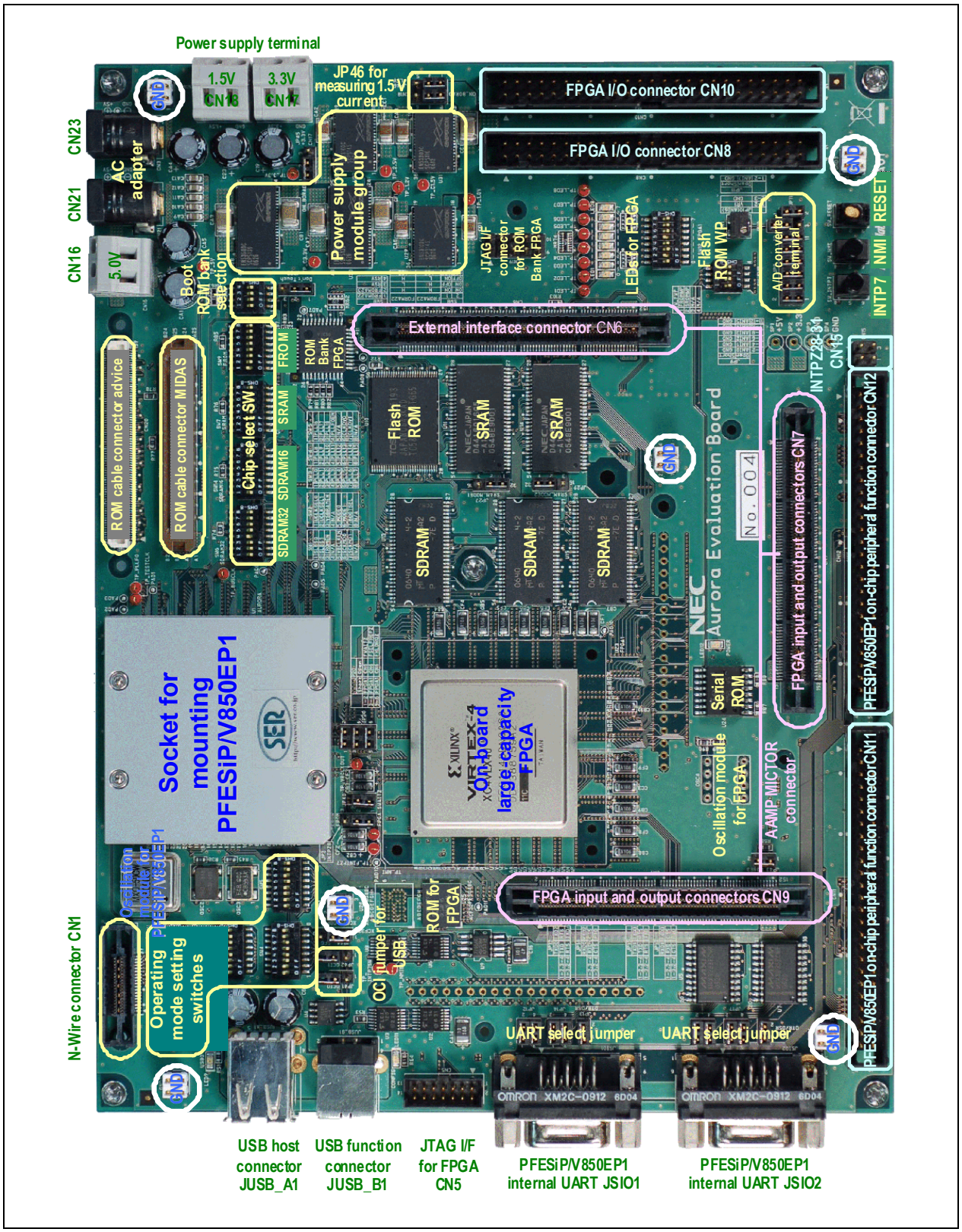
Remarks 1. The PFESiP EP-1 Evaluation Board is provided with expansion connectors compatible with the MICROSSP Evaluation Board. A stack board developed for the MICROSSP Evaluation Board can also be used for the PFESiP EP-1 Evaluation Board by programming the on-board FPGA.

2. See the PFESiP/V850EP1 User's Manual for the functions and specifications of the PFESiP/V850EP1.

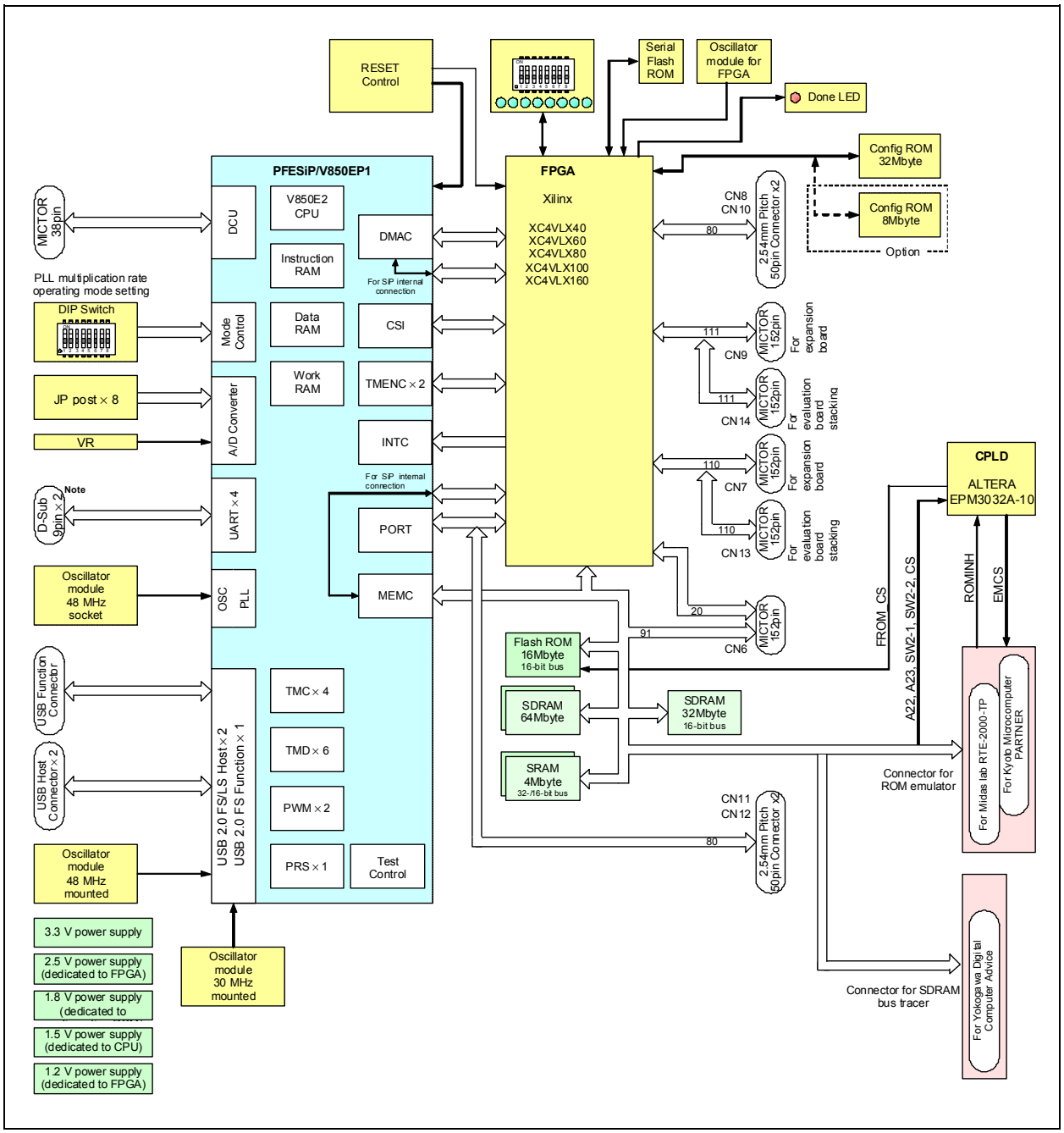
1.2 Appearance and Function of Each Part of PFESiP EP-1 Evaluation Board

The appearance and the function of each part of the PFESiP EP-1 Evaluation Board are shown below.

Figure 1-1. Function of Each Part



1.3 Summarized Block Diagram of PFESiP EP-1 Evaluation Board



CHAPTER 2 PFESiP EP-1 Evaluation Board ORDERING INFORMATION

Variations with different FPGA types mounted and provided or not provided with sockets and plugs for stacking can be selected for the PFESiP EP-1 Evaluation Board according to the application. A representative selection of the PFESiP EP-1 Evaluation Board is described below.

2.1 FPGA Selection

The PFESiP EP-1 Evaluation Board employs the Virtex®-4 Family LX Series made by Xilinx as the on-board FPGA. The FF1148 package is employed and an FPGA can be selected from FPGAs with a different capacitance and speed grade, but with a common footprint pattern. The number of I/Os that can be used is the same for any FPGA selected.

The XC4VLX40 is selected as the FPGA mounted as standard. When mounting an FPGA other than the XC4VLX40, conditions regarding the quantity may be added.

2.2 Ordering Restriction, Etc.

2.2.1 Delivery date, etc.

The PFESiP EP-1 Evaluation Board is manufactured on order. The delivery date is reported to the customer by summing up the approximate time required for procuring the components, manufacturing, evaluation, and packing.

2.2.2 Dedicated AC adapter

A dedicated AC adapter common to the MICROSSP™ Evaluation Board and PFESiP EP-1 Evaluation Board is optionally provided. Power can be supplied by using a lead wire from an external stabilization power supply. When wishing to use the dedicated AC adapter, request it optionally.

2.3 Standard Specifications of PFESiP EP-1 Evaluation Board

The standard specifications of the PFESiP EP-1 Evaluation Board are shown below.

Table 2-1. Standard Specifications of PFESiP EP-1 Evaluation Board

Item	Standard Specifications					
PFESiP/V850EP1 mounting method	■ Directly mounted					
FPGA size	Mounted FPGA	Size of reference circuit, equivalent to CB-IC	Logic cells	Distributed RAM	Block RAM	Number of I/Os
	■ XC4VLX40	350 K gates	41,472	288Kbit	1,728Kbit	640
FPGA speed grade	■ –11 (medium speed)					
FPGA mounting method	■ Directly mounted					
MICTOR connector	■ AMP MICTOR receptacle		AMP MICTOR receptacle is mounted.			
Dedicated AC adapter	■ None					

2.4 Selectable Specifications of PFESiP EP-1 Evaluation Board

The specifications can also be selected from the following detailed options, depending on conditions such as those regarding the quantity. Use the following table as a checklist when requesting an order. Contact NEC Electronics for the validity of a selection.

Table 2-2. Selectable Specifications of PFESiP EP-1 Evaluation Board

Item	Selectable Specifications					
PFESiP/V850EP1 mounting method	□ Directly mounted (standard)					
	□ Mounted on socket					
FPGA size	Mounted FPGA	Size of reference circuit, equivalent to CB-IC	Logic Cells	Distributed RAM	Block RAM	Number of I/Os
	□ XC4VLX40	350 K gates	41,472	288Kbit	1,728Kbit	640
	□ XC4VLX60	500 K gates	59,904	416Kbit	2,880Kbit	
	□ XC4VLX80	650 K gates	80,640	560Kbit	3.600Kbit	
	□ XC4VLX100	900 K gates	110,592	768Kbit	4,320Kbit	
	□ XC4VLX160	1,250 K gates	152,064	1056Kbit	5,184Kbit	
FPGA speed grade	□ –10 (low speed) □ –11 (medium speed: standard specification) □ –12 (high speed)					
FPGA mounting method	□ Directly mounted (standard)					
	□ Mounted on socket					
MICTOR connector	□ None		Two 50-pin general-purpose connectors are mounted. In this case, the FPGA connection test is not performed.			
	□ AMP MICTOR receptacle		AMP MICTOR receptacle is mounted.			
	□ AMP MICTOR plug		AMP MICTOR plug is mounted (used for stacking the PFESiP EP-1 Evaluation Boards).			
Dedicated AC adapter	□ None	–				
	□ Included	Dedicated AC adapter common to MICROSSP Evaluation Board and PFESiP EP-1 Evaluation Board				

CHAPTER 3 DEVELOPMENT TOOLS AND MIDDLEWARE

The following development tools and middleware are provided for developing systems using the PFESiP/V850EP1.

3.1 Development Tools

Real-Time OS	Compiler	Debugger	Server	In-Circuit Emulator	Remark
RX850pro (NEC Electronics Corporation)	CCV850 Note 1 (Green Hills Software, Inc.)	MULTI (Green Hills Software, Inc.)	rteserve (Advanced Data Controls Corp.)	RTE-2000-TP (Midas lab Inc.) RTE-2000H-TP (Midas lab Inc.)	No. of traces: 8
			YDCSERVE Note 2 (Advanced Data Controls Corporation)	advicePLUS (Yokogawa Digital Computer Corporation)	No. of traces: 8
		MicroVIEW-PLUS (Yokogawa Digital Computer Corporation)	–	advicePLUS (Yokogawa Digital Computer Corporation)	No. of traces: 8
	CA850 (NEC Electronics Corporation)	ID850QB Note 3 (NEC Electronics Corporation)	N-EXEC (Midas lab Inc.)	RTE-2000-TP (Midas lab Inc.) RTE-2000H-TP (Midas lab Inc.)	No. of traces: 8
			–	QB-V850MINI (NEC Electronics Corporation) (MINI CUBE)	No trace function
		PARTNER Note 4 (Kyoto Microcomputer Co., Ltd.)	–	PARTNER-Jet (Kyoto Microcomputer Corporation)	No. of traces: 4

Notes 1. Ver. 4.0, which supports pipeline optimization, is recommended for utilizing the performance of the V850E2 CPU.

2. “IDE FOR V800 WITH YDCSERVE”, which integrates CCV850, Multi, and YDCSERVE is also provided.

3. QB-V850MINI is provided with ID850QB.

4. PARTNER-Jet is provided with PARTNER.

3.2 Middleware

The PFESiP/V850EP1 has an on-chip USB host controller and USB function controller.

Generally, to use the USB function, a driver for the microcontroller provided with the USB function is required. Accordingly, the mass storage class sample driver of the USB function controller is provided.

USB driver package products are provided by GRAPE SYSTEMS INC.

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