RENESAS

8A3xxxx 48QFN

Evaluation Kit

Description

The 8Axxxx 48QFN EVK allows customers to evaluate Renesas' ClockMatrix (CM) devices (for example, 8A34043, 48QFN). This document discusses the following:

- The board's design, its power supply, and jumper settings
- The input and output connectors for normal operation
- How to bring up the board using the Timing Commander[™] software GUI
- How to configure and program the board to generate standard-compliant frequencies

Kit Contents

- 8A34xxx 48QFN Evaluation Board
- USB Type A cable

PC Requirements

- Renesas <u>Timing Commander™ Software</u> installed
- ClockMatrix GUI
- USB 2.0 or USB 3.0 interface
- Windows XP SP3 or later
- Processor: Minimum 1GHz
- Memory: Minimum 512MB; recommended 1GB
- Available disk space: Minimum 600MB (1.5GB 64-bit); recommended 1GB (2GB 64-bit)
- Network access during installation if the .NET framework is not currently installed on the system



Figure 1. 8A3xxxx 48QFN Evaluation Board



Contents

1.	Boar	d Design	3		
	1.1	Board Power Supply	4		
	1.2	Voltage Selection Jumpers	4		
	1.3	GPIO Switches, LEDs, and Test Points	5		
	1.4	USB Jack	5		
	1.5	Onboard EEPROM	5		
	1.6	I ² C /SPI Auxiliary Path Specifications	6		
2.	Work	Working with Timing Commander for Programing and Configuration			
	2.1	Default Operation	6		
	2.2	Using Timing Commander to Control the Board	8		
	2.3	Output Terminations and Rework to Receive a 1PPS Input	.12		
3.	How	to Upgrade the Firmware	.13		
	3.1	Upload Firmware to the RAM	.13		
	3.2	Upload Firmware into the EEPROM	.15		
	3.3	Verify the EEPROM Programming	.16		
4.	Sche	matic Diagrams	.17		
5.		ring Information			
6.	Revis	sion History	.17		

Figures

Figure 1. 8A3xxxx 48QFN Evaluation Board	1
Figure 2. 8A3xxxx 48QFN Evaluation Board – Detailed	3
Figure 3. Example of Voltage Jumpers	4
Figure 4. GPIO Setting and Status Display Area	5
Figure 5. Board Setting for Default Operation	7
Figure 6. Starting Up Timing Commander GUI	8
Figure 7. Selecting 8A34001 Using Personality File v4.6	9
Figure 8. Timing Commander GUI with a Settings File Opened	9
Figure 9. Setting I ² C for Connecting the Board with GUI	10
Figure 10. Green Band Appears when a Valid Connection is Made	10
Figure 11. Firmware Version Mismatch Warning Message	
Figure 12. Reading Firmware Version	11
Figure 13. Read Firmware Version of ClockMatrix Chip	11
Figure 14. AC Coupling and Terminations for Input Clock	12
Figure 15. Configuring CLK0 as CMOS to Receive a 1PPS Input	

1. Board Design

The following diagram identifies various components of the board: input and output SMA connectors, power supply jacks, and some jumper settings necessary for the board operations.



Figure 2. 8A3xxxx 48QFN Evaluation Board – Detailed

- Input SMA connectors There are two differential inputs labeled CLK0/nCLK0–CLK1/nCLK1. Each input clock can be configured differentially (LVDS, PECL 2.5V, and PECL 3.3V) or in single-ended format (CMOS).
- Output SMA connectors There are four outputs labeled as Q8/nQ8–Q11/nQ11. Each output clock can be configured differentially (LVDS, LVPECL, or user-defined amplitude), or in single-ended format (LVCMOS – in-phase or out-of-phase).
- GPIO switch, LEDs, and test points There are eight GPIOs available. Each GPIO can be set a "low" or "high" level (if input) or displayed with an LED (if output). Some GPIOs are used to set the chip in a certain working condition on power-up. For more information, see GPIO Switches, LEDs, and Test Points.
- **USB connector** A USB mini-connector connects the evaluation board to a PC for GUI communications. No power is drawn from the USB connector other than to power the FTDI USB chip.
- VCCO voltage selection jumpers Each output voltage can be individually supplied with 1.8V, 2.5V, or 3.3V. These jumpers are used to select the voltage for the output voltages.
- Reset button A small button is used to reset the board.
- OSCI Input connector An SMA connector, J45, can optionally supply a clock signal to overdrive the crystal.
- **OCXO/TCXO reference** An SMA connector, J46, can supply a local OCXO/TCXO reference as an optional reference for System DPLL.
- **Crystal** A crystal of various frequencies must be present for board operations. A 3225 footprint is provided for SMT crystals. For easy plug-in of a canned crystal, two through holes are also available.
- **EEPROM** An SO-8 socket is provided to hold an EEPROM device of compatible package. EEROM is used to store firmware and customer configuration data, if needed.

1.1 Board Power Supply

The board uses a single +5V supply for its power supplies. When running the board, set the bench power supply at 5V/2A. The red jack (J1) is positive; the black jack (J2) is the ground.

Multiple LDOs are used to generate 3.3V, 2.5V, and 1.8V from the +5V supply.

1.2 Voltage Selection Jumpers

There are nine headers/jumpers to select different voltages for different functional blocks of the chip. Each head is labeled pin 1 and pin 3 – jumping pin 1 and pin 2 will select 3.3V; jumping pin 2 and pin 3 will select 2.5V; no jumper will have 1.8V.

See the following example for JP4 and JP9 – JP4 will select 2.5V; JP9 will select 3.3V.



Figure 3. Example of Voltage Jumpers

The following list shows which head/jumper is used to select what voltage:

- JP1 VDDD
- JP2 VDDA
- JP3 VCC_GPIO_DC
- JP4 VDDO_Q8_3_5
- JP5 VDDO_Q2_4_11
- JP6 VDDO_1_10_7
- JP7 VDD_CLK0
- JP8 VDD_CLK1
- JP9 VDDO_Q0_9_6

1.3 GPIO Switches, LEDs, and Test Points

An 8-bit dip switch sets the logic levels for eight GPIOs. The following table shows the GPIO levels for each setting and the corresponding LED state.

Dip Switch Position	GPIO Logic Level	LED
Left	Low	On
Center	High if GPIO is configured as Input	High if GPIO is configured as Input
Center	High or Low according to the GPIO output setting	High or Low according to the GPIO output setting
Right	High	Off

See the picture and labels in Figure 4.

When the GPIOs are configured as outputs (such as User-Controlled or LOL indicator), the dip switch for the corresponding GPIO should be placed in the center position. The LED will indicate the state of the GPIO.



Figure 4. GPIO Setting and Status Display Area

1.4 USB Jack

The board has a USB mini-connector. The other end of the USB cable is a USB Type A connector going to a PC.

1.5 Onboard EEPROM

An onboard EEPROM is used to store device firmware and/or customer's configuration data. There are two headers/jumpers, JP10 and JP11, used to select the I²C communication paths for the EEPROM.

	JP10/JP11	JP10/JP11	
Jumper Position	Both Pin 1 and 2	Both Pin 2 and 3	
EEPROM I ² C Path	FDTI and EEPROM	EEPROM and CM Chip	

1.6 I²C /SPI Auxiliary Path Specifications

I²C and SPI connections can be configured using onboard jumpers. There are four headers/jumpers that control the auxiliary serial stream signals.

	JP12/JP13	JP12/JP13	JP14/JP15	JP14/JP15
Jumper Position	Pin 1 and 2	Pin 2 and 3	Pin 1 and 2	Pin 2 and 3
CM Chip Serial Port Path	SCLK/SDA Connected to on-board FTDI I ² C Chip (Default)	SCLK/SDA Connected to J4 for external I ² C/SPI controller use	NONE	SDI/nCS Connected to J4 for external I ² C/SPI controller use

Table 3. I²C/SPI Path Connections

2. Working with Timing Commander for Programing and Configuration

The following sections are best cross-referenced with the <u>ClockMatrix GUI Step-by-Step User Guide</u> that is available on the <u>ClockMatrix Timing Solutions</u> page and various ClockMatrix device product pages.

2.1 Default Operation

The board can operate off an EEPROM that has stored all information including firmware and a default configuration data. A default operation provides a sanity check on the board before running the board through the Timing Commander. Set the board in the following default conditions (see Figure 5 for jumper and switch positions).

- Set all the GPIOs to the center position. This will ensure that GPIO8 and GPIO9 are high and that the serial port is configured for I²C 1 byte addressing.
- VDDA = 3.3V, VCC_GPIO_DC = 3.3V, and VDDO_Qx = 3.3V
- Crystal frequency = 50MHz
- CLK0 = 25MHz
- EEPROM is connected to ClockMatrix chip through an I²C bus by jumping Pin 2 and 3 of JP10 and JP11

With the above default conditions ready, connect the board to the PC using a USB type A to USB mini cable and power up the board using a single +5V supply. On power-up, the ClockMatrix chip reads its firmware and configuration data from EEPROM and updates all registers. When this process is completed, the following frequencies are available:

- Q0 = 122.88MHz
- Q1 = 122.88MHz



Figure 5. Board Setting for Default Operation

2.2 Using Timing Commander to Control the Board

Once the default operation is successful, complete the following steps to configure and program the ClockMatrix device per your specific application requirements using Timing Commander GUI tools:

- 1. Power up the board and set the main serial port in I²C mode by GPIO9 = "high". Set GPIO8 = "high". Connect the board to the PC.
- 2. Start the Timing Commander software. You will see options of "New Settings File" and "Open Settings file". For a new configuration, select "New Settings File".

IDT Timing Commander New Settings File Open Settings File DT Timing Web Site User Guide	IDT Timing Commander	
	New Settings File	The settings File

Figure 6. Starting Up Timing Commander GUI



3. After selecting "New Settings File", a device selection window will pop-up. In the window, choose the intended device in the list (in this example, 8A34001 is selected). Click the button at the lower right corner of the window (red circle) to browse and select the correct personality file (in this example, personality v4.6 is selected). Click *OK*.

New Settings File	e	Cancel	
Product #	Description	ClockMatrix	
8A34000			
8A34001		8A34001	
8A34002	8A34002		
Personality C:\Users\szhe	eng\Desktop\TC_personality Clocl	kMatrix_V5.1.0_PR4.6.tcp	

Figure 7. Selecting 8A34001 Using Personality File v4.6

4. The GUI window with the 8A34001 block diagram will open for configurations; or if "Open Settings File" is selected in Step 3, you will be prompted to browse and select an existing **.tcs** file and the personality file. When the configuration file is open, all configured values will be displayed (see Figure 8).

8A34001					1
Diagram	Bit Sets	Registers			
Q					
A34001 VS.1.0 TCXO/OCXO Immare: PR4.6.0	49.152MHz Configure		onfigure TODs	Firmware Utility	Implemented:
Display input and output labels			1003	Generate EEPROM Hex	Configure APLL & Input xtal Configure inputs (dW, type, Invert, etc) Configure channels, Inc Input priorities Configure DCD frequencies Enter desired output frequencies
Enable Frequency 100.708MHz	System APLL	Stage 0	156.25MHz	Desired: >156.25MHz 158.25	 Enter desired output requencies Configure outputs (dv, type, vdd, etc) 12C read/write to attached chip Update firmware SYNC pulse
SYNCE CLK0	Te DCOs	625MHz Channel C	User-Defined	REFCLK_P/N CDR1	Phase adjustment Support for Combo Mode Input monitoring configuration GPIO configuration SPI read/write to attached chip
	xo	SOOMHZ	C1 C1 C C C C C C C C C C C C C C C C C		* SPI readwrite to attached chip * PWM decoding of outputs * PWM encoding of outputs * Output TDC config * TOD config
			156.25MHz	Desired:	Implemented in UI, not working
201.418 CLK2 - C	KE: 0,1,2,3 DPLL Mode	625MHz 625MHz 625MHz Channel 1	C2 C2 C2 C2 C2 C2 C2 C2 C2 C2	► 156.25MHz 156.25 C	Won't implement initially
CLK10 100.705MHz	Channel 1	nilgure	User-Defined	Desired:	GPIO control of ref mode * IRIG-8 operation * EEPROM writing * Contourations
201.416 CLK3	Synthesizer	625MHz	156.25MHz	Desired	* JTAG Interface * OTP
		ntigure 937.5MHz Channel 2		► 156.25MHz 156.25	Debug Solution Finder 📄 📑
	Synthesizer	937.5MH2 Channel 2		Desired: 156.25MHz 158.25	Execution Log (name) Execution Log (count)
	Channel 3 DPLL Mode		LVCMOS	Desired:	Execution Log (time)
		Stage 3 n/a		err 🚺	
	Ks: 0,1,2,3 DPLL Mode	644.5312MHz Channel 3		Desired:	

Figure 8. Timing Commander GUI with a Settings File Opened



5. In order to connect the board with Timing Commander (PC), click the button (red circle) at the up-right corner of the GUI to set up the communication protocols (see Figure 8).

After I²C and one-byte addressing are selected, click *OK* to close the window.



Figure 9. Setting I²C for Connecting the Board with GUI

6. Click on the chip symbol at the upper-right corner to initiate the connection. The connection is valid when a green band appears at the upper-right corner of the window, as shown in Figure 10.

*	_		
		()	1 ×
	Firmware Utility	Implemented: 	
>Q0 ⇒nQ0 User-Defined	Cenerate EEPROM Hex Desired: >156.25MHz 156.25 REFCLK_P/N CDR1	Configure channels, inc input priorities Configure DCO frequencies Enter desired output frequencies Configure outputs (div, type, vdd, etc) I2C read/write to attached chip Update firmware SYNC pulse Phase adjustment Support for Combo Mode Input monitoring configuration	

Figure 10. Green Band Appears when a Valid Connection is Made

7. If ClockMatrix chip's firmware, or firmware loaded from EEPROM, has a different version from that in the Personality file, a firmware version mismatch warning message will appear. Click "Close" button to close the message window and a connection is made.



Figure 11. Firmware Version Mismatch Warning Message

8. Once the connection is made, the firmware version can be read within the GUI. Click the "Firmware Utility" button to bring up the Firmware Utility window, as shown in Figure 12.



Figure 12. Reading Firmware Version

9. Within the Firmware Utility window, click the "Get Firmware Version" button to read the firmware version.



Figure 13. Read Firmware Version of ClockMatrix Chip



10. In the case where the firmware version mismatches each other, a firmware upgrade is necessary to update the chip's firmware. To do so, complete the steps in How to Upgrade the Firmware to update the chip's firmware.

2.3 Output Terminations and Rework to Receive a 1PPS Input

All outputs are terminated with a 100Ω resistor across the output pair. When the output is configured as PECL2.5 and PECL3.3 or user-defined differential, the output clock will still be switching. The amplitude may be different from expected until the hardware termination matches the signaling type configured for the output.

The following rework must be implemented in order to support a 1PPS input clock. All input clocks for this board are AC-coupled and terminated as shown in Figure 14.



Figure 14. AC Coupling and Terminations for Input Clock

For a 1PPS input, a single-ended input with DC-coupling is recommended. As such, the populated AC-coupling capacitor must be removed and the input must be configured as LVCMOS, not differential.

1. In Figure 14, to make CLK0 supportive of 1PPS input, first configure CLK0 as LVCMOS in Timing Commander (see Figure 15).



Figure 15. Configuring CLK0 as CMOS to Receive a 1PPS Input

 Once in LVCMOS mode, CLK0_P and CLK0_N will be two separate LVCMOS inputs instead of a differential pair. To make CLK0_P receive a 1PPS input, replace C881 with a 0Ω resistor; and at the same time, remove R765 and R770.

3. How to Upgrade the Firmware

3.1 Upload Firmware to the RAM

- 1. Connect to the EVK board.
- 2. Power up the board with no EEPROM present. This ensures the firmware is 4.0.2.7017, as displayed in the figure.
- 3. The GUI will indicate that the firmware on the chip does not match the GUI firmware. Press "Close".



4. Open the "Firmware Utility" window by clicking on the button as follows.



5. Update the Firmware first. Press "Update RAM to Current FW Only".

Contract Tell Print T. L. Prilling, Manhood, St.	8
Firmware Utility	
Firmware supported by personality: pipeline: 13403	
Get Firmware Version Reset Board	
Update RAM	
Update RAM to Current FW Only	
ЕЕРROM Туре: 24x1025 🔽 🗂	
Write Firmware to EEPROM Only	
Verify Firmware on EEPROM Only	
Erase EEPROM Firmware	

6. In the next window, press "Yes" and wait around 3-4 minutes.



7. Once the firmware is updated, the following window will indicate a successful update. Click "Close".



8. Press "Get Firmware Version" to verify that the RAM was updated correctly, then click "Close".

		Firmware Utility	
	-	Firmware supported by personality: pipeline: 13403	
	_	Get Firmware Version Reset Board	
	To C	Update RAM	
		Update RAN to Current FW Only	
-		EEPROM Type: 24x1025 -	
		Close	
	Firmware version: 4.6.0.13403.103467		

3.2 Upload Firmware into the EEPROM

- 1. Once the firmware has been updated to the chip (steps 1 to 8), install the EEPROM on the EVK board.
- 2. Press "Write Firmware to EEPROM Only".

<u>Firmware Utility</u>				
Firmware supported by personality: pipeline: 13403				
Get Firmware Version Reset Board				
Update RAM				
Update RAM to Current FW Only				
EEPROM Type: 24x1025 -				
Write Firmware to EEPROM Only				
Verify Firmware on EEPROM Only				
Erase EEPROM Firmware				

3. In the next window, press "Yes".



4. When asked to "Verify" the EEPROM, press "No".



5. In the next window, press "Close" to start the EEPROM write.



6. Wait about 5 minutes for the EEPROM write to complete. Click "Close" in the following window.



3.3 Verify the EEPROM Programming

- 7. Power cycle the board.
- 8. Disconnect and reconnect to the chip.
- 9. Read back the firmware version to ensure it is correct (see steps 3 to 7).

4. Schematic Diagrams

For schematic diagrams, see <u>ClockMatrix 48QFN Evaluation Board Schematic</u>.

5. Ordering Information

Part Number	Description
8A34043-EVK	8A3xxxx 48QFN Evaluation Kit

6. Revision History

Revision	Date	Description
1.01	Jun 3, 2025	 Reformatted to the latest Renesas template. Removed embedded schematics and added a web link to the schematics in section 4.
-	Feb 15, 2019	Initial release.

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