8V19N49x

Evaluation Board Manual

This document describes following about the 8V19N49x Evaluation Board (EVB). This board can be used to evaluate the 8V19N490B, 8V19N490-19, 8V19N490-24, and 8V19N491-36 devices. In this document, the 8V19N490B is used as an example.

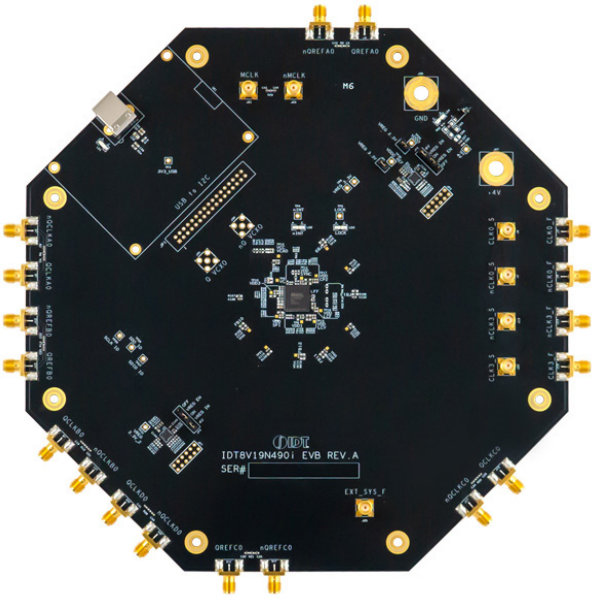
- Basic hardware and GUI setup
- Board power-up instructions
- Instructions to get active output signals using a provided configuration file
- Hardware modifications required for different conditions

Features

The board has SMA connectors to relevant I/O of the device:

- Two differential clock inputs
- Four differential clock outputs
- Three differential Sysref output, these outputs can also be configured to clock outputs
- One different output for direct VCXO buffer
- External VCXO
- Selectable output buffer voltage
- Laboratory power supply connectors
- Serial port for configuration and register read out

Board Diagram



PC Requirements

- Renesas Timing Commander Software installed
- 8V19N49X-XX GUI
- USB 2.0 or USB 3.0 Interface
- Windows XP SP3 or later
- Processor: Minimum 1GHz
- Memory: Minimum 512MB; recommended 1GB
- Available disk space:
  - Minimum 600MB (1.5GB 64-bit)
  - Recommended 1GB (2GB 64-bit)
- Network access during installation if the .NET framework is not currently installed on the system

Kit Contents

- 8V19N49x Evaluation Board
- USB Type A to Type B Cable
- *8V19N49x Evaluation Board Manual*

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Contents

1. Functional Description ... 3
1.1 Operational Characteristics ... 3
1.2 Setup and Configuration ... 3
1.2.1. Hardware Setup ... 3
1.2.2. Prepare the Software ... 4
1.2.3. Bring Up the GUI ... 5
1.2.4. Configure the Evaluation Board ... 8
1.2.5. Sysref Setup ... 9
2. Board Design ... 14
2.1 Schematic Diagrams ... 15
2.2 Bill of Materials ... 16
3. Typical Performance Graph ... 18
4. Ordering Information ... 19
5. Revision History ... 19

Figures

Figure 1. Labeled Board Image ... 4
Figure 2. 8V19N49X-XX BGA-100 Evaluation Board (Top) ... 14
Figure 3. 8V19N49X-XX BGA-100 Evaluation Board (Bottom) ... 15
Figure 4. Example Configuration Phase Noise ... 18

1. Functional Description

The 8V19N49x evaluation kit supports the evaluation of the 8V19N490B, a fully integrated FemtoClock RF Sampling Clock Generator and Jitter Attenuator. The device also supports JESD204B/C.

The 8V19N490B contains a two-stage PLL architecture. The first-stage PLL uses external VCXO and the second stage has an option to use an internal VCO. The internal VCO is built-in 2.94912GHz. This evaluation kit provides layout footprints for the first-stage external VCXO.

1.1 Operational Characteristics

When powering the board with a direct 4V supply, allow for excess current by setting the current limit to 1.5A. Before writing any registers to the device, roughly 0.72A should be seen pulled from the direct supply. The input voltage should not exceed 5V.

The board is designed to operate over the industrial temperature range from -40° to 85°C, ambient temperature.

It is recommended that the person operating the board use proper grounding to avoid ESD damage to the EVB.

1.2 Setup and Configuration

The setup and configuration is split into two separate areas being the hardware, GUI setup, and example Sysref output setup. The hardware setup consists of jumper orientations and a general overview of test instrument connection. The GUI setup shows how to establish a connection with the device through the Timing Commander software. Sysref output setup shows how to establish Sysref outputs for JESD204B compliance.

1.2.1. Hardware Setup

A direct 4V power supply should be attached to the evaluation board with the positive terminal at J27 and the ground source at J28. The USB type B cable should be connected at J26 and the computer that will be loading the Timing Commander software. For the initial setup, a differential clock source can be connected to CLK/nCLK and configured to 122.88MHz with 400mV to 800mV amplitude (there is on-board AC coupling and self bias).

For proper functionality out of the box, the jumpers on board should be placed to allow the correct voltages at each LDO and domain. The jumpers should be arranged as displayed in Table 1.

Table 1. Default Jumper Configurations

Jumper	Label	Default Orientation
JP6	4Vt o VREG_IN, VREG_EN to ON	ON, ON
JP2	4Vt o VREG_IN, VREG_EN to ON	ON, ON
JP4	VREG_3.3V - VDDO	ON
JP5	VREG_3.3V, VDDO_REF	ON
JP6	VREG_IN, VREG_EN	OFF

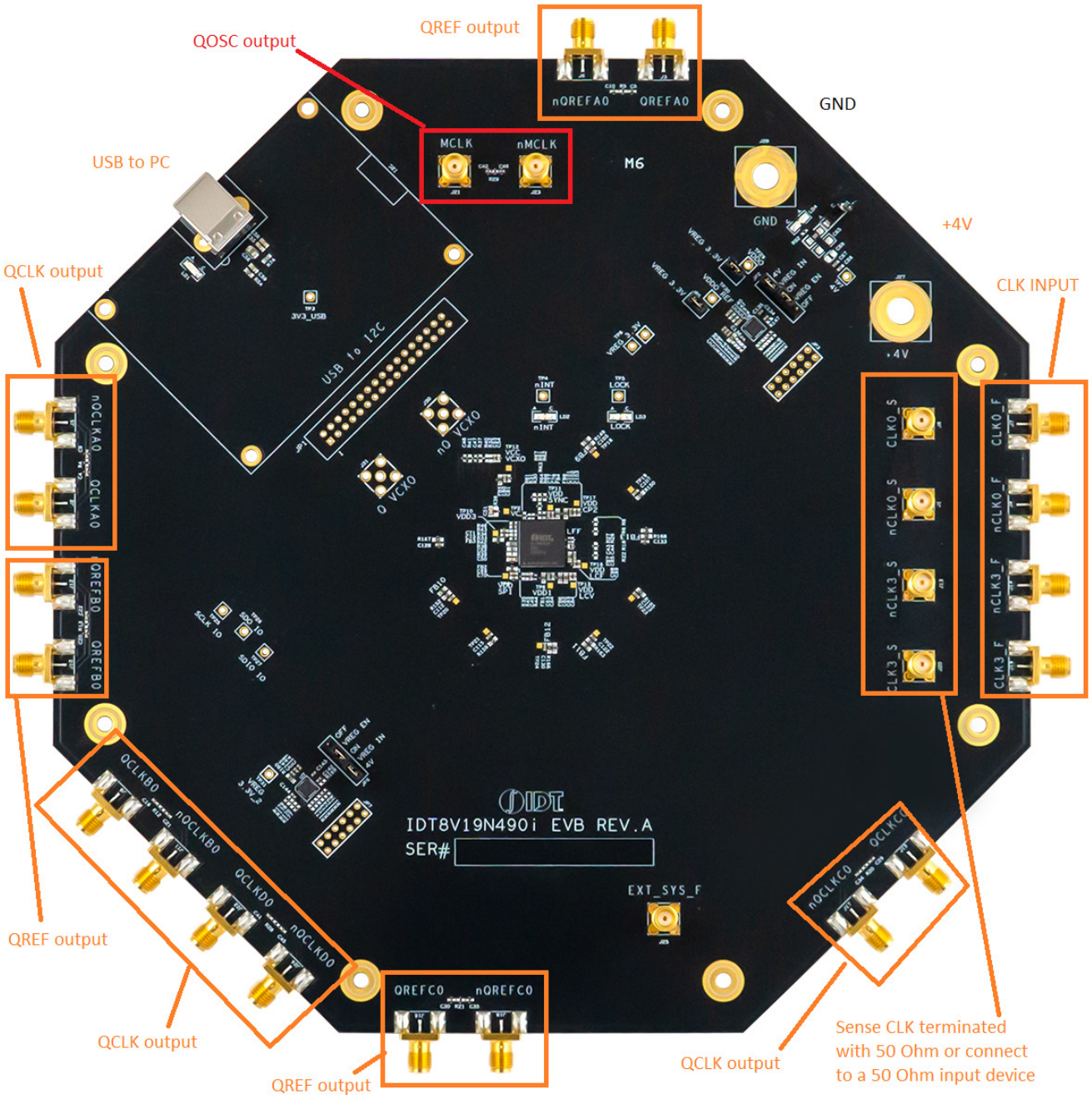


Figure 1. Labeled Board Image

1.2.2. Prepare the Software

1. Prior to starting the GUI, the Timing Commander software must be downloaded and installed.

   If Timing Commander is already installed on the computer, skip this step.

2. If the Timing Commander is not yet installed, please download and install the software from the Timing Commander product page.

3. After the software file is downloaded, double-click on TimingCommanderSetup.exe and follow the on-screen instructions to complete the setup.

1.2.3. Bring Up the GUI

1. After successfully installing the Timing Commander software, activate the software from the Window <start> at the bottom-left corner of the screen.
2. Start > IDT > Timing Commander.
3. Click <Open Setting File>.

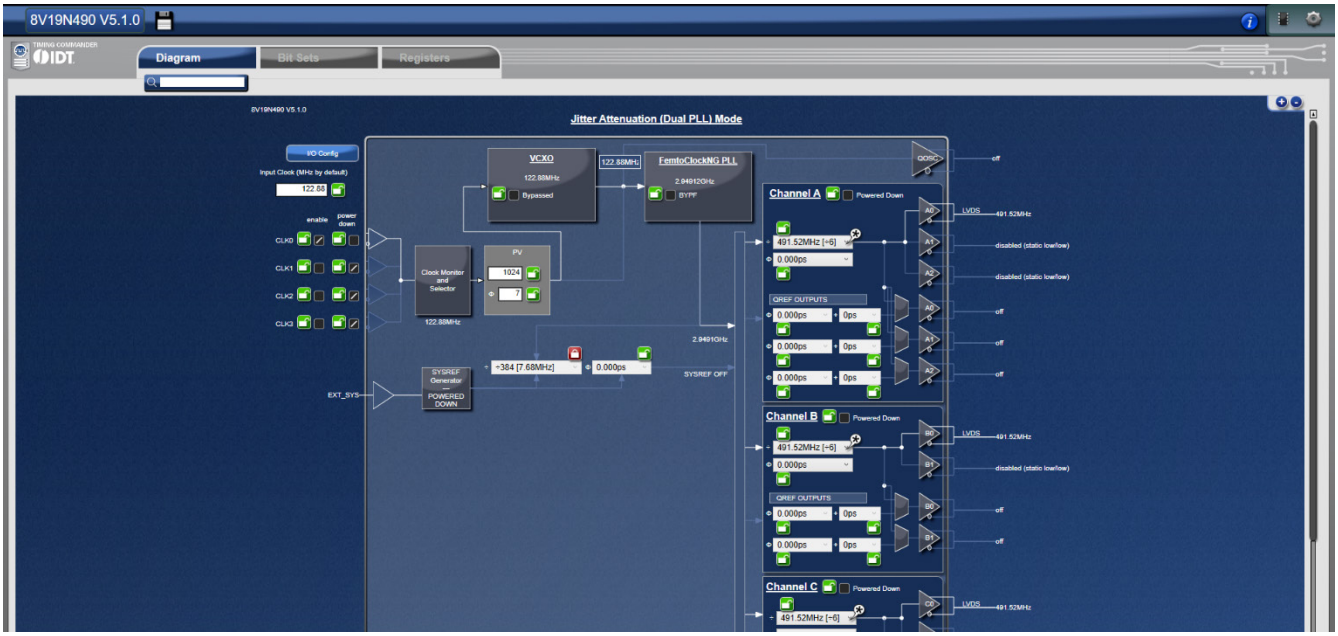
4. For the first-time use, if the proper part number does not appear, click the < Browse> button and select the settings file from the current working directory.

5. Select the example Timing Commander Settings file (.tcs) from the current working directory.
6. Click the < Browser> button to the choose Personality file from the folder.

   The latest version of the Timing Commander Personality file (.tcp) can be downloaded from the 8V19N49X-XX product page.

7. Select the personality file (.tcp) from the current working directory and click <Open>.

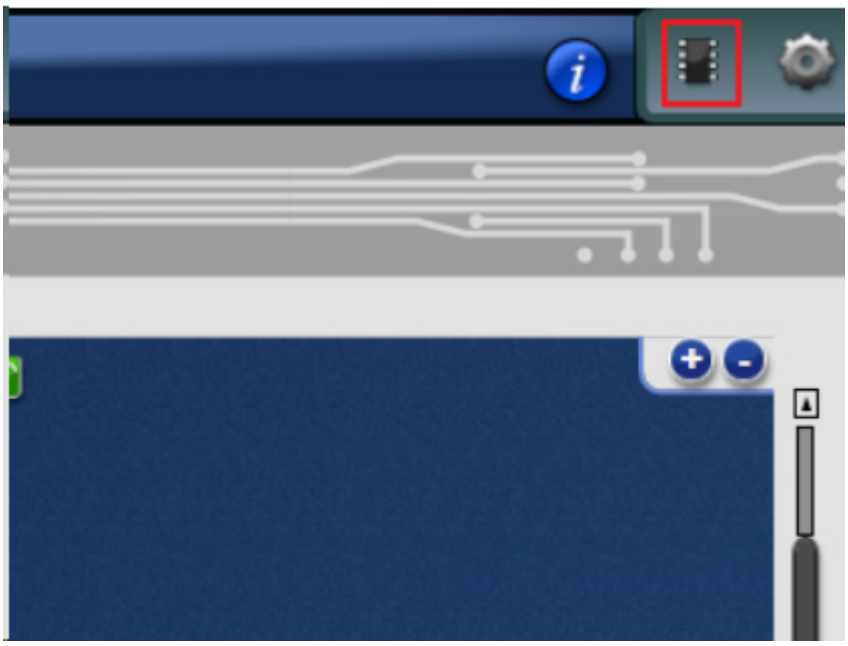
8. The GUI should display similar to the following screen. The input/output frequencies can be modified. Rolling your mouse wheel can zoom-in or zoom-out the display. If required, the parameters (e.g., input/output frequencies, charge pump, mux select etc.) can also be modified.



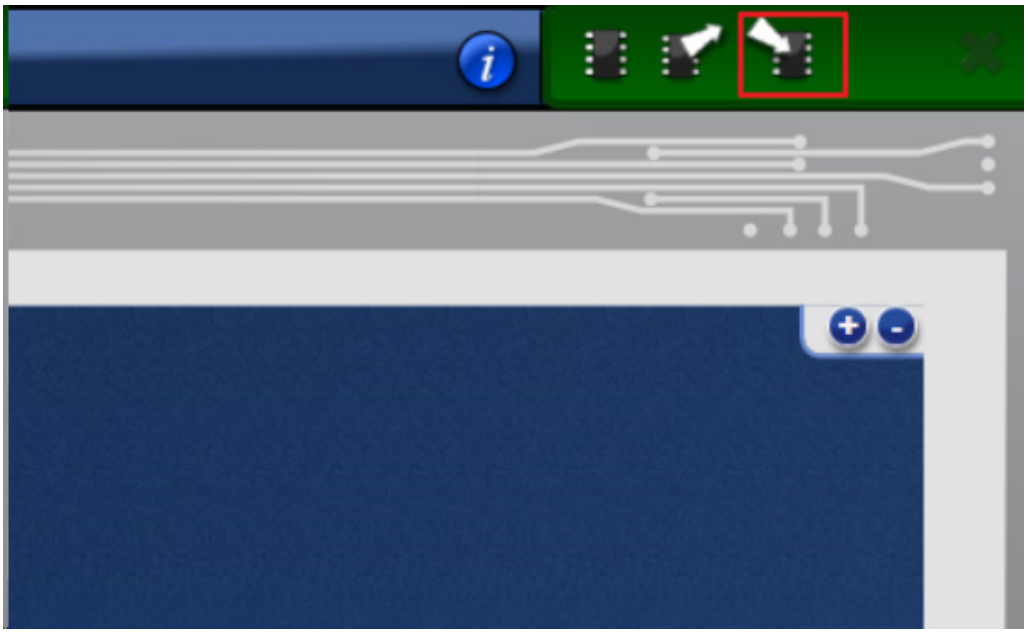
9. Click on any of the blocks to see the lower-level block diagram.

1.2.4. Configure the Evaluation Board

1. Click the top-right corner chip logo to establish a connection to the evaluation board.



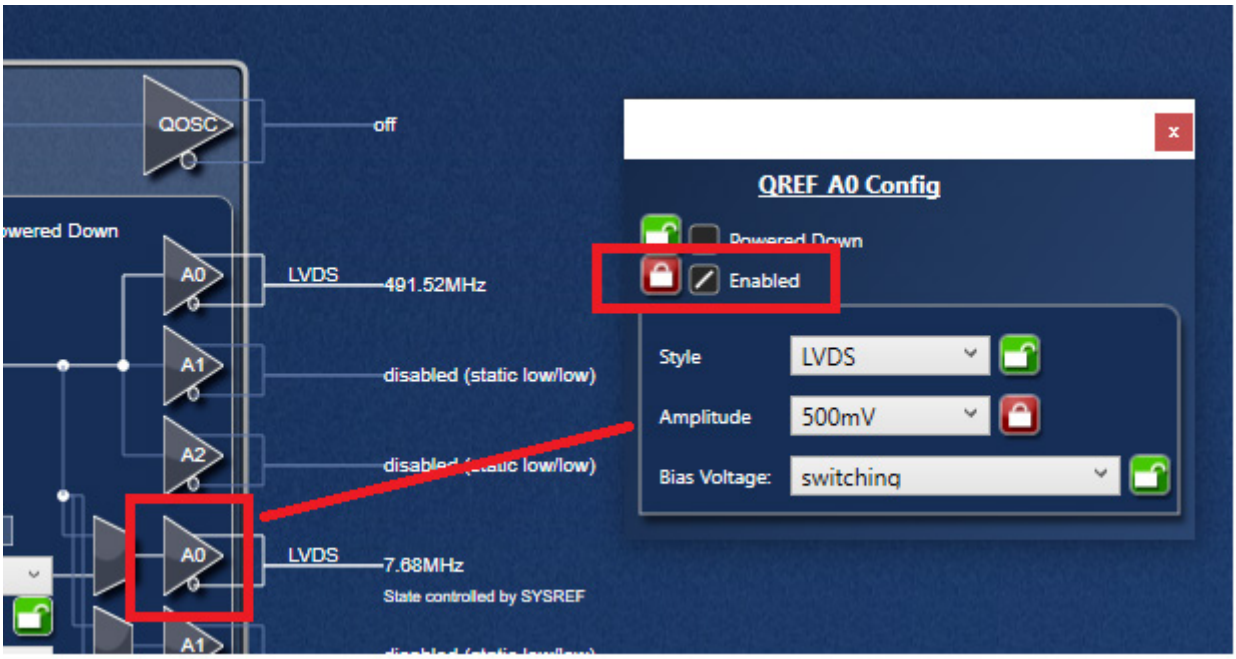
2. Click the arrow pointed down to the chip to write the data to the DUT registers.



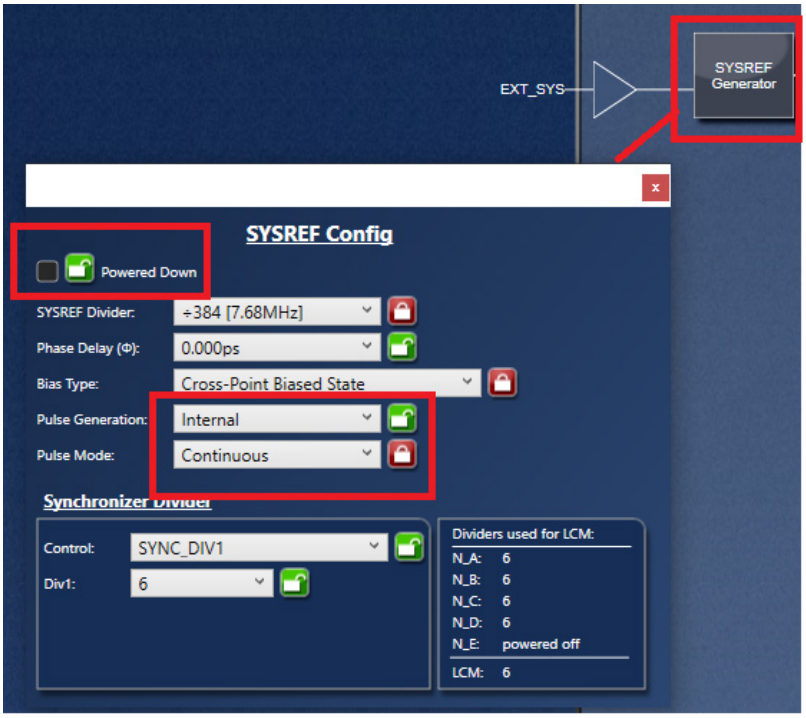
3. Click the <Initialize Device> button to activate the clock output.

1.2.5. Sysref Setup

1. Make sure the QREF output is Powered Up and Enabled.

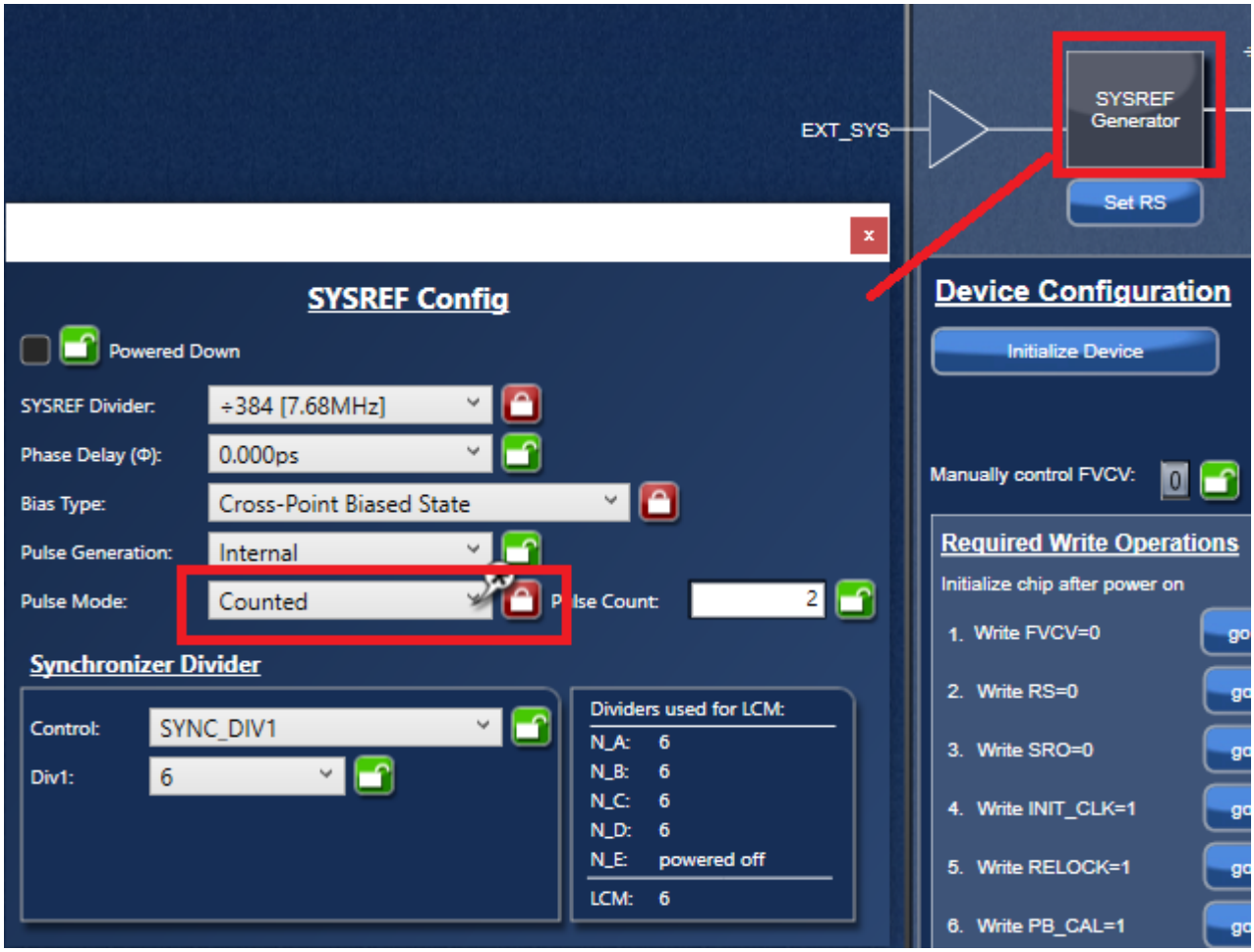


2. Double Click the SYSREF block.
   a. Make sure the SYSREF block is powered up.
   b. This example show <Internal Trigger>, <Continuous mode>.
      Note: If set to limit Count mode, make sure the scope captures in a single shot; otherwise the scope will not capture anything.

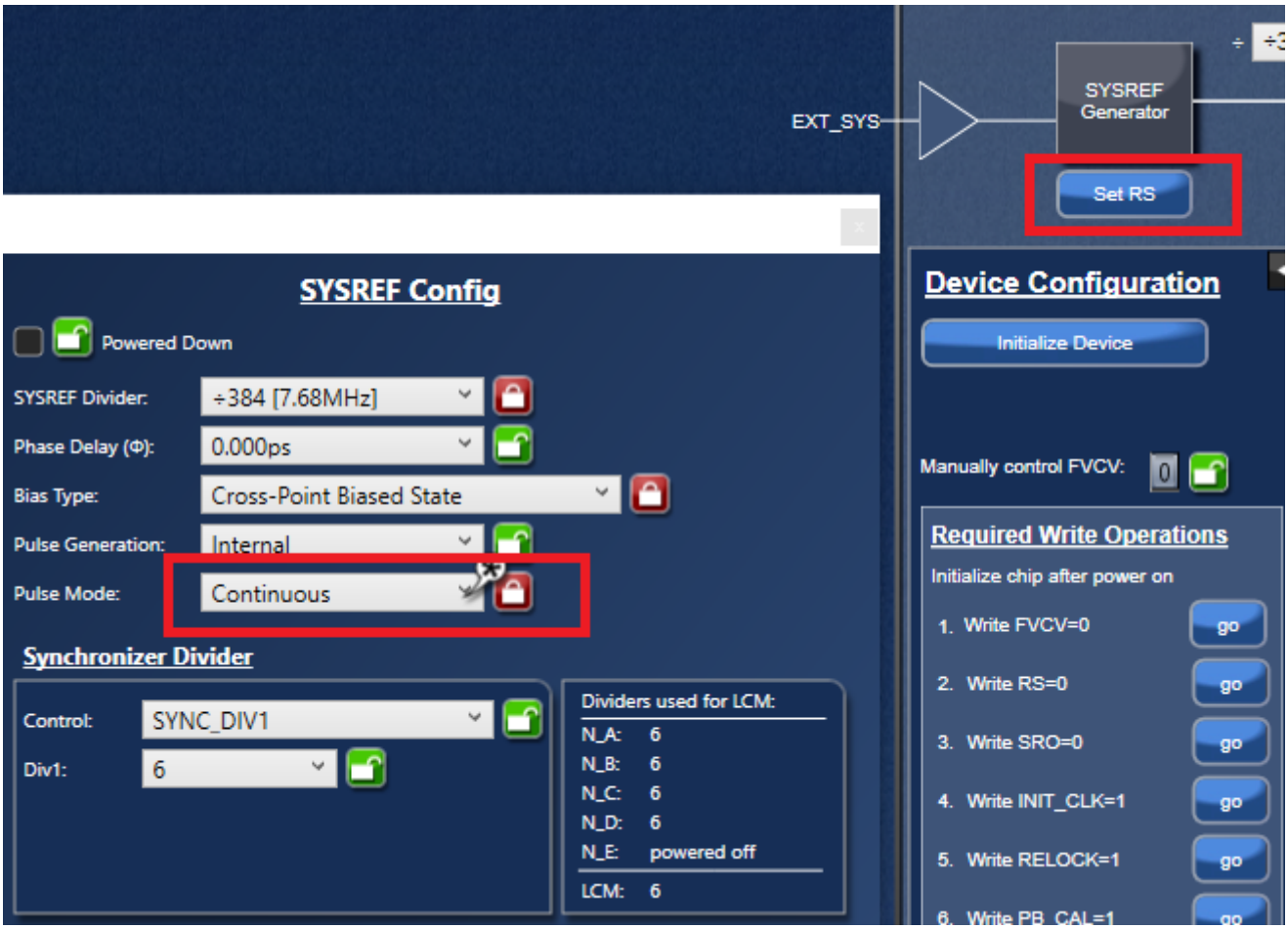


3. Power up and Write register data to the DUT.
4. After loading data after power up, click the <Initialize Device> button. The GUI will automatically write 1 to 9 as displayed below. The Write RS = 1 below is (write Register 70, D7 = 1). This activates the Sysref output. The Sysref (QREF) output should be active at this point.

5. To stop Sysref (QREF) output, change the Pulse mode to Limit Count. The Sysref output should stop at this point.



6. To re-activate the Sysref again.
   a. Change the Pulse mode to <Continuous>.
   b. Click the <Set RS> (This step Write R70, D7 = 1). The Sysref output should be active again at this point.



2. Board Design

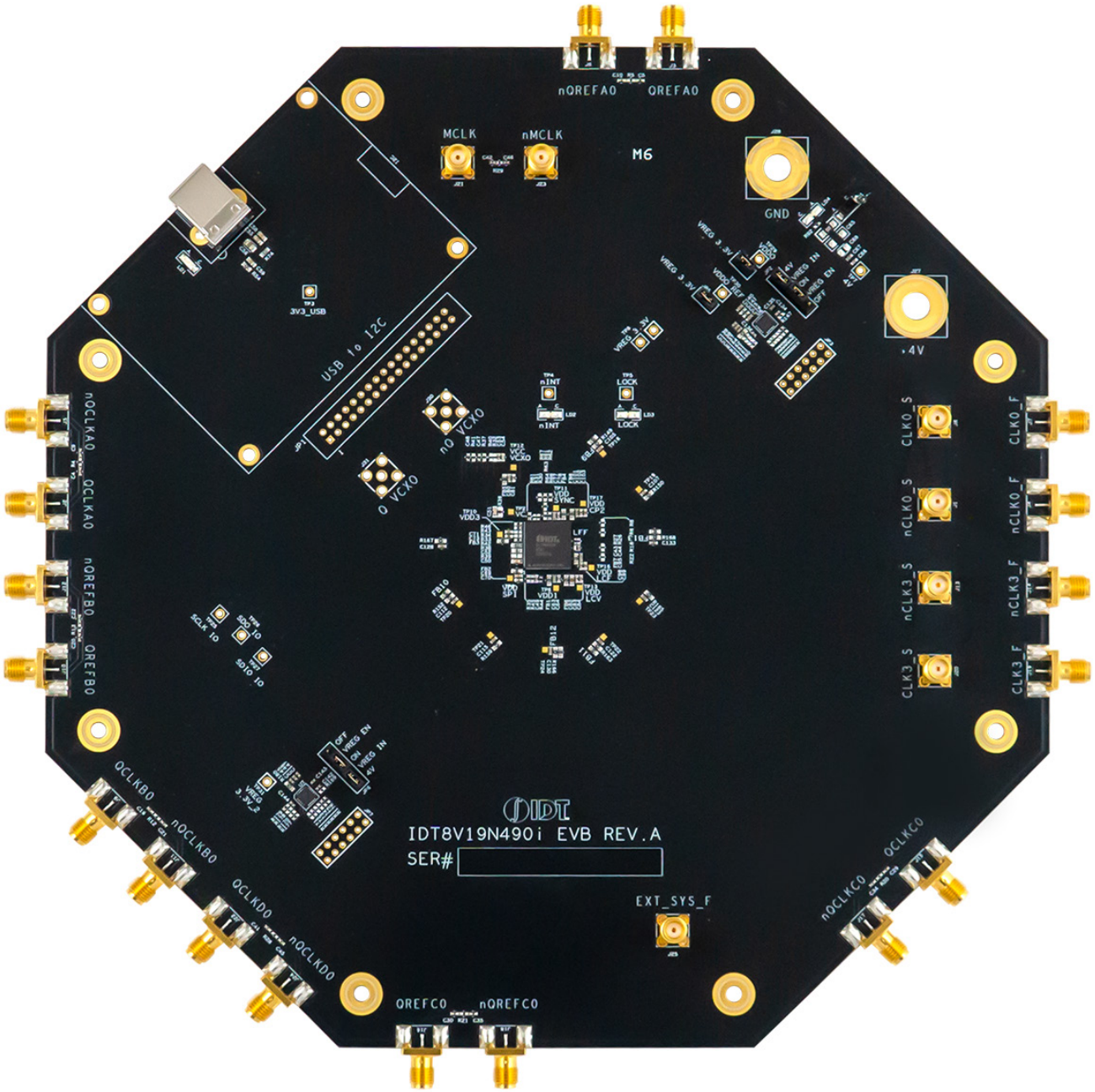


Figure 2. 8V19N49X-XX BGA-100 Evaluation Board (Top)

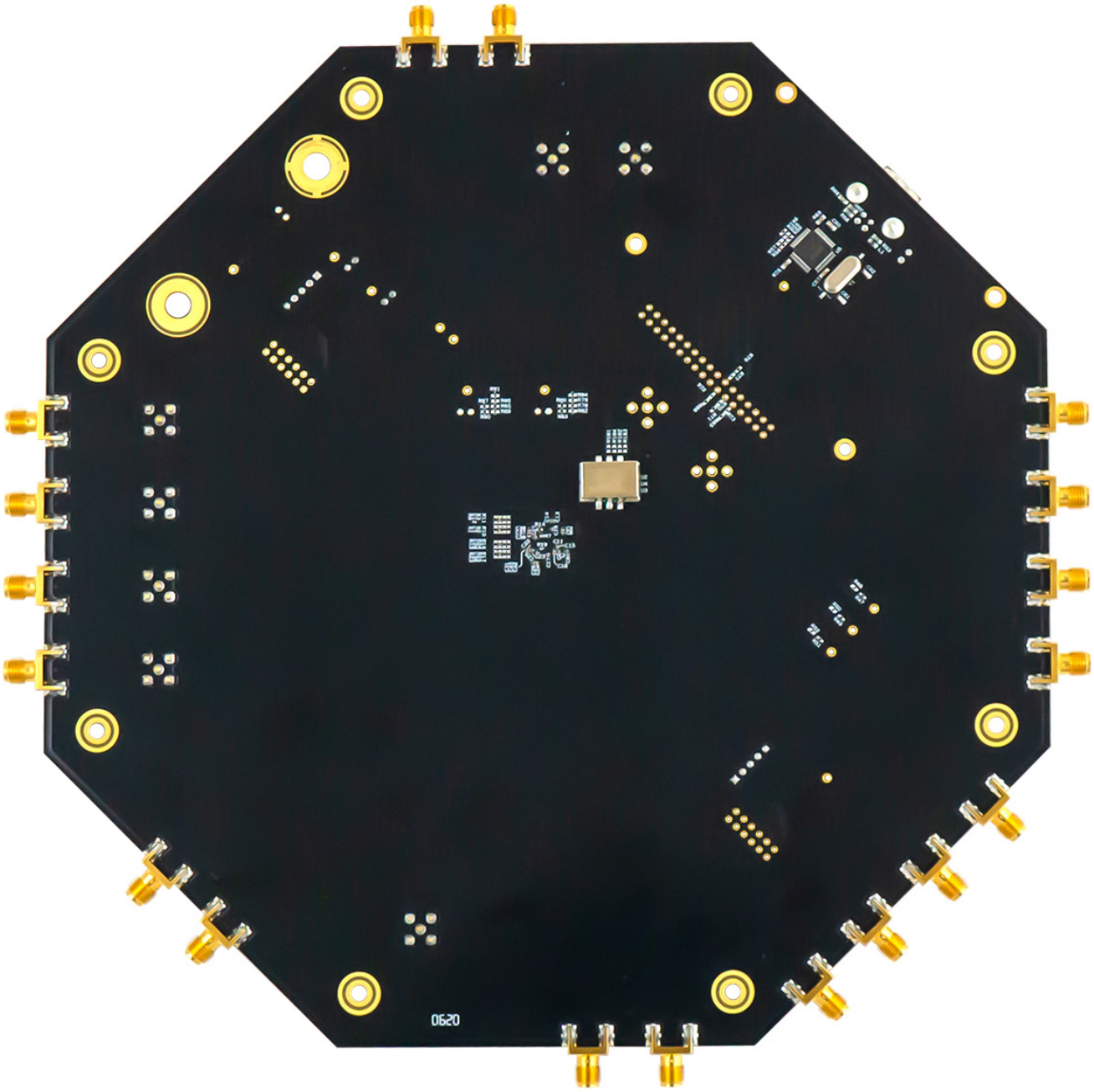


Figure 3. 8V19N49X-XX BGA-100 Evaluation Board (Bottom)

2.1 Schematic Diagrams

The EVB schematic diagrams can be downloaded from the 8V19N490 product page.

2.2 Bill of Materials

Item	Value	Qty	Reference	Manufacture Part Number
1	0.1u	19	C2;C3;C7;C8;C11;C13;C15;C16;C17;C23;C24;C25;C27;C31;C32;C33;C37;C39;C40	GRM033R60J104KE19D
2	100p	5	C6;C14;C18;C26;C38	GRM0335C1E101JA01D
3	0.1u	28	C1;C4;C5;C9;C10;C12;C19;C20;C21;C22;C28;C29;C30;C34;C35;C36;C41;C45;C64;C70;C73;C75;C78;C81;C83;C98;C102;C141	C1005X7R1C104K
4	0 Ohm	2	C47;C48	RC0402JR-070RL
5	0.1u	1	C49	C1005X7R1C104K
6	0.1uF	2	C53;C66	C1005X7R1C104K
7	10pF	1	C54	GRM1555C1H100JA01D
8	10u	9	C63;C69;C71;C74;C77;C80;C95;C101;C140	CL05A106MQ5NUNC
9	10uF	10	C67;C105;C107;C112;C115;C122;C123;C128;C130;C133	CL05A106MQ5NUNC
10	0.01u	3	C84;C99;C103	EMK105B7103KV-F
11	0	20	R1;R9;R15;R23;R37;R41;R59;R62;R65;R68;R71;R76;R154;R157;R158;R162;R172;R175;R176;R179	RC0402JR-070RL
12	5.1k	12	R2;R3;R10;R11;R16;R17;R24;R25;R45;R61;R78;R85	ERJ-2GEJ512X
13	13.3k	1	R35	ERJ-2RKF1332X
14	49.9	3	R42;R43;R46	ERJ-2RKF49R9X
15	100	5	R47;R49;R51;R83;R90	ERJ-2RKF1000X
16	10K	4	R56;R146;R160;R177	ERJ-2RKF1002X
17	1k	4	R63;R80;R87;R92	ERJ-2RKF1001X
18	33	3	R64;R81;R88	ERJ-2RKF33R0X
19	27n	1	C50	GRM155R71H273KE14J
20	4.7n	1	C51	GRM155R71H472KA01D
21	1u	1	C52	C1005X5R1C105K
22	51k	1	R36	MCR01MRTF5102
23	33k	1	R38	ERJ-2RKF3302X
24	0.1u	2	C42;C46	C1005X7R1C104K
25	33p	1	C43	GRM1555C1H330JA01D
26	0.1u	5	C44;C134;C136;C142;C144	C1005X7R1C104K
27	10u	8	C135;C137;C138;C139;C143;C145;C146;C147	CL05A106MQ5NUNC
28	2.8K, 1%	1	R14	ERJ-2RKF2801X
29	100	1	R27	ERJ-2RKF1000X
30	49.9	1	R44	ERJ-2RKF49R9X
31	0.1 uF	3	C55;C57;C59	GRM188R71H104KA93D
32	10000PF	1	C58	GRM188R71H103KA01D
33	0.047 uF	1	C60	C1005X7R1C473K050BC

Item	Value	Qty	Reference	Manufacture Part Number
34	33PF	2	C61;C62	GRM1885C2A330JA01D
35	10u	1	C82	C1608X5R1A106M
36	FERRITE_BEAD	13	FB1;FB2;FB3;FB4;FB5;FB6;FB7;FB8;FB9;FB10;FB11;FB12;FB13	BLM18BB221SN1D
37	600 ohm 500mA	1	L1	MMZ1608Y601B
38	680	1	R53	RC0603FR-07680RL
39	470	1	R54	RC0603FR-07470RL
40	27	2	R58;R60	RC0603FR-0727RL
41	1.5K	1	R66	RC0603FR-071K5L
42	10K	3	R69;R74;R75	RC0603FR-0710KL
43	0	2	R164;R180	RC0402JR-070RL
44	2	9	R149;R150;R152;R159;R163;R165;R166;R167;R168	MCR18ERTFL2R00
45	10 uF	1	C56	EMK212BJ106KG-T
46	VCXO, 122.88MHz	1	U2	[1] VG3225EFN 122.88M-CJHHBA or CVPD922 122.88MHz
47	+4V	1	J27	108-0740-001
48	GND	1	J28	108-0740-001
49	8V19N490B	1	U1	8V19N49x-xx
50	CGRA4004-G	1	D1	CGRA4004-G
51	Header_2Pin	2	JP4;JP5	TSW-102-07-F-S
52	Header_5Pin	2	JP2;JP6	TSW-105-07-F-S
53	Green	1	LD1	CMD15-21VGC/TR8
54	LED_0603_1206_H	3	LD2;LD3;LD4	LG L29K-G2J1-24-Z
55	ft2232_chip	1	U5	FT2232D
56	TPS7A8300	2	U6;U7	TPS7A8300
57	SMA_END_LAUNCH	18	J2;J3;J4;J5;J6;J7;J9;J10;J11;J12;J14;J15;J16;J17;J18;J19;J22;J24	LTI-SASF975ZGT
58	SMA_STRAIGHT	7	J1;J8;J13;J20;J21;J23;J25	LTI-SASF54GT-
59	6MHz	1	Y1	ECS60325PTR
60	USB PORT	1	J26	897-43-004-90-000000

1. VCXO can be vary. Examples:
   * Epson VG4315CA 122.88M
   * Epson VG3225EFN 122.88M CJHHBA
   * Crystek CVPD922 122.88MHz

3. Typical Performance Graph

The following figure shows example phase noise performance from the loaded example configuration.

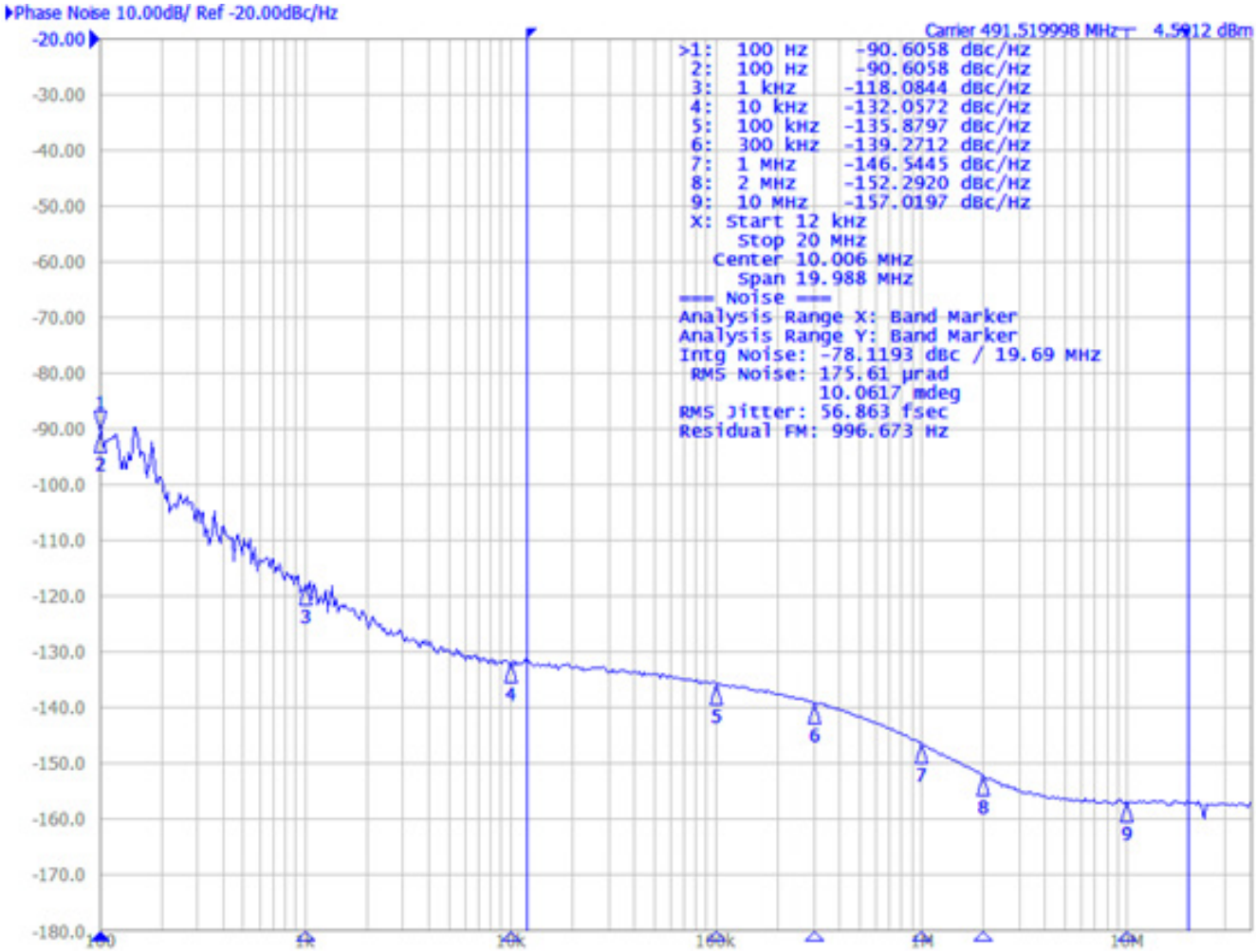


Figure 4. Example Configuration Phase Noise

4. Ordering Information

Part Number	Description
8V19N490B-EVK	8V19N490B Evaluation Board
8V19N490-24-EVK	8V19N490-24 Evaluation Board
8V19N490-19-EVK	8V19N490-19 Evaluation Board
8V19N491-36-EVK	8V19N491-36 Evaluation Board

5. Revision History

Revision	Date	Description
1.0	May 25, 2021	Initial release.

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