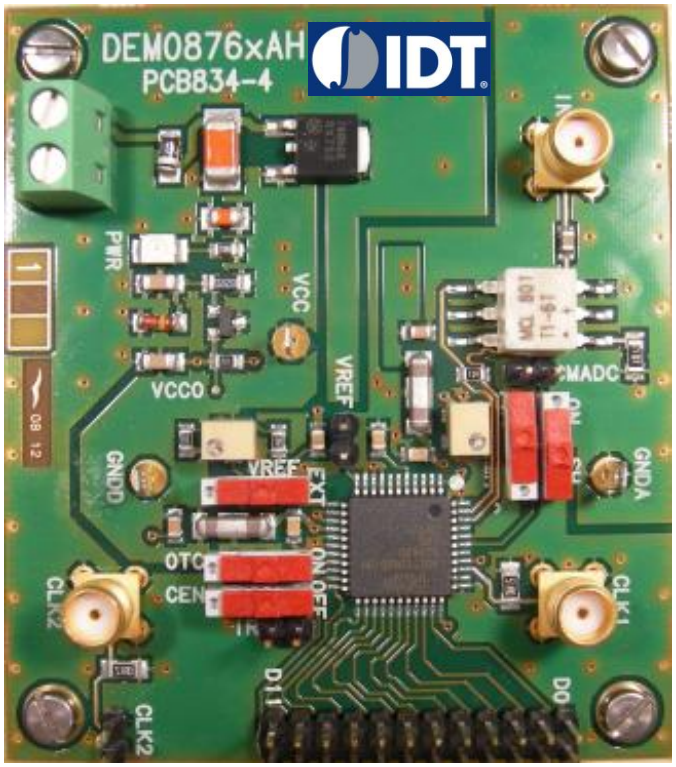
Quick Start

DEMO876xAH Demonstration Board for ADC1206S040/055/070 family

Rev. 2.0 — 2 July 2012 **Quick Start**

Document information

Info	Content
Keywords	DEMO876xAH, PCB834-4, Demonstration board, ADC, Converter, ADC1206S040/055/070
Abstract	This document describes how to use the demonstration board DEMO876xAH for the analog-to-digital converter ADC1206S040/055/070 family.
Overview	

Revision history

Rev	Date	Description
2.0	20120702	Rebranded.
0.5	20080610	Example added.

1. Quick start

1.1 Setup overview

Figure Fig 1 presents the connections to measure DEMO876xAH.

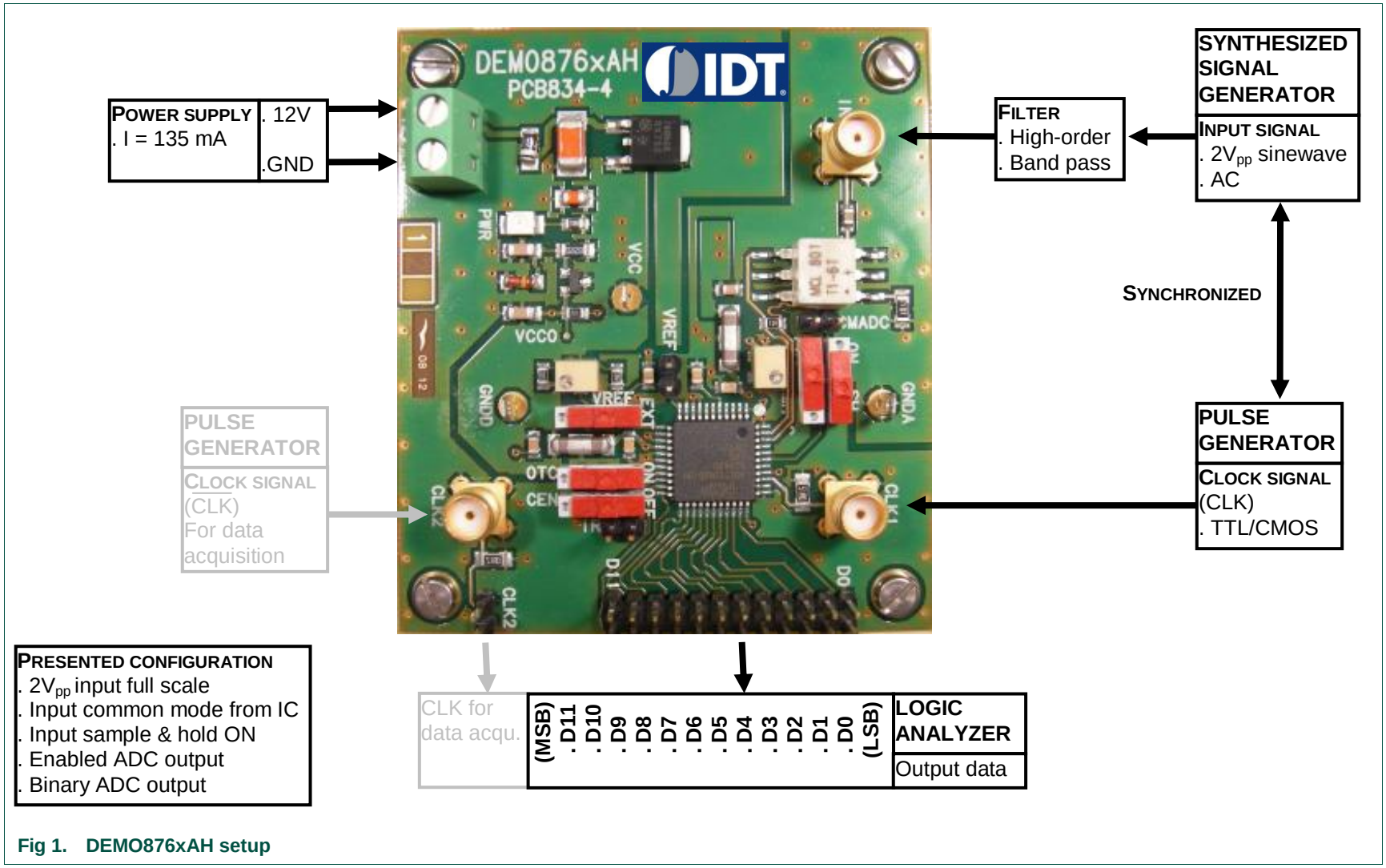
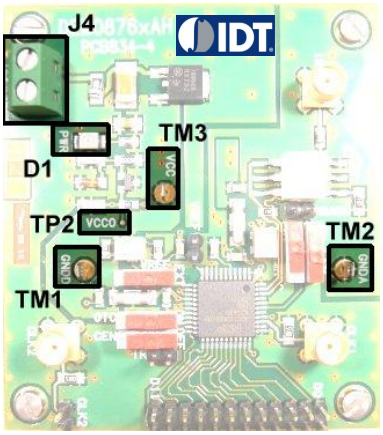


Fig 1. DEMO876xAH setup

1.2 Power supply

The board is powered with a single 12 V_{DC} power supply. A power supply regulator is used to supply all the circuitry on the board.

Table 1. General power supply

Name	Function	View
J4	Green connector – Power supply 12 V_{DC} / 135 mA.	
D8	PWR green light – It indicates the good supply plugging	
TM1	DGND test point – Digital ground	
TM2	AGND test point – Analog ground	
TM3	VCC test point – ADC core power supply	
TP2	VCCO test point – Output stage power supply	

1.3 Input signals (IN, CLK1)

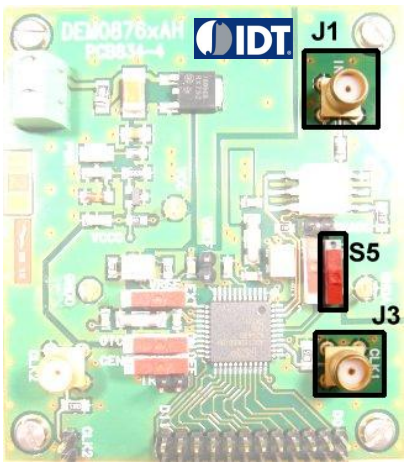
To ensure a good evaluation of the device, the input signal and the input clock must be synchronized together.

Moreover, the input frequency (Fi, MHz) and the clock frequency (Fclk, Msps) should follow the formula:

$$\frac{Fi}{Fclk} = \frac{M}{N}$$

,where M is an odd number of period and N is the number of samples.

Table 2. Input signals

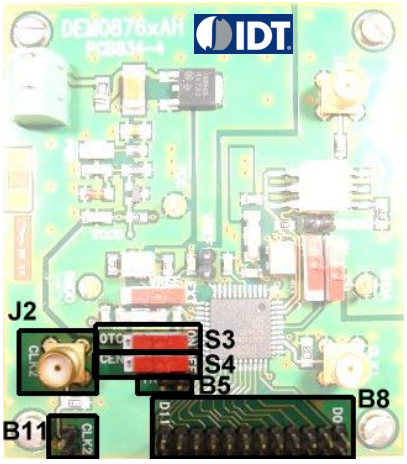
Name	Function	View
J1	IN connector – Analog input signal (50Ω matching)	
J3	CLK1 connector – Clock input signal (50Ω matching)	
S5	SH switch – Activation of the input sample-and-hold Active 7MHz < Fclk < 70MHz  Tracking mode Fi < 1 MHz 	

1.4 Output signals (D0 to D11, IR)

The digital output signal is available in binary or 2's complement format.

An optional clock connector is available to simplify the acquisition clock generation.

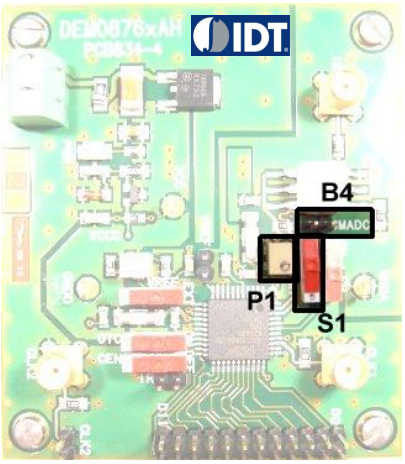
Table 3. Output signals

Name	Function	View
B8	Array connector – ADC digital output (D0 to D11)	
B5	IR test point – It indicates the out of range state of the analog input signal	
J2-B11	CLK2 connector – Optional clock for the data acquisition	
S3	OTC switch – Output format selection  Binary  2's complement	
S4	CEN switch – Output enable selection  Active output  High impedance output	

1.5 Input common mode (CMADC)

The input common mode can be set by the internal reference of the ADC or can be adjusted manually with a potentiometer.

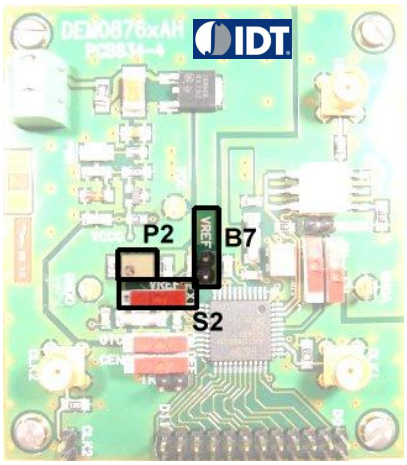
Table 4. Input common mode voltage adjustment

Name	Function	View
S1	Switch – Selection between internal and external common mode Internal common mode  External common mode 	
P1	Potentiometer – External common mode adjustment	
B4	CMADC test point – input common mode	

1.6 Input full scale (VREF)

The input full scale mode can be set by the internal reference of the ADC or can be adjusted manually with a potentiometer.

Table 5. Input full scale adjustment

Name	Function	View
S2	Ext switch – Selection between internal and external reference voltage  Internal reference  External reference	
P2	VREF potentiometer – External reference voltage adjustment	
B7	VREF test point – VREF reference voltage	

2. Example

2.1 Setup example

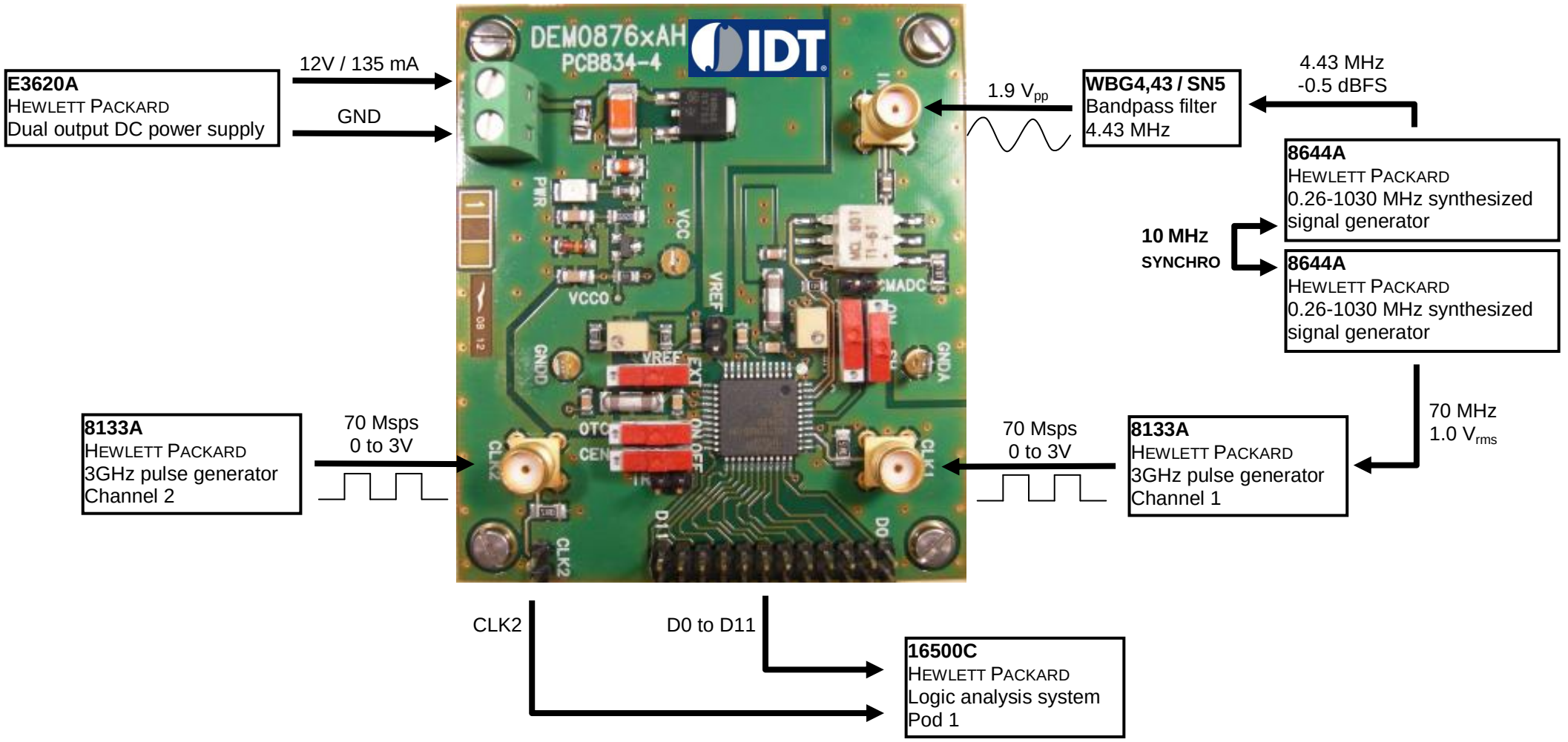


Fig 2. ADC1206S070 hardware setup