# Quick start ADC1443D/53D DB

Evaluation board for ADC1443D/53D series

Rev 03.1 — 2 June 2014

**Quick start** 

#### **Document information**

Info	Content
Keywords	ADC1443D DB,ADC1453D DB, ADC1159D DB, Evaluation board, JESD204B ADC, Kintex-7, BSX0254.
Abstract	This document describes how to setup the demonstration board ADC1443D/53D DB with the Xilinx Kintex-7 KC705 development board.
Overview	

The ADC1443D/53DWO Evaluation board is available in 4 versions: ADC1443D125WO-DB; ADC1443D160WO-DB; ADC1453D250WO-DB, ADC1159D250WO-DB. HMSC-FMC adaptor board is required to easily interoperate with Kintex-7 FMC connector.

#### **Revision history**

Rev	Date	Description
0.1	18 April 2012	Initial version
3.0	14 Feb 2013	Rebranding IDT
3.1	2 June 2014	Update to support ADC1453D250 and ADC1159D250



# Quick start ADC1443D/53D DB

# Quick start

#### 1. Overview of the evaluation board ADC1443D/53DWO-DB



#### 2. Switch and Jumpers default state



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#### 3. Board goal and general description

The ADC1443D/53DxxxWO/DB board along with Xilinx KC705 development board are aimed to provide a full and complete set to evaluate and demonstrate the ADC1x43D/53D series, analog to digital converters, compliant with JESD204B JEDEC serialization standard.

#### The ADCs

The board embeds 2 dual ADC devices with option for each ADC to receive a separate external clock input.



Each ADC is dual channel and needs to be fed with single-ended input (from SMA connector).

#### Power supplies

The board embeds a 5V power supply connector.



#### Downloading the FPGA bit file

The FPGA code, in the form of a bit file, requires to be downloaded via the KC705 external JTAG connector.



To download the Kintex-7 bit file, ISE Design Suite 13.3 or later is required from Xilinx, or at a minimum the Xilinx ChipeScope Pro 64-bit version tool.

The FPGA is responsible for de-serializing the serial stream coming From the ADC, according to the JESD204B standard.

Since we have 2 dual ADC on the board, each with 2 lanes, the HSDC\_SW\_ADC\_4.exe application allows to configure the FPGA and to choose which channel, ADC, lanes we want to acquire.

The FPGA is accessible via the same USB-to-SPI interface on the ADC board.



LED Information from the FPGA are available on the KC705 board



LED 7, when lighted, signals that the JESD204B link is operational.

LED5 and LED6 are toggling when FPGA receiver is getting a clock from ADC board.

Once the FPGA has decoded the Serial stream, It is stocked into a size variable internal memory (from 4K to 64k) and could be uploaded via SPI-to-USB to the HSDC\_SW\_ADC\_4.exe application and displayed as an FFT with all relevant information extracted.

An HSMC-to-FMC connector adapter makes it possible to connect the ADC1443D/53DWO demo board to the Xilinx KC705 board. A FMC High Pin Count (HPC) connector is required.



#### USB interface

The USB interface acts like a programming interface.

The main chip is an FTDI FT2232D that interface the USB Physical layer to the SPI interface for the Two ADCs and the clock generator.

The Board comes with the HSDC\_SW\_ADC\_4.exe application that controls all these components via USB.



Further instructions on how to install and operate the software are detailed in next section.

#### 4. Software and drivers install

#### 4.1 Labview Runtime 2010 install



#### Integrated Device Technology

6	Unzip	WinZip Self-Extractor - LVRTE2010std.exe       Image: Comparison of the specified folder press the Unzip button.         Unzip to folder:       Run WinZip         Image: Comparison of the specified folder press the Unzip button.       Run WinZip         Image: Comparison of the specified folder press the Unzip button.       Run WinZip         Image: Comparison of the specified folder press the Unzip button.       Run WinZip         Image: Comparison of the specified folder press the Unzip button.       Run WinZip         Image: Comparison of the specified folder press the Unzip button.       Glose         Image: Operative folder:       Glose         Image: Operative folder:       About         When gone unzipping open:       Help         .VSetup.exe       Help
7	ОК	WinZip Self-Extractor       240 file(s) unzipped successfully       OK
8	Next	Int.com/labview  Int.c
9	Next	NI LabVIEW Run-Time Engine 2010   Destination Directory   Select the primary installation directory.   Destination Directory   C:\Program Files\National Instruments\   Browse   << Back

10	Next	🐺 NI LabVIEW Run-Time Engine 2010	
		Features Select the features to install.	
		NI LabVIEW Run-Time Engine 2010     NI Variable Engine     DataSocket     NI LabVIEW 2010 Deployable License     USI	Libraries and other files necessary to execute LabVIEW 2010-built applications and shared libraries. Includes NI Reports, 3D graph support, and a browser plug-in that allows clients to view and control front panels remotely using a browser.
			This feature will be installed on the local hard drive.
			i nis readule will be installed on the local hard drive.
			This feature and its selected subcomponents may require up to 95 MB of disk space.
		Directory for NI LabVIEW Run-Time Engine 2010	Browse
		Restore Feature Defaults Disk Cost	<< Back Next >> Cancel
11	Select 'I accept the License	- 嗯 NI LabVIEW Run-Time Engine 2010	
	Agreement'	License Agreement You must accept the license(s) displayed below t	to proceed.
	Next	NATIONAL INSTRUMENTS SOF	TWARE LICENSE AGREEMENT
		INSTALLATION NOTICE: THIS IS A CONTRACT, BEF AND/OR COMPLETE THE INSTALLATION PROCESS DOWNLOADING THE SOFTWARE AND/OR CLICKIN COMPLETE THE INSTALLATION PROCESS, YOU C A GREEMENT AND YOU AGREE TO BE BOUND BY T BECOME A PARTY TO THIS AGREEMENT AND BE B CONDITIONS, CLICK THE APPROPRIATE BUTTON' DO NOT INSTALL OR USE THE SOFTWARE, AND R (30) DAYS OF RECEIPT OF THE SOFTWARE, AND R (30) DAYS OF RECEIPT OF THE SOFTWARE (WITH, ALONG WITH THEIR CONTAINERS) TO THE PLACE SHALL BE SUBJECT TO NI'S THEN CURRENT RET	S, CAREFULLY READ THIS AGREEMENT. BY IG THE APPLICABLE BUTTON TO ONSENT TO THE TERMS OF THIS 'HIS AGREEMENT. IF YOU DO NOT WISH TO OUND BY ALL OF ITS TERMS AND TO CANCEL THE INSTALLATION PROCESS, ETURN THE SOFTWARE WITHIN THIRTY ALL ACCOMPANYING WRITTEN MATERIALS, YOU OBTAINED THEM. ALL RETURNS URN POLICY.
			<< <u>Back Next &gt;&gt; Cancel</u>
12	Next	現 NI LabVIEW Run-Time Engine 2010	
		Adding or Changing         •NI Lab/IEW Run-Time Engine 2010         •NI Variable Engine         •DataSot/tet         •NI Variable Engine         •USI	INSTRUMENTS
		garo I lib	

13	Finish	RI LabVIEW Run-Time Engine 2010	
		The NI LabVIEW Run-Time Engine 2010 installation is complete.	
		<< Back	Next >> Einish
14	Restart	NI LabVIEW Run-Time Engine 2010         You must restart your computer to complete this operation.         If you need to install hardware now, shut down the computer. If you choose to restart later, restart your computer before running any of this software.         Bestart       Shut Down         Restart Later	

#### 4.2 Demoboard - USB-SPI driver install

1	Plug the USB cable in the demoboard USB connector				
2	The wizard will help to install the USB Serial Converter A				
3	Select 'Install from a list or specific location' Next	Found New Hardware Wizard  Welcome to the Found New Hardware Wizard  This wizard helps you install software for: USB Serial Converter A  USB Serial Converter A  If your hardware came with an installation CD ofloppy disk, insert it now.  What do you want the wizard to do?  Install from a list or specific location (Advanced) Click Next to continue.   < Back Next > Cancel			

#### Integrated Device Technology

4	Select 'Search for the best	Browse For Folder
4	driver in these locations'	Select the folder that contains drivers for your hardware.
	Select 'Include this location in the search'	Found New Hardware Wizard
	Browse	Search for the best driver in these locations Use the check boxes below to limit or expand the default search, which paths and reworkels media. The best driver found will be installed. To view any subfolders, click a plus sign above.
	Select the folder 'CDM2.08.12'	Search removable media (floppy, CD-ROM)     OK     Cancel       ✓ Include this Igcation in the search:     F:\offlines_files\NXP\2011\11-TUCANA\S8A_Softw.     Bgowse
	Next	<u>D</u> on't search. I will choose the driver to install. Choose this option to select the device driver from a list. Windows does not guarantee that the driver you choose will be the best match for your hardware.
		< Back Next > Cancel
5	Continue Anyway (Windows XP only)	Hardware Installation         Image: Converter A         has not passed Windows Logo testing to verfy its compatibility with Windows XP. (Tell me why this testing is important.)         Continuing your installation of this software may impair or destabilize the correct operation of your system either immediately or in the future. Microsoft strongly recommends that you stop this installation now and contact the hardware vendor for software that has passed Windows Logo testing.         Quantum Anyway       STOP Installation
6	Browse Select the file ' <b>ftdibus.sys</b> ' in the folder ' <b>CDM2.08.12\i386</b> '	Files Needed     Image: Cancel       The file ftdibus.sys' on FTDI USB Drivers Disk is needed.     OK       Type the path where the file is located, and then click     Cancel
	OK	Copy files from:          [1]\114ucana\s&a_tools\ftdi driver\windows 7\1388

7	Finish	Found New Hardware Wizard         Completing the Found New Hardware Wizard         The wizard has finished installing the software for:         USB Serial Converter A         Click Finish to close the wizard.         Click Finish to close the wizard.
8	The wizard will help to install th	e USB Serial Converter B (same as USB Serial Converter A)
9	The wizard will help to install th	e USB serial port
	The file 'ftser2k.sys' is in the fo	older 'CDM2.08.12\i386'

#### 5. ADC1443D/53DWO + Xilinx KC705 demo setup

## 5.1 Connecting ADC1443D/53DxxxWO and KC705 boards

To attach the ADC1443D/53DxxxWO board to the Xilinx KC705 board. Refer to Fig 10:

- 1. attach the HSMC-to-FMC adapter to the ADC1443DxxxWO demo board;
- 2. then attach the combined ADC1443 board and adapter to the FMC HPC (High Pin Count) connector of the KC705 board;
- 3. it is recommended to prop-up the feet of the ADC board to make it stable and level;
- connect an external clock signal to CLKP1 SMA connector (for example 153.6 MHz at +15 dBm level);
- connect the external input signal to INA1 and/or INB1 SMA connector (for example 170 MHz at +10 dBm level);
- 6. it is recommended for best dynamic performance to use an in-line external bandpass filter for the external input signal;
- 7. it is recommended, in order to support "coherent sampling", that the external clock and input signal generators be frequency locked (i.e. the "external ref out" of one is connected to the "external ref in" of the other).



#### 5.2 KC705 board start-up

It is highly recommended that the KC705 board be started <u>**before**</u> the ADC1443D/53DWO board. This is to help ensure a consistent startup process:

- make sure that the ADC1443D/53DxxxWO board USB and DC power cables are disconnected;
- connect the USB-JTAG and DC power cables to the KC705 board.
- ensure that the KC705 power switch is in the "on" position;

#### 5.3 Launch ChipScope Pro

Launch Xilinx Design Suite 13.3 (or later) ChipScope Pro analyzer (64-bit version).



Click icon to start JTAG search	
GhipScope Professore Profess	_
New Project	
AT	
ChipScope Pro	
NFO: ChipScope Pro Analyzer Version: 13.3 Q.76xd (Build 13300 11 276.1137)	<u> </u>
	0% 201 PM
Fig 12. ChipScope Pro start-up screen	

Perform search of JTAG chain.

Click "OK" to close pop-up window.

Γ

*	hain Device Window Help	
New Project JTAG Chain	Click OK	
INFO: ChipScope Pro	p Analyzer Version: 13.3 O 76rd (Bulld 13300 11 276.1137)	
COMMAND: open_ca INFO: Started ChipSc INFO: Successfully op INFO: Successfully op		



The search JTAG chain results are finally displayed. Check to make sure no errors are reported.

#### 5.4 Download Kintex-7 FPGA bit file

Downloading the Kintex-7 bit file requires use of the ChipScope Pro tool.

Go to the "Device" tab to configure the path where the bit file is located on your hard drive.



Browse for the FPGA bit file in path "C:..\ADC1443D\KC705 bit stream for WO board" and select the "jesd204\_ml605\_adc\_top.bit" file. Then click "OK" to start the download process.

ChipScope Pro An Eile View JTAG C C Project JTAG Chain	alyzer (new project) haan Device Window Help		
P DEV:0 MyDevice0     XADC Conso		First, browse for FPGA bit file	
	Partial Reconfiguration Bitstream Clean previous project setting Select New File		-
	Import Design-level CDC File NOTE: This operation cannot be undone. Design-level CDC File Auto-create Buses File: File: Director: C:LLoiseNMP HSC Demo TrainingADC1443DWC765 bit stream for	pScope Pro	)
	Select New File OK Cancel		
INFO: Successfully o INFO: Successfully o INFO: Cable: Digilen	able cope host (localhost 50001) pened connection to server. localhost 50001 (localhost/127.0.0.1) pened Digilent USE JTAG Cable LITAG-SMITI, Port 0. Speed: 10000000 Hz Units Inthe JTAG device Chain.	Second, click OK	
INFO: If cores were e	ppected to be found, see Answer Record 19337.		EN 🔺 🔐 att 🗐 3:19 P 4/19/2



The FPGA bit file download progress is indicated.

#### 5.5 ADC1443D/53DxxxWO board start-up

It is highly recommended that the KC705 board be started <u>**before**</u> the ADC1443D/53DWO board. This is to help ensure a consistent startup process:

- make sure that the KC705 board is powered and the FPGA bit file is downloaded (sections 5.1 - 5.4);
- connect the USB cable (first) and DC power cable to the ADC1443D/53DWO board;
- check to make sure green LEDs are lighted on the ADC1443D/53DWO board;



Fig 18. Check that ADC1443D/53DWO green LEDs are lighted



• check to make sure green LEDs are toggling on the KC705 board;

#### 5.6 Launch ADC1443 GUI

Run the application "HSDC\_SW\_ADC\_4.exe".

Configure the settings as appropriate for application per Fig 20 below.



	NE HSDC_SW_ADC_4.vi	Aug.			
		NXP HSC ADC acquisition s	software		QUIT
	NXP device: Chip#:	SPI control - JESD204x Registers SPI control - Read / Write Registers	Clock control Tools	Acquisition GPIB & Test cor	fig Info
	ADC1443D V 1 V Resolution MRA # Acq. Board:	ADC1443D SPI Read / Write Registers		Value	
	14   3   Xilinx •     Fin and Fs are:   Fixed is:		Register name	Address A B	
	Coherent 💌 Fs 💌	READ ALL REGISTERS			^
	Sampling rate Fs Fs Fs Level	Save registers to text file (".txt"):			
	153.600000000 Msps 0.00 dBm Fs jitter	ADC to save:			
	0.00000E+0 s Input freq. Fin (max. 1000 MHz)	ADC 1			
	Fin #1         Fin #1 level           170.006250000         MHz         0.00         dBm	SAVE REGISTERS TO FILE			
Click 'INITIALIZATION'	Fin #2 Fin #2 level 170.006250000 MHz 0.00 dBm	Load registers from text file (".txt"):			
	Fin jitter SPI clk div. 0.00000E+0 s 4	LOAD REGISTERS FROM FILE			
	Number of samples	•			
	8192	Dump registers to text file (".txt")			
		Start Address End Address SPI Chip Select			
	Initialize board	x 0 > x 400 Chip #1 v			
	Initialize board Comments				
		SPI Chip Select Address Value			
	Save & Restore settings 🕞	Chip #1 × 0 × 0 READ WRITE			-
	SAVE RESTORE				
	Fig 21. Click 'Initial	ization'			
	•				

After settings are selected, then click 'INITIALIZATION'.





#### 5.7 Download ADC1443 configuration file

Download the ADC1443 configuration file. This file configures the JESD204B internal registers.

In the field 'Load registers from text file (".txt")', browse and select the appropriate file Example: "ADC1453D\_ 250Msps\_SPI\_C.txt".

Then click 'LOAD REGISTERS FROM FILE' button.

	NXP HSC ADC acquisition software	QUIT
Copyright NXP	semiconductors 2012	
NXP device: Chip#:	SPI control - JESD204x Registers SPI control - Read / Write Registers Clock control	Tools Acquisition GPIB & Test config Info
ADC1443D • 1 •	ADC1443D SPI Read / Write Registers	
Resolution MRA # Acq. Board: 14 3 Xilinx -	ADCI445D SPI Read / Write Registers	Value
Fin and Fs are: Fixed is:	Regist	ter name Address A B
Coherent 💌 Fs 💌	READ ALL REGISTERS	
Sampling rate Fs	READ ALL REGISTERS	
Fs Fs Level	Save registers to text file (".txt"):	First browse for the
153.600000000 Msps 0.00 dBm		First, browse for the
0.00000E+0 s	ADC to save:	ADC1443 configuratior
Input freq. Fin (max. 1000 MHz)		file
Fin #1 Fin #1 level 170.006250000 MHz 0.00 dBm	SAVE REGISTERS TO FILE	
Fin #2 Fin #2 level	Load registers from text file (".txt"):	×0 ×0 ×0
170.006250000 MHz 0.00 dBm Fin jitter SPI clk div.		
0.00000E+0 s 4	LOAD REGISTERS FROM FILE	
Number of samples		
8192	Dump registers to text file (".txt")	*0 *0
RESET	Second	I, click 'LOAD REGISTERS
	Start Address End Address SPICH	
Acquisition board ready	×0 > ×400 Chip FROM	
NXP board ready	DUMP REGISTERS	
Comments		×0 ×0 ×0
	SPI Chip Select Address Value	
Save & Restore settings 🛛 🚘	Chip #1 💌 x0 x0 READ WRITE	×0 ×0 ×0
		· · · · · ·
SAVE RESTORE		

The Polarity for SYNC signal should be changed to fit with this FPGA bit file. To change the SYNC polarity for the ADC go to the following menu:

SPI control - Functional Registers - ADC1443D	SPI control - JESD204x Registers	SPI control - Read / Write Registers	Clock control Tools Acquis
JESD204x SPI Registers			
IP Main Control Registers	1		while Barel Char, Burnard Alignment
PLL Unlocked     ADCs / Lanes Conf     2 ADCs / 2 Lanes	igaración	E Polarity Sync Single Ended	sable Repl. Char Bypass Alignment
JESD204A Control & Lane Control Registers			
Scrambling Lane 1 Mode ADC Mode		ane 2 Mode Lane 2 Polarity	Pattern Out 2AA
ADC Control Registers			
ADC 1 Mode		ADC 2 Mode ADC Mode	Pattern In AA02
J			

Main Control Registe	rs							
PLL Unlocked	ADCs / Lanes Configu 2 ADCs / 2 Lanes : F=		Sync Polarity	Sync Sing		sable Repl. Char	Bypass Ali	gnment
SD204A Control & Lar	ie Control Redisters							
SD204A Control & Lar Scrambling	Lane 1 Mode	Lane 1 Polarity	Lane 2 Mo ADC Mod		ane 2 Polarity	Patt 2A	tern Out A	

#### 5.8 Load ChipScope Pro project

Using the ChipScope Pro tool, load the FPGA project file. This will enable debugging capabilities.

Go to the "File" tab to open the project:



Select 'No', to not save any changes.

ChipScope Pro Analyzer	
Do you want to save	the changes you made to project 'new project' ?
Yes	No Cancel
Fig 25. Select 'No'	Click 'No'

Browse for the FPGA project file and select the "chipscope3.cpj" file. The FPGA project is loaded with the following screen in Fig 26.



#### 5.9 Force a FPGA JESD204B link reset

A forced FPGA JESD204B link reset is required in order to enable initial data acquisition.

First, click on the "VIO Console" so that its corresponding window appears in the foreground.

Second, click on the 'reset' field value '0', so that it momentarily toggles to a '1'. This performs a reset for the FPGA JESD204B.



Writing 22 to address 0 , launch the sysref and allow the system to have a deterministic latency.

After the reset is performed, check that the LED on the KC705 board is lighted

Now you could use the Labview interface to capture using the external signal as a tigger.



### 5.10 View internal FPGA waveform result

After the forced FPGA JESD204B link reset has been issued, view the reconstructed waveform to make sure that a good JESD204B link is established.

First, click on the "Bus Plot" so that it's corresponding window appears in the foreground.

Second, select 'sine0' if viewing JESD204B lane corresponding to INB input of the ADC, and select 'sine1' if viewing JESD204B lane corresponding to INA input of the ADC.

Third, click on the 'T!' field to create a data trigger.





If waveform result looks bad, or is not as expected, then repeat FPGA JESD204B link reset explained in previous section 5.9. And then click "T!" afterwards to view new waveform result.

#### 5.1 Using ADC1443D/53D GUI to acquire data

After the forced FPGA JESD204B link reset has been issued, and the FPGA reconstructed waveform is confirmed to look as expected, then the ADC1443 GUI can be used henceforth to continuously acquire data and display and store results.

on the Acquisition tab, you could hit the save samples and specify a path to get the data

on a text file.

Choose Display# 1 on the scroll menu

And finally hit acquire to get the data



Under Reorganized Signal and Unreconstructed Signal Sub-Tab, you have the Sinwave temporal view



#### 6. Other notes on ADC1443D/53D GUI

#### 6.1 Software start-up

The ADC1443D/53D GUI applicaton will allow:

- the user to control features through the SPI;
- as well as performing any online data acquisition to evaluate the performances.

#### 6.2 Read / Write Registers





#### 6.3 Functional Registers





#### 6.1 Saving ADC samples



#### 7. ADC EVB HSMC connector pinout



#### 8. HSMC-FMC adaptor board pinout