EVB-RTP100E1P2G1FL-DSC

Low-Voltage GaN RTP100E1P2G1FL-DSC

Introduction

The EVB-RTP100E1P2G1FL-DSC evaluation board (EVB) provides an easy method to evaluate the electrical performance of the Renesas low voltage GaN, including how to optimize the circuit board to enable a high-efficiency and high-power density board capable of operating at high frequencies. This board also includes test points for measurement of the low voltage GaN switching waveforms and energy efficiency.

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1. Board Overview

This EVB-RTP100E1P2G1FL-DSC evaluation board is a synchronous buck converter containing two Renesas low-voltage GaN devices – RTP100E1P2G1FL-DSC in a half-bridge configuration driven by Renesas gate driver RRP68150. The low voltage GaNs are 1.2mΩ 100V enhancement-mode Gallium Nitride (GaN) FET in a 5 × 6 mm FCLGA package. Its footprint is compatible with standard silicon counterparts. The RRP68150 gate driver is a high frequency half-bridge driver designed specifically for enhancement mode GaN FETs.

The buck converter has a DC48V input, a DC12V output, a maximum output power of 360W, and operates between 250kHz and 500KHz switching frequencies. The dimension of the evaluation board is 53 × 53 mm.

The EVB-RTP100E1P2G1FL-DSC features:

- Highly flexible and user-friendly buck converter evaluation board
- Performance testing of Renesas Low voltage GaN over a wide range of Vin, Vout, Fsw, and Pout
- System performance experience using the Renesas RRP68150 gate driver

Figure 1. EVB-RTP100E1P2G1FL-DSC Board Image

2. Functional Description

2.1 Overview

The evaluation board's circuitry is divided into four parts (see Figure 2). Part 1 is a DC5V regulator that provides a stable and accurate DC5V voltage to the PWM and gate drive circuits. Part 2 is the PWM and dead-time control circuits. It converts the single square wave signal provided by the signal generator into two independent signals to drive the high-side and low-side GaNs, while adding an appropriate dead time to prevent shoot-through. Part 3 is the gate driver that provides 2A sourcing and 5.3A sinking peak current for the GaN devices switching. Part 4 is the power stage (two GaN devices RTP100E1P2G1FL-DSC, an inductor, and some input/output capacitors). This is the core part of the entire board and is responsible for converting DC48V to DC12V.

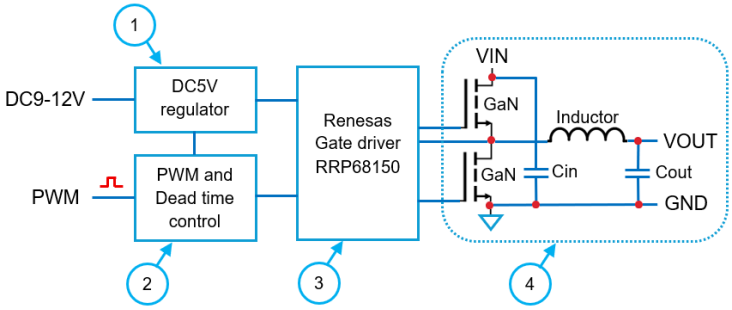


Figure 2. Block Diagram of the Buck Converter

Figure 3. EVB-RTP100E1P2G1FL-DSC Board

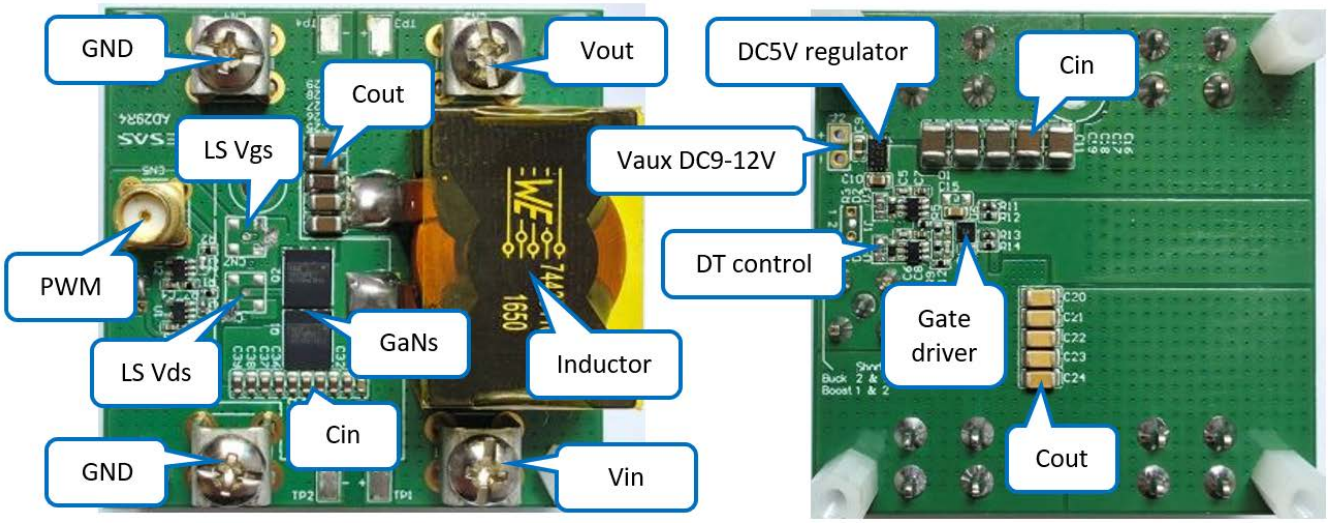


Figure 4. EVB Top (left) and Bottom (right) Views

Table 1. EVB Product Specifications

Input (V)	DC48V typical – DC80V (80% GaN-FET rated voltage)
Output (V)	DC12V typical – DC16V (Maximum output capacitor rated voltage)
Output (A)	30A maximum
Switching Frequency	250kHz–500kHz
Auxiliary Power Supply	DC9 – 2V
Renesas GaN FET	RTP100E1P2G1FL-DSC
Renesas Gate Driver	RRP68150-BH0

2.2 Renesas RTP100E1P2G1FL-DSC GaN FET

The RTP100E1P2G1FL-DSC 100V, 1.2mΩ is an enhancement mode Gallium Nitride (GaN) FET in a 5 × 6 mm FCLGA package using Renesas' Gen 1 REXGaN® platform. Utilizing advanced packaging technology, these devices deliver high-speed switching and enhanced thermal performance. Designed with footprint compatibility to standard silicon counterparts, these devices simplify the transition to GaN technology.

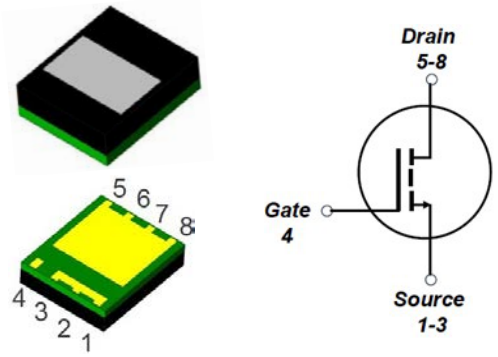


Figure 5. RTP100E1P2G1FL-DSC and Schematic Symbol

Features:

- Ultra-fast switching E-mode GaN HEMT
- JEDEC-qualified GaN technology
- Package footprint compatible to Si counterpart
- Low static losses
- Simplified thermal design
- Zero reverse recovery charge
- Low gate charge and output charge

V_{DS} (V)	100
$R_{DS(on)}$ (mΩ) Typical	1.2
Q_{OSS} (nC) typical	86
Q_G (nC) typical	28
Q_{rr} (nC) typical	0

2.3 Renesas RRP68150 Gate Driver

The RR68150 gate driver is a 5V-powered, high-frequency half-bridge driver for enhancement mode GaN FETs and low-threshold N-Channel MOSFETs. It features a 2A source and 5.3A sink current capability with its switching node supporting up to 100V DC. The driver's PWM inputs are 3.3/5V CMOS logic-compatible and can tolerate input voltages up to 14V, independent of the VDD supply voltage. The high-side bias voltage is generated using a bootstrap technique and is internally clamped at 5.4V. This clamping action prevents the gate voltage from exceeding the maximum gate-source voltage rating of the GaN FET. Its 5V operational supply enables convenient supply sharing with the controller.

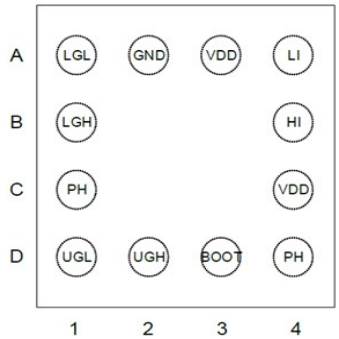


Figure 6. WLCSP12-2x2 Pin Assignments – Top View

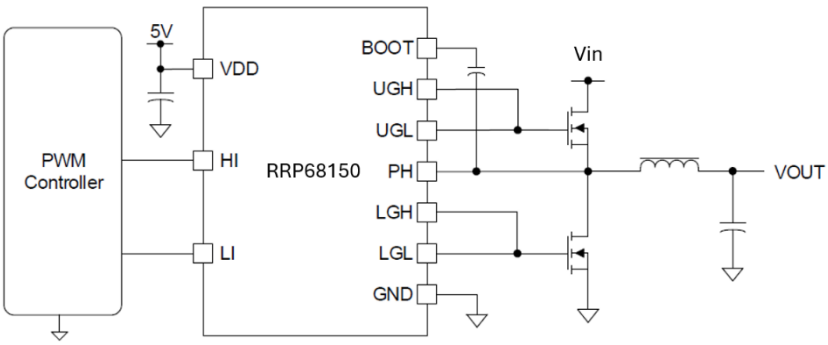


Figure 7. Typical Application Diagram

3. Board Features

3.1 Input PWM Signal

The evaluation board requires an input PWM signal to set the switching frequency and adjust the duty cycle to obtain the desired output voltage value. The PWM signal must be a square waveform, 0V for low-level signal and 5V (maximum 6.5V) for high-level signal. The input signal is connected to connector CN5. Figure 8 is the connector (Type SMA-KE) and Figure 9 is an example of the PWM signal

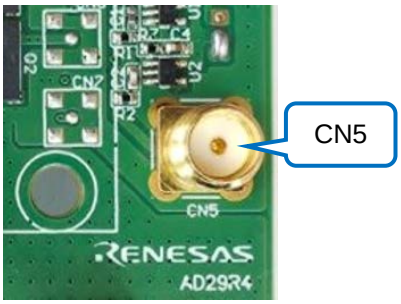


Figure 8. SMA-KE Connector

Vlow = 0V, Vhigh = 5V, Duty on 25%, 250kHz

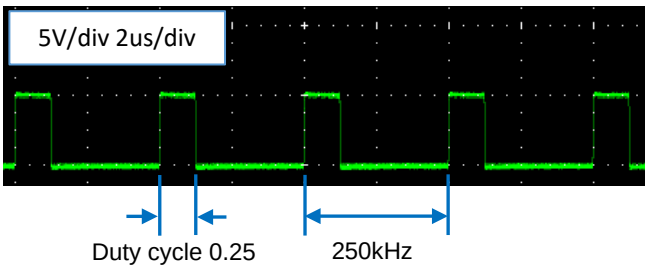


Figure 9. Input PWM Signal

3.2 Duty Cycle

The evaluation board is a buck converter, so the duty cycle can be calculated using the following formula. As the input voltage is DC48V, output voltage is DC12V. The calculated duty cycle is 0.25. In real application, the actual duty cycle is higher than the calculated value due to power loss. To adjust the duty cycle, set the other output voltages within 0 to 16V (16V is the maximum output capacitor rated voltage).

$$D = \frac{V_{out}}{V_{in}}$$

3.3 Dead Time

Synchronous buck converters consist of high-side and low-side GaNs. If the dead time is not set correctly, it may lead to a shoot-through. To prevent this, set a reasonable time according to GaN FET's switching behavior and PCB layout optimization. If the design is correct, it is recommended to set the dead time between 5ns and 15ns. It can effectively reduce the power loss without shoot-through.

Resistor R3 sets the dead time of the high-side GaN FET and resistor R4 sets the dead time of the low-side GaN FET (see Figure 10 and Figure 11). The required resistance value can be calculated using the formula below.

$$R_{DT}(\Omega) = 13.5 \times DT(ns) - 14$$

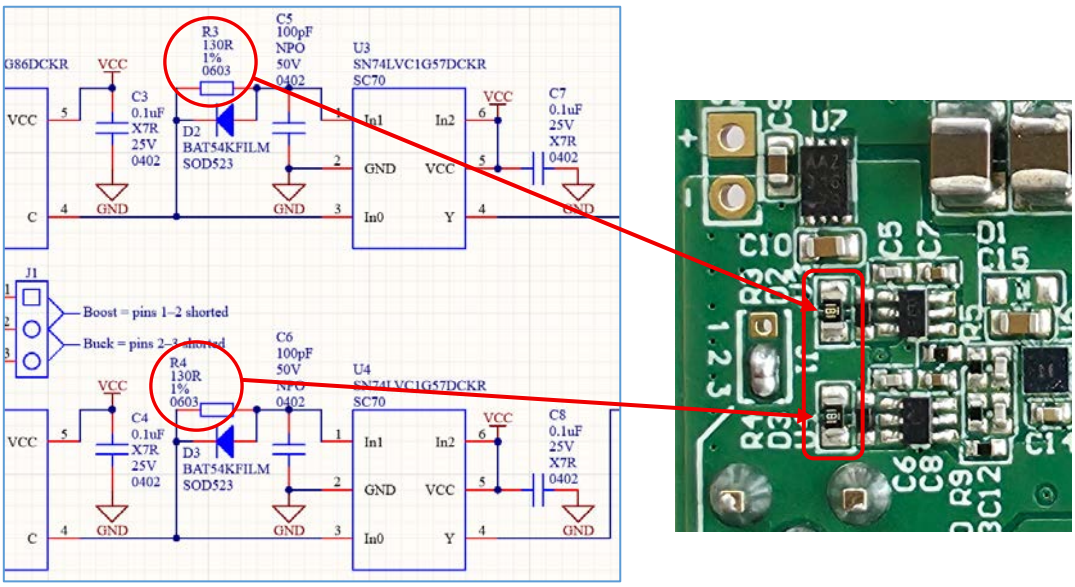


Figure 10. Resistors R3 and R4

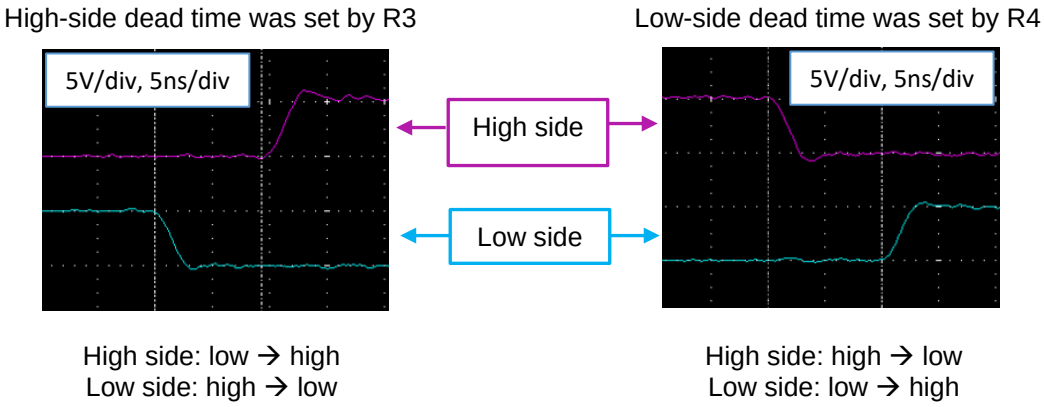


Figure 11. Resistor R3 and R4 Dead Time

3.4 Split-Gate Output

The gate driver RRP68150 on the evaluation board features split-gate outputs with strong sink capability, enabling independent control of turn-on and turn-off drive strength for optimized switching performance. In the schematic diagram shown in Figure 12, the resistors R11 and R12 control the on/off state of the high-side GaN Q1, while R13 and R14 control the on/off state of the low-side GaN Q2.

Users can adjust these four resistor values according to the buck converter's design parameters, such as switching frequency, input/output voltage values, and output power level, to control the drain-source voltage and gate-source voltage overshoot issues of the GaN FET.

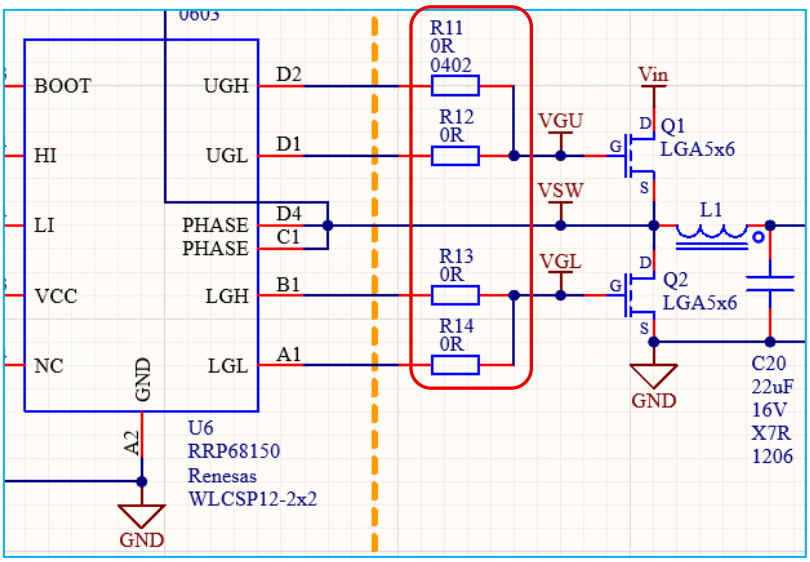


Figure 12. Gate Drive Resistors

4. Test Setup

4.1 Setup Procedure

1. Turn off the power before connecting any device and refer to Figure 13 and Figure 14 for the following steps.
2. Connect a signal generator to SMA-KE connector CN5 as shown in item 1.
3. Connect a DC9–12V power supply with a current limit of 0.5A to terminal J2 as shown in item 2.
4. Connect a DC48V power supply with a current limit of 9A to connectors CN1(+) and CN2(-) as shown in item 3.
5. Connect a DC voltage meter to TP1(+) and TP2(-) to measure input voltage as shown in item 4.
6. Connect an electronic load to connectors CN3(+) and CN4(-) for output load current measurement and TP3(+) and TP4(-) for output voltage measurement as shown in item 5 of Figure 13.
7. An axial fan (NMB: 4710PS-22T-B30) is put 13cm from the evaluation board and provides an air flow of 63.5 CFM as shown in Figure 14 item 6

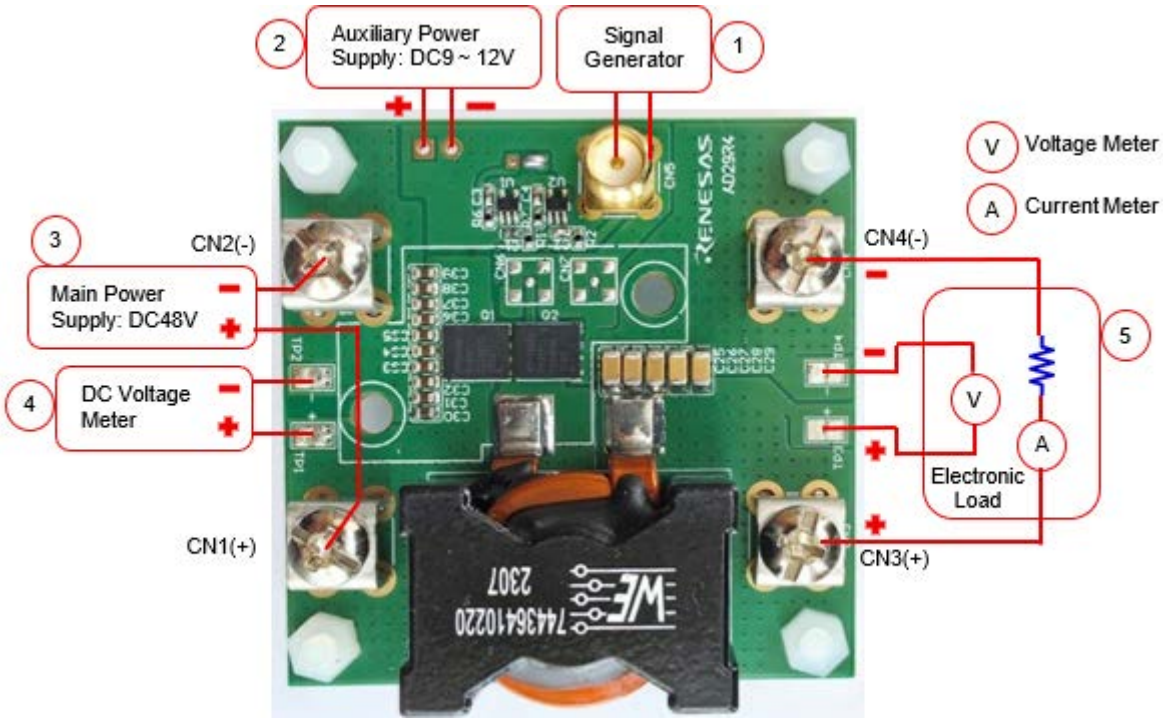


Figure 13. Setup Legend

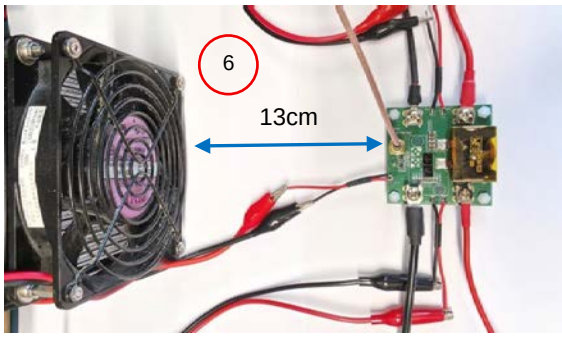


Figure 14. Axial Fan Airflow

4.2 Power-On Procedure

1. Complete the Setup Procedures.
2. Setup PWM signal on the signal generator as shown in Figure 15. Then, turn on the PWM signal to the board.
   a. Square wave
   b. Vlow: 0V
   c. Vhigh: 5V (typ), 6.5V (max)
   d. Duty cycle: 0.25
   e. Switching frequency: 250kHz

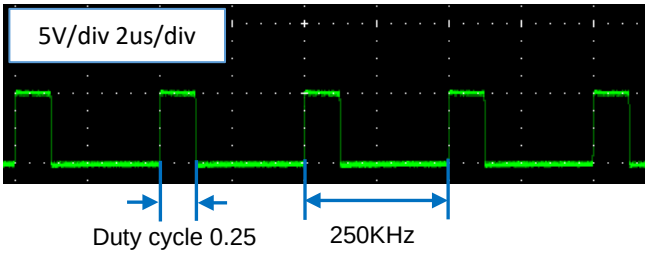


Figure 15. PWM Signal

3. Turn on auxiliary power supply and adjust the output voltage to DC9V or DC12V. The Vgs voltage waveform of the low-side GaN FET Q2 is shown in the Figure 16.

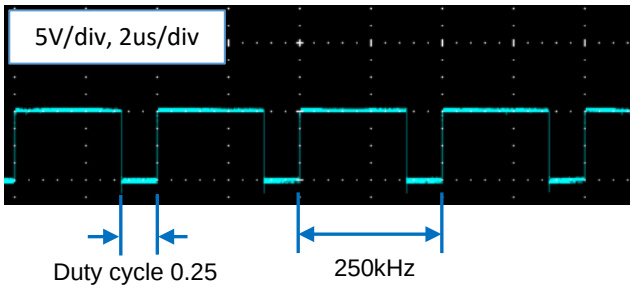


Figure 16. Vgs Voltage Waveform

There are two methods for measuring the Vgs switching waveform. The first method is to directly measure the component traces using a passive probe as shown in Figure 17. Use a spring clip to get a small ground loop. The second method is to measure the switching waveform using the MMCX jack at CN7 as shown in Figure 18 (the jack at CN7 is not provided).

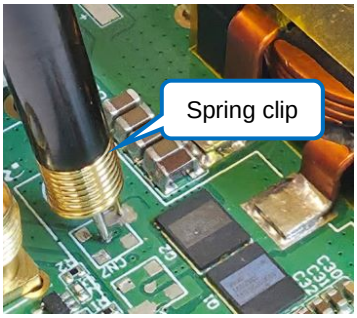


Figure 17. Passive Probe–Vgs

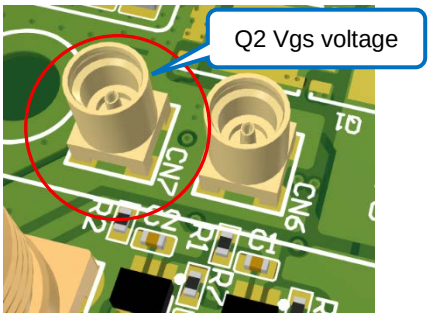


Figure 18. MMCX Jack–Vgs

4. Ensuring the initial main power supply voltage is 0V, turn on the power and slowly increase the voltage to DC48V. The Vds voltage waveform of the low-side GaN FET Q2 is shown in the Figure 19. The same methods can be used to measure the Vds voltage at Q2 as shown in Figure 20 and Figure 21 (the jack at CN6 is not provided).

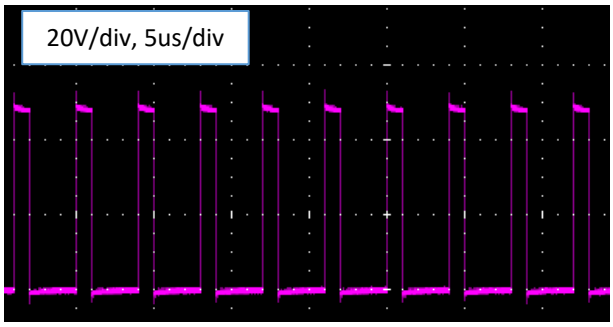


Figure 19. Vds Voltage Waveform

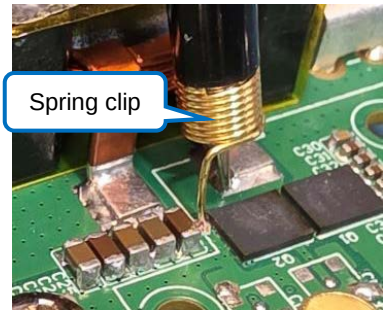


Figure 20. Passive Probe–Vds

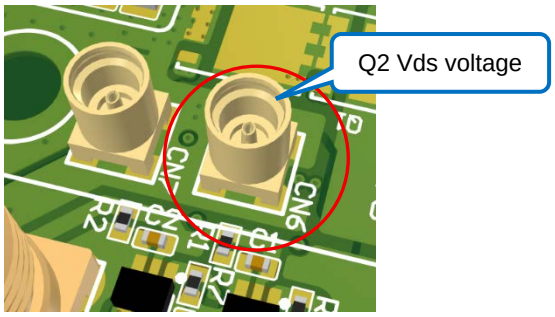


Figure 21. MMCX Jack–Vds

5. When the output voltage of the buck converter reaches DC12V, the output load current can be increased gradually to check the switching behavior, energy efficiency, and other parameters.
6. For shutdown, follow these steps in reverse.

5. Test Results

5.1 Energy Efficiency and Power Loss

Test conditions:

1. Input voltage was measured at TP1(+) and TP2(-).
2. Output voltage was measured at TP3(+) and TP4(-).
3. The energy efficiency was tested at an airflow of 63.5 CFM.
4. The distance between evaluation board and axial fan is 13cm.

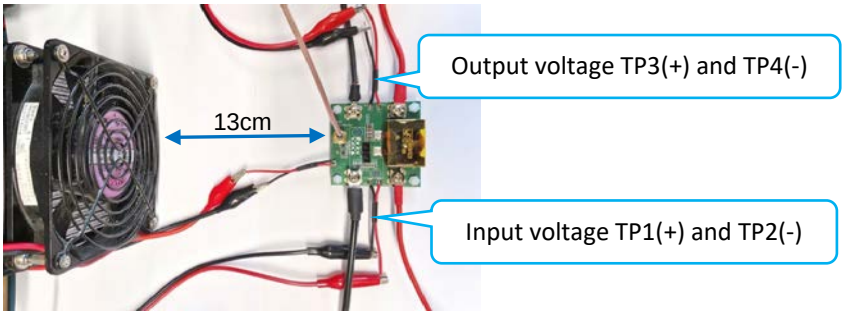


Figure 22. Axial Fan Layout

Figure 23 and Figure 24 show the energy efficiency and power loss results of the circuit board at three different switching frequencies (250kHz, 350kHz and 500kHz). Input voltage is DC48V. Output voltage is DC12V. Output current is 30A maximum. Inductor is 2.2µH Wurth 74436410220.

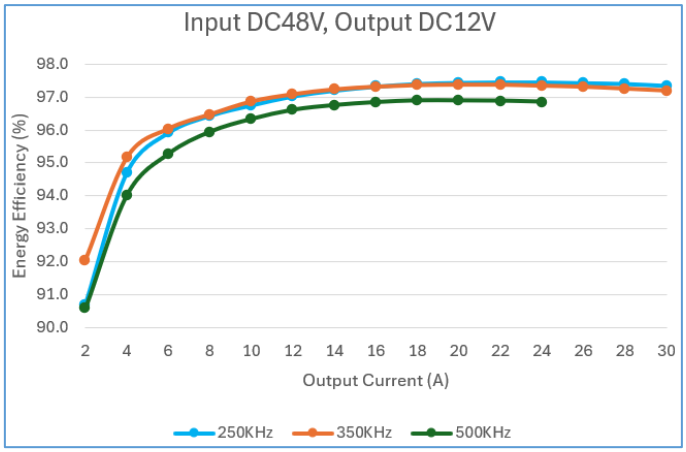


Figure 23. Energy Efficiency at Different Output Current and Switching Frequencies

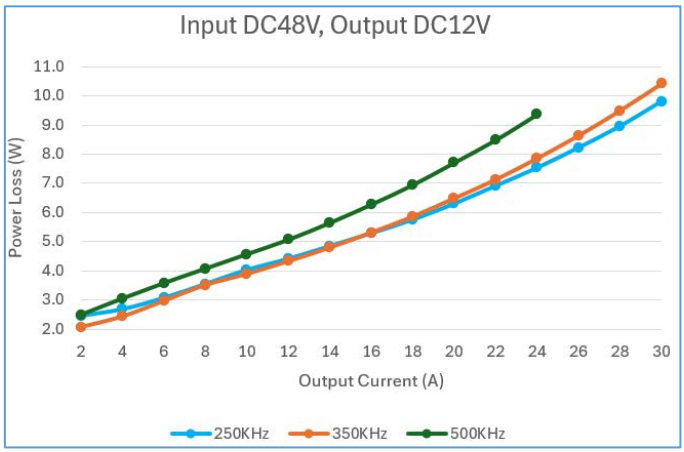


Figure 24. Power Loss at Different Output Current and Switching Frequencies

5.2 Thermal Performance

Table 2 and Table 3 show the maximum output current that GaNs can achieve at around 100 degrees Celsius, with and without airflow, with and without heatsink, and at different switching frequencies. Thermistors were used to test the temperature of the components.

Table 2. Component Temperature–No Heatsink Installed

Axial fan CFM 63.5	Switching Frequency	Max. O/P Current	Component Temp. at ambient 25°C		
			High side GaN	Low side GaN	L1
No	250KHz	21.0A	100.2°C	93.4°C	83.4°C
	350KHz	18.0A	101.1°C	88.6°C	72.5°C
	500KHz	12.5A	100.4°C	81.5°C	64.2°C
Yes	250KHz	30.0A	83.0°C	73.0'°C	52.9°C
	350KHz	30.0A	92.3°C	82.5°C	51.1°C
	500KHz	26.0A	100.0°C	82.3°C	47.3°C

Table 3. Component Temperature–Heatsink Installed

Axial fan CFM 63.5	Switching Frequency	Max. O/P Current	Component Temp. at ambient 25°C		
			Heatsink Point 1	Heatsink Point 2	L1
No	250KHz	23.0A	99.5°C	99.5°C	91.5°C
	350KHz	21.0A	100.2°C	100.0°C	83.6°C
	500KHz	17.0A	100.0°C	99.4°C	76.6°C
Yes	250KHz	30.0A	55.7°C	55.8°C	51.9°C
	350KHz	30.0A	61.1°C	61.1°C	50.1°C
	500KHz	30.0A	75.3°C	75.0°C	57.4°C

Figure 25 shows the measurement location. An axial fan was used in the thermal test; the same test setup as measuring the energy efficiency

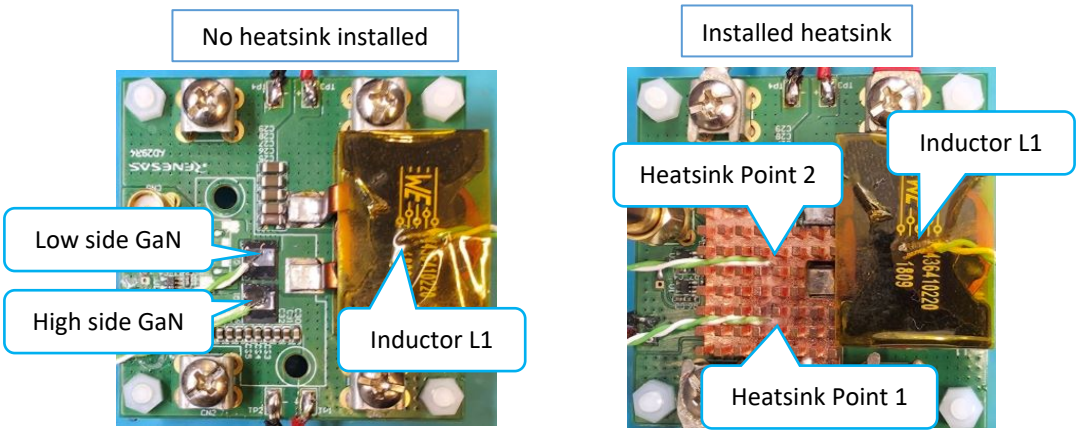


Figure 25. Measurement Location

5.3 Switching Node Voltage Waveforms

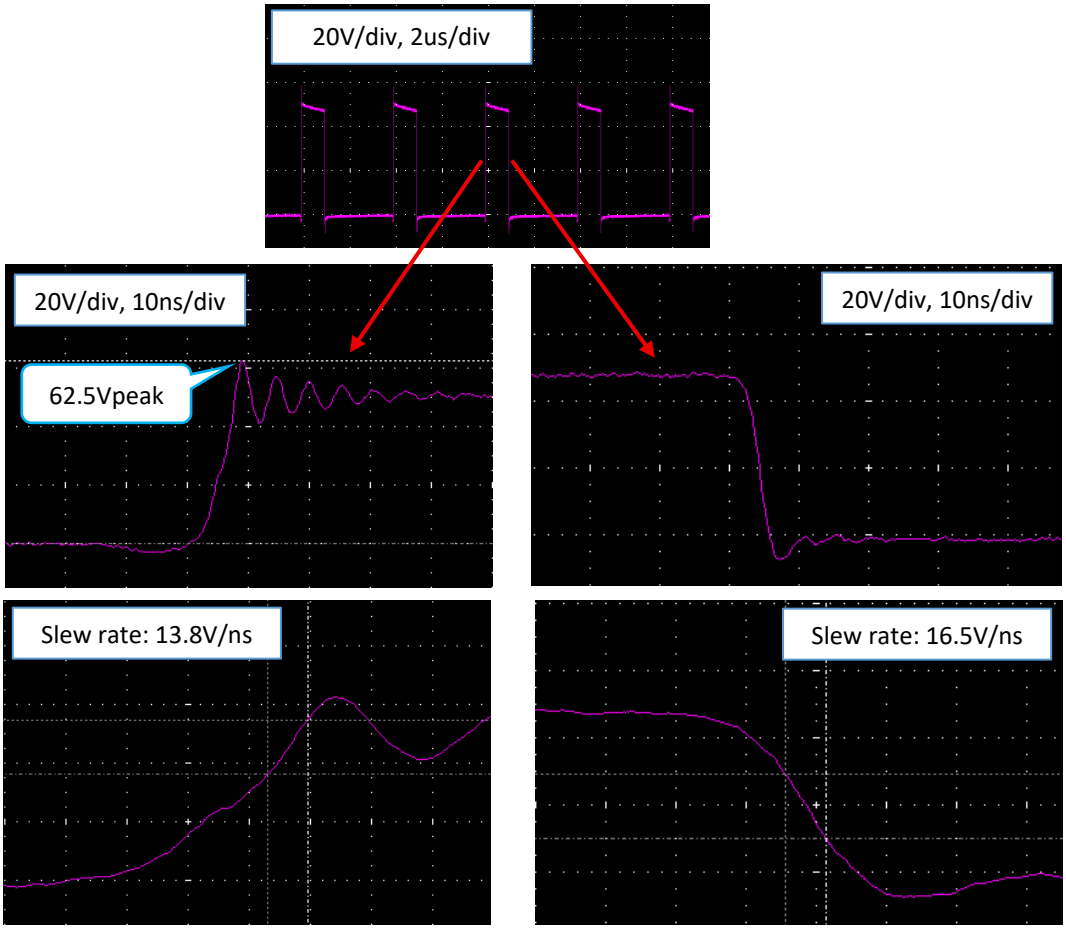


Figure 26. Switching Node Waveforms

6. Board Design and Schematic

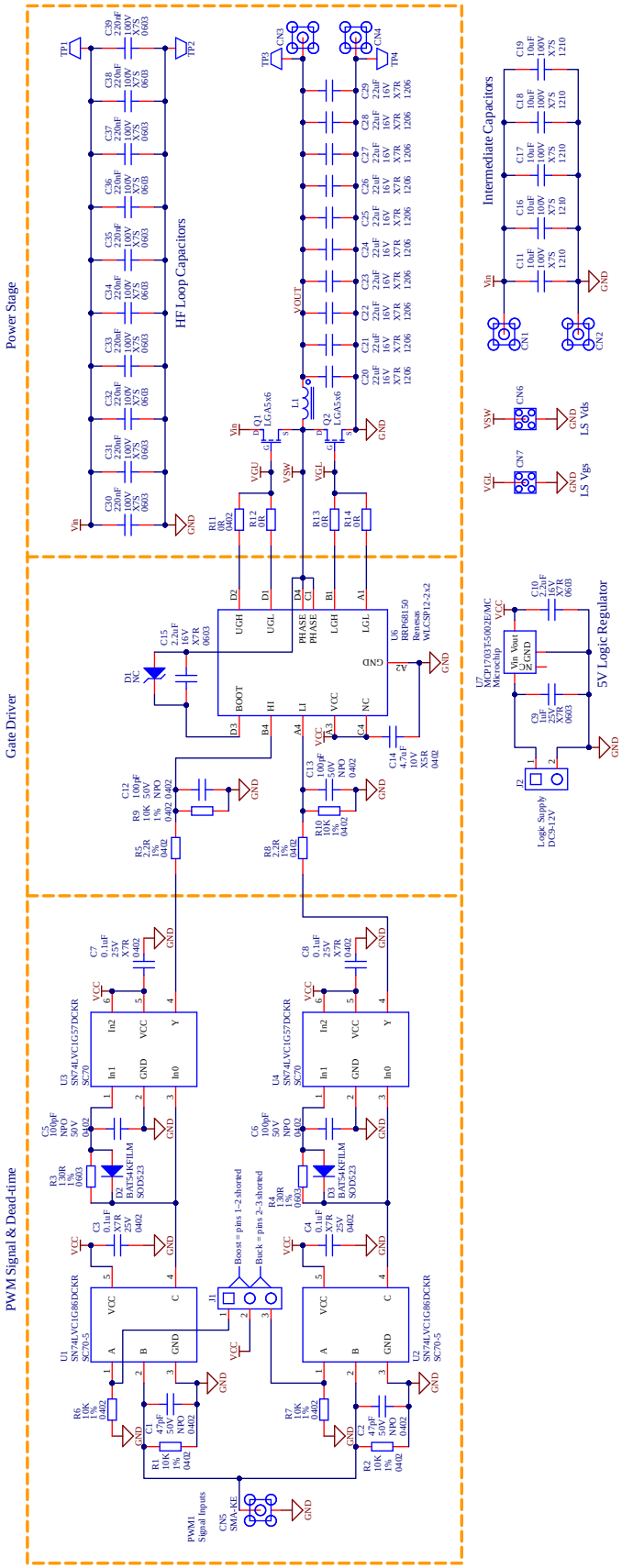


Figure 27. EVB Schematic

6.1 PCB Layout

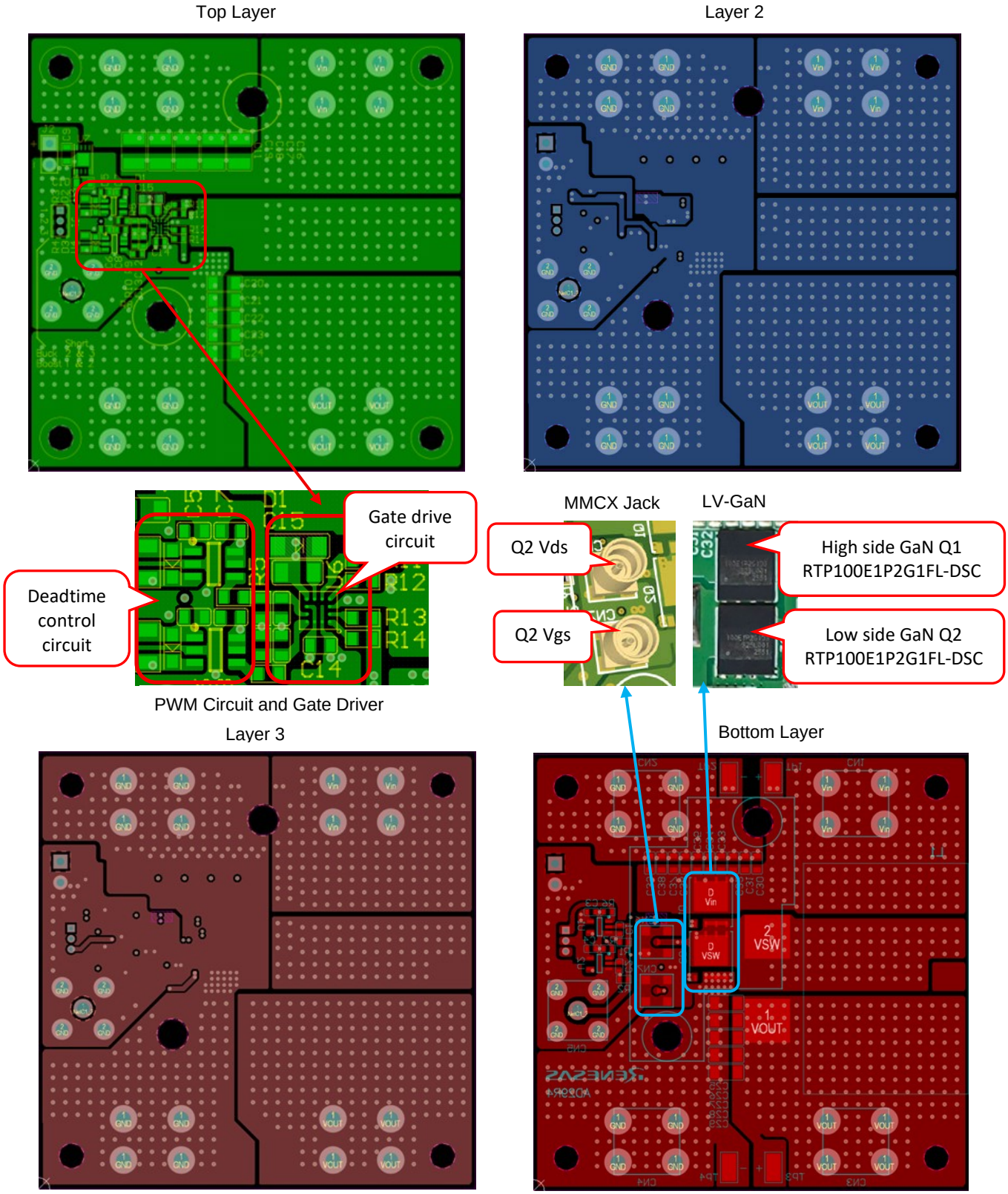


Figure 28. PCB Layout

PCB Specification: PCB file name: AD29R4
Size: 53 × 53 mm
Thickness: 1.6mm
Material: FR4, 2oz for all layers

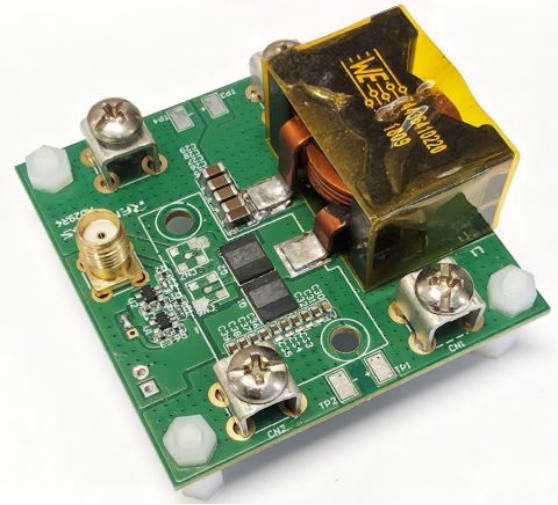
6.2 Bill of Materials

Item	Qty	Reference	Part Description	Manufacturer	Part Number
1	2	C1, C2	47pF, 50V, NPO, 0402		
2	4	C3, C4, C7, C8	0.1uF, 25V, X7R, 0402		
3	4	C5, C6, C12, C13	100pF, 50V, NPO, 0402		
4	1	C9	1uF, 25V, X7R, 0603		
5	2	C10, C15	2.2uF, 16V, X7R, 0603		
6	1	C14	4.7uF, 10V, X5R, 0402		
7	5	C11, C16, C17, C18, C19	10uF, 100V, X7S, 1210		
8	10	C20, C21, C22, C23, C24, C25, C26, C27, C28, C29	22uF, 16V, X7R, 1206		
9	10	C30, C31, C32, C33, C34, C35, C36, C37, C38, C39	220nF, 100V, X7R, 0603		
10	4	CN1, CN2, CN3, CN4	Connector	Keystone	7701
11	1	CN5	Connector	Kinghelm	KH-SMA-KE-Z
12	0	CN6, CN7	MMCX Jack	Molex	734152063
13	2	D2, D3	40 V 30 mA	ST	BAT54KFILM
14	1	L1	2.2uH	Wurth	74436410220
15	2	Q1, Q2	100V, 1.2mΩ, LV-GaN	Renesas	RTP100E1P2G1FL-DSC
16	6	R1, R2, R6, R7, R9, R10	10K, 1%, 0402		
17	2	R3, R4	130Ω, 1%, 0603		
18	2	R5, R8	2.2Ω, 5%, 0402		
19	4	R11, R12, R13, R14	0Ω, 0402		
20	2	U1, U2	SN74LVC1G86DCKR	TI	SN74LVC1G86DCKR
21	2	U3, U4	SN74LVC1G57DCKR	TI	SN74LVC1G57DCKR
22	1	U6	100V eGaN Driver	Renesas	RRP68150-BH0
23	1	U7	5.0 V 250 mA DFN	Microchip	MCP1703T-5002E/MC
24	1	PCB	Size: 53x53mmx1.6mm, 4 layers, 2oz	JDB	AD29R4
25	4	M1, M2, M3, M4	M3*10+6, Nylon, Hex Standoff, White		
26	1	HS1	Heatsink, copper		HD29R4
27	2	TIM	Size 8x15mm, Thickness 0.5mm, Thermal conductivity 6W/m.k		
28	2	Spacer	Material Nylon, 110°C		
29	2	M3 Screw	Size M3 x 10mm, Material 304 stainless steel		
30	2	M3 Nuts	M3 Hexagon nuts		
31	2	Washer	Nylon flat washer, ID3 x OD7 x T1mm		
32	1	Tape 1	Teflon tape, Size 3x16mm. Thickness 0.055mm, 250°C		
33	0	D1, J1, J2, TP1, TP2, TP3, TP4	No components		

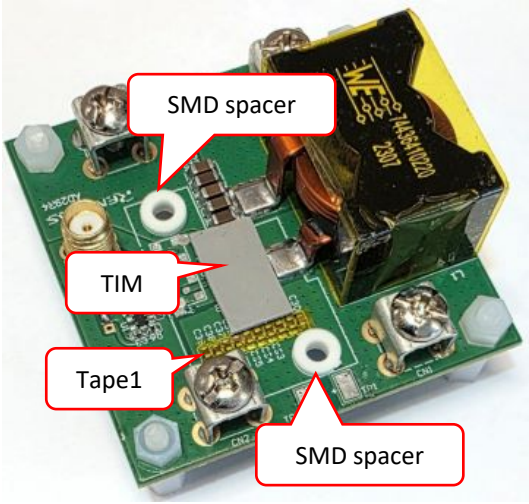
7. Heatsink Installation for GaN Devices

The GaN device RTP100E1P2G1FL-DSC provides a top-side cooling. The pictures below shows the steps for installing a heatsink on top of the GaN device.

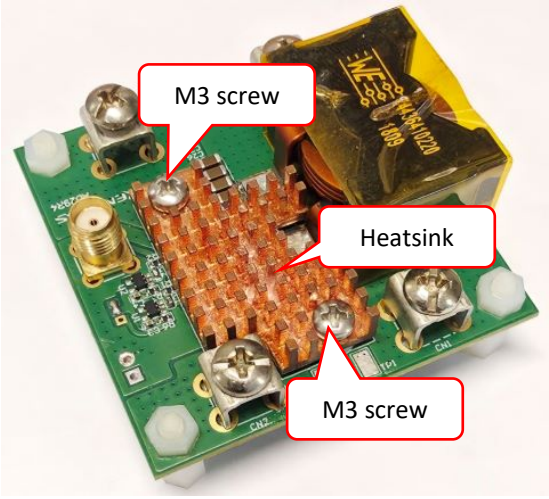
Step 1: Original EVB



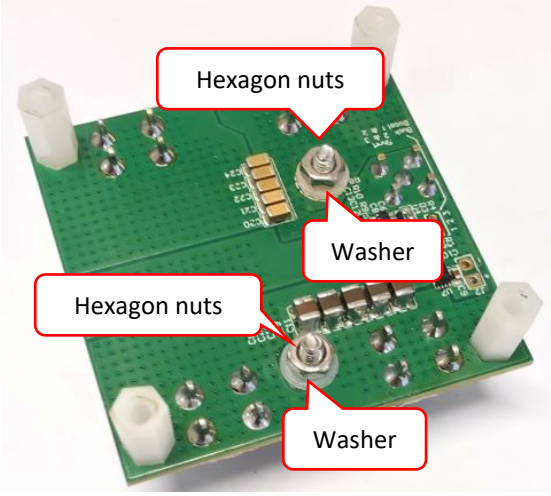
Step 2: Install SMD spacer and TIM



Step 3: Install heatsink and M3 screw



Step 4: Install washer and hexagon nuts



Spacer:
Part No: TW3
Material: Nylon
Temperature: 110°C

TIM:
Thermal conductivity > 5 W/m.k
Size: 8 × 15 mm. Thickness: 0.5 mm
Part No: A6200, t-Global Technology

Heatsink:
Material: Pure copper

Screw:
Size: M3 × 12mm
Material: Carbon steel

Washer:
Nylon flat washer, ID3 × OD7 × T1mm

Torque:
0.6–0.8 N.m

8. Ordering Information

Part Number	Description
EVB-RTP100E1P2G1FL-DSC	Low Voltage GaN RTP100E1P2G1FL-DSC Evaluation Board

9. Revision History

Revision	Date	Description
1.01	Oct 13, 2026	Updated Figure 4.
1.00	Sep 17, 2026	Initial release.

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