5V Input Wireless Power Charging Solution

IDTP9035-TX-A11 EVM USER GUIDE

Features

- WPC compliant
- Input voltage range – 4.75V~5.25V
- Output power –peak power is up to 5W
- With 5V/1.2A input adapter, peak power delivered at receiver end is greater than 4W
- Peek Efficiency (DC in to DC out) – 72%
- Status indication LEDs and buzzer
- System monitoring function enabled by firmware and GUI software
- Easy firmware update via USB and I²C

Evaluation Kit Contents

- IDTP9035 LV DEMO V1.1
- IDTP9035-TX-A11 UG Rev1.3 – this document
- JM60 Programming Dongle
- USB type A to micro-USB type B cable
- 5V AC to DC Power Adapter
- WPC "Qi" Compatible RX Energizer Sleeve
- IDTP9035 Product Datasheet
- CD containing:
  - IDTP9035 control software tool
  - PC_USB Driver software
  - Reference layout Gerber Files
  - Reference layout Cadence Allegro board files
  - Electronic copy of IDTP9035-EVAL manual
  - Electronic copy of IDTP9035 Product Datasheet

General Description

The IDTP9035 LV DEMO evaluation board serves to demonstrate the features and performance of the IDTP9035 Wireless Power Charging solution for Base Station with 5V input voltage and TX-A11 Coil Transmitter. The design allows in detail signal inspection access to different nodes of the schematic by the existing testing points, in this way the system designer may better understand the particularities and the keys functionality.

The evaluation module is a stand-alone application; all it needs is a 5V/1.2A DC power adapter and a WPC certified power receiver.

Optionally the EVM's activity can be monitored by I²C communication and GUI (graphical user interface) software through a USB cabled JM60 dongle board, which interfaces the EVM to the computer. The MAIN tab of the software tool provides real time plots of Coil Current, PWM Frequency, and Duty Cycle including different states of the microcontroller and FOD (foreign object detection).

The evaluation board utilizes an external EEPROM which contains Tx firmware to enable programmability. The external EEPROM memory chip is pre-programmed with a standard start-up program that is automatically loaded when 5V power is applied. The EEPROM can be reprogrammed to suit the needs of specific applications using the IDTP9035 software tool.

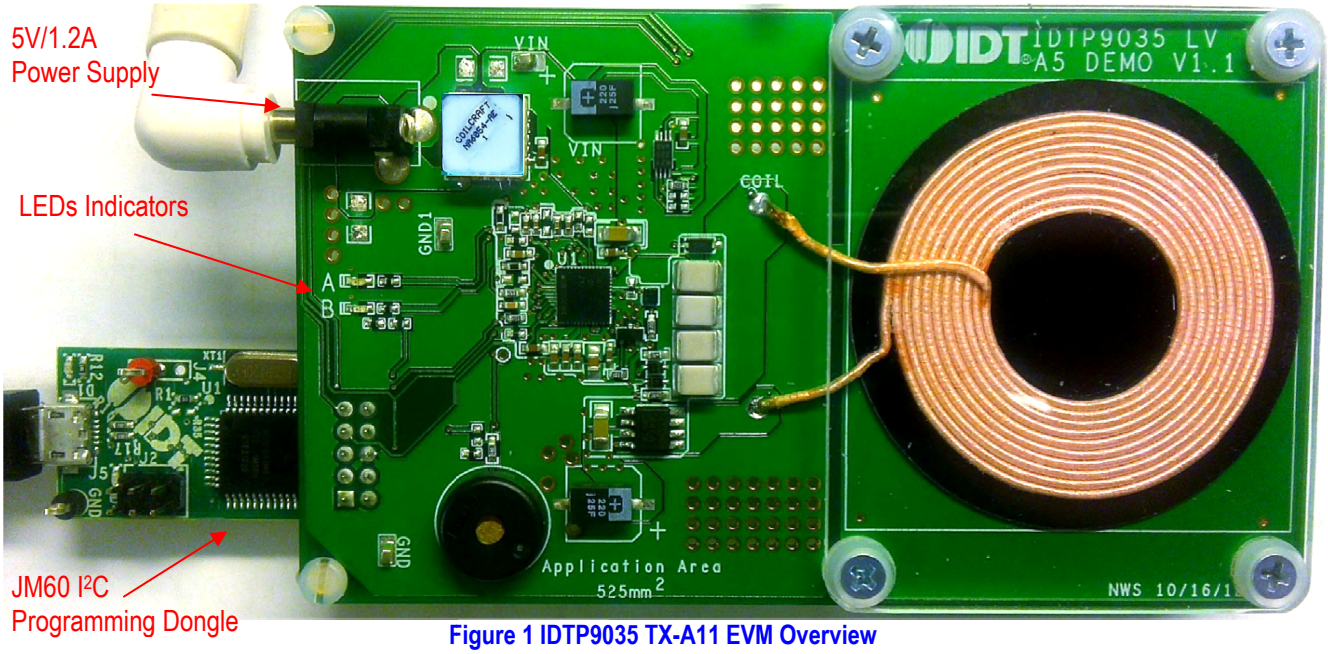

Figure 1 IDTP9035 TX-A11 EVM Overview

Item	Qty	Reference Designator	Description	Manufacturer	Part #	PCB Footprint
1	1	BZ1	BUZZER PIEZO 4KHZ 12.2MM PC MNT	TDK	PS1240P02CT3	BUZZER1
2	5	C3,C13,C29,C30, C31	CAP CER 1UF 35V 10% X5R 0603	Taiyo Yuden	GMK107BJ105KA-T	603
3	4	C5,C8,C15,C33	CAP CER 0.1UF 50V 10% X7R 0603	Murata	GRM188R71H104KA93D	603
4	2	C6,C14	CAP CER 10UF 25V 20% X5R 0805	TDK	C2012X5R1E106M	805
5	2	C9,C17	CAP CER 22UF 25V 10% X7R 1210	Murata	GRM32ER71E226KE15L	1210
6	2	C16,C39	CAP TANT 220UF 6.3V 20% D3L	NP	NP	NP
7	4	C19,C20,C21,C22	CAP CER 0.1UF 100V 5% NP0 1812	TDK	C4532C0G2A104J	2220
8	1	C23	CAP CER 0.022UF 100V X7R 0603	TDK	C1608X7R2A223K	603
9	1	C24	CAP CER 4700PF 100V 10% X7S 0402	TDK	C1005X7S2A472K	402
10	1	C25	CAP CER 1200PF 100V 5% NP0 0603	TDK	C1608C0G2A122J	603
11	1	C26	CAP CER 2200PF 50V 10% X7R 0402	Taiyo Yuden	UMK105B7222KV-F	402
12	1	C27	CAP CER 1800PF 50V 10% X7R 0402	Murata	GRM155R71H182KA01D	402
13	1	C28	CAP CER 3300PF 50V 10% X7R 0402	Murata	GRM155R71H332KA01D	402
14	1	D1	LED SMARTLED 630NM RED 0603 SMD	Osram	L29K-G1J2-1-0-2-R18-Z	0603_DIODE
15	2	D2,D4	SCHOTTKY RECT 20V 2A SOD323F	NXP	PMEG2020EJ	0603_DIODE
16	1	D5	LED SMARTLED GREEN 570NM 0603	Osram	LG L29K-G2J1-24-Z	0603_DIODE
17	1	D6	DIODE SWITCH 200V 250MW SOD123	Diodes INC	BAV21W-7-F	SOD123
18	1	D5	DIODE SWITCH 100V 150MW SOD-523	Diodes INC	1N4148WT-7	0402_DIODE
19	1	J1	CONN POWER JACK 2.1X5.5MM HI CUR	Cui Inc	PJ-002AH	JACK5mm
20	1	L1	6.3uH, Flexible Ferrite Coil	TDK	WT-505060-10K2-A11-G	IND_Y31-60014F
21	2	Q2 (Q1 and Q2)	20V(D-S), Power MOSFET complementary transistor	Vishay	Si4500BDY	SOIC8
22	1	Q4	MOSFET N-CH SGL 60V SOT-23	Zetex	ZXMN3B01FTA	SOT23_3
23	1	Q6	MOSFET N-CH SGL 60V SOT-23	Vishay	SiB488DK-T1-GE3	SC75_6LD
24	2	R6,R10	RES 4.99K OHM 1/10W 1% 0402 SMD	Panasonic	ERJ-2RKF4991X	402
25	2	R7,R9	RES 47 OHM 1/10W 5% 0603 SMD	Panasonic	ERJ-3GEYJ470V	603
26	1	R8	RES 499 OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF4990V	603
27	1	R14	RES 1.00K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1001V	603
28	1	R15	RES 20.0K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF2002V	603
29	1	R16	RES 422 OHM 1/10W 1% 0402 SMD	Panasonic	ERJ-2RKF4220X	603
30	3	R69,R70,R71,R72	RES 47K OHM 1/10W 5% 0402 SMD	Panasonic	ERJ-2GEJ473X	402
31	1	R18	RES 10.0K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1002V	603
32	1	R23	RES 20.0K OHM 1/10W 1% 0402 SMD	Panasonic	ERJ-2RKF2002X	402
33	3	R24,R29,R32	RES 10.0K OHM 1/16W 1% 0402 SMD	Yageo	RC0402FR-0710KL	402
34	2	R33,R34	RES 2.7K OHM 1/10W 5% 0402 SMD	Panasonic	ERJ-2GEJ272X	402
35	1	R38	RES 100K OHM 1/16W 1% 0402 SMD	Yageo	RC0402FR-07100KL	402
36	1	U1	IC EEPROM 64KBIT 400KHZ 8SOIC	Microchip	24LC64-I/SM	SOIC8
37	1	U2	Wireless TX Controller	IDT	IDTP9035	QFN48

1.2. *IDTP9035 LV DEMO V1.1 Generic Application Schematic*

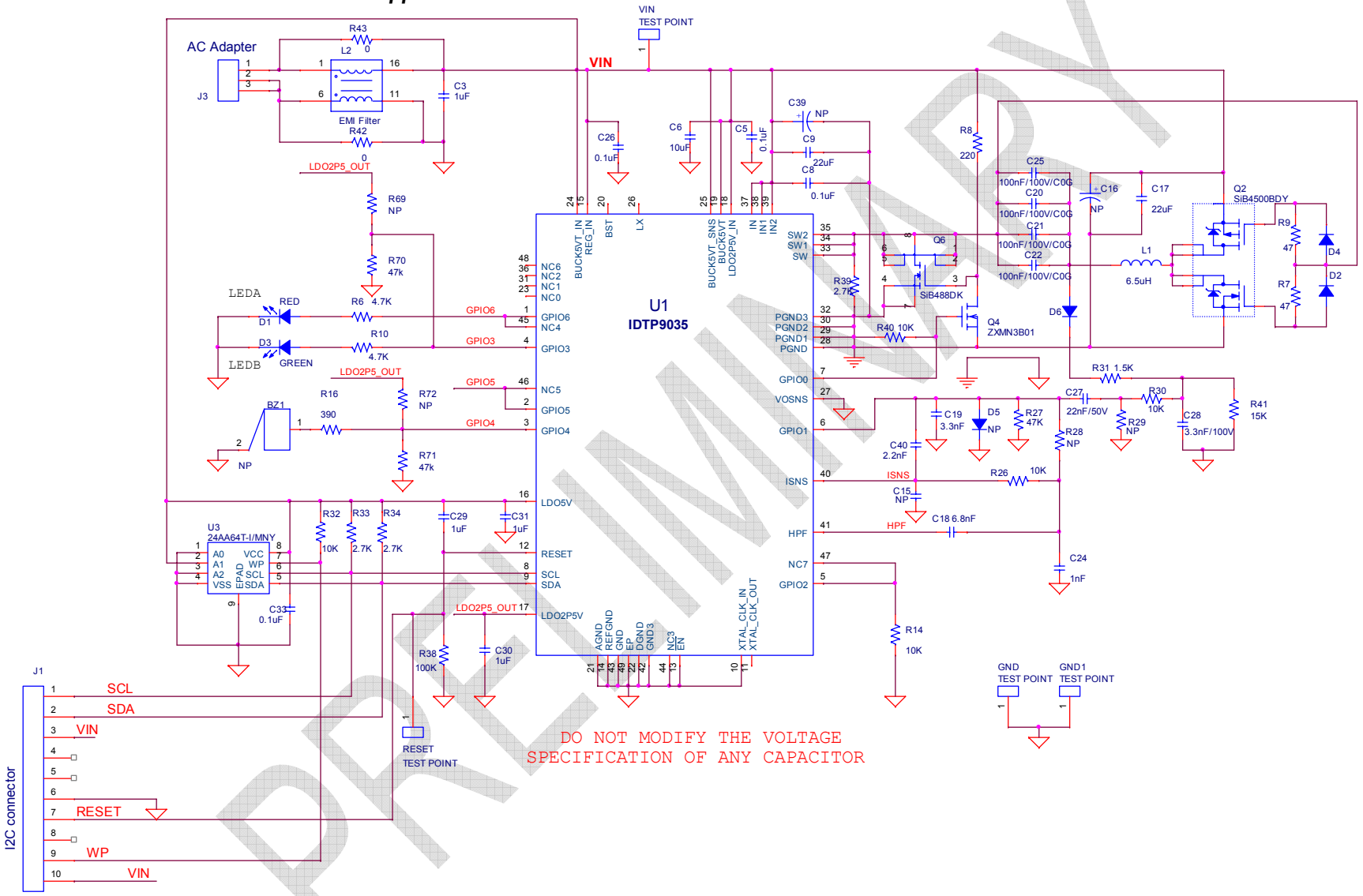

Figure 2 EVM Complete Application Schematic

The application schematic and the PCB layout are subject to change and they're not intended to be used for production purpose. Other components, which are not showed or populated, may be necessarily in order to comply with EMC test or thermal requirements.

1.3. Component placement map

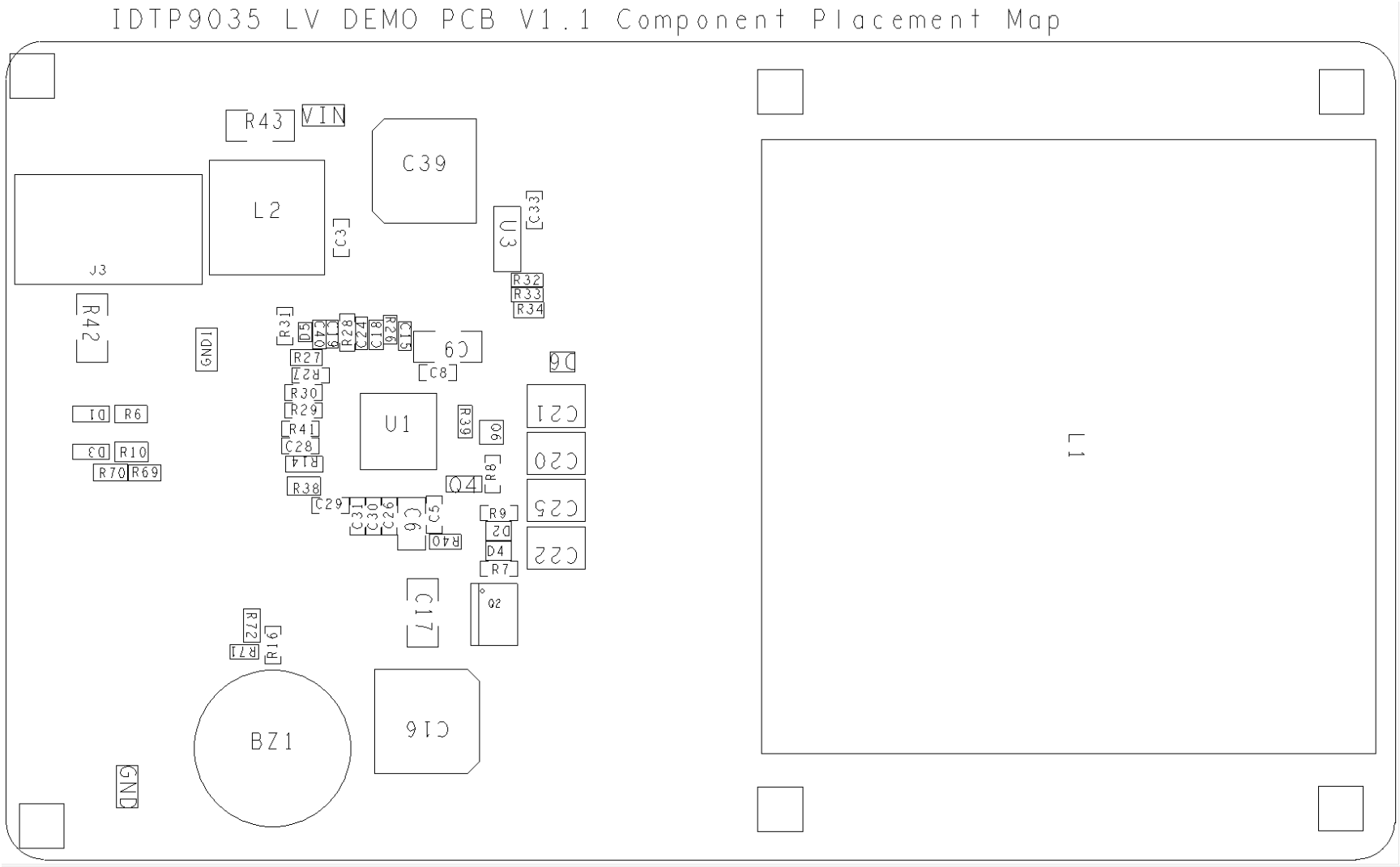

Figure 3 Top layer component map

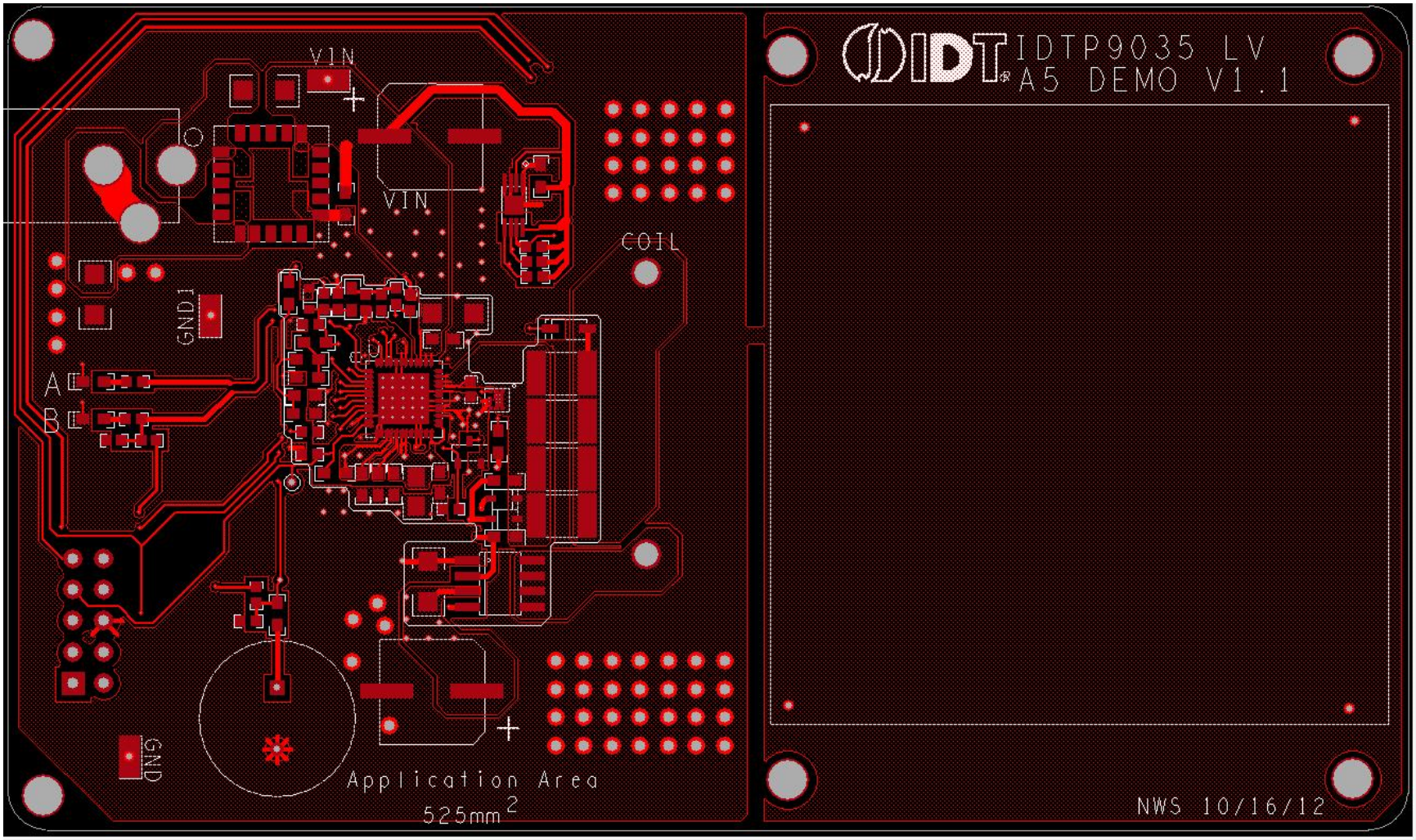

Figure 4 Top and Top Silkscreen Layer

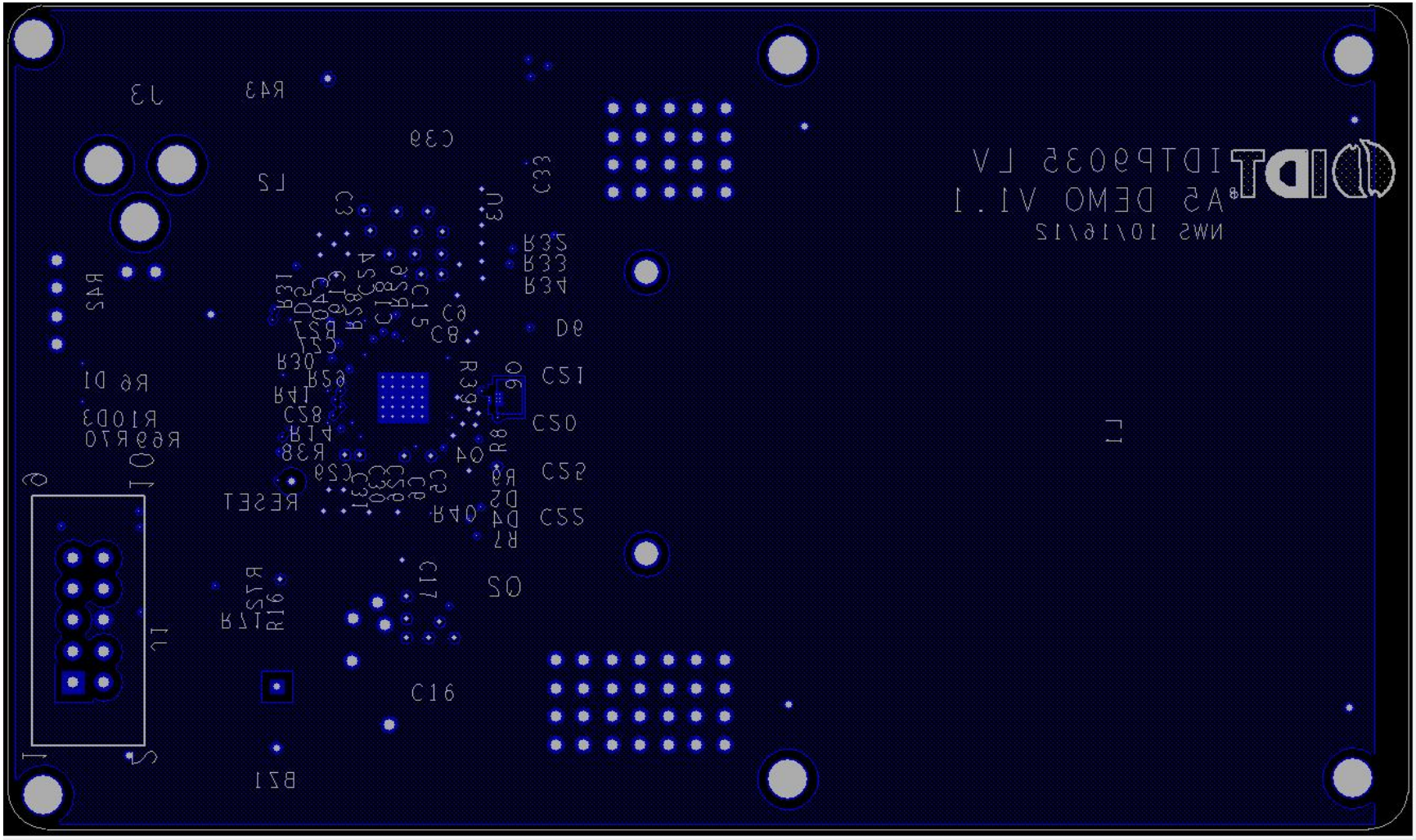

Figure 5 Bottom and Bottom Silkscreen Layer

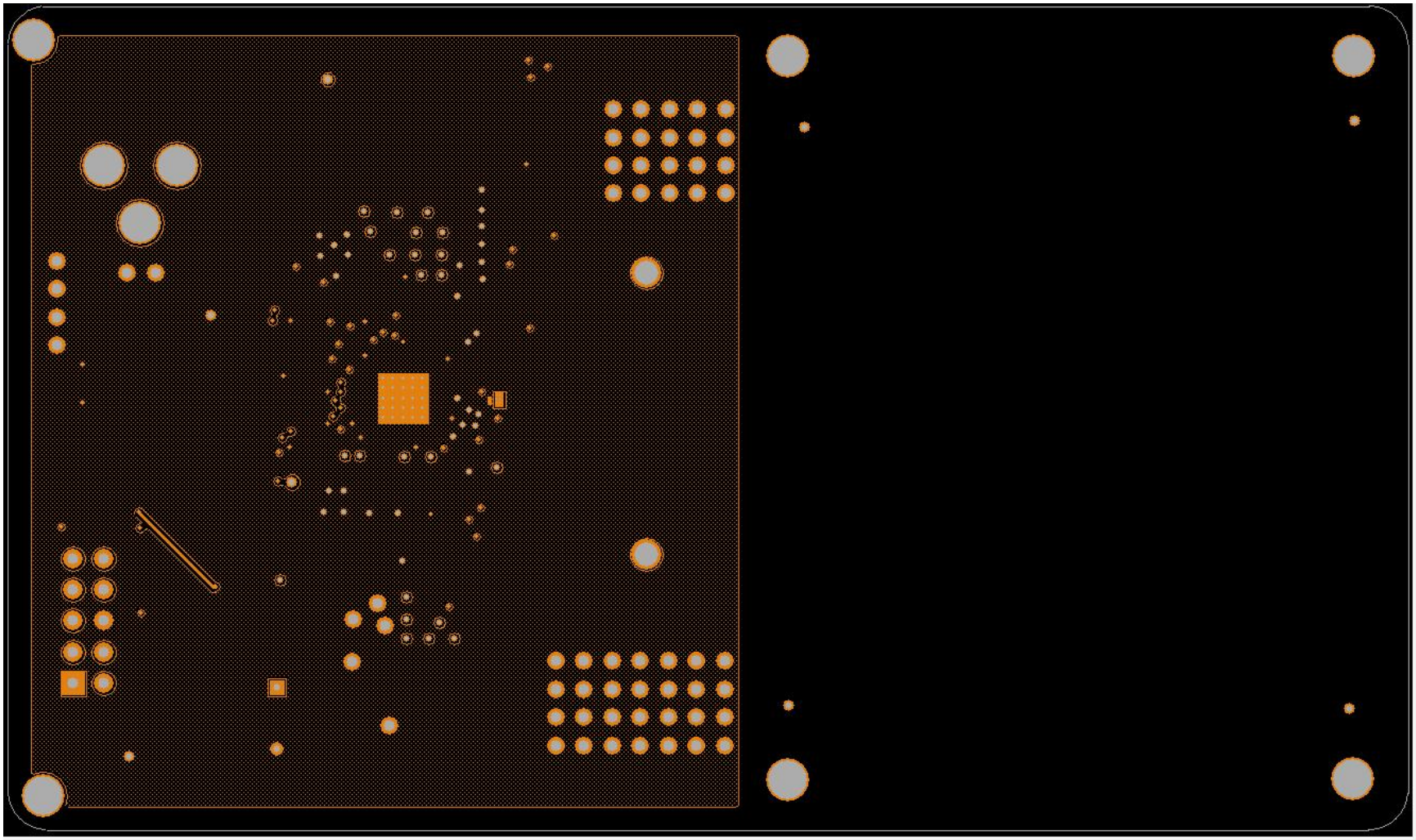

Figure 6 Mid 1 Layer

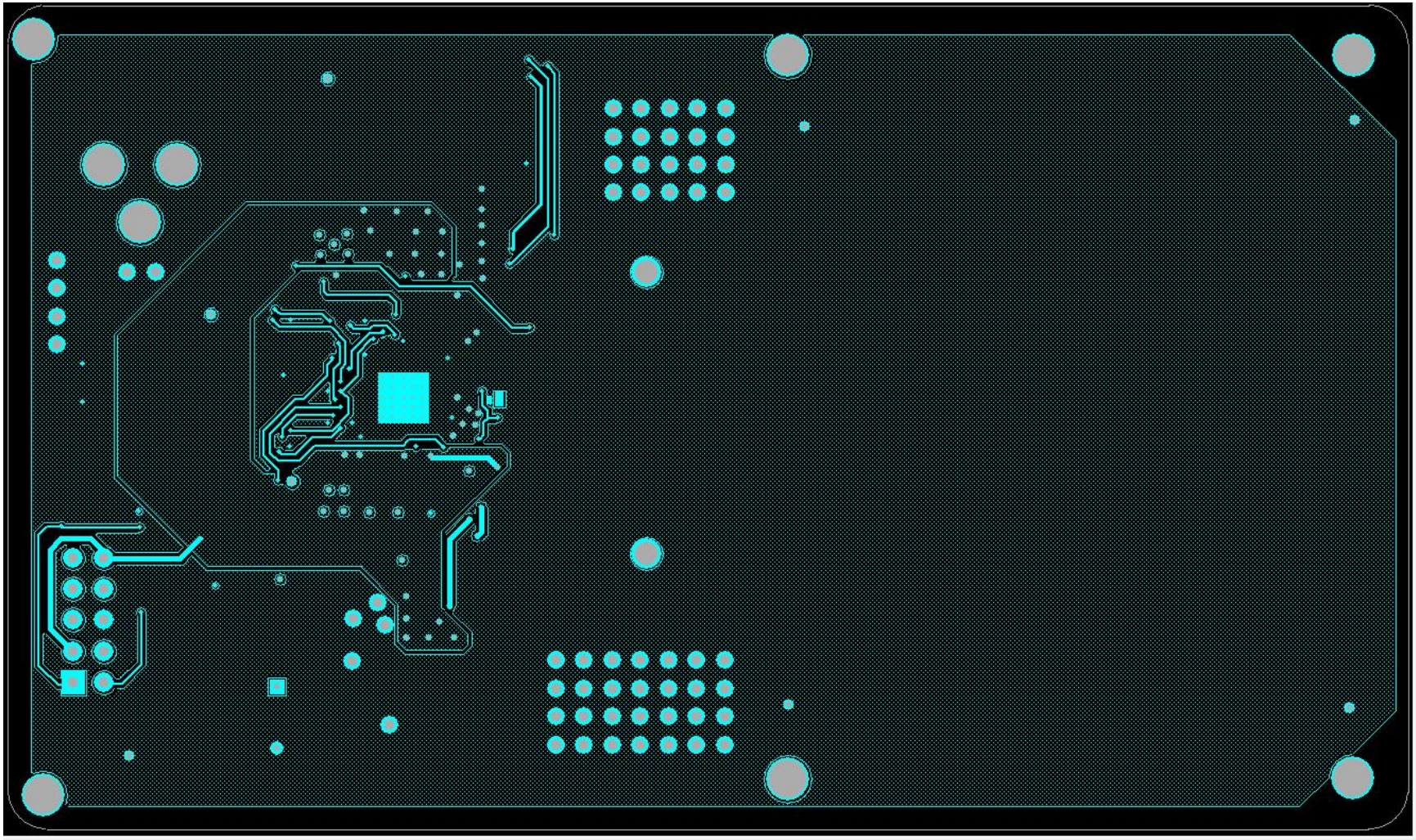

Figure 7 Mid 2 Layer

2. IMPORTANT NOTES

2.1. **PGND Layout Guide**- Care should be taken when routing the PGND connections of Input capacitors (C39, C9, C8), The Source of Q6, Q4, and Q2 (N-CH), and C17, C16. The provided layout file should be followed as closely as possible and deviations should regard the following image for priority. In general, Q6 must be placed close to the SW pins and PGND pins with Q4 placed close by. Q2 should be adjacent to the resonance capacitors.

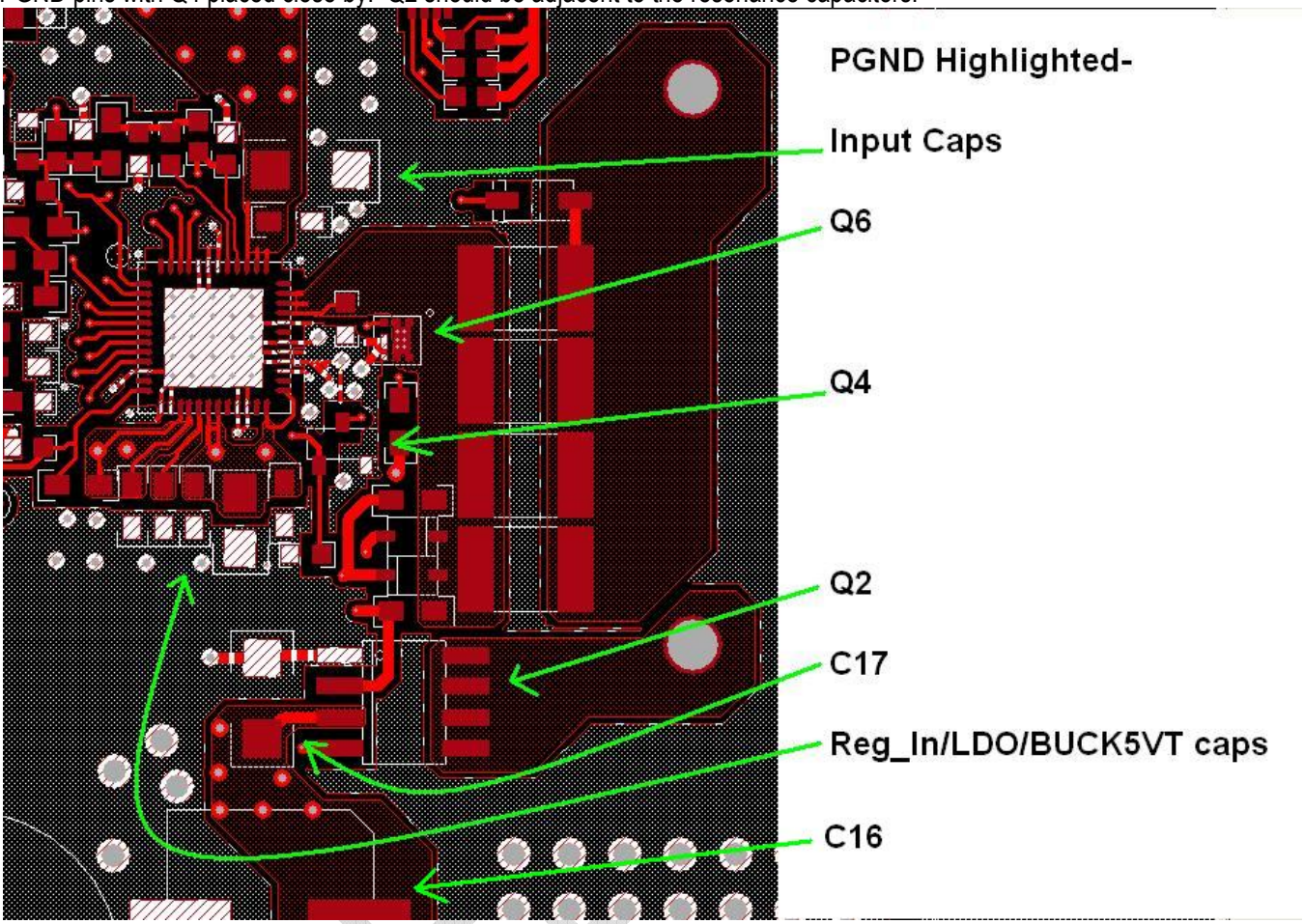

Figure 2 - PGND routing and component placement.

There should be an abundance of vias connecting these PGND connections to the ground layer which is best when placed on the layer directly below the Top layer of the board. This ground plane should not be used for routing and be directly connected to the E-PAD. The LDO and BUCK5VT capacitors should be placed in a row in close proximity of the device.

2.2. VIN Power Connections- The connection from the EMI filter to the Input capacitors should be made with a wide trace of metal or a plane and is best when kept on the top layer of the board. Multiple vias should be used when changing layers with these connections and layer changes should be kept to a minimum. See the image below for the optimal way to connect VIN to C16, C17 and the LDO/BUCK5VT capacitors to the main input capacitors C8, C9, and C39.

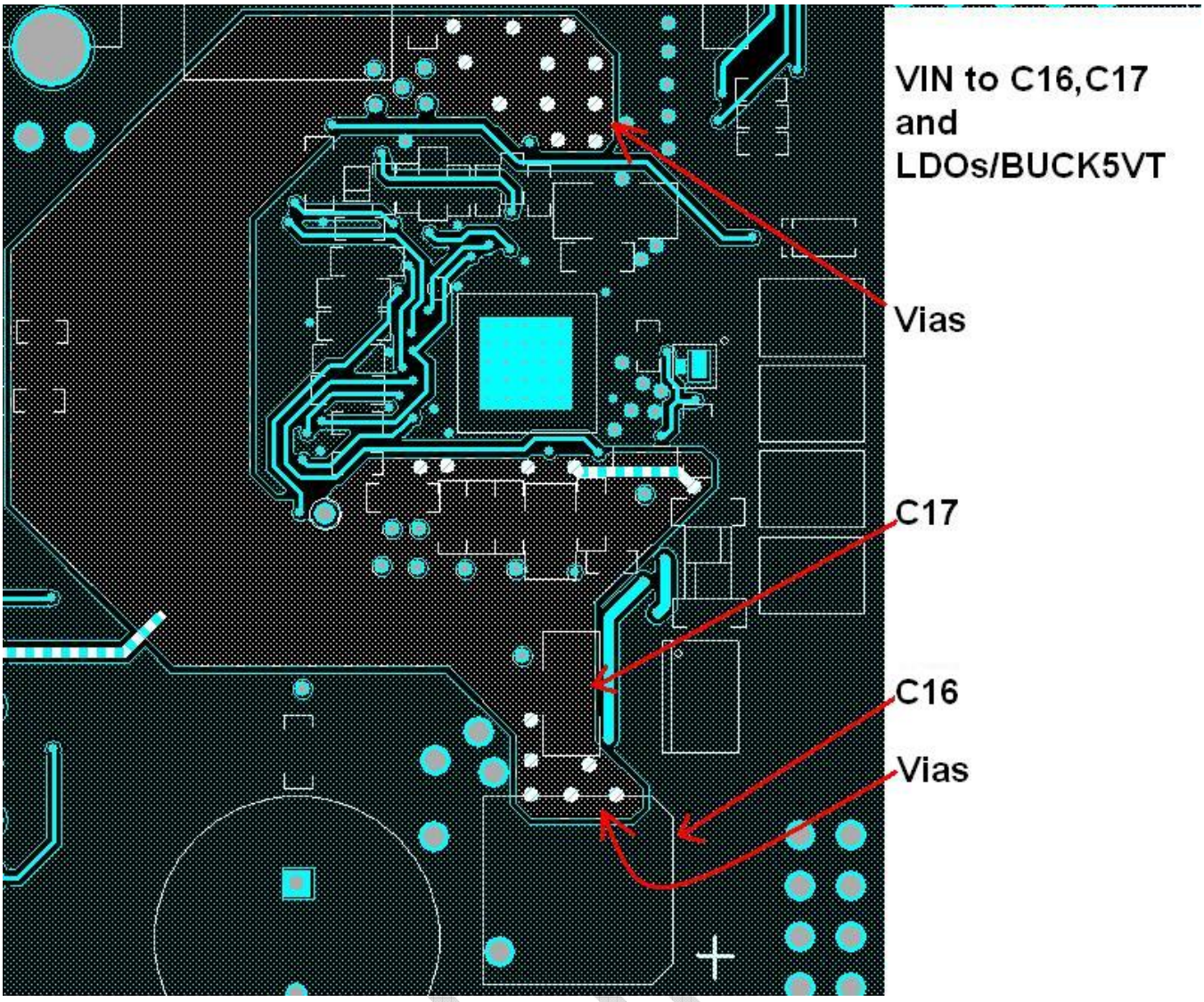

Figure 3 - VIN route to C16, C17 and LDO/BUCK5VT caps on inner layer using many vias for layer transitions

2.3. DEMODULATION noise considerations- Noise can cause interference with proper operation when injected into the DEMODULATION circuit, therefore the components should be placed near the PIN 1 corner of the device and the placement and orientation should be matched to the provided layout when placing the components and routing the signal lines. Furthermore to reduce the opportunity for noise injection they should be routed with 5 mil or 6 mil trace widths. In the attached image, the most critical signal lines have been highlighted and then circled in the schematic image for further clarification.

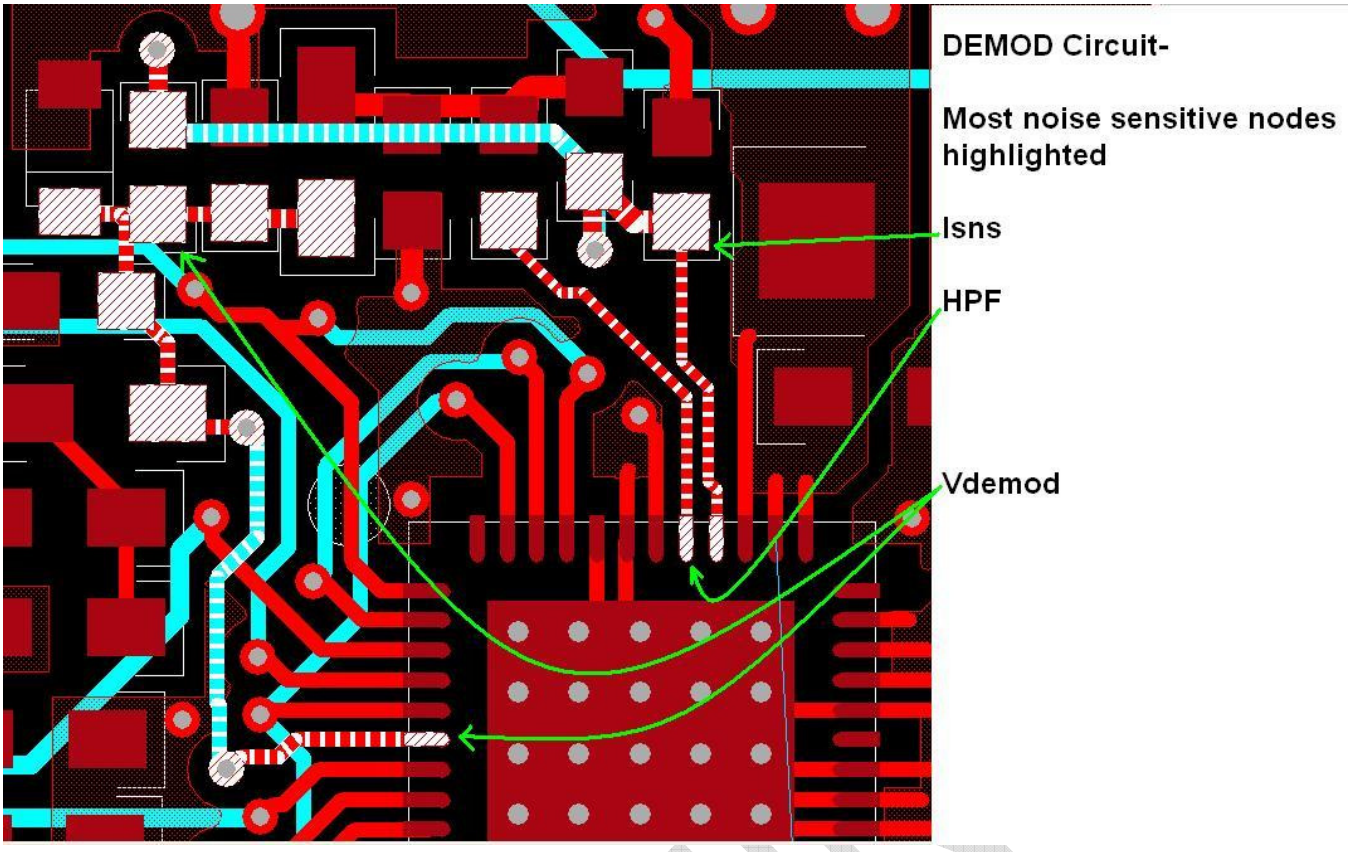

Figure 4 - DEMODULATION most noise sensitive nodes, placement routing recommendations

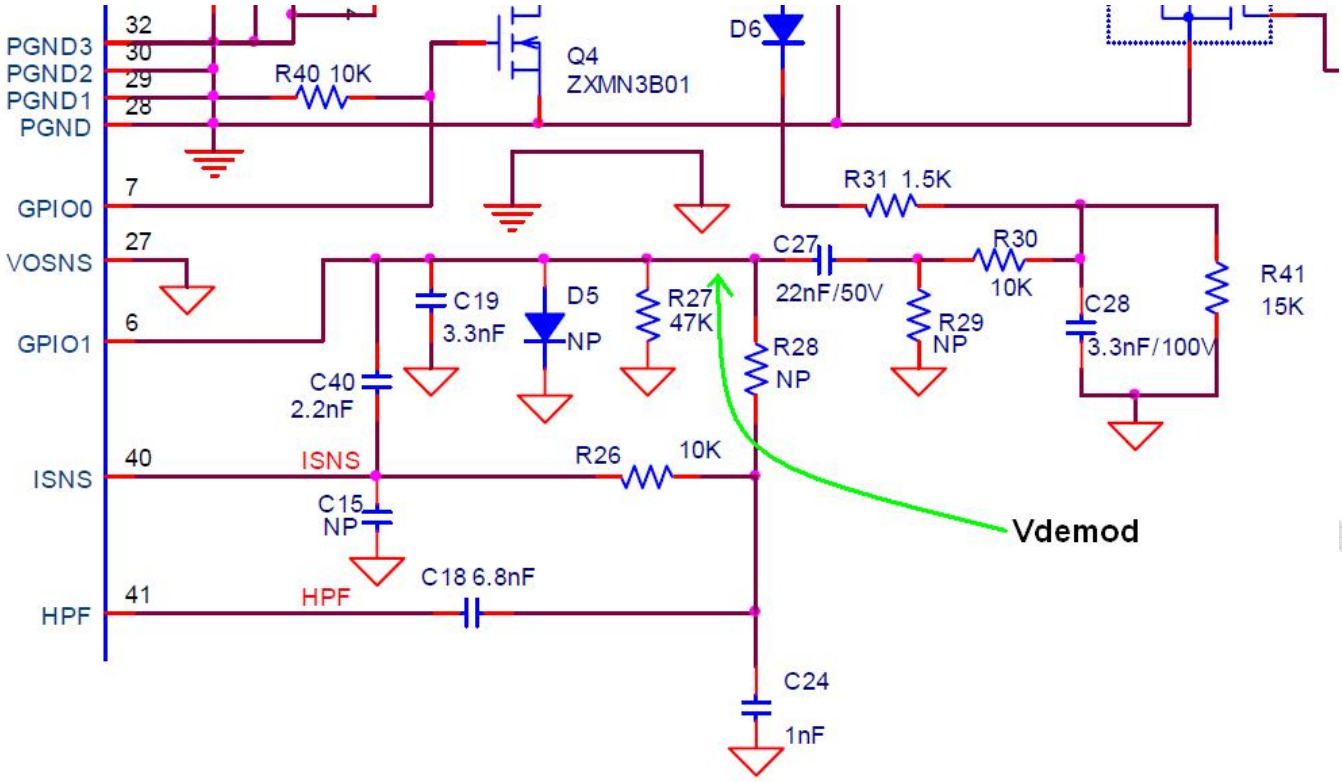

Figure 5 - DEMODULATION most noise sensitive nodes, schematic highlight (Isns, HPF, Vdemod)

Finally R31 should be kept close to the PIN 1 corner of the IDTP9035 to improve noise immunity of the circuit.

2.4. Thermal Considerations- A 5x5 matrix of 12 mils vias spaced at 33 mils apart should be placed within the EPAD. The Bottom Layer should be electrically tied to GND and directly connected to the E-PAD while being used as a solid ground plane as much as possible. Any signals on the bottom layer ground plane should not be placed in the area of the E-PAD in a manner that would impede heat dissipation from the E-PAD to the ground plane. Unused sections of the layout on inner layers should be filled with GND planes in order to improve noise shielding, increase heat dissipation, and reduce GND impedance.

3. ORDERING GUIDE

Table 1. Ordering Summary

PART NUMBER	MARKING	PRICE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
IDTP9035TX LV DEMO V1.0	IDTP9035TX LV DEMO V1.0	$149.00	0°C to +70°C	Box 14”x10”x2”	1

Revision History

November 6, 2012 Version V1.4. Add R70 and R71 pulldown resistors to LEDB and Buzzer.

February 5, 2013 Version 1.5. Correct BOM reference designators.

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