NEC

User's Manual

IE-703129-MC-EM1

In-Circuit Emulator Option Board

Target Device
V850E/CA2™ JUPITER

Document No. U16262EE3V0UM00
Date Published September 2002

Printed in Germany

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

MS-DOS and MS-Windows are either registered trademarks or trademarks of Microsoft Corporation in the United States and/or other countries.
PC/AT and PC DOS are trademarks of IBM Corp.

The related documents in this publication may include preliminary versions. However, preliminary versions are not marked as such.

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by th customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

M5 2000.03

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Europe) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 01
Fax: 0211-65 03 327

Sucursal en España
Madrid, Spain
Tel: 091- 504 27 87
Fax: 091- 504 28 60

Succursale Française
Vélizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

Filiale Italiana
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

Branch The Netherlands
Eindhoven, The Netherlands
Tel: 040-244 58 45
Fax: 040-244 45 80

Branch Sweden
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

United Kingdom Branch
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
Singapore
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Guarulhos, Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

Introduction

Readers

This manual is intended for users who design and develop application systems using the V850E/CA2^{TM} JUPITER.

Purpose

The purpose of this manual is to describe the proper operation of the IE-703129-MC-EM1, and their basic specifications.

Organization

This manual is broadly divided into the following parts.

- Overview
- Name and function of components
- Factory settings
- Cautions
- Debugger operation
- Limitations

How to Read This Manual

It is assumed that the reader of this manual has general knowledge of electrical engineering, logic circuits, and microcontrollers.
The IE-703129-MC-EM1 are used connected to the IE-V850E-MC-A in-circuit emulator. This manual explains the basic setup procedure and switch settings of the IE-703129-MC-EM1. For the names and functions, and the connection of parts, refer to the **IE-V850E-MC-A User's Manual**, which is a separate volume.

To understand the basic specifications and operation methods broadly
→ Read this manual in the order listed in **CONTENTS**.

To know the operation methods and command functions of the IE-V850E-MC-A, IE-703129-MC-EM1.
→ Read the user's manual of the debugger (separate volume) that is used.

Conventions

Note	:	Explanation of (Note) in the text
Caution	:	Item deserving extra attention
Remark	:	Supplementary explanation to the text
Numeric notation	:	Binary . . . xxxx or xxxB Decimal . . . xxxx Hexadecimal . . . xxxxH or 0x xxxx

Prefixes representing powers of 2 (address space, memory capacity)

K (kilo): $2^{10} = 1024$

M (mega): $2^{20} = 1024^2 = 1,048,576$

G (giga): $2^{30} = 1024^3 = 1,073,741,824$

Terminology The meanings of terms used in this manual are listed below.

Emulator	Combination of IE-V850E-MC-A and IE-703129-MC-EM1.
Target device	Device that is emulated.
Target system	The system (user-built system) to be debugged. This includes the target program and user-configured hardware.

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

- **Documents related to V850E/CA2**

Document Name	Document Number
V850E/CA2 Jupiter Hardware User's Manual	Under preparation
V850E1 User's Manual-Architecture	U14559EJ
µPD703128, µPD703129 Data Sheet	Under preparation

- **Documents related to development tools (User's Manual)**

Product Name	Document Number
IE-V850E-MC-A (In-circuit emulator)	U14487EJ
IE-703129-MC-EM1 (In-circuit emulator optional board)	This manual

Table of Contents

List of Figures

List of Tables

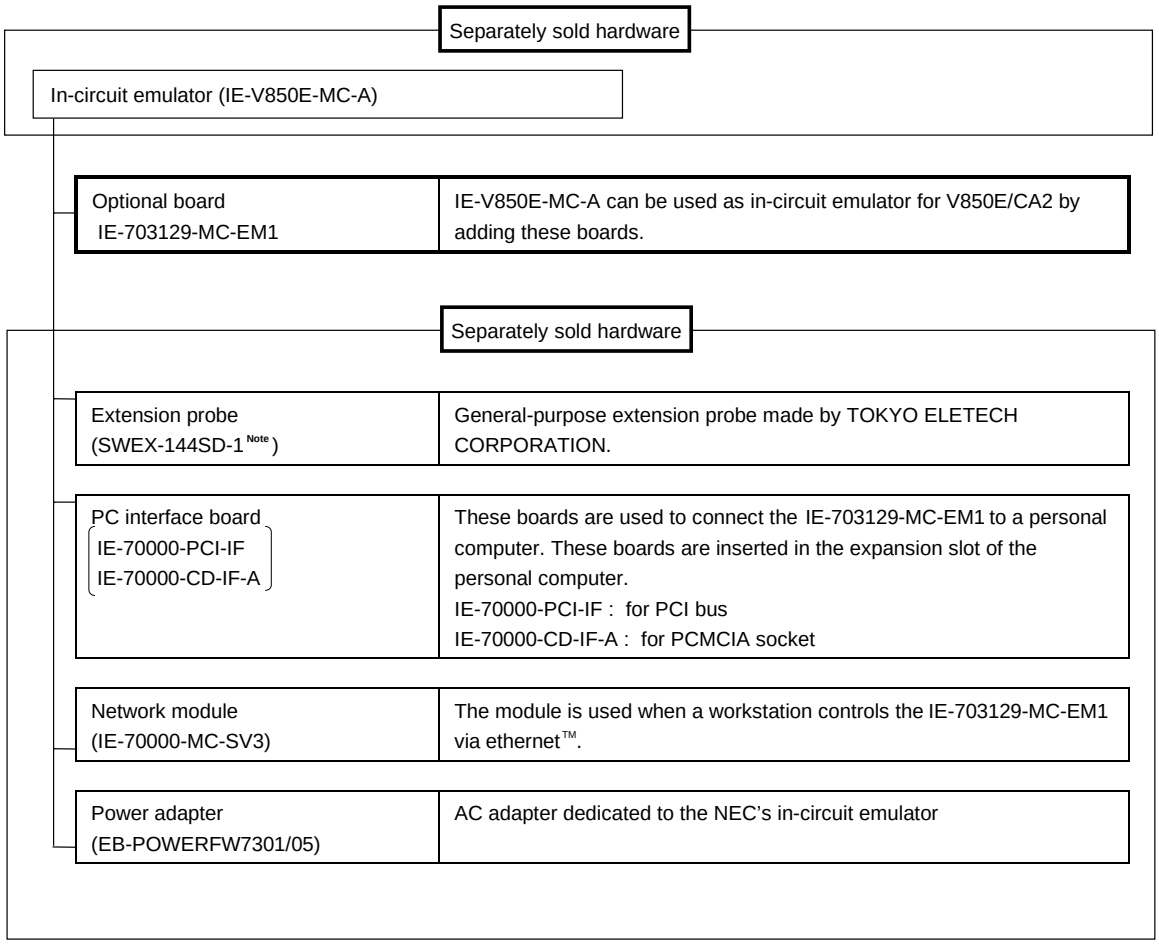
Chapter 1 Overview

The IE-703129-MC-EM1 is an optional board for the in-circuit emulator IE-V850E-MC-A. By connecting the IE-703129-MC-EM1 to IE-V850E-MC-A, hardware and software can be debugged efficiently in system development using the V850E/CA2 JUPITER.

In this manual, the basic setup sequences and switch settings of the IE-703129-MC-EM1 when connecting it to the IE-V850E-MC-A are described. For the names and functions of the parts of the IE-V850E-MC-A, and for the connection of elements, refer to the **IE-V850E-MC-A User's Manual** which is a separate volume.

1.1 Hardware Configuration

Figure 1-1: Hardware Configuration



Note: For further information, contact Daimaru Kogyo Co., Ltd.
Tokyo Electronic Components Division (TEL +81-3-3820-7112)
Osaka Electronic Components Division (TEL +81-6-244-6672)

1.2 Features (When Connected to IE-V850E-MC-A)

- Maximum operation frequency: 36 MHz
- Maximum operating frequency of the quartz oscillator: 5 MHz
- Extremely lightweight and compact
- Higher equivalence with target device can be achieved by omitting buffer between signal cables.
- Following pins can be masked: $\overline{\text{RESET}}$, NMI, $\overline{\text{WAIT}}$
- Two methods of connection to target system:
  - Direct connection of the IE-703129-MC-EM1
  - Attach an extension probe (sold separately) to the connection tab of the IE-703129-MC-EM1.
- Dimensions of the IE-703129-MC-EM1 are as follows.

Table 1-1: Dimensions of the IE-703129-MC-EM1

Parameter		Value
Power dissipation		0.6 W (at 36-MHz operation frequency)[Note]
External dimensions (Refer to **APPENDIX A DIMENSIONS**)	Height	41 mm
	Length	191.5 mm
	Width	121 mm
Weight		240 g

Note: The power dissipation is 11.6 W when IE-V850E-MC-A + IE-703129-MC-EM1.

1.3 Function Specifications (When Connected to IE-V850E-MC-A)

Table 1-2: Function Specifications

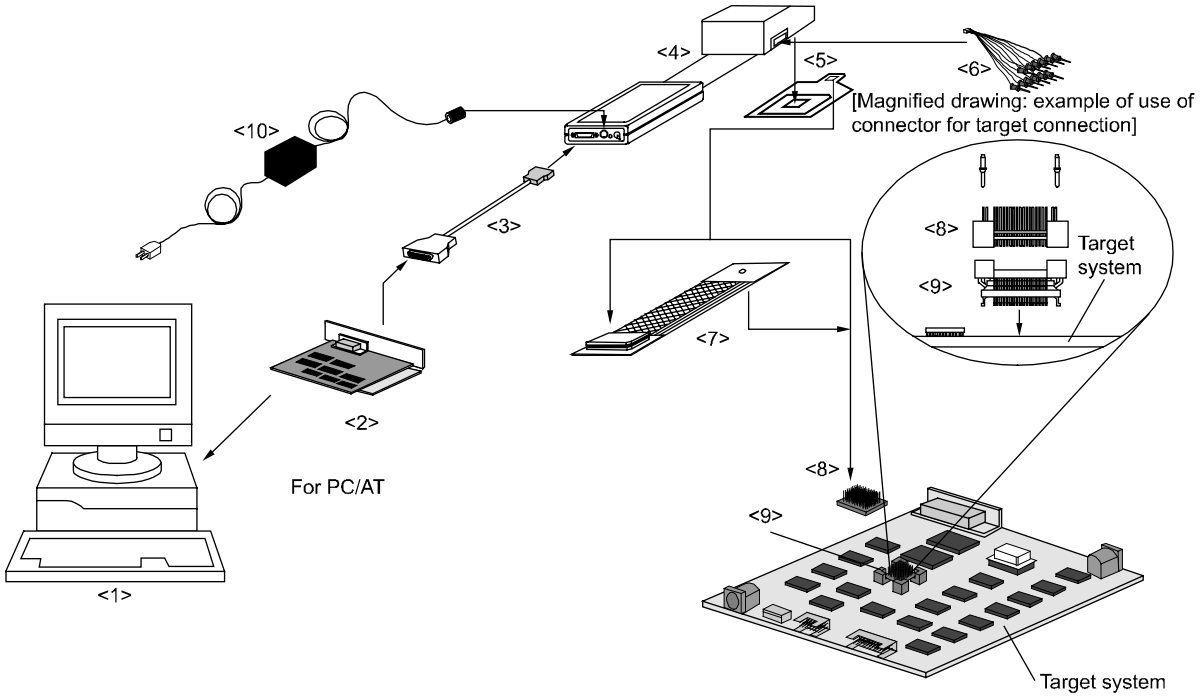
Parameter		Specification
Emulation memory capacity	Internal ROM	None
	External memory	4.5 Mbytes (mounted on the option board in three banks: 2 MB + 2 MB + 512 KB)
Execution/pass detection Coverage memory capacity	Internal ROM	None
	External memory	2 Mbytes
Memory access detection Coverage memory capacity	External memory	1 Mbyte
Trace memory capacity		168 bits × 32 Kframes
Time measurement function		Can be measured with time tag and timers (3 lines)
External logic probe		8-bit external trace is possible
		Event setting for trace/break is possible
Break function		Event break
		Step execution break
		Forced break
		Fail safe break • Illegal access to peripheral I/O • Access to guard space • Write to the ROM space

Caution: Some of the functions may not be supported depending on the debugger used.

1.4 System Configuration

The system configuration when connecting the IE-703129-MC-EM1 to the IE-V850E-MC-A, which is then connected to a personal computer (PC/AT compatible) is shown below.

Figure 1-2: System Configuration



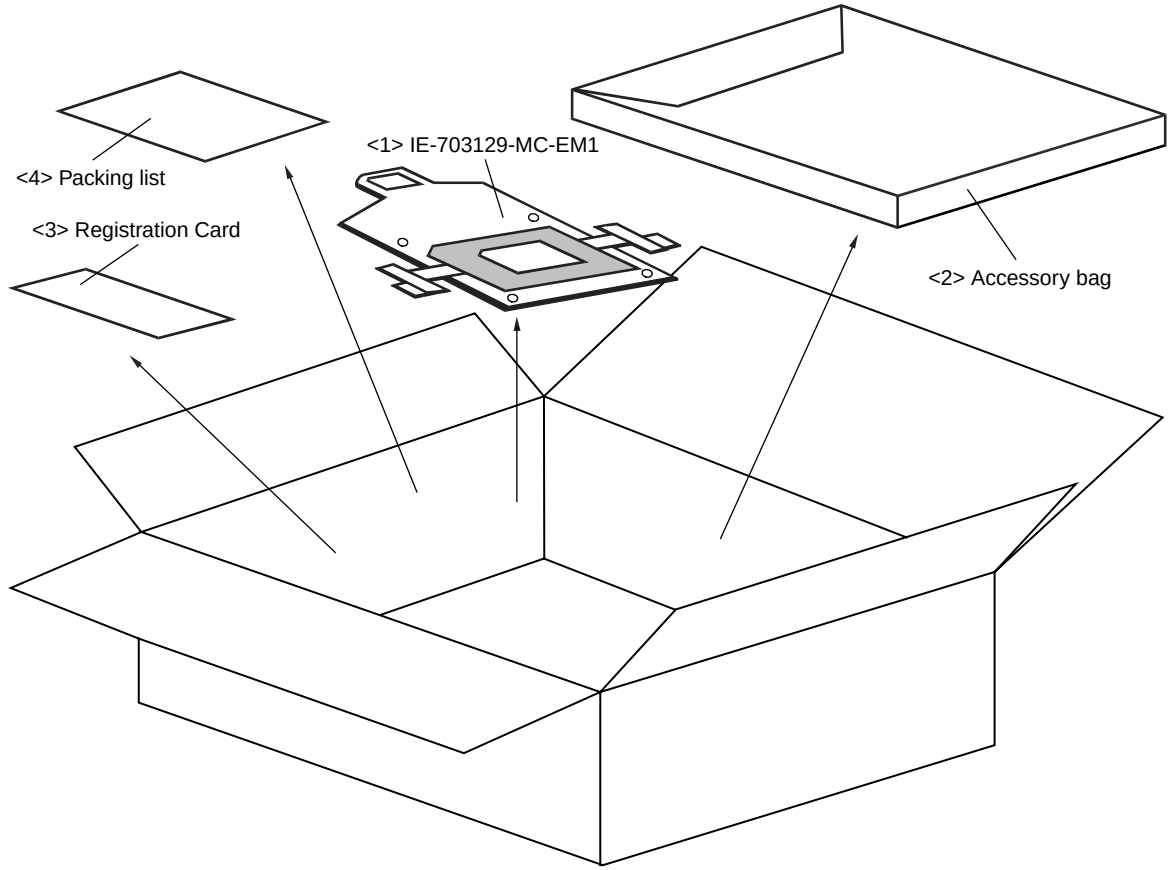
Remark

<1> Personal computer
<2> PC interface board (IE-70000-PCI-IF, IE-70000-CD-IF-A: sold separately)
<3> PC interface cable (included with IE-V850E-MC-A)
<4> In-circuit emulator (IE-V850E-MC-A: sold separately)
<5> In-circuit emulator option board (IE-703129-MC-EM1)
<6> External logic probe (included with IE-V850E-MC-A)
<7> Extension probe (SWEX-144SD-1: sold separately)
<8> Connector for emulator connection (YQPACK144SD: included)
<9> Connector for target connection (NQPACK144SD: included)
<10> Power adapter (EB-POWERFW7301/05: sold separately)

1.5 Contents in Carton

The carton of the IE-703129-MC-EM1 contains a main unit, guarantee card, packing list, and accessory bag. Make sure that the accessory bag contains this manual and connector accessories. In case of missing or damaged contents, contact an NEC sales representative or an NEC distributor.

Figure 1-3: Contents in Carton



<1> IE-703129-MC-EM1 × 1
<2> Accessory bag × 1
<3> Registration card × 1
<4> Packing list × 1

Caution: Make sure that the accessory bag contains this manual and an accessory list (1 sheet).

1.6 Connection between IE-V850E-MC-A and IE-703129-MC-EM1

The procedure for connecting the IE-V850E-MC-A and IE-703129-MC-EM1 is described below.

Caution: Connect carefully so as not to break or bend connector pins.

<1> Remove the pod cover (upper and lower) of the IE-V850E-MC-A.
<2> Set the PGA socket lever of the IE-703129-MC-EM1 to the OPEN position as shown in Figure 1-3 (b).
<3> Connect the IE-703129-MC-EM1 to the PGA socket at the back of the pod (refer to **Figure 1-3 (c)**). When connecting, position the IE-V850E-MC-A and IE-703129-MC-EM1 so that they are horizontal.
Spacers can be connected to fix the pod. (refer to **APPENDIX D MOUNTING OF PLASTIC SPACER**)
<4> Set the PGA socket lever of the IE-703129-MC-EM1 to the CLOSE position as shown in Figure 1-3 (b).
<5> Fix the IE-703129-MC-EM1 between the pod covers (upper and lower) with nylon rivets.
<6> Secure the pod cover (upper) end with nylon rivets.

Figure 1-4: Connection between IE-V850E-MC-A and IE-703129-MC-EM1 (1/2)

(a) Overview

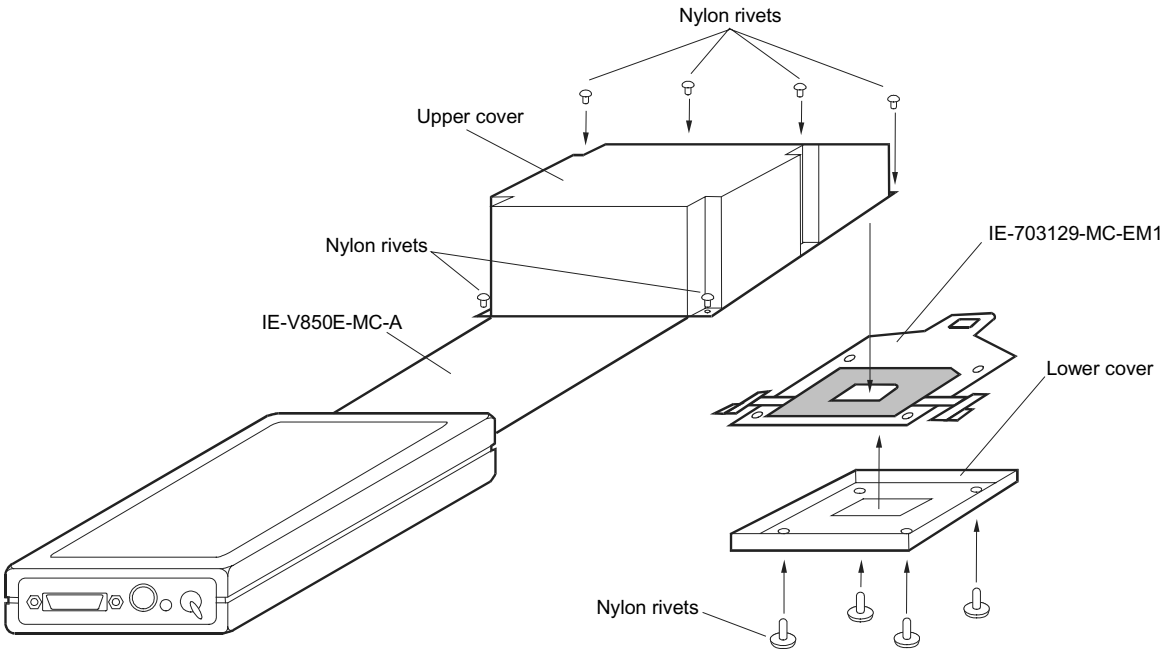
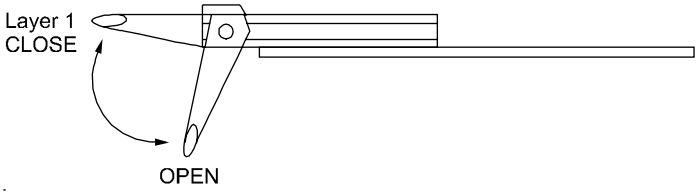
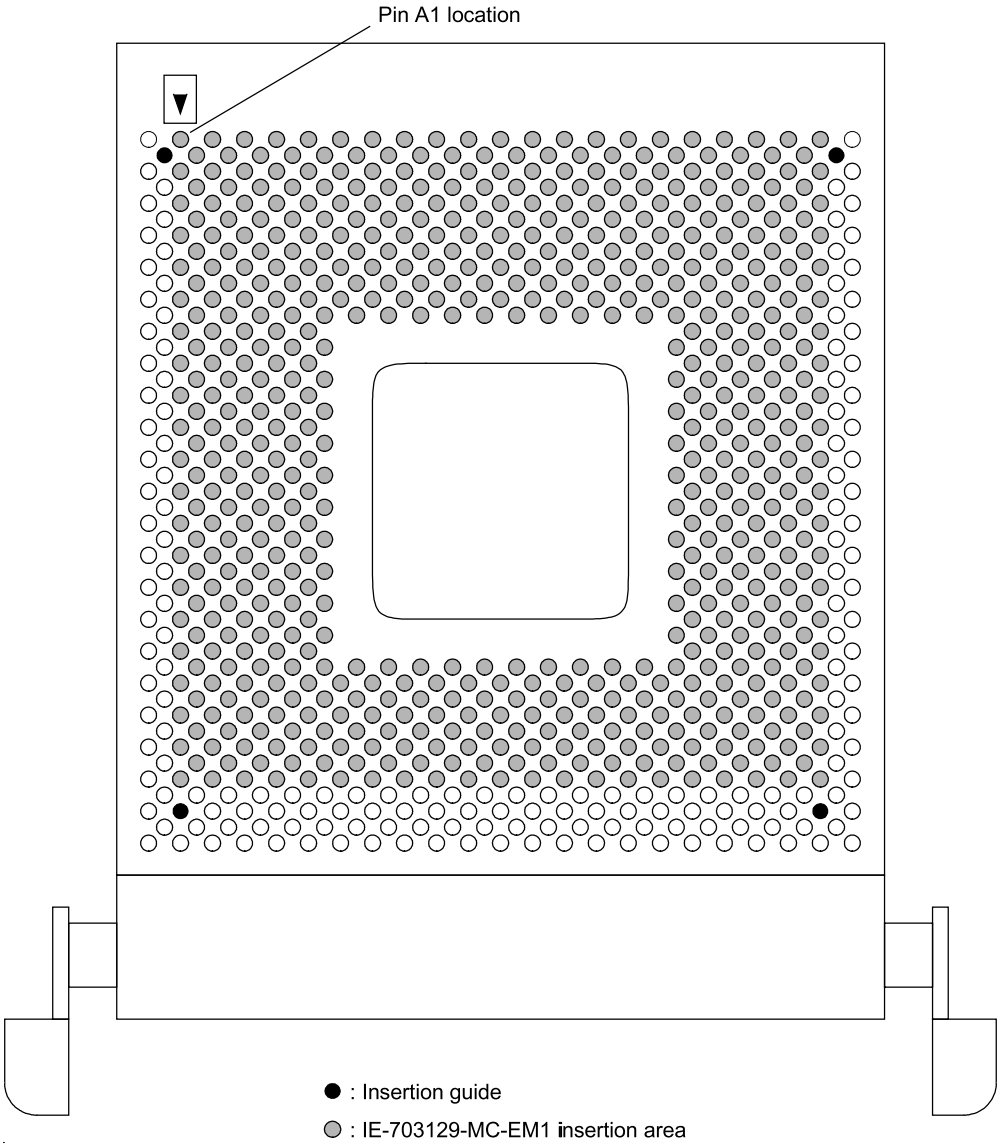


Figure 1-4: Connection between IE-V850E-MC-A and IE-703129-MC-EM1 (2/2)

(b) PGA Socket Lever of IE-703129-MC-EM1



(c) Connecting part (IE-703129-MC-EM1)



[MEMO]

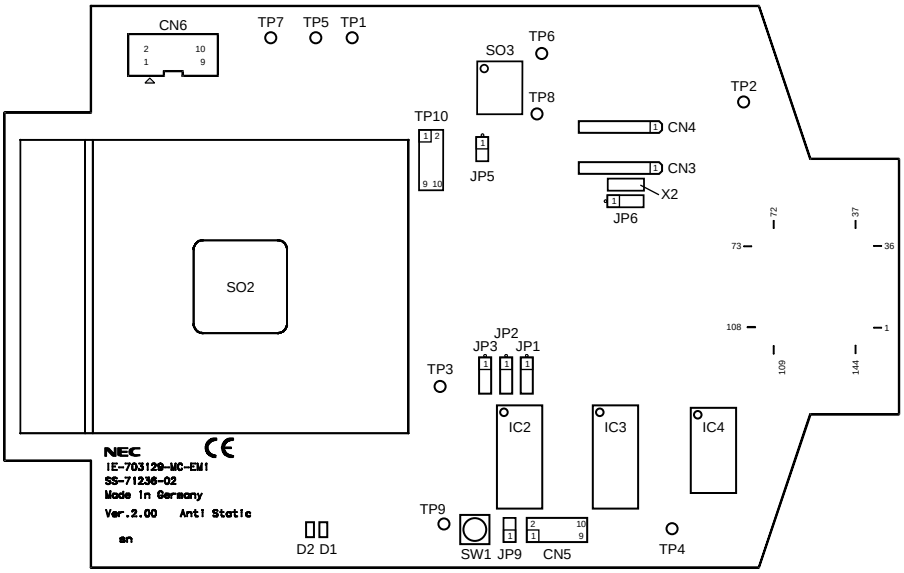
Chapter 2 Name and Function of Components

This chapter describes the names, functions, and switch settings of components comprising the IE-703129-MC-EM1. For the details of the pod, jumper, and switch positions, etc., refer to the **IE-V850E-MC-A User's Manual**.

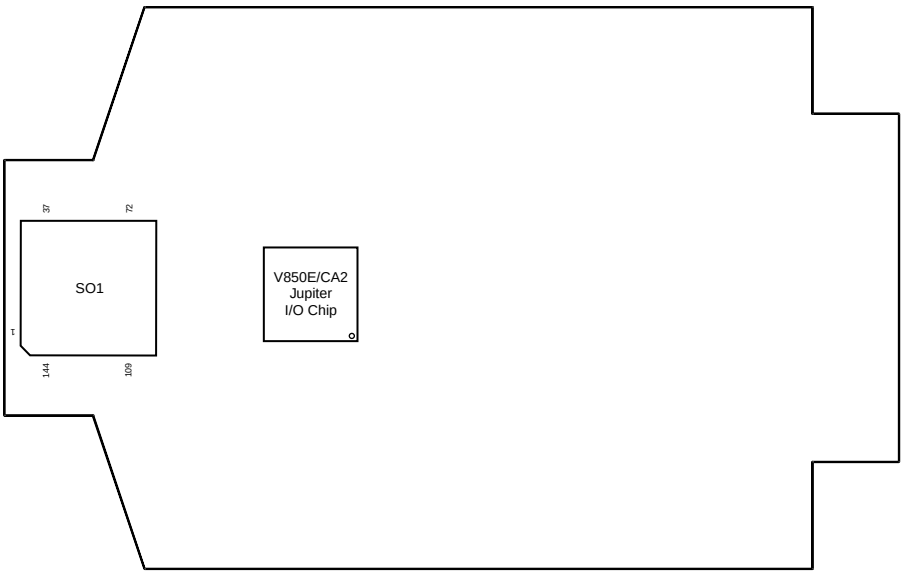
2.1 Component Name and Function of IE-703129-MC-EM1

Figure 2-1: IE-703129-MC-EM1

(a) Top View



(b) Bottom View



(1) Test pins

Table 2-1: Test pins

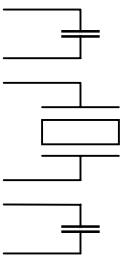
Test Pins	Function
TP1 - TP4	GND
TP5	5 V supply from IE-V850E-MC-A
TP6	Buffered 5 V from target
TP7	Buffered 3.3 V from target
TP8	Oscillator output (main clock)
TP9	Reset
TP10	Reserved

(2) Connector List

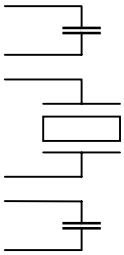
Table 2-2: Connector List

Connector	Function
CN1, CN2	Reserved
CN3	Socket for main-clock crystal incl. capacitors
CN4	Socket for sub-clock crystal incl. capacitors (not assembled)
CN5	Reserved
CN6	Ext. logic probe (3.3 V or 5 V) (refer to IE-V850E-MC-A User's Manual)

(a) Pin Configuration of CN3

Pin	Signal	Intended usage
1	GND	
2	Xtal (X1)	
3	Xtal (X1)	
4	GND	
5	Xtal (X2)	
6	Xtal (X2)	
7	GND	

(b) Pin Configuration of CN4

Pin	Signal	Intended usage
1	GND	
2	Xtal (XT1)	
3	Xtal (XT1)	
4	GND	
5	Xtal (XT2)	
6	Xtal (XT2)	
7	GND	

(c) Pin Configuration of CN6

Signal	Pin	Pin	Signal
EXTPROBE(0)	1	2	EXTPROBE(1)
EXTPROBE(2)	3	4	EXTPROBE(3)
EXTPROBE(7)	5	6	EXTPROBE(6)
EXTPROBE(5)	7	8	EXTPROBE(4)
GND	9	10	GND

(3) Sockets

Table 2-3: Sockets

Socket	Function
SO1	Socket for target connection (optionally via probe cable)
SO2	Socket for IE-V850E-MC-A connection
SO3	Socket of crystal oscillator module for main clock supply (1 to 5 MHz)

(4) LEDs

Table 2-4: LEDs

LED	Function
D1 (red)	Indicates program execution. 0: Program is executed 1: Program is halted
D2 (green)	Indicates detection of valid target power (3.3 V, 5 V, CVcc and GND)

(5) Buttons

Table 2-5: Buttons

Button	Function
SW1	Reset (Only EM1, not target hardware)

(6) Jumpers

Table 2-6: Jumper List

Jumper	Function	1-2	2-3
JP1	AV_{REF}	Target	Internal 5 V
JP2	AV_{DD}	Target	Internal 5 V
JP3	AV_{SS}	Target	Internal GND

Jumper	Function	Open	Closed
JP4	Stand-alone operation	Normal operation	Stand-alone operation

Jumper	Function	Open	Closed
JP5	Main clock source	Oscillator (internal or target)	Crystal (internal)

Jumper	Function	1-2	2-3
JP6	Sub-clock source selection	32.768 KHz (on board)	Target hardware

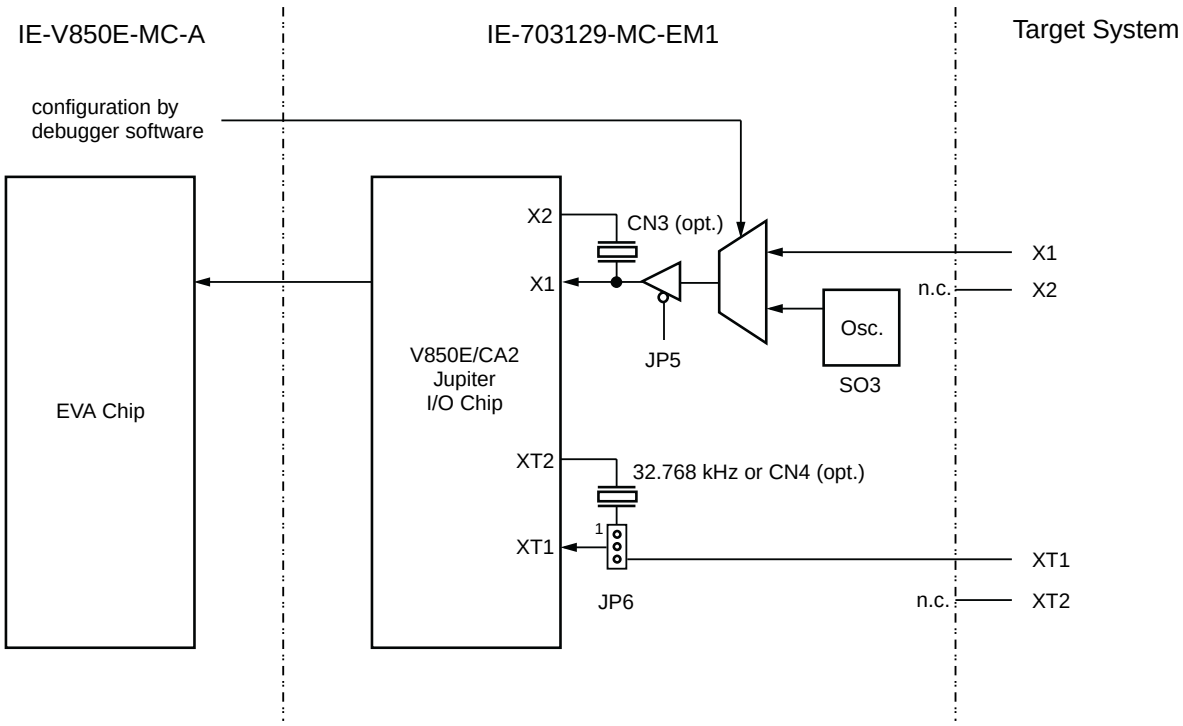
2.2 Clock Setting

2.2.1 Clock Structure

The main clock supply of IE-703129-MC-EM1 can be provided by an internal or external crystal oscillator (SO3) or an internal crystal/ceramic resonator (CN3). By default the IE-703129-MC-EM1 is equipped with a crystal oscillator on socket SO3 (4.000 MHz).

The sub-clock is usually connected to a 32.768 kHz crystal assembled on the IE-703129-MC-EM1. If a different crystal is to be used, it must be exchanged (CN4).

Figure 2-2: Clock Structure



2.2.2 Main clock setting

The following clock setting methods are available for main clock supply.

(1) Use the crystal oscillator mounted on SO3 of the IE-703129-MC-EM1 as internal clock (4.000 MHz).
(2) Change the crystal oscillator mounted on SO3 of the IE-703129-MC-EM1 and use it as the internal clock (permitted from 1.000 MHz to 5.000 MHz).
(3) Mount a crystal/ceramic resonator and capacitors on CN3 of the IE-703129-MC-EM1 and use it as the internal clock (permitted from 1.000 MHz to 5.000 MHz).
(4) Use a crystal oscillator target system as the external clock (clock input from target system).

Caution: When using an external clock, input the clock generated by the crystal oscillator to the X1 pin.

Table 2-7: Hardware Configuration for Main Clock Supply

Type of Clock	Clock Source Selection **Note 1**	SO3 Crystal/Ceramic Resonator	CN3 Crystal/Ceramic Resonator **Note 2**	JP5 Setting
(1) Crystal oscillator mounted on SO3 as internal clock	Internal	Factory setting (4.000 MHz)	Mounting prohibited	Open
(2) Customer specific crystal oscillator mounted on SO3 as the internal clock	Internal	Customer specific (1.000 to 5.000 MHz)	Mounting prohibited	Open
(3) Customer specific crystal/ceramic resonator and capacitors mounted on CN3 as internal clock	Internal	Crystal oscillator can either be removed or mounted	Customer specific (1.000 to 5.000 MHz)	Closed
(4) Crystal oscillator of the target system as the external clock (clock input from target system)	External	Crystal oscillator can either be removed or mounted	Mounting prohibited	Open

Notes: 1. Select the clock source when configuring the debugger (depends on the used debugger software).

2. A crystal/ceramic resonator must be applied close to the V850E/CA2 Jupiter I/O chip. Using a crystal/ceramic resonator on the target hardware is not possible.

2.2.3 Sub clock settings

The following clock setting methods are recommended for sub clock supply.

(1) Use the crystal (X2) mounted on the IE-703129-MC-EM1 (32.768 KHz).
(2) Use a crystal oscillator on the target system as the external clock (clock input from target system).

Caution: When using an external clock, input the clock generated by the crystal oscillator to the XT1 pin.

Table 2-8: Hardware Configuration for Sub Clock Supply

Type of Clock	CN4 Crystal/Ceramic Resonator	JP6 Setting
Crystal (X2) mounted on IE-703129-MC-EM1 (32.768 kHz)	Mounting prohibited	1-2
Crystal oscillator of the target system as the external clock (clock input from target system)	Mounting prohibited	2-3

2.3 Operation Mode

The IE-703129-MC-EM1 supports only the ROMless mode 1, similar to the V850E/CA2 Jupiter. For this the following mode setting has to be configured.

2.3.1 When emulator is used as stand-alone unit

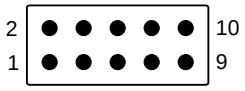
When using a debugger, be sure to set or select “Mode 1” in the debugger configuration. This configuration corresponds to ROM-less mode 1.
The mode pins MODE0, MODE1 and MODE2 are configured internally.

2.3.2 When emulator is connected to target system

When using a debugger, be sure to set or select “Mode 1” in the debugger configuration. This configuration corresponds to ROMless mode 1.
Emulation of the mode pins MODE0, MODE1 and MODE2 cannot be performed since the configuration is made internally by the debugger.
For settings of the mode pins refer to the **V850E/CA2 Jupiter Hardware User’s Manual**.

Chapter 3 Factory Settings

Table 3-1: Factory Settings

Item	Setting	Remark
JP1		Use internal 5 V for AV_{REF} by default.
JP2		Use internal 5 V for AV_{DD} by default.
JP3		Use internal GND for AV_{SS} by default.
JP4		Emulator operation is stand-alone by default.
JP5		Use crystal oscillator for main clock supply as default.
JP6		Use 32.768 KHz crystal mounted on IE-7031129-MC-EM1 for sub clock supply as default.
CN3		Connector for crystal/ceramic resonator for main clock supply is unpopulated by default.
CN5		Reserved
SO3	4.000-MHz crystal oscillator is mounted.	The main clock frequency can be changed by changing the crystal oscillator (1.000 MHz to 5.000 MHz)

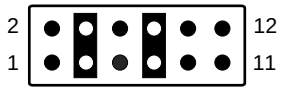
[MEMO]

Chapter 4 Cautions

4.1 Jumper Configuration of IE-V850E-MC-A

The configuration of jumper JP2 of the basic emulator board IE-V850E-MC-A has to be changed to the setting shown in Figure 4-1.

Figure 4-1: Configuration of IE-V850E-MC-A Jumper JP2



Caution: Setting the jumper JP2 of IE-V850E-MC-A to any other position will cause incorrect handling of interrupts.

4.2 Standby Release

In emulation mode the main clock oscillator is always running. Therefore, no oscillation stabilization time is required when stop mode or sub watch mode is released. As a consequence the emulator will wake up immediately from sub watch or stop mode while the target device always assures the oscillation stabilization time for main oscillator.

4.3 Pin Functions

4.3.1 MODE0 to MODE2 pins

When the emulator operates as a stand-alone unit, the operation mode of the emulator is ROM-less mode 1.
The MODE0 to MODE2 pins are connected as follows.

- MODE0: Connected to target connector (5.1 KΩ pull-up to +5 V on the IE-V850E-MC-A)
- MODE1: Connected to target connector (5.1 KΩ pull-up to +5 V on the IE-V850E-MC-A)
- MODE2: Connected to target connector (5.1 KΩ pull-up to +5 V on the IE-V850E-MC-A)

4.3.2 $\overline{\text{RESET}}$ input

The $\overline{\text{RESET}}$ input pin is connected to V_{DD} via a resistor (10 KΩ pull-up to +5 V). Therefore the behavior differs from the target device.

4.3.3 $\overline{\text{RESOUT}}$ output

The $\overline{\text{RESOUT}}$ output pin is driven by a CPLD. Driving capabilities and timing are different compared to the target device.

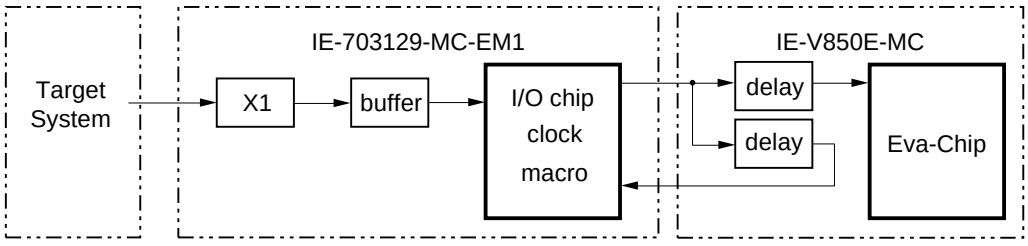
- Emulator: 24 mA via 100 Ω serial resistor
- Target device: 3 mA

4.3.4 Clock signals

(1) X1 signal

The input signal (X1 signal) from the target system is delayed because it passes through a buffer before it is input to the I/O chip of the emulator. Therefore the input characteristics may differ from the target device.

Figure 4-2: Diagram of X1 Signal Flow



(2) X2/XT2 signals

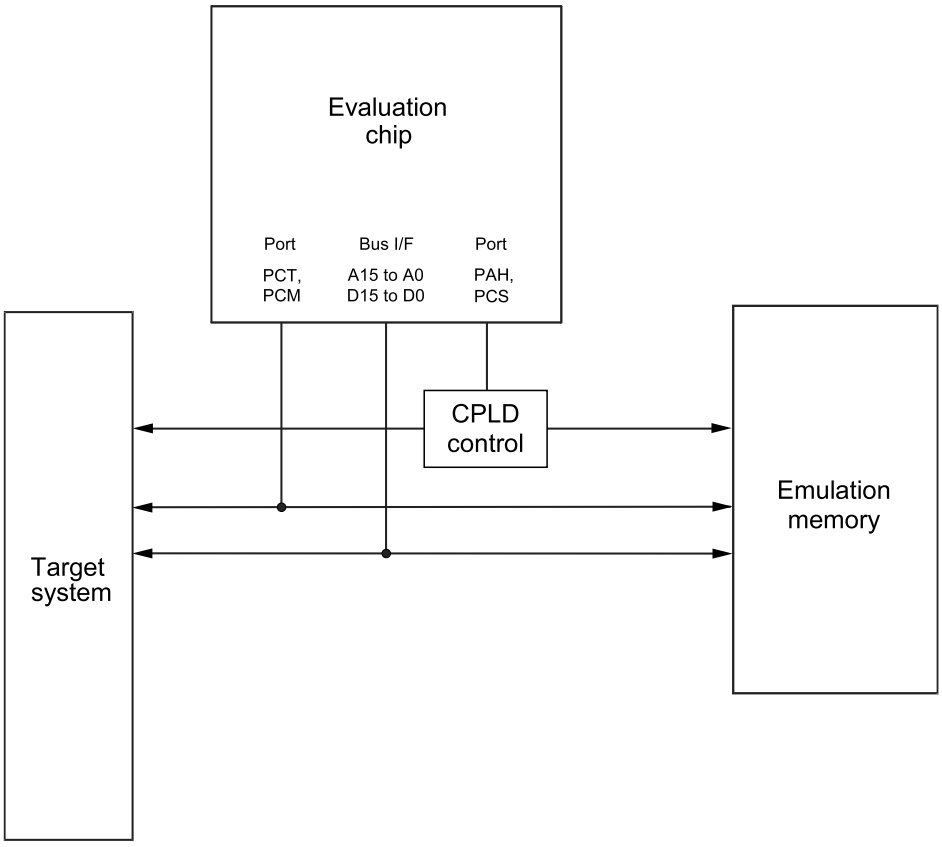
As crystal operation is not possible from target application, these lines are not connected.

4.3.5 Port pins

The ports PAH, PCS, PCT, and PCM, which are shared with the bus interface function, are not emulated by the I/O chip, but by the evaluation chip (refer to Figure 4-3).
Driving capabilities are different compared to the target device.

- Emulator: 6 mA
- Target device: 3 mA

Figure 4-3: Configuration of Ports PAH, PCS, PCT, and PCM



Emulation memory is connected to lines PCS4, PCS3, PCS0, PCT4, PCT1, and PCT0. This produces additional load.

4.3.6 Bus interface pins

(1) Behavior during break and program execution

The behavior of bus interface pins is shown in the following Table 4-1. This might be different to the target device (refer to **V850E/CA2 Jupiter Hardware User's Manual**).

Table 4-1: Bus Interface Pin Operation List

(a) During break

Pin Name	Waiting for Emulator Command	External Memory	
		Emulation RAM or Target System	
		R	W
A0 to A23	**Note**	**Note**	
D0 to D15	Hi-Z	**Note**	
$\overline{LWR}$ / $\overline{UWR}$	H	**Note**	
$\overline{RD}$	H	**Note**	
$\overline{CS0}$, $\overline{CS3}$, $\overline{CS4}$	H	**Note**	
$\overline{WAIT}$	Invalid	Maskable	

(b) During user program execution

Pin Name	External Memory		
	Emulation RAM or Target System		
	F	R	W
A0 to A23	**Note**		
D0 to D15	**Note**		
$\overline{LWR}$ / $\overline{UWR}$	**Note**		
$\overline{RD}$	**Note**		
$\overline{CS0}$, $\overline{CS3}$, $\overline{CS4}$	**Note**		
$\overline{WAIT}$	Maskable		

Note: Performs the same operation as the cycle that is generated by the target device program execution.

Remarks: 1. F : Instruction fetch
R : Read
W : Write

2. H : High-level output
Hi-Z : High-impedance

(2) Address lines A23 to A0

The address lines A15 to A0 and A23 to A16 (PAH7 to PAH0) have a different standby behaviour on the emulator compared to the target device.

Table 4-2: Standby Behavior of Address Lines A23 to A0/Port PAH

Port/ Bus interface	Target Device	Emulator	Remark
A15 to A0	Hold	Hi-Z	
A23 to A16	Hold	Hi-Z	Bus interface function of PAH
PAH7 to PAH0	Hold	Hold	Port mode of PAH

Driving capabilities are different compared to the target device.

- Emulator: 6 mA
- Target device: 3 mA

(3) Data lines D15 to D0

Since emulation memory is connected to the data lines D15 to D0, additional load has to be considered for the target system.
Driving capabilities are different compared to the target device.

- Emulator: 6 mA
- Target device: 3 mA

(4) Control lines $\overline{\text{RD}}$, $\overline{\text{LWR}}$, $\overline{\text{UWR}}$

Driving capabilities are different compared to the target device.

- Emulator: 6 mA
- Target device: 3 mA

(5) Chip select lines $\overline{\text{CS0}}$, $\overline{\text{CS3}}$, $\overline{\text{CS4}}$

All $\overline{\text{CSn}}$ signals can be used for selecting emulation memory or memory on a target system (n = 0, 3, 4). The definition is done by the emulation memory configuration with the CPLDCFG signals. As soon as an emulation memory block is assigned to a $\overline{\text{CSn}}$ signal, the signal is reserved for emulation memory and is not usable by a target system any more. In that case the target system will see a high-level (3.3 V) on that line. The level is generated by a CPLD and differs in the driver capability as follows.

- Emulator when $\overline{\text{CSn}}$ used for emulation memory: 3.3 V/ 24 mA via a 100 Ω serial resistor ($\overline{\text{CSn}}$ is fixed to high-level.)
- Emulator when $\overline{\text{CSn}}$ used for target system: 6 mA
- Target device: 3 mA

(6) $\overline{\text{WAIT}}$ input

When the emulator is in stand-alone mode (set by jumper JP4), the $\overline{\text{WAIT}}$ input is held to high-level (+3.3 V) via a 10 KΩ pull-up resistor.

4.3.7 Power supply voltage V_{DD5x}, V_{DD3x}

The emulator is supplied by its own power supply. Therefore the target voltage input at the target probe is only used as a sensing input, and the resulting power consumption may be less as it would be for the target device.
Nevertheless, when a target hardware is to be used (non stand-alone operation), the emulator needs to be connected to all power supply lines V_{DD5x}, V_{DD3x} as well as V_{SS5x}, V_{SS3x}.

4.3.8 Clock supply voltage CV_{DD}

The clock supply voltage input CV_{DD} behaves the same as the V_{DD3x} lines (ref. to **4.3.7 Power supply voltage VDD5x, VDD3x**). However, CV is not replicated by the emulator. Instead of this CV of I/O chip is derived from V_{DD}
Nevertheless, when a target hardware is to be used (non stand-alone operation), the emulator needs to be connected to the clock supply lines CV_{DD} and CV_{SS}.

4.3.9 AV_{DD}, AV_{REF}, AV_{SS} pins

Power supply of to these pins can be connected to the internally 5V power supply by jumpers JP1, JP2, and JP3 (factory setting). In that case resulting A/D converter values and load on AV_{DD}, AV_{REF}, AV_{SS} pins may differ.

4.4 Special Function Registers

4.4.1 Reset Source Monitor Flag

The reset source (external, or watchdog timer) cannot be distinguished by the RSM register of the clock controller during I/O emulation mode. Oscillation stabilization time is skipped after watchdog timer reset during sub watch mode.

4.4.2 Port (mode/ mode control) registers

(1) Unused register bits

Unused bits in the port mode control registers PMCCS, PMCCT and PMCCM are fixed to '1' in the emulator but fixed to '0' in the target device.

(2) Reset values

The reset values of the port mode registers PMAH, PMCS, PMCT and PMCS differ from the target device (ref. to Table 4-3).

Table 4-3: Differing Reset Values of Port (Mode/ Mode Control) Register

Register	Address	Reset Value		Remark
		Target Device	Emulator	
PAH	0x03FFF002	0x00	undefined	
PMAH	0x03FFF022	0x00	0xFF	Note 1
PMCS	0x03FFF028	0x18	0xFF	Note 1
PMCT	0x03FFF02A	0x03	0xFF/0x00	Note 2
PMCS	0x03FFF02C	0x01	0xFF	Note 1
PMCCT	0x03FFF04A	0x10	0x13	Note 2

Notes: 1. If necessary these registers can be set to their correct values within a start-up file (.rc or .mac) or within a user application.

2. Since the bus control lines $\overline{RD}$, $\overline{LWR}$, and $\overline{UWR}$ are required for emulation purpose, the alternative port function PCT0, PCT1, and PCT4 cannot be used. The reset values are set correspondingly.

(3) Port mode settings for bus interface function

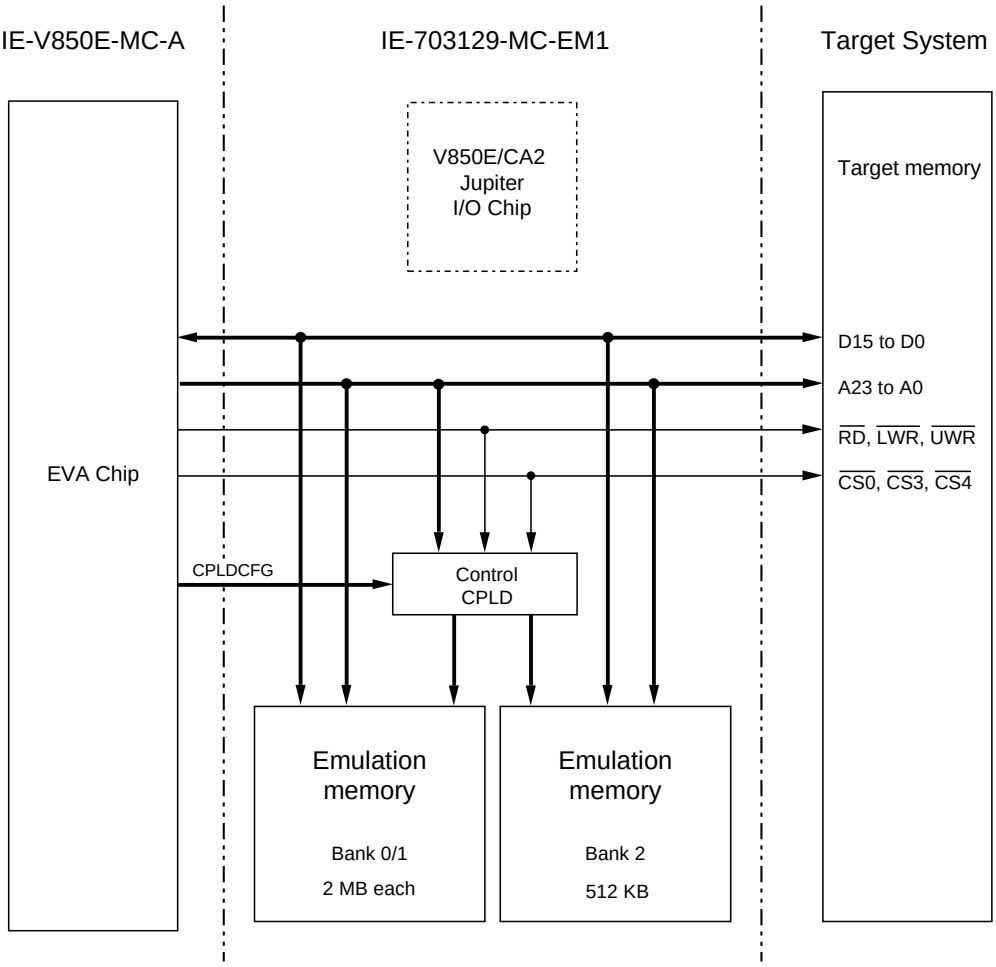
If using bus interface functions the required I/O mode setting for the respective port bit is not forced automatically in the target device. In fact the corresponding port mode bit has to be configured according to the bus interface function. For the emulator the port mode setting is not necessary if the bus interface function is enabled. Therefore, the bus interface function behaves different in the emulator and the target device.

(4) Read values of PAH port register

In the real-chip PAH port register bits are fixed to low level when read, if alternative address line output function of the corresponding port pin of PAH is used. In opposite to this the emulator shows the port register value when using the alternative function.
If the corresponding pin of PAH is used as general purpose I/O the input pin value or the port register output value is read. This is the same behaviour for real-chip and emulator.

4.5 Emulation Memory

Figure 4-4: Configuration of Emulation Memory



The emulation memory must be configured before downloading a program. For this a 16-bit port (CPLDCFG) is provided to setup the CPLD on the IE-703129-MC-EM1.The CPLDCFG port is mapped at address 0xfffff006, and is not available on the target device. For more details refer to **5.2 Start-up for Green Hills Multi 2000**, or **5.3 Start-up for V850 IAR Embedded Workbench** respectively.

Emulation memory is split into three banks: bank0 (1M x 16 or 1M x 8), bank1 (1 M x 16 or 1 M x 8) and bank2 (256 K x 16 or 256 K x 8).
Each bank can be connected to any of the three chip-select signals $\overline{CS0}$, $\overline{CS3}$, or $\overline{CS4}$, or it can be disabled. If more than one bank is connected to the same $\overline{CSn}$ line, the sizes add up to a larger memory (n = 0, 3, 4).
All banks can be write-protected independently (even, if they are associated with the same CS line).
Each bank can be configured to be used as 8-bit or 16-bit memory. If the 8-bit mode is used, half of the memory is left unused. All banks associated with the same $\overline{CSn}$ line must be configured to the same data width.
Any memory connected to the CS0 line must be configured to 16-bit data width.

Emulation memory must be accessed with at least one data wait state, which is specified in the data wait control register DWC0 for $\overline{CS0}$ and $\overline{CS3}$ areas, and in the data wait control register DWC1 for $\overline{CS4}$ area.

The address lines A23 to A16 can either be used as address lines or as port pins, depending on the amount of memory required. The address lines A22 to A16 must be configured by the CPLDCFG port to set them up as address lines or port pins. Address line A23/PAH7 is not used for emulation memory and does not need to be set up by the CPLDCFG port.

When using emulation memory, the following lines must be configured to BCU mode:

D15 to D0
A15 to A0
any of the used A22 to A16
$\overline{RD}$, $\overline{LWR}$, $\overline{UWR}$
any of the required $\overline{CSn}$ signals (n = 0, 3, 4)

Caution: A target hardware may possibly work without some of the above lines using a sophisticated circuitry. The EM1 board however does not support this. If emulation memory is used, the above lines are mandatory.

Table 4-4: Function of configuration lines CPLDCFG15 to CPLDCFG0

Port	Source
CPLDCFG15	Reserved (1)
CPLDCFG14	Used to clock in the configuration data
CPLDCFG13, CPLDCFG12	Reserved (1)
On falling edge of CPLDCFG14:	
CPLDCFG11	Selects whether bank 2 is accessed in 8-bit mode (1) or 16-bit mode (0)
CPLDCFG10	Selects whether bank 2 is write-protected (1) or not (0)
CPLDCFG9, CPLDCFG8	Selects the CS line to which bank 2 belongs to (00B = CS0, 01B = CS3, 10B = CS4, 11B= disabled)
CPLDCFG7	Selects whether bank 1 is accessed in 8-bit mode (1) or 16-bit mode (0)
CPLDCFG6	Selects whether bank 1 is write-protected (1) or not (0)
CPLDCFG5, CPLDCFG4	Selects the CS line to which bank 1 belongs to (00B = CS0, 01B = CS3, 10B = CS4, 11B= disabled))
CPLDCFG3	Selects whether bank 0 is accessed in 8-bit mode (1) or 16-bit mode (0)
CPLDCFG2	Selects whether bank 0 is write-protected (1) or not (0)
CPLDCFG1, CPLDCFG0	Selects the CS line to which bank 0 belongs to (00B = CS0, 01B = CS3, 10B = CS4, 11B= disabled)
On rising edge of CPLDCFG14:	
CPLDCFG11 to CPLDCFG7	Reserved (0)
CPLDCFG6 to CPLDCFG0	Selects whether A22 to A16 (PAH6 to PAH0) is a port pin (1) or an address line (0)

4.6 Emulated Function Blocks

The IE-703129-MC-EM1 emulator option board is based on a target device, the V850E/CA2 Jupiter I/O chip. The following table shows the functions, which are not or not complete emulated by the I/O chip itself. For these functions a deviation between target device and emulator behavior might be possible.

Table 4-5: Functions Emulated by Other Hardware than Real-chip

Emulation	Function
Eva Chip D703191	Bus interface ports (PAH, PAL, PDL, PCS, PCT, PCM)
Eva Chip D703191	External memory interface
Eva Chip D703191	CPU
Eva Chip D703191	IRAM
Eva Chip D703191	iCache
Eva Chip D703191	INTC (Interrupt controller)
Eva Chip D703191	DMA controller
Eva Chip D703191	Reset
Eva Chip D703191	Mode pins

4.7 Extension Probe

For best signal quality use the emulator without an extension probe if possible. When necessary use the SWEX-144SD extension probe. Do not use more than one extension probe in serial.

Chapter 5 Debugger Operation

5.1 Operation of FCAN Interface

The FCAN address space is mapped in the external target memory area and therefore must be configured in the .rc-file, when using Green Hills Multi 2000, or the Hardware Setup dialog box, when using V850 IAR Embedded Workbench. For more details how to set up the address mapping refer to **4.4.1 Reset Source Monitor Flag**.

5.2 Start-up for Green Hills Multi 2000

The start-up procedure differs from typical emulator operation, as the emulation memory is mapped as target memory, it has to be configured before usage. A sample .rc-file is shown in Figure 5-1.

Figure 5-1: Sample .rc file for Green Hills Multi 2000 (1/3)

```
//
//  Sample.rc
//
//  Start-up file for Jupiter EM1 test program
//  (C) Copyright by NEC Electronics (Europe) GmbH
//
//  Revisions:
//  02/02/05  ME Initial.
//
//
************************************************************************

// connect to target
remote 850eserv

// reset cpu (and emulator/trace)
target reset a

// Jupiter has 0kB ROM and 16kB RAM
target cpu r=0 a=28
target mode romless16
target reset

// clock: int/ext
target clock int

// unmask/mask target pins (r=reset, n=nmi, w=wait, h=hldrq, s=hwstop,
// e=emwait)
target pinmask k
target pinmask w h s e
```

Figure 5-1: Sample .rc file for Green Hills Multi 2000 (2/3)

```
// set SFR values of alpha-ports (due to difference to real-chip)
target SFR PMCCT= 0x13 // different to real-chip (0x10)
target SFR PMAH = 0x00
target SFR PMCS = 0x18
target SFR PMCT = 0x00 // different to real-chip (0x03)
target SFR PMCM = 0x01
target SFR PAH = 0x00
target SFR PCS = 0x00
target SFR PCT = 0x00
target SFR PCM = 0x00

//** This next section configures the EM1 board to match the target
//** hardware
//** memory configuration. This configuration may only be done once, as all
//** data represents physical connections, that can not be changed at
//** run-time. The used registers ARE NOT DEVICE REGISTERS. They merely
//** configure the EM1.


// CPLDCFG_FCT
target m h c 0xfffff046
target 0x0000
target.
// CPLDCFG_DIR
target m h c 0xfffff026
target 0x0000
target.

// bits 15, 13, 12: always 1

// 1: all RAMs on CS0, 16bit, r/w
// on falling edge of bit 14:
//
// bit 01-00: selects which CS RAM0 (2MB)   belongs to (00=CS0, 01=CS3,
// 10=CS4, 11=disabled)
// bit 02 : selects whether RAM0 (2MB)   is write-protected (1) or not (0)
// bit 03 : selects whether RAM0 (2MB)   is accessed in 8-bit mode (1) or
// 16-bit mode (0)
//
// bit 05-04: selects which CS RAM1 (2MB)   belongs to (00=CS0, 01=CS3,
// 10=CS4, 11=disabled)
// bit 06 : selects whether RAM1 (2MB)   is write-protected (1) or not (0)
// bit 07 : selects whether RAM1 (2MB)   is accessed in 8-bit mode (1) or
// 16-bit mode (0)
//
// bit 09-08: selects which CS RAM2 (512kB) belongs to (00=CS0, 01=CS3,
// 10=CS4, 11=disabled)
// bit 10 : selects whether RAM2 (512kB) is write-protected (1) or not (0)
// bit 11 : selects whether RAM2 (512kB) is accessed in 8-bit mode (1) or
// 16-bit mode (0)
target m h c 0xfffff006
target 0xf000
target.
target m h c 0xfffff006
target 0xb000
target.
```

Figure 5-1: Sample .rc file for Green Hills Multi 2000 (3/3)

```
// 2: all AHs as address lines
// on rising edge of bit 14:
// bit 06-00: selects whether A[22:16] (=PAH[6:0]) is a port pin (1) or
// an address line (0)
// bit 11-07: reserved (0)
target m h c 0xfffff006
target 0xb000
target.
target m h c 0xfffff006
target 0xf000
target.

// map memory (user: 4.5MB to CS0)
target map u=0x0000000,0x00fffff
target map u=0x0100000,0x01fffff
target map u=0x0200000,0x02fffff
target map u=0x0300000,0x03fffff
target map u=0x0400000,0x04fffff
// FCAN area:
target map u=0x1800000,0x18fffff

// configure CS
target SFR CSC0 = 0x2007

// load program to memory
load

// reset CSC to default value
target SFR CSC0 = 0x2c11


// display opcodes in ASM view
_OPCODE = 1
_ASMCACHE = 0

// setup GUI
button Reset target reset
button Trace tracewin

// indicate success
"\r\n"
"--------------------\r\n"
"Initialization done.\r\n"
"\r\n"

//************************************************************** EOF
```

5.3 Start-up for V850 IAR Embedded Workbench

The start-up procedure differs from typical emulator operation, as the emulation memory is mapped as target memory. It has to be configured in the Hardware Setup Dialog before usage. When starting the debugger the emulator has to be initialized first by a C-SPY setup macro. A sample setup macro file is shown in Figure 5-2.

Figure 5-2: Sample C-Spy Setup Macro File for V850 IAR Embedded Workbench) (1/3)

```
//
//  sample.mac
//
//  Sample start-up file for Jupiter EM1
//  (C) Copyright by NEC Electronics (Europe) GmbH
//
//  Revisions:
//  2002/06/11 ME Initial.
//
//  Note:
//  The skeleton may and should remain unchanged. To adapt the EM1 to the
//  target application only the four lines in the bounded section should
//  be changed.
//
//
*******************************************************************************

execUserPreload()
 {
 __message "execUserPreload: Init Jupiter EM1 board\n";
  configureEM1();
 }

execUserSetup(){ configureEM1(); }
execUserReset(){ configureEM1(); }


configureEM1()
 {
  // This next section configures the EM1 board to match the target
  // hardware
  // memory configuration. This configuration may only be done once, as all
  // data represents physical connections, that can not be changed at
  // run-time. The used registers ARE NOT DEVICE REGISTERS. They merely
  // configure the EM1.

  __var RAM0, RAM1, RAM2, PAHPINS_AS_PORT;
  __var CS0, CS3, CS4, DISABLED, READWRITE, WRITEPROTECTED, WIDTH16BIT,
    WIDTH8BIT;
  __var config1, config2, b11, b12, b13, b21, b22, b23;

  CS0      = 0x00;
  CS3      = 0x01;
  CS4      = 0x02;
  DISABLED = 0x03;
```

Figure 5-2: Sample C-Spy Setup Macro File for V850 IAR Embedded Workbench) (2/3)

```
 READWRITE         = 0x00;
  WRITEPROTECTED   = 0x04;

  WIDTH16BIT= 0x00;
  WIDTH8BIT = 0x08;

  // ************************************************************************
  // *** User application dependent section (begin)
  // ************************************************************************


  RAM0 = CS0 | READWRITE | WIDTH16BIT;   // 2MB
  RAM1 = CS0 | READWRITE | WIDTH16BIT;   // 2MB
  RAM2 = CS0 | READWRITE | WIDTH16BIT;   // 512kB
  PAHPINS_AS_PORT = 0x70;   // A[22:16]=PAH[6:0]: 1=portpin; 0=addressline


  // ************************************************************************
  // *** User application dependent section (end)
  // ************************************************************************


  config1 = ( ( RAM0 & 0x0f ) << 0 ) | ( ( RAM1 & 0x0f ) << 4 ) |
            ( ( RAM2 & 0x0f ) << 8 ) | 0xb000; // bit14 falling edge config

  config2 = ( PAHPINS_AS_PORT & 0x7f) | 0xb000; // bit14 rising edge config

  b11 = (config1 & 0x00ff );
  b12 = (config1 & 0xff00 | 0x4000 ) >> 8;
  b13 = (config1 & 0xff00 & 0xbfff ) >> 8;

  b21 = (config2 & 0x00ff );
  b22 = (config2 & 0xff00 & 0xbfff ) >> 8;
  b23 = (config2 & 0xff00 | 0x4000 ) >> 8;

  // CPLDCFG_FCT
  __writeMemoryByte( 0x00, 0xfffff046, "Memory" );
  __writeMemoryByte( 0x00, 0xfffff047, "Memory" );
  // CPLDCFG_DIR
  __writeMemoryByte( 0x00, 0xfffff026, "Memory" );
  __writeMemoryByte( 0x00, 0xfffff027, "Memory" );
  // CPLDCFG falling edge
  __writeMemoryByte( b11,  0xfffff006, "Memory" );
  __writeMemoryByte( b12,  0xfffff007, "Memory" );
  __writeMemoryByte( b13,  0xfffff007, "Memory" );
  // CPLDCFG rising  edge
  __writeMemoryByte( b21,  0xfffff006, "Memory" );
  __writeMemoryByte( b22,  0xfffff007, "Memory" );
  __writeMemoryByte( b23,  0xfffff007, "Memory" );


  // set SFR values of alpha-ports (due to difference to real-chip)
  __writeMemoryByte( 0x13, 0xfffff04a, "Memory" );  // PMCCT= 0x13
[different to real-chip (0x10)]
  __writeMemoryByte( 0x00, 0xfffff022, "Memory" );  // PMAH = 0x00
```

Figure 5-2: Sample C-Spy Setup Macro File for V850 IAR Embedded Workbench) (3/3)

```
  __writeMemoryByte( 0x18, 0xfffff028, "Memory" );  // PMCS = 0x18
  __writeMemoryByte( 0x00, 0xfffff02a, "Memory" );  // PMCT = 0x00
[different to real-chip (0x03)]
  __writeMemoryByte( 0x01, 0xfffff02c, "Memory" );  // PMCM = 0x01
  __writeMemoryByte( 0x00, 0xfffff002, "Memory" );  // PAH  = 0x00
  __writeMemoryByte( 0x00, 0xfffff008, "Memory" );  // PCS  = 0x00
  __writeMemoryByte( 0x00, 0xfffff00a, "Memory" );  // PCT  = 0x00
  __writeMemoryByte( 0x00, 0xfffff00c, "Memory" );  // PCM  = 0x00
 }
```

Chapter 6 Limitations

6.1 Emulation Memory

Emulation memory size is limited to 4.5 MB.
Emulation memory must be selected by a $\overline{CSn}$ line (n = 0, 3, 4). That $\overline{CSn}$ line cannot be used for the target application.
Additional memory can be connected as target memory.

6.2 Bus Interface Control Pins

Any of the signals $\overline{RD}$, $\overline{LWR}$, $\overline{UWR}$ as well as the used $\overline{CSn}$ lines (n = 0, 3, 4) must be configured as control line for the emulator to work. These lines cannot be used as port pins.

6.3 External Flash Programming

External flash programming via FlashMaster is not supported.

6.4 In-circuit Emulator IE-V850E-MC-A

The in-circuit emulator option board IE-703129-MC-EM1 should be operated only with an in-circuit emulator IE-V850E-MC-A, control code “G” or following.

6.5 Software Development Tools

For correct operation in conjunction with the instruction cache it is mandatory to use the latest version of the following files with the development/debugging tools.

6.5.1 Green Hills Multi 2000

- ex85032.dll version 5.60 or higher
- 850eserv.exe version 2.000 or higher

6.5.2 V850 IAR Embedded Workbench

- ex85032.dll version 5.60 or higher

[MEMO]

Appendix A Package Drawings

Figure A-1: IE-V850E-MC + IE-703129-MC-EM1 (Unit: mm)

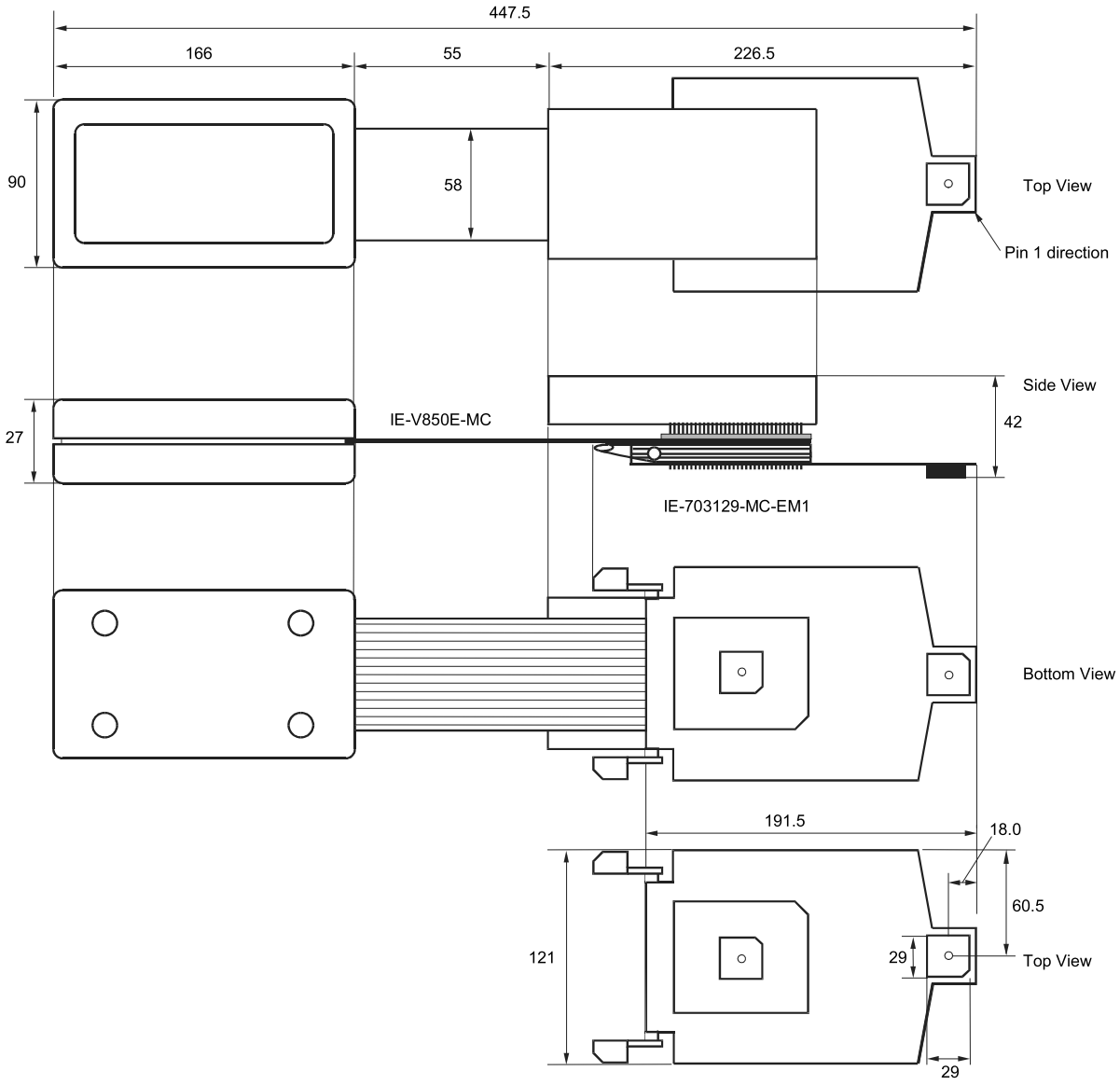


Figure A-2: SWEX-144SD-1 (Unit: mm)

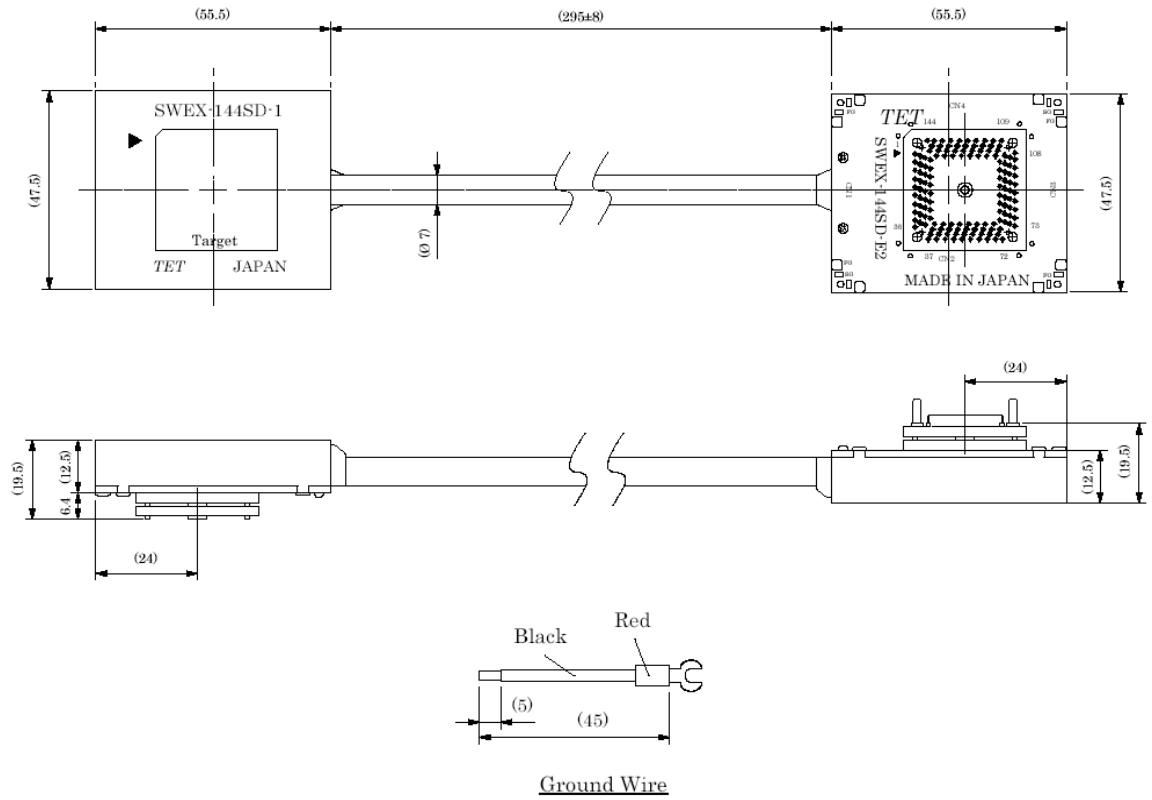
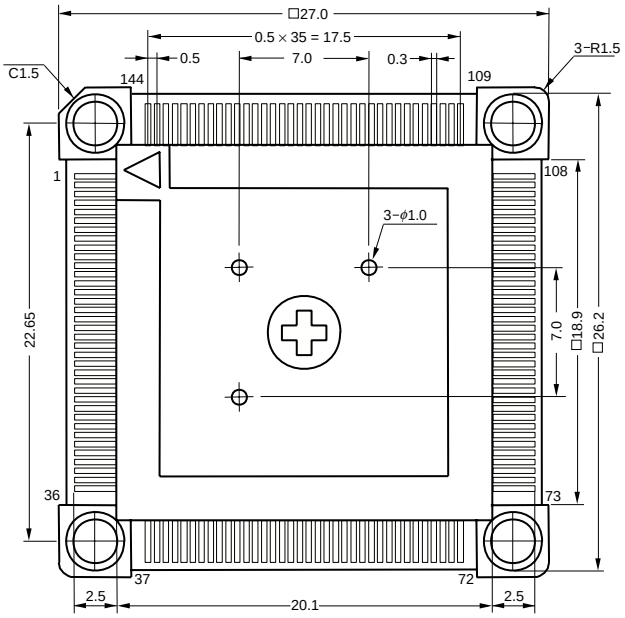
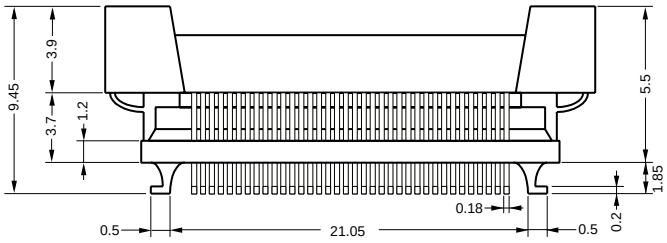


Figure A-3: NQPACK144SD (Unit: mm)

[Top view]



[Side view]



[Bottom view]

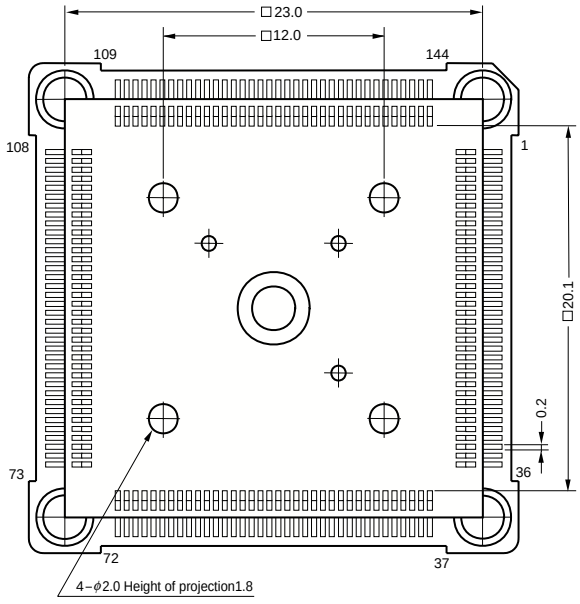
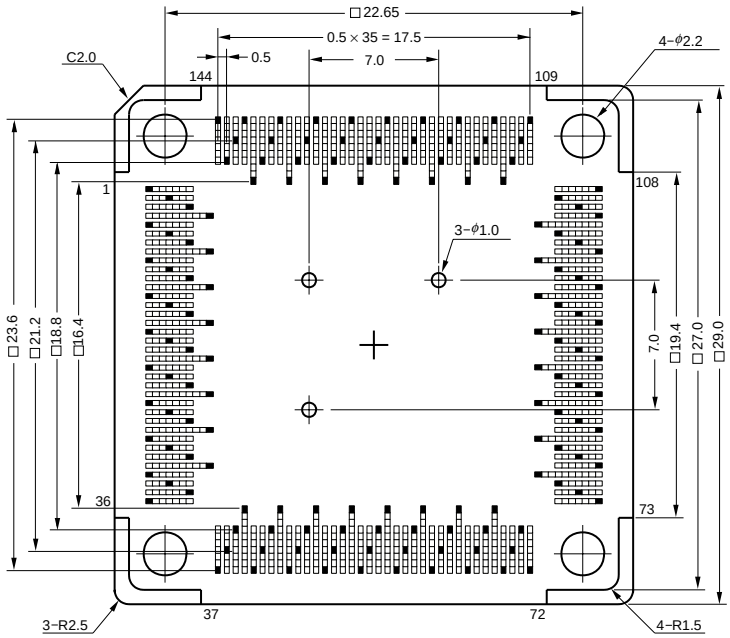
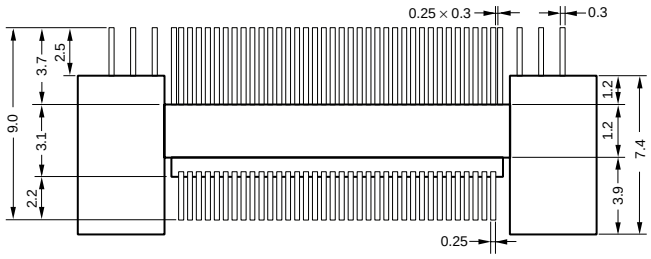


Figure A-4: YQPACK144SD (Unit: mm)

[Top view]



[Side view]



[Bottom view]

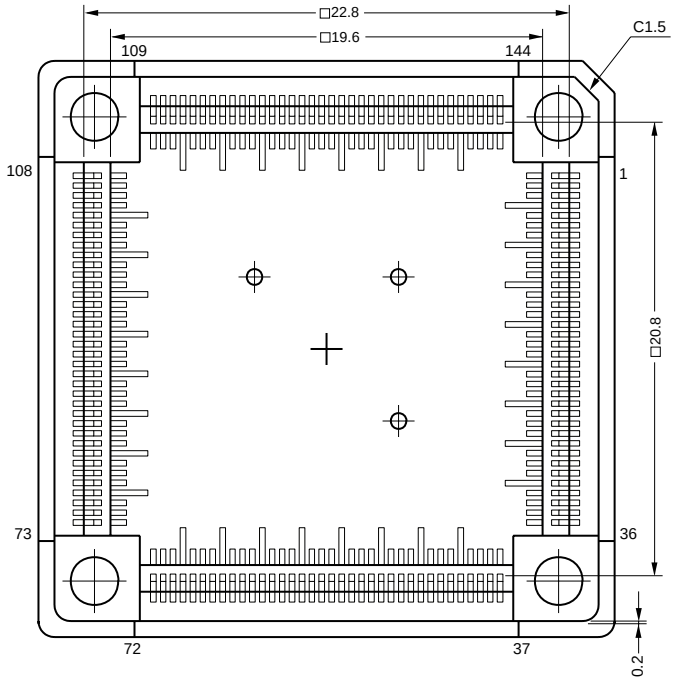
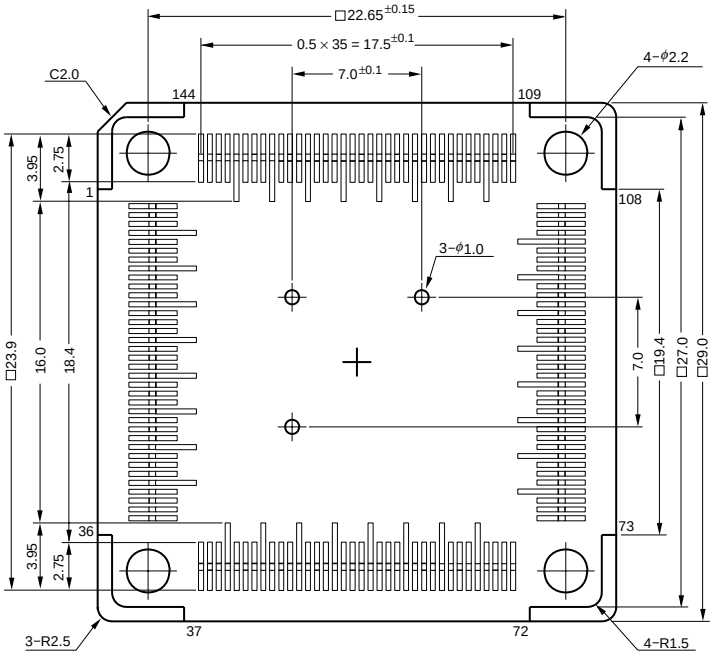
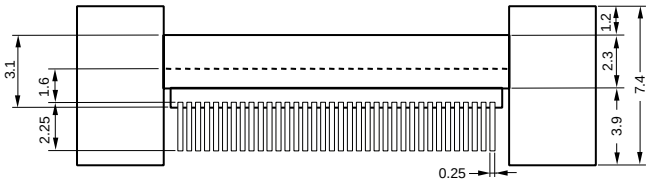


Figure A-5: HQPACK144SD (Unit: mm)

[Top view]



[Side view]



[Bottom view]

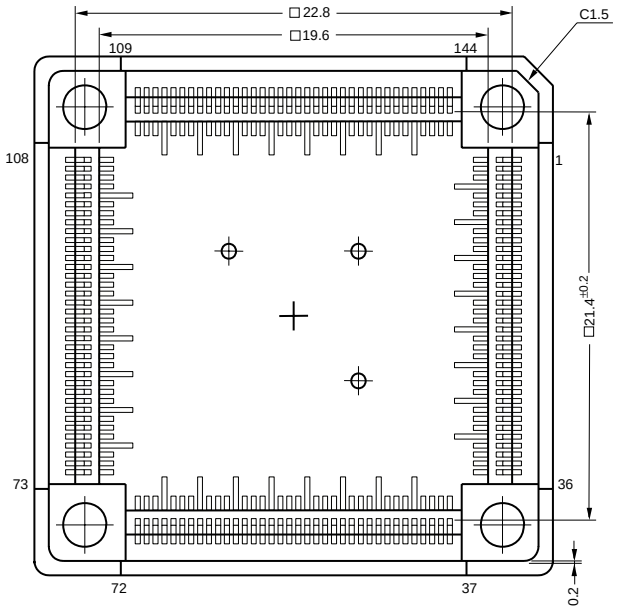
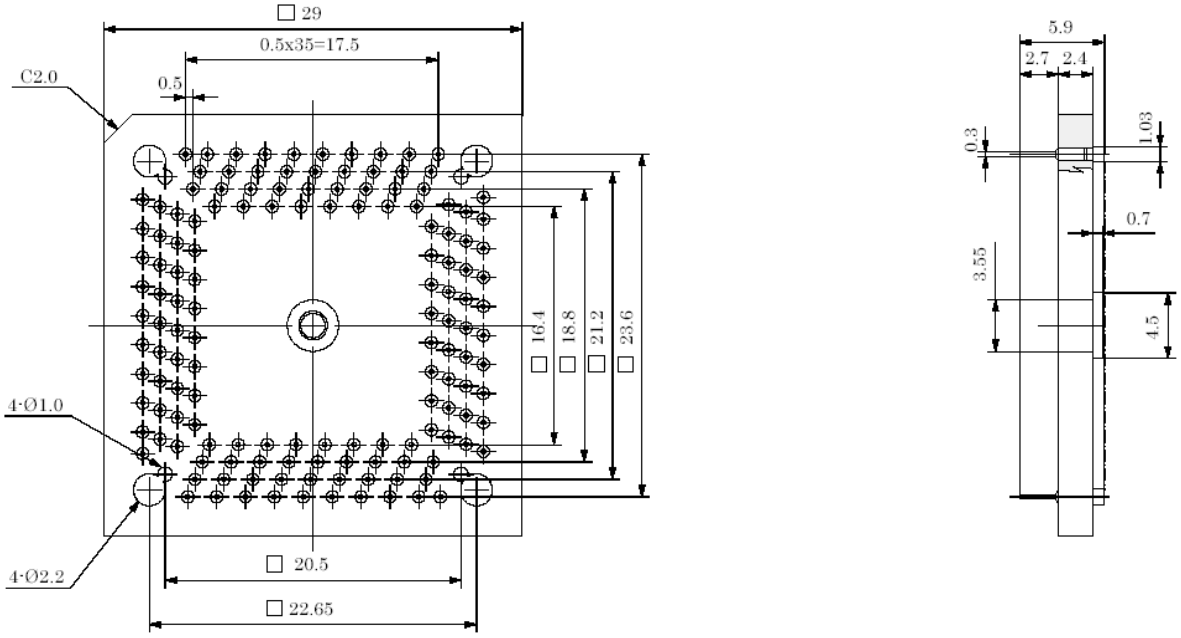


Figure A-6: YQSOCKET144DN (Unit: mm)



Appendix B Example of Use of Connector for Target Connection

Figure B-1: When directly connecting device to target system (Connector for target connection is not used)

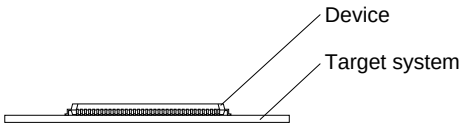


Figure B-2: When equipping device by using connector for target connection

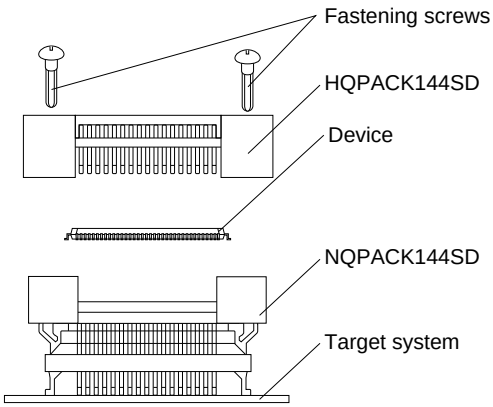
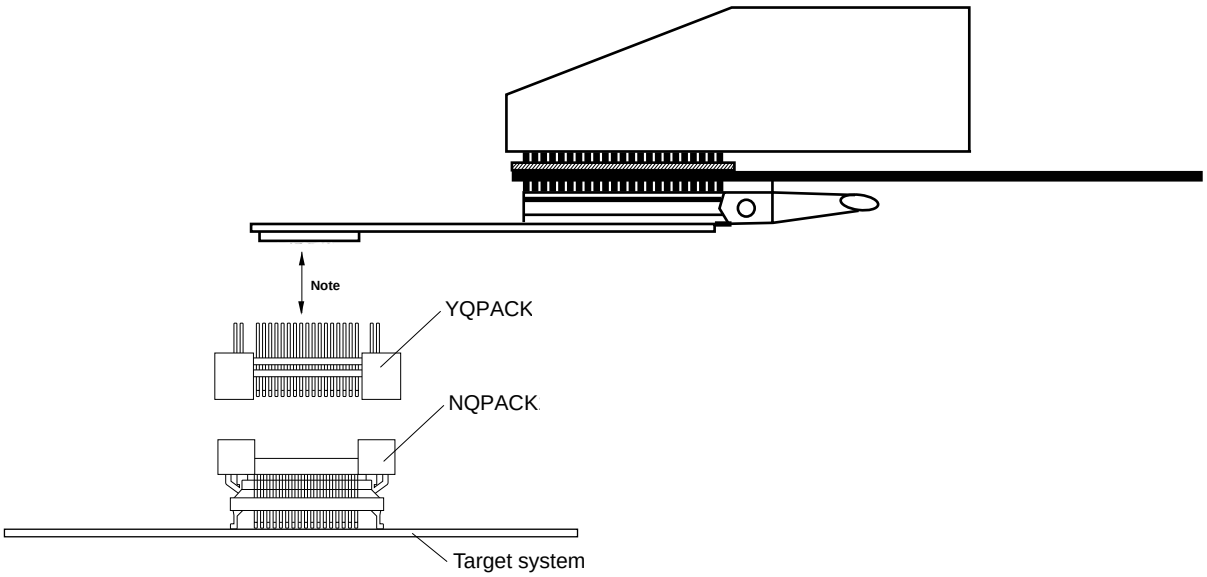


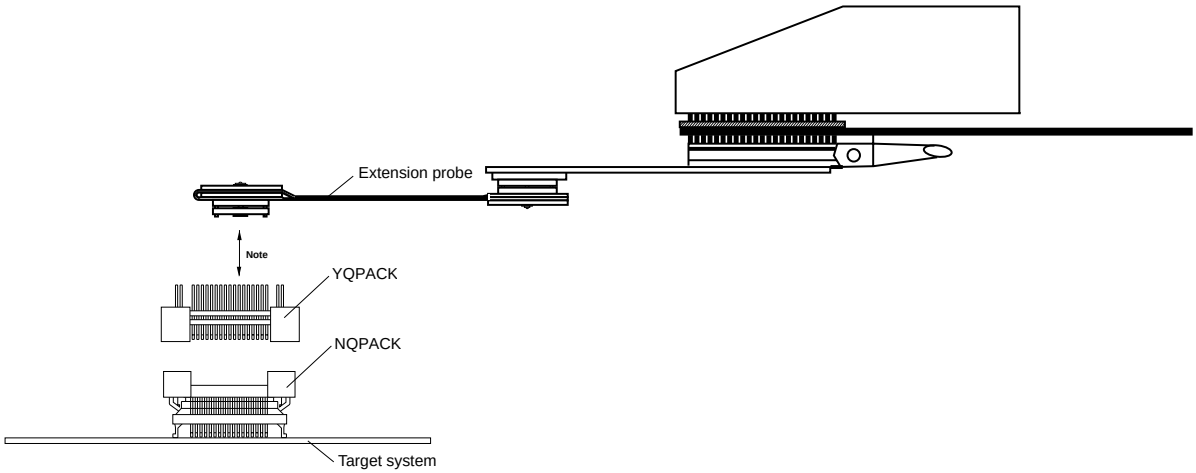
Figure B-3: Connection between emulator and target system

(a) When extension probe is not used



Note: Connector for emulator connection (YQSOCKET144SDN) can be inserted at this position for height adjustment.

(b) Example of use of extension probe



Note: Connector for emulator connection (YQSOCKET144SDN) can be inserted at this position for height adjustment.

Appendix C Connectors for Target Connection

C.1 Use

(1) When mounting NQPACK144SD to target system

<1> Coat the tip of four projections (points) at the bottom of the NQPACK144SD with two-component type epoxy adhesive (cure time longer than 30 min.) and bond the NQPACK144SD to the target system. If not bonded properly, the pad of the printed circuit board may peel off when the emulator is removed from the target system. If the lead of the NQPACK144SD does not coincide with the pad of the target system easily, perform step <2> to adjust the position.

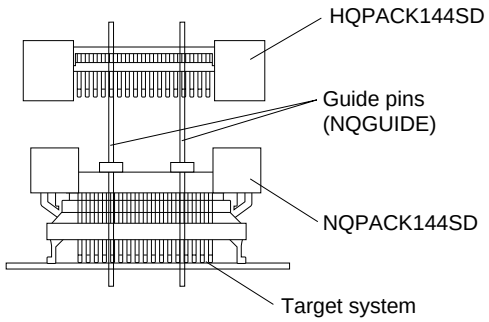
<2> To adjust the position, insert the guide pins for position-adjustment (NQGUIDE) provided with NQPACK144SD into the pin holes at the upper side of NQPACK144SD (refer to **Figure C-1**).
The diameter of a hole is ϕ = 1.0 mm. There are three non-through holes (refer to **APPENDIX A DIMENSIONS**).

<3> After setting the HQPACK144SD, solder NQPACK144SD to the target system. By following this sequence, adherence of flux or solder sputtering to contact pins of the NQPACK144SD can be avoided.

- Recommended soldering condition…Reflow : 240°C, 20 sec. max.
  Partial heating : 240°C, 10 sec. max. (per pin row)

<4> Remove the guide pins.

Figure C-1: Mounting of NQPACK144SD



Remark: NQPACK144SD: Connector for target connection
HQPACK144SD: Cover for device installation

(2) When setting device

Caution: Check for abnormal conditions such as resin burr or bent pins before setting a device to the NQPACK144SD. Moreover, check that the hold pins of the HQPACK144SD are not broken or bent before setting HQPACK144SD. If there are broken or bent pins, fix them with a thin, flat plate such as a blade.

<1> Make sure that the NQPACK144SD is clean and the device pins are parallel (flat) before setting a device to the NQPACK144SD. Then, after mounting the NQPACK144SD to the target board, set the device and HQPACK144SD (refer to **Figure C-2**).

<2> Using the screws provided with the HQPACK144SD (four locations: M2 × 6 mm), secure the HQPACK144SD, device, and NQPACK144SD.
Tighten the screws in a crisscross pattern with the provided screwdriver or driver with torque gauge (avoid tightening strongly only one screw). Tighten the screws with 0.55 kg·f·cm (0.054 N·m) max. torque. Excessive tightening may diminish conductivity.
At this time, each pin is fixed inside the plastic wall dividers by the contact pin of the NQPACK144SD and the hold pin of the HQPACK144SD (refer to **Figure C-3**). Thus, pins cannot cause a short with pins of neighboring devices.

Figure C-2: Mounting Device

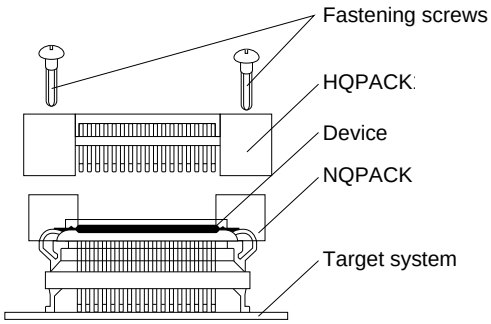
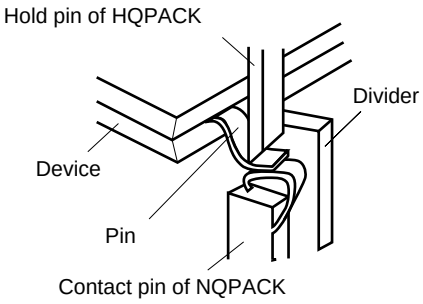


Figure C-3: NQPACK144SD and Device Pin



C.2 Cautions on Handling Connectors

(1) When taking connectors out of the case, remove the sponge while holding the main unit.

(2) When soldering the NQPACK144SD to the target system, cover the HQPACK144SD to protect it against splashing flux.

- Recommended soldering conditions Reflow : 240°C, 20 sec. max.
  Partial heating : 240°C, 10 sec. max. (per pin row)

(3) Check for abnormal conditions such as resin burr or bent pins before setting a device to the NQPACK144SD. Moreover, check that the hold pins of the HQPACK144SD are not broken or bent before setting HQPACK144SD. If there are broken or bent pins, fix them with a thin, flat plate such as a blade.

(4) When securing the YQPACK144SD (connector for emulator connection) or HQPACK144SD to the NQPACK144SD with screws, tighten the four screws temporarily with the provided screwdriver or driver with torque gauge, then tighten the screws in a crisscross pattern (with 0.054 N·m max. torque).
Excessive tightening of only one screw may diminish conductivity.
If the conductivity is diminished after screw-tightening, stop tightening, remove the screws and check whether the NQPACK144SD is stained and make sure the device pins are parallel.

(5) Device pins do not have high strength. Repeatedly connecting to the NQPACK144SD may cause pins to bend. When setting a device to the NQPACK144SD, check and adjust bent pins.

[MEMO]

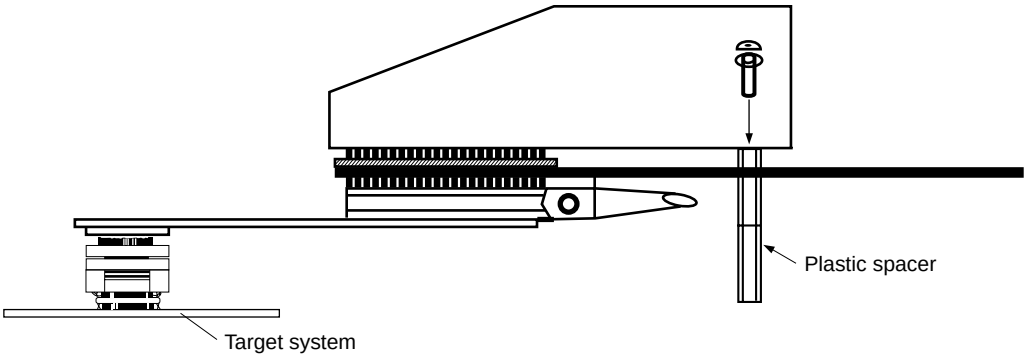
Appendix D Mounting of Plastic Spacer

This chapter describes the mounting method for the plastic spacer supplied with the IE-V850E-MC-A. When using the emulator connected to the target system, mount the plastic spacer as shown in Figure D-1 to fix the pod horizontally.

(1) Mounting IE-V850E-MC-A to plastic spacer

<1> Remove the nylon rivet from the rear part of the pod.
<2> Tighten the plastic spacer with the supplied plastic screw.
<3> To adjust the height, use a user spacer or stand.

Figure D-1: Mounting Method of Plastic Spacer



[MEMO]

Appendix E Revision History

Item	Date published	Document No.	Comment
1	September 2002	U16262EE3V0UM00	Correction of the subclock crystal frequency to 32.768 KHz on page 24 and page 27.
2			Removing of former chapter 4.4.1 “Programmable Peripheral Area (FCAN Interface)” on page 37.
3			Addition of chapter 6.4 “In-circuit Emulator IE-V850E-MC-A” on page 47.
4			Addition of chapter 6.5 “Software Development Tools” on page 47.

[MEMO]

NEC

Facsimile Message

From:

Name

Company

Tel. FAX

Address

Although NEC has taken all possible steps to ensure that the documentation supplied to our customers is complete, bug free and up-to-date, we readily accept that errors may occur. Despite all the care and precautions we've taken, you may encounter problems in the documentation. Please complete this form whenever you'd like to report errors or suggest improvements to us.

Thank you for your kind support.

North America
NEC Electronics Inc.
Corporate Communications Dept.
Fax: +1-800-729-9288
+1-408-588-6130

Europe
NEC Electronics (Europe) GmbH
Market Communication Dept.
Fax: +49-211-6503-274

South America
NEC do Brasil S.A.
Fax: +55-11-6462-6829

Hong Kong, Philippines, Oceania
NEC Electronics Hong Kong Ltd.
Fax: +852-2886-9022/9044

Korea
NEC Electronics Hong Kong Ltd.
Seoul Branch
Fax: +82-2-528-4411

Taiwan
NEC Electronics Taiwan Ltd.
Fax: +886-2-2719-5951

Asian Nations except Philippines
NEC Electronics Singapore Pte. Ltd.
Fax: +65-250-3583

Japan
NEC Semiconductor Technical Hotline
Fax: +81- 44-435-9608

I would like to report the following error/make the following suggestion:

Document title: _____

Document number: _____ Page number: _____

If possible, please fax the referenced page or drawing.

Document Rating	Excellent	Good	Acceptable	Poor
Clarity	☐	☐	☐	☐
Technical Accuracy	☐	☐	☐	☐
Organization	☐	☐	☐	☐