

# ISL91211AII-EV1Z

## User's Manual: Evaluation Board

### Core Power Solutions

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## ISL91211AII-EV1Z

### Evaluation Board

The ISL91211AII-EV1Z platform allows quick evaluation of the high performance features of the [ISL91211A](#) multi-output PMIC, that has four controllers capable of configuring its power stages for 2+1+1 channel outputs. Each channel can deliver up to 5A continuous output current per phase. The ISL91211A uses the Renesas proprietary R5 modulator technology to maintain accurate voltage regulation, while providing excellent efficiency and transient response. It also supports the standard I<sup>2</sup>C and SPI communication protocols, ideal for systems using a single-cell battery.

### Key Features

- Small, compact design
- Supports both I<sup>2</sup>C and SPI bus communication protocols
- Adjustable V<sub>OUT</sub> and independent DVS control for all three channels
- Real-time fault protection and monitor (OC, UV, OV, OT)
- Six-layer board design optimized for thermal performance and efficiency
- Connectors, test points, and jumpers for easy measurements
- Built-in load transient circuits for each output channel

### Specifications

The board is designed to operate at the following operating conditions:

- Input voltage rating from 2.5V to 5.5V
- Programmable output voltage range of 0.3V to 2V  
**Note:** Output range of 2V can be supported ONLY by factory OTP when requesting samples, not available with the standard ISL91211A.
- 2+1+1 configuration with 5A maximum load current/phase
- 4MHz switching frequency
- Default DVS slew rate of 3mV/μs
- Power-up sequence: VOUT1→VOUT2→VOUT3, 1ms delay between each rail
- Power-down sequence: SW1-3 power down at the same time
- Operating temperature range: -40°C to +85°C
- VOUT1, 2, and 3 = 0.9V

### Ordering Information

Part Number	Description
ISL91211AII-EV1Z	Evaluation board

### Related Literature

For a full list of related documents, visit our website:

- [ISL91211A](#) device page

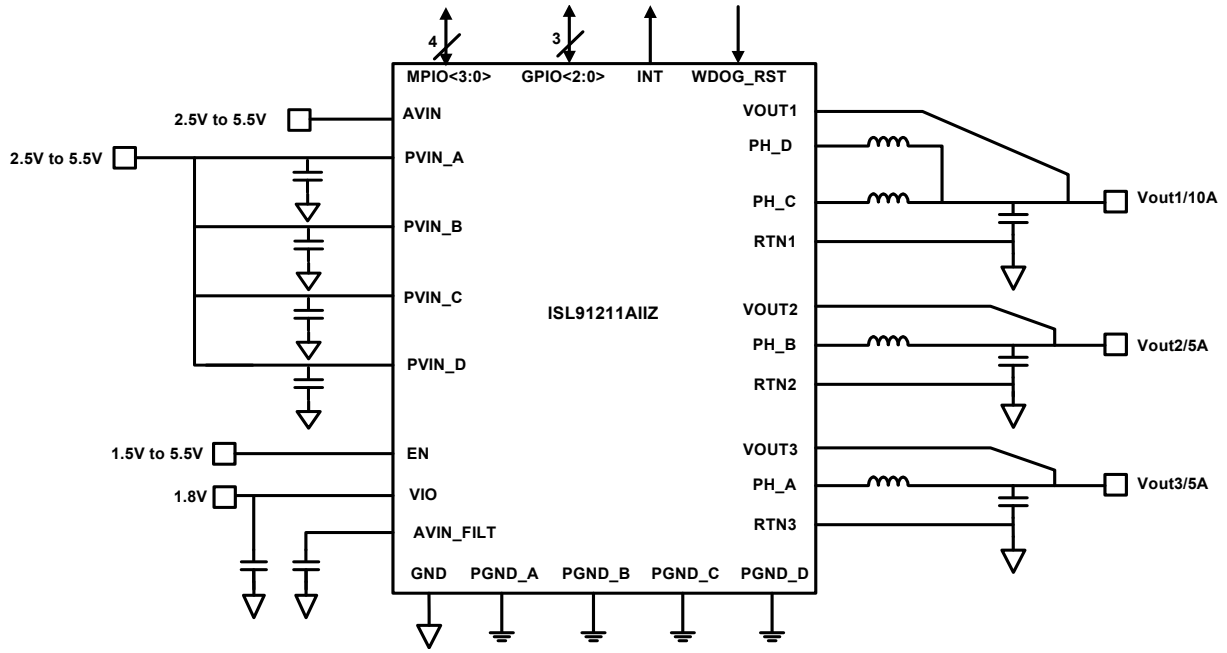


Figure 1. ISL91211A 2+ 1+1 Block Diagram

## 1. Overview

### 1.1 Contents

The ISL91211AII-EV1Z evaluation board includes:

- ISL91211AII-EV1Z evaluation board
- Evaluation software
- Renesas mini USB I<sup>2</sup>C dongle with USB cable (ISLUSBMINIEVAL1Z)
- All applicable documentation

### 1.2 Recommended Equipment

- 0V to 10V power supply with at least 10A current sourcing capability (VIN SUPPLY BIAS)
- 0V to 10V power supply with at least 1A current sourcing capability (VCC\_6V SUPPLY BIAS)
- Electronic loads capable of sinking current up to 10A
- Digital multimeter
- 500MHz quad-trace oscilloscope
- Dual edge slew rate controllable signal generator
- Differential probe (for load transient current measurement)

## 2. Functional Description

The ISL91211AII-EV1Z evaluation board provides a simple platform to demonstrate the feature-rich ISL91211A PMIC. It has a 0.9V output (default) on each of its output channels after start-up and each output voltage can be programmed by I<sup>2</sup>C/SPI. The evaluation board has been functionally optimized for best performance, working harmoniously with the factory default tuning on the ISL91211A. The input power and load connections are provided through multi-pin connectors for high current operations.

The ISL91211AII-EV1Z evaluation board is shown in [Figure 9 on page 10](#). [Table 1](#) lists the key test points and jumpers. The internal registers of the ISL91211A can be accessed by the I<sup>2</sup>C/SPI through the on-board header J24 (SPI) and J42 (I<sup>2</sup>C).

**Table 1. Description of Important Test Points and Jumpers**

Test Point(s)	Description
J6(+), J7(-)	Header for connecting V <sub>IN</sub> supply
J35(+), J38(-)	Buck1 Header for connecting external load
J37(+), J58(-)	Buck2 Header for connecting external load
J57(+), J36(-)	Buck3 Header for connecting external load
J3	V <sub>IN</sub> Kelvin connection for efficiency measurements
J15	Buck1 V <sub>OUT</sub> Kelvin connection for efficiency measurements
J18	Buck2 V <sub>OUT</sub> Kelvin connection for efficiency measurements
J56	Buck3 V <sub>OUT</sub> Kelvin connection for efficiency measurements
TP1	VCC_6V SUPPLY for VIO LDO and load transient circuits
J60	Buck1 driver input for load transient circuit
J61	Buck2 driver input for load transient circuit
J62	Buck3 driver input for load transient circuit
J52	Load transient current sense, 1A/10mV
J55	Load transient current sense, 1A/10mV
J59	Load transient current sense, 1A/10mV
J24	Header for connecting to SPI interface
J42B	Header for connecting to I <sup>2</sup> C interface
SW1	Enable/disable IC

The evaluation software GUI window for ISL91211A is shown in [Figure 8 on page 9](#). The schematic of the ISL91211AII-EV1Z evaluation board is shown in [Figure 13 on page 12](#). The PCB layout images for all layers are shown in [Figures 17 through 24](#) starting on [page 18](#). The bill of materials of the ISL91211AII-EV1Z is shown in [“ISL91211AII-EV1Z Evaluation Board Bill of Materials” on page 16](#).

### 2.1 Operating Range

The V<sub>IN</sub> range of the board is 2.5V to 5.5V. The adjustable V<sub>OUT</sub> range for the ISL91211AII-EV1Z is 0.3V to 2.0V. The I<sub>OUT</sub> range of the board is 0A to 5A per phase. The operating ambient temperature range is -40°C to +85°C.

**Note:** 2V operating range requires factory OTP support.

### 2.2 Quick Start Guide

For the ISL91211AII-EV1Z evaluation board, the default output voltage is set at 0.9V for all three outputs. No jumper configurations are needed to power up the part into its default state. When minimum bias conditions are met, all the settings and features are instead loaded through the one-time programmable memory inside the IC. The following Setup Guide describes how to power up the board for proper operation.

## 2.2.1 Setup Guide

1. Place scope probes on the  $V_{OUT}$  test point and other test points of interest.
2. Connect a power supply to J6 and J7 (VIN Supply), with voltage setting between 2.5V and 5.5V, this biases the PVIN and AVIN pins of the IC, but no start-up sequence has initiated and the quiescent current should be less than 1mA.
3. Connect a second power supply to TP1 (VCC\_6V) with the voltage set to 6V. This biases the VIO and Chip Enable pin as well as the on-board load transient circuits. ISL91211A boots up its internal reference, loads the default register settings, and then initiates a power-on sequence by toggling SW1 to the ENABLE position. All three outputs should turn on in the Pulse Skipping mode if there are no external loads present, and  $V_{OUT}$  should default to 0.9V.
4. During the start-up sequence, all three outputs should turn on sequentially, from Buck1 to Buck2 and next Buck3. Buck1 turns on with a 1.4ms delay from the Chip Enable pin going high, while the other Buck regulators turn on 1ms apart.
5. To initiate a shutdown sequence, toggle SW1 to the DISABLE position, and the ISL91211A turns off all the buck regulators at the same time.

## 2.2.2 I<sup>2</sup>C and SPI Communication

ISL91211A supports I<sup>2</sup>C communication by default, a USB to I<sup>2</sup>C communication dongle (ISLUSBMINIEVAL1Z) is included with each ISL91211AII-EV1Z, and the Renesas Graphical User Interface (GUI) supports this tool across all operating systems.

1. To communicate with ISL91211A using I<sup>2</sup>C, connect the Renesas USB to I<sup>2</sup>C dongle to J42B. Make sure R93 is present on the board, as it provides the pull-up from SPI\_SS to 1.8V VIO supply.

**Note:** For the SPI communication option using the GUI, contact Renesas [support](#).

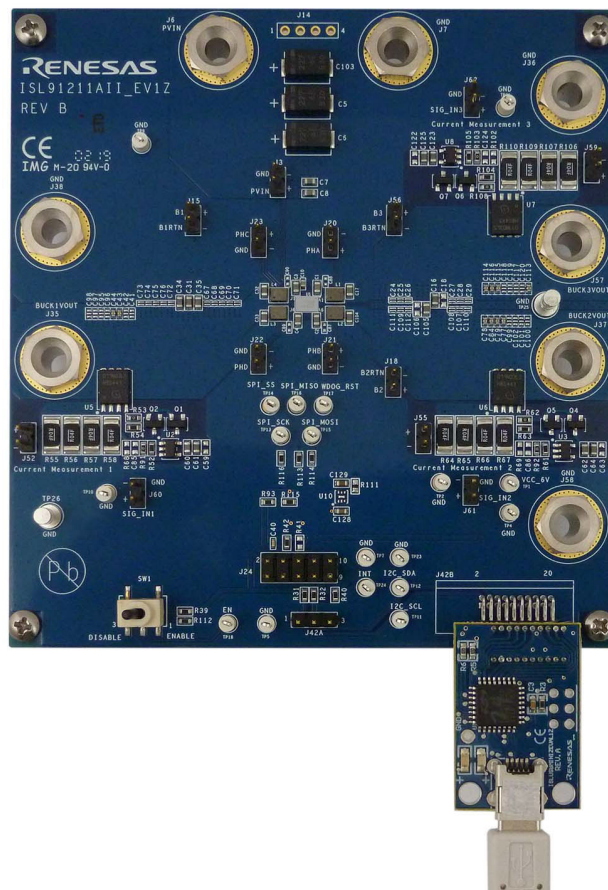


Figure 2. Communication Dongle Connection

### 2.2.3 Efficiency Measurement

1. Connect a power supply between J6 (PVIN) and J7 (GND) (VIN supply), with voltage setting between 2.8 and 5.5V, its current limit should be set high enough to support the maximum load current with additional headroom. If the power supply supports remote sense lines, use a Kelvin connection on J3. Otherwise, a multimeter needs to be connected at J3.
2. Apply 6V to TP1 (VCC\_6V) to initiate the start-up sequence and all three outputs turn on. To get an accurate single channel measurement, disable the other two outputs using the Renesas GUI.
3. Turn on the electronic load at VOUTx. The connection should be made at J35 (VOUT1), J37 (VOUT2), or J57 (VOUT3). Make sure the load current does not exceed 5A per phase, and the correct wire gauge is used when attaching the electronic load.
4. Measure the output voltage with a multimeter. The voltage should regulate within datasheet spec limits.
5. To determine efficiency, measure input and output voltages at the Kelvin sense test points (S+ and S-), which are located at J3 (VIN SENSE) and J15 (BUCK1 SENSE), J18 (BUCK2 SENSE), or J56 (BUCK3 SENSE) headers. Measure the input and output currents from the VIN power supply and the electronic load. Calculate efficiency based on these measurements. For detailed setup information, see [Figure 11 on page 11](#).

### 2.2.4 Load Transient Measurement

1. Go through the quick start procedure. The ISL91211AII-EVZ should already be powered up with 2.8V to 5.5V at J6 (VIN supply) and 6V at TP1 (VCC\_6V).
2. Connect a slew rate controllable signal generator to the transient load circuit input, J60 (TRANSIENT 1 PULSE GEN), J61 (TRANSIENT 2 PULSE GEN), or J62 (TRANSIENT 2 PULSE GEN).
3. Program the signal generator to pulse mode, set the frequency to 100Hz, ON duration to 200µs, and signal amplitude from 0V to 2V. The load transient circuit starts to turn on when the input is ~2.6V. When in doubt, always connect the signal generator output to an oscilloscope set to 1MΩ termination. The slew rate of the pulse, both rising and falling, should be conservatively slow, for example, 1µs.
4. Connect a differential probe to monitor load current across the sense resistors J52 (ISENSE1), J55 (ISENSE2), or J59 (ISENSE3). The load current can be accurately converted to a voltage at 1A/10mV. Make sure the vertical scale of the oscilloscope is set properly to display the full amplitude of the load profile.
5. Connect a second differential probe at the VOUT sense points connected to the VOUT decoupling capacitors, J15 (BUCK1 SENSE), J18 (BUCK2 SENSE), or J56 (BUCK3 SENSE).
6. Set the oscilloscope to measure the rise and fall times and maximum level of the load current. Slowly increase the signal generator amplitude and slew rate until the desired load profile is achieved. For detailed setup information, see [Figure 12 on page 11](#).

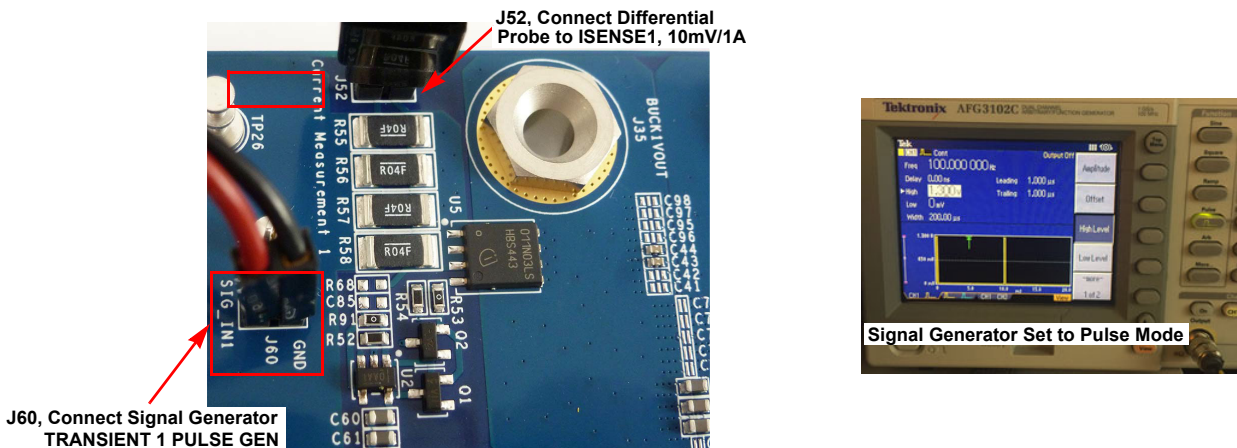


Figure 3. Buck1 Transient Load Connection Example

### 2.3 Evaluation Software Installation and Use

1. Extract the package and run **Autorun.exe**. Follow the instructions to install the Multiphase PMIC I<sup>2</sup>C Control Tool software.
2. Attach the USB-I<sup>2</sup>C interface (ISLUSBMINIEVAL1Z) dongle to computer using the supplied USB cable.
3. Attach the USB-I<sup>2</sup>C interface dongle to J42B on the ISL91211AII-EV1Z evaluation board. Follow the instructions in "[Setup Guide](#)" on page 6, connect the power supplies, DC load, and other test equipment to the ISL91211AII-EV1Z evaluation board and then apply power.
4. Start the Multiphase PMIC I<sup>2</sup>C Control Tool software. Select **Start > Programs > Renesas > Multiphase PMIC I<sup>2</sup>C Control Tool**.
5. Select **ISL91211** from the "Select Product" drop down menu. Click the **Connect** button on the GUI to establish connection between GUI and the dongle. The LED on the dongle lights up. If a connection is not detected, the software shows a red X next to **I<sup>2</sup>C Communication**. Press **Reset** to reconnect dongle.

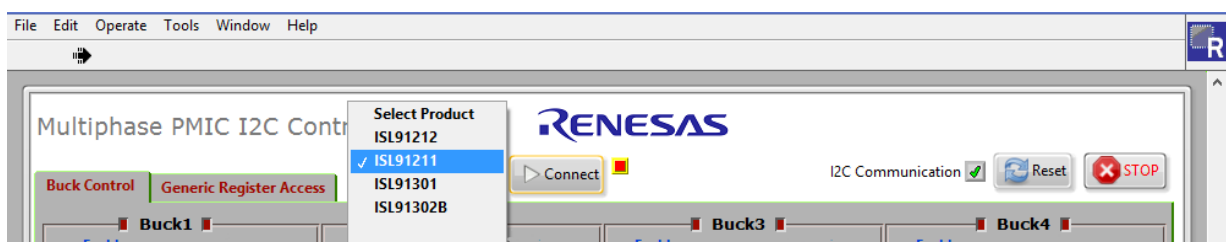


Figure 4. Product Selection Menu and I<sup>2</sup>C Communication OK Indicator

6. After the evaluation software establishes a connection to the USB- I<sup>2</sup>C interface dongle, the software loads a blank start-up script by default and reads all the pertinent register values to show on screen.
7. You should see Buck1 enabled, and the default DVS0 values should be 0.9V. If no fault conditions occurred during the board power-up, all the fault indicators (UV, OV, and OC) should be clear rather than red.
8. To change the output voltage, enter the desired value in voltages in the DVS0 control. There are also four default DVS values that are loaded as part of ISL91211A one time programmable memory space. You can go to any of them and activate a DVS command by clicking on the **DVS Pointer**.

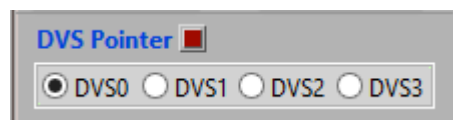


Figure 5. DVS Pointer Selection

9. Changing the **Max Voltage** control changes the internal feedback divider between ratios of 1x, 0.8x, and 0.6x. This changes the maximum output voltage the ISL91211A can support, with maximum being 2V. **Note:** The smallest DVS resolution the IC and the software can support is no less than the maximum voltage divided by 1023.
10. After the evaluation software is up and running without hiccup, it polls all the registers at 2s intervals by default. You can disable this feature by clearing the **Continuous Read** option.

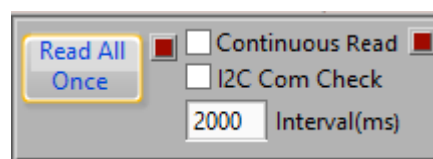


Figure 6. Continuous Read and Manual Read All Options

- 11. The fault indicators self-clear when the software reads the register through Continuous Read or the fault is removed. Three additional replica fault indicators (UV, OV, and OC) latch the faults so they clear only after you click **Push to Clear** in the event of spurious fault condition.

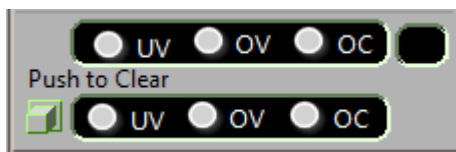


Figure 7. Fault Indicators

**Note:** The default switching frequency of the ISL91211A is set to 4MHz and slew rates for both DVS and power-up/down are set to 3mV/μs. These settings, along with many other features are programmable only through OTP request or a Startup Script and are not supported by evaluation software. For more information, please contact your local Renesas [support](#).

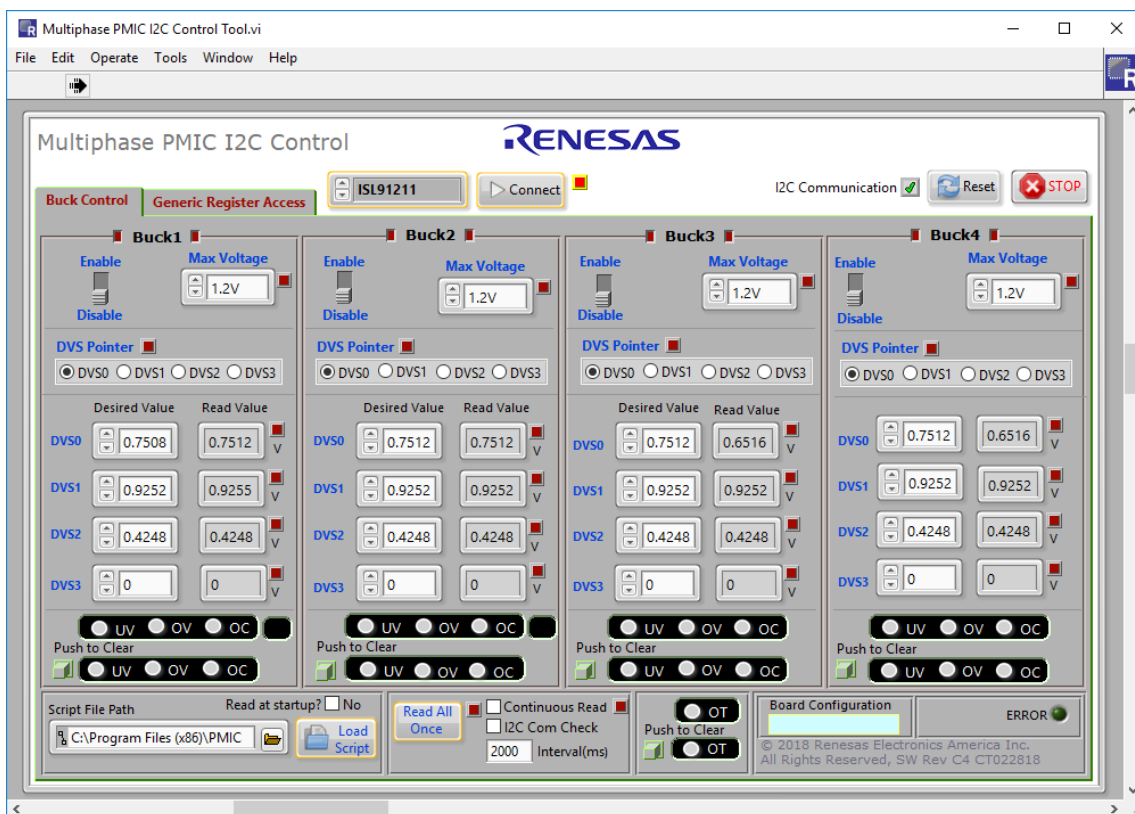


Figure 8. ISL91211A Evaluation Software Window

### 3. PCB Layout Guidelines

The ISL91211AII-EV1Z board is a 6-layer FR4 board. The main components are the ISL91211A, the passive filter components, test points, and connectors. A 220nH inductor is located close to each phase node of the ISL91211A, and 5x22µF in addition to 2x4.3µF low ESR capacitors are populated for dual phase rail and 2x22µF plus 4x4.3µF low ESR capacitors for single phase rails. PVIN is distributed using a power plane on an inner layer with a 10µF capacitor placed in close proximity to the PVIN and PGND balls of the power stage. In addition, there is a 10µF AVIN filter capacitor placed next to the ISL91211A referenced to a quiet ground plane.

The PCB layout is a very critical design step in making sure the designed converter works under optimum conditions. For the ISL91211A, the power loop is composed of the inductor, output capacitors, phase node, and PGND pins. It is necessary to keep this loop as short as possible and the connecting traces among them should be direct, short, and wide. The phase nodes of ISL91211A are very noisy, so keep remote sense signals away from traces coming out of the phase nodes, and do not route them under the inductor in an adjacent layer. Place the input capacitor as close as possible to the PVIN and PGND pins. Also, there should be a large unbroken ground plane that should connect all the decoupling capacitors together.

The heat of the ISL91211A is mainly dissipated through the GND and PHASE plane vias under the IC. To maximize thermal performance, use as much copper area as possible connecting to these vias. In addition, a solid ground plane is helpful for better EMI performance.

#### 3.0.1 Key Layout Strategies

- Place input capacitors as close as possible to their respective PVIN and PGND pins to minimize parasitic loop inductance.
- Route phase nodes with short, wide traces and avoid any sensitive nodes.
- Route the remote sense lines directly to the load using small, low inductance capacitors at the load for bypassing.
- Output capacitors should be close to the inductors and have a low impedance path to the PGND pins.
- Keep digital and phase nodes from intersecting AVIN\_FILT, VOUT, and RTN lines.
- Create a PGND plane on the 2nd layer of the PCB below the power components and bumps carrying high switching currents.

#### 3.1 ISL91211AII-EV1Z Evaluation Board

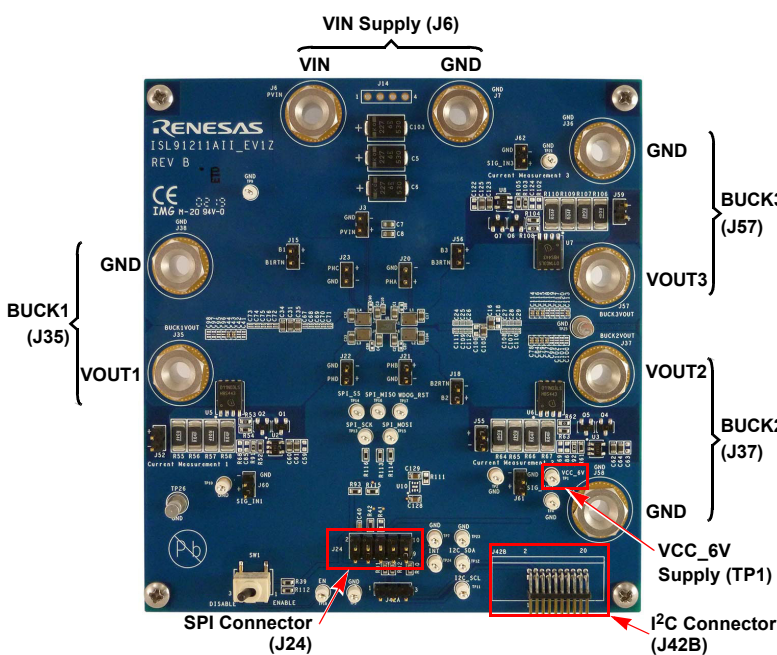


Figure 9. ISL91211AII-EV1Z Top View

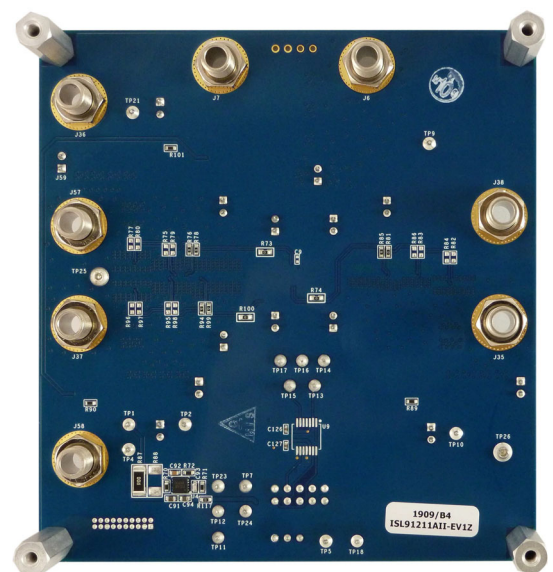


Figure 10. ISL91211AII-EV1Z Bottom View

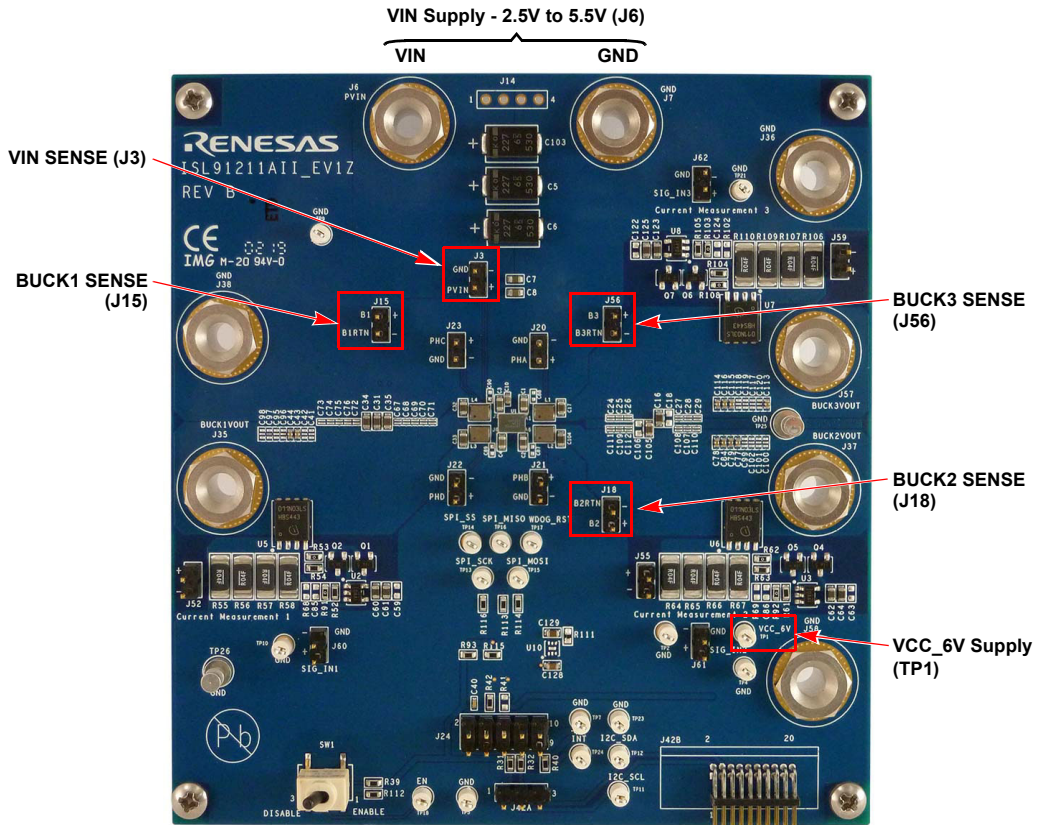


Figure 11. ISL91211AII-EV1Z Efficiency Measurement Connections

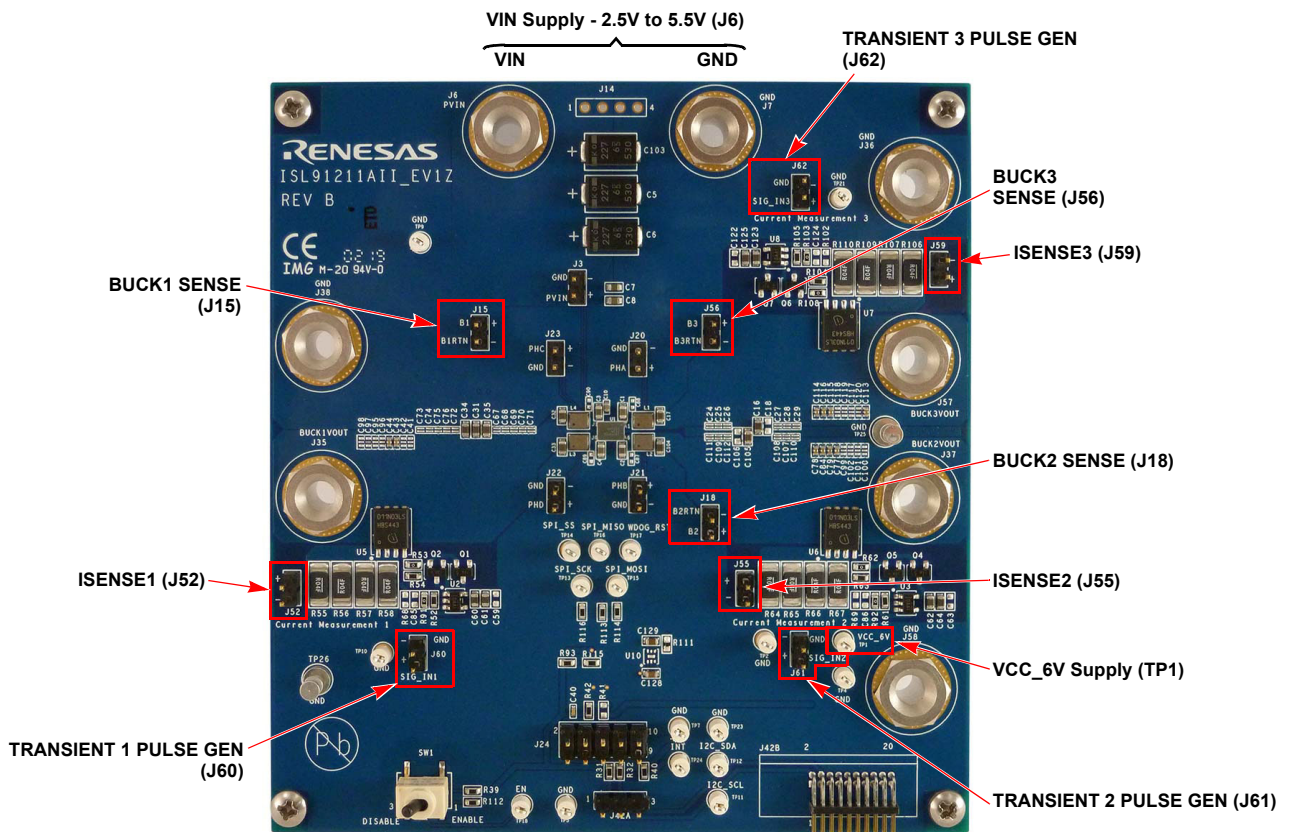


Figure 12. ISL91211AII-EV1Z Load Transient Measurement Connections

### 3.2 ISL91211AII-EV1Z PCB Schematics

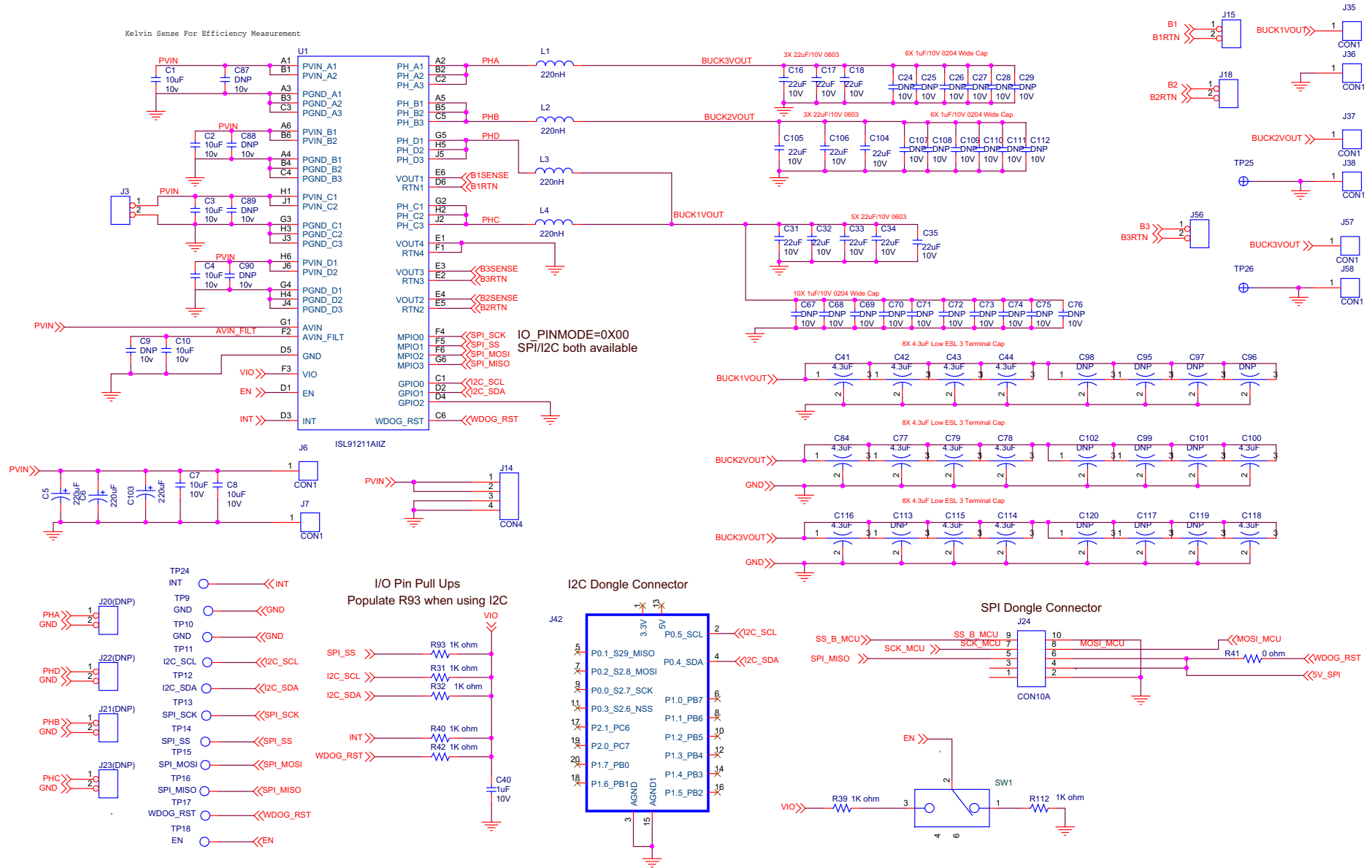
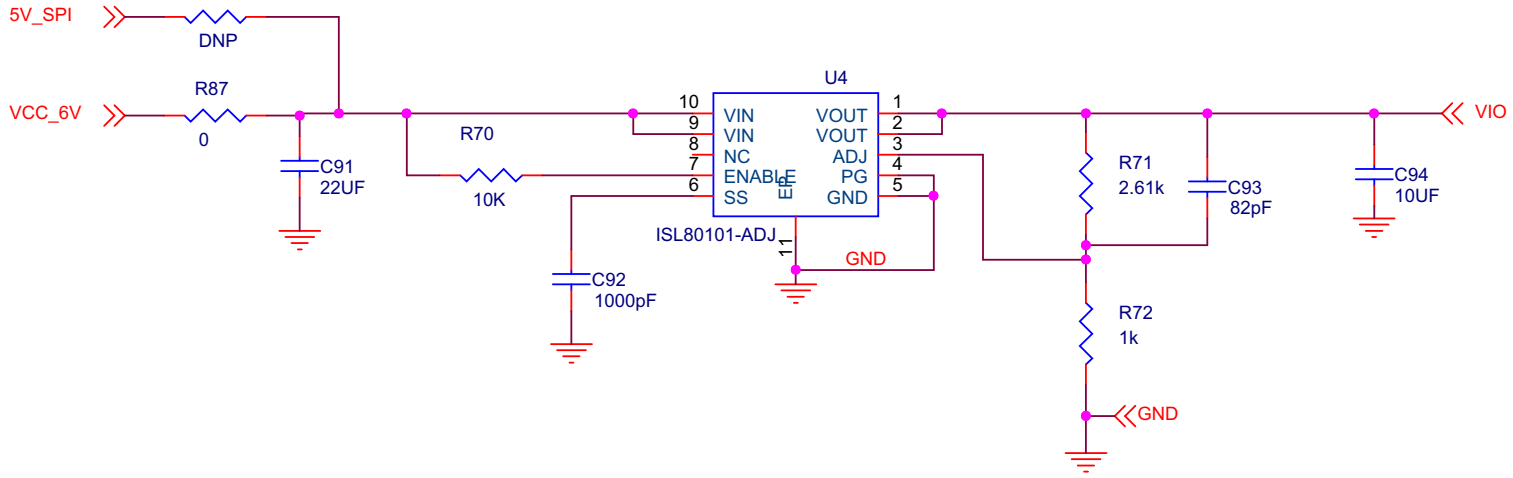


Figure 13. ISL91211AII-EV1Z



Output sense resistors for each rail.

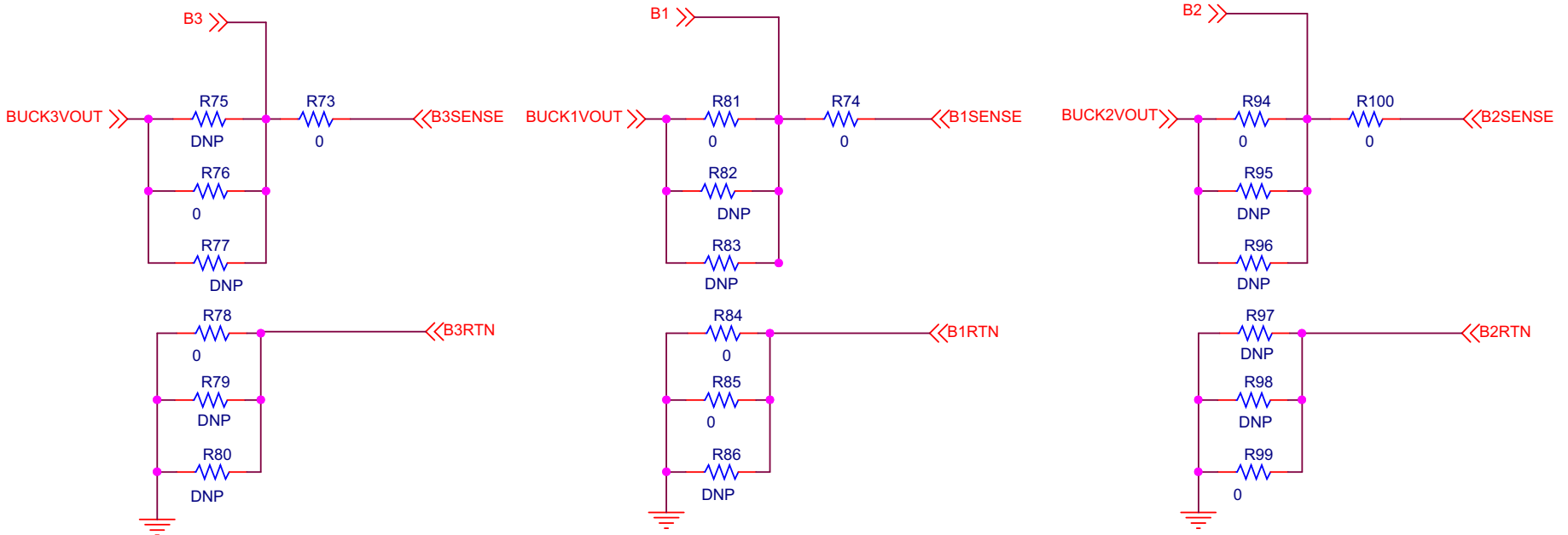
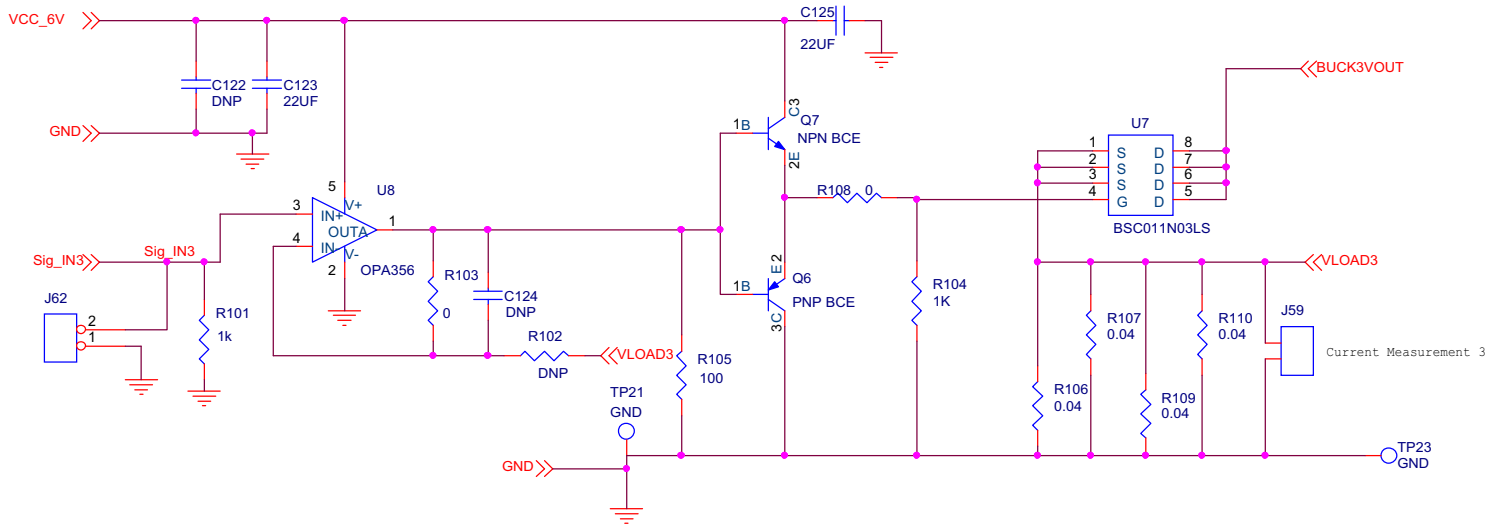


Figure 14. VIO Regulator and Feedback Resistors



Transient Load Circuit for Buck 3



Set signal generator minimum amplitude at J62 = 1V+, current measurement at J59 is 10mV/1A

Figure 16. Transient Load Circuit for Buck3

### 3.3 ISL91211AII-EV1Z Evaluation Board Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, ISL91211AII-EV1Z, REVB, ROHS	Imagineering Inc	ISL91211AII-EV1ZREVBPCB
0	C24-C29, C67, C68-C76 C107-C112	CAP, SMD, 0201, DNP-PLACE HOLDER, ROHS		
2	C126, C127	CAP, SMD, 0402, 0.1µF, 10V, 10%, X5R, ROHS	Murata	GRM155R61A104KA01D
1	C40	CAP, SMD, 0402, 1.0µF, 10V, 10%, X5R, ROHS	Murata	GRM155R61A105KE15D
1	C10	CAP, SMD, 0402, 10µF, 10V, 20%, X5R, ROHS	Samsung	CL05A106MP5NUNC
0	C9, C87, C88, C89, C90	CAP, SMD, 0402, DNP-PLACE HOLDER, ROHS		
1	C92	CAP, SMD, 0603, 1000pF, 100V, 10%, X7R, ROHS	Venkel	C0603X7R101-102KNE
2	C128, C129	CAP, SMD, 0603, 10µF, 16V, 10%, X5R, ROHS	Murata	GRM188R61C106KAALD
16	C16, C17, C31, C32, C33, C34, C35, C60, C61, C62, C64, C91, C104, C105, C123, C125	CAP, SMD, 0603, 22µF, 10V, 20%, X5R, ROHS	TDK	C1608X5R1A226M
0	C18, C59, C63, C85, C86, C106, C122, C124	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS		
7	C1, C2, C3, C4, C7, C8, C94	CAP-AEC-Q200, SMD, 0603, 10µF, 10V, 20%, X5R, ROHS	Taiyo Yuden	LMK107BBJ106MAHT
10	C43, C44, C77, C78, C79, C84, C113, C114, C115, C116	CAP-AEC-Q200, SMD, 0402, 4.3µF, 2.5V, 20%, ROHS	Murata	NFM15PC435R0E3D
1	C93	CAP-AUTO, SMD, 0603, 82pF, 250V, 5%, C0G/NP0, ROHS	Taiyo Yuden	QVS107CG820JCHT
3	C5, C6, C103	CAP-TANT, SMD, 7.3x4.3, 220µF, 6.3V, 20%, 40mΩ, ROHS	Kemet	T520D227M006ATE040
4	L1, L2, L3, L4	COIL-PWR CHOKE INDUCTOR, SMD, 2.5x2mm, 0.22µH, 20%, 6.3A, ROHS	Cyntec Co.,Ltd.	HMLB25201T-R22MSR-01
8	J6, J7, J35, J36, J37, J38, J57, J58	CONN-JACK, BANANA-SS-SDRLESS, VERTICAL, 0.40Length, ROHS	Johnson Components	108-0740-102
2	TP25, TP26	CONN-TURRET, TERMINAL POST, TH, ROHS	Keystone	1514-2
18	TP1, TP2, TP4, TP5, TP7, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP21, TP23, TP24	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	Keystone	5002
1	J24	CONN-HEADER, 2x5, BRKAWY-2x36, 2.54mm, ROHS	Berg/FCI	67996-272HLF
14	J3, J15, J18, J20, J21, J22, J23, J52, J55, J56, J59, J60, J61, J62	CONN-HEADER, 1x2, RETENTIVE, 2.54mm, 0.230x0.120, ROHS"	Berg/FCI	69190-202HLF
1	J42A	CONN-HEADER, TH, 1x3, 2mmPITCH, 3.5mmMATING, 2.3mmPOST, ROHS	Harwin Inc	M22-2510305
1	J42B	CONN-HEADER, TH, 2x10, 1.27mmPITCH, R/A, ROHS	Harwin Inc	M50-3901042
1	U4	IC-ADJ.V, 1A LDO REGULATOR, 10P, DFN, 3x3, ROHS	Renesas	ISL80101IRAJZ
1	U1	IC-4-PHASE, 3-OUTPUT PMIC, 54P, WLCSP, ROHS	Renesas	ISL91211AIIZ
3	U2, U3, U8	IC-OP-AMP, R/R OUTPUT, SMD, 5P, SOT23-5, 200MHZ, ROHS	Texas Instruments	OPA356AIDBVR

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
3	U5, U6, U7	TRANSIST-MOS, N-CHANNEL, 30V, 100A, SMD, 8P, PG-TDSON-8, ROHS	Infineon Technology	BSC011N03LS
3	Q1, Q4, Q7	TRANSISTOR-NPN, SMD, SOT-23, 40V, 200mA, 350mW, ROHS	Fairchild	MMBT3904
3	Q2, Q5, Q6	TRANSISTOR-PNP, SMD, SOT-23, 40V, 200mA, 350mW, ROHS	Fairchild	MMBT3906
1	R111	RES-AEC-Q200, SMD, 0402, 10k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-2RKF1002X
3	R52, R61, R105	RES-AEC-Q200, SMD, 0603, 100Ω, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1000V
14	R31, R32, R39, R40, R42, R54, R63, R72, R89, R90, R93, R101, R104, R112	RES-AEC-Q200, SMD, 0603, 1k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1001V
5	R113, R114, R115, R116, R70	RES-AEC-Q200, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1002V
1	R71	RES-AEC-Q200, SMD, 0603, 2.61k, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF2611V
16	R53, R62, R73, R74, R76, R78, R81, R85, R91, R92, R94, R99, R100, R103, R108, R117	RES-AEC-Q200, SMD, 0603, 0Ω, 1/10W, TF, ROHS	Panasonic	ERJ-3GEY0R00V
0	R41, R68, R69, R75, R77, R79, R80, R82, R83, R84, R86, R95, R96, R97, R98, R102	RES, SMD, 0603, DNP-PLACE HOLDER, ROHS		
1	R87	RES-AEC-Q200, SMD, 2010, 0Ω, 3/4W, TF, ROHS	Stackpole	RMCF2010ZT0R00
0	R88	RES, SMD, 2010, DNP, DNP, DNP, TF, ROHS		
12	R55, R56, R57, R58, R64, R65, R66, R67, R106, R107, R109, R110	RES-AEC-Q200, SMD, 2010, 0.04Ω, 1W, 1%, CURR.SENSE, ROHS	Vishay/Dale	WSL2010R0400FEA18
1	SW1	SWITCH-TOGGLE, SMD, 6PIN, SPDT, 2POS, ON-NONE-ON, ROHS	ITT Industries/ C&K Division	GT11MSCBE
4	Four corners	SCREW, 4-40x1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	Building Fasteners	PMSSS 440 0025 PH
4	Four corners	STANDOFF, 4-40x3/4in, F/F, HEX, ALUMINUM, 0.25 OD, ROHS	Keystone	2204
0	C41, C42, C95-C102, C117-C120	DO NOT POPULATE OR PURCHASE		
0	J14	DO NOT POPULATE OR PURCHASE		
0	U9, U10	DO NOT POPULATE OR PURCHASE		

### 3.4 ISL91211AII-EV1Z PCB Layout

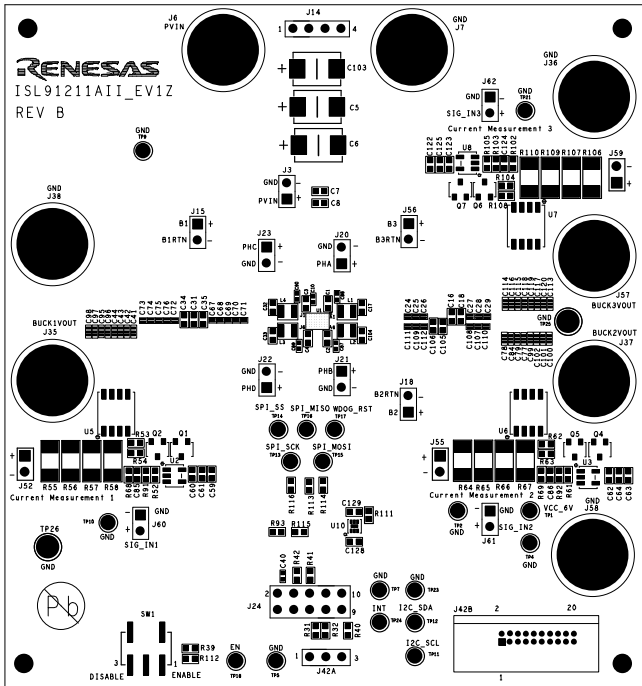


Figure 17. Top Silkscreen Layer

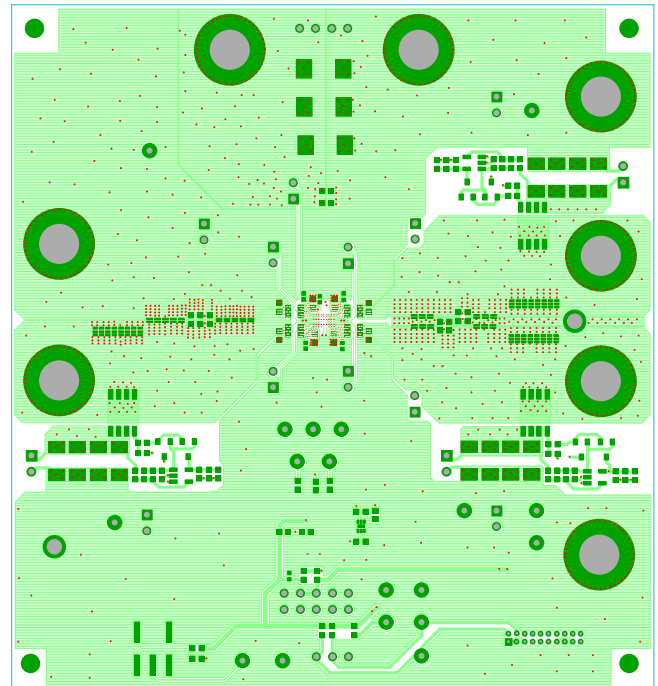


Figure 18. Top Layer

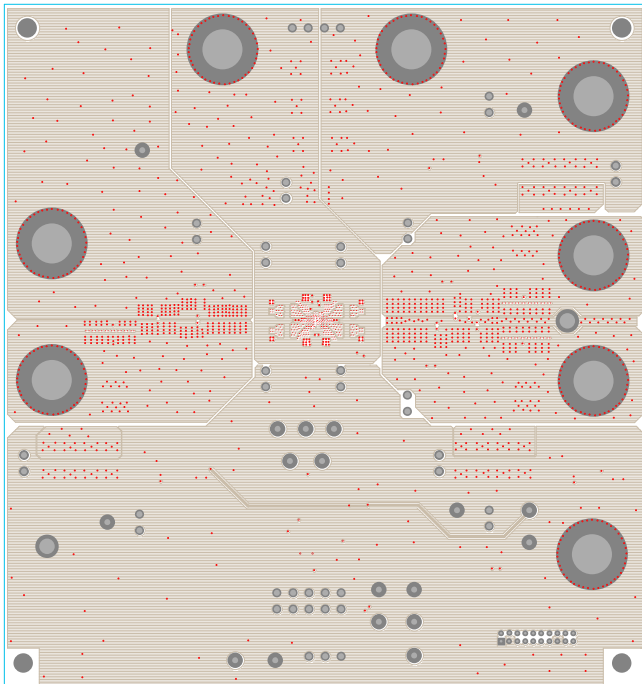


Figure 19. Layer 2 (PVIN Plane)

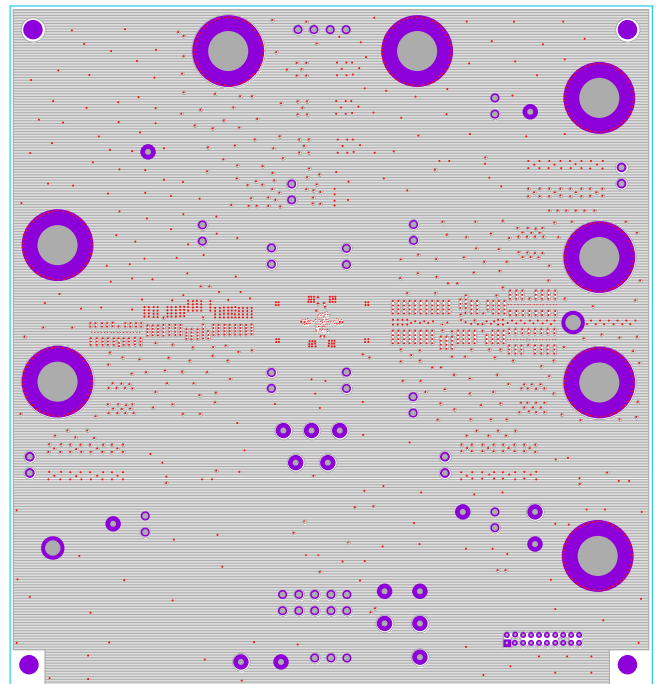


Figure 20. Layer 3 (GND Plane)

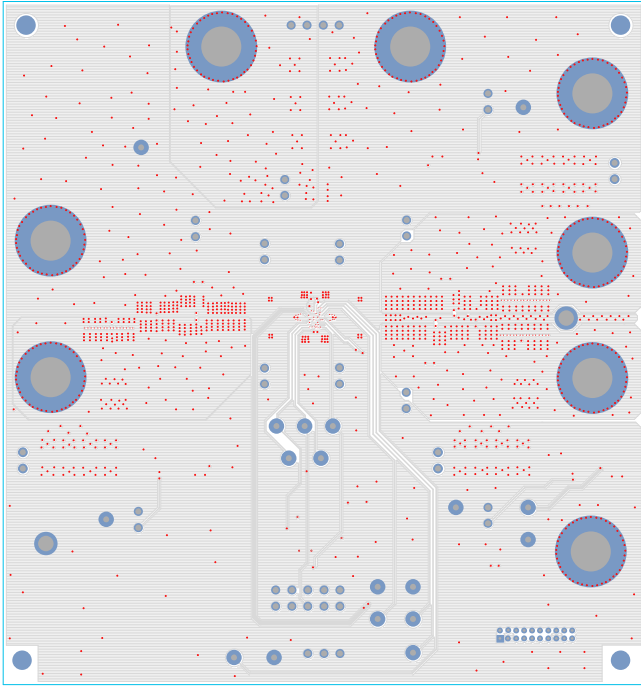


Figure 21. Layer 4 (IO Communications)

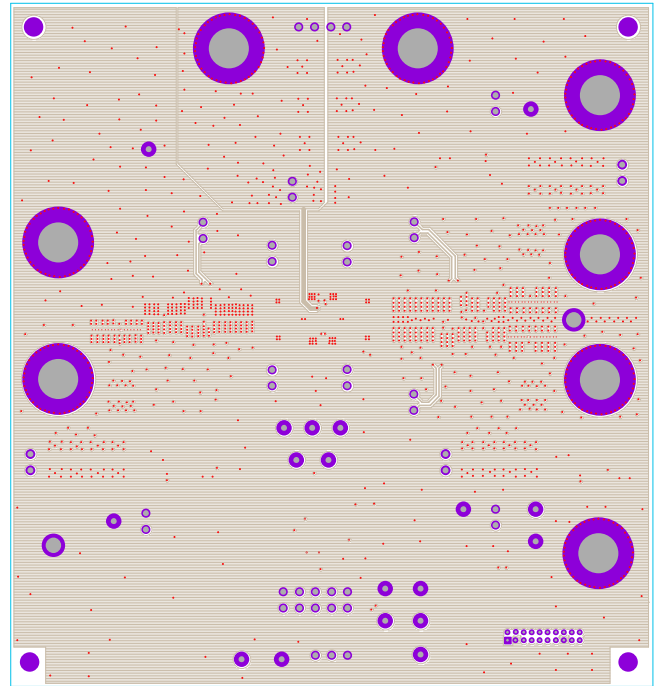


Figure 22. Layer 5 (GND Plane)

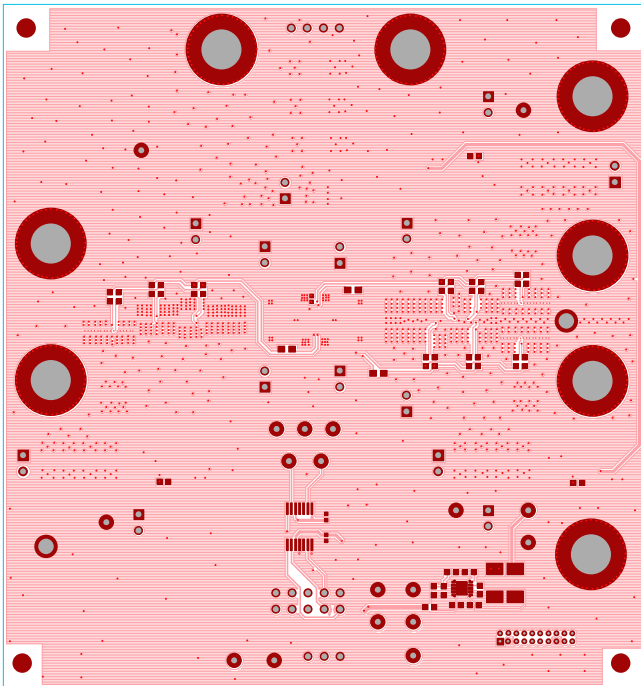


Figure 23. Bottom Layer (Remote Sense Lines)

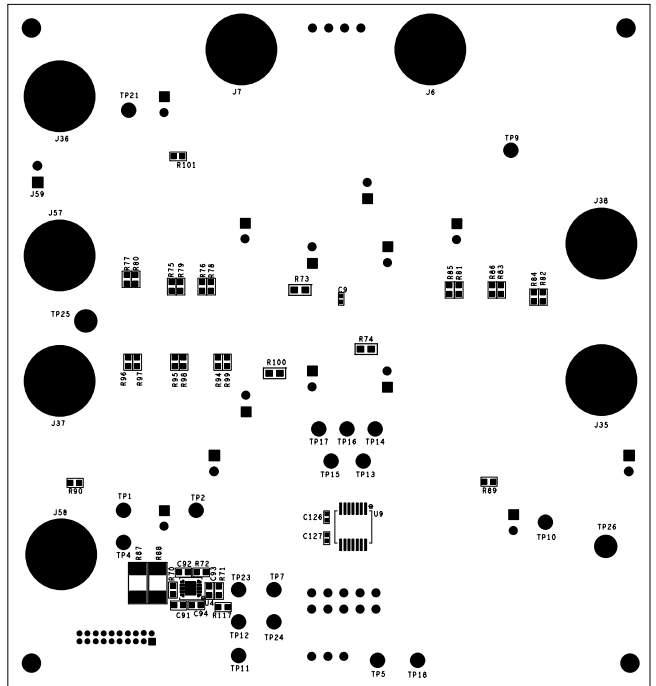


Figure 24. Bottom Silk Screen Layer

### 4. Typical Performance Curves

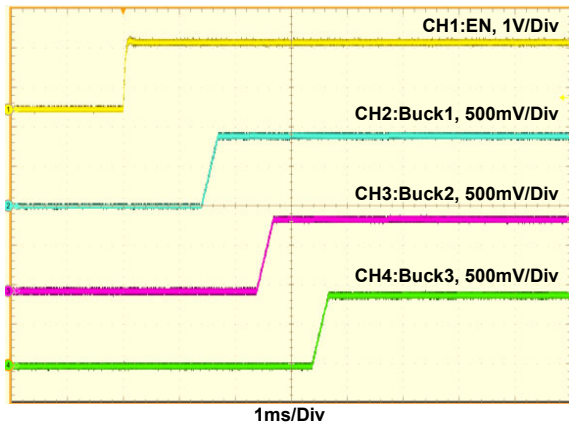


Figure 25. Start-Up by EN, VOUT1, 2, 3 = 0.9V

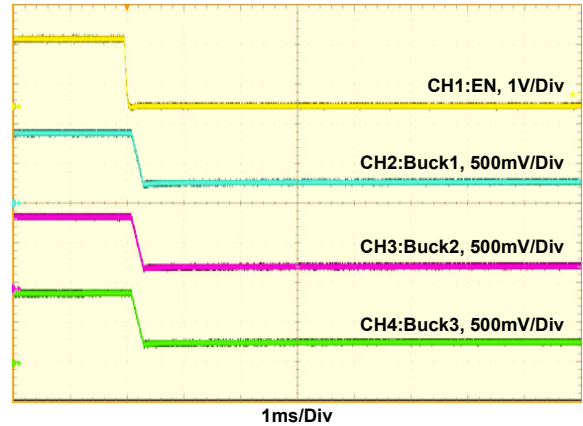


Figure 26. Shutdown by EN, VOUT1, 2, 3 = 0.9V

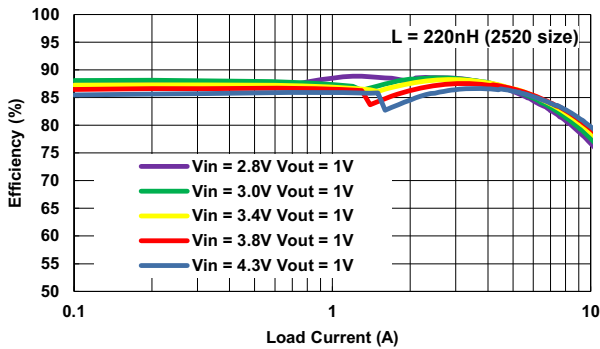


Figure 27. Dual-Phase Efficiency (V<sub>OUT</sub> = 1V), Continuous Load Sweep (0.1A to 10A)

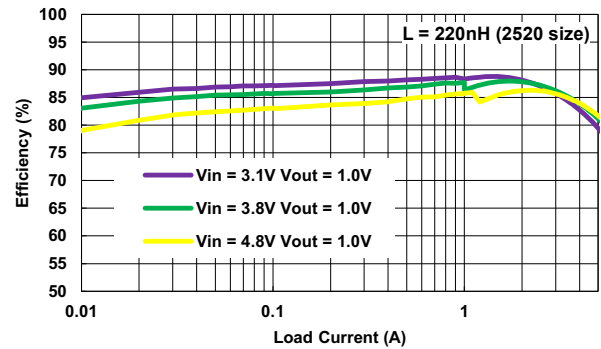
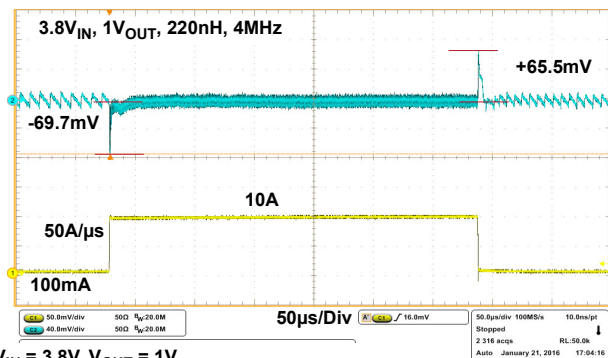
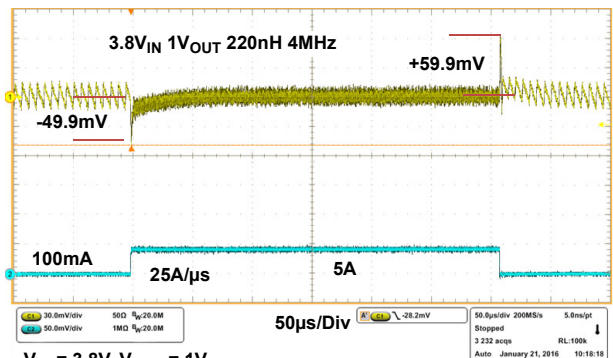


Figure 28. Single-Phase Efficiency (V<sub>OUT</sub> = 1V), Continuous Load Sweep (0.01A to 5A)



V<sub>IN</sub> = 3.8V, V<sub>OUT</sub> = 1V  
 Load Step Slew Rate: 50A/µs, 0.1A to 10A  
 220nH Inductor (Cyntec)  
 3x22µF Capacitor (0603 6.3V Murata)  
 6x4.7µF Capacitor (0603 10V)

Figure 29. Dual-Phase Load Transient (10A/200ns)



V<sub>IN</sub> = 3.8V, V<sub>OUT</sub> = 1V  
 Load Step Slew Rate: 25A/µs, 0.1A to 5A  
 220nH Inductor (Cyntec)  
 1x22µF Capacitor (0603 6.3V Murata)  
 6x4.3µF Capacitor (Low ESL)

Figure 30. Single-Phase Transient (5A/200ns)

## 5. Revision History

Rev.	Date	Description
2.00	Sep.24.19	<p>Added Revision History</p> <p>Updated to new template.</p> <p>Page 1, Specifications - updated:</p> <ul style="list-style-type: none"><li>• from: DVS slew rate of 2.5mV/μs to: • Default DVS slew rate of 3mV/μs.</li><li>• from: Power-up sequence: SW→SW2→SW3, 1ms delay between each rail to: Power-up sequence: VOUT1→VOUT2→VOUT3, 1ms delay between each rail</li></ul> <p>Updated Figure 1</p> <p>Updated Table 1</p> <p>Removed Note from Operating Range section.</p> <p>Setup Guide step 2 updated from: Connect a power supply to J6 to: Connect a power supply to J6 and J7.</p> <p>Updated Note in I<sup>2</sup>C and SPI Communications section.</p> <p>Updated Evaluation Software Installation and Use section.</p> <p>Updated board photos, schematics, PCB layouts.</p>

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(Rev.4.0-1 November 2017)

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