ISL91212BEVAL1Z

The ISL91212BEVAL1Z evaluation board allows quick evaluation of the high performance features of the ISL91212B multi-output PMIC, which has four controllers capable of configuring its power stages for 1+1+1+1 channel outputs. Each channel can deliver up to 5A continuous output current per phase. The ISL91212B uses the proprietary Renesas R5 modulator technology to maintain accurate voltage regulation while providing excellent efficiency and transient response. The ISL91212BEVAL1Z also supports the standard I^2C protocol, which is ideal for systems using a single-cell battery.

Specifications

The board is designed to operate at the following operating conditions:

- Input voltage rating from 2.5V to 5.5V
- Programmable output voltage range of 0.3V to 2V
- 1+1+1+1 configuration with 5A maximum load current/phase
- 2MHz default switching frequency
- DVS slew rate of 2.5mV/µs
- Power-up/Power-down sequence: BUCK1-4 power up/power down at the same time
- Operating temperature range: -40°C to +85°C
- V_{OUT1} = 1.0V, V_{OUT2} = 1.5V, V_{OUT3} = 0.75V, V_{OUT4} = 0.75V

Features

- Small, compact design
- Supports I^2C communication protocol
- Adjustable V_{OUT} and independent DVS control for both channels
- Real-time fault protection and monitoring (OC, UV, OV, and OT)
- Six layer board design optimized for thermal performance and efficiency
- Connectors, test points, and jumpers for easy measurements
- Built-in load transient circuits for each output channel

Contents

The ISL91212BEVAL1Z evaluation board shipment contains:

- ISL91212BEVAL1Z evaluation board
- Evaluation software
- Renesas mini USB I^2C dongle with USB cable (ISLUSBMINIEVAL1Z)

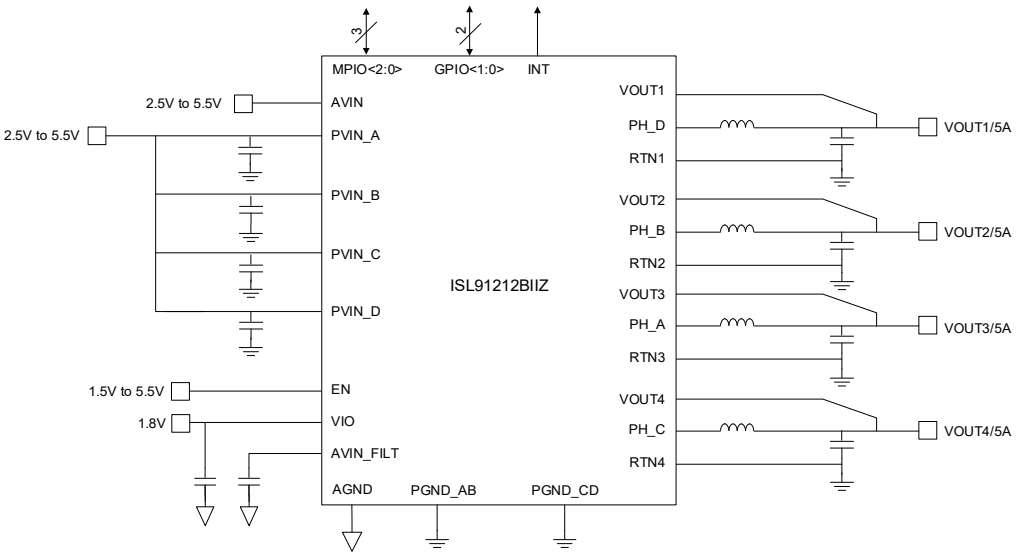

Figure 1. Block Diagram

Contents

1. Functional Description

The ISL91212BEVAL1Z evaluation board provides a simple platform to demonstrate the feature-rich ISL91212B PMIC. The ISL91212BEVAL1Z has a 1.0V, 1.5V, 0.75V, and 0.75V output (default) on each output channel after start-up, and the I^2C can program each output voltage. The ISL91212BEVAL1Z is functionally optimized for best performance, working harmoniously with the factory default tuning on the ISL91212B. The input power and load connections are provided through multi-pin connectors for high-current operations.

The ISL91212BEVAL1Z is shown in Figure 11. The ISL91212BEVAL1Z's key test points and jumpers are listed in Table 1. The I^2C can access the ISL91212B's internal registers through the on-board header J_{72} (I^2C).

Table 1. Important Test Points and Jumpers

Test Point	Description
J_6(+), J_7(-)	Header for connecting VIN supply
J_{35}(+), J_{65}(-)	Buck1 header for connecting external load
J_{37}(+), J_{58}(-)	Buck2 header for connecting external load
J_{57}(+), J_{36}(-)	Buck3 header for connecting external load
J_{64}(+), J_{38}(-)	Buck4 header for connecting external load
J_3	V_{IN} Kelvin connection for efficiency measurements
J_{71}	Buck1 V_{OUT} Kelvin connection for efficiency measurements
J_{68}	Buck2 V_{OUT} Kelvin connection for efficiency measurements
J_{70}	Buck3 V_{OUT} Kelvin connection for efficiency measurements
J_{69}	Buck4 V_{OUT} Kelvin connection for efficiency measurements
TP_1	VCC_6V supply for VIO LDO and load transient circuits
J_{60}	Buck1 driver input for load transient circuit
J_{61}	Buck2 driver input for load transient circuit
J_{62}	Buck3 driver input for load transient circuit
J_{66}	Buck4 driver input for load transient circuit
J_{52}	Buck1 load transient current sense, 1A/10mV
J_{55}	Buck2 load transient current sense, 1A/10mV
J_{59}	Buck3 load transient current sense, 1A/10mV
J_{67}	Buck4 load transient current sense, 1A/10mV
J_{72}	Header for connecting to I^2C interface

The Multiphase PMIC I2C Control Tool (ISL91212B evaluation software) GUI is shown in Figure 10. The ISL91212BEVAL1Z schematic is shown in Figure 15 through Figure 18. The PCB layout images for all layers are shown in Figure 19 through Figure 26. The ISL91212BEVAL1Z bill of materials is shown in Table 3.

1.1 Recommended Equipment

- 0V to 10V power supply with at least 10A current sourcing capability (VIN SUPPLY BIAS)
- 0V to 10V power supply with at least 1A current sourcing capability (VCC_6V SUPPLY BIAS)
- Electronic loads capable of sinking current up to 10A
- Digital multimeter
- 500MHz quad trace oscilloscope
- Dual edge slew rate controllable signal generator
- Differential probe (for load transient current measurement)

1.2 Operating Range

The ISL91212BEVAL1Z V_{IN} range is 2.5V to 5.5V. The adjustable V_{OUT} range is 0.3V to 2.0V. The I_{OUT} range is 0A to 5A per phase. The operating ambient temperature range is -40°C to +85°C.

1.3 Quick Start Guide

The ISL91212BEVAL1Z's default output voltages are shown in Table 2:

Table 2. Default Output Voltages

V_{OUT1}	1.0V
V_{OUT2}	1.5V
V_{OUT3}	0.75V
V_{OUT4}	0.75V

No jumper configurations are needed to power the ISL91212BEVAL1Z into its default state. After the minimum bias conditions are met, all the settings and features are loaded through the one-time programmable memory inside the IC. See Setting Up the ISL91212BEVAL1Z for information about how to power up the board for proper operation.

1.3.1 Setting Up the ISL91212BEVAL1Z

1. Place scope probes on the V_{OUT} test point and other test points of interest.
2. Connect a power supply to J_6 and J_7 (VIN SUPPLY) with a voltage setting between 2.5V and 5.5V. This connection biases the PVIN and AVIN pins but does not initiate the startup sequence. The quiescent current should be less than 1mA.
3. Connect a second power supply to TP_1 (VCC_6V) with the voltage set to 6V. This connection biases the VIO Chip Enable pin, and onboard load transient circuits. The ISL91212B boots up its internal reference, loads the default register settings, and initiates a power-on sequence. If no external loads are present, the four outputs should turn on in Pulse Skipping mode. V_{OUT1} defaults to 1.0V, V_{OUT2} defaults to 1.5V, V_{OUT3} defaults to 0.75V, and V_{OUT4} defaults to 0.75V.
4. During the startup sequence, the four outputs should turn on simultaneously. The outputs turn on with a 1.4ms delay from the Chip Enable pin going high.
5. To initiate the shutdown sequence, toggle Switch SW_1 to the DISABLE position to put EN to GND. The ISL91212BEVIZ turns off all the buck regulators at the same time.

1.3.2 Enabling I²C Communication

The ISL91212B supports I²C communication by default. A USB to I²C communication dongle (ISLUSBMINIEVAL1Z) is included with each ISL91212BEVAL1Z board, and the evaluation software supports this tool across all operating systems.

To communicate with ISL91212B using I²C, connect the Renesas USB to the I²C dongle to J_{72}.

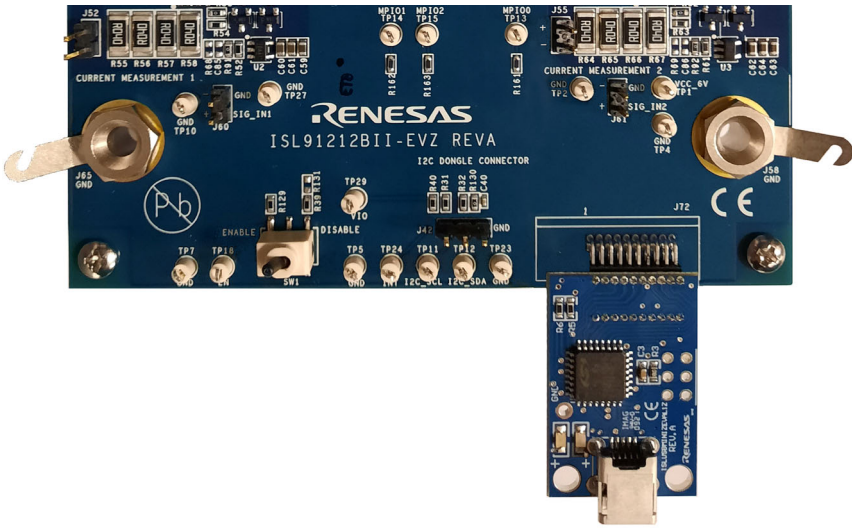

Figure 2. Communication Dongle Connection

1.3.3 Measuring Efficiency

1. Connect a power supply at J_6 (VIN) with the voltage setting between 2.5V and 5.5V. Set the power supply's current limit high enough to support the maximum load current with additional headroom. If the power supply supports remote sense lines, use a Kelvin connection on J_3. Otherwise, connect a multimeter at J_3.
2. Apply 6V to TP_1 (VCC_6V) to initiate the startup sequence. All four outputs turn on. Disable the other three outputs using the **Enable/Disable** switch in the GUI to get an accurate single channel measurement.
3. Turn on the electronic load at VOUTx. Make the connection at J_{35} (V_{OUT1}), J_{37} (V_{OUT2}), J_{57} (V_{OUT3}), or J_{64} (V_{OUT4}). Ensure the load current does not exceed 5A per phase, and use the correct wire size when attaching the electronic load.
4. Measure the output voltage with a multimeter. The voltage should regulate within the limits specified in the *ISL91212B Datasheet*.
5. To determine efficiency:
   a. Measure the input and output voltages at the Kelvin sense test points (S+ and S-), which are located at J_3 (VIN SENSE), J_{71} (BUCK1 SENSE), J_{68} (BUCK2 SENSE), J_{70} (BUCK3 SENSE), and J_{69} (BUCK4 SENSE).
   b. Measure the input and output currents from the VIN power supply and the electronic load.
   c. Calculate efficiency based on these measurements. For detailed setup information, see Figure 13.

1.3.4 Measuring Load Transients

1. Complete the setup procedure (see Setting Up the ISL91212BEVAL1Z). The ISL91212BEVAL1Z should be powered up with 2.5V to 5.5V at J_6 (VIN supply) and 6V at TP_1 (VCC_6V).
2. Connect a slew rate controllable signal generator to the transient load circuit input J_{60} (TRANSIENT 1 PULSE GEN), J_{61} (TRANSIENT 2 PULSE GEN), J_{62} (TRANSIENT 3 PULSE GEN), or J_{66} (TRANSIENT 4 PULSE GEN).

3. Program the signal generator to Pulse mode and set the frequency to 100Hz, the ON duration to 200µs, and the signal amplitude from 0V to 2V. The load transient circuit turns on when the input is ~2.6V. When in doubt, connect the signal generator output to an oscilloscope set to 1MΩ termination. The slew rate of the pulse, both rising and falling, should be conservatively slow (for example, 1µs).
4. Connect a differential probe to monitor load current across the sense resistors J_{52} (ISENSE1), J_{55} (ISENSE2), J_{59} (ISENSE3), or J_{67} (ISENSE4). The load current can be accurately converted to a voltage at 1A/10mV. Ensure the vertical scale of the oscilloscope is set properly to display the full amplitude of the load profile.
5. Connect a second differential probe at the VOUT sense points connected to the VOUT decoupling capacitors J_{15} (BUCK1 SENSE), J_{18} (BUCK2 SENSE), J_{56} (BUCK3 SENSE), or J_{63} (BUCK4 SENSE).
6. Set the oscilloscope to measure the rise and fall times and the maximum level of the load current. Slowly increase the signal generator amplitude and slew rate until the required load profile is achieved. For detailed setup information, see Figure 14.

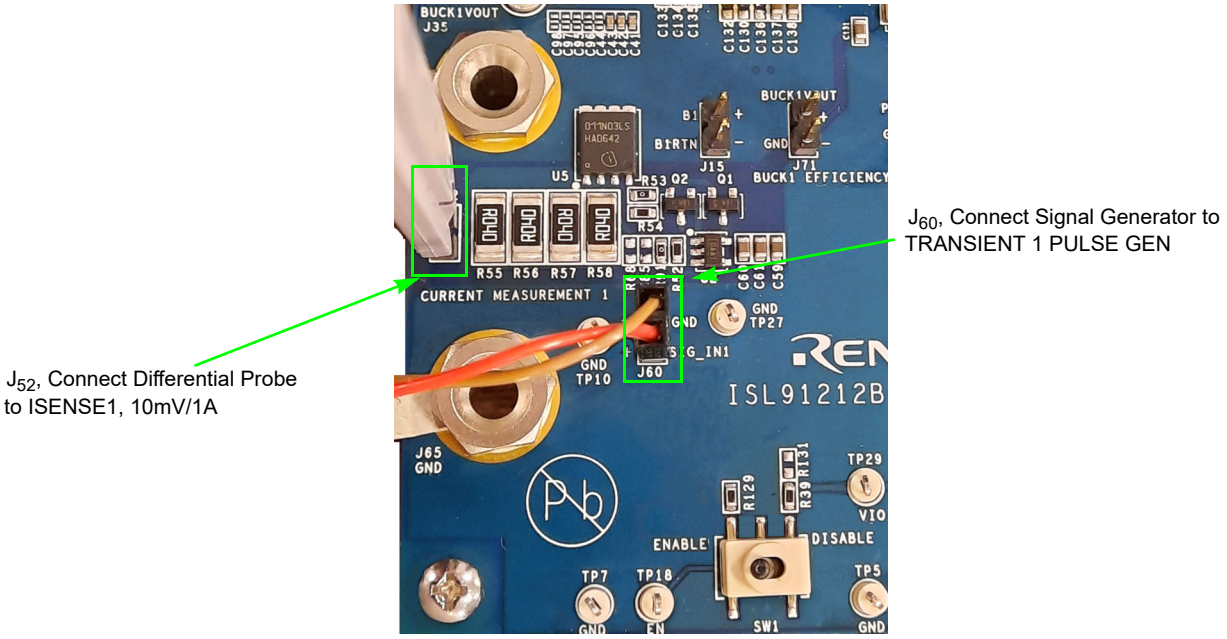

Figure 3. BUCK1 Transient Load Connection Example

1.4 Installing and Using the Evaluation Software

1. Download the Multiphase PMIC I2C Control Tool from the ISL91212B product page, and double-click **AutoRun.exe**. Follow the instructions in the installation wizard to install the software.
2. Attach the USB-I^{2}C interface (ISLUSBMINIEVAL1Z) dongle to the computer using the supplied USB cable.
3. Attach the USB-I^{2}C interface dongle to J_{72} on the ISL91212BEVAL1Z.
4. Follow the instructions in Setting Up the ISL91212BEVAL1Z to connect the power supplies, DC load, and other test equipment to the ISL91212BEVAL1Z.
5. Apply power to the ISL91212BEVAL1Z.
6. Navigate to the Start menu and select **Programs** > **Renesas** > **Multiphase PMIC I2C Control Tool** to start the Multiphase PMIC I2C Control Tool software.

7. Select **ISL91212** from the **Select Product** drop-down menu in the GUI.

Figure 4. Product Select Menu and I²C Communication OK Indicator

8. Click the **Connect** button to establish a connection between the GUI and the dongle. The LED light on the dongle turns on.
   a. The software shows a green check mark next to **I2C Communication** if a connection is detected.

Figure 5. I²C Communication OK Indicator

   b. The software shows a red X next to **I2C Communication** if a connection is not detected. Click **Reset** to reconnect the dongle.
9. After the evaluation software establishes a connection to the USB-I²C interface dongle, the software loads a blank startup script by default. It reads all the pertinent register values to show on the screen.
10. Buck1, Buck2, Buck3, and Buck4 are all enabled. The default DVS0 values are1.0V for Buck1, 1.5V for Buck2, 0.75V for Buck3, and 0.75V for Buck4.
    a. If no fault conditions occurred during board power-up, all the fault indicators (UV, OV, OC) are clear.
    b. If fault conditions occurred during board power-up, the fault indicators are red.
11. To change the output voltage, enter the value in voltages in the DVS0 control. Four default DVS values are loaded as part of the ISL91212B one-time programmable memory space. The user can select any of them and activate a DVS command by clicking the DVS pointer when the corresponding BUCKx_DVSCTRL bit is 0.

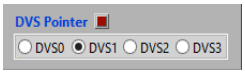

Figure 6. DVS Pointer Selection

12. Changing the **Max Voltage** controls changes the internal feedback divider between ratios of 1x, 0.8x, and 0.6x. This changes the maximum output voltage the ISL91212B can support, with a maximum of 2V. The smallest DVS resolution the IC and the software can support is no less than the maximum voltage divided by 1024.
13. The evaluation software polls all the registers at 2s intervals by default. You can disable this feature by deselecting the **Continuous Read** option.

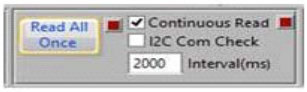

Figure 7. Continuous Read and Manual Read All Options

14. The fault indicators self-clear when the software reads the register through Continuous Read or the fault is removed. Three additional replica fault indicators (UV, OV, and OC) latch the faults so they clear only after you click **Push to Clear** if a spurious fault condition occurs.

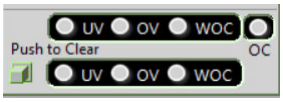

Figure 8. Fault Indicators

15. Select the **Generic Register Access** tab to write into or read from a specific register.
16. Select the register name from the drop-down menu to update the **Register Address** box with the address of the selected register.
17. To write data, enter the data to be written in the **Data In** field, then click **Write**.
18. To read data that has been written, click **Read**. The read value appears in the **Data Out** field.

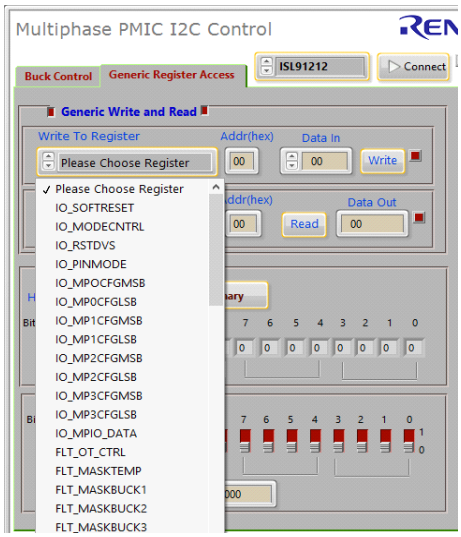

Figure 9. Generic Register Access

Note: The ISL91212BEVAL1Z's default switching frequency is 2MHz, and the slew rates for DVS and power-up/down are 2.5mV/µs. These settings and many other features are programmable only through an OTP request or a startup script and are not supported by the evaluation software. For more information, contact your local Renesas sales representative.

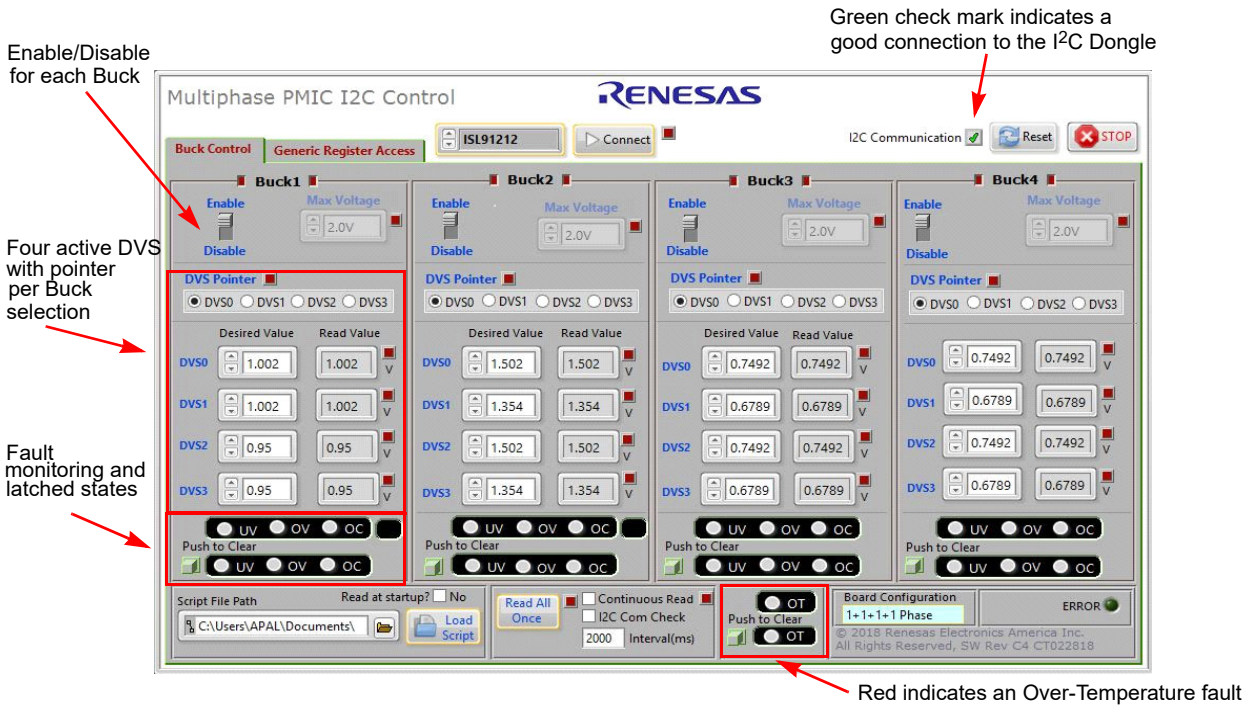

Figure 10. ISL91212B Evaluation Software Window

2. PCB Layout Guidelines

The ISL91212BEVAL1Z board is a 6-layer FR4 board. The main components are the ISL91212B and its passive filter components, test points, and connectors. The Buck inductor is located close to each phase node of the ISL91212B, and Buck output filter capacitors are populated at the output of each inductor. PVIN is distributed using a power plane on an inner layer with the Buck input filter capacitor placed in close proximity to the PVIN and PGND balls of the power stage. The AVIN filter capacitor is placed next to the ISL91212B, referenced to a quiet ground plane.

The PCB layout is a critical design step in ensuring the designed converter works under optimum conditions. The ISL91212BEVAL1Z's power loop consists of the inductor, output capacitors, phase node, and PGND pins. Keep this loop as short as possible. The connecting traces among them should be direct, short, and wide. To minimize the noise coupling, keep remote sense signals away from traces coming out of the phase nodes, and do not route them under the inductor in an adjacent layer. Place the input capacitor as close as possible to the PVIN and PGND pins, and a large unbroken ground plane should connect all the decoupling capacitors together.

Heat is dissipated mainly through the GND and PHASE plane vias under the IC. To maximize thermal performance, use as much copper area as possible connecting to these vias. In addition, a solid ground plane is helpful for better EMI performance.

2.1 Key Layout Strategies

- Place input capacitors as close as possible to their respective PVIN and PGND pins to minimize parasitic loop inductance.
- Route phase nodes with short, wide traces and avoid any sensitive nodes.
- Route the remote sense lines directly to the load using small, low inductance capacitors at the load for bypassing.
- Place output capacitors close to the inductors with a low impedance path to the PGND pins.
- Prevent digital and phase nodes from intersecting the AVIN_FILT, VOUT, and RTN lines.
- Create a PGND plane on the second layer of the PCB below the power components and bumps carrying high switching currents.

2.2 Evaluation Board

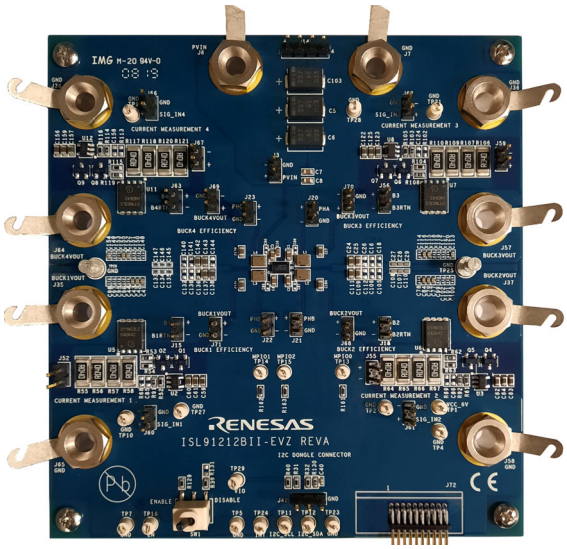

Figure 11. ISL91212BEVAL1Z Top View

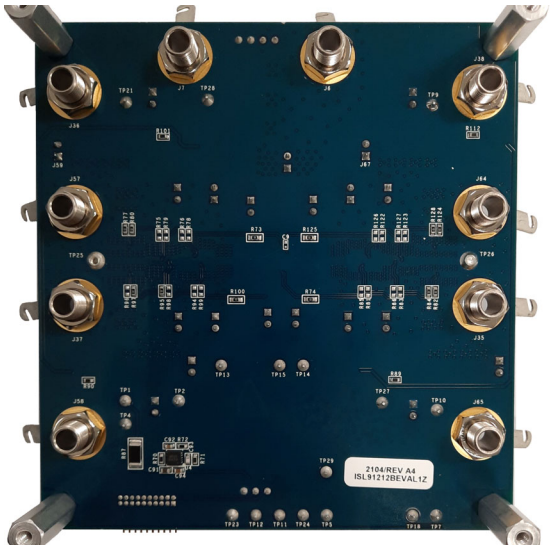

Figure 12. ISL91212BEVAL1Z Bottom View

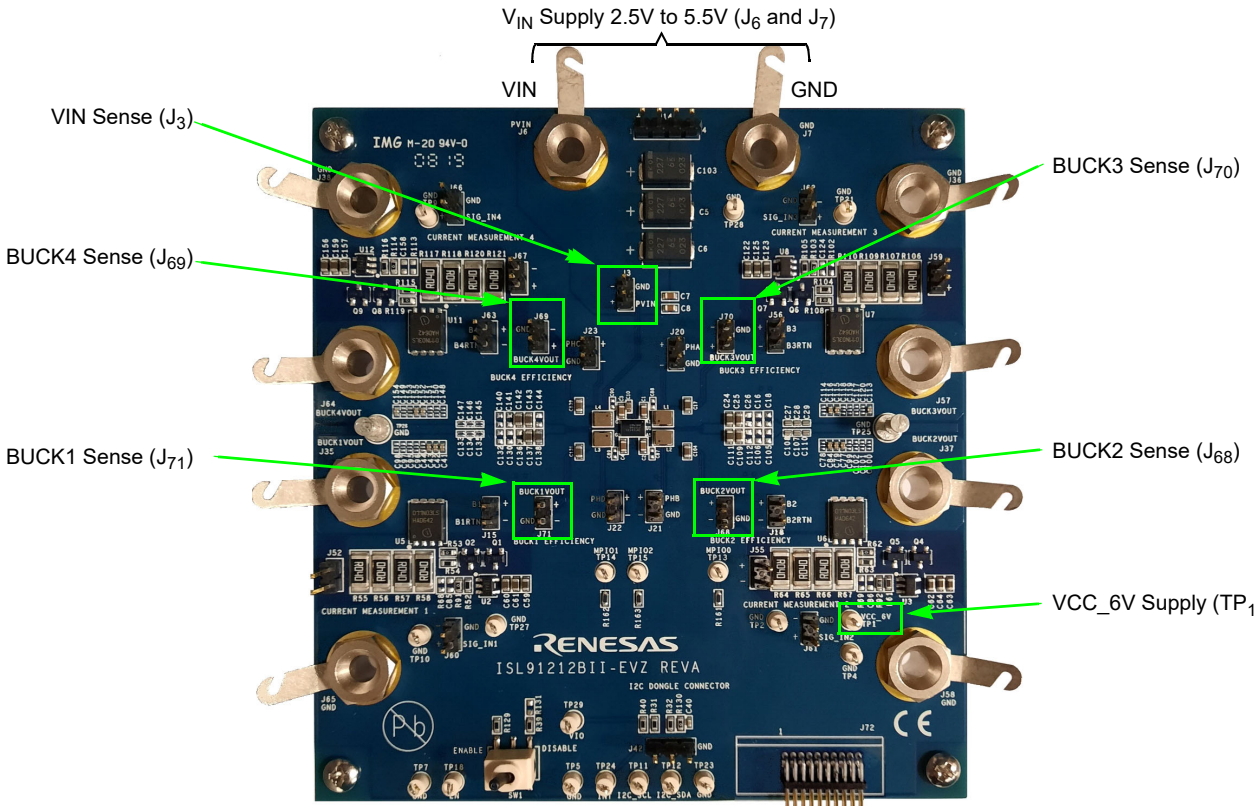

Figure 13. ISL91212BEVAL1Z Efficiency Measurement Connections

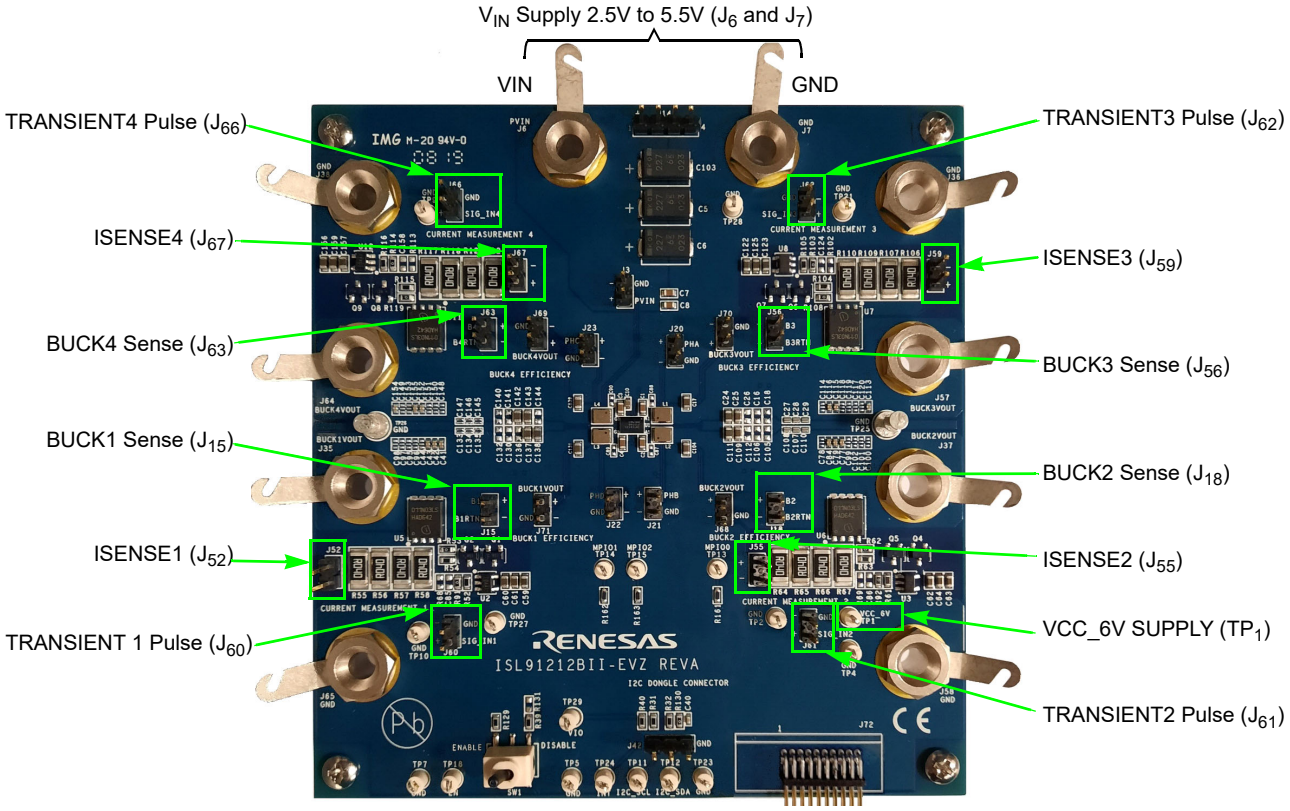

Figure 14. ISL91212BEVAL1Z Load Transient Measurement Connections

2.3 Schematics

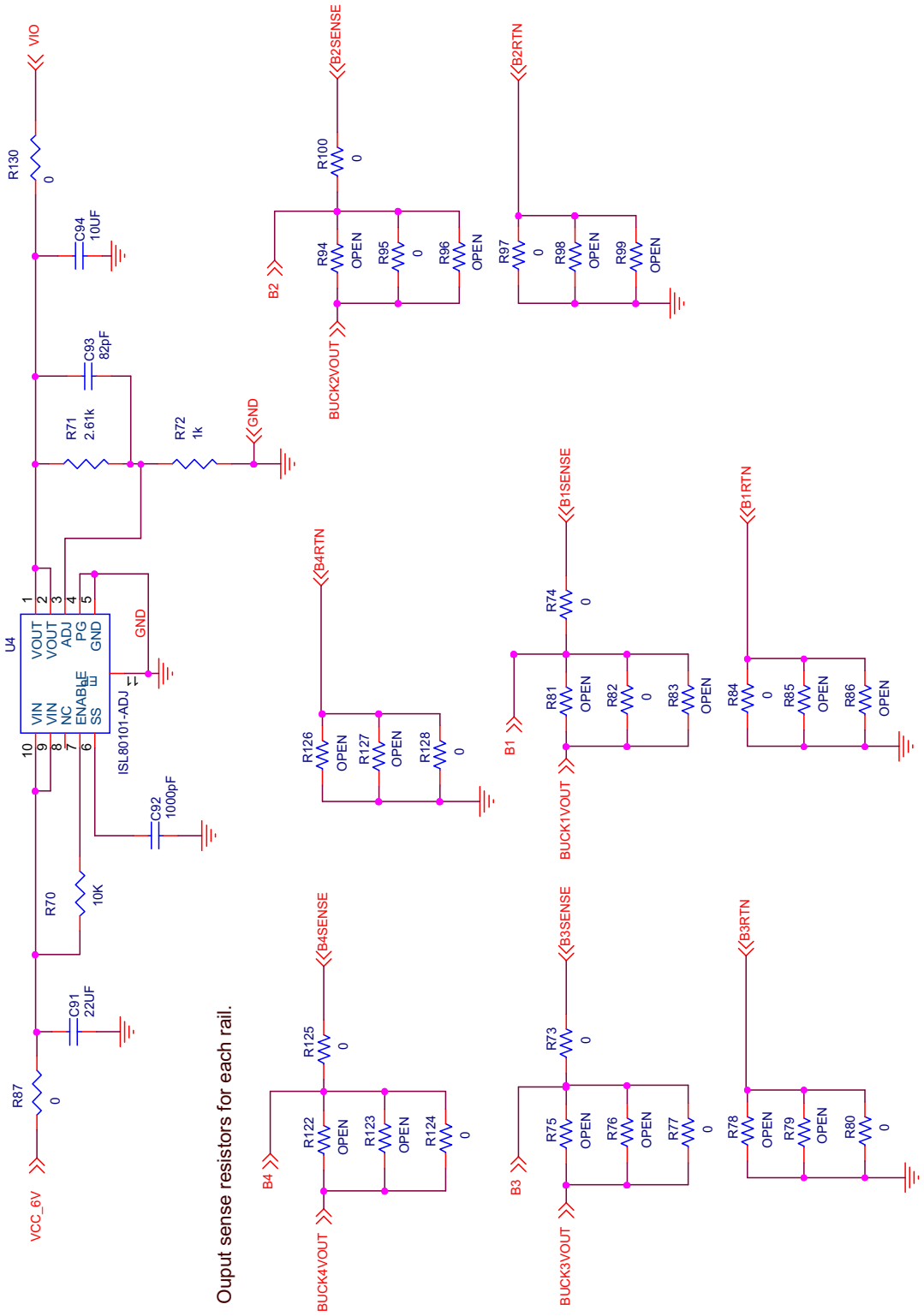

Figure 15. ISL91212BEVAL1Z Schematic - Page 1[1]

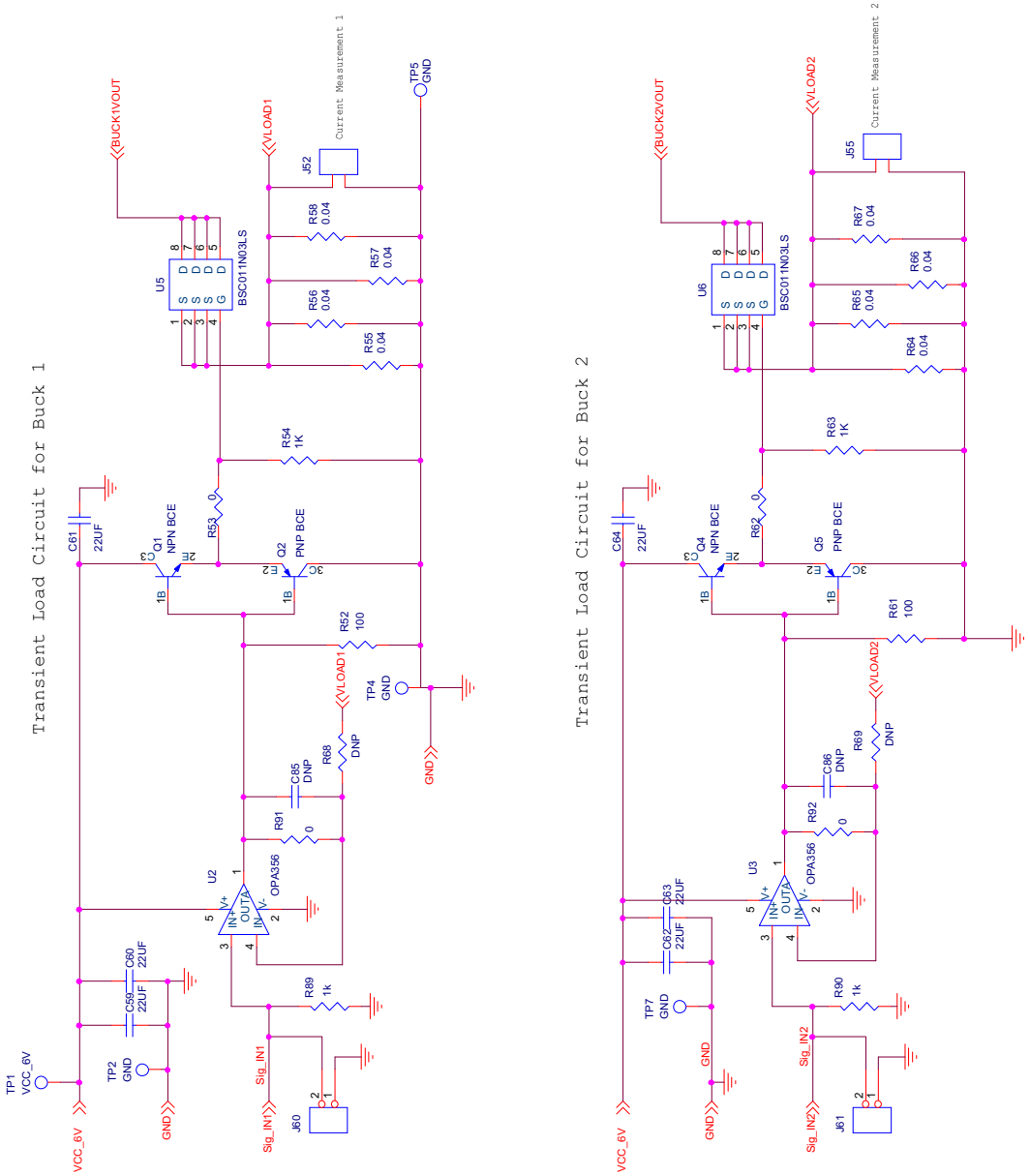

Figure 16. ISL91212BEVAL1Z Schematic - Page 2

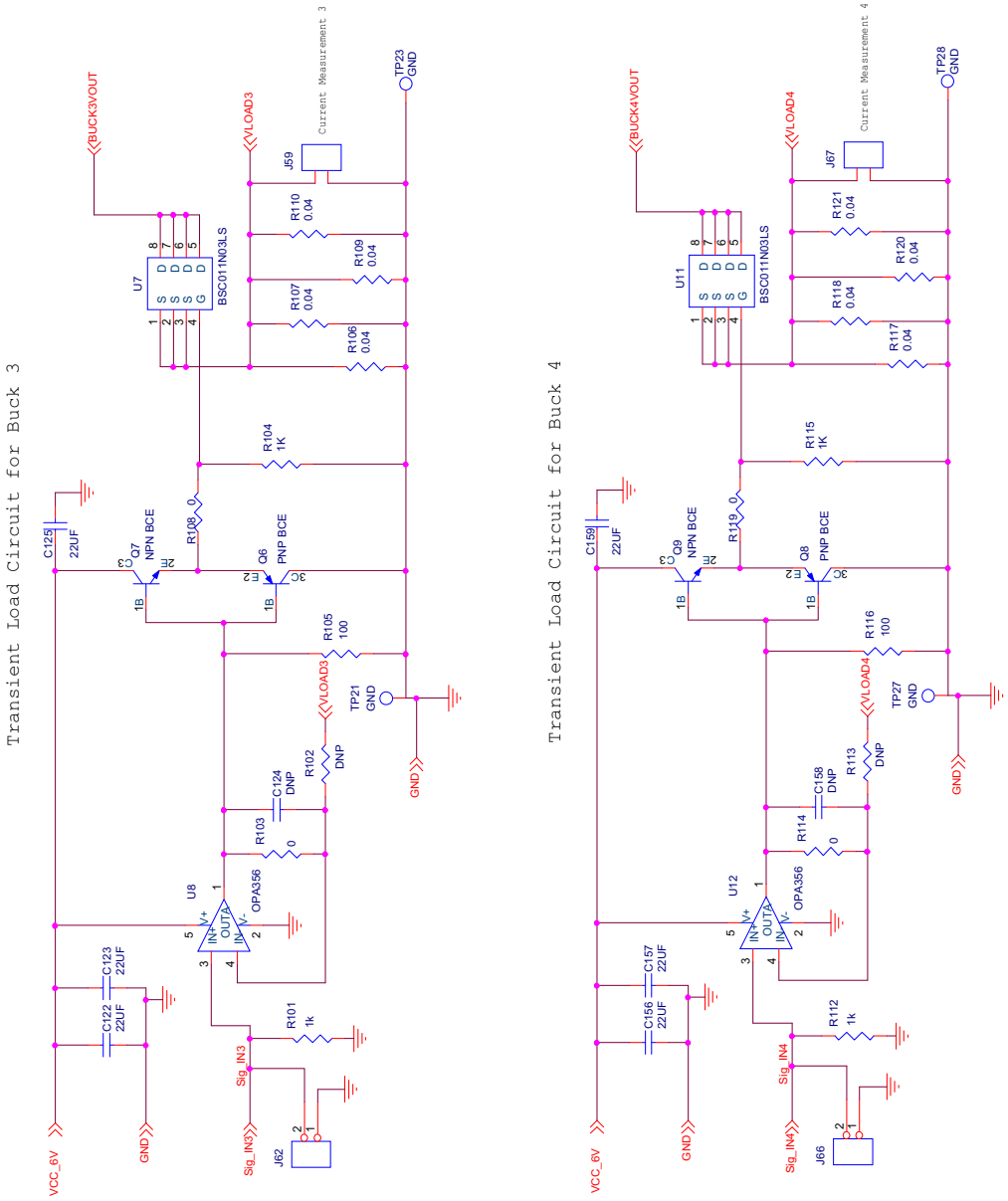

Figure 17. ISL91212BEVAL1Z Schematic - Page 3

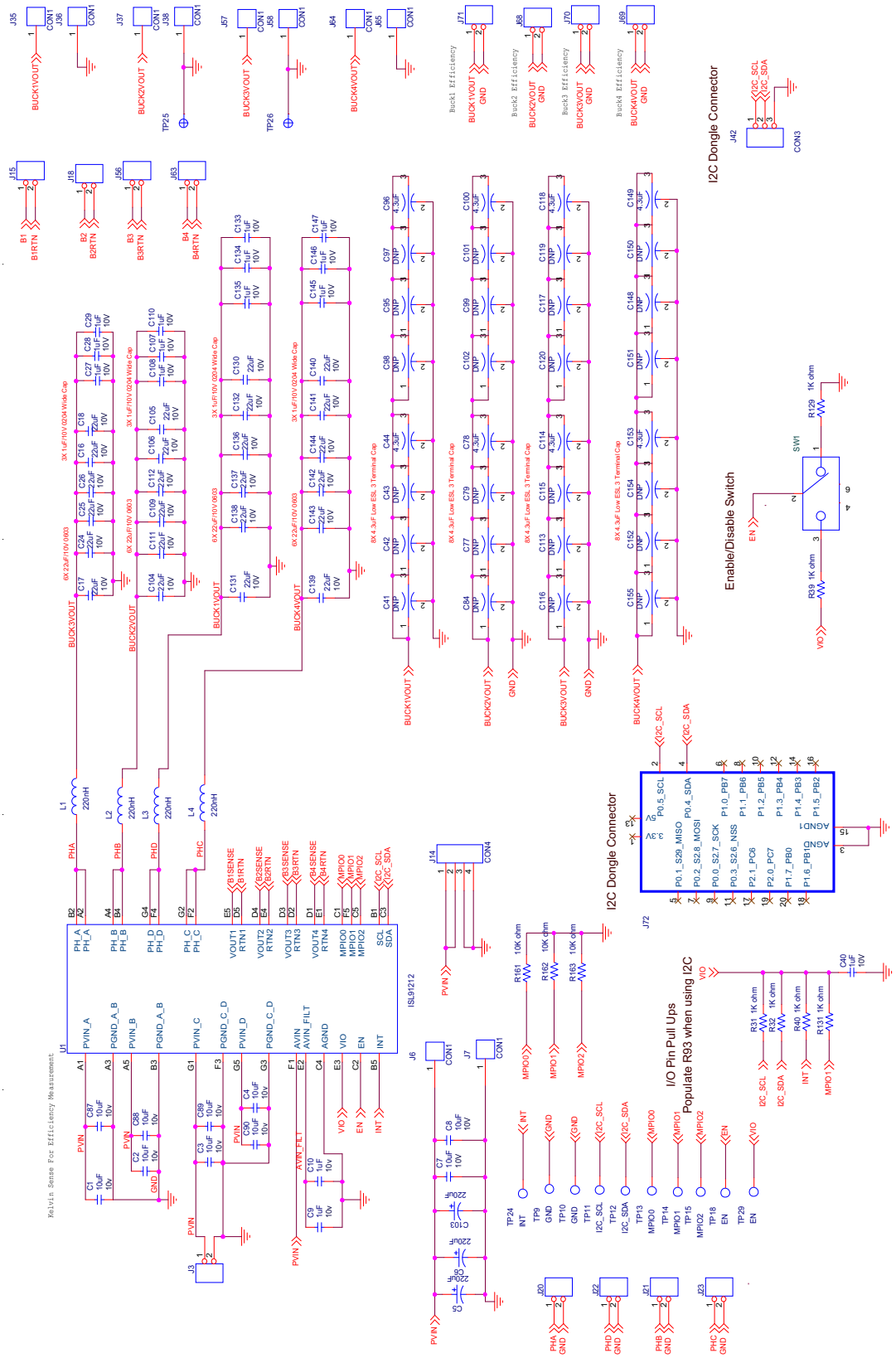

Figure 18. ISL91212BEVAL1Z Schematic - Page 4

1. For the component values in the schematics, see Bill of Materials.

2.4 Bill of Materials

Table 3. ISL91212BEVAL1Z Evaluation Board Bill of Materials

Qty	Top Components	Bottom Components	Description	Part Number	Manufacturer
1	-	C93	82pF, NP0, 0603	QVS107CG820JCHT	Taiyo Yuden
1	-	C92	1000pF, 50V, X7R, 0603	C0603X7R101-102KNE	Venkel
1	C40	-	1µF, 10V, X5R, 0402	GRM155R61A105KE15D	Murata
12	C41, C42, C43, C77, C79, C84, C113, C115, C116, C152, C154, C155	-	4.3µF Multi-Terminal, 4V, X5R, 0402	NFM15PC435R0G3D	Murata
7	C1, C2, C3, C4, C7, C8	C94	10µF, 10V, X5R, 0603	GRM188R61A106ME69D	Murata
1	C10	-	10µF, 10V, X5R, 0402	CL05A106MP5NUNC	Samsung Electronics
25	C17, C24, C25, C59, C60, C61, C62, C63, C64, C104, C109, C111, C122, C123, C125, C131, C137, C138, C139, C142, C143, C156, C157, C159	C91	22µF, 10V, X5R, 0603	C1608X5R1A226M080AC	TDK
3	C5, C6, C103	-	220µF, 6.3V, Polymer Tant, D Case	T520D227M006ATE040	Kemet
6	C27, C28, C29, C107, C108, C110	-	1uF,6.3V,X5R,0204	JWK105BJ105MP-F	Taiyo Yuden
20	R53, R62, R91, R92, R103, R108, R114, R130	R73, R74, R77, R80, R82, R84, R95, R97, R100, R124, R125, R128	0Ω, 1/10W, 0603	CR0603-10W-000T	Venkel
1	-	R87	RES SMD 0.0Ω JUMPER 3/4W 2010	RMCF2010ZT0R00	Stackpole
16	R55, R56, R57, R58, R64, R65, R66, R67, R106, R107, R109, R110, R117, R118, R120, R121	-	0.04Ω, 1%, 1W, 2010	CSRN2010FK40L0	Stackpole
4	R52, R61, R105, R116	-	100Ω, 1%, 1/10W, 0603	CR0603-10W-1000FT	Venkel
14	R31, R32, R39, R40, R54, R63, R104, R115, R129	R72, R89, R90, R101, R112	1.0kΩ, 1%, 1/10W, 0603	ERJ-3EKF1001V	Panasonic
1	-	R71	2.61kΩ, 1%, 1/10W, 0603	CR0603-10W-2611FT	Venkel
4	R161,R162,R163	R70	10kΩ, 1%, 1/10W, 0603	CR0603-10W-1002FT	Venkel
4	L1, L2, L3, L4	-	0.22µH, 10mΩ, 6.6A, 2520 Inductor	PIFE25201T-R22MS	Cyntec
4	Q1, Q4, Q7, Q9	-	Trans NPN 40V 0.2A SOT-23	MMBT3904	Fairchild
4	Q2, Q5, Q6, Q8	-	Trans PNP 40V 0.2A SOT-23	MMBT3906	Fairchild
10	J6, J7, J35, J36, J37, J38, J57, J58, J64, J65	-	Conn Banana Jack Threaded 12AWG	108-0740-102	Cinch Connectivity

Table 3. ISL91212BEVAL1Z Evaluation Board Bill of Materials (Cont.)

Qty	Top Components	Bottom Components	Description	Part Number	Manufacturer
21	TP1, TP2, TP3, TP4, TP5, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP18, TP21, TP23, TP24, TP27, TP28, TP29	-	Conn-Gen, Compact Test Point, Vertical, White	5002	Keystone
21	J3, J15, J18, J20, J21, J22, J23, J52, J55, J56, J59, J60, J61, J62, J63, J66, J67, J68, J69, J70, J71	-	2 Pin Header, 100 mil spacing	77311-118-02LF	FCI
1	J42	-	3 Pin Header, 100 mil spacing	61300311121	Wurth
1	J14	-	4 Pin Header, 100 mil spacing	61300411121	Wurth
1	J72	-	Right angle connector	M50-3901042	Harwin Inc.
1	SW1	-	Switch-Toggle, SMD, 6 Pin, SPDT, 2POS, On-None-On, RoHS	GT11MSCBE	ITT Industries/ C&K Division
1	U1	-	ISL91212B, 6x9 0.4mm Pitch WLCSP	ISL91212	Renesas
4	U2, U3, U8, U12	-	IC OPAMP VFB 200MHZ RRO SOT23-5	OPA356AIDBVR	Texas Instruments
1	-	U4	IC REG LDO ADJ 1A 10DFN	ISL80101IRAJZ	Renesas
4	U5, U6, U7, U11	-	MOSFET N-CH 30V 100A PG-TDSON-8	BSC011N03LSCT-ND	Infineon
0	C44, C78, C87, C88, C89, C90,C95, C96, C97, C98, C99, C100, C101, C102, C114, C117, C118, C119, C120, C148, C149, C150, C151, C153	C9	Capacitor, 0402, DNP	Any	Any
0	C133, C134, C135, C145, C146, C147	-	Capacitor, 0204, DNP	Any	Any
0	C16, C18, C26, C85, C86, C105, C106, C112, C124, C130, C132, C136, C140, C141, C144, C158	-	Capacitor, 0603, DNP	Any	Any
0	R68, R69, R86, R94, R96, R98, R99, R102, R113, R131	R75, R76, R78, R79, R81, R83, R85, R86, R122, R123, R126, R127	Resistor, 0603, DNP	Any	Any

2.5 Board Layout

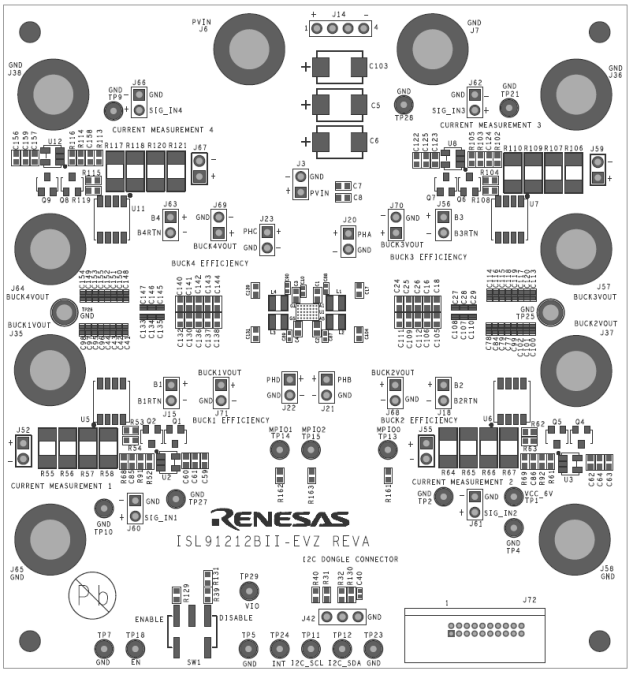

Figure 19. Top Silkscreen Layer

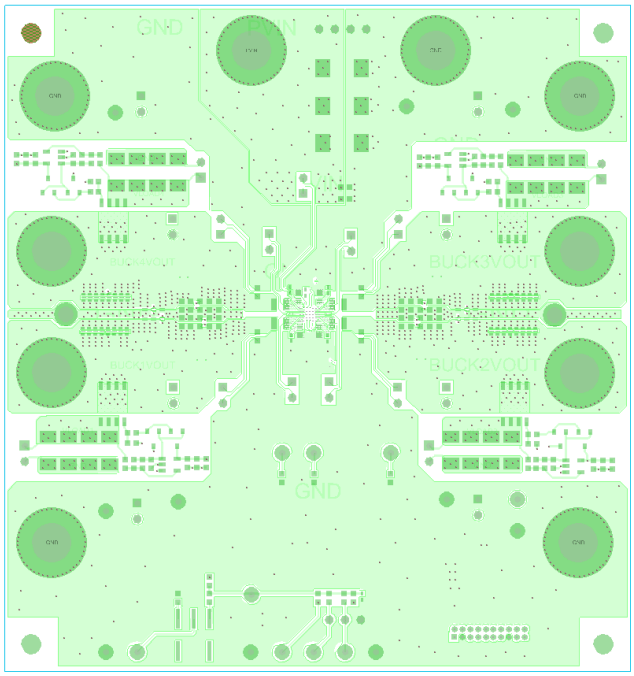

Figure 20. Top Layer

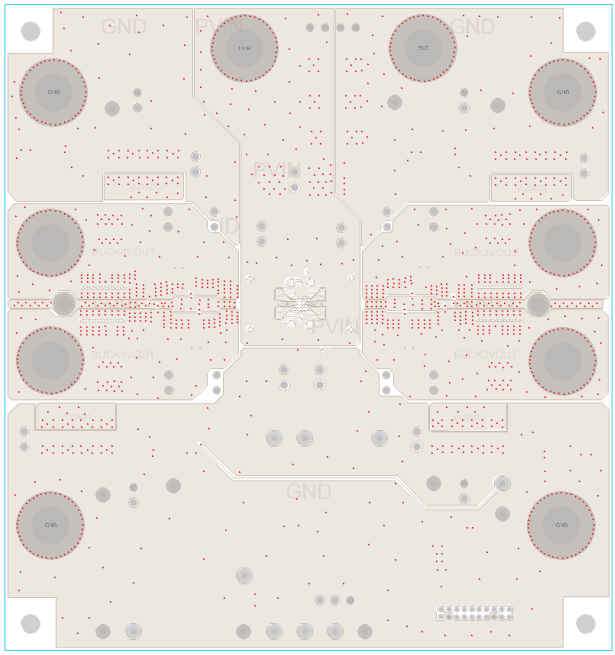

Figure 21. Layer 2 (PVIN Plane)

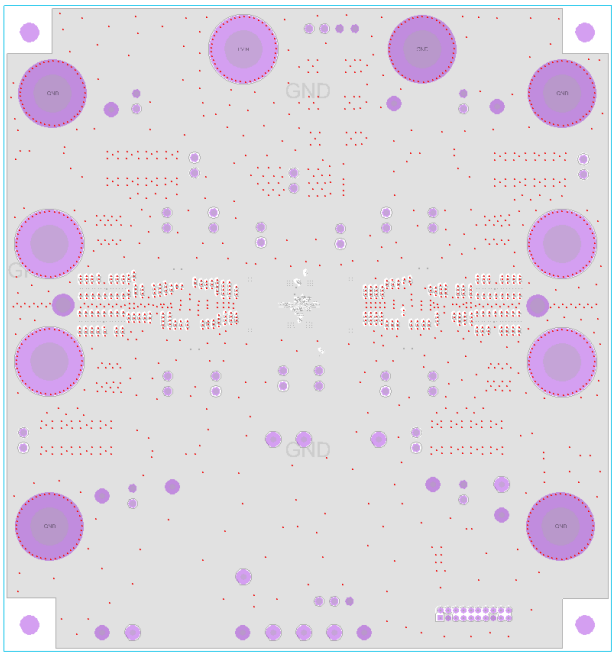

Figure 22. Layer 3 (GND Plane)

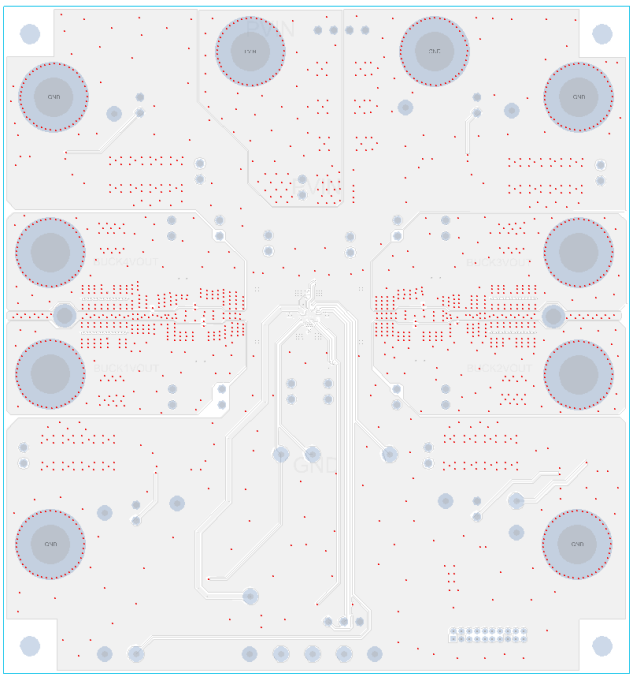

Figure 23. Layer 4 (IO Communications)

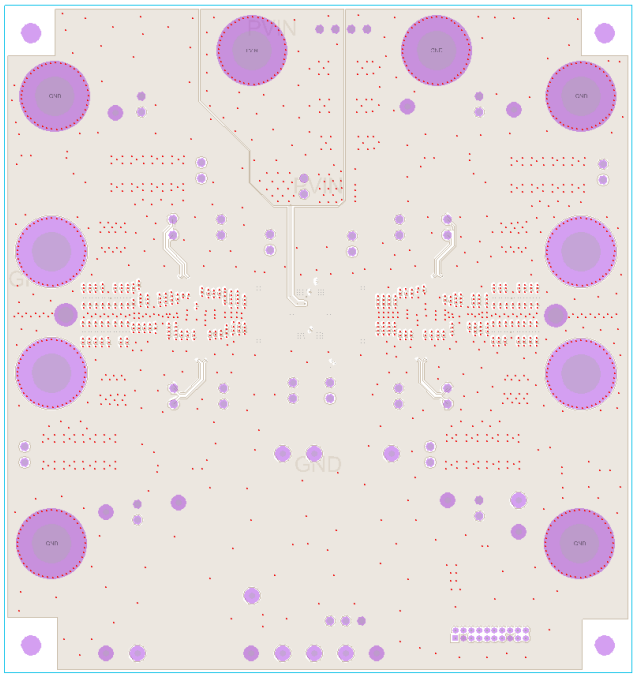

Figure 24. Layer 5 (GND Plane)

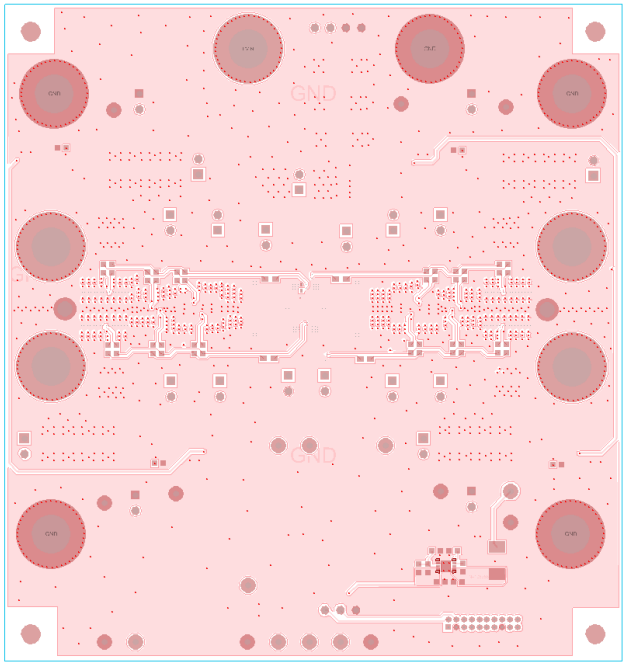

Figure 25. Bottom Layer (Remote Sense Lines)

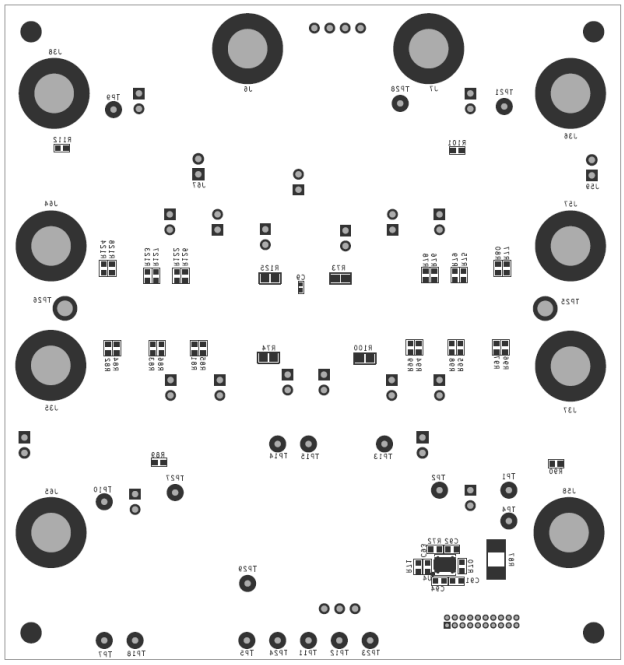

Figure 26. Bottom Silk Screen Layer

3. Typical Performance Curves

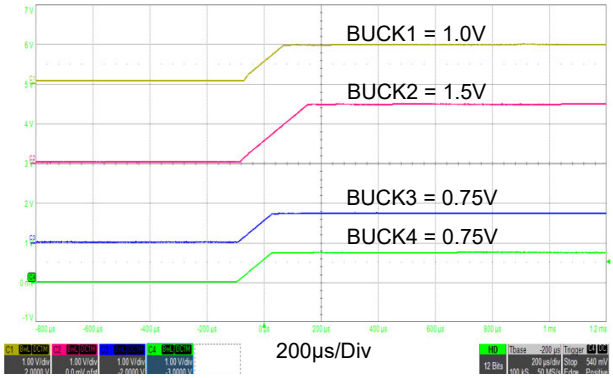

Figure 27. Startup by EN Pin

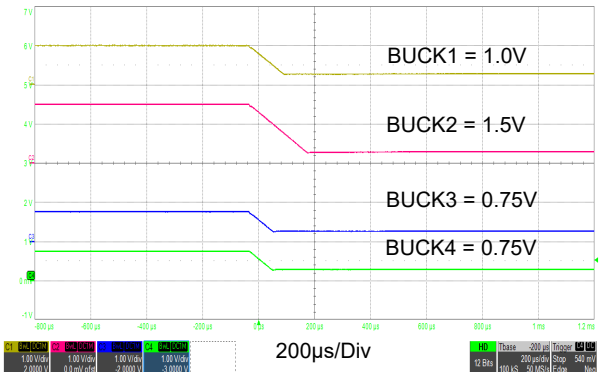

Figure 28. Shutdown by EN Pin

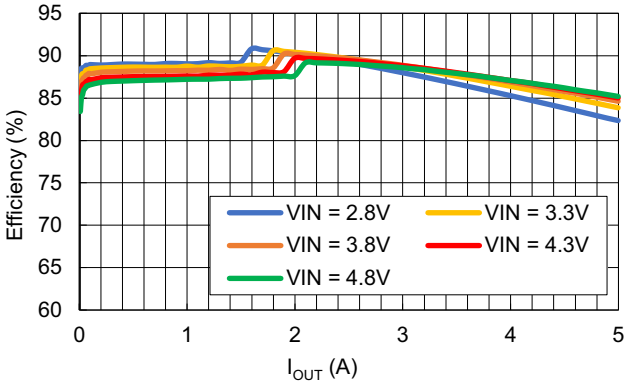

Figure 29. Efficiency (V_{OUT} = 1V), Continuous Load Sweep (0.1A to 5A), f_{sw} = 2MHz

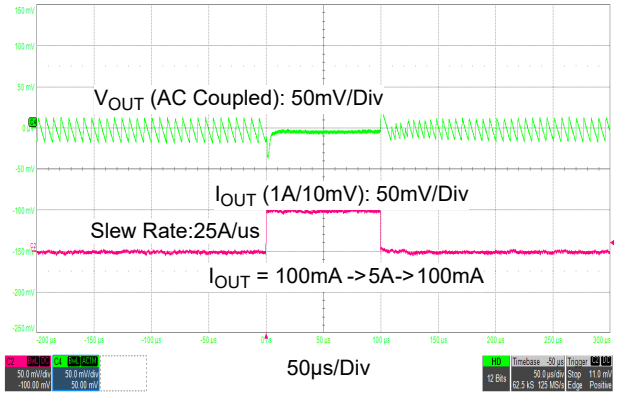

Figure 30. Load Transient(5A/200ns) V_{IN} = 3.8V, V_{OUT} = 1V Load Step Slew Rate = 25A/µs, 0.1A to 5A

4. Ordering Information

Part Number	Description
ISL91212BEVAL1Z	ISL91212B evaluation board

5. Revision History

Rev.	Date	Description
2.00	Jun 28, 2023	Applied new template. Updated Figures 2, 3, 11-14, 19-28, and 30. Updated description for Buck outputs and deleted the GUI figure with Enable/Disable switch in section Measuring Efficiency. Updated description for GUI installation and DVS pointer selection in section Installing and Using the Evaluation Software. Removed main components value in section PCB Layout Guidelines. Added note to schematics. Updated Bill of Materials
1.00	Nov 15, 2018	Initial release

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