P9415-R-EVK Evaluation Kit

The P9415-R-EVK Wireless Power Evaluation Board serves to demonstrate the features and performance of the 9415-R 15W Wireless Power Receiver with WattShare™ mode. The P9415-R-EVK is designed for evaluation purpose only. It must not be used for module or mass production purposes.

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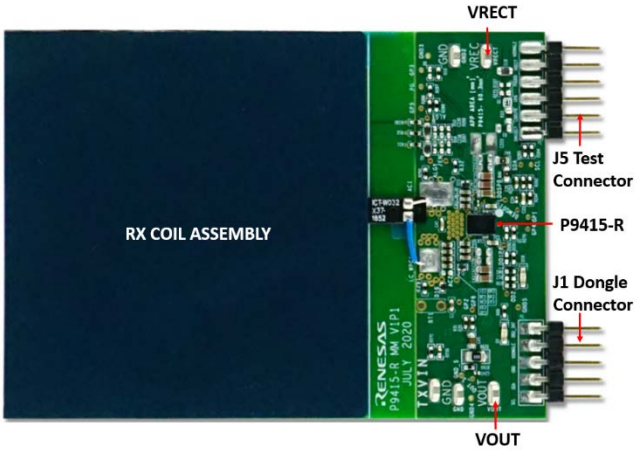
1. Features

- Receives up to 15W of power from Qi Extended Power Profile (EPP) Transmitter
- Transmits up to 5W of power in WattShare™ (TRx) mode
- WPC1.2.4 Extended Power Profile (15W) compatible
- WPC 1.3 Specification hardware ready
- Up to 87% system efficiency in Receiver mode
- Uses thin profile receiver coil (0.3mm)
- Score line to break the applications circuit for prototyping
- Easy configuration of design parameters using P9415-R Windows GUI
- Connector compatible with “WPD-USB-DONGLE” USB to I2C dongle
- 4-layer PCB with 1 oz. copper
- Extensive support collateral: Schematics, Layout files, BOM
- Supports Bi-Directional communications
- X-Y alignment coils embedded in the PCB
- Embedded 32-bit ARM® Cortex®-M0 processor
- Supports I2C 400kHz standard interface and GPIOs

2. Evaluation Kit Contents

- P9415-R Evaluation Board assembled with Coil



3. Overview

The P9415-R-EVK Wireless Power Evaluation Board serves to demonstrate the features and performance of the 9415-R 15W Wireless Power Receiver with WattShare™ mode. Renesas P9243-GB-EVK Evaluation Board or any other Qi certified Extended Power Profile (EPP) transmitter can be used as the power transmitter for P9415-R-EVK Evaluation Board testing.

The P9415-R-EVK demonstrates a high-efficiency, turnkey reference design supported by comprehensive online, digital resources to significantly expedite design-in effort and enable rapid prototyping.

Using the P9415-R Windows GUI customers can quickly customize operating parameters for their custom applications. Operating parameters such as foreign object detection (FOD) parameters can be configured by either writing to internal SRAM registers via the I2C interface, or by loading a custom configuration generated by the P9415-R Windows GUI into The P9415-R features Multiple-time programmable (MTP) non-volatile memory. WPD-USB-DONGLE is required to connect P9415-R-EVK with the windows GUI and needs to be ordered separately.

4. Setup

4.1 Required or Recommended User Equipment

The following additional lab equipment is required for using the kit:

- P9243-GB-EVK Evaluation Board or any WPC certified transmitter for Rx mode test
- DC power source or travel adapter to power P9243-GB-EVK Evaluation Board or any WPC certified transmitter
- P9222-R-EVK or any WPC certified receiver for Watt-share (Tx) mode test
- Electronic load that can be connected to P9415-R-EVK
- WPD-USB-DONGLE for connecting with P9415-R Wireless Power Pro GUI on computer and doing I2C transactions. WPD-USB- DONGLE is not shipped along with evaluation board and needs to be ordered separately

4.2 Required Software on Computer

Visit the P9415-R-EVK webpage and download latest version of the P9415-R Wireless Power Pro GUI, and USB drivers from the Renesas website. The Window GUI software provides an intuitive graphical user interface for reading and writing to P9415-R registers and program custom user configurations to internal MTP memory.

4.2.1. Software Installation

Follow these procedures to install the software:

1. Do not connect the WPD-USB-DONGLE before installing the software.
2. Run the downloaded USB Drivers Setup executable file and follow the user prompts to install the USB drivers.
3. After finishing the setup of the USB drivers, connect one of the WPD-USB-DONGLE to the USB port. Wait for a few moments to let Windows® map the drivers for the dongle.
4. Open the Device Manager from the Windows control panel and check the devices listed under “Universal Serial Bus controllers” section. “FT4222H Interface A” and “FT4222H Interface B” should appear in this section as shown in Figure 1.
5. Run the P9415-R Window GUI exe file.

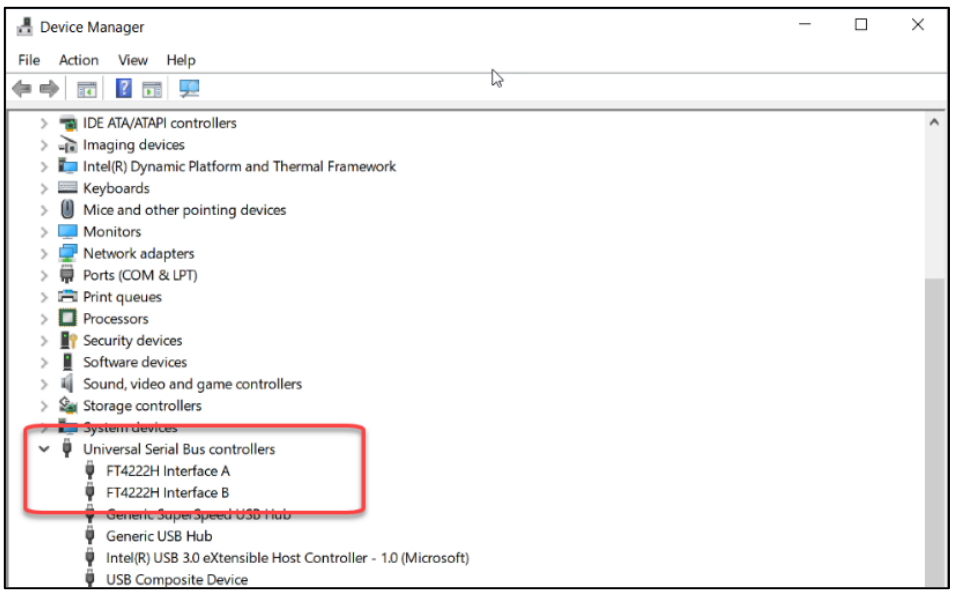


Figure 1. Windows Device Manager Display for the USB Connection

4.3 Usage Guide

The P9415-R Evaluation board allows for demonstration of the performance and functionality of the P9415-R device in a lab bench test environment. For complex or electrically sensitive situations, it is recommended to use the reference layout to integrate this design into the final system to eliminate hardware limitations or signal degradation introduced by long leads.

4.4 Kit Hardware Connections for Rx Mode

Follow these procedures to set up the kit as shown in Figure 2.

1. Set up the P9243-GB Evaluation Board (or other transmitter board) according to the board's user manual and apply power.
2. Place the P9415-R-EVK Board on the transmitter coil surface with the coil back facing upwards. P9415-R-EVK PCB boards act as a spacer between Tx surface and Rx coil.
3. Verify that the green LEDs on both kits are illuminated, indicating that power transfer has been established.

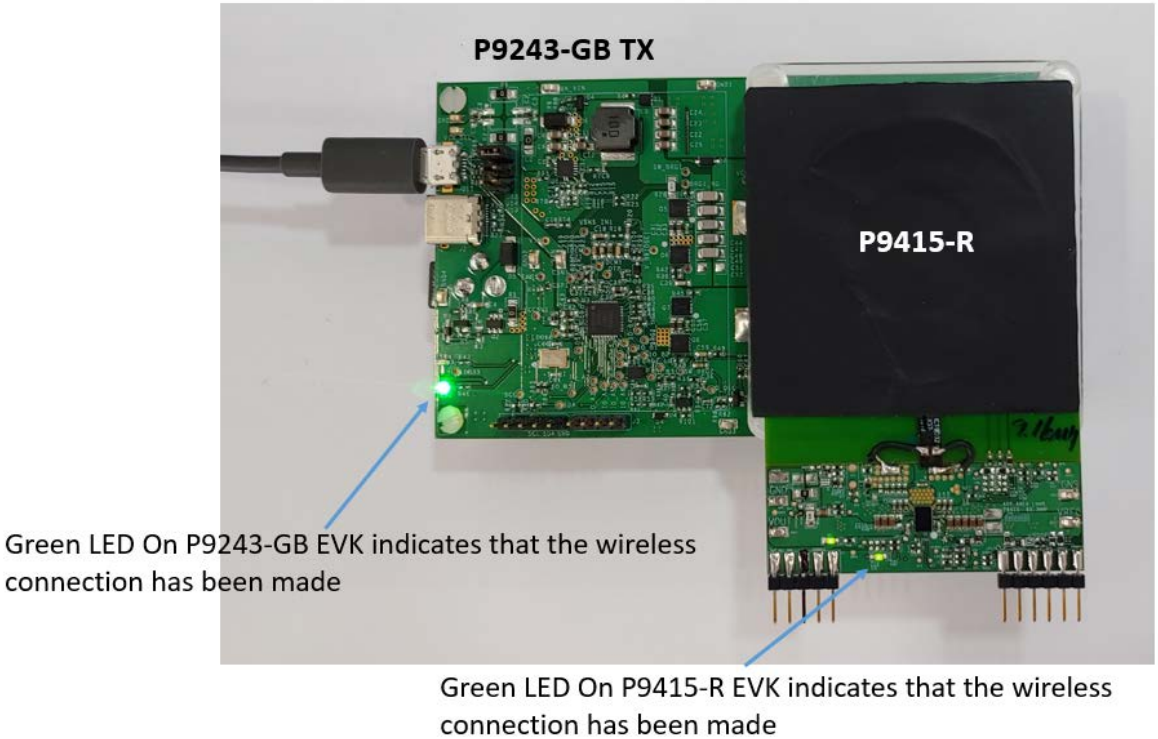


Figure 2. Evaluation Kit Connections for Rx Mode Test (1)

4.4.1. Start Guide for Rx Operation

Place the bottom side of P9415-R EVK onto P9243-GB Tx or other WPC certified Tx unit. P9415-R EVK includes a 58 × 58 × 0.3 mm TRx coil assembly. The charging pad may be a pre-powered and may be powered after placing the Rx coil on Tx charging pad.

Verify that green LED on P9415-R is illuminating and measure Rx output voltage at the VOUT test point to ground (GND). Up to 1A load may be connected between VOUT and the GND terminals. For convenience and measurement accuracy, two test points have been placed which allow for kelvin voltage sensing of the output voltage to omit conduction losses during evaluation (VOUT and GND). These should be utilized when performing efficiency measurements. The I2C dongle connector J1 can be used to interface with WPD-USB-DONGLE dongle for programming the user configurable design parameters and it can be used to monitor the system status, mode, operating frequency, voltage and current.

4.5 Kit Hardware Connections for Wattshare (Tx) mode

Follow these procedures to set up the kit as shown in Figure 3.

1. Supply power on P9415-R-EVK VOUT with DC power supply (7.0V).
2. Connect USB dongle on P9415-R-EVK J1 connector. USB dongle black line (GND) should be on J1 Pin3.
3. Send Tx mode command with P9415-R Wireless Power Pro GUI (write 0x01 on 0x0076 register).
4. Place the P9222-R-EVK Board or WPC certified receiver on the reverse side of P9415-R-EVK.

   P9415-R-EVK PCB boards acts as a spacer between Tx surface and Rx coil.
5. Verify that the green LEDs on P9222-R-EVK is illuminated, which indicates that power transfer has been established.

Figure 3. Evaluation Kit Connections for Rx Mode Test (2)

4.5.1. Start Guide for Wattshare Tx mode Operation

The P9415-R-EVK can be configured as a wireless power transmitter. The device uses an on-chip full/half-bridge inverter, a PWM generator, a modulator/demodulator for communication, and a microcontroller to produce an AC power signal to drive external L-C tank to operate as a wireless power transmitter (TRx). The P9415-R-EVK uses the same L-C tank in both Rx mode and TRx mode. In TRx mode, the power needs to be applied on the VOUT pin first which is the same node as the power receiver output when the device operates in Rx Mode. Ensure that P9415-R-EVK is not on the Tx pad to avoid Tx conflict.

1. Supply power (5V – 9V) on P9415-R-EVK VOUT or Tx VIN Test point.
2. Write 0x0001 data to 0x0076 register to enable TRx mode with Renesas GUI or any other I2C tool.
3. P9415-R-EVK starts sending digital pings after enabling TRx mode. Probe AC1 and check digital ping waveform.

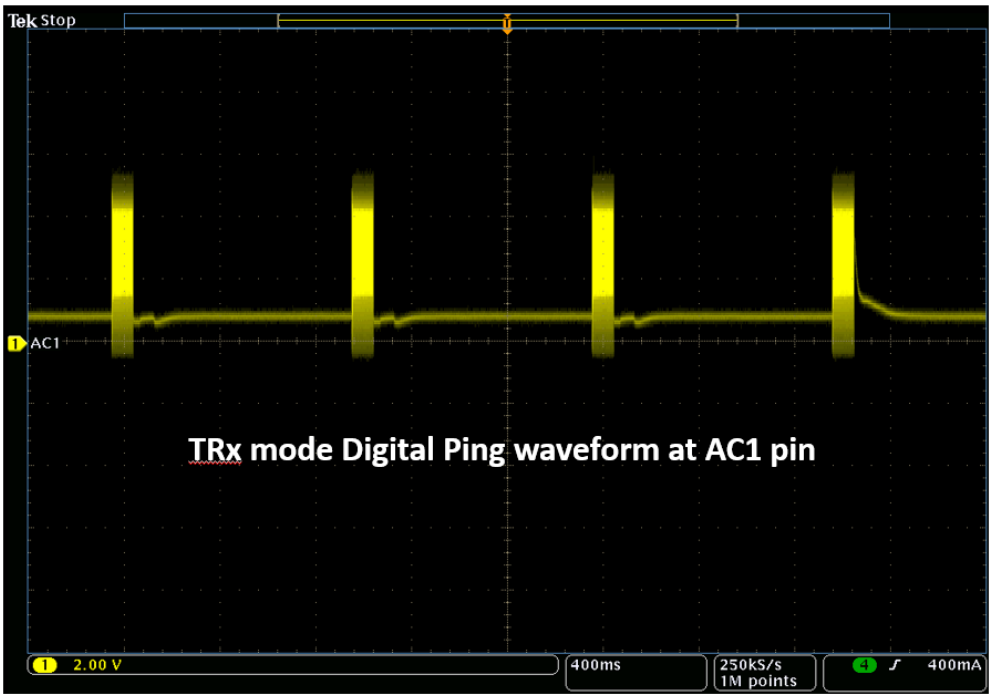


Figure 4. TRx Mode Digital Ping Waveform

4. Place WPC compliant Receiver on P9415-R-EVK TRx coil. P9415-R will detect Rx device and start power transfer right after WPC ID and Configuration packet.

   Probe Rx VRECT and Rx VOUT and check if charging is functional.

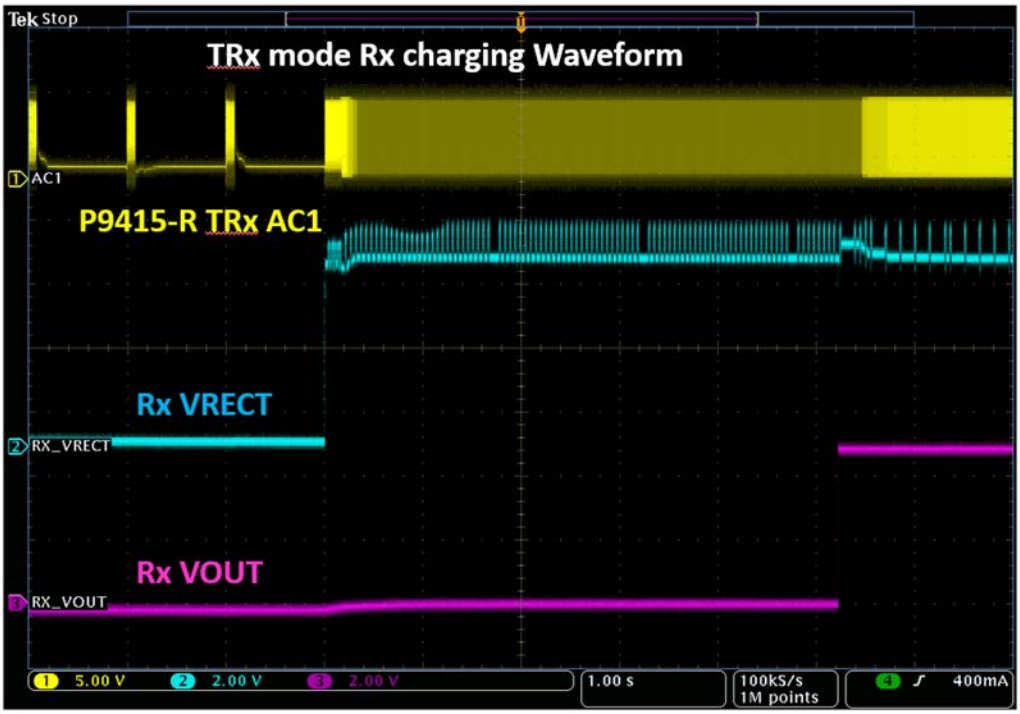


Figure 5. TRx Mode Rx Charging Waveform

5. TRx default digital ping frequency is 145kHz and the normal operating frequency range is from 130kHz to 145kHz in the default configuration. It can be changed to 110kHz – 148kHz using the P9415-R GUI.

4.5.2. Wattshare™ Tx Mode Input Voltage

The P9415-R can transfer up to 5W of power in TRx mode. It follows the WPC 1.2.4 BPP protocol to transfer the power to other Qi-certified receivers such as Mobile devices, wearables and hearables. The maximum power delivered in TRx mode is dependent on the input voltage on VOUT pin, coil characteristics such as AC resistance, and the friendly metal around the coil. Because the coil used for power transfer in TRx mode has high AC resistance compared to transmitter coil used in a charging pad, the input voltage on the VOUT pin in TRx mode must be around 7V to 9V to deliver 5W of power to the receiver.

5. P9415-R Evaluation Board Test Point and Connector

There are many test points placed around P9415-R EVK PCB board that can be used for quick and easy evaluation of P9415-R performance. VOUT, VRECT and GND have large size test points for easy test cable connection for supplying power and loading. J1 and J5 are the pin type connector for USB-I2C bridge dongle interface connection and system configuration and monitoring.

5.1 P9415-R Evaluation Board Test Point Placement

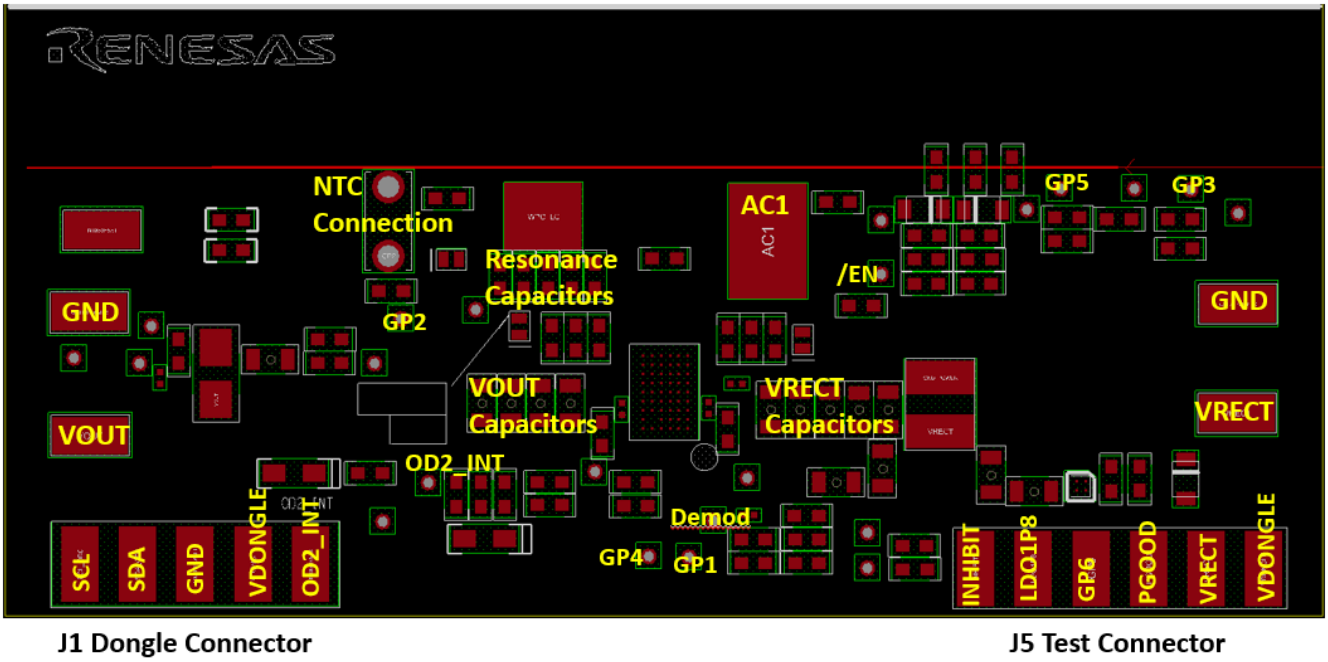


Figure 6. Evaluation Board Test Point Placement

5.1.1. J1 Dongle Connector Pin Descriptions

Table 1. J1 Dongle Connector Pin Descriptions

Pin Number	Name	Type	Description
1	SCL	Input	I2C Interface Clock signal.
2	SDA	Input /Output	I2C Interface Data signal.
3	GND	Power	Ground reference.
4	VDONGLE	Power	Dongle power supply from USB Dongle cable (optional).
5	OD2_INT	Output	Interrupt Signal from P9415-R. Connect OD2_INT to AP GPIO with PU (optional).

5.1.2. J5 Test Connector Pin Descriptions

Table 2. J5 Test Connector Pin Descriptions

Pin Number	Name	Type	Description
1	INHIBIT	Input	Software Enable Pin, active High.
2	LDO1P8	Power	Internal power regulator 1.8V.
3	GP6	Input	EPP disable, High = EPP disable, Low = EPP enable.
4	PGOOD	Output	Power Good indication output.
5	VRECT	Power	VRECT power supply from USB dongle (optional).
6	VDONGLE	Power	Dongle power supply from USB dongle (optional).

6. Hardware Connections–Renesas USB-I2C Dongle to Window GUI

The P9415-R firmware provides great flexibility to customize operating parameters for custom applications. Default values of the P9415-R operating parameters such as output voltage, FOD parameters, and current limit are set in the firmware programmed into the internal multi-time programmable (MTP) memory. Based on the end application, the P9415-R operating parameters can be configured by either writing to internal SRAM registers or program parameter permanently to internal MTP memory via the I2C interface.

Connect the USB-Bridge dongle to PC via USB connector. Attach the Bridge to the I2C terminal J1 dongle on the P9415-R EVK DEMO board as shown on Figure 8. The dongle should only be plugged-in in one direction, extending away from the P9415-R EVK PCB, and dongle cable black line (ground) should be connected in J1 Pin3 GND.

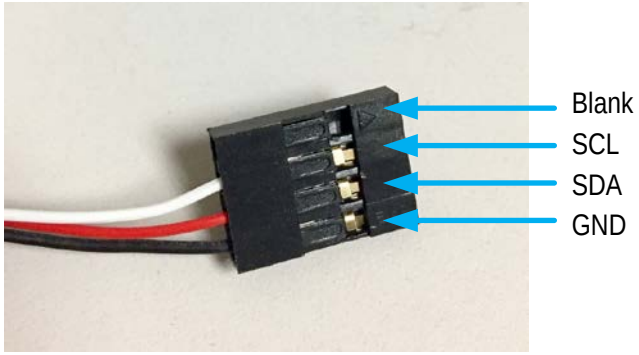


Figure 7. USB to I2C Dongle Header of “USB-FTDI-V2-1” (FTDI) Dongle

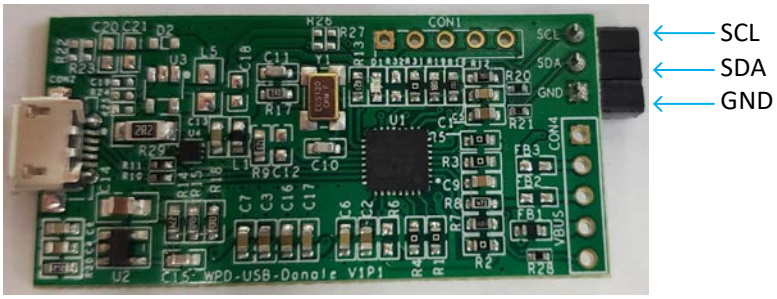


Figure 8. USB to I2C Dongle Header of "WPD-USB-DONGLE"

Figure 9. USB-I2C Bridge Connected to I2C Terminal J1 of P9415-R EVK Demo Board; USB Cable

To access the device, connect USB-Bridge dongle to P9415-R as shown in Figure 8 and follow below procedures.

1. Ensure the USB drivers and P9415-R Wireless Power Pro GUI tool are installed successfully in PC.
2. Place P9415-R-EVK on WPC TX or apply 5V DC from GND connection to the VOUT test point without Tx.
3. Connect WPD-USB-DONGLE to J1 of P9415-R-EVK.
4. Open GUI program. Initial GUI screen is in Figure 9 and the user is prompted to select I2C address.
5. P9415-R default I2C address is 0x3B. Click connect button. If dongle connection is made successfully, P9415 will be displayed in GUI as shown in Figure 10.
6. If P9415 is not displayed in GUI, check if P9415-R-EVK is powered on properly and plug USB cable again.

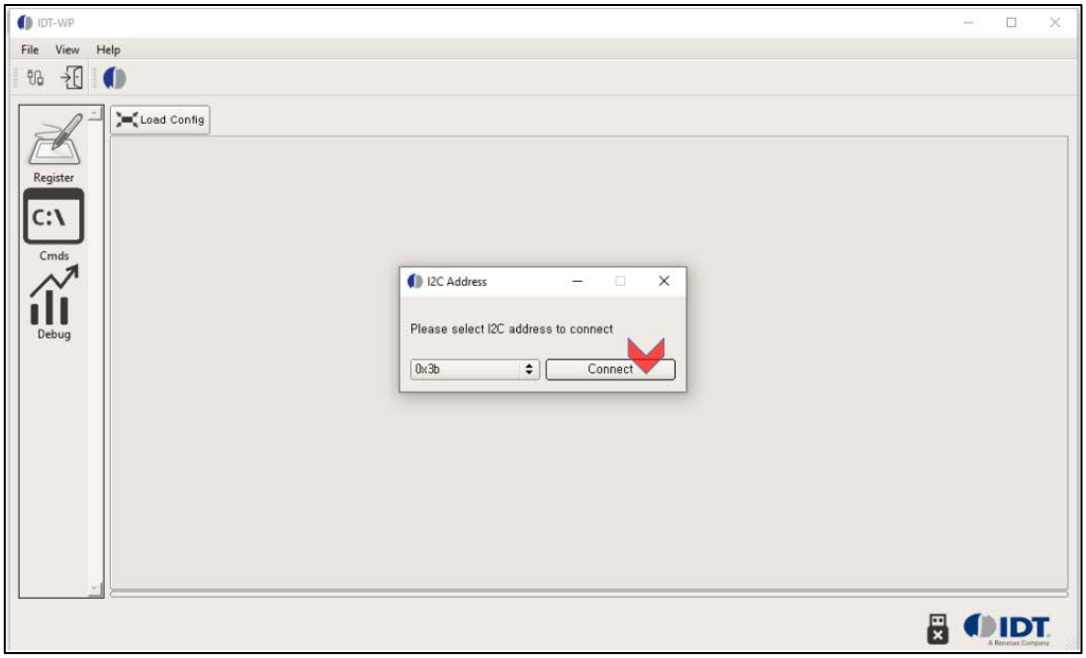


Figure 10. Initial Screen of P9415-R GUI

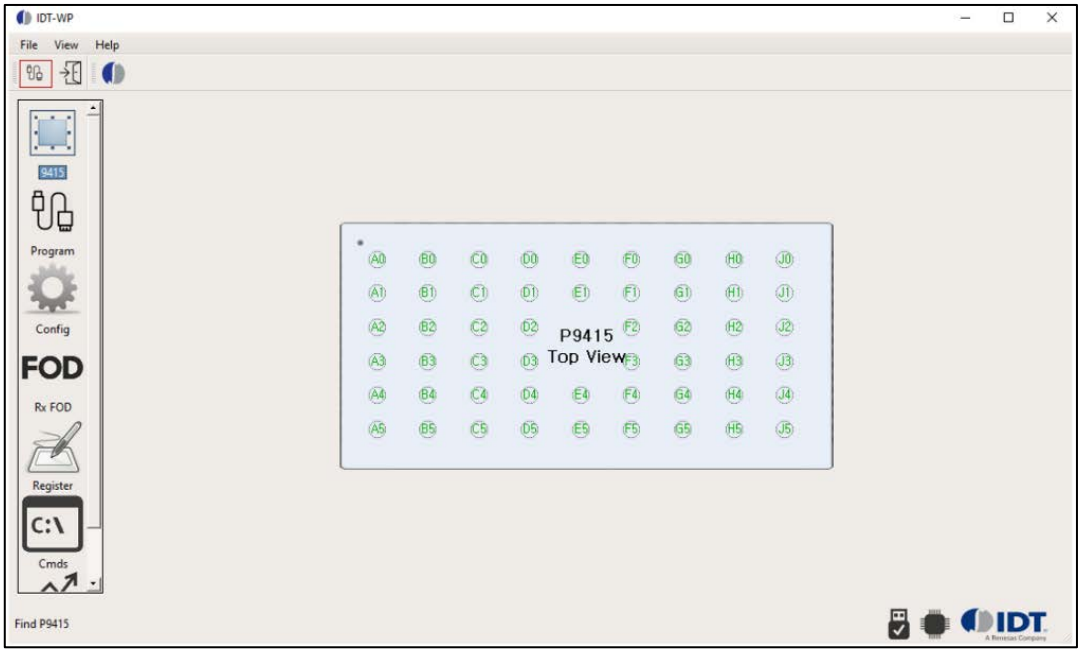


Figure 11. Successful Connection GUI Screen

6.1 Using the Windows GUI

There are many functions in GUI for user to access system operation information, update FW, and modify configurable parameters.

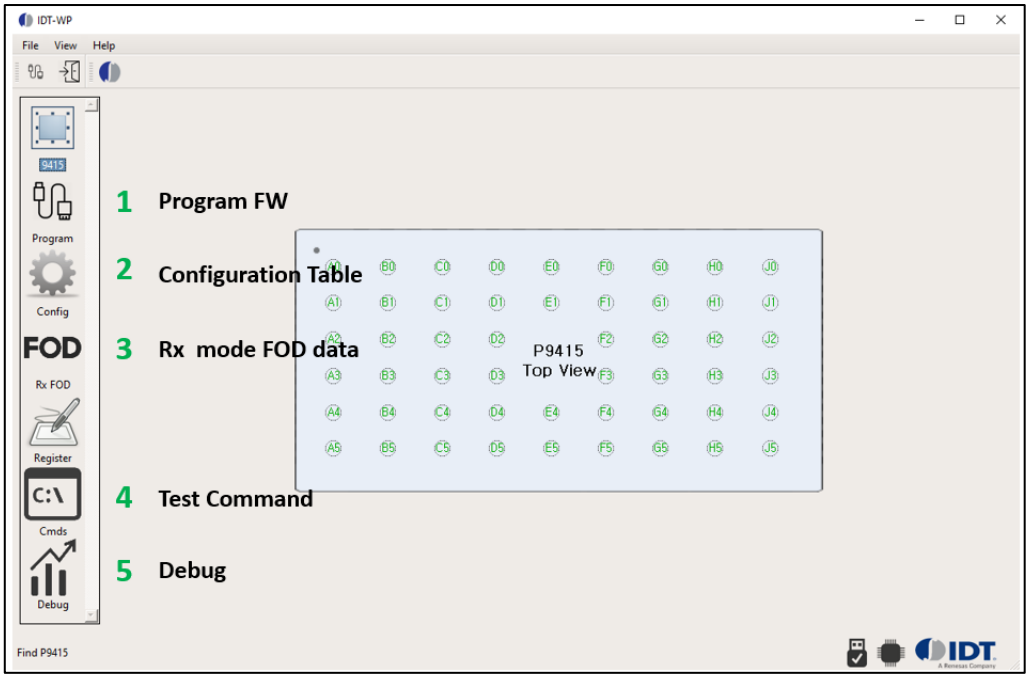


Figure 12. GUI Function Screen

1. **Pr**ogram FW button. Update the FW with this function. Click and see the FW program command window in bottom of the GUI. First select the target FW to update and click Program MTP, then FW will be updated.

   Note: For programming the new firmware to the P9415-R device, remove the P9415-R-EVK from the transmitter pad. Power the device from an external 5V–7.5V power source on VOUT test point of P9415-R-EVK.

2. **Configuration Table**. With table Rx BPP, Rx EPP and Tx operation parameters can be read and saved in internal MTP memory after modification.

   Place P9415-R on Tx pad to make it powered on or supply 5V–7.5V directly on P9415-R VOUT without Tx and then click Read Default Parameters in top side of GUI configuration table. Several sections of default parameters will be displayed on GUI such like Tx, Rx EPP and Rx BPP mode parameters.

   If there is any parameter you want to make a change, update the value and click Configure parameters to MTP, then new value will be saved in internal MTP. New parameters will be applied from next time wireless charging operation after saving. You can also save your configuration table in your local drive Save *Config Table* and *Read Customer Config Table* button on top side of GUI configuration table.

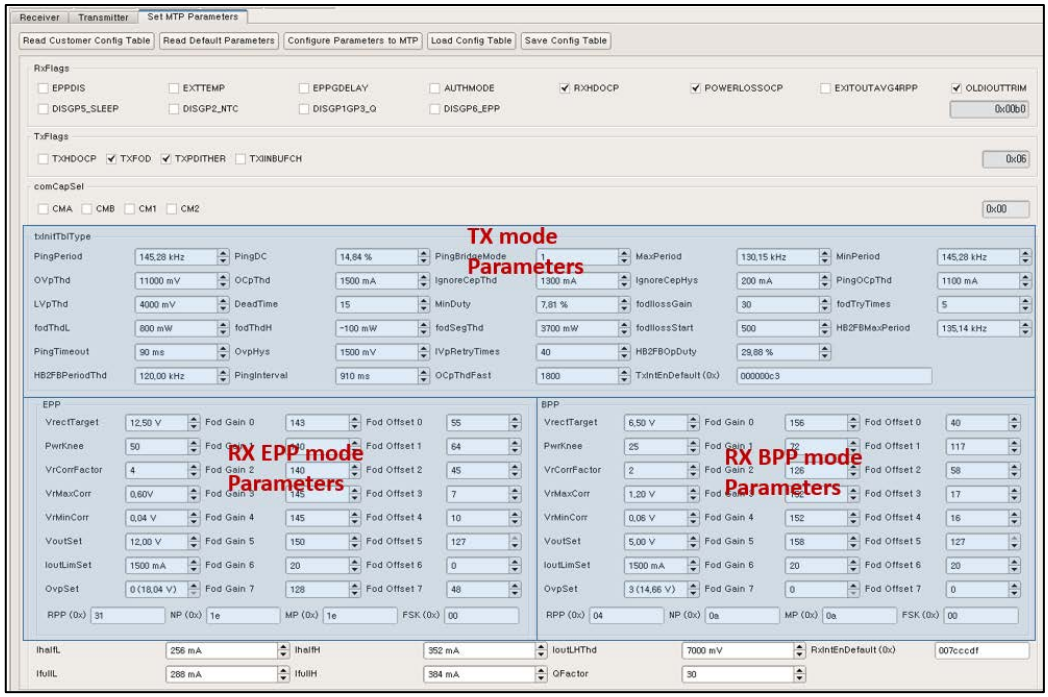


Figure 13. Configuration Parameter Table

3. **RX Mode FOD Data**. This function displays FOD gain and offset data on GUI. Click *Get All* button to view FOD parameters in running Rx mode. Rx BPP and EPP mode may have different FOD parameters. You can change FOD parameter values during running FOD test. New value will be applied immediately. Note that parameter value changed here will be lost and return back to default in MTP if there is power loss during the test because this parameter value is volatile and stays in internal SRAM registers.

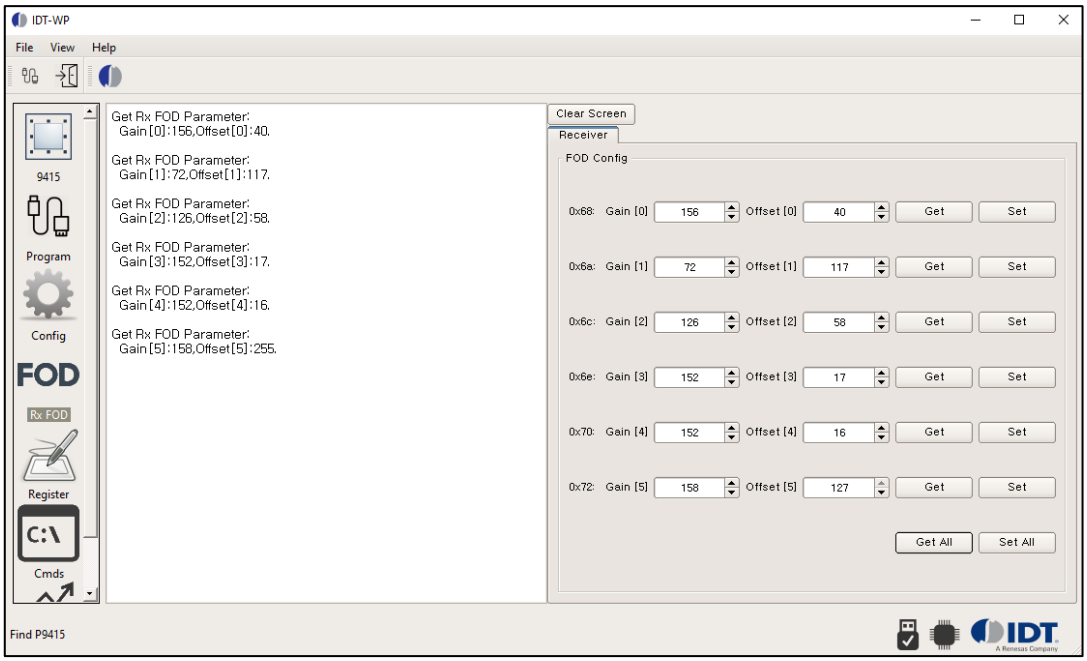


Figure 14. Rx FOD Parameter Data

4. **Test Command**. Use the command script to read and write data to P9415-R register.

   There are several command script examples. For example, if you want to read 2byte data from register address 0x0068, please type in ‘regRead:0068 2’ in blank command block and click Send cmd button, then GUI will return read value in window. If you want to write 2byte data 0x01 and 0xCF into register address 0x0071, please type in ‘regWrite 0071 2 01 CF’ in blank command block and click Send cmd button, then GUI will display write result on window.

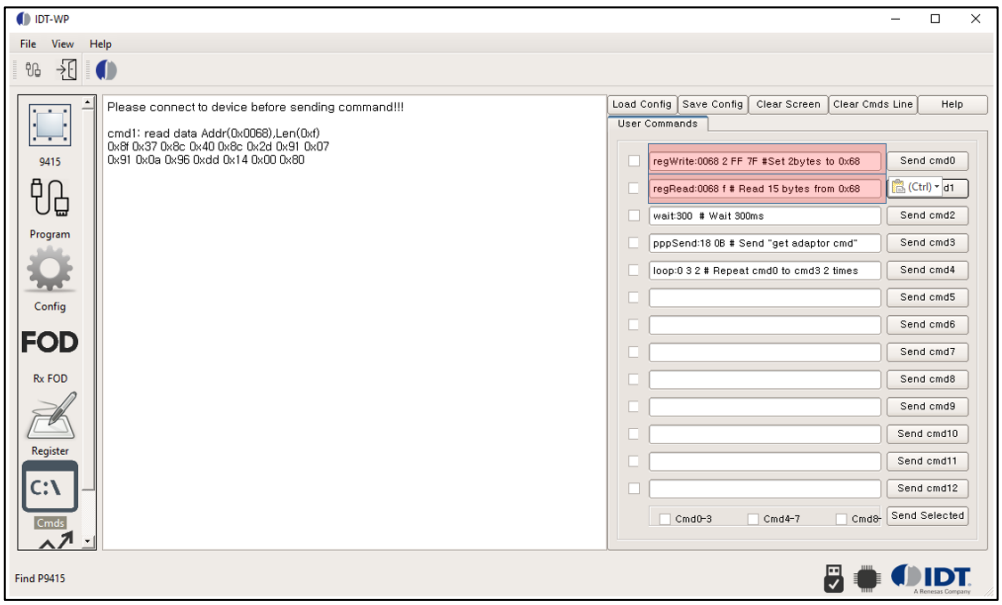


Figure 15. Test Command Window

5. **Debug**. Monitors system operation in regular time base. Below example is configured to read VOUT, VRECT, external temperature NTC and Iout during Rx mode charging. You can set read interval and register address you want to monitor. Different data format is available decimal and hexa. You may want to use formula to convert ADC result into actual voltage or current.

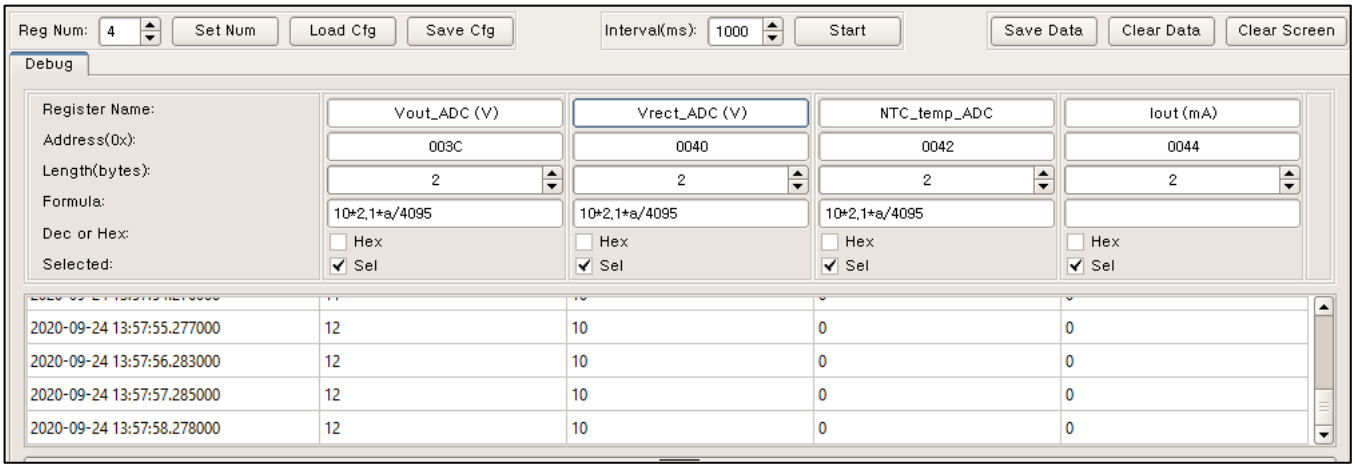


Figure 16. Debug Window

7. TRx Wireless Power Coil

The TRx coil is dependent on customer requirements and most are custom designs. Renesas recommends the following TRx coil as it was installed in P9415-R demo board.

- Ls = 8 to 10µH
- DCR = < 0.3Ω
- ACR = < 0.4Ω

Table 3. Coil Manufacturer

Output Power	Vendor	Part Number	Inductance at 100kHz	Resonant Caps (Cs)	DC Resistance at 20℃
15W	Luxshare	ICTR-QS5858031L-MW034	9.0 ±0.2µH	400nF	195mΩ ±10%

8. Resonance Capacitors

The series resonance capacitors (C32, C33, C34, C36, and C37) are critical components and must be chosen carefully. All current that flows to the load flows through these components plus any current loss in the rectifier AC to DC conversion. The recommended capacitor is the 100nF Murata (GRM155C71H104KE19, X7S, 50V, or GRM155R61H104KE19, X5R, 50V), which have an ESR < 0.1ohms at 100kHz. The GRM155C71H104KE19 capacitor is the best choice based on ESR value and DC bias effects. If another capacitor is chosen, inspecting the ESR vs. Frequency curve of the manufacturer's capacitor datasheet is necessary to compare ESR characteristics as well as the DC bias effects on the capacitor value. Adding non-populated (NP) component placement (C37) is advised if the additional capacitance is needed for a particular Rx coil.

9. PCLAMP Connection

The P9415-R has an internal automatic DC clamping feature to protect the device from events that cause high voltages to occur on the AC or DC side of the rectifier. The clamping engages by the VRECT connection to the PCLAMP pin. The VRECT node must be connected to the PCLAMP pin at all times during Rx mode operation. For greater than 5W operation, the VRECT node is connected to the PCLAMP pin using a 50Ω to 100Ω resistor with greater than 1/4W rating with 2.5x or greater over-power surge capability. For space-constrained designs, the PCLAMP pin can be directly connected to the VRECT node for 5W or lower power operation.

Also, there is an option for external FET and resistor clamping by the use of the ECLAMP_DRV pin which can output 5V to drive the gate of external MOSFET. This output is synchronized with the internal PCLAMP signal. ECLAMP_DRV can provide additional clamping capability as needed and there is no thermal increase in the IC side because clamping energy is consumed in external components.

10. Transient Voltage Suppressors

The Transient Voltage Suppressor (TVS) is an active device that will direct high voltages from the input to ground, thus protecting the wireless power device or other downstream ICs from being exposed to high voltages.

Transient Voltage Suppressor diodes should be added to the design from the AC1 and AC2 nodes to GND or from AC1 to AC2. These components are useful to rapidly limit incoming ESD surges or situations when the TX incoming power exceeds the expected power and VRECT voltage rises above target and Over-voltage protection threshold in less than 10µs to aid in voltage limiting the incoming AC waveforms in conjunction with the PCLAMP power limiting circuitry.

A balance in Reverse Standoff Voltage (VRWM), Clamping Voltage (VCL), Break-down Voltage (VBR) relative to the expected VRECT operating voltage VRECT (be sure minimum VBR is less than maximum operating VRECT value and that VCL is less than VRECT absolute maximum voltage) should be reached.

Table 4. Transient Voltage Suppressors (TVS) Recommendations

V_{MLDO} = 12V D24V0L1B2LP
VRWM = 24V maximum
VBR = 26V minimum at 1mA
VCL = 42V maximum at 1A pp

11. GPIO and GPOD Pins

The P9415-R has general-purpose input-output (GPIO) pins. The OD0-OD4 and GP0-GP6 pins are all multi-functional.OD0-OD4 pins have an open-drained structure and GP0-GP6 pins have a push-pull structure.

11.1 OD0/SCL Pin

The OD0 pin has a digital function open-drain structure. It is assigned to SCL of the I2C function for the serial interface between the AP and the P9415-R. An external pull-up register on the SCL line is required for I2C communication and 1.8V power is pulled up in P9415-R demo board. OD0 can operate up to 5V.

11.2 OD1/SDA Pin

The OD1 pin is set as a digital function open-drain structure. It is assigned to the SDA function of the I2C serial interface bus between the AP and the P9415-R. An external pull-up resistor on the SDA line is required for I2C communication and 1.8V power is pulled up in P9415-R demo board. OD1 can operate up to 5V.

11.3 OD2/INT Pin

The OD2 pin is set as a digital function open-drain structure. It is assigned as the /INT signal for interrupt notification to the AP. /INT pin indicates a major change of states or error modes such as over-current, over-voltage, or over-temperature event. Connect this pin to the AP I/O voltage rail using an external pull-up resistor. The P9415-R drives this pin LOW to notify the AP of status changes.

11.4 OD3/ALIGN_X Pin and OD4/ALIGN_Y Pin

The XY alignment feature allows the P9415-R to sense its relative position to the Tx coil magnetic field center. When used, the XY alignment coils should be connected to pins OD3(X-alignment coil input) and 0D4 (Y-alignment coil input). These signals are internally rectified, filtered, and sensed through the ADC. The ADC values that represent Align X coil signal strength and Align Y coil signal strength can be read in 0x38 and 0x39 registers respectively.

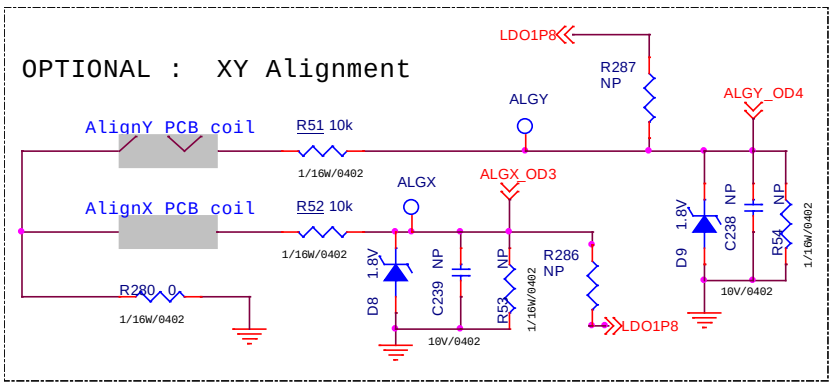


Figure 17. Typical XY Align Coil Schematic Level Connection Guide

11.5 GP0/PWRGD Pin

The GP0 pin is a digital output referenced to LDO1P8. The AP can use the power good signal to turn on the charging connection indicator or other system functions. Power good (PWRGD) pin is pulled low by default. In BPP mode, the power good pin is pulled high when MLDO is enabled. In EPP mode, the power good pin is pulled high at the end of the negotiation phase by default. It can be configured to be pulled high when MLDO Vout is enabled.

11.6 GP1/Q Main Pin and GP3/Q Offset Pin

GP1 and GP3 are digital inputs used to configure Q factor value by resistor combination. If both GP1 and GP3 are low (< 0.2V), the P9415-R reports the default value programmed in the firmware. Q is 30 in the default configuration and can be changed with a P9415-R Wireless Power Pro GUI; otherwise, the default Q factor value is decided by the following tables.

Table 5. Q Factor Main – GP1

GP1 ≥ Vmin	GP1 < Vmax	Q_Main	Pup(R)	Pdown(R)
0.2	0.55V	30	100K	27K
0.55V	0.90V	40	100K	68K
0.90V	1.25V	50	100K	150K
1.25V	1.60V	60	47K	180K
1.60V	1.98V	70	47K	NP

Table 6. Q Factor Offset – GP3

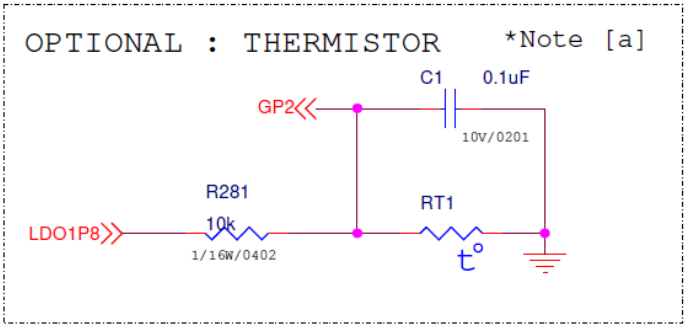
GP3 ≥ Vmin	GP3 < Vmax	Q_Offset	Pup(R)	Pdown(R)
0V	0.2V	+0	NP	47K
0.2	0.55V	+1	100K	27K
0.55V	0.90V	+2	100K	68K
0.90V	1.25V	+4	100K	150K
1.25V	1.60V	+6	47K	180K
1.60V	1.98V	+8	47K	NP

For example, if both GP1 and GP3 are pulled up, the reported Q factor value is 78(70+8). The AP can also change the reported Q factor by writing to register 0x55 before the negotiation phase.

11.7 GP2/ External Thermistor Pin

The GP2 pin is connected to the internal ADC and can measure the voltage of the thermistor connected to measure the external temperature on either the receiver coil or the PCB. The P9415-R sends interrupts to the AP if the voltage reaches below the threshold level (0.6V default, configurable) to allow the AP an opportunity to reduce the temperature and prevent power transfer interruptions. The AP must convert the ADC value into a pin voltage using the below equation. Voltage can be converted into temperature information based on the thermistor manufacturer datasheet information.

Equation:



$$\text{Voltage on GP2 Pin in mV} = (\text{Register 0x42 [11:0] Data} / 4095) * 10 * 2.1$$

Figure 18. GP2 Pin External Connection to Thermistor Configuration

11.8 GP4/I2C Address Select Pin

The pin is used to select the P9415-R device I2C slave address. When this pin is pulled high to LDO1P8, I2C Address is 0x3F and when this pin pulled low to GND, I2C Address is 0x3B (default). The slave address is a 7-bit I2C address.

11.9 GP5/INHIBIT Pin

The GP5 / INHIBIT pin is a digital input referenced to LDO1P8 and gets polled during the startup. When the INHIBIT pin is low, the Rx mode is enabled. Pulling the INHIBIT pin high will prevent the P9415-R from connecting to the transmitter. The AP can use this pin to safely enable and disable wireless power transfer function with proper VRECT node protections. If this pin is driven high in the power transfer phase, the P9415 R will send an End Power Transfer packet to the transmitter and wireless power transfer will be disabled while VRECT protection is alive.

11.10 GP6/EPP_DISABLE Pin

The GP6 is assigned as a digital input referenced to LDO1P8. When the EPP_DISABLE pin is high, the Rx EPP mode is disabled and the P9415-R operates in BPP mode. When it is low, the Rx mode is determined by the internal mode configuration setting value in the firmware. If not used, connect this pin to ground.

12. Foreign Object Detection

When metallic objects are exposed to an alternating magnetic field, eddy currents cause such objects to heat up. Examples of such parasitic metal objects are coins, keys, paper clips, etc. The amount of heating depends on the strength of the coupled magnetic field, as well as the characteristics of the object, such as its resistivity, size, and shape. In a wireless power transfer system, the heating manifests itself as a power loss, and therefore a reduction in power-transfer efficiency. Moreover, if no appropriate measures are taken, the heating could be sufficient that the foreign object could become heated to an unsafe temperature.

In the Extended Power Profile, there are two methods of foreign object detection (FOD). One is by measuring the system quality factor before entering the power transfer phase, and the other is to measure the power loss difference between the received power and the transmitted power during the power transfer phase. Before entering the power transfer phase, the P9415-R sends a reference Q-factor (default 30) in the negotiation phase. The transmitter measures the Q-factor on its coil and compares it with the reference Q-factor provided by the P9415-R. If the difference is large, the transmitter presumes that there is a foreign object (FO) between the Tx and Rx and shuts down. The power loss foreign object detection method is used in both the Extended Power Profile (EPP) and the Basic Power Profile (BPP) modes power transfer phase. During the power transfer phase, the P9415-R continuously sends to the transmitter the amount of power received using the Received Power Packet (RPP). The transmitter will compare the RPP packet information received from the receiver with its measured transmitted power. If there is a significant difference, the transmitter presumes that there is a foreign object (FO) between Tx and Rx that is absorbing the transmitted power and will stop the power transfer to avoid heating of FO.

12.1 FOD Parameters in Receiver Mode

For a WPC power loss foreign object detection to function effectively, the receiver must account and compensate for all of their known losses. Such losses, for example, could be due to resistive losses or nearby metals that are part of the receiver. Because the system accurately measures its power and accounts for all known losses, it can thereby detect foreign objects because they cause an unknown loss. The WPC specification requires that a power receiver must report to the power transmitter its received power (PPR) in an RPP. The maximum value of the received power accuracy $P\Delta$ depends on the maximum power of the power receiver as defined in below Table.

The power receiver must determine its PPR with an accuracy of $\pm P\Delta$, and report its received power as PRECEIVED = PPR + $P\Delta$. This means that the reported received power is always greater than or equal to the transmitted power (PPT) if there is no foreign object (FO) present on the interface surface.

Table 7. Recommended Maximum Estimated Power Loss

Maximum Power (W)	Maximum $P\Delta$ (mW)
5	350
10	500
15	750

The compensation algorithm includes parameter values that are programmable either internal register or customer configuration table in MTP. Programmability is necessary so that the calibration settings can be optimized to match the power transfer characteristics of each particular WPC system to include the power losses of the transmit and receive coils, battery, shielding, and case materials under no-load to full-load conditions. The values are based on the comparison of the received power against a reference power curve so that any foreign object can be sensed when the received power is different than the expected system power.

FOD parameters consist of eight sections. Each section is divided by output current and consists of gain and offset to compensate for Rx internal power loss; each section is also adjusted for Reported Rx power. The following comprises the Rx load current ranges for the FOD sections.

- FOD section [0] is from 0mA to section 0 current mA
- FOD section [1] is reserved
- FOD section [2] is from section 0 current mA to 351mA
- FOD section [3] is from 352mA or section 0 671mA
- FOD section [4] is from 672mA to 863mA
- FOD section [5] is more than 864mA

Section 0 current is the point where the internal rectifier changes bridge configuration from half-bridge to full-bridge. In the default configuration, If VOUT is set to less than 7V, section0 current is 288mA. If Voutset is higher than 7V, section0 current is 384mA, section2 is not used and section3 starts from 384mA. There is around ±30mA load current hysteresis for changing the FOD sections. These settings can be changed using the *P9415-R Wireless Power Pro GUI*.

The formula of Rx Reported Power is:

$$Rx\ Reported\ Power[0..5] = Power(Rx\ delivered\ power) * FOD\ Gain[0 \ldots 5] + Offset[0..5]$$

Place the receiver with the P9415-R on the Nok9 FOD transmitter. Ramp the current on the output of the P9415-R in steps of 50mA to 100mA and monitor power difference between the Nok9 transmitted power and the receiver reported power value. The difference should be within maximum Power loss delta as shown in Table 7. If the difference exceeds the maximum power loss delta, adjust the FOD gain or FOD offset of that particular output current section to bring the difference back to within range. The AP can modify the FOD gain and FOD offset by writing to the Foreign Object Detection Customer Registers (0x68-0x77). In the final product, the AP can use the VRECTON interrupt or battery charger interrupt as a trigger to update the FOD registers.

12.2 FOD Parameters in Transmitter Mode

For a WPC power loss foreign object detection to function effectively, the transmitter must set the FOD threshold at a reasonable value by accounting all its known losses such as Coil resistance loss and losses because of metal around the coil integrated into the product. In the power transfer phase, the P9415-R will continuously calculate the difference between its measured transmitted power and RPP packet information received from the receiver. If the difference is higher than the FOD threshold, the P9415-R presumes that there is a foreign object (FO) between Tx and Rx that is absorbing the transmitted power and will stop the power transfer to avoid heating of FO.

FOD threshold value changes based on the Received Power Packet value (RPP) from the receiver. In the default configuration, If RPP is larger than 3700mW (FodSegThd), the FOD threshold is -100mW (FodThdH) and if RPP is less than 3700mW, the FOD threshold is 800mW (FodThdL)

The FodSegThd, FodThdH, and FodThdL are configurable by config table in MTP using the P9415-R Wireless Power Pro GUI.

FOD criteria: FOD threshold > Transmitted Power (PPT) – Received Power (RPP)

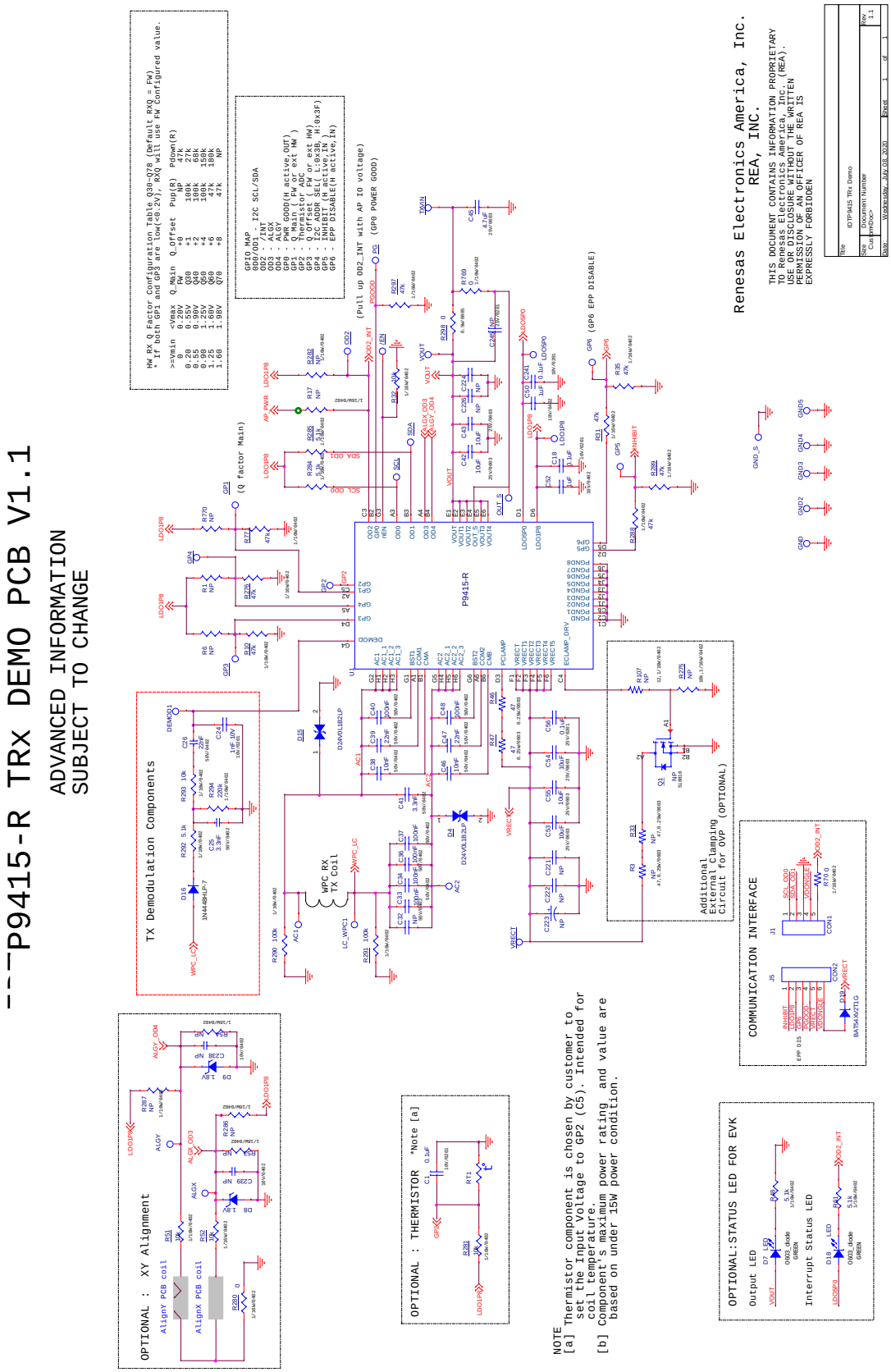
13. I2C Function

The P9415-R uses standard I2C slave implementation protocol to communicate with a host Application Processor (AP) or other I2C peripherals. The I2C slave address is decided by GP4 voltage. During the P9415-R power-up, if the GP4 pin is pulled down, the I2C address is 0x3B. During the P9415-R power-up, if the GP4 pin is pulled high, the I2C address is 0x3F.

The communication protocol is implemented using 8 bits for data and 16 bits for addresses. Note that some values require multiple registers and therefore span multiple addresses. For example, the address of the device ID high byte is 0001HEX and the low byte address is 0000HEX.

The AP can write to only the registers that are marked as Read/Write (RW). Registers marked as Read Only (R) should never be sent a Write command. Likewise, register locations marked Reserved should not receive a Write command. When writing to a RW register that contains a combination of RW fields and reserved fields, a read-modify-write should be performed to the intended bit/field only. All other bits, including reserved bits should NOT be modified.

14. P9415-R TRX Demo PCB v1.1 Schematic



15. Bill of Materials (P9415-R-EVK Demo Board Rev1.1)

Item	Quantity	Reference	Value	Description	Part Number	PCB footprint
1	23	GP1,DEMOD1,OD2,GP2,AC2,GP3,GND3,GP4,GND4, GP5,GND5,GP6,LDO1P8,LDO5P0,SDA,SCL,OUT_S,G P0,GND_S,EN_AP,ALGY,ALGX,/EN	PTH_TP	Test Pad		10mil_35pad_1
2	3	LC_WPC1,AC1,TXVIN	NP	PC TEST POINT MINIATURE	NP	test_pt_sm_135x70
3	1	C1	0.1uF	CAP CER 0.1UF 10V X5R 0402	GRM155R61A104KA01J	402
4	5	C18,C56,C241	0.1uF	CAP CER 0.1UF 10V X5R 0201	GRM033R61A104ME15D	201
5	1	C24	1nF 10V	CAP CER 1000PF 10V X7R 0201	100R05W102KV4T	201
6	2	C25,C41	3.3nF	CAP CER 3300PF 50V X7R 0402	CL05B332KB5NNNC	402
7	3	C26,C39,C47	22nF	CAP CER 0.022UF 50V X7R 0402	GRM155R71H223KA12D	402
8	1	C32	NP	CAP CER 0.1UF 50V X5R 0402	NP	402
9	6	C33,C34,C36,C37,C40,C48	100nF	CAP CER 0.1UF 50V X5R 0402	GRM155R61H104KE19D	402
10	2	C38,C46	10nF	CAP CER 10000PF 50V X5R 0402	CGA2B3X5R1H103M050BB	402
11	5	C42,C43,C53,C54,C55	10uF	CAP CER 10UF 35V X5R 0603	GRM188R6YA106MA73D	603
12	1	C45	4.7uF	CAP CER 4.7UF 25V X5R 0603	CC0603MRX5R8BB475	603
13	2	C50,C52	1uF	CAP CER 1UF 10V X5R 0402	GRM153R61A105ME95D	402
14	2	C238,C239	NP	CAP CER 3300PF 50V X7R 0402	NP	402
15	1	C223	NP	CAP TANT POLY 6.8UF 35V 1411	NP	cap_pol_3p5x2p8mm
16	3	C221,C222,C224	NP	CAP CER 10UF 35V X5R 0603	NP	603
17	1	C245	NP	CAP CER 1000PF 25V X7R 0201	NP	201
18	2	D4,D15	D24V0L1B2LP	Bidirectional ESD protection diode	D24V0L1B2LP	dfn1006_2ld_diode
19	2	D7,D18	LED	LED GREEN CLEAR SMD	LTST-C191KGKT	0603_diode
20	2	D8,D9	1.8V	DIODE ZENER 1.8V 250MW SOD523	CMOZ1L8	SOD523
21	1	D16	DIODE	DIODE GEN PURP 80V 125MA 2DFN	1N4448HLP-7	dfn1006_2ld_diode
22	1	D19	BAT54XV2T1G	DIODE SCHOTTKY 30V 200MA SOD523	BAT54XV2T1G	SOD523
23	5	GND2,VRECT,VOUT,GND	TP	PC TEST POINT MINIATURE	5015	test_pt_sm_135x70
24	1	J1	CON1	CONN HEADER VERT 5POS 2.54MM	68000-105HLF	header_1x5_SMD
25	1	J5	CON2	CONN HEADER VERT 6POS 2.54MM	68002-206HLF	header_1x6_SMD
26	1	Q1	NP	MOSFET N-CH 30V	NP	BGA-4
27	1	RT1	NP		NP	NTC2
28	12	R1,R3,R6,R17,R33,R53,R54,R107,R275, R286,R287, R770	NP	RES SMD 150K OHM 1% 1/16W 0402	NP	402
29	2	R46,R47	47	RES SMD 47 OHM 5% 1/4W 0603	ESR03EZPJ470	603
30	7	R10,R32,R51,R52,R281,R282,R293	10k	RES SMD 10K OHM 5% 1/16W 0402	RC0402JR-0710KL	402
31	7	R31,R35,R276,R288,R289,R297,R771	47k	RES SMD 47K OHM 5% 1/16W 0402	RC0402JR-0747KL	402
32	5	R48,R61,R284,R285,R292	5.1k	RES SMD 5.1K OHM 5% 1/16W 0402	RC1005F512CS	402
33	2	R290,R291	100k	RES SMD 100K OHM 5% 1/16W 0402	RC0402JR-07100KL	402
34	1	R294	220k	RES SMD 220K OHM 5% 1/16W 0402	RC0402JR-07220KL	402
35	1	R298	0	RES 0 OHM 1% 1/2W 0805	CRCW08050000Z0EAHP	805
36	3	R70,R280,R769	0	RES SMD 0 OHM JUMPER 1/16W 0402	RC0402JR-070RL	402
37	1	U1	P9415-R		P9415-R	csp53_2p8x4_0p4mm

16. P9415-R-EVK PCB Layout

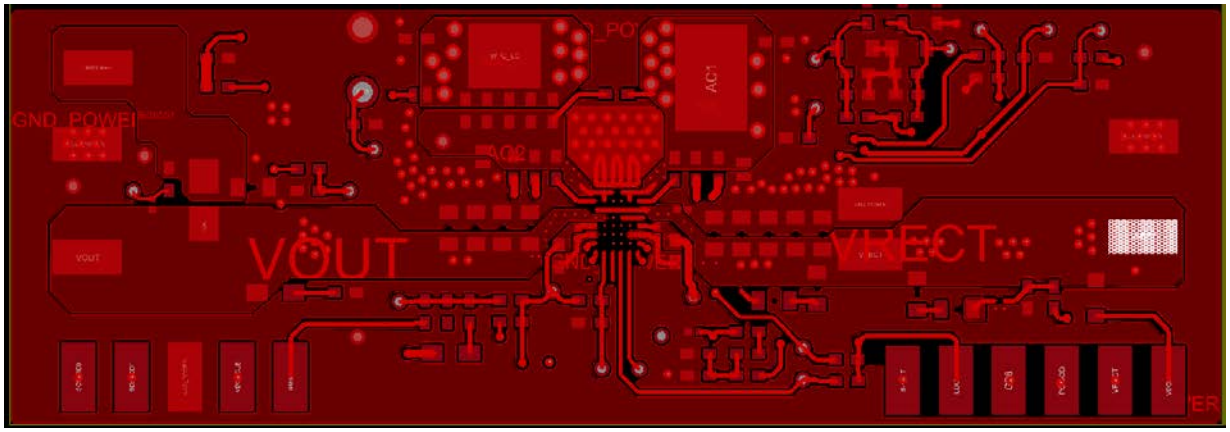


Figure 19. Top Layer

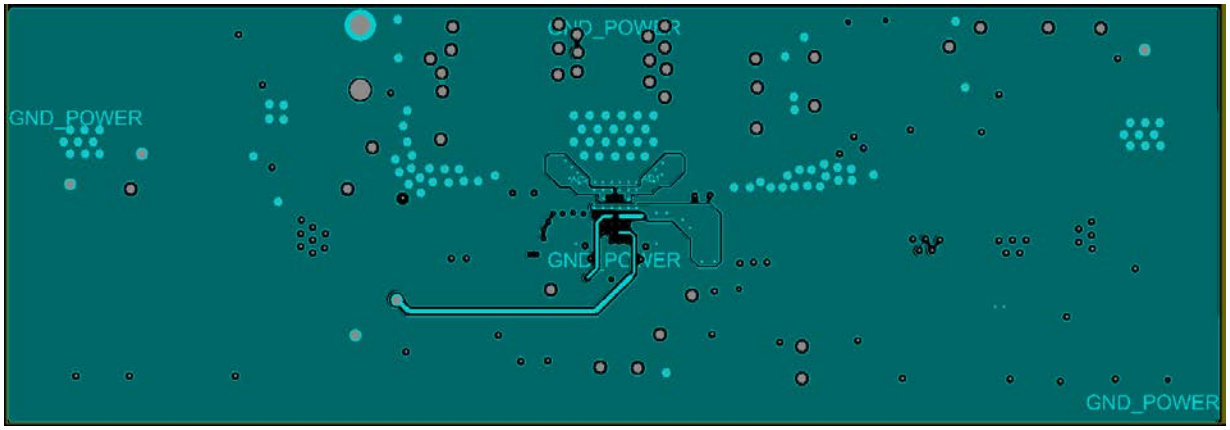


Figure 20. Layer2 (GND Layer)

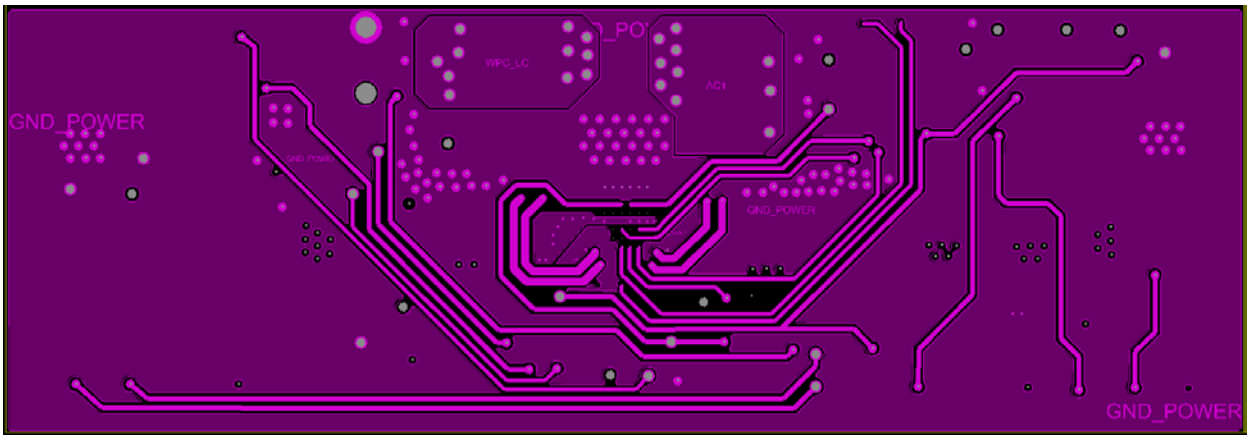


Figure 21. Layer4 (POWER/Signal/GND Layer)

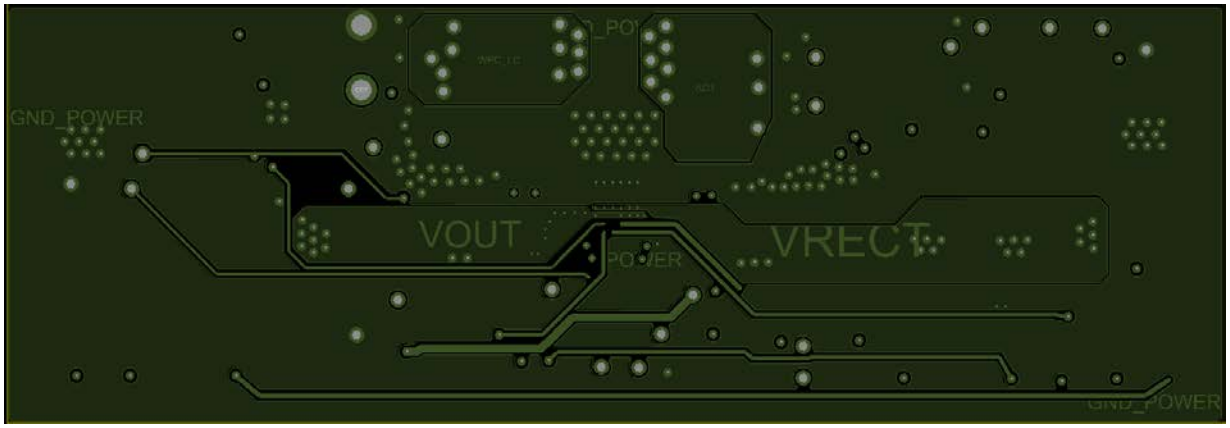


Figure 22. Bottom Layer

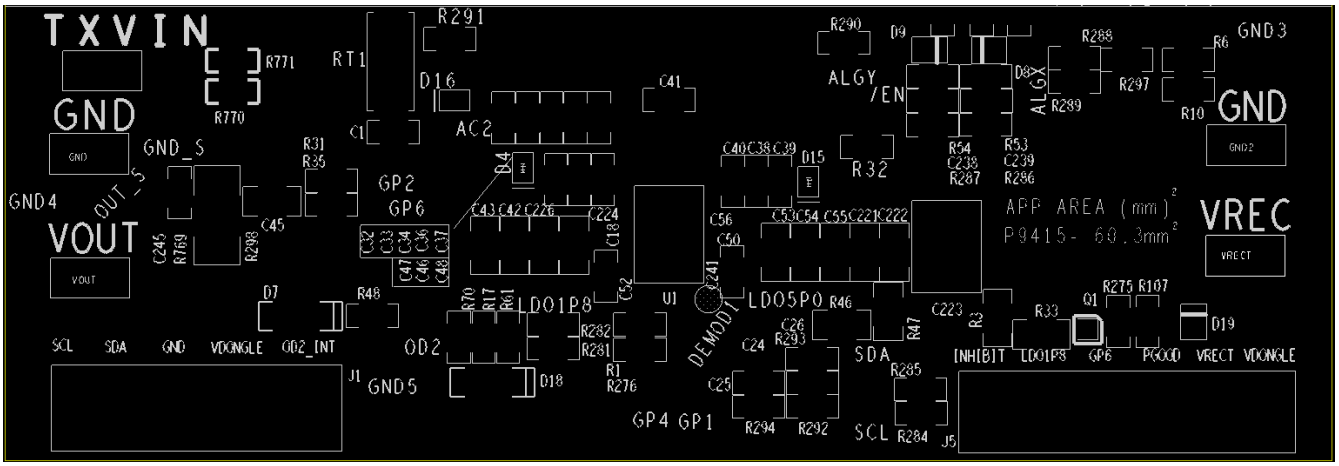


Figure 23. Top Silkscreen Layer

17. Ordering Information

Part Number	Description
P9415-R-EVK	P9415-R Evaluation board
WPD-USB-DONGLE	USB to I2C don required to connect with P9415-R Windows GUI. It is not included in the P9415-R-EVK evaluation kit and needs to be ordered separately.

18. Revision History

Revision	Date	Description
1.0	May 27, 2021	Initial release.

Appendix A–List of Registers

Table 8. Chip ID (0x00, 0x01)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x00 [7:0]	Chip_ID_L	R	0x15	Chip ID low byte
0x01 [7:0]	Chip_ID_H	R	0x94	Chip ID high byte

Table 9. HW Revision Register, HW_Rev (0x02)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x02 [7:0]	HW_Rev	R	0x06	Hardware Revision 0x00 (default).

Table 10. Customer Code Register, Customer Code (0x03)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x03 [7:0]	CustomerCode	R	0x00	Customer code. 0x00 (default).

Table 11. CustomerID Register (0x04)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x04 [15:0]	CustomerID	R	0x0000	CustomerID

Table 12. ProjectID Register (0x06)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x06 [15:0]	ProjectID	R	0x0005	Project ID

Table 13. Firmware Revision Major (0x08)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x08 [7:0]	Major	R	0x02	Firmware major revision

Table 14. Firmware Revision Minor (0x09)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x09 [7:0]	Minor	R	0x01	Firmware minor revision

Table 15. Firmware Revision Beta (0x0A)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x0a [7:0]	beta	R	0x00	Firmware revision beta

Table 16. Date Register (0x0C)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x0c [96:0]	Date	R	–	12-byte string initialized with FW compile data code. The format of the string is: “Mmm DD YYYY”, where Mmm is a three letter Month code, followed by the date in the month and the year. The string is terminated with 0x00.

Table 17. Time Register, (0x18)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x18 [64:0]	Time	R	–	8-byte string initialized with FW compile time code. The format of the string is: “HH:MM:SS”. The string is not zero terminated.

Table 18. Part Number Register (0x20)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x20 [32:0]	Part Number	R	0x52000000	Part number.

Note: The bit definition in Rx mode and Tx mode is different.

Table 19. System Interrupt Clear Register (0x28, 0x29, 0x2A, 0x2B) in Rx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x2B [7:0]	Reserved	R/W	0	Reserved
0x2A [7]	OVERCURRWARN	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.
0x2A [6]	ADTERROR	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.
0x2A [5]	ADTRCVD	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.
0x2A [4]	ADTSENT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.
0x2A [3]	NTCOVERTEMP	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.
0x2A [2]	VRECTON	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.
0x2A [1:0]	Reserved	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [7]	VSWITCHFAILED	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [6]	SLEEPMODE	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [5]	IDAUTHSUCCESS	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [4]	IDAUTHFAILED	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [3]	BCSUCCESS	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [2]	BCTIMEOUT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers’ bit. This bit is self-cleared to 0 (by M0) afterward.

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x29 [1]	TXAUTHSUCCESS	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x29 [0]	TXAUTHFAILED	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [7]	LDODISABLE	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [6]	LDOENABLE	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [5]	MODECHHGED	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [4]	TXDATARCVD	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [3]	VSWITCHSUCCESS	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [2]	OVERTEMP	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [1]	OVERVOLT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [0]	OVERCURR	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.

Note: The bit definition in Rx mode and Tx mode is different.

Table 20. System Interrupt Clear Register (0x28, 0x29, 0x2A, 0x2B) in Tx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x2B [7:0]	Reserved	R/W	0	Reserved
0x2A [7:0]	Reserved	R/W	0	Reserved
0x29 [7:1]	Reserved	R/W	0	Reserved
0x29 [0]	CSP_RECEIVE_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [7]	TX_INIT_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [6]	GET_DPING_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [5]	MODECHNGED	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [4]	GET_CFG_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [3]	GET_ID_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [2]	GET_SS_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [1]	START_DPING_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.
0x28 [0]	EPT_TYPE_INT	R/W	0	AP writes 1 to clear the corresponding Interrupt Registers' bit. This bit is self-cleared to 0 (by M0) afterward.

Note: The bit definition in Rx mode and Tx mode is different.

Table 21. System Status Register (0x2C, 0x2D, 0x2E, 0x2F) in Rx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x2F [7:0]	Reserved	R	0	Reserved
0x2E [7]	OVERCURRWARN	R	0	1 = Indicates the Iout is closed to Ilim value
0x2E [6]	ADTERROR	R	0	1 = Indicates error condition happens in the communication channel. Cleared together with the corresponding interrupt flag.
0x2E [5]	ADTRCVD	R	0	1 = Indicates data was received from the Com channel and is pending to be read. Cleared together with the corresponding interrupt flag.
0x2E [4]	ADTSENT	R	0	1 = Indicates data message was processed (sent) in the Com Channel and the Write Buffer is available to accept new data. Cleared together with the corresponding interrupt flag.
0x2E [3]	NTCOVERTEMP	R	0	1 = Indicates the NTC value exceeds the threshold
0x2E [2]	VRECTON	R	0	Indicates AC power is applied. The flag is set before the Configuration Packet. It is cleared on system reset or when power is removed. An interrupt event is generated on SET event.
0x2E [1:0]	Reserved	R	0	Reserved
0x2D [7]	VSWITCHFAILED	R	0	1 = Indicates the voltage switch command is failed.
0x2D [6]	SLEEPMODE	R	0	1 = Indicates the Rx is in sleep mode
0x2D [5]	IDAUTHSUCCESS	R	0	1 = Indicates the ID authentication is passed
0x2D [4]	IDAUTHFAILED	R	0	1 = Indicates the ID authentication is failed
0x2D [3]	BCSUCCESS	R	0	1 = Indicates the backchannel packet is received by Tx
0x2D [2]	BCTIMEOUT	R	0	1 = Indicates the backchannel packet is sending failed.
0x2D [1]	TXAUTHSUCCESS	R	0	1 = Indicates the Device authentication is passed.
0x2D [0]	TXAUTHFAILED	R	0	1 = Indicates the Device authentication is failed.
0x2C [7]	LDODISABLE	R	0	1 = Indicates the LDO is disabled
0x2C [6]	LDOENABLE	R	0	1 = Indicates the LDO is enabled
0x2C [5]	MODECHHGED	R	0	1 = Indicates the work mode of P9415 is changed
0x2C [4]	TXDATARCVD	R	0	1 = Indicates the proprietary packet from Tx is received.
0x2C [3]	VSWITCHSUCCESS	R	0	1 = Indicates the voltage switch command is successful.
0x2C [2]	OVERTEMP	R	0	1 = Indicates the die temperature exceeds the OTP threshold.
0x2C [1]	OVERVOLT	R	0	1 = Indicates the voltage on Vrect exceeds the OVP threshold
0x2C [0]	OVERCURR	R	0	1 = Indicates the current exceeds the OCP threshold.

Note: The bit definition in Rx mode and Tx mode is different.

Table 22. System Status Register (0x2C, 0x2D, 0x2E, 0x2F) in Tx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x2F [7:0]	Reserved	R	0	Reserved
0x2E [7:0]	Reserved	R	0	Reserved
0x2D [7:1]	Reserved	R	0	Reserved
0x2D [0]	CSP_RECEIVE_INT	R	0	1 = Indicates the CSP packet is received. Cleared together with the corresponding interrupt flag
0x2C [7]	TX_INIT_INT	R	0	1 = Indicates the Tx initialization is finished
0x2C [6]	GET_DPING_INT	R	0	1 = Indicates the P9415 works in Tx mode, but is put on another working Tx device.
0x2C [5]	MODECHNGED	R	0	1 = Indicates the work mode of P9415 is changed.
0x2C [4]	GET_CFG_INT	R	0	1 = Indicates the configuration packet is received.
0x2C [3]	GET_ID_INT	R	0	1 = Indicates the Identification packet is received.
0x2C [2]	GET_SS_INT	R	0	1 = Indicates the Signal Strength packet is received.
0x2C [1]	START_DPING_INT	R	0	1 = Indicates the digital ping starts
0x2C [0]	EPT_TYPE_INT	R	0	1 = Indicates the error is met and recommend AP to remove power in this case. AP could read the error type from TRx End Power Transfer Reason Register

Note: The bit definition in Rx mode and Tx mode is different.

Table 23. System Interrupt Register (0x30, 0x31, 0x32, 0x33) in Rx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x33 [7:0]	Reserved	R	0	Reserved
0x32 [7]	OVERCURRWARN	R	0	1 = Indicates the Iout is closed to Ilim value 0 = No such condition
0x32 [6]	ADTERROR	R	0	1 = Indicates error condition happens in the communication channel. 0 = No such condition
0x32 [5]	ADTRCVD	R	0	1 = Indicates data was received from the Com channel and is pending to be read. 0 = No such condition
0x32 [4]	ADTSENT	R	0	1 = Indicates data message was processed (sent) in the Com Channel and the WriteBuffer is available to accept new data. 0 = No such condition
0x32 [3]	NTCOVERTEMP	R	0	1 = Indicates the NTC value exceeds the threshold 0 = No such condition
0x32 [2]	VRECTON	R	0	1 = Indicates AC power is applied. The flag is set before the Configuration Packet. It is cleared on system reset or when power is removed. An interrupt event is generated on SET event. 0 = No such condition
0x32 [1:0]	Reserved	R	0	Reserved
0x31 [7]	VSWITCHFAILED	R	0	1 = Indicates the voltage switch command is failed. 0 = No such condition
0x31 [6]	SLEEPMODE	R	0	1 = Indicates the Rx is in sleep mode 0 = No such condition
0x31 [5]	IDAUTHSUCCESS	R	0	1 = Indicates the ID authentication is passed 0 = No such condition
0x31 [4]	IDAUTHFAILED	R	0	1 = Indicates the ID authentication is failed 0 = No such condition

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x31 [3]	BCSUCCESS	R	0	1 = Indicates the backchannel packet is received by Tx 0 = No such condition
0x31 [2]	BCTIMEOUT	R	0	1 = Indicates the backchannel packet is sending failed. 0 = No such condition
0x31 [1]	TXAUTHSUCCESS	R	0	1 = Indicates the Device authentication is passed. 0 = No such condition
0x31 [0]	TXAUTHFAILED	R	0	1 = Indicates the Device authentication is failed. 0 = No such condition
0x30 [7]	LDODISABLE	R	0	1 = Indicates the LDO is disabled 0 = No such condition
0x30 [6]	LDOENABLE	R	0	1 = Indicates the LDO is enabled 0 = No such condition
0x30 [5]	MODECHHGED	R	0	1 = Indicates the work mode of P9415 is changed 0 = No such condition
0x30 [4]	TXDATARCVD	R	0	1 = Indicates the proprietary packet from Tx is received. 0 = No such condition
0x30 [3]	VSWITCHSUCCESS	R	0	1 = Indicates the voltage switch command is successful. 0 = No such condition
0x30 [2]	OVERTEMP	R	0	1 = Indicates the die temperature exceeds the OTP threshold. 0 = No such condition
0x30 [1]	OVERVOLT	R	0	1 = Indicates the voltage on Vrect exceeds the OVP threshold 0 = No such condition
0x30 [0]	OVERCURR	R	0	1 = Indicates the current exceeds the OCP threshold. 0 = No such condition

Note: The bit definition in Rx mode and Tx mode is different.

Table 24. System Interrupt Register (0x30, 0x31, 0x32, 0x33) in Tx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x33 [7:0]	Reserved	R	0	Reserved
0x32 [7:0]	Reserved	R	0	Reserved
0x31 [7:1]	Reserved	R	0	Reserved
0x31 [0]	CSP_RECEIVE_INT	R	0	1 = Indicates the CSP packet is received. 0 = No such condition
0x30 [7]	TX_INIT_INT	R	0	1 = Indicates the Tx initialization is finished 0 = No such condition
0x30 [6]	GET_DPING_INT	R	0	1 = Indicates the P9415 works in Tx mode, but is put on another working Tx device. 0 = No such condition
0x30 [5]	MODECHNGED	R	0	1 = Indicates the work mode of P9415 is changed. 0 = No such condition
0x30 [4]	GET_CFG_INT	R	0	1 = Indicates the configuration packet is received. 0 = No such condition
0x30 [3]	GET_ID_INT	R	0	1 = Indicates the Identification packet is received. 0 = No such condition
0x30 [2]	GET_SS_INT	R	0	1 = Indicates the Signal Strength packet is received. 0 = No such condition
0x30 [1]	START_DPING_INT	R	0	1 = Indicates the digital ping starts 0 = No such condition
0x30 [0]	EPT_TYPE_INT	R	0	1 = Indicates error is met and recommend AP to remove power in this case. 0 = No such condition

Note: The bit definition in Rx mode and Tx mode is different.

Table 25. System Interrupt Enable Register (0x34, 0x35, 0x36, 0x37) in Rx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x37 [7:0]	Reserved	R/W	0	Reserved
0x36 [7]	OVERCURRWARN	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x36 [6]	ADTERROR	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x36 [5]	ADTRCVD	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x36 [4]	ADTSENT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x36 [3]	NTCOVERTEMP	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x36 [2]	VRECTON	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x36 [1:0]	Reserved	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [7]	VSWITCHFAILED	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [6]	SLEEPMODE	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x35 [5]	IDAUTHSUCCESS	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [4]	IDAUTHFAILED	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [3]	BCSUCCESS	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [2]	BCTIMEOUT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [1]	TXAUTHSUCCESS	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x35 [0]	TXAUTHFAILED	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [7]	LDODISABLE	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [6]	LDOENABLE	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [5]	MODECHHGED	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [4]	TXDATARCVD	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [3]	VSWITCHSUCCESS	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [2]	OVERTEMP	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [1]	OVERVOLT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [0]	OVERCURR	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.

Note: The bit definition in Rx mode and Tx mode is different.

Table 26.System Interrupt Enable Register (0x34, 0x35, 0x36, 0x37) in Tx Mode

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x36 [7:0]	Reserved	R/W	0	Reserved
0x36 [7:0]	Reserved	R/W	0	Reserved
0x35 [7:1]	Reserved	R/W	0	Reserved
0x35 [0]	CSP_RECEIVE_INT	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [7]	TX_INIT_INT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [6]	GET_DPING_INT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [5]	MODECHNGED	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [4]	GET_CFG_INT	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [3]	GET_ID_INT	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [2]	GET_SS_INT	R/W	0	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [1]	START_DPING_INT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.
0x34 [0]	EPT_TYPE_INT	R/W	1	1 = Corresponding interrupt is enabled. 0 = Corresponding interrupt is disabled.

Note: The bit definition in Rx mode and Tx mode is different.

The alignment registers provide information about the positioning of the RX coil relative the TX coil. The AP may use this information to inform the user of possible reduced power transfer level due to receiver misalignment and suggest repositioning of the RX to improve coupling. The magnitude of the alignment information depends on the coil sizes and shall not be used for absolute distance measurement.

Table 27. Alignment X-Axis Register (0x38)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x38 [7:0]	Align[0]	R	–	8-bit signed integer representing X-axis alignment.

Table 28. Alignment Y-Axis Register (0x39)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x39 [7:0]	Align[1]	R	–	8-bit signed integer representing Y-axis alignment.

Table 29. Charge Status Register (0x3A)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3a [7:0]	SSChargeStau	RW	0x00	In RX mode the AP writes this register with the value intended to be sent as payload to the Charge Status Packet. The FW does not verify or modify the value in any way. The value should be filled based on the following: 0x0 = Reserved 0x1 = Charge status packet sent with parameter = 1 (1%) 0x2 = Charge status packet send with parameter = 2 (2%) … 0x64 = Charge status packet send with parameter = 100 (100%) 0x65-0xFE = Reserved 0xFF = No battery charge device or not providing charge status packet

Note: After writing to this register, Send Charge Status bit of Command Register (0x4E) needs to be set for transmission to begin.

Table 30. End of Power Transfer Code Register (0x3B)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3b [7:0]	EPTCode	R/W	0x00	In RX mode the AP writes this register with the value intended to be sent as payload to the Charge Status Packet. The FW does not verify or modify the value in any way. A WPC End of Power Transfer packet/message will be sent based on the following: 0 = WPC mode, unknown EPT should be sent. 1 = WPC mode, End of Charge EPT packet should be sent. 2 = WPC mode, Internal Fault EPT packet should be sent. 3 = WPC mode, Over Temperature EPT packet should be sent. 4 = WPC mode, Over Voltage EPT packet should be sent. 5 = WPC mode, Over Current EPT packet should be sent. 6 = WPC mode, Battery Failure EPT packet should be sent. 7 = WPC mode, Reconfiguration EPT packet should be sent. 8 = WPC mode, No Response EPT packet should be sent. 9-254 = Reserved

Table 31. Vout ADC Register (0x3C)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3c [15:0]	Vout ADC	R	–	12-bit of current main LDO Vout ADC value. Vout = ADC_Vout Value/4095*10*2.1(V)

Table 32. Vout Set Register (0x3E)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3e [15:0]	Vout_Set	R/W	–	Set the output voltage of the main LDO. VoutSet = (Vout_mV - 2800)*10/84 AP through this register, target Vrect will be automatically set for best efficiency.

Table 33. Vrect ADC (0x40)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x40 [15:0]	Vrect ADC	R	–	12 LSB of current Vrect ADC value. Vrect = ADC_Vrect Value/4095*10*2.1 (V).

Table 34. External Temperature Register ADC (0x42)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x42 [15:12]	Reserved	R	0	Reserved
0x42 [11:0]	NtcTemp	R	–	12-bit raw data of the thermistor ADC reading on GP2 pin. Vol_gp2 = NtcTemp / 4095 * 10 * 2.1(V)

Table 35. IOut Register (0x44)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x44 [15:0]	IOut	R	–	In RX mode the AP may read this register to get current Iout level in mA. In TX mode the register holds the Power Supply current Iin in mA.

Table 36. Die Temperature Register (0x46)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x46 [15:0]	DieTemp	R	–	12bit of current Die Temperature ADC value. Formula converting ADC value. Die Temperature in Celsius Degree is t_die [degC] = (ADC code * 0.075) - 174.

Table 37. AC Period Register (0x48)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x48 [15:0]	ACPeriod	R	–	Read back the AC Period. The value is presented by number of 6MHz clocks per 64 AC cycles. The AC frequency can be calculated as: F(kHz) = 64 * 6000 / ACPeriod;

Table 38. Iout Limit Set Register (0x4A)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x4a [7:0]	ILim	R	0x0E	Set main LDO current limit in 0.1A steps. The limit level is set to the value plus 0.1A.

Table 39. Signal Strength Packet (0x4B)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x4b [7:0]	SignalStrength	R	–	Signal Strength Packet sent by 9415 at beginning of power transfer

Table 40. System Mode Register (0x4D)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x4d [7]	BACKPOWERED	R	–	Indication P9415 is powered by Vrect or Vout, but Tx function is not enabled.
0x4d [6:4]	Reserved	R	–	Reserved
0x4d [3]	EXTENDED	R	–	Indicates WPC EPP mode.
0x4d [2]	TXMODE	R	–	Indication of WP Transmitter mode.
0x4d [1]	Reserved	R	–	Reserved
0x4d [0]	WPCMODE	R	–	Indicates the FW is in WP Receiver mode.

Table 41. System Command Register (0x4E)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x4F [7]	MPRENEGOTIATE	W	0	AP sets 1 to launch re-negotiation. P9415 clears the bit after processing the command
0x4F [6]	SETIDAUTNOK	W	0	AP sets 1 to set ID authentication pass flag. P9415 clears the bit after processing the command
0x4F [5:2]	Reserved	W	0	Reserved
0x4F [1]	CCACTIVATE	W	0	AP sets 1 to enabled WPC 1.3 communication. P9415 clears the bit after processing the command
0x4F [0]	SOFTRESTART	W	0	AP sets 1 to restart P9415. P9415 clears the bit after processing the command
0x4E [7]	VSWITCH	W	0	AP sets 1 to send Voltage Switch command. P9415 clears the bit after processing the command
0x4E [6]	Reserved	W	0	Reserved
0x4E [5]	CLRINT	W	0	AP sets 1 to clear the interrupt. P9415 clears the bit after processing the command
0x4E [4]	SENDCSP	W	0	AP sets 1 to send Charge Status Packet in Rx mode. P9415 clears the bit after processing the command
0x4E [3]	SENDEOP	W	0	AP sets 1 to send End of Power Transfer Packet in Rx mode. P9415 clears the bit after processing the command
0x4E [2]	SHA1AUTH	W	0	AP sets 1 to enable device authentication. P9415 clears the bit after processing the command
0x4E [1]	LDOTGL	W	0	AP sets 1 to toggle LDO ON/OFF. P9415 clears the bit after processing the command
0x4E [0]	SENDPROPP	W	0	AP sets 1 to enable send the proprietary packet. P9415 clears the bit after processing the command

Note: It takes time to implement the command. AP could write new command to System Command Register 3–5ms after the previous command.

Table 42. Foreign Object Detection Registers (FOD) (0x68-0x77)

The FOD registers are divided into eight pairs. Each pair has one byte for gain setting and one byte for offset setting. The first six pairs control the Received Power calculation for six power sectors during the Power Transfer phase. The seventh pair calibrates the internal DC Load. The set values of the FOD registers are found with the help of a Renesas developed calibration procedure using the nok9 tester.

The firmware initializes the FOD registers for BPP mode. The correct set is loaded at the completion of the ID and Configuration Phase. The AP can modify the registers at any time if needed to update the values.

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x68 [7:0]	GAIN_0	R/W	–	FOD coefficients for Power Region 0: Gain (slope settings).
0x69 [7:0]	OFFSET_0	R/W	–	FOD coefficients for Power Region 0: Offset settings.
0x6A [7:0]	GAIN_1	R/W	–	FOD coefficients for Power Region 1: Gain (slope settings).
0x6B [7:0]	OFFSET_1	R/W	–	FOD coefficients for Power Region 1: Offset settings.
0x6C [7:0]	GAIN_2	R/W	–	FOD coefficients for Power Region 2: Gain (slope settings).
0x6D [7:0]	OFFSET_2	R/W	–	FOD coefficients for Power Region 2: Offset settings.
0x6E [7:0]	GAIN_3	R/W	–	FOD coefficients for Power Region 3: Gain (slope settings).
0x6F [7:0]	OFFSET_3	R/W	–	FOD coefficients for Power Region 3: Offset settings.
0x70 [7:0]	GAIN_4	R/W	–	FOD coefficients for Power Region 4: Gain (slope settings).
0x71 [7:0]	OFFSET_4	R/W	–	FOD coefficients for Power Region 4: Offset settings.
0x72 [7:0]	GAIN_5	R/W	–	FOD coefficients for Power Region 5: Gain (slope settings).
0x73 [7:0]	OFFSET_5	R/W	–	FOD coefficients for Power Region 5: Offset settings.
0x74 [7:0]	GAIN_6	R/W	–	FOD coefficients for Power Region 6: Gain (slope settings).
0x75 [7:0]	OFFSET_6	R/W	–	FOD coefficients for Power Region 6: Offset settings.
0x76 [7:0]	GAIN_7	R/W	–	FOD coefficients for Power Region 7: Gain (slope settings).
0x77[7:0]	OFFSET_7	R/W	–	FOD coefficients for Power Region 7: Offset settings.

Table 43. Vin Register in Tx Mode (0x70)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x70 [15:0]	TxVin	R	–	Input voltage, value in mV.

Table 44. Vrect Register in Tx Mode (0x72)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x72 [15:0]	TxVrect	R	–	Vrect voltage in Tx mode, value in mV.

Table 45. End Power Transfer Reason Register (0x74)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x75 [7]	EPT_POCP	R	0	1 = Indicates over current protect during digital ping 0 = No such error
0x75 [6]	EPT_OTP	R	0	1 = Over current error 0 = No such error
0x75 [5]	EPT_FOD	R	0	1 = FOD error 0 = No such error
0x75 [4]	EPT_LVP	R	0	1 = Vrect is less than low voltage protection threshold 0 = No such error
0x75 [3]	EPT_OVP	R	0	1 = Over voltage error 0 = No such error
0x75 [2]	EPT_OCP	R	0	1 = Over current error 0 = No such error
0x75 [1]	Reserved	R	0	Reserved
0x75 [0]	EPT_CEP_TIMEOUT	R	0	1 = CEP timeout 0 = No such error
0x74 [7]	EPT_TIMEOUT	R	0	1 = Watch dog timeout 0 = No such error
0x74 [6:1]	Reserved	R	0	Reserved
0x74 [0]	EPT_CMD	R	0	1 = End power transfer packet has been received 0 = No such error

Table 46. System Command Register (0x76)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x77 [7:0]	Reserved	W	0	Reserved.
0x76 [7]	Reserved	W	0	Reserved.
0x76 [6]	CTCMND	W	0	AP sets 1 to set CT command. The P9415 will read CT command from CT Command register and implement. P9415 clears the bit after processing the command.
0x76 [5]	TX_CLRINT	W	0	AP sets 1 to clear interrupt. P9415 clears the bit after processing the command.
0x76 [4]	Reserved	W	0	Reserved
0x76 [3]	TX_BC	W	0	AP sets 1 to send a proprietary packet to Rx. P9415 clears the bit after processing the command
0x76 [2]	TX_DIS	W	0	AP sets 1 to disable Tx mode. P9415 clears the bit after processing the command.
0x76 [1]	Reserved	W	0	Reserved
0x76 [0]	TX_EN	W	0	AP sets 1 to enable Tx mode. P9415 clears the bit after processing the command

Note: It costs time to implement the command. AP could write new command to System Command Register 3–5ms after the previous command.

Table 47. Over Voltage Threshold Register in Tx Mode (0x98)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x98 [15:0]	OVpThd	R/W	0x2AF8	Over-voltage threshold in Tx mode, value in mV.

Table 48. Over Current Threshold Register in Tx Mode (0x9A)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x9A [15:0]	OCpThd	R/W	0x05DC	Over-current threshold in Tx mode, value in mA.

Table 49. FOD Low Segment Threshold Register in Tx Mode (0xA8)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xA8 [15:0]	FodThdL	R/W	0x0320	FOD threshold for low level segment in Tx mode, value in mW.

Table 50. FOD High Segment Threshold Register in Tx Mode (0xAA)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xAA [15:0]	fodThdH	R/W	0xFF9C	FOD threshold for high level segment in Tx mode, value in mW.

Table 51. FOD Segment Threshold Register in Tx Mode (0xAC)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xAC [15:0]	fodSegThd	R/W	0x0E74	Threshold for two segment FOD threshold. Value in mW. If Rx Power is higher than FOD Segment Threshold, the High Level FOD Threshold is used, otherwise, the Low Level FOD Threshold is used as FOD threshold.

Table 52. Ping Interval Register in Tx Mode (0xBA)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0xBA [15:0]	PingInterval	R/W	0x038E	The interval between each digital ping, value in ms.

Bi-di Communication Registers

Table 53. Write Data Type and Length Register for WPC 1.3 (0x1A0)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x1A1[7]	WrLsSize	R/W	0	7 LSB of packet size
0x1A0[7:5]	WrMsSize	R/W	0	3 MSB of packet size
0x1A0 [4:0]	WrType	R/W	0	Type of packet

Table 54. Write Data Register for WPC 1.3 (0x1A4~0x39F)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x1A4[508]	WrData	R/W	0	Raw data which is intended to send to Tx

Table 55. Read Data Register for WPC 1.3 (0x3A4~0x59F)

Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x3A4[508]	RdData	R	0	Raw data which is received from Tx

Table 56. Read Data Register for WPC 1.3 (0x196)

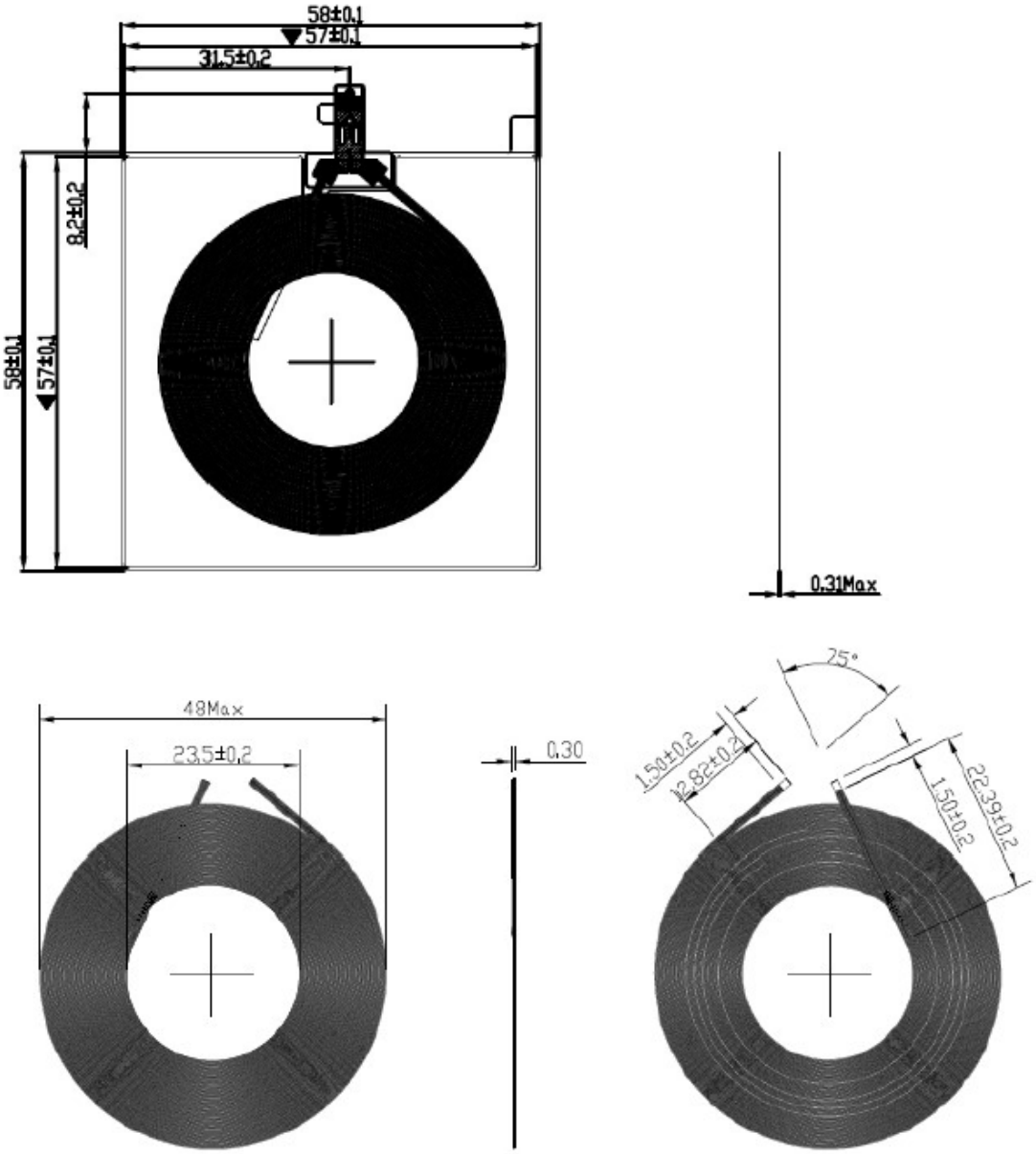
Address and Bit	Register Field Name	R/W	Default Value	Function and Description
0x196[15:0]	ccRdSize	R	0	Length of the raw data received from Tx

Procedure of WPC1.3 Bi-di Communication

1. Clear interrupt.
2. AP writes raw data to Write Data Register (0x1A4).
3. AP writes type and data length to Write Data Type and Length Register (0x1A0, 2 bytes).
4. AP writes command 0x02 to system command register (0x4F, 1 byte) to send the data out.
5. AP waits for interrupt (ADTRCVD).
6. AP reads received data length from Read Data Register (0x196, 2 bytes).
7. AP reads received data from Read Data Register (0x3A4).

Appendix B–Wireless Power Coil Key Specifications from Luxshare (ICTR-QS5858031L-MW034)

(1)尺寸 Dimensions (Unit: mm):



(2)电气参数 Electrical Characteristics:

No.	参数 Parameter	规格 Specification	测试设备 Test Instrument
1	电感 Inductance	9.0±0.2μH	KEYSIGHT E4980A LCR METER or EQUIVALENT (@100kHz 1.0 Vrms)
2	直流阻抗 DC Resistance	195mΩ+/-10%	KEYSIGHT E4980A LCR METER or EQUIVALENT
3	交流阻抗 AC Resistance	235mΩ+/-10%	KEYSIGHT E4980A LCR METER or EQUIVALENT (@100kHz 1.0 Vrms)

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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