User's Manual

8

The sales of these products are limited for China, Hong Kong, and India.

μPD79F7023, 79F7024

User's Manual: Hardware

8-Bit Single-Chip Microcontrollers

Renesas Electronics
www.renesas.com

Rev.1.10 Nov 2013

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.

   “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.

   Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(2012.4)

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

How to Use This Manual

Readers

This manual is intended for user engineers who wish to understand the functions of the μPD79F7023, 79F7024 and design and develop application systems and programs for these devices.

The target products are as follows.

- μPD79F7023, 79F7024

Purpose

This manual is intended to give users an understanding of the functions described in the **Organization** below.

Organization

The μPD79F7023, 79F7024 manual is separated into two parts: this manual and the instructions edition (common to the 78K/0 Series).

μPD79F7023, 79F7024 User's Manual Hardware	**78K/0 Series User's Manual Instructions**
• Pin functions • Internal block functions • Interrupts • Other on-chip peripheral functions • Electrical specifications	• CPU functions • Instruction set • Explanation of each instruction

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, logic circuits, and microcontrollers.

- To gain a general understanding of functions:
  → Read this manual in the order of the **CONTENTS**.
- How to interpret the register format:
  → For a bit number enclosed in angle brackets, the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.
- To know details of the 78K0 microcontroller instructions:
  → Refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representations:	$\overline{\times\times\times}$ (overscore over pin and signal name)	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numerical representations:	Binary	···×××× or ××××B
	Decimal	···××××
	Hexadecimal	···××××H

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD79F7023, 79F7024 User's Manual: Hardware	This manual
78K/0 Series User's Manual Instructions	U12326E
78K0/Kx2 Flash Memory Programming (Programmer) Application Note	U17739E
78K0/Kx2 Flash Memory Self Programming User's Manual	U17516E
78K0 Microcontrollers Self Programming Library Type 01 User's Manual	U18274E

Documents Related to Flash Memory Programming (User's Manual)

Document Name	Document No.
PG-FP5 Flash Memory Programmer User's Manual	R20UT0008E
QB-MINI2 On-Chip Debug Emulator with Programming User's Manual	R20UT0449E
QB-Programmer Programming GUI Operation	U18527E

Documents Related to Development Tools (Hardware) (User's Manual)

Document Name	Document No.
QB-MINI2 On-Chip Debug Emulator with Programming User's Manual	R20UT0449E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Development Tools (Software)

Document Name		Document No.
RA78K0 Ver.3.80 Assembler Package User's Manual[Note 1]	Operation	U17199E
	Language	U17198E
	Structured Assembly Language	U17197E
78K0 Assembler Package RA78K0 Ver.4.01 Operating Precautions (Notification Document)[Note 1]		ZUD-CD-07-0181-E
CC78K0 Ver.3.70 C Compiler User's Manual[Note 2]	Operation	U17201E
	Language	U17200E
78K0 C Compiler CC78K0 Ver. 4.00 Operating Precautions (Notification Document)[Note 2]		ZUD-CD-07-0103-E
SM+ System Simulator User's Manual	Operation	U18601E
	User Open Interface	U18212E
ID78K0-QB Ver.2.94 Integrated Debugger User's Manual	Operation	U18330E
ID78K0-QB Ver.3.00 Integrated Debugger User's Manual	Operation	U18492E
PM plus Ver.5.20[Note 3] User's Manual		U16934E
PM+ Ver.6.30[Note 4] User's Manual		U18416E

Notes 1. This document is installed into the PC together with the tool when installing RA78K0 Ver. 4.01. For descriptions not included in "78K0 Assembler Package RA78K0 Ver. 4.01 Operating Precautions", refer to the user's manual of RA78K0 Ver. 3.80.

2. This document is installed into the PC together with the tool when installing CC78K0 Ver. 4.00. For descriptions not included in "78K0 C Compiler CC78K0 Ver. 4.00 Operating Precautions", refer to the user's manual of CC78K0 Ver. 3.70.

3. PM plus Ver. 5.20 is the integrated development environment included with RA78K0 Ver. 3.80.

4. PM+ Ver. 6.30 is the integrated development environment included with RA78K0 Ver. 4.01. Software tool (assembler, C compiler, debugger, and simulator) products of different versions can be managed.

Other Documents

Document Name	Document No.
Semiconductor Package Mount Manual	**Note**
Quality Grades on NEC Semiconductor Devices	C11531E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E
Semiconductor Reliability Handbook	R51ZZ0001E

Note See the "Semiconductor Package Mount Manual" website (http://www.renesas.com/products/package/manual/index.jsp).

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

CONTENTS

CHAPTER 1 OUTLINE

1.1 Features

- 78K0 CPU core
- I/O ports, ROM and RAM capacities

Item / Products	I/O ports	Program Memory (Flash Memory)	Data Memory (Internal High-Speed RAM)
μPD79F7023	16 (CMOS I/O: 13, CMOS input: 3)	8 KB	512 bytes
μPD79F7024		16 KB	768 bytes

- Low power consumption
  - Internal high-speed oscillation mode: 140 μA (TYP.) (at f_{CPU} = 1 MHz operation)
  - STOP mode: 2.0 μA (TYP.) (at V_{DD} = 5.0 V)
- Clock
  - High-speed system clock … Selected from the following three sources
    - Ceramic/crystal oscillator: 1 to 10 MHz
    - External clock: 1 to 10 MHz
    - Internal high-speed oscillator: 4 MHz ± 3 % (T_A = –40 to +85 °C), 4 MHz ± 2 % (T_A = –20 to +70 °C)
  - Low-speed system oscillator 240 kHz ± 10 % … Watchdog timer, timer clock in intermittent operation
- Power-on-clear (POC) circuit
- Low-voltage detector (LVI) (An interrupt/reset (selectable) is generated when the detection voltage is reached))
  - Detection voltage: Selectable from eleven levels between 2.7 and 4.24 V
- Single-power-supply flash memory
  - Flash self programming enabled
  - Software protection function: Protected from outside party copying (no flash reading command)
- Safety function
  - Watchdog timer operated by clock independent from CPU
    … A hang-up can be detected even if the system clock stops
  - Supply voltage drop detectable by LVI
    … Appropriate processing can be executed before the supply voltage drops below the operation voltage
  - Equipped with option byte function
    … Important system operation settings set in hardware

○ Timer
- 16-bit timer/event counter … PPG output, capture input, external event counter input
- 8-bit timer H … PWM output, operable with low-speed internal oscillation clock
- 8-bit timer/event counter 5 … External event counter input
- Watchdog timer … Operable with low-speed internal oscillation clock

Item / Products	16-bit timer/event counter	8-bit timer	Watchdog timer
µPD79F7023	1 ch	Timer H: 1 ch Timer 5: 1 ch	1 ch
µPD79F7024			

○ Serial interface
- UART … Asynchronous 2-wire serial interface

Item / Products	UART
µPD79F7023	1 ch
µPD79F7024	

○ 8-bit resolution A/D conversion: 5 ch
○ Operational amplifier: 2 ch
○ Compiler: 1 ch
○ On-chip debug function …Available to control for the target device, and to reference memory
○ Assembler and C language supported
○ Development tools
- Support for simplified emulator (MINICUBE2)

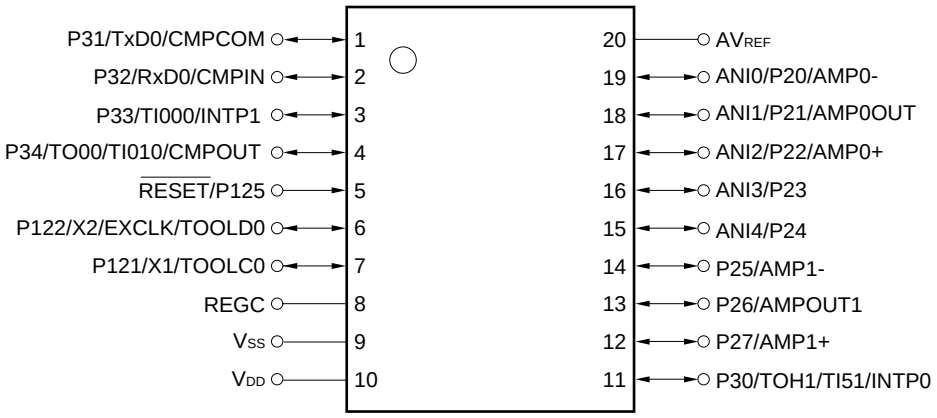
○ Power supply voltage: V_{DD} = 2.7 to 5.5 V
○ Operating ambient temperature: T_A = –40 to +85°C

1.2 Ordering Information

Pin count	Package	ROM	RAM	Semiconductor	Part Number
20-pin	20-pin plastic SSOP (7.62 mm (300))	8 KB	512 B	Product contains no lead in any area (Terminal finish is Ni/Pd/Au plating)	µ PD79F7023MC-CAA-AX
		16 KB	768 B		µ PD79F7024MC-CAA-AX

Remark All these products are lead free products.

1.3 Pin Configuration (Top View)



AMP0-, AMP0+, AMP1-, AMP1+ :	Amplifier Input	P30 to P34 :	Port 3
		P121, P122, P125 :	Port 12
AMP0OUT, AMP1OUT :	Amplifier Output	REGC :	Regulator Capacitance
ANI0 to ANI4 :	Analog Input	$\overline{\text{RESET}}$:	Reset
AVREF :	Analog Reference Voltage	RxD0 :	Receive Data
		TI000, TI010, TI51 :	Timer Input
CMPCOM :	Comparator Common Input	TO00, TOH1 :	Timer Output
		TOOLC0 :	Clock Input for Tool
CMPIN	Comparator Input	TOOLD0 :	Data Input/Output for Tool
CMPOUT	Comparator Output	TxD0 :	Transmit Data
EXCLK :	External Clock Input (Main System Clock)	VDD :	Power Supply
		VSS :	Ground
INTP0, INTP1 :	External Interrupt Input	X1, X2 :	Crystal Oscillator (Main System Clock)
P20 to P27 :	Port 2		

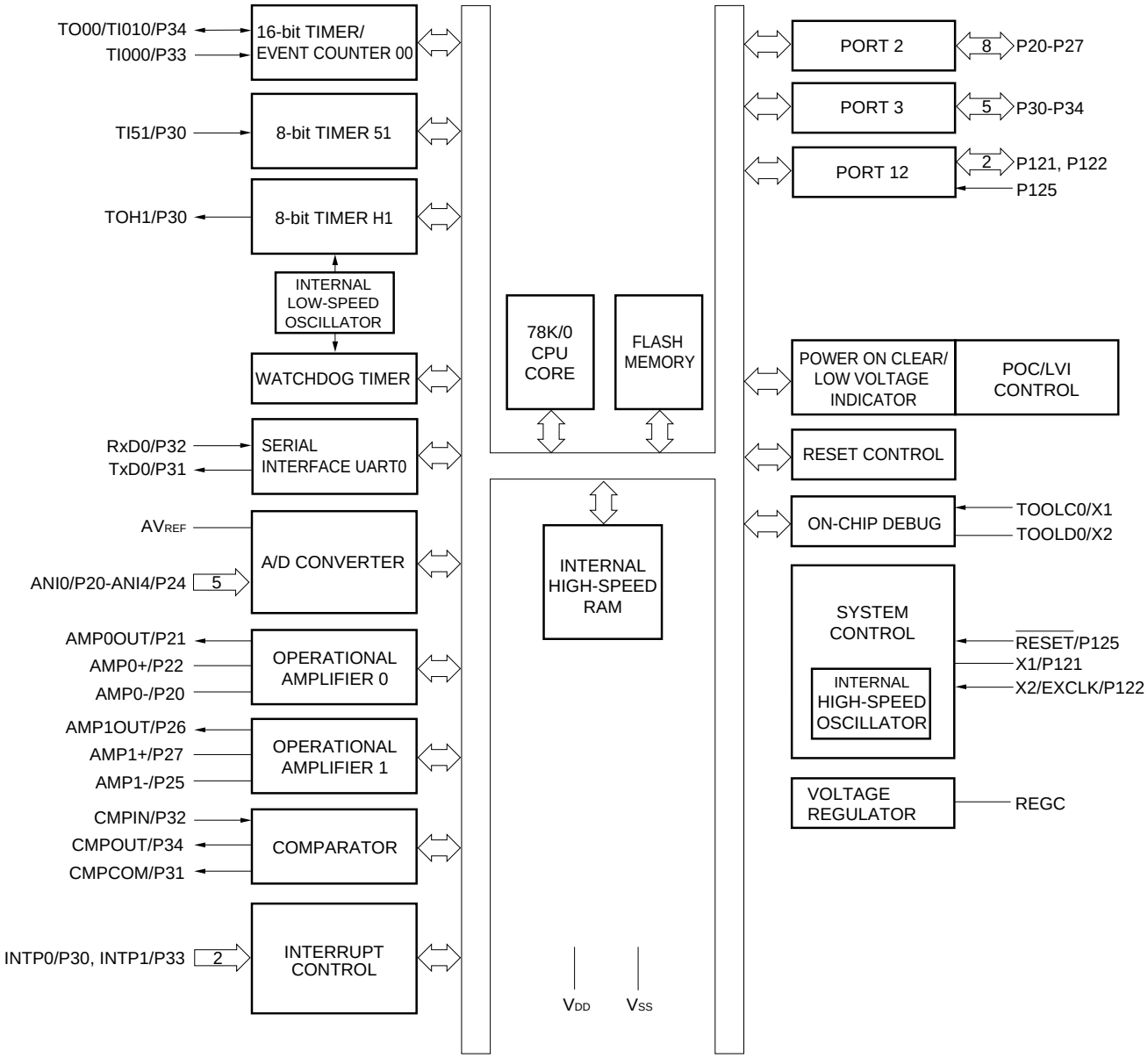
Cautions 1. VSS functions alternately as the ground potential of the A/D converter. Be sure to connect VSS to a stabilized GND (= 0 V).

2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 µF).

3. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT, ANI2/P22/AMP0+, ANI3/P23, ANI4/P24, P31/TxD0/CMPCOM, and P32/RxD0/CMPIN are set in the analog input mode after release of reset.

4. $\overline{\text{RESET}}$/P125 immediately after release of reset is set in the external reset input.

1.4 Block Diagram



Cautions 1. VSS functions alternately as the ground potential of the A/D converter. Be sure to connect VSS to a stabilized GND (= 0 V).

2. Connect the REGC pin to VSS via a capacitor (0.47 to 1 µF).

3. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT/PGAIN, ANI2/P22/AMP0+, ANI3/P23, and ANI4/P24 are set in the analog input mode after release of reset.

4. $\overline{\text{RESET}}$/P125 immediately after release of reset is set in the external reset input.

1.5 Outline of Functions

Item			µPD79F7023	µPD79F7024
Internal memory		Flash memory (self-programming supported)	8 KB	16 KB
		High-Speed RAM	512 bytes	768 bytes
Memory space			64 KB	
Clock	Main	High-speed system (crystal/ceramic oscillation, external clock input)	1 to 10 MHz: V_{DD} = 2.7 to 5.5 V	
		Internal high-speed oscillation	4 MHz ± 3 % (T_A = –40 to +85 °C), 4 MHz ± 2 % (T_A = –20 to +70 °C)	
	Internal low-speed oscillation		240 kHz ± 10 %	
General-purpose registers			8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Instruction set			• 8-bit operation, 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, and Boolean operation) • BCD adjust, etc.	
I/O ports (total)			16	
	CMOS I/O		15	
	CMOS input		1	
Timer	16 bits (TM0)		1 ch (PPG output: 1, capture input: 2)	
	8 bits (TM5)		1 ch	
	8 bits (TMH)		1 ch (PWM output: 1)	
	Watchdog (WDT)		1 ch	
Serial interface		UART	1 ch	
8-bit A/D converter (AV_{REF} = 2.7 to 5.5 V)			5 ch	
Operational amplifier (Products with operational amplifier)			2 ch (V_{DD} = 2.2 to 5.5 V)	
Comparator			1 ch	
Vectored interrupt Internal sources		External	3	
		Internal	8	
Reset			• Reset using $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-clear • Internal reset by low-voltage detector	
On-chip debug function			Provided	
Power supply voltage			V_{DD} = 2.7 to 5.5 V	
Operating ambient temperature			T_A = –40 to +85°C	
Package			20-pin plastic SSOP (7.62 mm (300))	

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Function List

There are two types of pin I/O buffer power supplies: AV_{REF} and V_{DD}. The relationship between these power supplies and the pins is shown below.

Table 2-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27
V_{DD}	Pins other than P20 to P27

(1) Port functions

Function Name	I/O	Function	After Reset	Alternate Function
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0/AMP0-
P21				ANI1/AMP0OUT
P22				ANI2/AMP0+
P23				ANI3
P24				ANI4
P25				AMP1-
P26				AMP1OUT
P27				AMP1+
P30	I/O	Port 3. 5-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOH1/TI51/INTP0
P31			Analog input	TxD0/CMPCOM
P32				RxD0/CMPIN
P33			Input port	TI000/INTP1
P34				TO00/TI010/CMPOUT
P121	I/O	Port 12. P121, P122 is 2-bit I/O port. P125 is 1-bit input-only port. For only P125, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	X1/TOOLC0
P122				X2/EXCLK/TOOLD0
P125	Input		Reset input	$\overline{\text{RESET}}$

(2) Non-port functions

Function Name	I/O	Function	After Reset	Alternate Function
ANI0	Input	A/D converter analog input	Analog input	P20/AMP0-
ANI1				P21/AMP0OUT
ANI2				P22/AMP0+
ANI3				P23
ANI4				P24
AMP0-	Input	Operational amplifier 0 input	Analog input	P20/ANI0
AMP0+				P22/ANI2
AMP0OUT	Output	Operational amplifier 0 output		P21/ANI1
AMP1-	Input	Operational amplifier 1 input	Analog input	P25
AMP1+				P27
AMP1OUT	Output	Operational amplifier 1 output		P26
CMPCOM	Input	Comparator common input	Analog input	P31/TxD0
CMPIN	Output	Comparator input		P32/RxD0
CMPOUT	Output	Comparator output	Input port	P34/TO00/TI010
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P30/TOH1/TI51
INTP1				P33/TI000
REGC	–	Connecting regulator output (1.9 V/2.5 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 µF).	–	–
$\overline{\text{RESET}}$	Input	System reset input	Reset input	P125
RxD0	Input	Serial data input to UART0	Input port	P32/CMPIN
TxD0	Output	Serial data output from UART0		P31/CMPCOM
TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture registers (CR000, CR010) of 16-bit timer/event counter 00	Input port	P33/INTP1
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P34/TO00/CMPOUT
TI51	Input	External count clock input to 8-bit timer/event counter 51	Input port	P30/TOH1/INTP0
TO00	Output	16-bit timer/event counter 00 output	Input port	P34/TI010/CMPOUT
TOH1	Output	8-bit timer H1 output	Input port	P30/TI51/INTP0
X1	–	Connecting resonator for main system clock	Input port	P121/TOOLC0
X2				P122/EXCLK/TOOLD0
EXCLK	Input	External clock input for main system clock	Input port	P122/X2/TOOLD0
V_{DD}	–	Positive power supply for pins other than port 2	–	–
AV_{REF}		A/D converter reference voltage input and positive power supply for port 2 and A/D converter		
V_{SS}	–	Ground potential	–	–
TOOLC0	Input	Clock input for flash memory programmer/on-chip debugger	Input port	P121/X1
TOOLD0	I/O	Data I/O for flash memory programmer/on-chip debugger		P122/X2/EXCLK

2.2 Description of Pin Functions

2.2.1 P20 to P27 (port 2)

P20 to P27 function as an I/O port. These pins also function as pins for A/D converter analog input, and operational amplifier I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P20 to P27 function as an I/O port. P20 to P27 can be set to input or output port in 1-bit units using port mode register 2 (PM2).

(2) Control mode

P20 to P27 function as A/D converter analog input, and operational amplifier I/O.

(a) ANI0 to ANI4

These are A/D converter analog input pins. When using these pins as analog input pins, refer to **(5) ANI0/P20 to ANI4/P24** in **10.6 Cautions for A/D Converter**.

(b) AMP0+, AMP0-

These are operational amplifier 0 input pins.

(c) AMP0OUT

This is an operational amplifier 0 output pin.

(d) AMP1+, AMP1-

These are operational amplifier 1 input pins.

(e) AMP1OUT

This is an operational amplifier 1 output pin.

Caution ANI0/P20 to ANI4/P24 are set in the analog input mode after release of reset.

2.2.2 P30 to P34 (port 3)

P30 to P34 function as an I/O port. These pins also function as pins for external interrupt request input, timer I/O, and clock I/O and data I/O for serial interface, comparator I/O.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P30 to P34 function as an I/O port. P30 to P34 can be set to input or output port in 1-bit units using port mode register 3 (PM3). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 3 (PU3).

(2) Control mode

P30 to P34 function as external interrupt request input, timer I/O, and clock I/O and data I/O for serial interface, comparator I/O.

(a) INTP0, INTP1

These are external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) TI000

This is a pin for inputting an external count clock to 16-bit timer/event counter 00 and is also for inputting a capture trigger signal to the capture registers (CR000, CR010) of 16-bit timer/event counter 00.

(c) TI010

This is a pin for inputting a capture trigger signal to the capture register (CR000) of 16-bit timer/event counter 00.

(d) TO00

This is a timer output pin of 16-bit timer/event counter 00.

(e) TI51

This is an external count clock input pin to 8-bit timer/event counter 51.

(f) TOH1

This is a timer output pin of 8-bit timer H1.

(g) RxD0

This is a serial data input pin for serial interface UART0.

(h) TxD0

This is a serial data output pin for serial interface UART0.

(i) CMPCOM

This is a comparator common input pin.

(j) CMPIN

This is a comparator input pin.

(k) CMPOUT

This is a comparator output pin.

2.2.3 P121, P122, P125 (port 12)

P121, P122 function as an I/O port. P125 functions as an Input port. These pins also function as pins for potential input for external low-voltage detection, connecting resonator for main system clock, external clock input for main system clock, external reset input, and clock input and data I/O for flash memory programmer/on-chip debugger.

Set bit 5 (RSTM) of the reset pin mode register (RSTMASK) to 1 when using P125/$\overline{\text{RESET}}$ as an input port, and clear RSTM to 0 when using P125/$\overline{\text{RESET}}$ as an external reset input.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P121, P122, and P125 function as an I/O port. P120 to P125 can be set to input or output port using port mode register 12 (PM12). Only for P125, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

(2) Control mode

P121, P122, and P125 function as pins for potential input for external low-voltage detection, connecting resonator for main system clock, external clock input for main system clock, external reset input, and clock input and data I/O for flash memory programmer/on-chip debugger.

(a) X1, X2

These are pins for connecting a resonator for main system clock.

(b) EXCLK

This is an external clock input pin for main system clock.

(c) $\overline{\text{RESET}}$

This is an active-low system reset input pin.

(d) TOOLC0

This is a clock input pin for flash memory programmer/on-chip debugger.

(e) TOOLD0

This is a data I/O pin for flash memory programmer/on-chip debugger.

Caution Because $\overline{\text{RESET}}$/P125 is set in the external reset input immediately after release of reset, if a reset signal is generated during low level input, the reset status continues until the input rises to the high level.

Remark For how to connect a flash memory programmer using TOOLC0/X1, TOOLD0/X2, refer to **CHAPTER 21 FLASH MEMORY**. For how to connect TOOLC0/X1, TOOLD0/X2 and an on-chip debug emulator, refer to **CHAPTER 22 ON-CHIP DEBUG FUNCTION**.

2.2.4 AV_{REF}, V_{DD}, V_{SS}

These are the power supply/ground pins.

(a) AV_{REF}

This is the A/D converter reference voltage input pin and the positive power supply pin of port 2 and A/D converter.

When the A/D converter is not used, connect this pin directly to V_{DD}[Note].

Note Make the AV_{REF} pin the same potential as the V_{DD} pin when port 2 is used as a digital port.

(b) V_{DD}

V_{DD} is a positive power supply pin.

(c) V_{SS}

V_{SS} is a ground potential pin[Note].

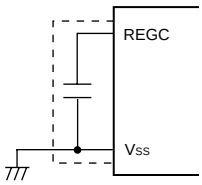
Note V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

2.2.5 REGC

This is a pin for connecting regulator output stabilization capacitance for internal operation and an internally connected pin.

(a) REGC

This is a pin for connecting regulator output (1.9 V/2.5 V) stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF). However, when using the STOP mode that has been entered since operation of the internal high-speed oscillation clock and external main system clock, 0.47 μF is recommended. Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-2 shows the types of pin I/O circuits and the recommended connections of unused pins.
Refer to **Figure 2-1** for the configuration of the I/O circuit of each type.

Table 2-2. Pin I/O Circuit Types

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
ANI0/P20/AMP0-	11-P	I/O	<Digital input setting> Independently connect to AV_{REF} or V_{SS} via a resistor. <Digital output setting and analog input setting > Leave open. Note 1
ANI1/P21/AMP0OUT	11-S		
ANI2/P22/AMP0+	11-N		
ANI3/P23	11-G		
ANI4/P24			
P25/AMP1-	11-P		
P26/AMP1OUT	11-S		
P27/AMP1+	11-N		
P30/TOH1/TI51/INTP0	5-AH		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P31/TxD0/CMPCOM	5-BD		<Digital input setting> Independently connect to AV_{REF} or V_{SS} via a resistor. <Digital output setting and analog input setting > Leave open. Note 1
P32/RxD0/CMPIN	5-BB		
P33/TI000/INTP1	5-AH		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P34/TO00/TI010/CMPOUT			
P121/X1/TOOLC0 Note 2	37-H		
P122/X2/EXCLK/TOOLD0 Note 2			
$\overline{\text{RESET}}$/P125	42-B	Input	Connect directly to V_{DD} or via a resistor.
AV_{REF}	–	–	Connect directly to V_{DD}.

Notes 1. If this pin is left open when specified as an analog input pin, the input voltage level might become undefined. It is therefore recommended to leave this pin open after specifying it as a digital output pin.

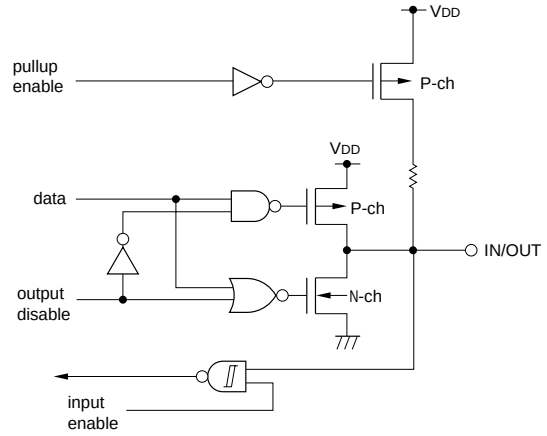
2. Use recommended connection above in input port mode (refer to **Figure 5-2 Format of Clock Operation Mode Select Register (OSCCTL)**) when these pins are not used.

Cautions 1. ANI0/P20/AMP0-, ANI1/P21/AMP0OUT, ANI2/P22/AMP0+, ANI3/P23, and ANI4/P24 are set in the analog input mode after release of reset.

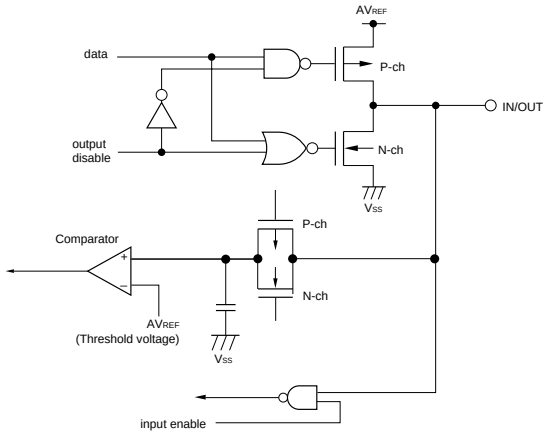
2. Because $\overline{\text{RESET}}$/P125 is set in the external reset input immediately after release of reset, if a reset signal is generated during low level input, the reset status continues until the input rises to the high level.

Figure 2-1. Pin I/O Circuit List (1/2)

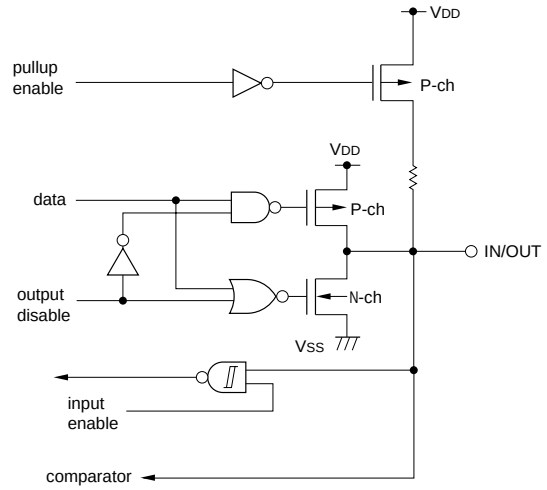
Type 5-AH



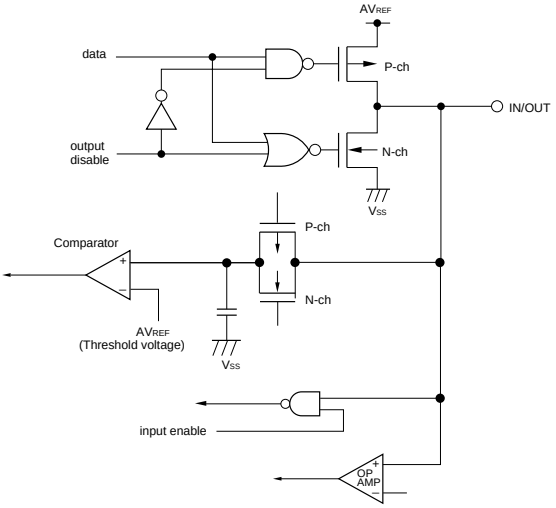
Type 11-G



Type 5-BB



Type 11-N



Type 5-BD

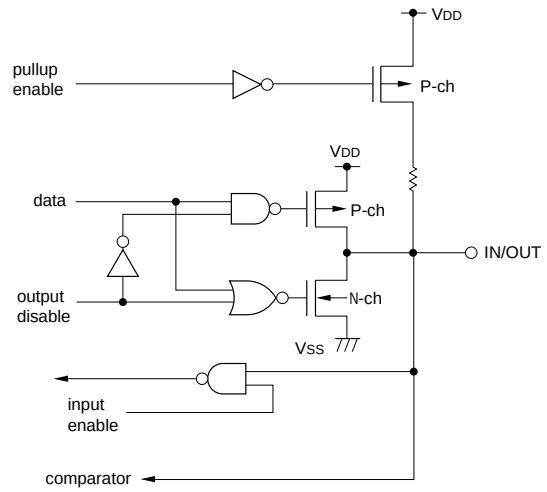
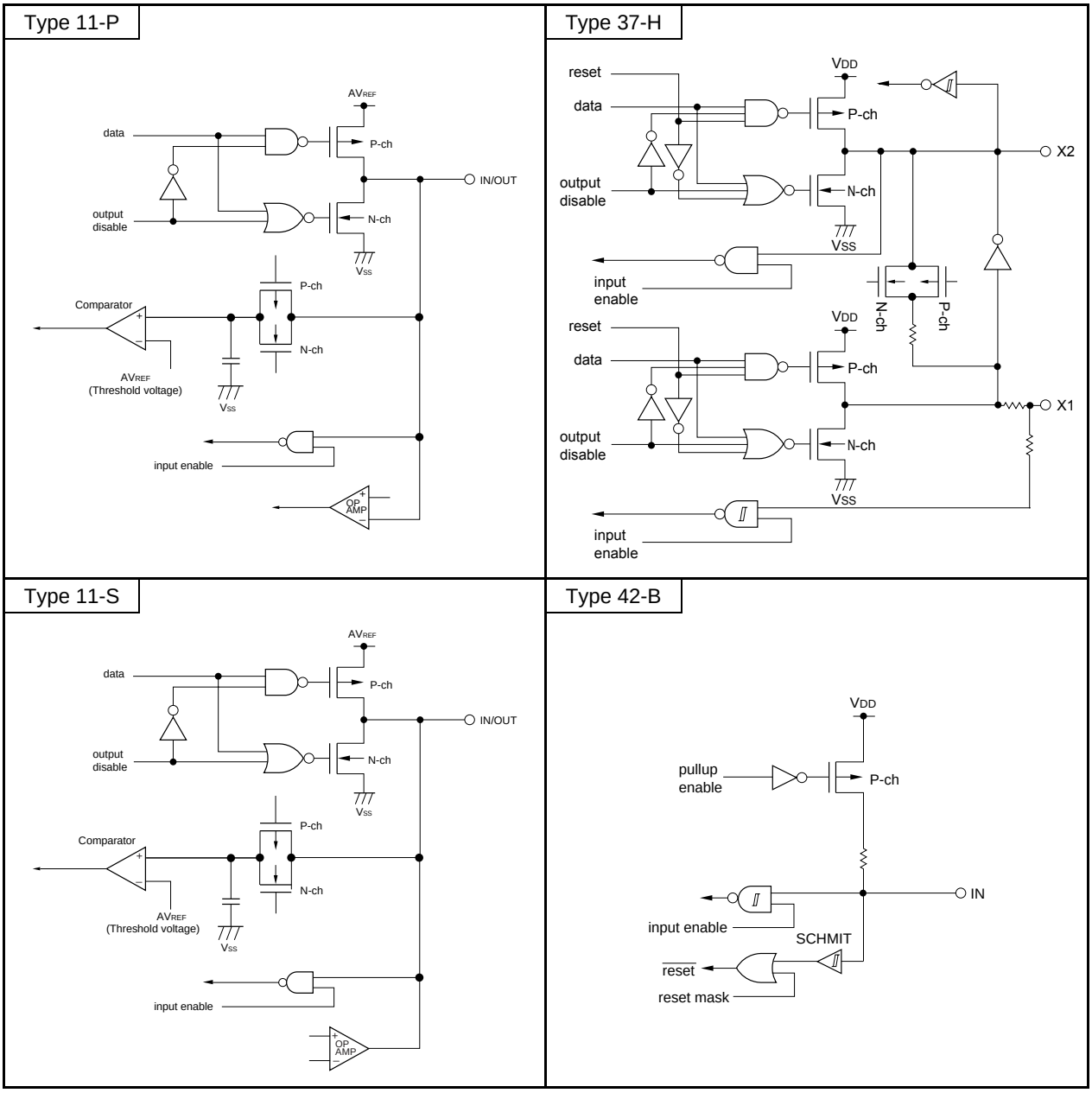


Figure 2-1. Pin I/O Circuit List (2/2)



CHAPTER 3 CPU ARCHITECTURE

3.1 Memory Space

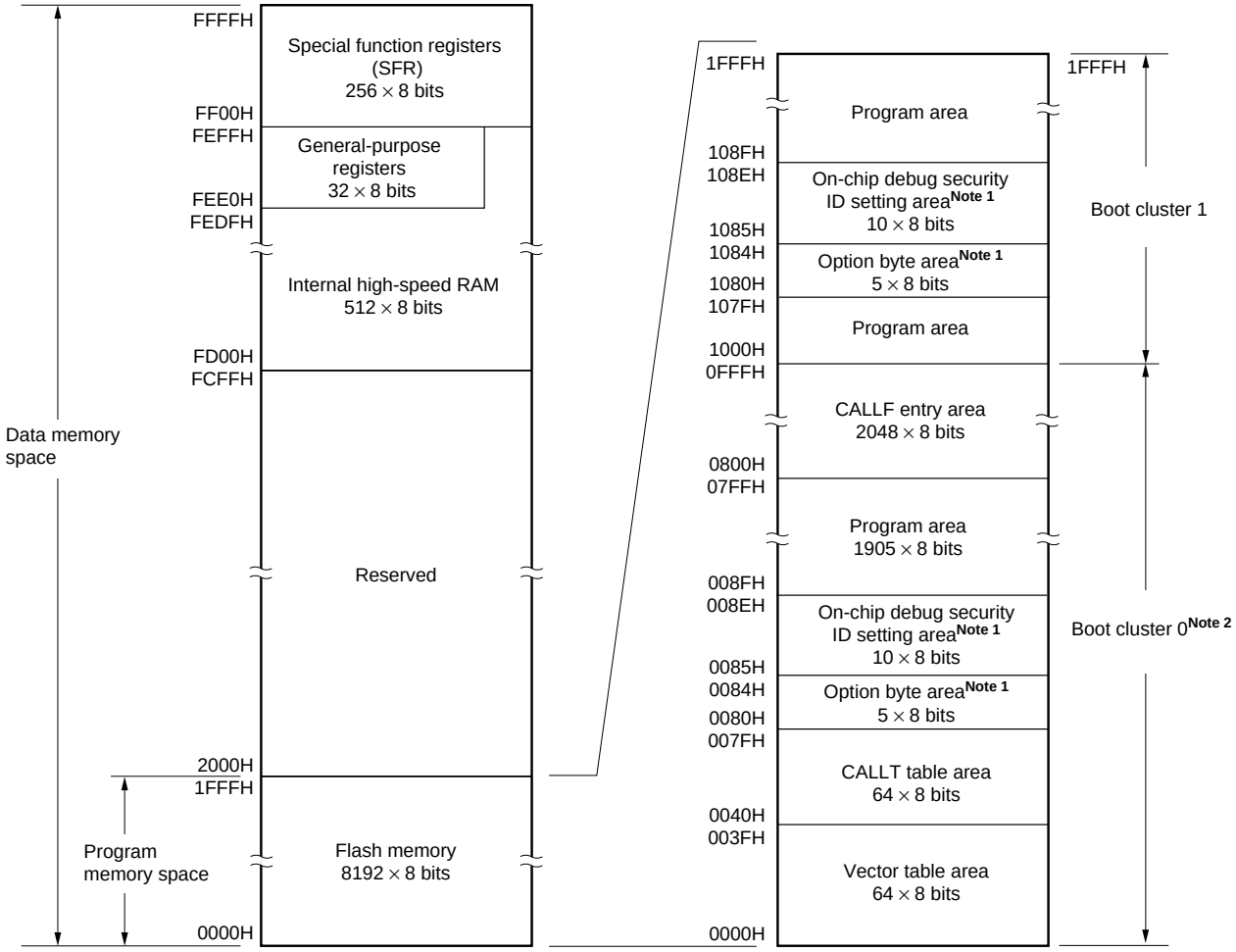
Products in the µPD79F7023, 79F7024 can access a 64 KB memory space. Figures 3-1, 3-2 show the memory maps.

Caution Reset signal generation makes the setting of the ROM area undefined. Therefore, set the value corresponding to each product as indicated below after release of reset.

Table 3-1. Set Values of Internal Memory Size Switching Register (IMS)

Products	IMS	ROM Capacity	Internal High-Speed RAM Capacity
µPD79F7023	42H	8 KB	512 bytes
µPD79F7024	04H	16 KB	768 bytes

Figure 3-1. Memory Map (µPD79F7023)



Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (refer to **21.6 Security Settings**).

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, refer to **Table 3-2 Correspondence Between Address Values and Block Numbers in Flash Memory**.

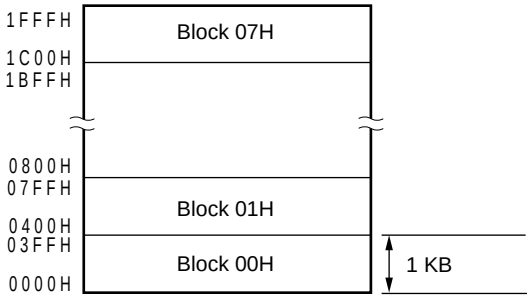
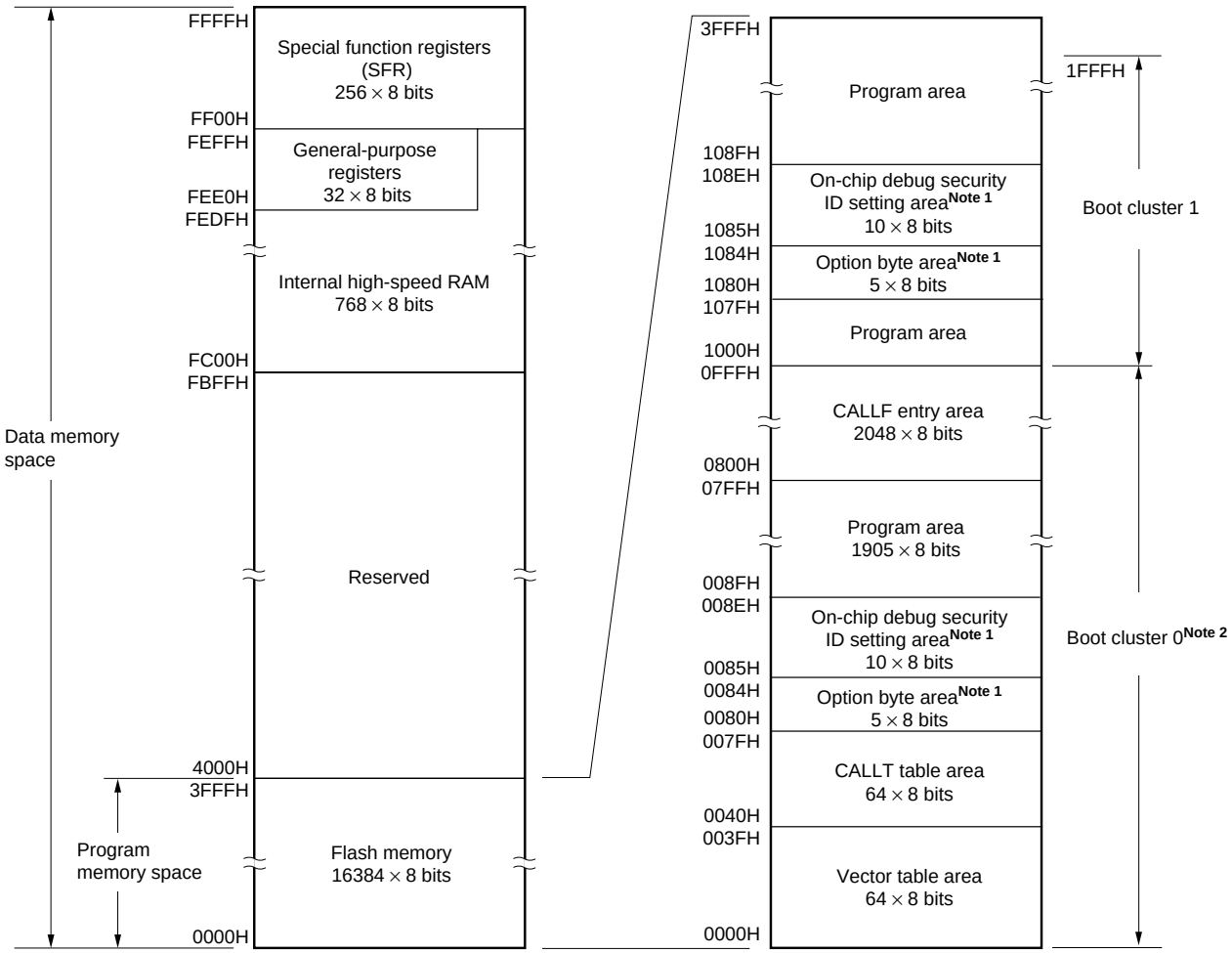


Figure 3-2. Memory Map (µPD79F7024)

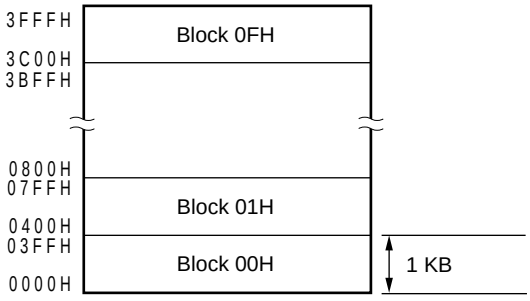


Notes 1. When boot swap is not used: Set the option bytes to 0080H to 0084H, and the on-chip debug security IDs to 0085H to 008EH.

When boot swap is used: Set the option bytes to 0080H to 0084H and 1080H to 1084H, and the on-chip debug security IDs to 0085H to 008EH and 1085H to 108EH.

2. Writing boot cluster 0 can be prohibited depending on the setting of security (refer to **21.6 Security Settings**).

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, refer to **Table 3-2 Correspondence Between Address Values and Block Numbers in Flash Memory**.



Correspondence between the address values and block numbers in the flash memory are shown below.

Table 3-2. Correspondence Between Address Values and Block Numbers in Flash Memory

Address Value	Block Number
0000H to 03FFH	00H
0400H to 07FFH	01H
0800H to 0BFFH	02H
0C00H to 0FFFH	03H
1000H to 13FFH	04H
1400H to 17FFH	05H
1800H to 1BFFH	06H
1C00H to 1FFFH	07H
2000H to 23FFH	08H
2400H to 27FFH	09H
2800H to 2BFFH	0AH
2C00H to 2FFFH	0BH
3000H to 33FFH	0CH
3400H to 37FFH	0DH
3800H to 3BFFH	0EH
3C00H to 3FFFH	0FH

Remark µPD79F7023: Block numbers 00H to 07H
µPD79F7024: Block numbers 00H to 0FH

3.1.1 Internal program memory space

The internal program memory space stores the program and table data. Normally, it is addressed with the program counter (PC).

µPD79F7023, 79F7024 incorporate internal ROM (flash memory), as shown below.

Table 3-3. Internal ROM Capacity

Product	Internal ROM	
	Structure	Capacity
µPD79F7023	Flash memory	8192 × 8 bits (0000H to 1FFFH)
µPD79F7024		16384 × 8 bits (0000H to 3FFFH)

The internal program memory space is divided into the following areas.

(1) Vector table area

The 64-byte area 0000H to 003FH is reserved as a vector table area. The program start addresses for branch upon reset or generation of each interrupt request are stored in the vector table area.

Of the 16-bit address, the lower 8 bits are stored at even addresses and the higher 8 bits are stored at odd addresses.

Table 3-4. Vector Table

Vector Table Address	Interrupt Source
0000H	$\overline{\text{RESET}}$ input, POC, LVI, WDT
0004H	INTLVI
0006H	INTP0
0008H	INTP1
000AH	INTCMP
0014H	INTSR0
0016H	INTST0
001AH	INTTMH1
0020H	INTTM000
0022H	INTTM010
0024H	INTAD
002AH	INTTM51
003EH	BRK

(2) CALLT instruction table area

The 64-byte area 0040H to 007FH can store the subroutine entry address of a 1-byte call instruction (CALLT).

(3) Option byte area

A 5-byte area of 0080H to 0084H and 1080H to 1084H can be used as an option byte area. Set the option byte at 0080H to 0084H when the boot swap is not used, and at 0080H to 0084H and 1080H to 1084H when the boot swap is used. For details, refer to **CHAPTER 20 OPTION BYTE**.

(4) On-chip debug security ID setting area

A 10-byte area of 0085H to 008EH and 1085H to 108EH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 0085H to 008EH when the boot swap is not used and at 0085H to 008EH and 1085H to 108EH when the boot swap is used. For details, refer to **CHAPTER 22 ON-CHIP DEBUG FUNCTION**.

(5) CALLF instruction entry area

The area 0800H to 0FFFH can perform a direct subroutine call with a 2-byte call instruction (CALLF).

3.1.2 Internal data memory space

μPD79F7023, 79F7024 incorporate the following RAMs.

(1) Internal high-speed RAM

Table 3-5. Internal High-Speed RAM Capacity

Product	Internal High-Speed RAM
μPD79F7023	512 × 8 bits (FD00H to FEFFH)
μPD79F7024	768 × 8 bits (FC00H to FEFFH)

The 32-byte area FEE0H to FEFFH is assigned to four general-purpose register banks consisting of eight 8-bit registers per bank.

This area cannot be used as a program area in which instructions are written and executed.

The internal high-speed RAM can also be used as a stack memory.

3.1.3 Special function register (SFR) area

On-chip peripheral hardware special function registers (SFRs) are allocated in the area FF00H to FFFFH (refer to **Table 3-6 Special Function Register List** in **3.2.3 Special function registers (SFRs)**).

Caution Do not access addresses to which SFRs are not assigned.

3.1.4 Data memory addressing

Addressing refers to the method of specifying the address of the instruction to be executed next or the address of the register or memory relevant to the execution of instructions.

Several addressing modes are provided for addressing the memory relevant to the execution of instructions for the µPD79F7023, 79F7024 microcontrollers, based on operability and other considerations. For areas containing data memory in particular, special addressing methods designed for the functions of special function registers (SFR) and general-purpose registers are available for use. Figures 3-3 and 3-4 show correspondence between data memory and addressing. For details of each addressing mode, refer to **3.4 Operand Address Addressing**.

Figure 3-3. Correspondence Between Data Memory and Addressing (µPD79F7023)

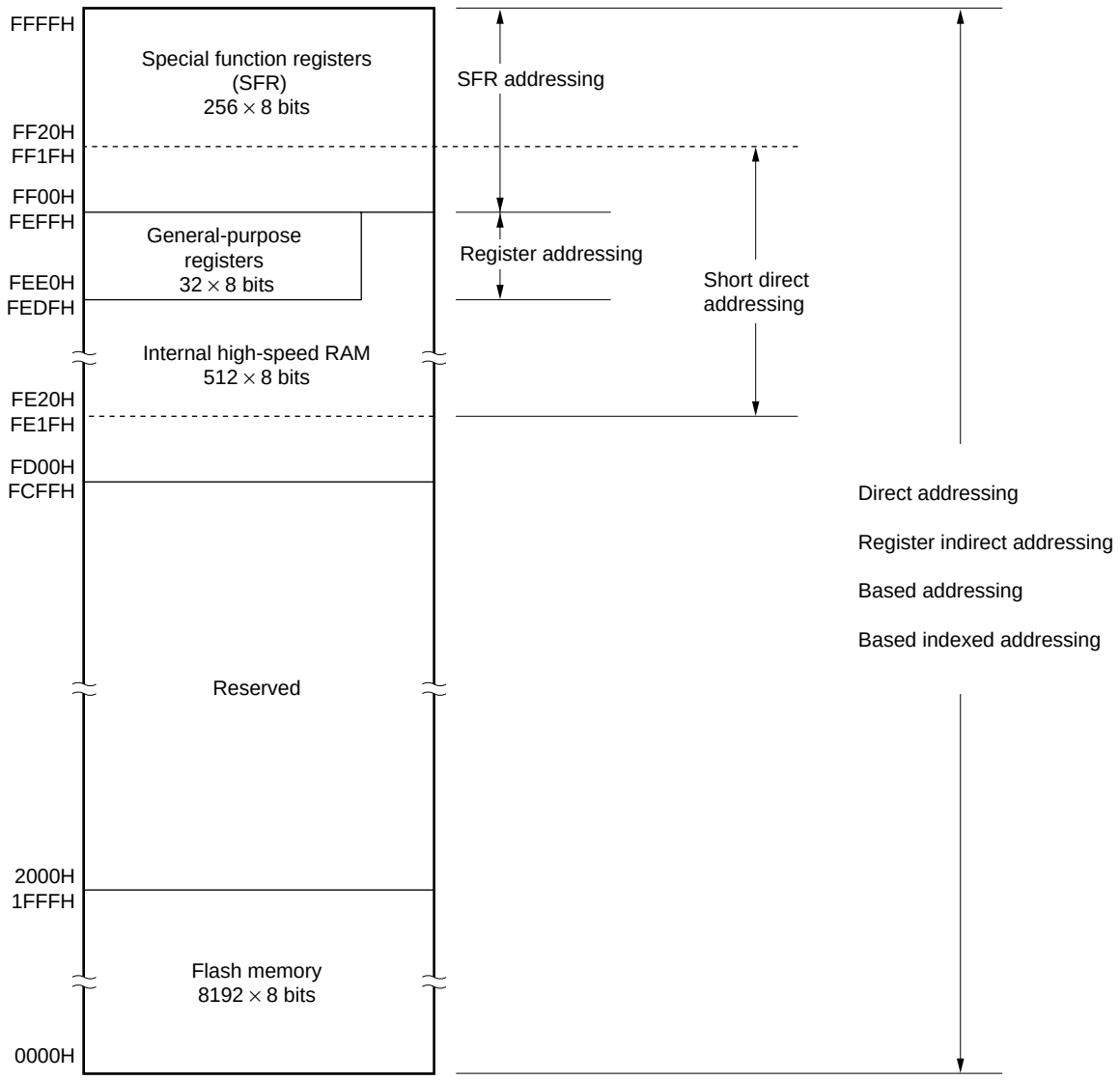
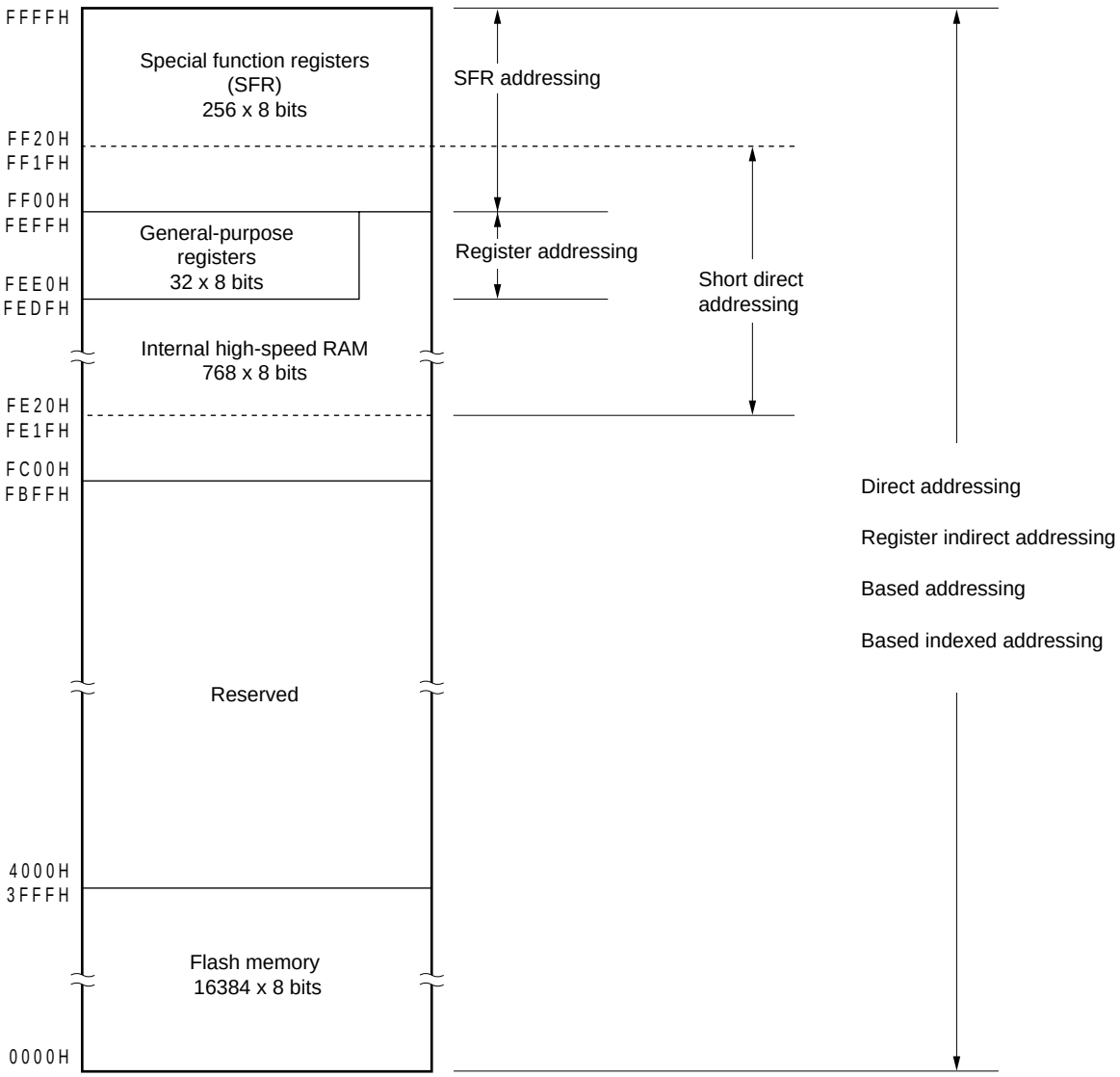


Figure 3-4. Correspondence Between Data Memory and Addressing (µPD79F7024)



3.2 Processor Registers

The μPD79F7023, 79F7024 incorporate the following processor registers.

3.2.1 Control registers

The control registers control the program sequence, statuses and stack memory. The control registers consist of a program counter (PC), a program status word (PSW) and a stack pointer (SP).

(1) Program counter (PC)

The program counter is a 16-bit register that holds the address information of the next program to be executed.

In normal operation, PC is automatically incremented according to the number of bytes of the instruction to be fetched.

When a branch instruction is executed, immediate data and register contents are set.

Reset signal generation sets the reset vector table values at addresses 0000H and 0001H to the program counter.

Figure 3-5. Format of Program Counter

	15															0
PC	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

(2) Program status word (PSW)

The program status word is an 8-bit register consisting of various flags set/reset by instruction execution.

Program status word contents are stored in the stack area upon vectored interrupt request acknowledge or PUSH PSW instruction execution and are restored upon execution of the RETB, RETI and POP PSW instructions.

Reset signal generation sets PSW to 02H.

Figure 3-6. Format of Program Status Word

	7							0
PSW	IE	Z	RBS1	AC	RBS0	0	ISP	CY

(a) Interrupt enable flag (IE)

This flag controls the interrupt request acknowledge operations of the CPU.

When 0, the IE flag is set to the interrupt disabled (DI) state, and all maskable interrupt requests are disabled.

When 1, the IE flag is set to the interrupt enabled (EI) state and interrupt request acknowledgment is controlled with an in-service priority flag (ISP), an interrupt mask flag for various interrupt sources, and a priority specification flag.

The IE flag is reset (0) upon DI instruction execution or interrupt acknowledgment and is set (1) upon EI instruction execution.

(b) Zero flag (Z)

When the operation result is zero, this flag is set (1). It is reset (0) in all other cases.

(c) Register bank select flags (RBS0 and RBS1)

These are 2-bit flags to select one of the four register banks.

In these flags, the 2-bit information that indicates the register bank selected by SEL RBn instruction execution is stored.

(d) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(e) In-service priority flag (ISP)

This flag manages the priority of acknowledgeable maskable vectored interrupts. When this flag is 0, low-level vectored interrupt requests specified by a priority specification flag register (PR0L, PR0H, PR1L) (refer to **14.3 (3) Priority specification flag registers (PR0L, PR0H, PR1L)**) can not be acknowledged. Actual request acknowledgment is controlled by the interrupt enable flag (IE).

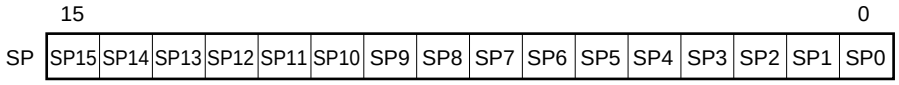
(f) Carry flag (CY)

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal high-speed RAM area can be set as the stack area.

Figure 3-7. Format of Stack Pointer



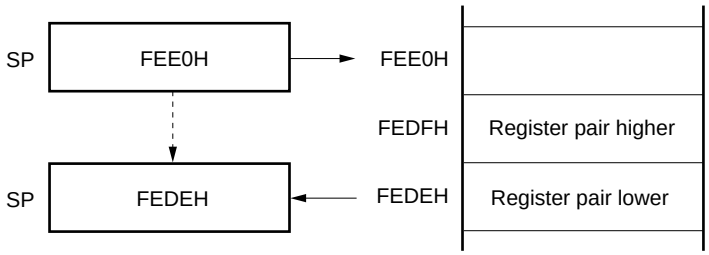
The SP is decremented ahead of write (save) to the stack memory and is incremented after read (restored) from the stack memory.

Each stack operation saves/restores data as shown in Figures 3-8 and 3-9.

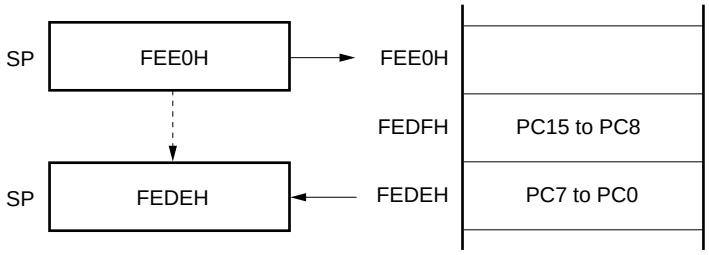
Caution Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack.

Figure 3-8. Data to Be Saved to Stack Memory

(a) PUSH rp instruction (when SP = FEE0H)



(b) CALL, CALLF, CALLT instructions (when SP = FEE0H)



(c) Interrupt, BRK instructions (when SP = FEE0H)

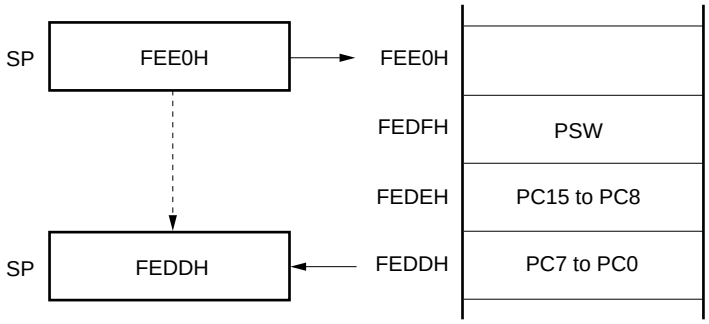
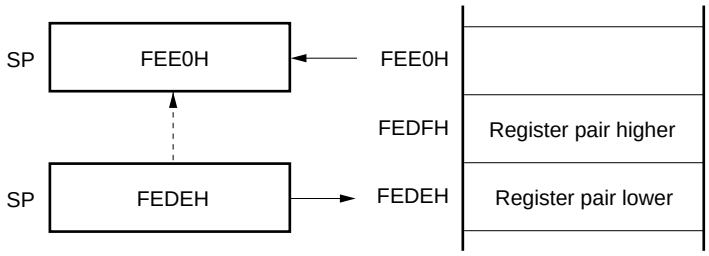
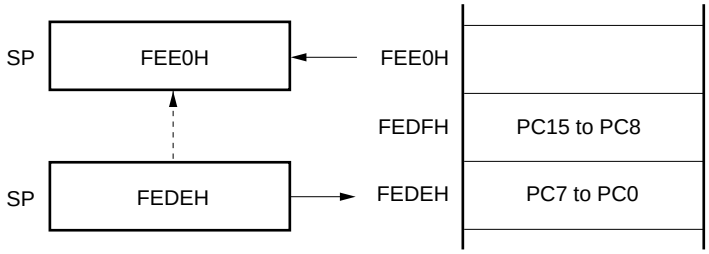


Figure 3-9. Data to Be Restored from Stack Memory

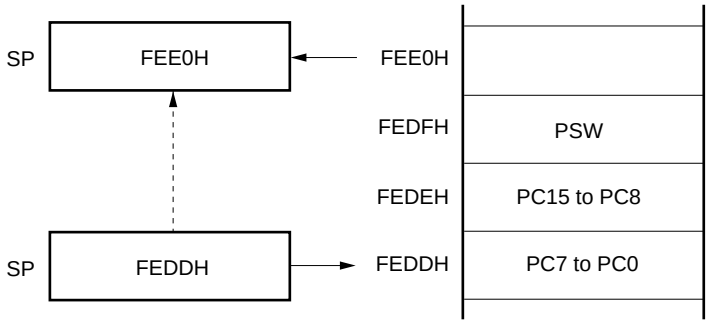
(a) POP rp instruction (when SP = FEDEH)



(b) RET instruction (when SP = FEDEH)



(c) RETI, RETB instructions (when SP = FEDDH)



3.2.2 General-purpose registers

General-purpose registers are mapped at particular addresses (FEE0H to FEFFH) of the data memory. The general-purpose registers consists of 4 banks, each bank consisting of eight 8-bit registers (X, A, C, B, E, D, L, and H).

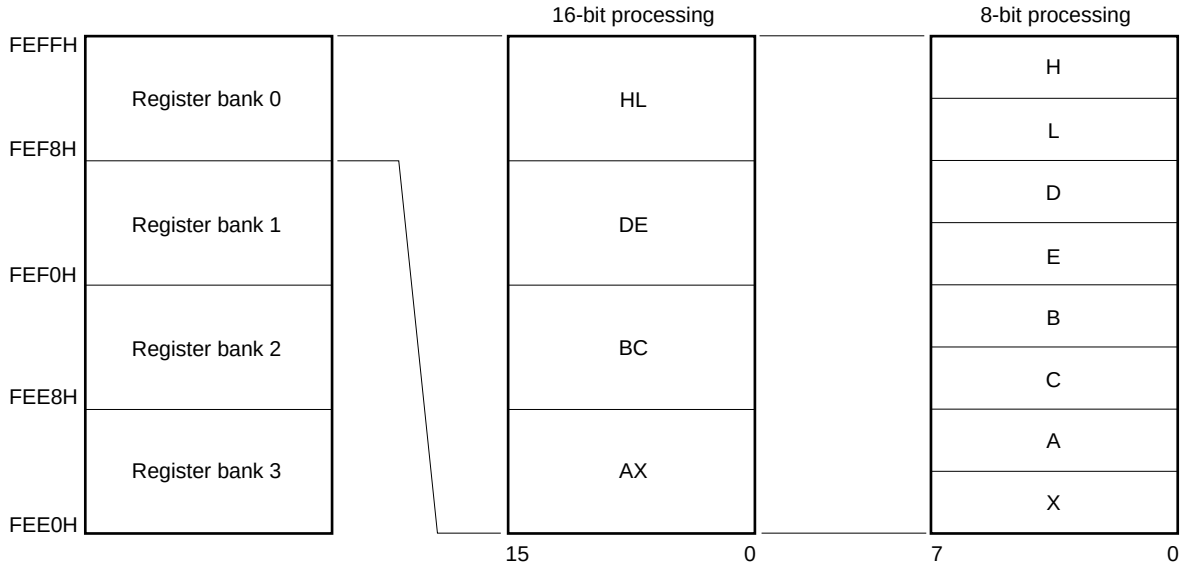
Each register can be used as an 8-bit register, and two 8-bit registers can also be used in a pair as a 16-bit register (AX, BC, DE, and HL).

These registers can be described in terms of function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL) and absolute names (R0 to R7 and RP0 to RP3).

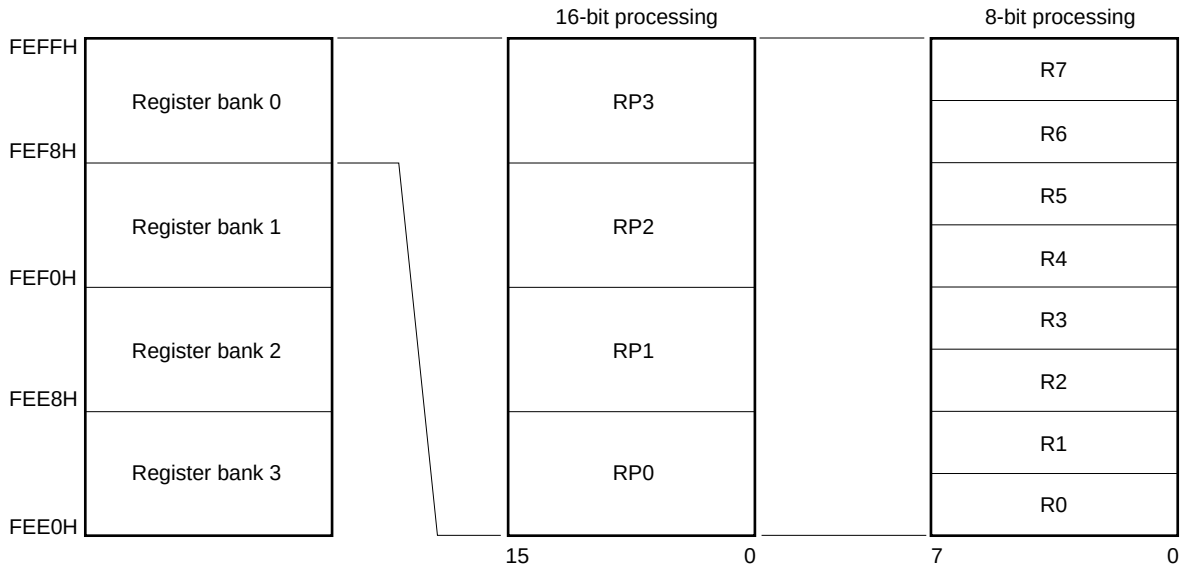
Register banks to be used for instruction execution are set by the CPU control instruction (SEL RBn). Because of the 4-register bank configuration, an efficient program can be created by switching between a register for normal processing and a register for interrupts for each bank.

Figure 3-10. Configuration of General-Purpose Registers

(a) Function name



(b) Absolute name



3.2.3 Special function registers (SFRs)

Unlike a general-purpose register, each special function register has a special function.

SFRs are allocated to the FF00H to FFFFH area.

Special function registers can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulatable bit units, 1, 8, and 16, depend on the special function register type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describe the symbol reserved by the assembler for the 1-bit manipulation instruction operand (sfr.bit).
  This manipulation can also be specified with an address.
- 8-bit manipulation
  Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr).
  This manipulation can also be specified with an address.
- 16-bit manipulation
  Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (sfrp).
  When specifying an address, describe an even address.

Table 3-6 gives lists of the special function registers. The meanings of items in the table are as follows.

- Symbol
  Symbol indicating the address of a special function register. It is a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0. When using the RA78K0, ID78K0-QB, and system simulator, symbols can be written as an instruction operand.
- R/W
  Indicates whether the corresponding special function register can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulatable bit units
  Indicates the manipulatable bit unit (1, 8, or 16). "–" indicates a bit unit for which manipulation is not possible.
- After reset
  Indicates each register status upon reset signal generation.

Table 3-6. Special Function Register List (1/4)

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF00H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF01H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF02H	P2	P27	P26	P25	P24	P23	P22	P21	P20	R/W	√	√	–	00H	
FF03H	P3	0	0	0	P34	P33	P32	P31	P30	R/W	√	√	–	00H	
FF04H to FF08H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF09H	ADCRH	–	–	–	–	–	–	–	–	R	–	√	–	00H	
FF0AH	RXB0	–	–	–	–	–	–	–	–	R	–	√	–	FFH	
FF0BH	TXS0	–	–	–	–	–	–	–	–	R/W	–	√	–	FFH	
FF0CH	P12	0	0	P125	0	0	P122	P121	0	R/W	√	√	–	00H	
FF0DH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF0EH	ADS	0	0	0	0	0	<ADS2>	<ADS1>	<ADS0>	R/W	√	√	–	00H	
FF0FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF10H	TM00	–	–	–	–	–	–	–	–	R	–	–	√	0000H	
FF11H		–	–	–	–	–	–	–	–						
FF12H	CR000	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	
FF13H		–	–	–	–	–	–	–	–						
FF14H	CR010	–	–	–	–	–	–	–	–	R/W	–	–	√	0000H	
FF15H		–	–	–	–	–	–	–	–						
FF16H to FF19H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF1AH	CMP01	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	
FF1BH	CMP11	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	
FF1CH to FF1EH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF1FH	TM51	–	–	–	–	–	–	–	–	R	–	√	–	00H	
FF20H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF21H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF22H	PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	R/W	√	√	–	FFH	
FF23H	PM3	1	1	1	PM34	PM33	PM32	PM31	PM30	R/W	√	√	–	FFH	
FF24H to FF2AH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

Table 3-6. Special Function Register List (2/4)

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF2BH	FPCTL	0	0	0	0	0	0	0	<FLMDPUP>	R/W	√	√	–	00H	
FF2CH	PM12	1	1	PM125	1	1	PM122	PM121	1	R/W	√	√	–	FFH	
FF2DH	RSTMASK	0	0	RSTM	0	0	0	0	0	R/W	√	√	–	00H	
FF2EH to FF32H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF33H	PU3	0	0	0	PU34	PU33	PU32	PU31	PU30	R/W	√	√	–	00H	
FF34H to FF3BH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF3CH	PU12	0	0	PU125	0	0	0	0	0	R/W	√	√	–	20H	
FF3DH	RMC	–	–	–	–	–	–	–	–	R/W	–	√	–	00H	
FF3EH to FF47H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF48H	EGP	0	0	0	0	0	EGP2	EGP1	EGP0	R/W	√	√	–	00H	
FF49H	EGN	0	0	0	0	0	EGN2	EGN1	EGN0	R/W	√	√	–	00H	
FF4AH to FF4FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF50H	ASIM0	<POWER0>	<TXE0>	<RXE0>	PS01	PS00	CL0	SL0	1	R/W	√	√	–	01H	
FF51H	BRGC0	TPS01	TPS00	0	MDL04	MDL03	MDL02	MDL01	MDL00	R/W	–	√	–	FFH	
FF52H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF53H	ASIS0	0	0	0	0	0	PE0	FE0	OVE0	R	–	√	–	00H	
FF54H to FF5FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF60H	AMPM	<OPAMP0E>	0	0	0	<OPAMP1E>	0	0	0	R/W	√	√	–	00H	
FF61H	CMPCTL	<CMP0EN>	<CDFS1>	<CDFS0>	<CMPOUTEN>	<CREGSEL>	<CFLG>	<COUTEN>	<CINV>	R/W	√	√	–	00H	
FF62H	CMPPC	0	0	0	0	0	0	<CMPCOMPC>	<CMPINPC>	R/W	√	√	–	00H	
FF63H to FF6FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

Table 3-6. Special Function Register List (3/4)

Address	Symbol	Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
		7	6	5	4	3	2	1	0		1	8	16		
FF70H	TMHMD1	<TMHE1>	CKS12	CKS11	CKS10	TMMD11	TMMD10	<TOLEV1>	<TOEN1>	R/W	√	√	–	00H	
FF71H	TMCYC1	0	0	0	0	0	RMC1	NRZB1	<NRZ1>	R/W	√	√	–	00H	
FF72H to FF85H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF86H	TMC00	0	0	0	0	TMC003	TMC002	TMC001	<OVF00>	R/W	√	√	–	00H	
FF87H	PRM00	ES110	ES100	ES010	ES000	0	0	PRM001	PRM000	R/W	√	√	–	00H	
FF88H	CRC00	0	0	0	0	0	CRC002	CRC001	CRC000	R/W	√	√	–	00H	
FF89H	TOC00	0	<OSPT00>	<OSPE00>	TOC004	<LVS00>	<LVR00>	TOC001	<TOE00>	R/W	√	√	–	00H	
FF8AH to FF8FH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF90H	ADM	<ADCS>	0	FR2	FR1	FR0	LV1	LV0	<ADCE>	R/W	√	√	–	00H	
FF91H to FF96H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF97H	ADPC	ADPC7	ADPC6	ADPC5	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0	R/W	√	√	–	00H	
FF98H	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF99H	WDTE	–	–	–	–	–	–	–	–	R/W	–	√	–	1AH/9AH[Note1]	
FF9AH to FF9EH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
FF9FH	OSCCTL	<EXCLK>	<OSCSEL>	0	0	0	0	0	0	R/W	√	√	–	00H	
FFA0H	RCM	<RSTS>	0	0	0	0	0	<LSRSTOP>	<RSTOP>	R/W	√	√	–	80H[Note2]	
FFA1H	MCM	0	0	0	0	0	<XSEL>	<MCS>	<MCM0>	R/W	√	√	–	00H	
FFA2H	MOC	<MSTOP>	0	0	0	0	0	0	0	R/W	√	√	–	80H	
FFA3H	OSTC	0	0	0	MOST11	MOST13	MOST14	MOST15	MOST16	R	√	√	–	00H	
FFA4H	OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0	R/W	–	√	–	05H	
FFA5H to FFABH	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

Notes 1. The reset value of WDTE is determined by setting of option byte.

2. The value of this register is 00H immediately after a reset release but automatically changes to 80H after oscillation accuracy stabilization of high-speed internal oscillator has been waited.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

Table 3-6. Special Function Register List (4/4)

Address	Symbol		Bit No.								R/W	Number of Bits Manipulated Simultaneously			After Reset	Reference page
			7	6	5	4	3	2	1	0		1	8	16		
FFACH	RESF		0	0	0	WDTRF	0	0	0	LVIRF	R	–	√	–	00H Note1	
FFADH to FFB0H	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFB1H	CR51		–	–	–	–	–	–	–	–	R/W	–	√	–	00H	
FFB2H	TCL51		0	0	0	0	0	TCL512	TCL511	TCL510	R/W	√	√	–	00H	
FFB3H	TMC51		<TCE51>	TMC516	0	0	0	0	TMC511	0	R/W	√	√	–	00H	
FFB4H to FFBDH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFBEH	LVIM		<LVION>	0	0	0	0	0	<LVIMD>	<LVIF>	R/W	√	√	–	00H Note2	
FFBFH	LVIS		0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0	R/W	√	√	–	00H Note3	
FFC0H to FFDFH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFE0H	IF0	IF0L	0	0	0	0	<CMPIF>	<PIF1>	<PIF0>	<LVIIF>	R/W	√	√	√	00H	
FFE1H		IF0H	<TMIF010>	<TMIF000>	0	0	<TMIFH1>	0	<STIF0>	<SRIF0>	R/W	√	√		00H	
FFE2H	IF1	IF1L	0	0	0	0	<TMIF51>	0	0	<ADIF>	R/W	√	√	√	00H	
FFE3H		–	0	0	0	0	0	0	0	0	–	–	–		00H	
FFE4H	MK0	MK0L	1	1	1	1	<CMPMK>	<PMK1>	<PMK0>	<LVIMK>	R/W	√	√	√	FFH	
FFE5H		MK0H	<TMMK010>	<TMMK000>	1	1	<TMMKH1>	1	<STMK0>	<SRMK0>	R/W	√	√		FFH	
FFE6H	MK1	MK1L	1	1	1	1	<TMMK51>	1	1	<ADMK>	R/W	√	√	√	FFH	
FFE7H		–	1	1	1	1	1	1	1	1	–	–	–		FFH	
FFE8H	PR0	PR0L	1	1	1	1	<CMPPR>	<PPR1>	<PPR0>	<LVIPR>	R/W	√	√	√	FFH	
FFE9H		PR0H	<TMPR010>	<TMPR000>	1	1	<TMPRH1>	1	<STPR0>	<SRPR0>	R/W	√	√		FFH	
FFEAH	PR1	PR1L	1	1	1	1	<TMPR51>	1	1	<ADPR>	R/W	√	√	√	FFH	
FFEBH		–	1	1	1	1	1	1	1	1	–	–	–		FFH	
FFECH to FFEFH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFF0H	IMS		RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	R/W	–	√	–	CFH Note4	
FFF1H to FFFAH	–		–	–	–	–	–	–	–	–	–	–	–	–	–	–
FFFBH	PCC		0	0	0	0	0	PCC2	PCC1	PCC0	R/W	√	√	–	01H	

Notes 1. The reset value of RESF varies depending on the reset source.

2. The reset values of LVIM vary depending on the reset source and setting of option byte.

3. The reset values of LVIS vary depending on the reset source.

4. Reset signal generation makes the setting of the ROM area undefined. Therefore, set the value corresponding to each product as indicated in Table 3-1 after release of reset.

Remark For a bit name enclosed in angle brackets (<>), the bit name is defined as a reserved word in the RA78K0, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0.

3.3 Instruction Address Addressing

An instruction address is determined by contents of the program counter (PC) and is normally incremented (+1 for each byte) automatically according to the number of bytes of an instruction to be fetched each time another instruction is executed. When a branch instruction is executed, the branch destination information is set to PC and branched by the following addressing (for details of instructions, refer to the **78K/0 Series Instructions User's Manual (U12326E)**).

3.3.1 Relative addressing

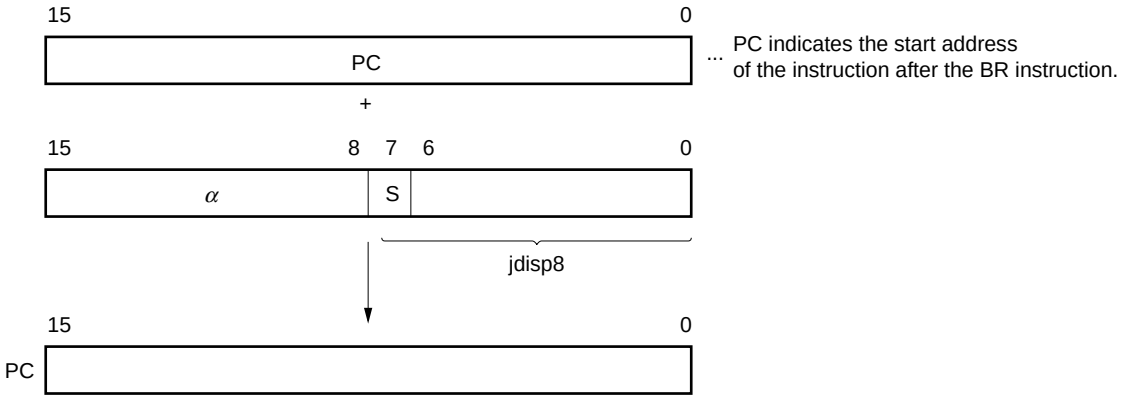
[Function]

The value obtained by adding 8-bit immediate data (displacement value: jdisp8) of an instruction code to the start address of the following instruction is transferred to the program counter (PC) and branched. The displacement value is treated as signed two's complement data (−128 to +127) and bit 7 becomes a sign bit.

In other words, relative addressing consists of relative branching from the start address of the following instruction to the −128 to +127 range.

This function is carried out when the BR $addr16 instruction or a conditional branch instruction is executed.

[Illustration]



When S = 0, all bits of α are 0.
When S = 1, all bits of α are 1.

3.3.2 Immediate addressing

[Function]

Immediate data in the instruction word is transferred to the program counter (PC) and branched.

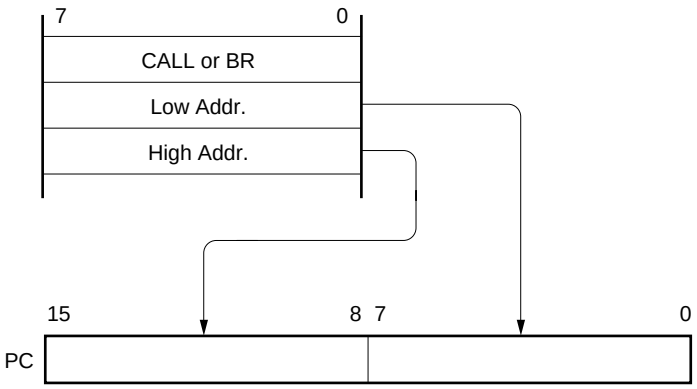
This function is carried out when the CALL !addr16 or BR !addr16 or CALLF !addr11 instruction is executed.

CALL !addr16 and BR !addr16 instructions can be branched to the entire memory space.

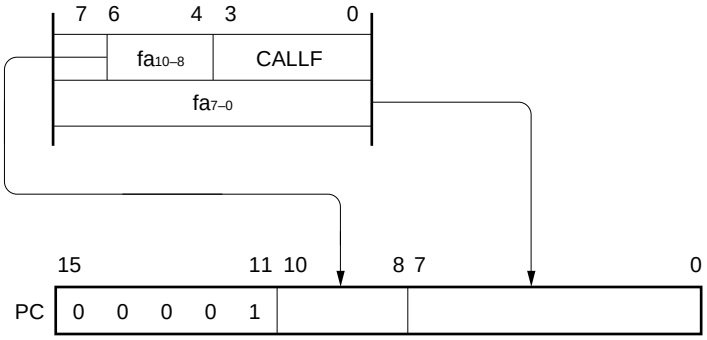
The CALLF !addr11 instruction is branched to the 0800H to 0FFFH area.

[Illustration]

In the case of CALL !addr16 and BR !addr16 instructions



In the case of CALLF !addr11 instruction



3.3.3 Table indirect addressing

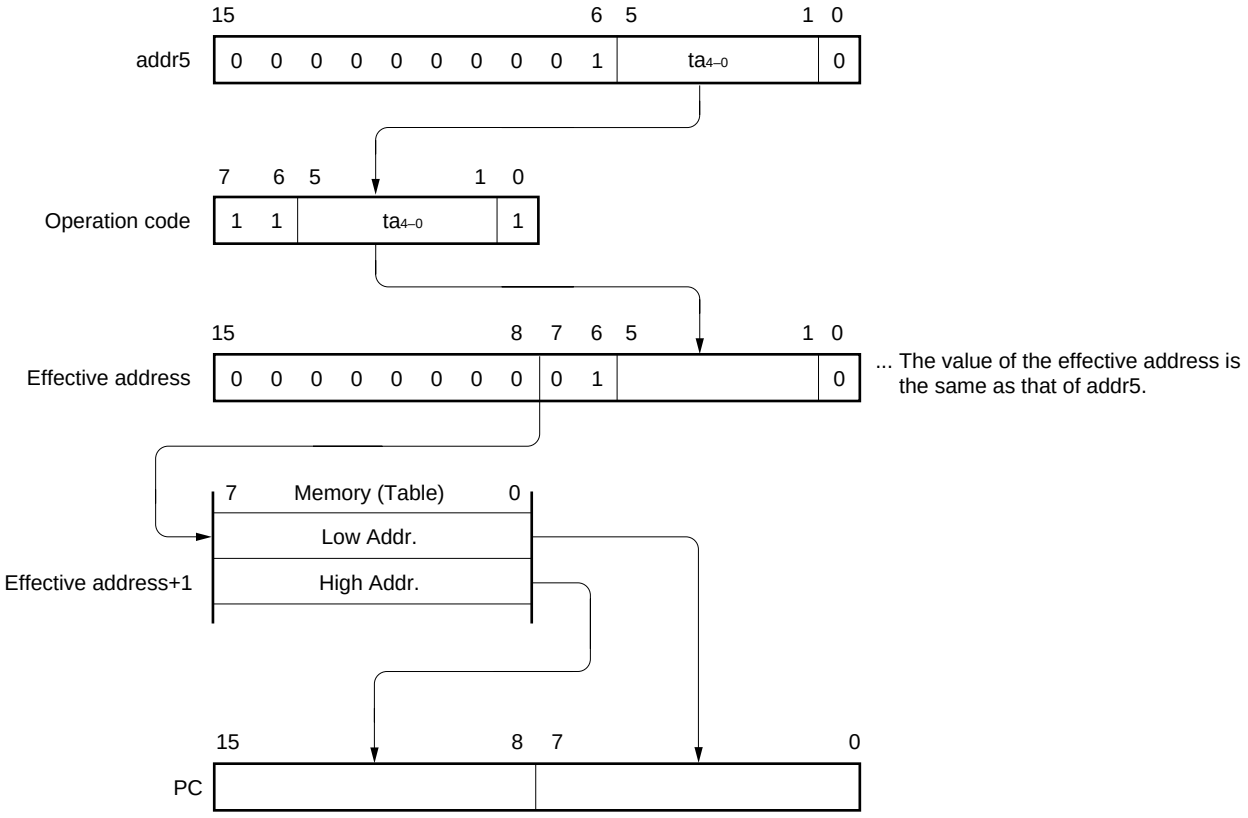
[Function]

Table contents (branch destination address) of the particular location to be addressed by bits 1 to 5 of the immediate data of an operation code are transferred to the program counter (PC) and branched.

This function is carried out when the CALLT [addr5] instruction is executed.

This instruction references the address that is indicated by addr5 and is stored in the memory table from 0040H to 007FH, and allows branching to the entire memory space.

[Illustration]



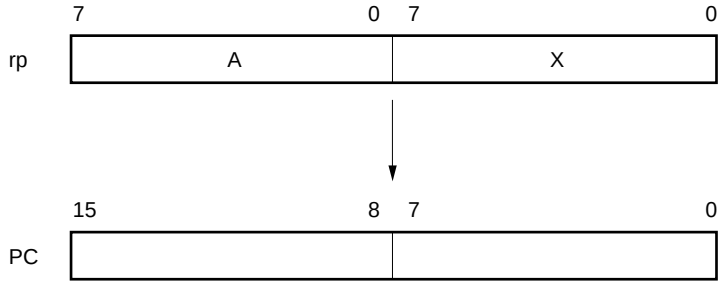
3.3.4 Register addressing

[Function]

Register pair (AX) contents to be specified with an instruction word are transferred to the program counter (PC) and branched.

This function is carried out when the BR AX instruction is executed.

[Illustration]



3.4 Operand Address Addressing

The following methods are available to specify the register and memory (addressing) to undergo manipulation during instruction execution.

3.4.1 Implied addressing

[Function]

The register that functions as an accumulator (A and AX) among the general-purpose registers is automatically (implicitly) addressed.

Of the μPD79F7023, 79F7024 instruction words, the following instructions employ implied addressing.

Instruction	Register to Be Specified by Implied Addressing
MULU	A register for multiplicand and AX register for product storage
DIVUW	AX register for dividend and quotient storage
ADJBA/ADJBS	A register for storage of numeric values that become decimal correction targets
ROR4/ROL4	A register for storage of digit data that undergoes digit rotation

[Operand format]

Because implied addressing can be automatically determined with an instruction, no particular operand format is necessary.

[Description example]

In the case of MULU X

With an 8-bit × 8-bit multiply instruction, the product of the A register and X register is stored in AX. In this example, the A and AX registers are specified by implied addressing.

3.4.2 Register addressing

[Function]

The general-purpose register to be specified is accessed as an operand with the register bank select flags (RBS0 to RBS1) and the register specify codes of an operation code.

Register addressing is carried out when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the operation code.

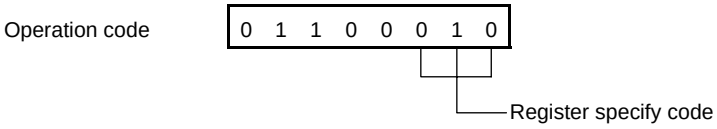
[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

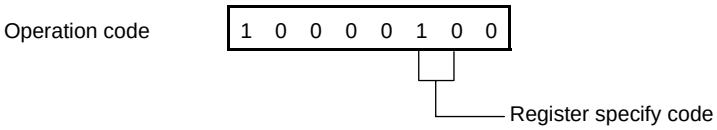
'r' and 'rp' can be described by absolute names (R0 to R7 and RP0 to RP3) as well as function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL).

[Description example]

MOV A, C; when selecting C register as r



INCW DE; when selecting DE register pair as rp



3.4.3 Direct addressing

[Function]

The memory to be manipulated is directly addressed with immediate data in an instruction word becoming an operand address.

This addressing can be carried out for all of the memory spaces.

[Operand format]

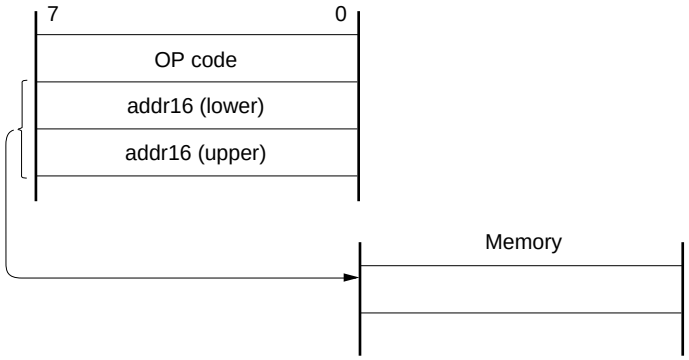
Identifier	Description
addr16	Label or 16-bit immediate data

[Description example]

MOV A, !0FE00H; when setting !addr16 to FE00H

Operation code	1 0 0 0 1 1 1 0	OP code
	0 0 0 0 0 0 0 0	00H
	1 1 1 1 1 1 1 0	FEH

[Illustration]



3.4.4 Short direct addressing

[Function]

The memory to be manipulated in the fixed space is directly addressed with 8-bit data in an instruction word.

This addressing is applied to the 256-byte space FE20H to FF1FH. Internal high-speed RAM and special function registers (SFRs) are mapped at FE20H to FEFFH and FF00H to FF1FH, respectively.

The SFR area (FF00H to FF1FH) where short direct addressing is applied is a part of the overall SFR area. Ports that are frequently accessed in a program and compare and capture registers of the timer/event counter are mapped in this area, allowing SFRs to be manipulated with a small number of bytes and clocks.

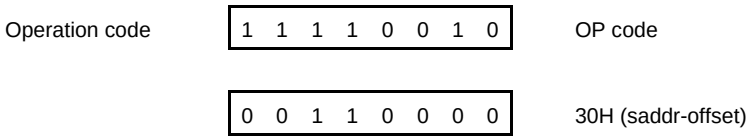
When 8-bit immediate data is at 20H to FFH, bit 8 of an effective address is set to 0. When it is at 00H to 1FH, bit 8 is set to 1. Refer to the **[Illustration]** shown below.

[Operand format]

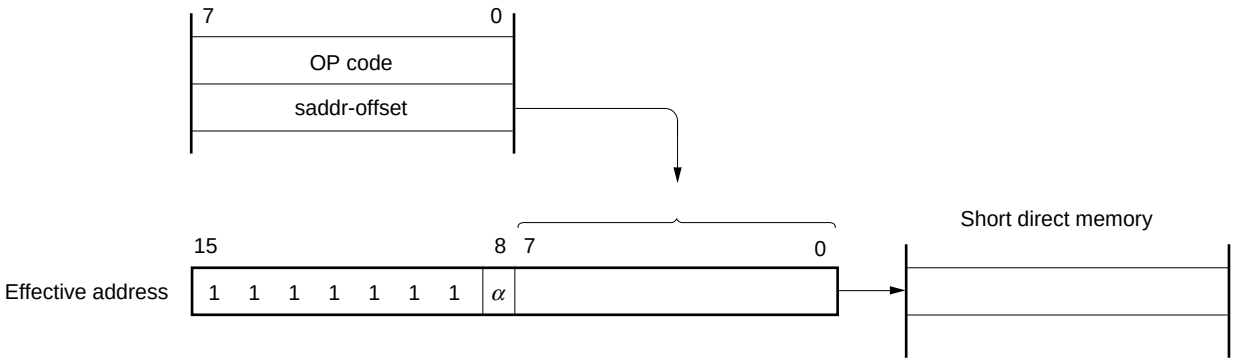
Identifier	Description
saddr	Immediate data that indicate label or FE20H to FF1FH
saddrp	Immediate data that indicate label or FE20H to FF1FH (even address only)

[Description example]

```
LB1 EQU 0FE30H   ; Defines FE30H by LB1.
      :
MOV LB1, A       ; When LB1 indicates FE30H of the saddr area and the value of register A is transferred to that
                   address
```



[Illustration]



When 8-bit immediate data is 20H to FFH, $\alpha = 0$

When 8-bit immediate data is 00H to 1FH, $\alpha = 1$

3.4.5 Special function register (SFR) addressing

[Function]

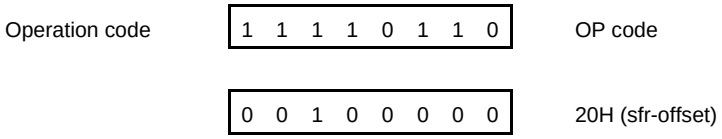
A memory-mapped special function register (SFR) is addressed with 8-bit immediate data in an instruction word. This addressing is applied to the 240-byte spaces FF00H to FFCFH and FFE0H to FFFFH. However, the SFRs mapped at FF00H to FF1FH can be accessed with short direct addressing.

[Operand format]

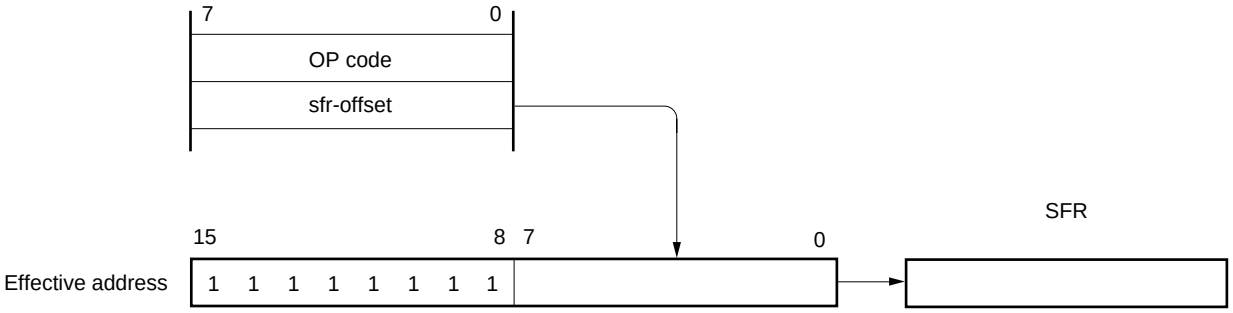
Identifier	Description
sfr	Special function register name
sfrp	16-bit manipulatable special function register name (even address only)

[Description example]

MOV PM0, A; when selecting PM0 (FF20H) as sfr



[Illustration]



3.4.6 Register indirect addressing

[Function]

Register pair contents specified by a register pair specify code in an instruction word and by a register bank select flag (RBS0 and RBS1) serve as an operand address for addressing the memory.

This addressing can be carried out for all of the memory spaces.

[Operand format]

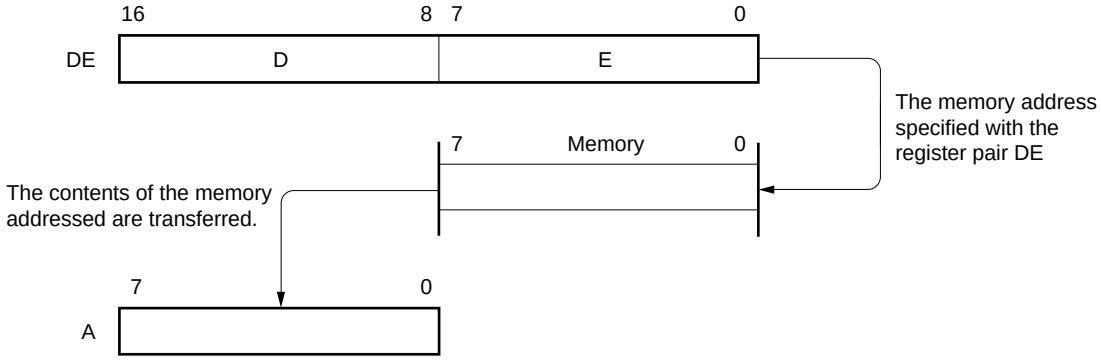
Identifier	Description
–	[DE], [HL]

[Description example]

MOV A, [DE]; when selecting [DE] as register pair

Operation code	1	0	0	0	0	1	0	1

[Illustration]



3.4.7 Based addressing

[Function]

8-bit immediate data is added as offset data to the contents of the base register, that is, the HL register pair in the register bank specified by the register bank select flag (RBS0 and RBS1), and the sum is used to address the memory. Addition is performed by expanding the offset data as a positive number to 16 bits. A carry from the 16th bit is ignored.

This addressing can be carried out for all of the memory spaces.

[Operand format]

Identifier	Description
–	[HL + byte]

[Description example]

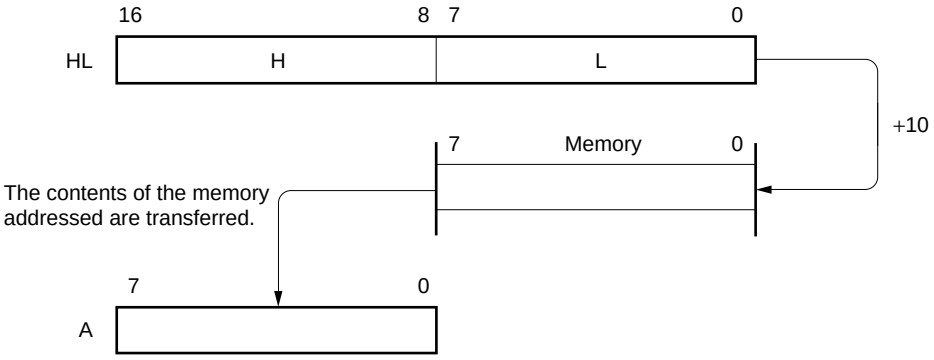
MOV A, [HL + 10H]; when setting byte to 10H

Operation code

1	0	1	0	1	1	1	0

0	0	0	1	0	0	0	0

[Illustration]



3.4.8 Based indexed addressing

[Function]

The B or C register contents specified in an instruction word are added to the contents of the base register, that is, the HL register pair in the register bank specified by the register bank select flag (RBS0 and RBS1), and the sum is used to address the memory. Addition is performed by expanding the B or C register contents as a positive number to 16 bits. A carry from the 16th bit is ignored.

This addressing can be carried out for all of the memory spaces.

[Operand format]

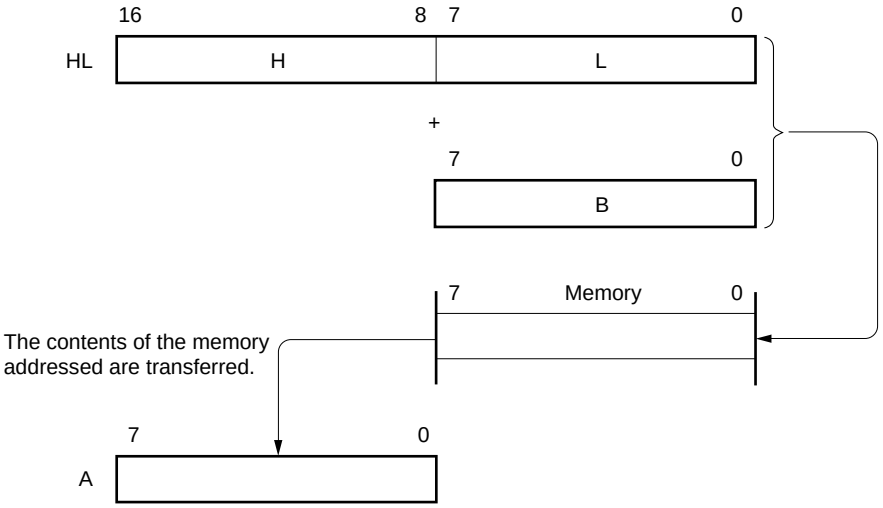
Identifier	Description
–	[HL + B], [HL + C]

[Description example]

MOV A, [HL +B]; when selecting B register

Operation code	1	0	1	0	1	0	1	1

[Illustration]



3.4.9 Stack addressing

[Function]

The stack area is indirectly addressed with the stack pointer (SP) contents.

This addressing method is automatically employed when the PUSH, POP, subroutine call and return instructions are executed or the register is saved/reset upon generation of an interrupt request.

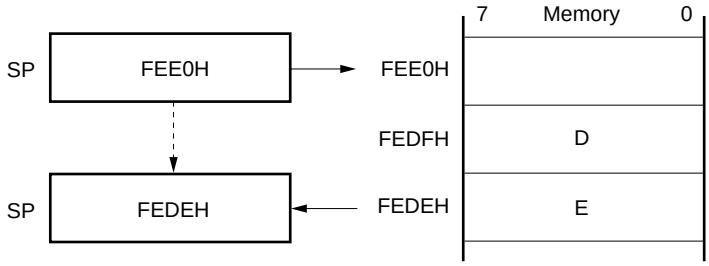
With stack addressing, only the internal high-speed RAM area can be accessed.

[Description example]

PUSH DE; when saving DE register

Operation code	1	0	1	1	0	1	0	1

[Illustration]



CHAPTER 4 PORT FUNCTIONS

4.1 Port Functions

There are two types of pin I/O buffer power supplies: AV_{REF} and V_{DD}. The relationship between these power supplies and the pins is shown below.

Table 4-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF}	P20 to P27
V_{DD}	Pins other than P20 to P27

µPD79F7023, 79F7024 microcontrollers are provided with digital I/O ports, which enable variety of control operations. The functions of each port are shown in Table 4-2.

In addition to the function as digital I/O ports, these ports have several alternate functions. For details of the alternate functions, refer to **CHAPTER 2 PIN FUNCTIONS**.

Table 4-2. Port Functions

Function Name	I/O	Function	After Reset	Alternate Function
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Analog input	ANI0/AMP0-
P21				ANI1/AMP0OUT
P22				ANI2/AMP0+
P23				ANI3
P24				ANI4
P25				AMP1-
P26				AMP1OUT
P27				AMP1+
P30	I/O	Port 3. 5-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOH1/TI51/INTP0
P31			Analog input	TxD0/CMPCOM
P32				RxD0/CMPIN
P33			Input port	TI000/INTP1
P34				TO00/TI010/CMPOUT
P121	I/O	Port 12. P121, P122 is 2-bit I/O port. P125 is 1-bit input-only port. For only P125, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	X1/TOOLC0
P122				X2/EXCLK/TOOLD0
P125	Input		Reset input	$\overline{\text{RESET}}$

4.2 Port Configuration

Ports include the following hardware.

Table 4-3. Port Configuration

Item	Configuration
Control registers	Port mode registers (PMxx): PM2, PM3, PM12 Port registers (Pxx): P2, P3, P12 Pull-up resistor option registers (PUxx): PU3, PU12 Reset pin mode register (RSTMASK) A/D port configuration register (ADPC)
Port	Total: 16 (CMOS I/O: 15, CMOS input: 1)
Pull-up resistor	Total: 6

4.2.1 Port 2

Port 2 is an I/O port with an output latch. Port 2 can be set to the input mode or output mode in 1-bit units using port mode register 2 (PM2).

This port can also be used for A/D converter analog input, and operational amplifier I/O.

When using P20/AMP0-/ANI0 to P24/ANI4, set the registers according to the pin function to be used (refer to **Tables 4-4** to **4-8**).

To use P20/AMP0-/ANI0 to P24/ANI4 as a digital input or a digital output, it is recommended to select a pin to use starting with the furthest pin from AV_{REF} (P24/ANI4 pin). To use P20/AMP0-/ANI0 to P24/ANI4 as an analog input, it is recommended to select a pin to use starting with the closest pin to V_{SS} (P24/ANI4 pin).

Reset signal generation sets port 2 to analog input.

Figures 4-1 to 4-7 show block diagrams of port 2.

Caution Make the AV_{REF} pin the same potential as the V_{DD} pin when port 2 is used as a digital port.

Table 4-4. Setting Functions of P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins

ADPC Register	PM2 Register	OPAMP0E bit	ADS Register (n = 0, 2)	P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins
Digital I/O selection	Input mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital input
	Output mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital output
Analog input selection	Input mode	0	Selects ANIn.	Analog input (to be converted into digital signals)
			Does not select ANIn.	Analog input (not to be converted into digital signals)
		1	Selects ANIn.	Analog input (to be converted into digital signals), operational amplifier 0 input
			Does not select ANIn.	Operational amplifier 0 input
	Output mode	–	–	Setting prohibited

Remark ADPC: A/D port configuration register
PM2: Port mode register 2
OPAMP0E: Bit 7 of operational amplifier control register (AMPM)
ADS: Analog input channel specification register

Table 4-5. Setting Functions of P21/ANI1/AMP0OUT Pin

ADPC Register	PM2 Register	OPAMP1E bit	ADS Register	P21/ANI1/AMP0OUT Pin
Digital I/O selection	Input mode	0	Selects ANI1.	Setting prohibited
			Does not select ANI1.	Digital input
		1	–	Setting prohibited
	Output mode	0	Selects ANI1.	Setting prohibited
			Does not select ANI1.	Digital output
		1	–	Setting prohibited
Analog I/O selection	Input mode	0	Selects ANI1.	Analog input (to be converted into digital signals)
			Does not select ANI1.	Analog input (not to be converted into digital signals)
		1	Selects ANI1.	Operational amplifier 0 output (to be converted into digital signals)
			Does not select ANI1.	Operational amplifier 0 output (not to be converted into digital signals)
	Output mode	–	–	Setting prohibited

Table 4-6. Setting Functions of P23/ANI3, P24/ANI4 Pins

ADPC Register	PM2 Register	ADS Register(n = 3, 4)	P23/ANI3, P24/ANI4 Pins
Digital I/O selection	Input mode	Selects ANIn.	Setting prohibited
		Does not select ANIn.	Digital input
	Output mode	Selects ANIn.	Setting prohibited
		Does not select ANIn.	Digital output
Analog input selection	Input mode	Selects ANIn.	Analog input (to be converted into digital signals)
		Does not select ANIn.	Analog input (not to be converted into digital signals)
	Output mode	–	Setting prohibited

Remark ADPC: A/D port configuration register
PM2: Port mode register 2
OPAMP0E: Bit 7 of operational amplifier control register (AMPM)
ADS: Analog input channel specification register

Table 4-7. Setting Functions of P25/AMP1-, P27/AMP1+ Pins

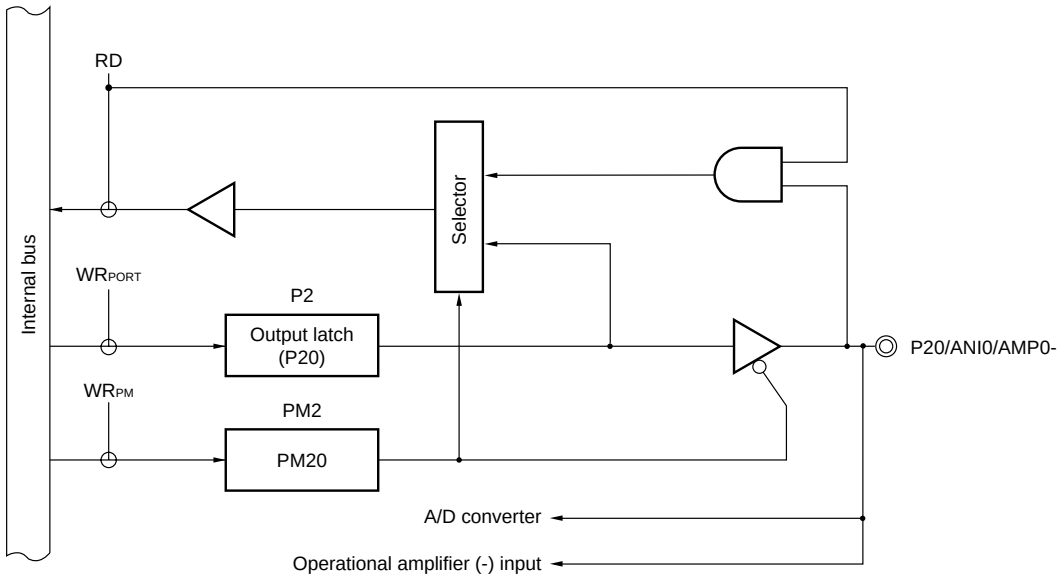
ADPC Register	PM2 Register	OPAMP1E bit	P25/AMP1-, P27/AMP1+ Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	0	Analog input (to be converted into digital signals)
		1	Operational amplifier 1 input
	Output mode	–	Setting prohibited

Table 4-8. Setting Functions of P26/AMP1OUT Pin

ADPC Register	PM2 Register	OPAMP1E bit	P23/ANI3, P24/ANI4 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	0	Analog input (to be converted into digital signals)
		1	Operational amplifier 1 output
	Output mode	–	Setting prohibited

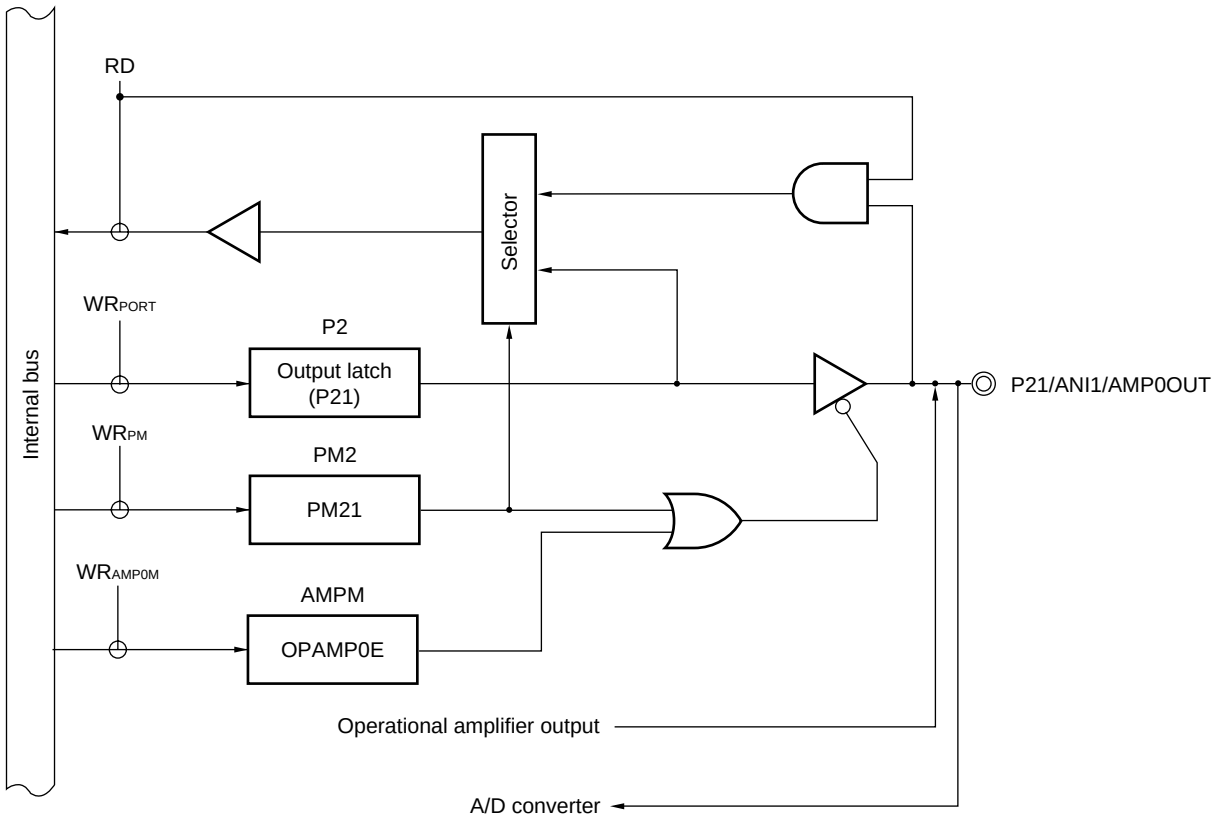
Remark ADPC: A/D port configuration register
PM2: Port mode register 2
OPAMP0E: Bit 7 of operational amplifier control register (AMPM)

Figure 4-1. Block Diagram of P20



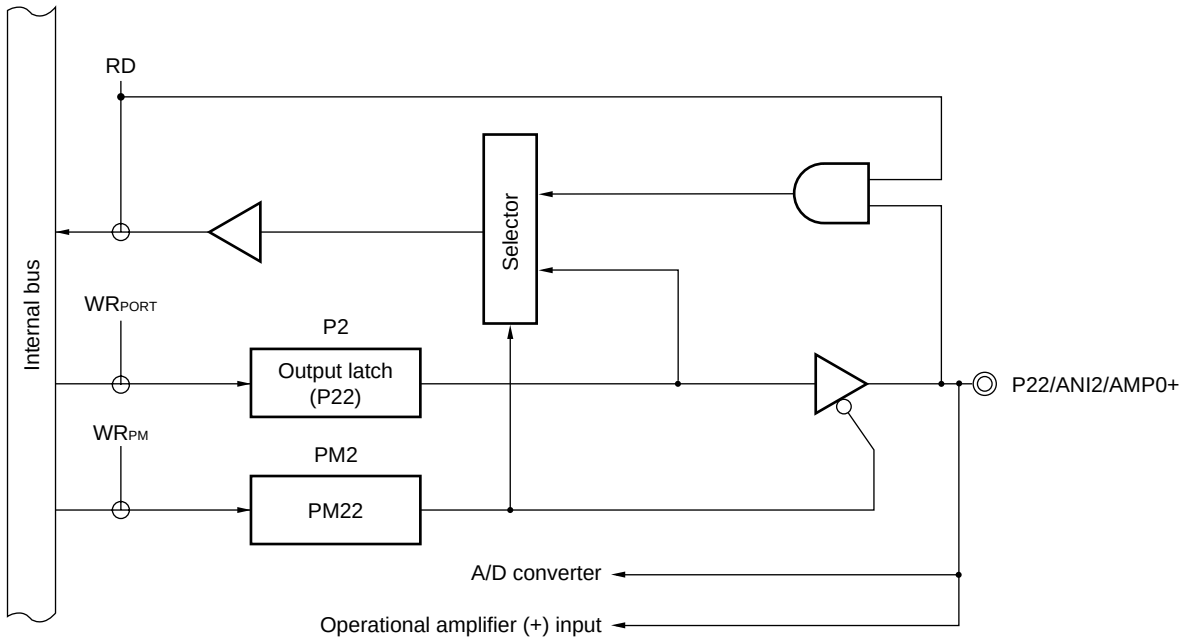
P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Figure 4-2. Block Diagram of P21



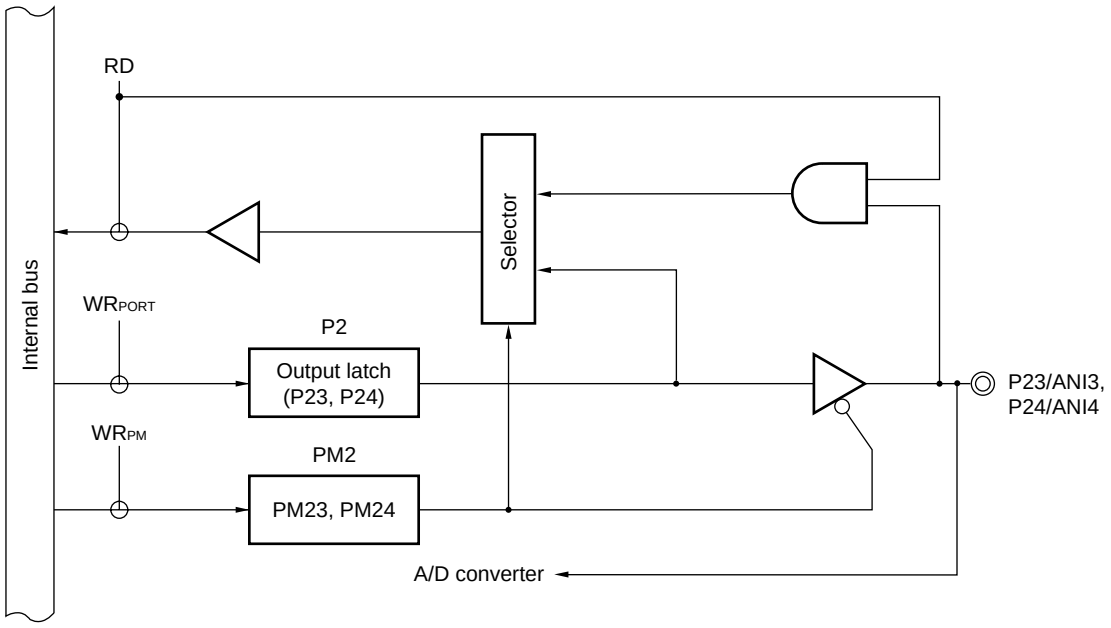
P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Figure 4-3. Block Diagram of P22



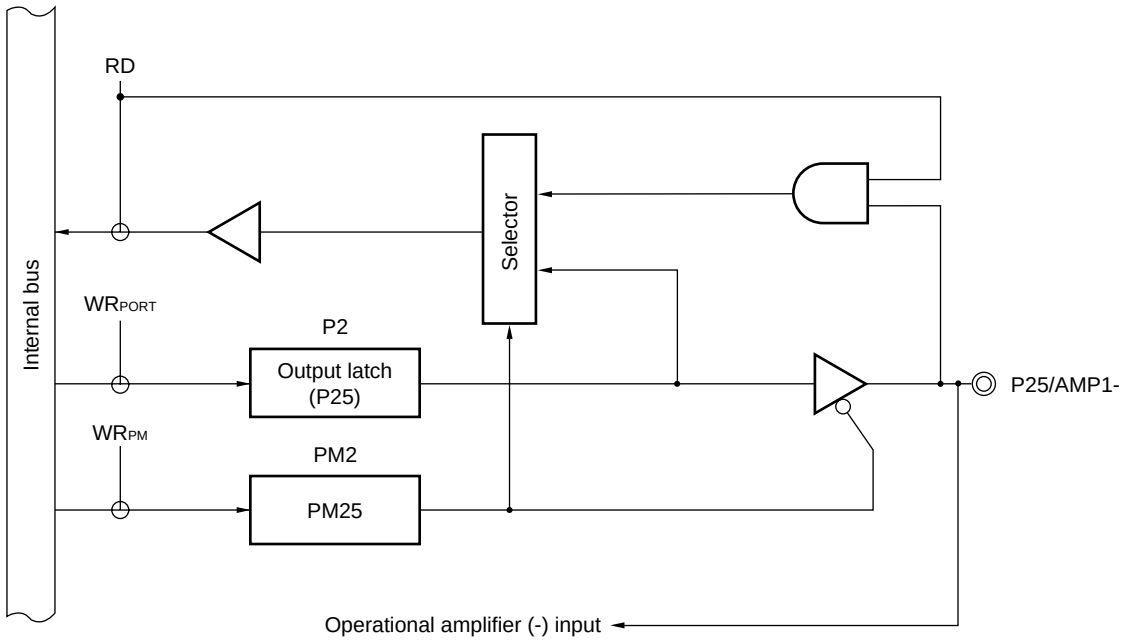
P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Figure 4-4. Block Diagram of P23, P24



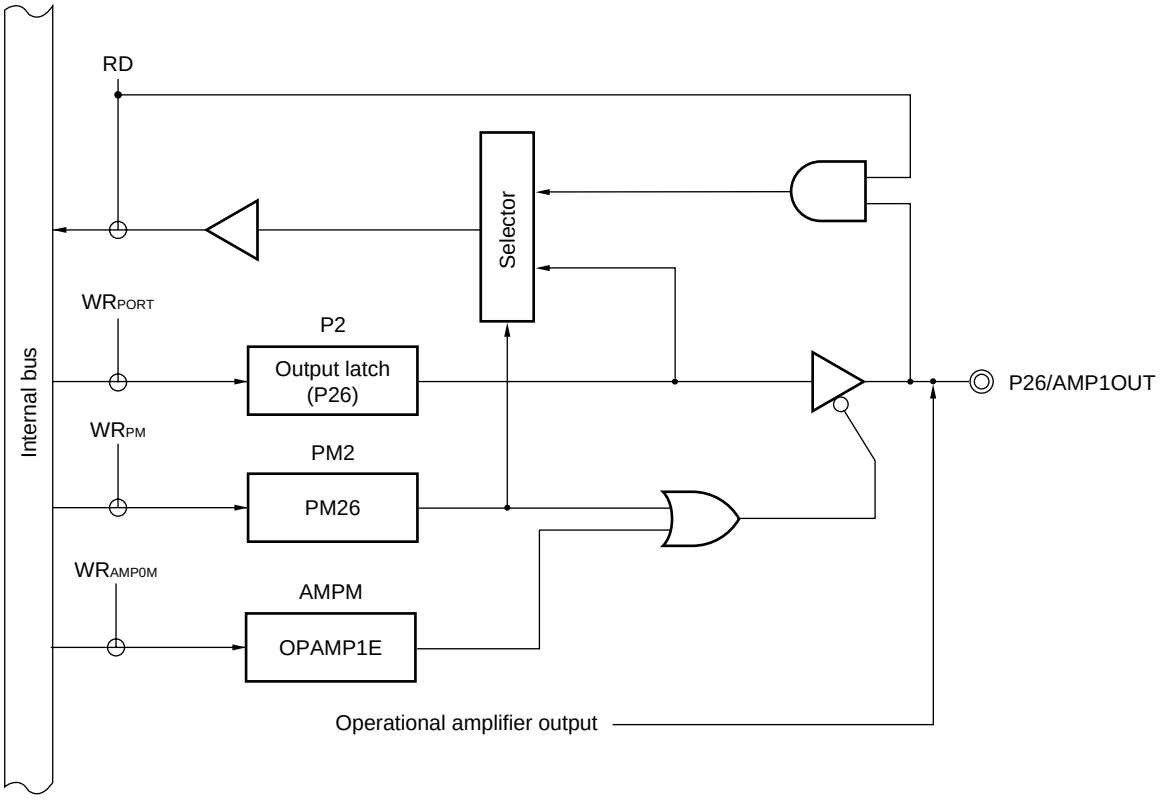
P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Figure 4-5. Block Diagram of P25



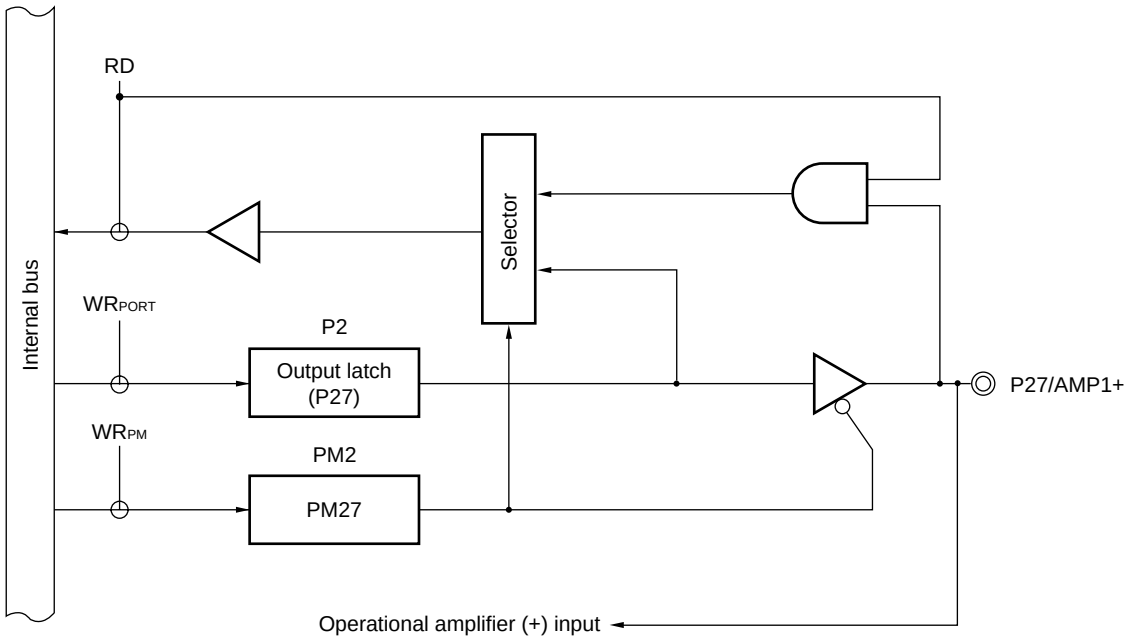
P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Figure 4-6. Block Diagram of P26



P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Figure 4-7. Block Diagram of P27



P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

4.2.2 Port 3

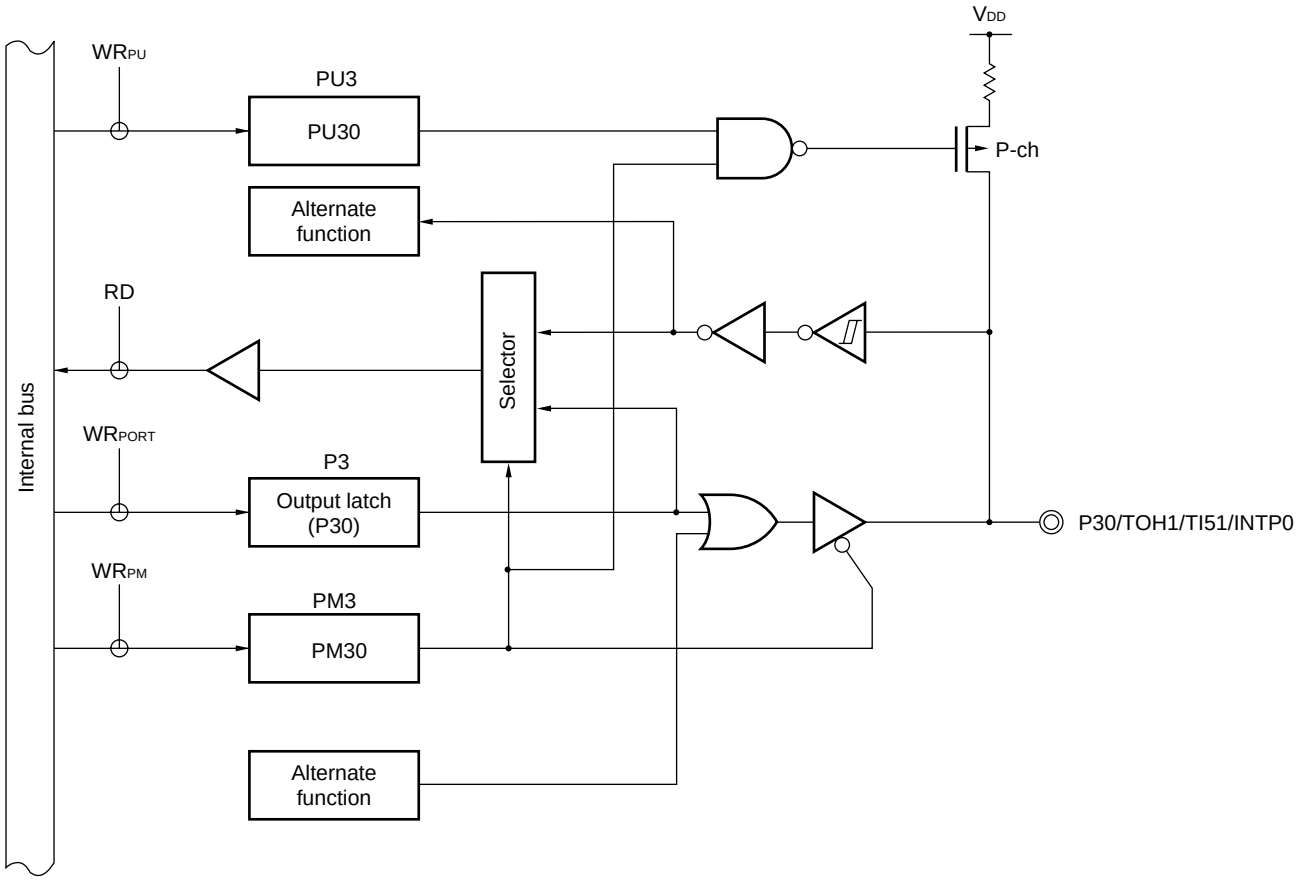
Port 3 is an I/O port with an output latch. Port 3 can be set to the input mode or output mode in 1-bit units using port mode register 3 (PM3). When the P30 to P34 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 3 (PU3).

This port can also be used for external interrupt request input, timer I/O, and clock I/O and data I/O for serial interface, comparator I/O.

Reset signal generation sets port 3 to input mode.

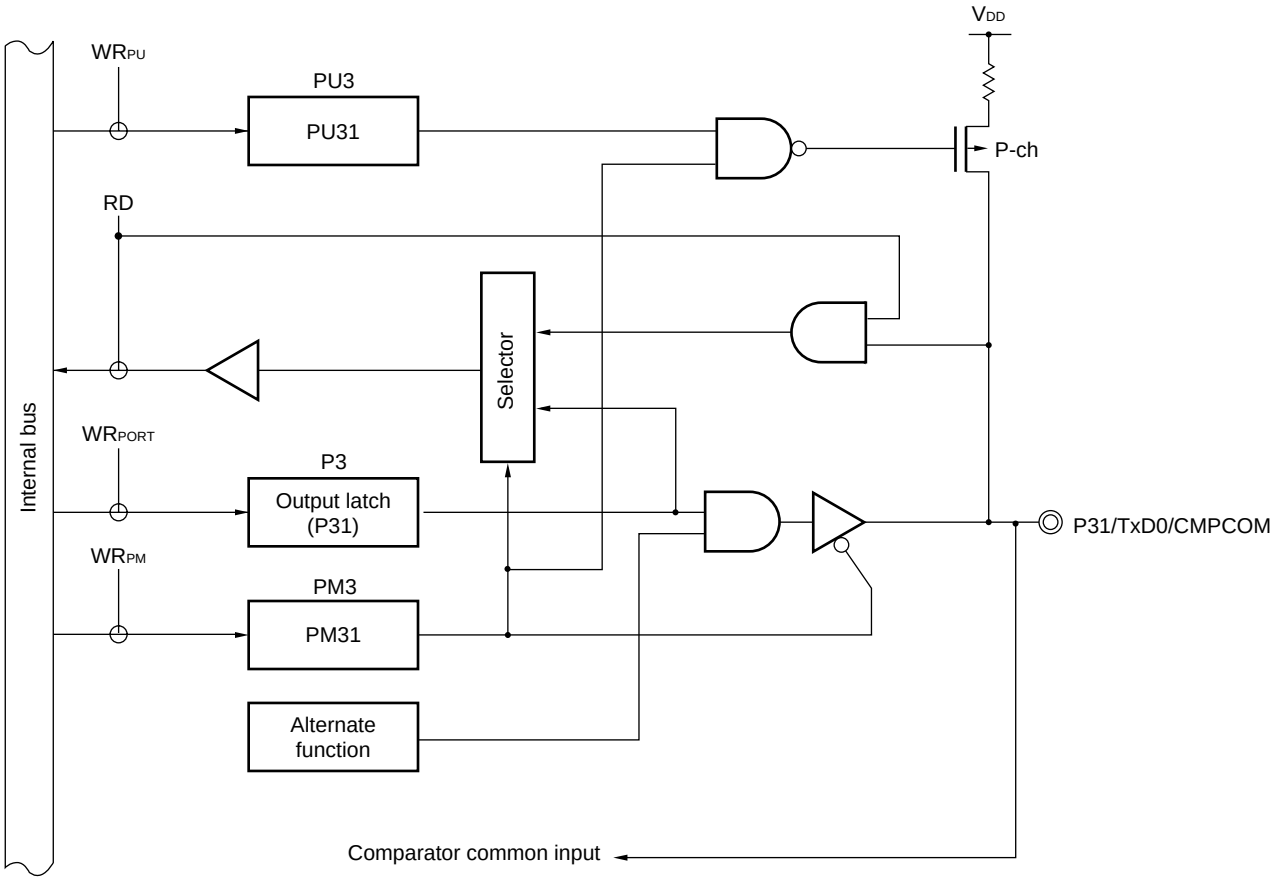
Figures 4-8 to 4-12 show block diagrams of port 3.

Figure 4-8. Block Diagram of P30



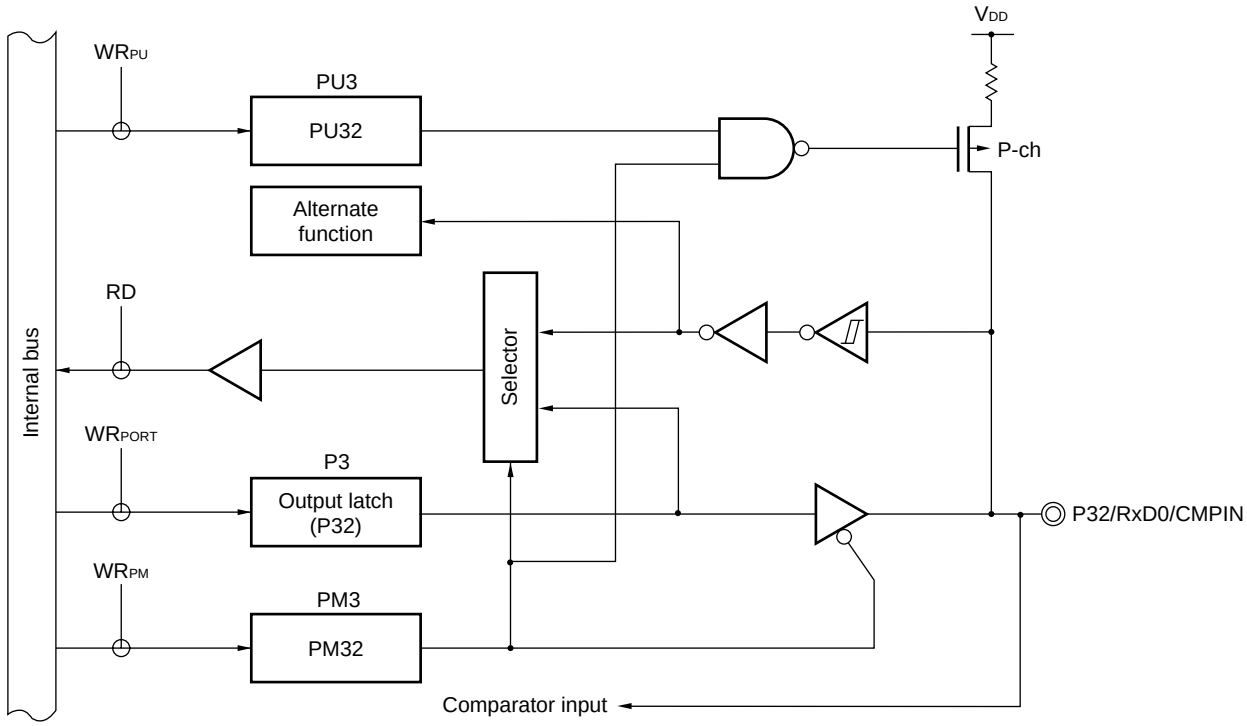
P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Figure 4-9. Block Diagram of P31



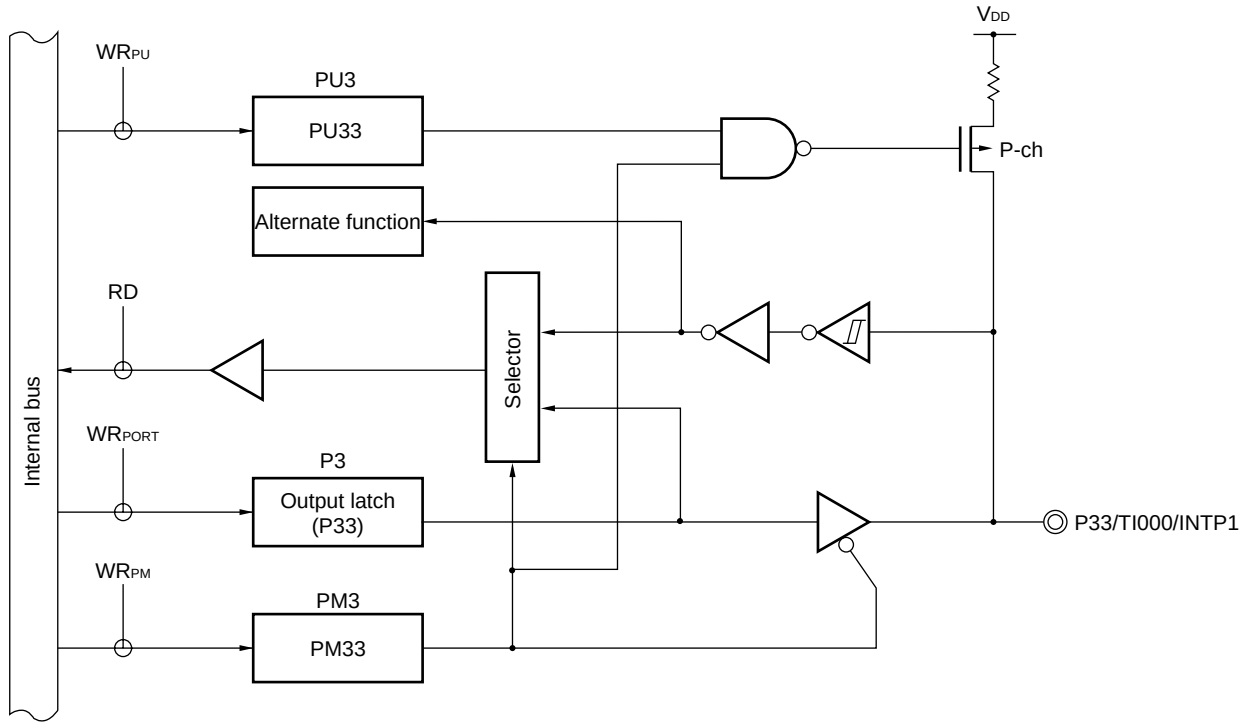
P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Figure 4-10. Block Diagram of P32



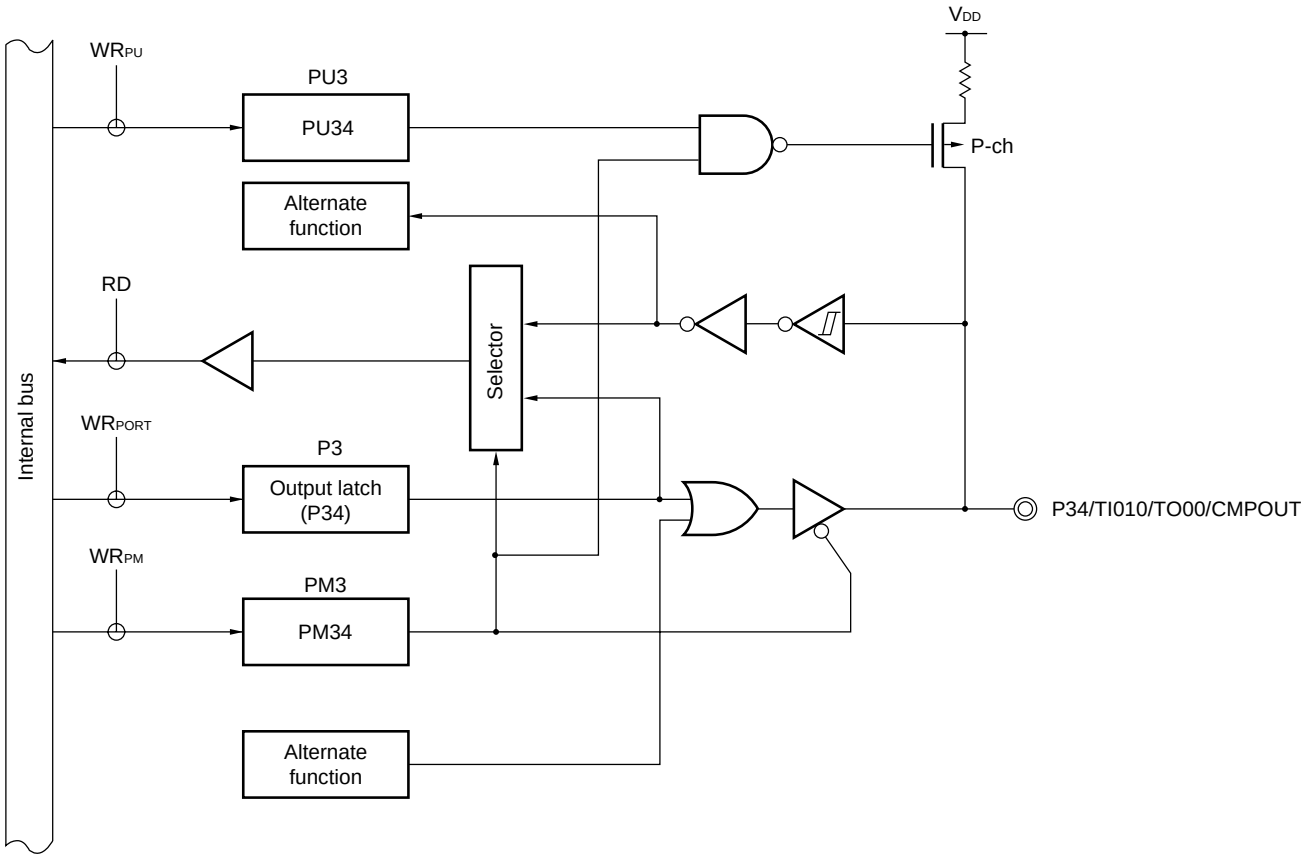
P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Figure 4-11. Block Diagram of P33



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

Figure 4-12. Block Diagram of P34



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

4.2.3 Port 12

P121, P122 function as an I/O port with an output latch. P125 can be set to the input mode or output mode in 1-bit units using port mode register 12 (PM12).

P125 functions as an Input port.

When used as an input port for P121 and P122, use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

This port can also be used as pins for connecting resonator for main system clock, external clock input for main system clock, external reset input, and clock input and data I/O for flash memory programmer/on-chip debugger.

Set bit 5 (RSTM) of the reset pin mode register (RSTMASK) to 1 when using P125/$\overline{\text{RESET}}$ as an input port, and clear RSTM to 0 when using P125/$\overline{\text{RESET}}$ as an external reset input.

Reset signal generation sets port 12 to input mode.

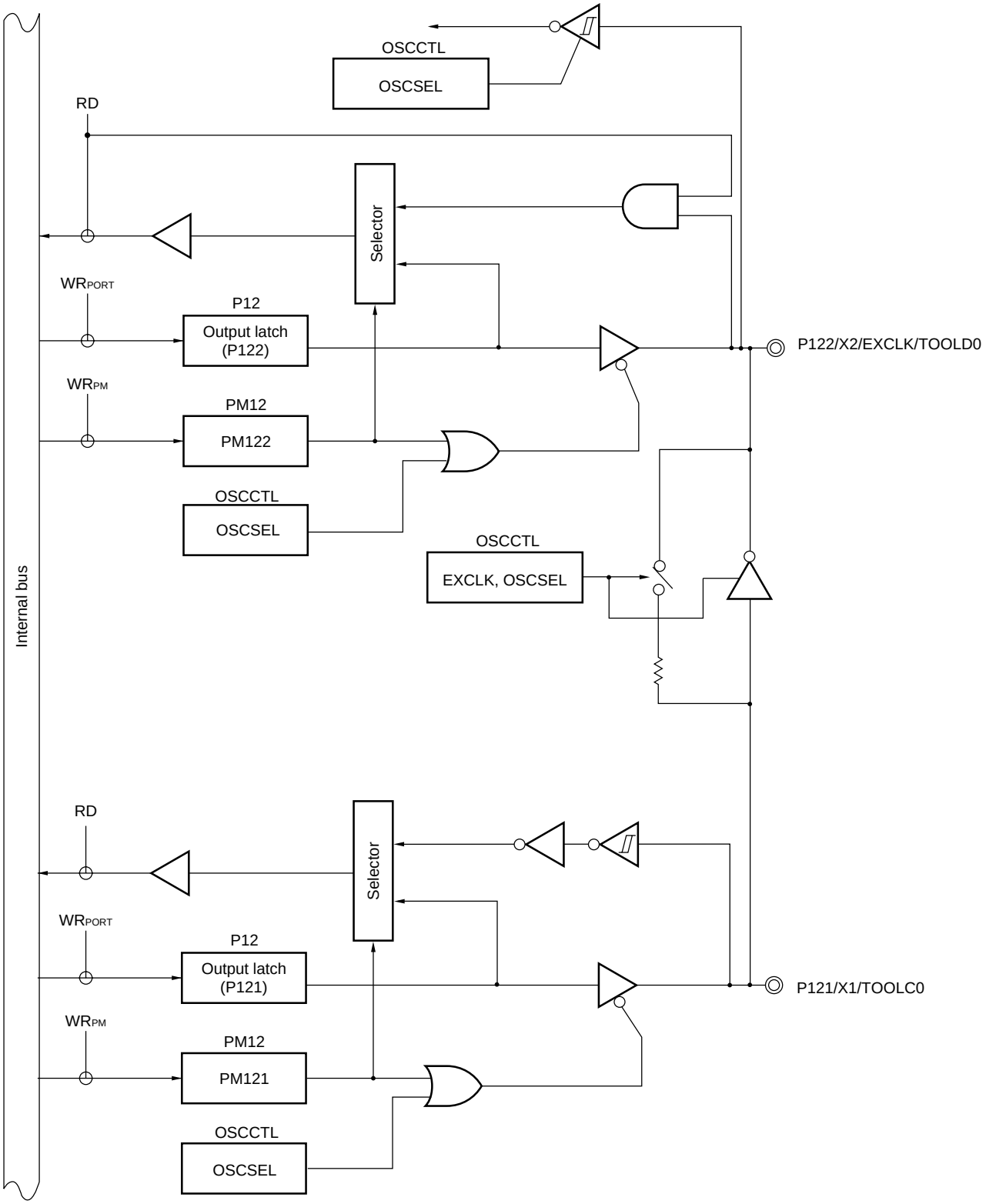
Figures 4-13, 4-14 show block diagrams of port 12.

Cautions 1. When using the P121, P122 pins to connect a resonator for the main system clock (X1, X2) or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, refer to 5.3 (1) Clock operation mode select register (OSCCTL)). The reset value of OSCCTL is 00H (all of the P121, P122 pins are Input port pins).

2. $\overline{\text{RESET}}$/P125 is set in an external reset input after a reset release.

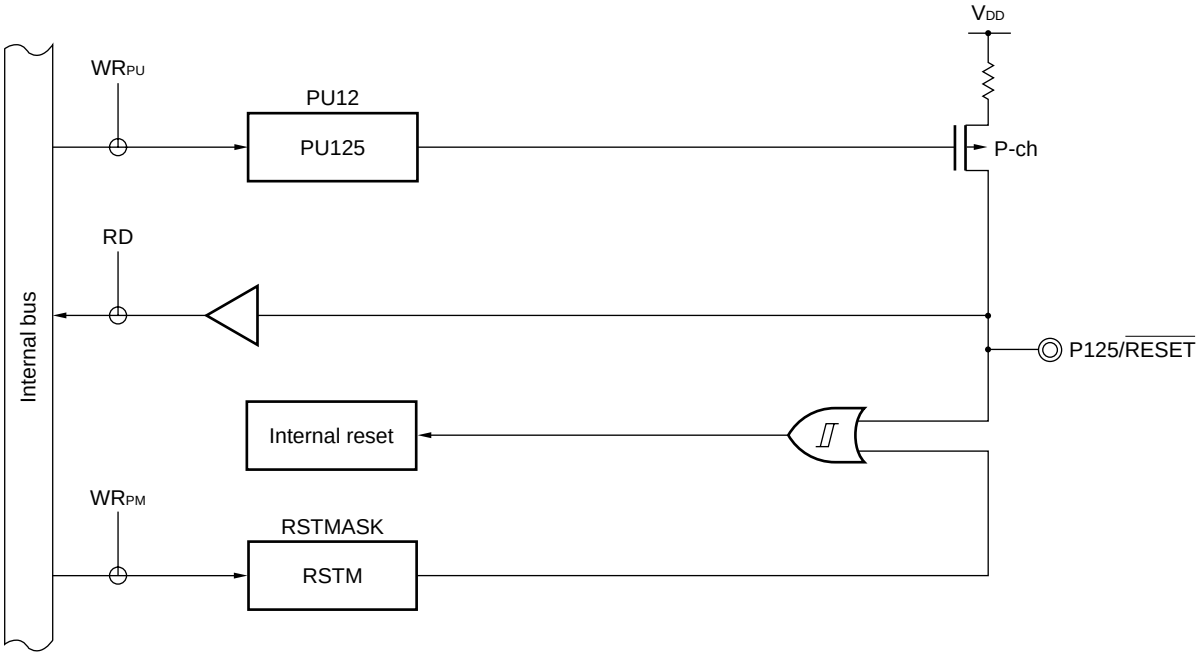
3. Because $\overline{\text{RESET}}$/P125 is set in the external reset input immediately after release of reset, if a reset signal is generated during low level input, the reset status continues until the input rises to the high level.

Figure 4-13. Block Diagram of P121, P122



P12: Port register 12
PU12: Pull-up resistor option register 12
PM12: Port mode register 12
OSCCTL: Clock operation mode select register
RD: Read signal
WR××: Write signal

Figure 4-14. Block Diagram of P125



PU12: Pull-up resistor option register 12
RD: Read signal
WR××: Write signal
RSTMASK: Reset pin mode register

Caution Because $\overline{\text{RESET}}$/P125 is set in the external reset input immediately after release of reset, if a reset signal is generated during low level input, the reset status continues until the input rises to the high level.

Remark After reset, the external reset function and the pull-up resistor are enabled (RSTM = 0, PU125 = 1). Set RSTM bit to 1 when using as a port function.

4.3 Registers Controlling Port Function

Port functions are controlled by the following five types of registers.

- Port mode registers (PMxx)
- Port registers (Pxx)
- Pull-up resistor option registers (PUxx)
- Reset pin mode register (RSTMASK)
- A/D port configuration register (ADPC)

(1) Port mode registers (PMxx)

These registers specify input or output mode for the port in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

When port pins are used as alternate-function pins, set the port mode register by referencing **4.5 Settings of Port Mode Register and Output Latch When Using Alternate Function**.

Figure 4-15. Format of Port Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM2	PM27 Note 1	PM26 Note 1	PM25 Note 1	PM24 Note 1	PM23 Note 1	PM22 Note 1	PM21 Note 1	PM20 Note 1	FF22H	FFH	R/W
PM3	1	1	1	PM34	PM33 Note 2	PM32 Note 2	PM31	PM30	FF23H	FFH	R/W
PM12	1	1	1	1	1	PM122	PM121	1	FF2CH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 2, 3, 12; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Notes 1. If this pin is set as an analog input by using the ADPC register, be sure to set it to input mode.

2. If this pin is set as an analog input by using the CMPPC register, be sure to set it to input mode.

Caution Be sure to set bits 5 to 7 of PM3, bits 0, 3 to 7 of PM12 to 1.

(2) Port registers (Pxx)

These registers write the data that is output from the chip when data is output from a port.

If the data is read in the input mode, the pin level is read. If it is read in the output mode, the output latch value is read.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 4-16. Format of Port Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P2	P27Note 1	P26Note 1	P25Note 1	P24Note 1	P23Note 1	P22Note 1	P21Note 1	P20Note 1	FF02H	00H (output latch)	R/W
P3	0	0	0	P34	P33Note 1	P32Note 1	P31	P30	FF03H	00H (output latch)	R/W
P12	0	0	P125	0	0	P122Note 2	P121Note 2	0	FF0CH	00H (output latch)	R/W

Pmn	m = 2, 3, 12; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Notes 1. If this pin is set as an analog input and to input mode, do not access the output latch.

2. “0” is always read from the output latch of the pin in the X1 oscillation mode or external clock input mode.

(3) Pull-up resistor option registers (PUxx)

These registers specify whether the on-chip pull-up resistors are to be used or not. On-chip pull-up resistors can be used in 1-bit units only for the bits set to input mode of the pins to which the use of an on-chip pull-up resistor has been specified in these registers. On-chip pull-up resistors cannot be connected to bits set to output mode and bits used as alternate-function output pins, regardless of the settings of these registers.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H (sets only PU12 to 20H).

Figure 4-17. Format of Pull-up Resistor Option Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU3	0	0	0	PU34	PU33	PU32	PU31	PU30	FF33H	00H	R/W
PU12	0	0	PU125	0	0	0	0	0	FF3CH	20H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 3, 12; n = 0 to 5)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

(4) Reset pin mode register (RSTMASK)

This register sets the pin function of $\overline{\text{RESET}}$/P125 (external reset input/input-dedicated port).

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 4-18. Format of Reset Pin Mode Register (RSTMASK)

Address: FF2DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
RSTMASK	0	0	RSTM	0	0	0	0	0

RSTM	$\overline{\text{RESET}}$/P125 pin function selection
0	Using as external reset input ($\overline{\text{RESET}}$)
1	Using as input-dedicated port (P125)

(5) A/D port configuration register (ADPC)

ADPC switches the P20/AMP0-/ANI0 to P27/AMP1+ pins to digital I/O or analog I/O of port. Each bit of ADPC corresponds to a pin of port 2 and can be specified in 1-bit units.

The register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears ADPC to 00H.

Figure 4-19. Format of A/D Port Configuration Register (ADPC)

Address: FF97H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	ADPC7	ADPC6	ADPC5	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0

ADPCn	Digital I/O or analog I/O selection (n = 0 to 7)
0	Analog I/O
1	Digital I/O

Cautions 1. Set the pin set to analog input to the input mode by using port mode register 2 (PM2).

2. If data is written to ADPC, a wait cycle is generated. Do not write data to ADPC when the peripheral hardware clock is stopped. For details, refer to CHAPTER 26 CAUTIONS FOR WAIT.

4.4 Port Function Operations

Port operations differ depending on whether the input or output mode is set, as shown below.

4.4.1 Writing to I/O port

(1) Output mode

A value is written to the output latch by a transfer instruction, and the output latch contents are output from the pin.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

A value is written to the output latch by a transfer instruction, but since the output buffer is off, the pin status does not change.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

4.4.2 Reading from I/O port

(1) Output mode

The output latch contents are read by a transfer instruction. The output latch contents do not change.

(2) Input mode

The pin status is read by a transfer instruction. The output latch contents do not change.

4.4.3 Operations on I/O port

(1) Output mode

An operation is performed on the output latch contents, and the result is written to the output latch. The output latch contents are output from the pins.
Once data is written to the output latch, it is retained until data is written to the output latch again.
The data of the output latch is cleared when a reset signal is generated.

(2) Input mode

The pin level is read and an operation is performed on its contents. The result of the operation is written to the output latch, but since the output buffer is off, the pin status does not change.
The data of the output latch is cleared when a reset signal is generated.

4.5 Settings of Port Mode Register and Output Latch When Using Alternate Function

To use the alternate function of a port pin, set the port mode register and output latch as shown in **Table 4-9**.

Table 4-9. Settings of Port Mode Register and Output Latch When Using Alternate Function (1/2)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P20	ANI0[Note]	Input	1	×
	AMP0-[Note]	Input	1	×
P21	ANI1[Note]	Input	1	×
	AMP0OUT[Note]	Output	1	×
P22	ANI2[Note]	Input	1	×
	AMP0+[Note]	Input	1	×
P23, P24	ANI3, ANI4[Note]	Input	1	×
P25	AMP1-	Input	1	×
P26	AMP1OUT	Output	1	×
P27	AMP1+	Input	1	×
P30	INTP0	Input	1	×
	TI51	Input	1	×
	TOH1	Output	0	0
P31	TxD0	Output	0	1
	CMPCOM	Input	1	×
P32	RxD0	Input	1	×
	CMPIN	Input	1	×
P33	INTP1	Input	1	×
	TI000	Input	1	×
P34	TO00	Input	1	×
	TI010	Output	0	0
	CMPOUT	Output	0	0

Note The pin function can be selected by using ADPC register, PM2 register, ADS register, and AMPH register. Refer to **Tables 4-4** to **4-8** of **4.2.1 Port 2**.

Remark ×: Don't care
PM××: Port mode register
P××: Port output latch

Table 4-9. Settings of Port Mode Register and Output Latch When Using Alternate Function (2/2)

Pin Name	Alternate Function		PM××	P××
	Function Name	I/O		
P121	X1[Note 1]	–	×	×
	TOOLC0	Input	×	×
P122	X2[Note 1]	–	×	×
	EXCLK[Note 1]	Input	×	×
	TOOLD0	I/O	×	×
P125	$\overline{\text{RESET}}$[Note 2]	Input	×	×

Notes 1. When using the P121 and P122 pins to connect a resonator for the main system clock (X1, X2) or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode or external clock input mode must be set by using OSCCTL register (for details, refer to **5.3 (1) Clock operation mode select register (OSCCTL)**). The reset value of OSCCTL is 00H (both P121 and P122 are input port pins).

2. Clear RSTM bit (bit 5 of RSTMASK register) to 0 when using P125 as an external reset input ($\overline{\text{RESET}}$).

Remark ×: Don't care
PM××: Port mode register
P××: Port output latch

4.6 Cautions on 1-Bit Manipulation Instruction for Port Register n (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the output latch value of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P20 is an output port, P21 to P27 are input ports (all pin statuses are high level), and the port latch value of port 1 is 00H, if the output of output port P20 is changed from low level to high level via a 1-bit manipulation instruction, the output latch value of port 2 is FFH.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A 1-bit manipulation instruction is executed in the following order in the µPD79F7023, 79F7024 microcontrollers.

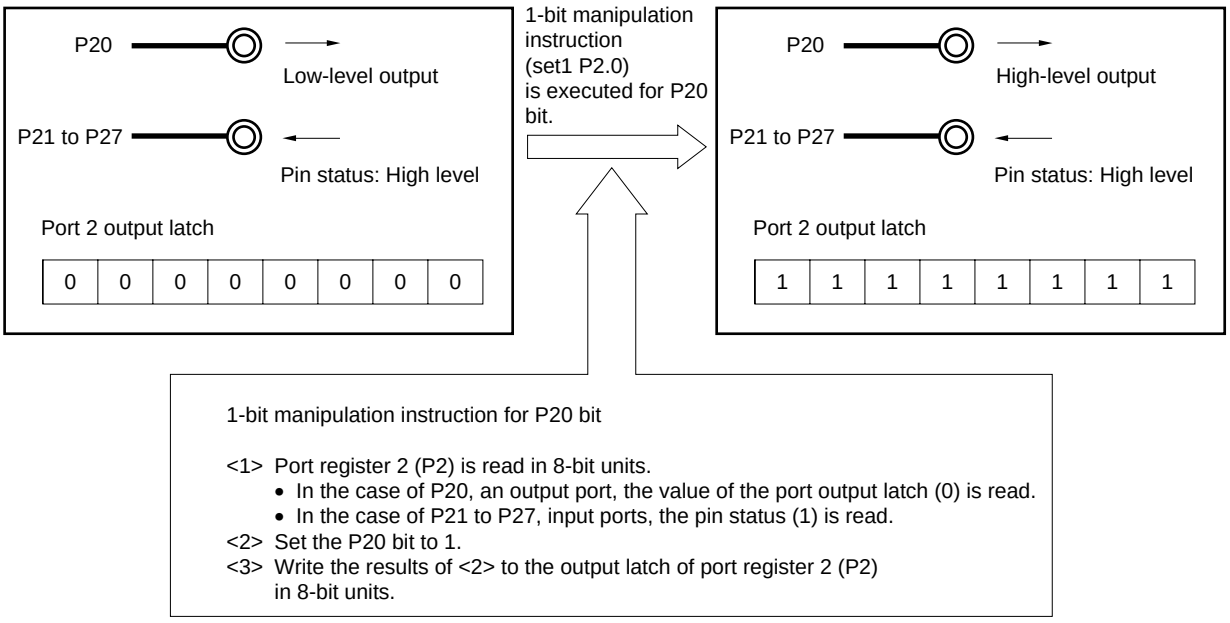
<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the output latch value (0) of P20, which is an output port, is read, while the pin statuses of P21 to P27, which are input ports, are read. If the pin statuses of P21 to P27 are high level at this time, the read value is FEH.

The value is changed to FFH by the manipulation in <2>.

FFH is written to the output latch by the manipulation in <3>.

Figure 4-20 1-Bit Manipulation Instruction (P20)



Remark The following instructions are 1-bit manipulation instructions.

- MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1

CHAPTER 5 CLOCK GENERATOR

5.1 Functions of Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware.
The following three kinds of system clocks and clock oscillators are selectable.

(1) Main system clock

<1> X1 oscillator

This circuit oscillates a clock of f_X = 1 to 10 MHz by connecting a resonator to X1 and X2.
Oscillation can be stopped by executing the STOP instruction or using the main OSC control register (MOC).

<2> Internal high-speed oscillator

This circuit oscillates a clock of f_{IH} = 4 MHz (TYP.). After a reset release, the CPU always starts operating with this internal high-speed oscillation clock. Oscillation can be stopped by executing the STOP instruction or using the internal oscillation mode register (RCM).

An external main system clock (f_{EXCLK} = 1 to 10 MHz) can also be supplied from the EXCLK/X2/P122 pin. An external main system clock input can be disabled by executing the STOP instruction or using RCM.
As the main system clock, a high-speed system clock (X1 clock or external main system clock) or internal high-speed oscillation clock can be selected by using the main clock mode register (MCM).

Remark f_X: X1 clock oscillation frequency
f_{IH}: Internal high-speed oscillation clock frequency
f_{EXCLK}: External main system clock frequency

(2) Internal low-speed oscillation clock (clock for watchdog timer)

- **Internal low-speed oscillator**

This circuit oscillates a clock of f_{IL} = 240 kHz (TYP.). After a reset release, the internal low-speed oscillation clock always starts operating.
Oscillation can be stopped by using the internal oscillation mode register (RCM) when “internal low-speed oscillator can be stopped by software” is set by option byte.
The internal low-speed oscillation clock cannot be used as the CPU clock. The following hardware operates with the internal low-speed oscillation clock.

- Watchdog timer
- 8-bit timer H1 (when f_{IL}, $f_{IL}/2^7$, or $f_{IL}/2^9$ is selected)

Remark f_{IL}: Internal low-speed oscillation clock frequency

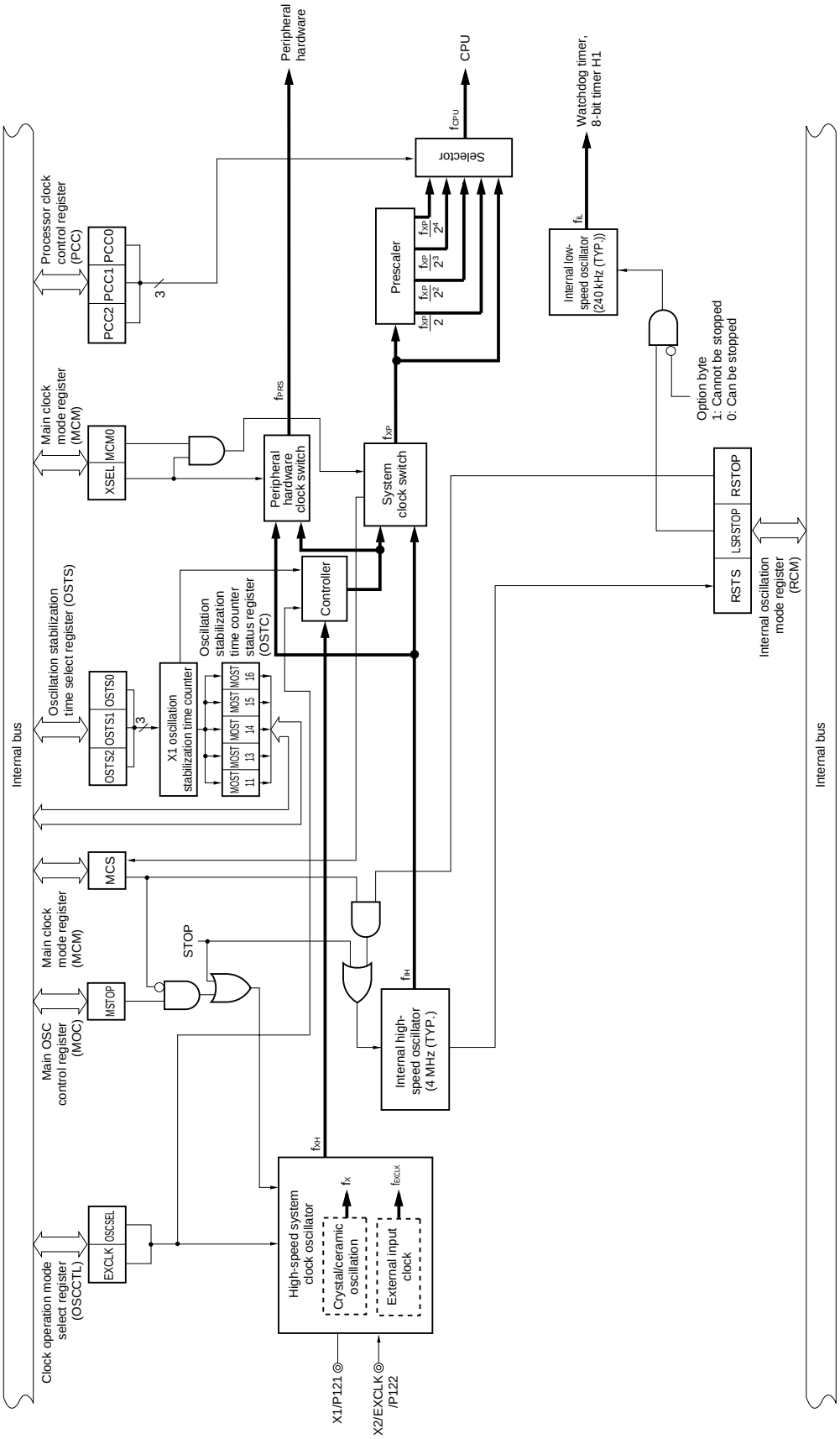
5.2 Configuration of Clock Generator

The clock generator includes the following hardware.

Table 5-1. Configuration of Clock Generator

Item	Configuration
Control registers	Clock operation mode select register (OSCCTL) Processor clock control register (PCC) Internal oscillation mode register (RCM) Main OSC control register (MOC) Main clock mode register (MCM) Oscillation stabilization time counter status register (OSTC) Oscillation stabilization time select register (OSTS)
Oscillators	X1 oscillator Internal high-speed oscillator Internal low-speed oscillator

Figure 5-1. Block Diagram of Clock Generator



Remark f_X: X1 clock oscillation frequency
f_{IH}: Internal high-speed oscillation clock frequency
f_{EXCLK}: External main system clock frequency
f_{XH}: High-speed system clock frequency
f_{XP}: Main system clock frequency
f_{PRS}: Peripheral hardware clock frequency
f_{CPU}: CPU clock frequency
f_{IL}: Internal low-speed oscillation clock frequency

5.3 Registers Controlling Clock Generator

The following seven registers are used to control the clock generator.

- Clock operation mode select register (OSCCTL)
- Processor clock control register (PCC)
- Internal oscillation mode register (RCM)
- Main OSC control register (MOC)
- Main clock mode register (MCM)
- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)

(1) Clock operation mode select register (OSCCTL)

This register selects the operation modes of the high-speed system clock.

OSCCTL can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 5-2. Format of Clock Operation Mode Select Register (OSCCTL)

Address: FF9FH After reset: 00H R/W

Symbol	<7>	<6>	5	4	3	2	1	0
OSCCTL	EXCLK	OSCSEL	0	0	0	0	0	0

EXCLK	OSCSEL	High-speed system clock pin operation mode	P121/X1 pin	P122/X2/EXCLK pin
0	0	Input port mode	Input port	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Cautions 1. To change the value of EXCLK and OSCSEL, be sure to confirm that bit 7 (MSTOP) of the main OSC control register (MOC) is 1 (the X1 oscillator stops or the external clock from the EXCLK pin is disabled).

2. Be sure to clear bits 0 to 5 to 0.

(2) Processor clock control register (PCC)

This register is used to select the CPU clock and the division ratio.

PCC is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PCC to 01H.

Figure 5-3. Format of Processor Clock Control Register (PCC)

Address: FFFBH After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
PCC	0	0	0	0	0	PCC2	PCC1	PCC0

PCC2	PCC1	PCC0	CPU clock (f_{CPU}) selection
0	0	0	f_{XP}
0	0	1	f_{XP}/2 (default)
0	1	0	$f_{XP}/2^2$
0	1	1	$f_{XP}/2^3$
1	0	0	$f_{XP}/2^4$
Other than above			Setting prohibited

Cautions 1. Be sure to clear bits 3 to 7 to 0.

2. The peripheral hardware clock (f_{PRS}) is not divided when the division ratio of the PCC is set.

Remark f_{XP}: Main system clock oscillation frequency

The fastest instruction can be executed in 2 clocks of the CPU clock in the µPD79F7023, 79F7024 microcontrollers. Therefore, the relationship between the CPU clock (f_{CPU}) and the minimum instruction execution time is as shown in Table 5-2.

Table 5-2. Relationship between CPU Clock and Minimum Instruction Execution Time

CPU Clock (f_{CPU})	Minimum Instruction Execution Time: $2/f_{CPU}$	
	Main System Clock	
	High-Speed System Clock[Note]	Internal High-Speed Oscillation Clock[Note]
	At 10 MHz Operation	At 4 MHz (TYP.) Operation
f_{XP}	0.2 µs	0.5 µs (TYP.)
$f_{XP}/2$	0.4 µs	1.0 µs (TYP.)
$f_{XP}/2^2$	0.8 µs	2.0 µs (TYP.)
$f_{XP}/2^3$	1.6 µs	4.0 µs (TYP.)
$f_{XP}/2^4$	3.2 µs	8.0 µs (TYP.)

Note The main clock mode register (MCM) is used to set the main system clock supplied to CPU clock (high-speed system clock/internal high-speed oscillation clock) (refer to **Figure 5-3**).

(3) Internal oscillation mode register (RCM)

This register sets the operation mode of internal oscillator.

RCM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 80H[Note 1].

Figure 5-4. Format of Internal Oscillation Mode Register (RCM)

Address: FFA0H After reset: 80H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	2	<1>	<0>
RCM	RSTS	0	0	0	0	0	LSRSTOP	RSTOP

RSTS	Status of internal high-speed oscillator
0	Waiting for accuracy stabilization of internal high-speed oscillator
1	Stability operating of internal high-speed oscillator

LSRSTOP	Internal low-speed oscillator oscillating/stopped
0	Internal low-speed oscillator oscillating
1	Internal low-speed oscillator stopped

RSTOP	Internal high-speed oscillator oscillating/stopped
0	Internal high-speed oscillator oscillating
1	Internal high-speed oscillator stopped

Notes 1. The value of this register is 00H immediately after a reset release but automatically changes to 80H after internal high-speed oscillator has been stabilized.

2. Bit 7 is read-only.

Caution When setting RSTOP to 1, be sure to confirm that the CPU operates with a clock other than the internal high-speed oscillation clock. Specifically, set under the following condition.

- **When MCS = 1 (when CPU operates with the high-speed system clock)**

In addition, stop peripheral hardware that is operating on the internal high-speed oscillation clock before setting RSTOP to 1.

(4) Main OSC control register (MOC)

This register selects the operation mode of the high-speed system clock.

This register is used to stop the X1 oscillator or to disable an external clock input from the EXCLK pin when the CPU operates with a clock other than the high-speed system clock.

MOC can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 80H.

Figure 5-5. Format of Main OSC Control Register (MOC)

Address: FFA2H After reset: 80H R/W

Symbol	<7>	6	5	4	3	2	1	0
MOC	MSTOP	0	0	0	0	0	0	0

MSTOP	Control of high-speed system clock operation	
	X1 oscillation mode	External clock input mode
0	X1 oscillator operating	External clock from EXCLK pin is enabled
1	X1 oscillator stopped	External clock from EXCLK pin is disabled

Cautions 1. Clear MSTOP to 0 while the regulator mode control register (RMC) is 00H.

2. When setting MSTOP to 1, be sure to confirm that the CPU operates with a clock other than the high-speed system clock. Specifically, set under the following condition.

- **When MCS = 0 (when CPU operates with the internal high-speed oscillation clock)**

In addition, stop peripheral hardware that is operating on the high-speed system clock before setting MSTOP to 1.

3. Do not clear MSTOP to 0 while bit 6 (OSCSEL) of the clock operation mode select register (OSCCTL) is 0 (input port mode).

4. The peripheral hardware cannot operate when the peripheral hardware clock is stopped. To resume the operation of the peripheral hardware after the peripheral hardware clock has been stopped, initialize the peripheral hardware.

(5) Main clock mode register (MCM)

This register selects the main system clock supplied to CPU clock and clock supplied to peripheral hardware clock.

MCM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 5-6. Format of Main Clock Mode Register (MCM)

Address: FFA1H After reset: 00H R/W[Note]

Symbol	7	6	5	4	3	<2>	<1>	<0>
MCM	0	0	0	0	0	XSEL	MCS	MCM0

XSEL	MCM0	Selection of clock supplied to main system clock and peripheral hardware	
		Main system clock (f_{XP})	Peripheral hardware clock (f_{PRS})
0	0	Internal high-speed oscillation clock (f_{IH})	Internal high-speed oscillation clock (f_{IH})
0	1		
1	0		High-speed system clock (f_{XH})
1	1	High-speed system clock (f_{XH})	

MCS	Main system clock status
0	Operates with internal high-speed oscillation clock
1	Operates with high-speed system clock

Note Bit 1 is read-only.

Cautions 1. XSEL can be changed only once after a reset release.

2. A clock other than f_{PRS} is supplied to the following peripheral functions regardless of the setting of XSEL and MCM0.

- **Watchdog timer (operates with internal low-speed oscillation clock)**
- **When "f_{IL}", "$f_{IL}/2^7$", or "$f_{IL}/2^9$" is selected as the count clock for 8-bit timer H1 (operates with internal low-speed oscillation clock)**
- **Peripheral hardware selects the external clock as the clock source (Except when the external count clock of TM00 is selected (TI000 pin valid edge))**

(6) Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter. When X1 clock oscillation starts with the internal high-speed oscillation clock used as the CPU clock, the X1 clock oscillation stabilization time can be checked.

OSTC can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset is released (reset by $\overline{\text{RESET}}$ input, POC, LVI, and WDT), the STOP instruction and MSTOP (bit 7 of MOC register) = 1 clear OSTC to 00H.

Figure 5-7. Format of Oscillation Stabilization Time Counter Status Register (OSTC)

Address: FFA3H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	0	0	0	MOST11	MOST13	MOST14	MOST15	MOST16

MOST11	MOST13	MOST14	MOST15	MOST16	Oscillation stabilization time status	
						f_X = 10 MHz
1	0	0	0	0	$2^{11}/f_X$ min.	204.8 µs min.
1	1	0	0	0	$2^{13}/f_X$ min.	819.2 µs min.
1	1	1	0	0	$2^{14}/f_X$ min.	1.64 ms min.
1	1	1	1	0	$2^{15}/f_X$ min.	3.27 ms min.
1	1	1	1	1	$2^{16}/f_X$ min.	6.55 ms min.

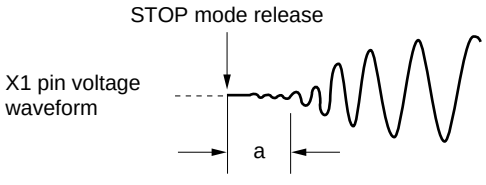
Cautions 1. After the above time has elapsed, the bits are set to 1 in order from MOST11 and remain 1.

2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts (“a” below).



Remark f_X: X1 clock oscillation frequency

(7) Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation waits for the time set using OSTS after the STOP mode is released.

When the internal high-speed oscillation clock is selected as the CPU clock, confirm with OSTC that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using OSTC.

OSTS can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets OSTS to 05H.

Figure 5-8. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection	
				f_X = 10 MHz
0	0	1	$2^{11}/f_X$	204.8 µs
0	1	0	$2^{13}/f_X$	819.2 µs
0	1	1	$2^{14}/f_X$	1.64 ms
1	0	0	$2^{15}/f_X$	3.27 ms
1	0	1	$2^{16}/f_X$	6.55 ms
Other than above			Setting prohibited	

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

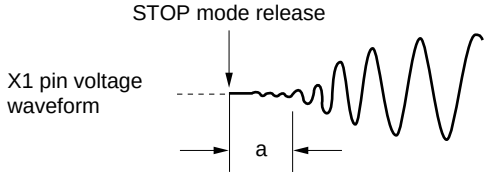
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts (“a” below).



Remark f_X: X1 clock oscillation frequency

5.4 System Clock Oscillator

5.4.1 X1 oscillator

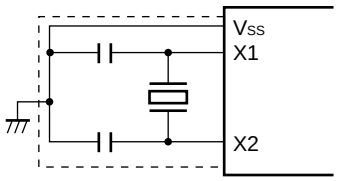
The X1 oscillator oscillates with a crystal resonator or ceramic resonator (1 to 10 MHz) connected to the X1 and X2 pins.

An external clock can also be input. In this case, input the clock signal to the EXCLK pin.

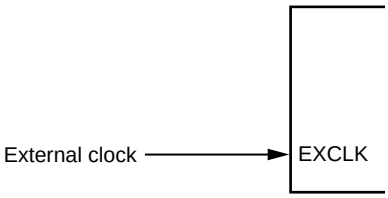
Figure 5-9 shows an example of the external circuit of the X1 oscillator.

Figure 5-9. Example of External Circuit of X1 Oscillator

(a) Crystal or ceramic oscillation



(b) External clock



Cautions are listed on the next page.

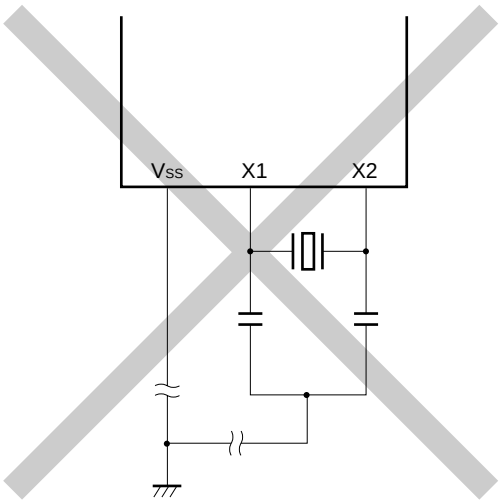
Caution When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the Figure 5-10 to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as VSS. Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

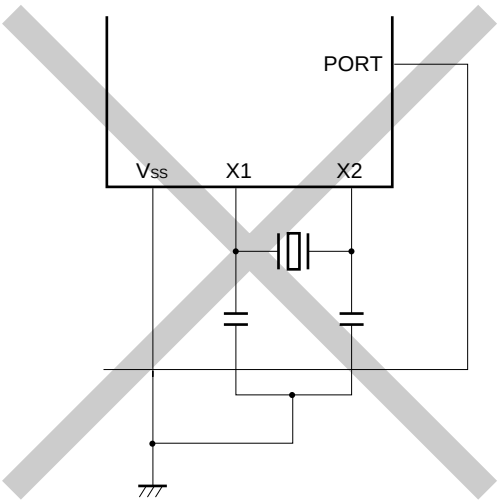
Figure 5-10 shows examples of incorrect resonator connection.

Figure 5-10. Examples of Incorrect Resonator Connection (1/2)

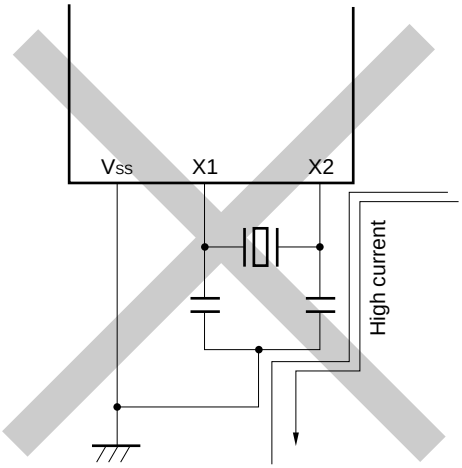
(a) Too long wiring



(b) Crossed signal line



(c) Wiring near high alternating current



(d) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)

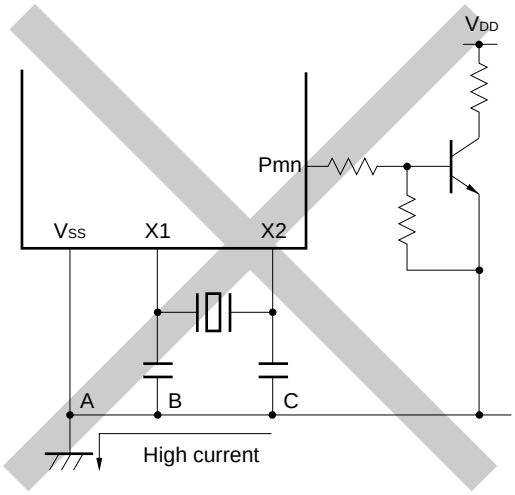
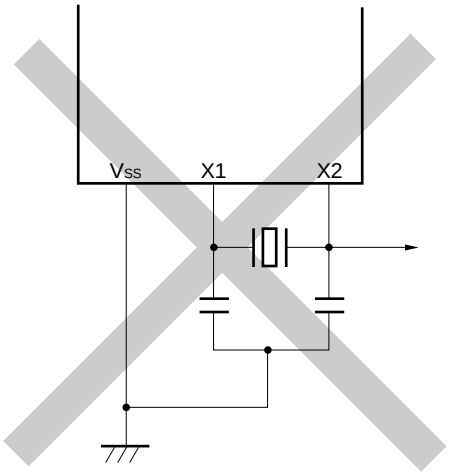


Figure 5-10. Examples of Incorrect Resonator Connection (2/2)

(e) Signals are fetched



5.4.2 Internal high-speed oscillator

The internal high-speed oscillator is incorporated in the µPD79F7023, 79F7024. Oscillation can be controlled by the internal oscillation mode register (RCM).

After a reset release, the internal high-speed oscillator automatically starts oscillation.

5.4.3 Internal low-speed oscillator

The internal low-speed oscillator is incorporated in the µPD79F7023, 79F7024.

The internal low-speed oscillation clock is only used as the watchdog timer and the clock of 8-bit timer H1. The internal low-speed oscillation clock cannot be used as the CPU clock.

“Can be stopped by software” or “Cannot be stopped” can be selected by the option byte. When “Can be stopped by software” is set, oscillation can be controlled by the internal oscillation mode register (RCM).

After a reset release, the internal low-speed oscillator automatically starts oscillation, and the watchdog timer is driven (240 kHz (TYP.)) if the watchdog timer operation is enabled using the option byte.

5.4.4 Prescaler

The prescaler generates the CPU clock by dividing the main system clock when the main system clock is selected as the clock to be supplied to the CPU.

5.5 Clock Generator Operation

The clock generator generates the following clocks and controls the operation modes of the CPU, such as standby mode (refer to **Figure 5-1**).

- Main system clock f_{XP}
  - High-speed system clock f_{XH}
    X1 clock f_X
    External main system clock f_{EXCLK}
  - Internal high-speed oscillation clock f_{IH}
- Internal low-speed oscillation clock f_{IL}
- CPU clock f_{CPU}
- Peripheral hardware clock f_{PRS}

The CPU starts operation when the internal high-speed oscillator starts outputting after a reset release in the μPD79F7023, 79F7024 microcontrollers, thus enabling the following.

(1) Enhancement of security function

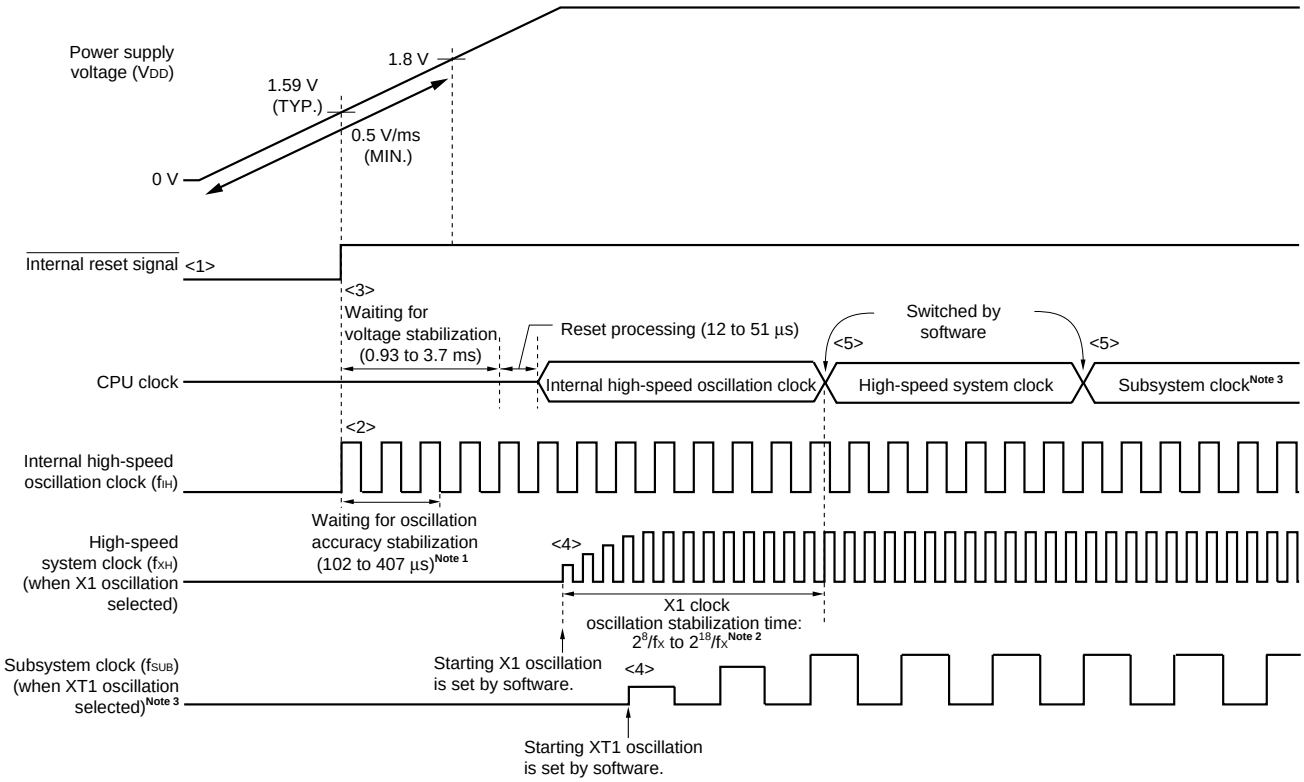
When the X1 clock is set as the CPU clock by the default setting, the device cannot operate if the X1 clock is damaged or badly connected and therefore does not operate after reset is released. However, the start clock of the CPU is the internal high-speed oscillation clock, so the device can be started by the internal high-speed oscillation clock after a reset release. Consequently, the system can be safely shut down by performing a minimum operation, such as acknowledging a reset source by software or performing safety processing when there is a malfunction.

(2) Improvement of performance

Because the CPU can be started without waiting for the X1 clock oscillation stabilization time, the total performance can be improved.

When the power supply voltage is turned on, the clock generator operation is shown in Figures 5-11 and 5-12.

Figure 5-11. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Stopped Is Set (Option Byte: LVISTART = 0))



<1> When the power is turned on, an internal reset signal is generated by the power-on-clear (POC) circuit.

<2> When the power supply voltage exceeds 1.59 V (TYP.), the reset is released and the internal high-speed oscillator automatically starts oscillation.

<3> When the power supply voltage rises with a slope of 0.5 V/ms (MIN.), the CPU starts operation on the internal high-speed oscillation clock after the reset is released and after the stabilization times for the voltage of the power supply and regulator have elapsed, and then reset processing is performed.

<4> Set the start of oscillation of the X1 clock via software (refer to **(1)** in **5.6.1 Example of controlling high-speed system clock**).

<5> When switching the CPU clock to the X1 clock, wait for the clock oscillation to stabilize, and then set switching via software (refer to **(3)** in **5.6.1 Example of controlling high-speed system clock**).

Notes 1. The internal voltage stabilization time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

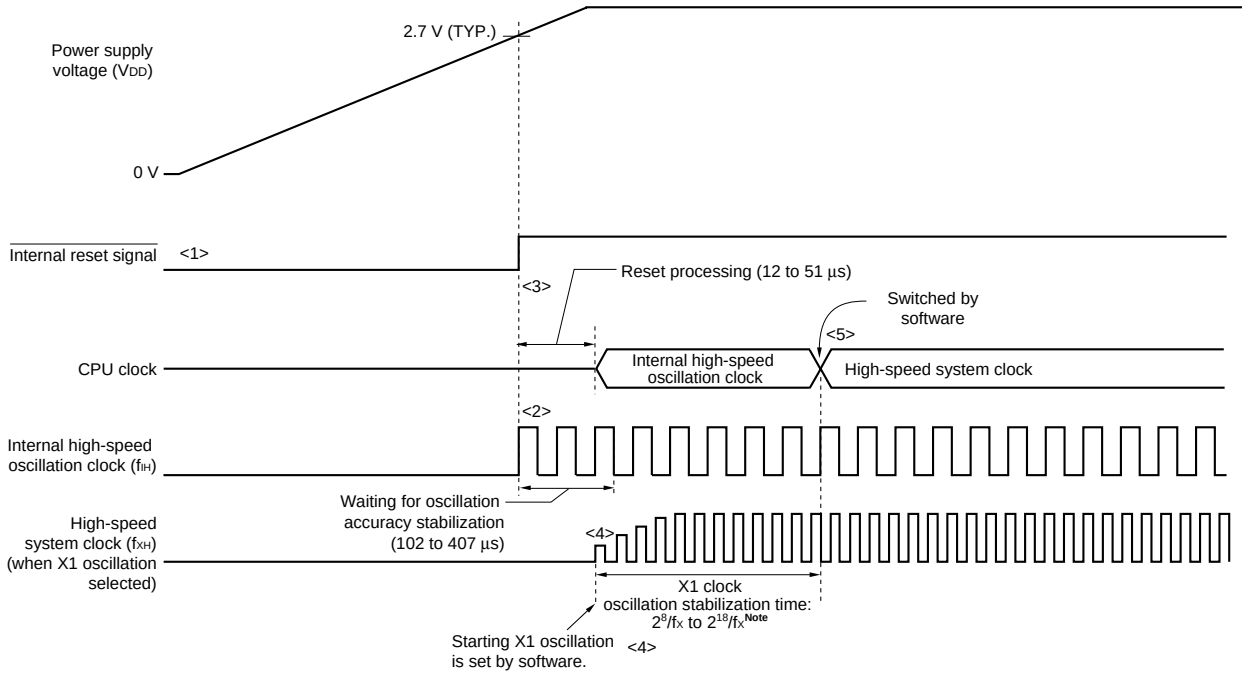
2. When releasing a reset (above figure) or releasing STOP mode while the CPU is operating on the internal high-speed oscillation clock, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC). If the CPU operates on the high-speed system clock (X1 oscillation), set the oscillation stabilization time when releasing STOP mode using the oscillation stabilization time select register (OSTS).

Cautions 1. If the voltage rises with a slope of less than 0.5 V/ms (MIN.) from power application until the voltage reaches 2.7 V, input a low level to the $\overline{\text{RESET}}$ pin from power application until the voltage reaches 2.7 V, or set the LVI default start function enabled by using the option byte (LVISTART = 1) (refer to Figure 5-12). When a low level has been input to the $\overline{\text{RESET}}$ pin until the voltage reaches 2.7 V, the CPU operates with the same timing as <2> and thereafter in Figure 5-11, after the reset has been released by the $\overline{\text{RESET}}$ pin.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

Remark While the microcontroller is operating, a clock that is not used as the CPU clock can be stopped via software settings. The internal high-speed oscillation clock and high-speed system clock can be stopped by executing the STOP instruction (refer to **(4)** in **5.6.1 Example of controlling high-speed system clock**, **(3)** in **5.6.2 Example of controlling internal high-speed oscillation clock**).

Figure 5-12. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Enabled Is Set (Option Byte: LVISTART = 1))



<1> When the power is turned on, an internal reset signal is generated by the power-on-clear (POC) circuit.

<2> When the power supply voltage exceeds 2.7 V (TYP.), the reset is released and the internal high-speed oscillator automatically starts oscillation.

<3> After the reset is released and reset processing is performed, the CPU starts operation on the internal high-speed oscillation clock.

<4> Set the start of oscillation of the X1 clock via software (refer to **(1)** in **5.6.1 Example of controlling high-speed system clock**).

<5> When switching the CPU clock to the X1 clock, wait for the clock oscillation to stabilize, and then set switching via software (refer to **(3)** in **5.6.1 Example of controlling high-speed system clock**).

Note When releasing a reset (above figure) or releasing STOP mode while the CPU is operating on the internal high-speed oscillation clock, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC). If the CPU operates on the high-speed system clock (X1 oscillation), set the oscillation stabilization time when releasing STOP mode using the oscillation stabilization time select register (OSTS).

Cautions 1. A voltage oscillation stabilization time (0.93 to 3.7 ms) is required after the supply voltage reaches 1.59 V (TYP.). If the supply voltage rises from 1.59 V (TYP.) to 2.7 V (TYP.) within the power supply oscillation stabilization time, the power supply oscillation stabilization time is automatically generated before reset processing.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

Remark While the microcontroller is operating, a clock that is not used as the CPU clock can be stopped via software settings. The internal high-speed oscillation clock and high-speed system clock can be stopped by executing the STOP instruction (refer to **(4)** in **5.6.1 Example of controlling high-speed system clock**, **(3)** in **5.6.2 Example of controlling internal high-speed oscillation clock**).

5.6 Controlling Clock

5.6.1 Example of controlling high-speed system clock

The following two types of high-speed system clocks are available.

- X1 clock: Crystal/ceramic resonator is connected across the X1 and X2 pins.
- External main system clock: External clock is input to the EXCLK pin.

When the high-speed system clock is not used, the X1/P121 and X2/EXCLK/P122 pins can be used as input port pins.

Caution The X1/P121 and X2/EXCLK/P122 pins are in the input port mode after a reset release.

The following describes examples of setting procedures for the following cases.

(1) When oscillating X1 clock
(2) When using external main system clock
(3) When using high-speed system clock as CPU clock and peripheral hardware clock
(4) When stopping high-speed system clock

(1) Example of setting procedure when oscillating the X1 clock

<1> Setting P121/X1 and P122/X2/EXCLK pins and selecting X1 clock or external clock (OSCCTL register)
When EXCLK is cleared to 0 and OSCSEL is set to 1, the mode is switched from port mode to X1 oscillation mode.

EXCLK	OSCSEL	Operation Mode of High-Speed System Clock Pin	P121/X1 Pin	P122/X2/EXCLK Pin
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	

<2> Controlling oscillation of X1 clock (MOC register)
If MSTOP is cleared to 0, the X1 oscillator starts oscillating.

<3> Waiting for the stabilization of the oscillation of X1 clock
Check the OSTC register and wait for the necessary time.
During the wait time, other software processing can be executed with the internal high-speed oscillation clock.

Cautions 1. Do not change the value of EXCLK and OSCSEL while the X1 clock is operating.
2. Set the X1 clock after the supply voltage has reached the operable voltage of the clock to be used (refer to CHAPTER 24 ELECTRICAL SPECIFICATIONS).

(2) Example of setting procedure when using the external main system clock

<1> Setting P121/X1 and P122/X2/EXCLK pins and selecting operation mode (OSCCTL register)
When EXCLK and OSCSEL are set to 1, the mode is switched from port mode to external clock input mode.

EXCLK	OSCSEL	Operation Mode of High-Speed System Clock Pin	P121/X1 Pin	P122/X2/EXCLK Pin
1	1	External clock input mode	Input port	External clock input

<2> Controlling external main system clock input (MOC register)
When MSTOP is cleared to 0, the input of the external main system clock is enabled.

Cautions 1. Do not change the value of EXCLK and OSCSEL while the external main system clock is operating.
2. Set the external main system clock after the supply voltage has reached the operable voltage of the clock to be used (refer to CHAPTER 24 ELECTRICAL SPECIFICATIONS).

(3) Example of setting procedure when using high-speed system clock as CPU clock and peripheral hardware clock

<1> Setting high-speed system clock oscillation[Note]
(Refer to **5.6.1 (1) Example of setting procedure when oscillating the X1 clock** and **(2) Example of setting procedure when using the external main system clock.**)

Note The setting of <1> is not necessary when high-speed system clock is already operating.

<2> Setting the high-speed system clock as the main system clock (MCM register)

When XSEL and MCM0 are set to 1, the high-speed system clock is supplied as the main system clock and peripheral hardware clock.

XSEL	MCM0	Selection of Main System Clock and Clock Supplied to Peripheral Hardware	
		Main System Clock (f_{XP})	Peripheral Hardware Clock (f_{PRS})
1	1	High-speed system clock (f_{XH})	High-speed system clock (f_{XH})

Caution If the high-speed system clock is selected as the main system clock, a clock other than the high-speed system clock cannot be set as the peripheral hardware clock.

<3> Setting the main system clock as the CPU clock and selecting the division ratio (PCC register)

The main system clock is supplied to the CPU. To select the CPU clock division ratio, use PCC0, PCC1, and PCC2.

PCC2	PCC1	PCC0	CPU Clock (f_{CPU}) Selection
0	0	0	f_{XP}
0	0	1	f_{XP}/2 (default)
0	1	0	$f_{XP}/2^2$
0	1	1	$f_{XP}/2^3$
1	0	0	$f_{XP}/2^4$
Other than above			Setting prohibited

(4) Example of setting procedure when stopping the high-speed system clock

The high-speed system clock can be stopped in the following two ways.

- Executing the STOP instruction and stopping the X1 oscillation (disabling clock input if the external clock is used)
- Setting MSTOP to 1 and stopping the X1 oscillation (disabling clock input if the external clock is used)

(a) To execute a STOP instruction

<1> Setting to stop peripheral hardware

Stop peripheral hardware that cannot be used in the STOP mode (for peripheral hardware that cannot be used in STOP mode, refer to **CHAPTER 15 STANDBY FUNCTION**).

<2> Setting the X1 clock oscillation stabilization time after standby release

When the CPU is operating on the X1 clock, set the value of the OSTS register before the STOP instruction is executed.

<3> Executing the STOP instruction

When the STOP instruction is executed, the system is placed in the STOP mode and X1 oscillation is stopped (the input of the external clock is disabled).

(b) To stop X1 oscillation (disabling external clock input) by setting MSTOP to 1

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the high-speed system clock. When CLS = 0 and MCS = 1, the high-speed system clock is supplied to the CPU, so change the CPU clock to a clock other than the high-speed system clock.

MCS	CPU Clock Status
0	Internal high-speed oscillation clock
1	High-speed system clock

<2> Stopping the high-speed system clock (MOC register)

When MSTOP is set to 1, X1 oscillation is stopped (the input of the external clock is disabled).

Caution Be sure to confirm that MCS = 0 or CLS = 1 when setting MSTOP to 1. In addition, stop peripheral hardware that is operating on the high-speed system clock.

5.6.2 Example of controlling internal high-speed oscillation clock

The following describes examples of clock setting procedures for the following cases.

(1) When restarting oscillation of the internal high-speed oscillation clock
(2) When using internal high-speed oscillation clock as CPU clock, and internal high-speed oscillation clock or high-speed system clock as peripheral hardware clock
(3) When stopping the internal high-speed oscillation clock

(1) Example of setting procedure when restarting oscillation of the internal high-speed oscillation clock[Note 1]

<1> Setting restart of oscillation of the internal high-speed oscillation clock (RCM register)

When RSTOP is cleared to 0, the internal high-speed oscillation clock starts operating.

<2> Waiting for the oscillation accuracy stabilization time of internal high-speed oscillation clock (RCM register)

Wait until RSTS is set to 1[Note 2].

Notes 1. After a reset release, the internal high-speed oscillator automatically starts oscillating and the internal high-speed oscillation clock is selected as the CPU clock.

2. This wait time is not necessary if high accuracy is not necessary for the CPU clock and peripheral hardware clock.

(2) Example of setting procedure when using internal high-speed oscillation clock as CPU clock, and internal high-speed oscillation clock or high-speed system clock as peripheral hardware clock

<1> • Restarting oscillation of the internal high-speed oscillation clock[Note]
(Refer to **5.6.2 (1) Example of setting procedure when restarting oscillation of the internal high-speed oscillation clock**).

• Oscillating the high-speed system clock[Note]
(This setting is required when using the high-speed system clock as the peripheral hardware clock. Refer to **5.6.1 (1) Example of setting procedure when oscillating the X1 clock** and **(2) Example of setting procedure when using the external main system clock.**)

Note The setting of <1> is not necessary when the internal high-speed oscillation clock or high-speed system clock is already operating.

<2> Selecting the clock supplied as the main system clock and peripheral hardware clock (MCM register)
Set the main system clock and peripheral hardware clock using XSEL and MCM0.

XSEL	MCM0	Selection of Main System Clock and Clock Supplied to Peripheral Hardware	
		Main System Clock (f_{XP})	Peripheral Hardware Clock (f_{PRS})
0	0	Internal high-speed oscillation clock (f_{IH})	Internal high-speed oscillation clock (f_{IH})
0	1		
1	0		High-speed system clock (f_{XH})

<3> Selecting the CPU clock division ratio (PCC register)
The main system clock is supplied to the CPU. To select the CPU clock division ratio, use PCC0, PCC1, and PCC2.

PCC2	PCC1	PCC0	CPU Clock (f_{CPU}) Selection
0	0	0	f_{XP}
0	0	1	f_{XP}/2 (default)
0	1	0	$f_{XP}/2^2$
0	1	1	$f_{XP}/2^3$
1	0	0	$f_{XP}/2^4$
Other than above			Setting prohibited

(3) Example of setting procedure when stopping the internal high-speed oscillation clock

The internal high-speed oscillation clock can be stopped in the following two ways.

- Executing the STOP instruction to set the STOP mode
- Setting RSTOP to 1 and stopping the internal high-speed oscillation clock

(a) To execute a STOP instruction

<1> Setting of peripheral hardware

Stop peripheral hardware that cannot be used in the STOP mode (for peripheral hardware that cannot be used in STOP mode, refer to **CHAPTER 15 STANDBY FUNCTION**).

<2> Setting the X1 clock oscillation stabilization time after standby release

When the CPU is operating on the X1 clock, set the value of the OSTS register before the STOP instruction is executed. To operate the CPU immediately after the STOP mode has been released, set MCM0 to 0, switch the CPU clock to the internal high-speed oscillation clock, and check that RSTS is 1.

<3> Executing the STOP instruction

When the STOP instruction is executed, the system is placed in the STOP mode and internal high-speed oscillation clock is stopped.

(b) To stop internal high-speed oscillation clock by setting RSTOP to 1

<1> Confirming the CPU clock status (PCC and MCM registers)

Confirm with CLS and MCS that the CPU is operating on a clock other than the internal high-speed oscillation clock.

When CLS = 0 and MCS = 0, the internal high-speed oscillation clock is supplied to the CPU, so change the CPU clock to a clock other than the internal high-speed oscillation clock.

MCS	CPU Clock Status
0	Internal high-speed oscillation clock
1	High-speed system clock

<2> Stopping the internal high-speed oscillation clock (RCM register)

When RSTOP is set to 1, internal high-speed oscillation clock is stopped.

Caution Be sure to confirm that MCS = 1 or CLS = 1 when setting RSTOP to 1. In addition, stop peripheral hardware that is operating on the internal high-speed oscillation clock.

5.6.3 Example of controlling internal low-speed oscillation clock

The internal low-speed oscillation clock cannot be used as the CPU clock.

Only the following peripheral hardware can operate with this clock.

- Watchdog timer
- 8-bit timer H1 (if f_{IL} is selected as the count clock)

In addition, the following operation modes can be selected by the option byte.

- Internal low-speed oscillator cannot be stopped
- Internal low-speed oscillator can be stopped by software

The internal low-speed oscillator automatically starts oscillation after a reset release, and the watchdog timer is driven (240 kHz (TYP.)) if the watchdog timer operation has been enabled by the option byte.

(1) Example of setting procedure when stopping the internal low-speed oscillation clock

<1> Setting LSRSTOP to 1 (RCM register)

When LSRSTOP is set to 1, the internal low-speed oscillation clock is stopped.

(2) Example of setting procedure when restarting oscillation of the internal low-speed oscillation clock

<1> Clearing LSRSTOP to 0 (RCM register)

When LSRSTOP is cleared to 0, the internal low-speed oscillation clock is restarted.

Caution If "Internal low-speed oscillator cannot be stopped" is selected by the option byte, oscillation of the internal low-speed oscillation clock cannot be controlled.

5.6.4 Clocks supplied to CPU and peripheral hardware

The following table shows the relation among the clocks supplied to the CPU and peripheral hardware, and setting of registers.

Table 5-4. Clocks Supplied to CPU and Peripheral Hardware, and Register Setting

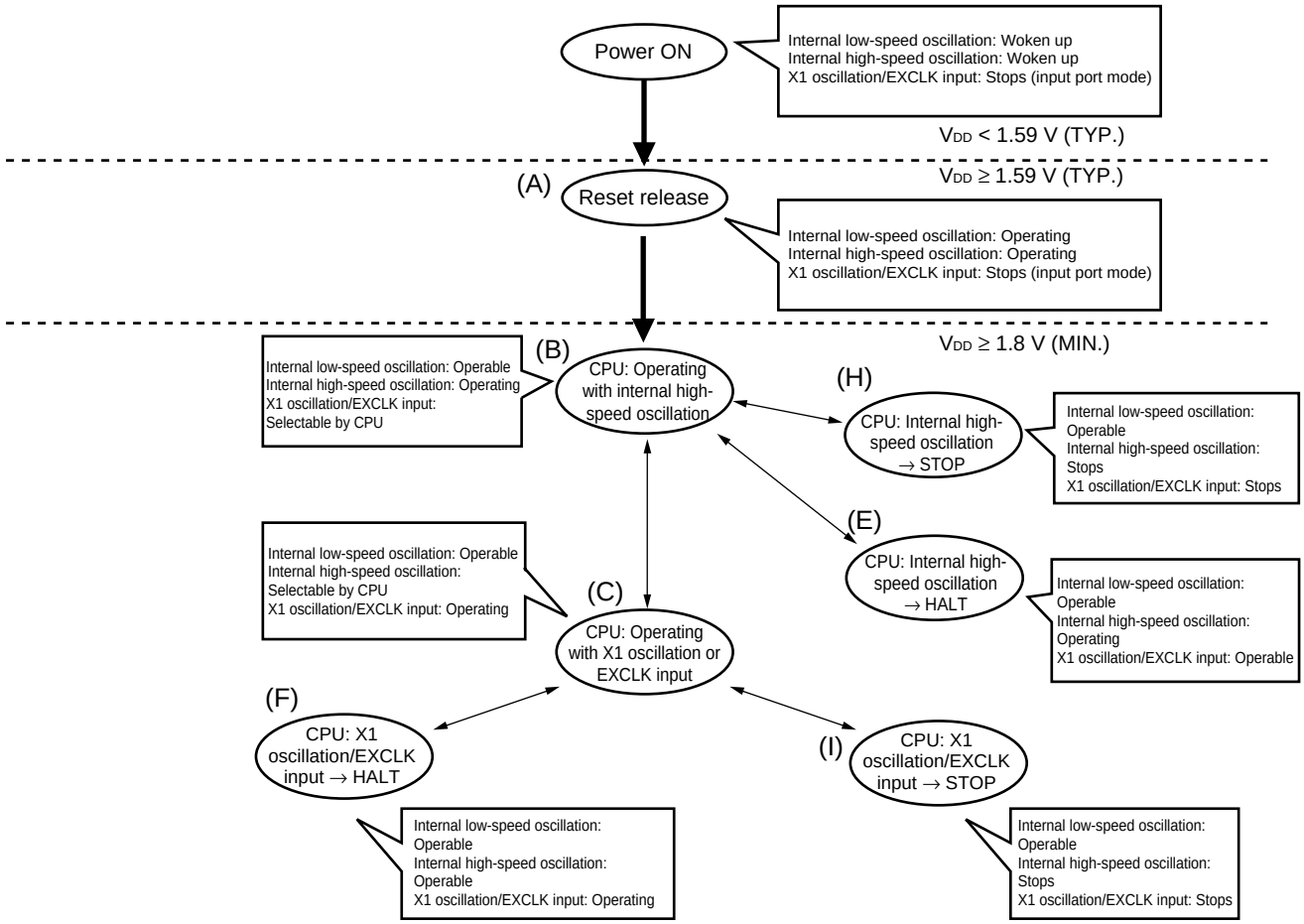
Supplied Clock		XSEL	MCM0	EXCLK
Clock Supplied to CPU	Clock Supplied to Peripheral Hardware			
Internal high-speed oscillation clock		0	×	×
Internal high-speed oscillation clock	X1 clock	1	0	0
	External main system clock	1	0	1
X1 clock		1	1	0
External main system clock		1	1	1

Remark XSEL: Bit 2 of the main clock mode register (MCM)
MCM0: Bit 0 of MCM
EXCLK: Bit 7 of the clock operation mode select register (OSCCTL)
×: don't care

5.6.5 CPU clock status transition diagram

Figure 5-13 shows the CPU clock status transition diagram of this product.

Figure 5-13. CPU Clock Status Transition Diagram (When LVI Default Start Mode Function Stopped Is Set (Option Byte: LVISTART = 0))



Remark When LVI default start function enabled is set (option byte: LVISTART = 1), the CPU clock status changes to (A) in the above figure when the supply voltage exceeds 2.7 V (TYP.), and to (B) after reset processing (12 to 51 μs).

Table 5-5 shows transition of the CPU clock and examples of setting the SFR registers.

Table 5-5. CPU Clock Transition and SFR Register Setting Examples (1/2)

(1) CPU operating with internal high-speed oscillation clock (B) after reset release (A)

Status Transition	SFR Register Setting
(A) → (B)	SFR registers do not have to be set (default status after reset release).

(2) CPU operating with high-speed system clock (C) after reset release (A)

(The CPU operates with the internal high-speed oscillation clock (B) immediately after a reset release.)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLK	OSCSEL	MSTOP	OSTC Register	XSEL	MCM0
(A) → (B) → (C) (X1 clock)	0	1	0	Must be checked	1	1
(A) → (B) → (C) (external main system clock)	1	1	0	Must not be checked	1	1

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (refer to CHAPTER 24 ELECTRICAL SPECIFICATIONS).

(3) CPU clock changing from internal high-speed oscillation clock (B) to high-speed system clock (C)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	EXCLK	OSCSEL	MSTOP	OSTC Register	XSEL[Note]	MCM0
(B) → (C) (X1 clock)	0	1	0	Must be checked	1	1
(B) → (C) (external main system clock)	1	1	0	Must not be checked	1	1

Unnecessary if these registers are already set

Unnecessary if the CPU is operating with the high-speed system clock

Note The value of this flag can be changed only once after a reset release. This setting is not necessary if it has already been set.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (refer to CHAPTER 24 ELECTRICAL SPECIFICATIONS).

Remarks 1. (A) to (I) in Table 5-5 correspond to (A) to (I) in Figure 5-13.

2. EXCLK, OSCSEL: Bits 7 and 6 of the clock operation mode select register (OSCCTL)
MSTOP: Bit 7 of the main OSC control register (MOC)
XSEL, MCM0: Bits 2 and 0 of the main clock mode register (MCM)

Table 5-6. CPU Clock Transition and SFR Register Setting Examples (2/2)

(4) CPU clock changing from high-speed system clock (C) to internal high-speed oscillation clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	RSTOP	RSTS	MCM0
(C) → (B)	0	Confirm this flag is 1.	0

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

(5) • HALT mode (E) set while CPU is operating with internal high-speed oscillation clock (B)
• HALT mode (F) set while CPU is operating with high-speed system clock (C)

Status Transition	Setting
(B) → (E) (C) → (F)	Executing HALT instruction

(6) • STOP mode (H) set while CPU is operating with internal high-speed oscillation clock (B)
• STOP mode (I) set while CPU is operating with high-speed system clock (C)

(Setting sequence) →

Status Transition	Setting	
(B) → (H) (C) → (I)	Stopping peripheral functions that cannot operate in STOP mode	Executing STOP instruction

Remarks 1. (A) to (I) in Table 5-5 correspond to (A) to (I) in Figure 5-13.

2. MCM0: Bit 0 of the main clock mode register (MCM)
RSTS, RSTOP: Bits 7 and 0 of the internal oscillation mode register (RCM)

5.6.6 Condition before changing CPU clock and processing after changing CPU clock

Condition before changing the CPU clock and processing after changing the CPU clock are shown below.

Table 5-6. Changing CPU Clock

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
Internal high-speed oscillation clock	X1 clock	Stabilization of X1 oscillation • MSTOP = 0, OSCSEL = 1, EXCLK = 0 • After elapse of oscillation stabilization time	Internal high-speed oscillator can be stopped (RSTOP = 1).
	External main system clock	Enabling input of external clock from EXCLK pin • MSTOP = 0, OSCSEL = 1, EXCLK = 1	Internal high-speed oscillator can be stopped (RSTOP = 1).
X1 clock	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator • RSTOP = 0	X1 oscillation can be stopped (MSTOP = 1).
External main system clock			External main system clock input can be disabled (MSTOP = 1).

5.6.7 Time required for switchover of main system clock

By setting bits 0 to 2 (PCC0 to PCC2) of the processor clock control register (PCC), the division ratio of the main system clock can be changed.

The actual switchover operation is not performed immediately after rewriting to PCC; operation continues on the pre-switchover clock for several clocks (refer to **Table 5-7**).

Table 5-7. Time Required for Switchover of Main System Clock Cycle Division Factor

Set Value Before Switchover			Set Value After Switchover														
PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0	PCC2	PCC1	PCC0
			0	0	0	0	0	1	0	1	0	0	1	1	1	0	0
0	0	0				16 clocks			16 clocks			16 clocks			16 clocks		
0	0	1	8 clocks						8 clocks			8 clocks			8 clocks		
0	1	0	4 clocks			4 clocks						4 clocks			4 clocks		
0	1	1	2 clocks			2 clocks			2 clocks						2 clocks		
1	0	0	1 clock			1 clock			1 clock			1 clock					

Remark The number of clocks listed in Table 5-7 is the number of CPU clocks before switchover.

By setting bit 0 (MCM0) of the main clock mode register (MCM), the main system clock can be switched (between the internal high-speed oscillation clock and the high-speed system clock).

The actual switchover operation is not performed immediately after rewriting to MCM0; operation continues on the pre-switchover clock for several clocks (refer to **Table 5-8**).

Whether the CPU is operating on the internal high-speed oscillation clock or the high-speed system clock can be ascertained using bit 1 (MCS) of MCM.

Table 5-8. Maximum Time Required for Main System Clock Switchover

Set Value Before Switchover	Set Value After Switchover	
MCM0	MCM0	
	0	1
0		$1 + 2f_{IH}/f_{XH}$ clock
1	$1 + 2f_{XH}/f_{IH}$ clock	

Caution When switching the internal high-speed oscillation clock to the high-speed system clock, bit 2 (XSEL) of MCM must be set to 1 in advance. The value of XSEL can be changed only once after a reset release.

Remarks 1. The number of clocks listed in Table 5-8 is the number of main system clocks before switchover.

2. Calculate the number of clocks in Table 5-8 by removing the decimal portion.

Example When switching the main system clock from the internal high-speed oscillation clock to the high-speed system clock (@ oscillation with f_{IH} = 8 MHz, f_{XH} = 10 MHz)

$1 + 2f_{IH}/f_{XH} = 1 + 2 \times 8/10 = 1 + 2 \times 0.8 = 1 + 1.6 = 2.6 \rightarrow 2$ clocks

5.6.8 Conditions before clock oscillation is stopped

The following lists the register flag settings for stopping the clock oscillation (disabling external clock input) and conditions before the clock oscillation is stopped.

Table 5-9. Conditions Before the Clock Oscillation Is Stopped and Flag Settings

Clock	Conditions Before Clock Oscillation Is Stopped (External Clock Input Disabled)	Flag Settings of SFR Register
Internal high-speed oscillation clock	MCS = 1 (The CPU is operating on the high-speed system clock)	RSTOP = 1
X1 clock	MCS = 0 (The CPU is operating on the internal high-speed oscillation clock)	MSTOP = 1
External main system clock		

5.6.9 Peripheral hardware and source clocks

The following lists peripheral hardware and source clocks incorporated in the µPD79F7023, 79F7024 microcontrollers.

Table 5-10. Peripheral Hardware and Source Clocks

Peripheral Hardware \ Source Clock		Peripheral Hardware Clock (f_{PRS})	Internal Low-Speed Oscillation Clock (f_{IL})	External Clock from Peripheral Hardware Pins
16-bit timer/event counter 00		Y	N	Y (TI000 pin)[Note]
8-bit timer/event counter	51	Y	N	Y (TI51 pin)[Note]
8-bit timer	H1	Y	Y	N
Watchdog timer		N	Y	N
A/D converter		Y	N	N
Serial interface	UART0	Y	N	N

Note Do not start the peripheral hardware operation with the external clock from peripheral hardware pins when in the STOP mode.

Remark Y: Can be selected, N: Cannot be selected

CHAPTER 6 16-BIT TIMER/EVENT COUNTER 00

6.1 Functions of 16-Bit Timer/Event Counter 00

16-bit timer/event counter 00 has the following functions.

(1) Interval timer

16-bit timer/event counter 00 generates an interrupt request at the preset time interval.

(2) Square-wave output

16-bit timer/event counter 00 can output a square wave with any selected frequency.

(3) External event counter

16-bit timer/event counter 00 can measure the number of pulses of an externally input signal.

(4) One-shot pulse output

16-bit timer event counter 00 can output a one-shot pulse whose output pulse width can be set freely.

(5) PPG output

16-bit timer/event counter 00 can output a rectangular wave whose frequency and output pulse width can be set freely.

(6) Pulse width measurement

16-bit timer/event counter 00 can measure the pulse width of an externally input signal.

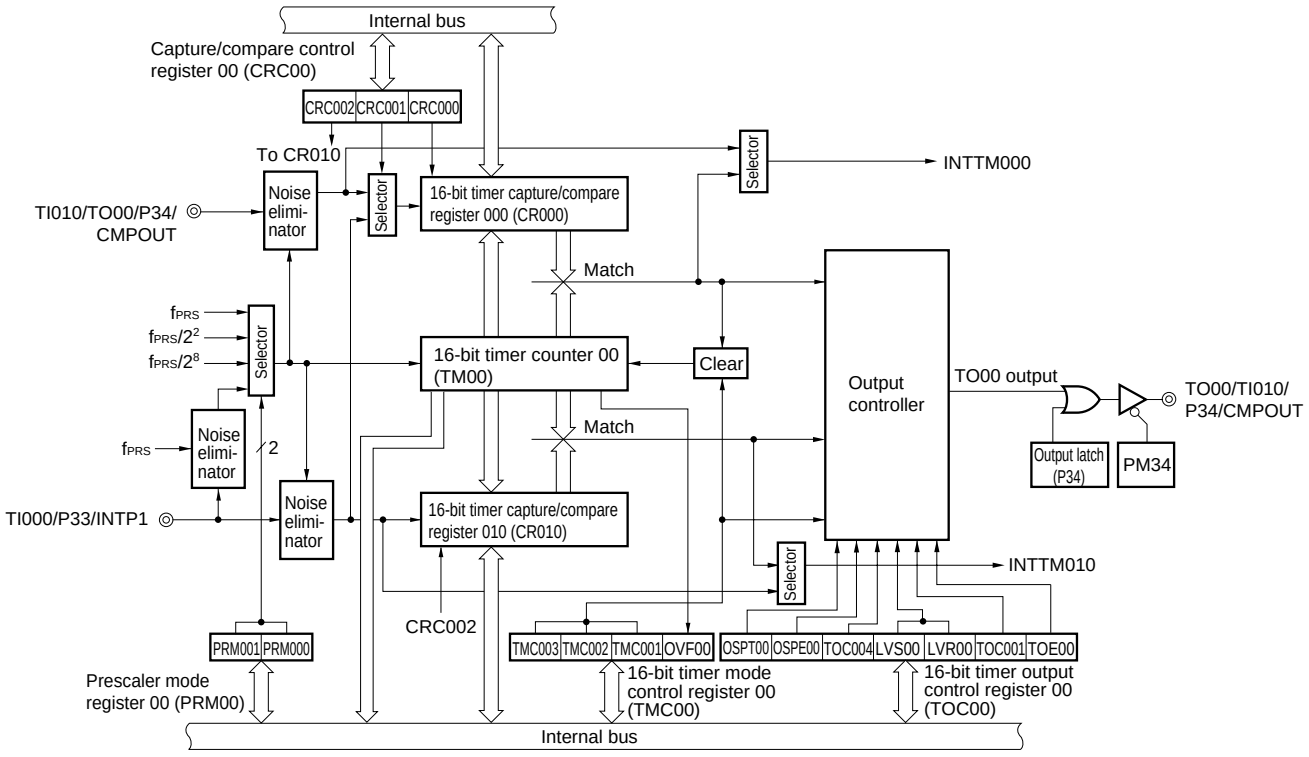
6.2 Configuration of 16-Bit Timer/Event Counter 00

16-bit timer/event counter 00 includes the following hardware.

Table 6-1. Configuration of 16-Bit Timer/Event Counter 00

Item	Configuration
Time/counter	16-bit timer counter 00 (TM00)
Register	16-bit timer capture/compare registers 000, 010 (CR000, CR010)
Timer input	TI000, TI010
Timer output	TO00, output controller
Control registers	16-bit timer mode control register 00 (TMC00) 16-bit timer capture/compare control register 00 (CRC00) 16-bit timer output control register 00 (TOC00) Prescaler mode register 00 (PRM00) Port mode register 3 (PM3) Port register 3 (P3)

Figure 6-1. Block Diagram of 16-Bit Timer/Event Counter 00



Cautions 1. The valid edge of TI010 and timer output (TO00) cannot be used for the P34 pin at the same time. Select either of the functions.

2. If clearing of bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) to 00 and input of the capture trigger conflict, then the captured data is undefined.

3. To change the mode from the capture mode to the comparison mode, first clear the TMC003 and TMC002 bits to 00, and then change the setting.

A value that has been once captured remains stored in CR000 unless the device is reset. If the mode has been changed to the comparison mode, be sure to set a comparison value.

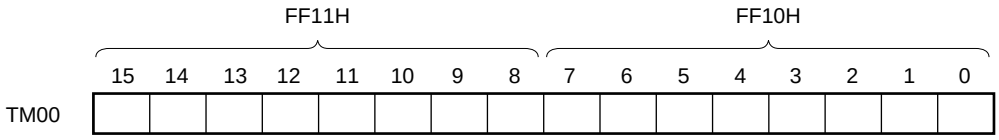
(1) 16-bit timer counter 00 (TM00)

TM00 is a 16-bit read-only register that counts count pulses.

The counter is incremented in synchronization with the rising edge of the count clock.

Figure 6-2. Format of 16-Bit Timer Counter 00 (TM00)

Address: FF10H, FF11H After reset: 0000H R



The count value of TM00 can be read by reading TM00 when the value of bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) is other than 00. The value of TM00 is 0000H if it is read when TMC003 and TMC002 = 00.

The count value is reset to 0000H in the following cases.

- At reset signal generation
- If TMC003 and TMC002 are cleared to 00
- If the valid edge of the TI000 pin is input in the mode in which the clear & start occurs when inputting the valid edge to the TI000 pin
- If TM00 and CR000 match in the mode in which the clear & start occurs when TM00 and CR000 match
- OSPT00 is set to 1 in one-shot pulse output mode or the valid edge is input to the TI000 pin

Caution Even if TM00 is read, the value is not captured by CR010.

(2) 16-bit timer capture/compare register 000 (CR000), 16-bit timer capture/compare register 010 (CR010)

CR000 and CR010 are 16-bit registers that are used with a capture function or comparison function selected by using CRC00.

Change the value of CR000 while the timer is stopped (TMC003 and TMC002 = 00).

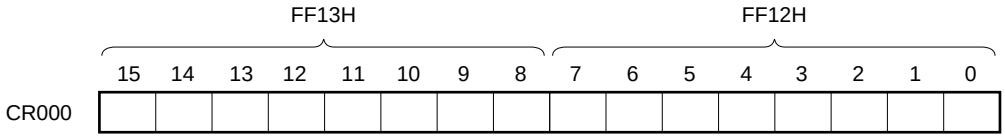
The value of CR010 can be changed during operation if the value has been set in a specific way. For details, refer to **6.5.1 Rewriting CR010 during TM00 operation**.

These registers can be read or written in 16-bit units.

Reset signal generation clears these registers to 0000H.

Figure 6-3. Format of 16-Bit Timer Capture/Compare Register 000 (CR000)

Address: FF12H, FF13H After reset: 0000H R/W



(i) When CR000 is used as a compare register

The value set in CR000 is constantly compared with the TM00 count value, and an interrupt request signal (INTTM000) is generated if they match. The value is held until CR000 is rewritten.

Caution CR000 does not perform the capture operation when it is set in the comparison mode, even if a capture trigger is input to it.

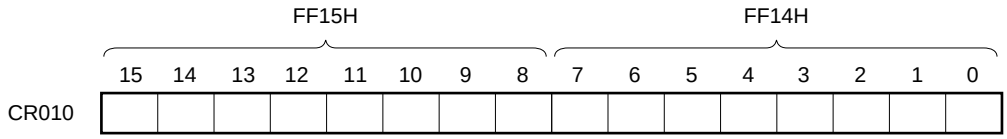
(ii) When CR000 is used as a capture register

The count value of TM00 is captured to CR000 when a capture trigger is input.

As the capture trigger, an edge of a phase reverse to that of the TI000 pin or the valid edge of the TI010 pin can be selected by using CRC00 or PRM00.

Figure 6-4. Format of 16-Bit Timer Capture/Compare Register 010 (CR010)

Address: FF14H, FF15H After reset: 0000H R/W



(i) When CR010 is used as a compare register

The value set in CR010 is constantly compared with the TM00 count value, and an interrupt request signal (INTTM010) is generated if they match.

Caution CR010 does not perform the capture operation when it is set in the comparison mode, even if a capture trigger is input to it.

(ii) When CR010 is used as a capture register

The count value of TM00 is captured to CR010 when a capture trigger is input.

It is possible to select the valid edge of the TI000 pin as the capture trigger. The TI000 pin valid edge is set by PRM00.

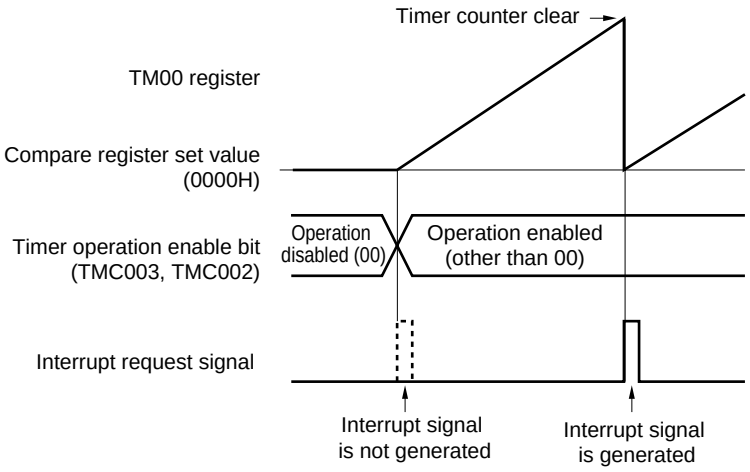
(iii) Setting range when CR000 or CR010 is used as a compare register

When CR000 or CR010 is used as a compare register, set it as shown below.

Operation	CR000 Register Setting Range	CR010 Register Setting Range
Operation as interval timer	0000H < N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH Normally, this setting is not used. Mask the match interrupt signal (INTTM010).
Operation as square-wave output		
Operation as external event counter		
Operation in the clear & start mode entered by TI000 pin valid edge input	0000H[Note] ≤ N ≤ FFFFH	0000H[Note] ≤ M ≤ FFFFH
Operation as free-running timer		
Operation as PPG output	M < N ≤ FFFFH	0000H[Note] ≤ M < N
Operation as one-shot pulse output	0000H[Note] ≤ N ≤ FFFFH (N ≠ M)	0000H[Note] ≤ M ≤ FFFFH (M ≠ N)

Note When 0000H is set, a match interrupt immediately after the timer operation does not occur and timer output is not changed, and the first match timing is as follows. A match interrupt occurs at the timing when the timer counter (TM00 register) is changed from 0000H to 0001H.

- When the timer counter is cleared due to overflow
- When the timer counter is cleared due to TI000 pin valid edge (when clear & start mode is entered by TI000 pin valid edge input)
- When the timer counter is cleared due to compare match (when clear & start mode is entered by match between TM00 and CR000 (CR000 = other than 0000H, CR010 = 0000H))



Remarks 1. N: CR000 register set value, M: CR010 register set value

2. For details of the operation enable bits (bits 3 and 2 (TMC003 and TMC002)), refer to **6.3 (1) 16-bit timer mode control register 00 (TMC00)**.

Table 6-2. Capture Operation of CR000 and CR010

External Input Signal / Capture Operation	TI000 Pin Input		TI010 Pin Input	
Capture operation of CR000	CRC001 = 1 TI000 pin input (reverse phase)	Set values of ES010 and ES000 Position of edge to be captured	CRC001 bit = 0 TI010 pin input	Set values of ES110 and ES100 Position of edge to be captured
		01: Rising		01: Rising
		00: Falling		00: Falling
		11: Both edges (cannot be captured)		11: Both edges
	Interrupt signal	INTTM000 signal is not generated even if value is captured.	Interrupt signal	INTTM000 signal is generated each time value is captured.
Capture operation of CR010	TI000 pin input[Note]	Set values of ES010 and ES000 Position of edge to be captured		
		01: Rising		
		00: Falling		
		11: Both edges		
	Interrupt signal	INTTM010 signal is generated each time value is captured.		

Note The capture operation of CR010 is not affected by the setting of the CRC001 bit.

Caution To capture the count value of the TM00 register to the CR000 register by using the phase reverse to that input to the TI000 pin, the interrupt request signal (INTTM000) is not generated after the value has been captured. If the valid edge is detected on the TI010 pin during this operation, the capture operation is not performed but the INTTM000 signal is generated as an external interrupt signal. To not use the external interrupt, mask the INTTM000 signal.

Remark CRC001: Refer to **6.3 (2) Capture/compare control register 00 (CRC00)**.
ES110, ES100, ES010, ES000: Refer to **6.3 (4) Prescaler mode register 00 (PRM00)**.

6.3 Registers Controlling 16-Bit Timer/Event Counter 00

Registers used to control 16-bit timer/event counter 00 are shown below.

- 16-bit timer mode control register 00 (TMC00)
- Capture/compare control register 00 (CRC00)
- 16-bit timer output control register 00 (TOC00)
- Prescaler mode register 00 (PRM00)
- Port mode register 3 (PM3)
- Port register 3 (P3)

(1) 16-bit timer mode control register 00 (TMC00)

TMC00 is an 8-bit register that sets the 16-bit timer/event counter 00 operation mode, TM00 clear mode, and output timing, and detects an overflow.

Rewriting TMC00 is prohibited during operation (when TMC003 and TMC002 = other than 00). However, it can be changed when TMC003 and TMC002 are cleared to 00 (stopping operation) and when OVF00 is cleared to 0.

TMC00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears TMC00 to 00H.

Caution 16-bit timer/event counter 00 starts operation at the moment TMC003 and TMC002 are set to values other than 00 (operation stop mode), respectively. Set TMC003 and TMC002 to 00 to stop the operation.

Figure 6-5. Format of 16-Bit Timer Mode Control Register 00 (TMC00)

Address: FF86H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
TMC00	0	0	0	0	TMC003	TMC002	TMC001	OVF00

TMC003	TMC002	Operation enable of 16-bit timer/event counter 00
0	0	Disables 16-bit timer/event counter 00 operation. Stops supplying operating clock. Clears 16-bit timer counter 00 (TM00).
0	1	Free-running timer mode
1	0	Clear & start mode entered by TI000 pin valid edge input[Note]
1	1	Clear & start mode entered upon a match between TM00 and CR000

TMC001	Condition to reverse timer output (TO00)
0	• Match between TM00 and CR000 or match between TM00 and CR010
1	• Match between TM00 and CR000 or match between TM00 and CR010 • Trigger input of TI000 pin valid edge

OVF00	TM00 overflow flag
Clear (0)	Clears OVF00 to 0 or TMC003 and TMC002 = 00
Set (1)	Overflow occurs.
OVF00 is set to 1 when the value of TM00 changes from FFFFH to 0000H in all the operation modes (free-running timer mode, clear & start mode entered by TI000 pin valid edge input, and clear & start mode entered upon a match between TM00 and CR000). It can also be set to 1 by writing 1 to OVF00.	

Note The TI000 pin valid edge is set by bits 5 and 4 (ES010, ES000) of prescaler mode register 00 (PRM00).

(2) Capture/compare control register 00 (CRC00)

CRC00 is the register that controls the operation of CR000 and CR010.

Changing the value of CRC00 is prohibited during operation (when TMC003 and TMC002 = other than 00).

CRC00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CRC00 to 00H.

Figure 6-6. Format of Capture/Compare Control Register 00 (CRC00)

Address: FF88H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CRC00	0	0	0	0	0	CRC002	CRC001	CRC000

CRC002	CR010 operating mode selection
0	Operates as compare register
1	Operates as capture register

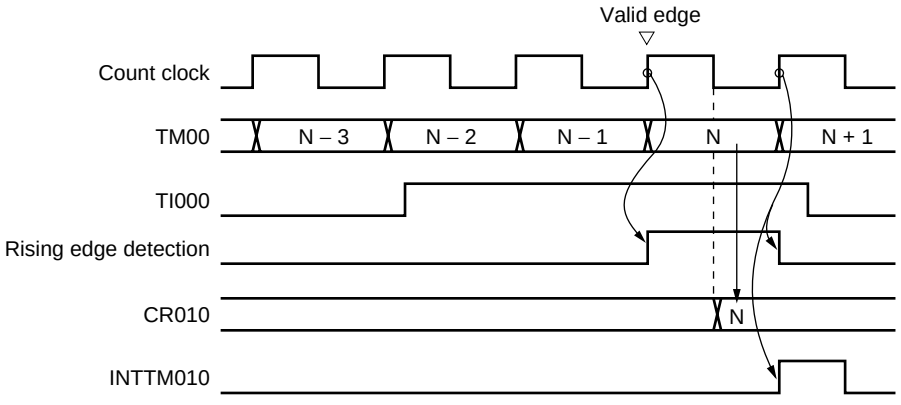
CRC001	CR000 capture trigger selection
0	Captures on valid edge of TI010 pin
1	Captures on valid edge of TI000 pin by reverse phase[Note]
The valid edge of the TI010 and TI000 pin is set by PRM00. If ES010 and ES000 are set to 11 (both edges) when CRC001 is 1, the valid edge of the TI000 pin cannot be detected.	

CRC000	CR000 operating mode selection
0	Operates as compare register
1	Operates as capture register
If TMC003 and TMC002 are set to 11 (clear & start mode entered upon a match between TM00 and CR000), be sure to set CRC000 to 0.	

Note When the valid edge is detected from the TI010 pin, the capture operation is not performed but the INTTM000 signal is generated as an external interrupt signal.

Caution To ensure that the capture operation is performed properly, the capture trigger requires a pulse two cycles longer than the count clock selected by prescaler mode register 00 (PRM00).

Figure 6-7. Example of CR010 Capture Operation (When Rising Edge Is Specified)



(3) 16-bit timer output control register 00 (TOC00)

TOC00 is an 8-bit register that controls the TO00 output.

TOC00 can be rewritten while only OSPT00 is operating (when TMC003 and TMC002 = other than 00). Rewriting the other bits is prohibited during operation.

However, TOC004 can be rewritten during timer operation as a means to rewrite CR010 (refer to **6.5.1 Rewriting CR010 during TM00 operation**).

TOC00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears TOC00 to 00H.

Caution Be sure to set TOC00 using the following procedure.

<1> Set TOC004 and TOC001 to 1.

<2> Set only TOE00 to 1.

<3> Set either of LVS00 or LVR00 to 1.

Figure 6-8. Format of 16-Bit Timer Output Control Register 00 (TOC00)

Address: FF89H After reset: 00H R/W

Symbol	7	<6>	<5>	4	<3>	<2>	1	<0>
TOC00	0	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00

OSPT00	One-shot pulse output trigger via software
0	–
1	One-shot pulse output
The value of this bit is always “0” when it is read. Do not set this bit to 1 in a mode other than the one-shot pulse output mode. If it is set to 1, TM00 is cleared and started.	

OSPE00	One-shot pulse output operation control
0	Successive pulse output
1	One-shot pulse output
One-shot pulse output operates correctly in the free-running timer mode or clear & start mode entered by TI000 pin valid edge input. The one-shot pulse cannot be output in the clear & start mode entered upon a match between TM00 and CR000.	

TOC004	TO00 output control on match between CR010 and TM00
0	Disables inversion operation
1	Enables inversion operation
The interrupt signal (INTTM010) is generated even when TOC004 = 0.	

LVS00	LVR00	Setting of TO00 output status
0	0	No change
0	1	Initial value of TO00 output is low level (TO00 output is cleared to 0).
1	0	Initial value of TO00 output is high level (TO00 output is set to 1).
1	1	Setting prohibited

- LVS00 and LVR00 can be used to set the initial value of the TO00 output level. If the initial value does not have to be set, leave LVS00 and LVR00 as 00.
- Be sure to set LVS00 and LVR00 when TOE00 = 1.
  LVS00, LVR00, and TOE00 being simultaneously set to 1 is prohibited.
- LVS00 and LVR00 are trigger bits. By setting these bits to 1, the initial value of the TO00 output level can be set. Even if these bits are cleared to 0, TO00 output is not affected.
- The values of LVS00 and LVR00 are always 0 when they are read.
- For how to set LVS00 and LVR00, refer to **6.5.2 Setting LVS00 and LVR00**.
- The actual TO00/TI010/P01 pin output is determined depending on PM01 and P01, besides TO00 output.

TOC001	TO00 output control on match between CR000 and TM00
0	Disables inversion operation
1	Enables inversion operation
The interrupt signal (INTTM000) is generated even when TOC001 = 0.	

TOE00	TO00 output control
0	Disables output (TO00 output fixed to low level)
1	Enables output

(4) Prescaler mode register 00 (PRM00)

PRM00 is the register that sets the TM00 count clock and TI000 and TI010 pin input valid edges.

Rewriting PRM00 is prohibited during operation (when TMC003 and TMC002 = other than 00).

PRM00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears PRM00 to 00H.

Cautions 1. Do not apply the following setting when setting the PRM001 and PRM000 bits to 11 (to specify the valid edge of the TI000 pin as a count clock).

- **Clear & start mode entered by the TI000 pin valid edge**
- **Setting the TI000 pin as a capture trigger**

2. If the operation of the 16-bit timer/event counter 00 is enabled when the TI000 or TI010 pin is at high level and when the valid edge of the TI000 or TI010 pin is specified to be the rising edge or both edges, the high level of the TI000 or TI010 pin is detected as a rising edge. Note this when the TI000 or TI010 pin is pulled up. However, the rising edge is not detected when the timer operation has been once stopped and then is enabled again.

3. The valid edge of TI010 and timer output (TO00) cannot be used for the P34 pin at the same time. Select either of the functions.

Figure 6-9. Format of Prescaler Mode Register 00 (PRM00)

Address: FF87H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PRM00	ES110	ES100	ES010	ES000	0	0	PRM001	PRM000

ES110	ES100	TI010 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

ES010	ES000	TI000 pin valid edge selection
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both falling and rising edges

PRM001	PRM000	Count clock selection		
			f_{PRS} = 2 MHz	f_{PRS} = 5 MHz
0	0	f_{PRS}	2 MHz	5 MHz
0	1	$f_{PRS}/2^2$	500 kHz	1.25 MHz
1	0	$f_{PRS}/2^8$	7.81 kHz	19.53 kHz
1	1	TI000 valid edge Notes 1, 2		

Notes 1. The external clock from the TI000 pin requires a pulse longer than twice the cycle of the peripheral hardware clock (f_{PRS}).

2. Do not start timer operation with the external clock from the TI000 pin when in the STOP mode.

Remark f_{PRS}: Peripheral hardware clock frequency

(5) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P34/TO00/TI010/CMPOUT pin for timer output, set PM34 and the output latches of P34 to 0.

When using the P33/TI000/INTP1 and P34/TI010/TO00/CMPOUT pins for timer input, set PM33 and PM34 to 1. At this time, the output latches of P33 and P34 may be 0 or 1.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM3 to FFH.

Figure 6-10. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	1	1	PM34	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

6.4 Operation of 16-Bit Timer/Event Counter 00

6.4.1 Interval timer operation

If bits 3 and 2 (TMC003 and TMC002) of the 16-bit timer mode control register (TMC00) are set to 11 (clear & start mode entered upon a match between TM00 and CR000), the count operation is started in synchronization with the count clock.

When the value of TM00 later matches the value of CR000, TM00 is cleared to 0000H and a match interrupt signal (INTTM000) is generated. This INTTM000 signal enables TM00 to operate as an interval timer.

Remarks 1. For the setting of I/O pins, refer to **6.3 (5) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

Figure 6-11. Block Diagram of Interval Timer Operation

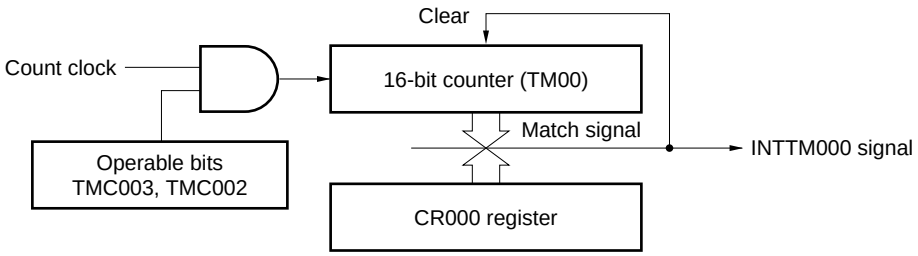


Figure 6-12. Basic Timing Example of Interval Timer Operation

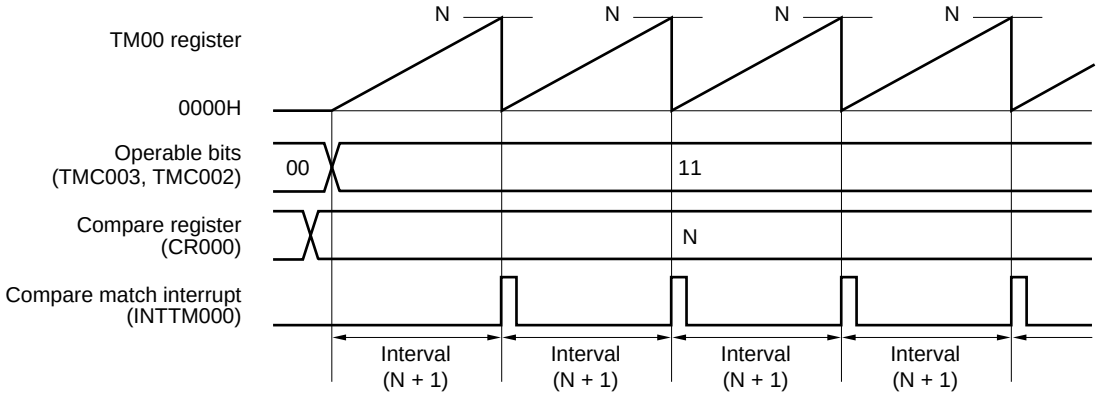


Figure 6-13. Example of Register Settings for Interval Timer Operation

(a) 16-bit timer mode control register 00 (TMC00)

				TMC003	TMC002	TMC001	OVF00
0	0	0	0	1	1	0	0

Clears and starts on match between TM00 and CR000.

(b) Capture/compare control register 00 (CRC00)

					CRC002	CRC001	CRC000
0	0	0	0	0	0	0	0

CR000 used as compare register

(c) 16-bit timer output control register 00 (TOC00)

	OSPT00	OSPE00	TOC004	LVS00	LVR00	TOC001	TOE00
0	0	0	0	0	0	0	0

(d) Prescaler mode register 00 (PRM00)

ES110	ES100	ES010	ES000	3	2	PRM001	PRM000
0	0	0	0	0	0	0/1	0/1

Selects count clock

(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

If M is set to CR000, the interval time is as follows.

- Interval time = (M + 1) × Count clock cycle

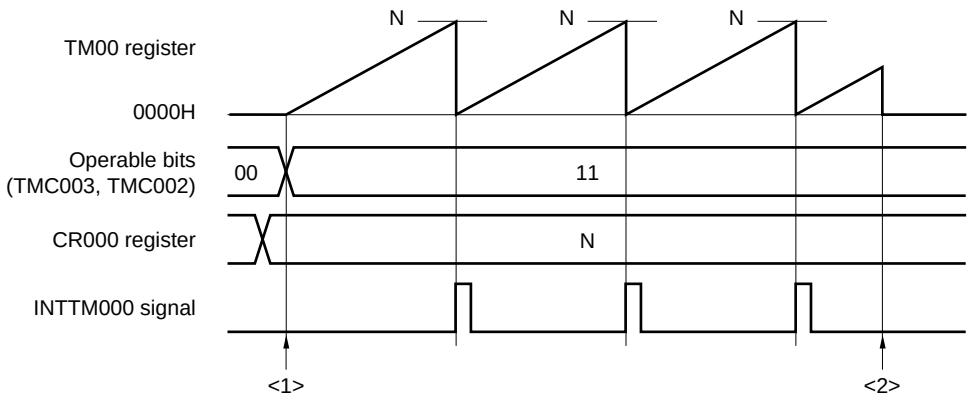
Setting CR000 to 0000H is prohibited.

(g) 16-bit capture/compare register 010 (CR010)

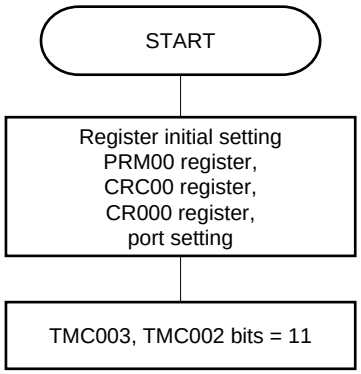
Usually, CR010 is not used for the interval timer function. However, a compare match interrupt (INTTM010) is generated when the set value of CR010 matches the value of TM00.

Therefore, mask the interrupt request by using the interrupt mask flag (TMMK010).

Figure 6-14. Example of Software Processing for Interval Timer Function



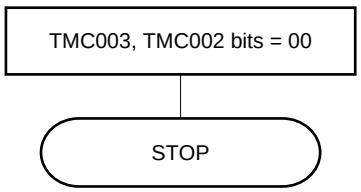
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 11.

Starts count operation

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

6.4.2 Square-wave output operation

When 16-bit timer/event counter 00 operates as an interval timer (refer to **6.4.1**), a square wave can be output from the TO00 pin by setting the 16-bit timer output control register 00 (TOC00) to 03H.

When TMC003 and TMC002 are set to 11 (count clear & start mode entered upon a match between TM00 and CR000), the counting operation is started in synchronization with the count clock.

When the value of TM00 later matches the value of CR000, TM00 is cleared to 0000H, an interrupt signal (INTTM000) is generated, and TO00 output is inverted. This TO00 output that is inverted at fixed intervals enables TO0n to output a square wave.

Remarks 1. For the setting of I/O pins, refer to **6.3 (5) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

Figure 6-15. Block Diagram of Square-Wave Output Operation

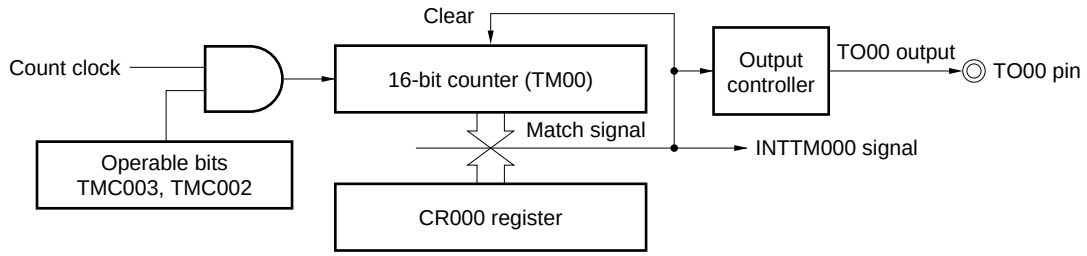


Figure 6-16. Basic Timing Example of Square-Wave Output Operation

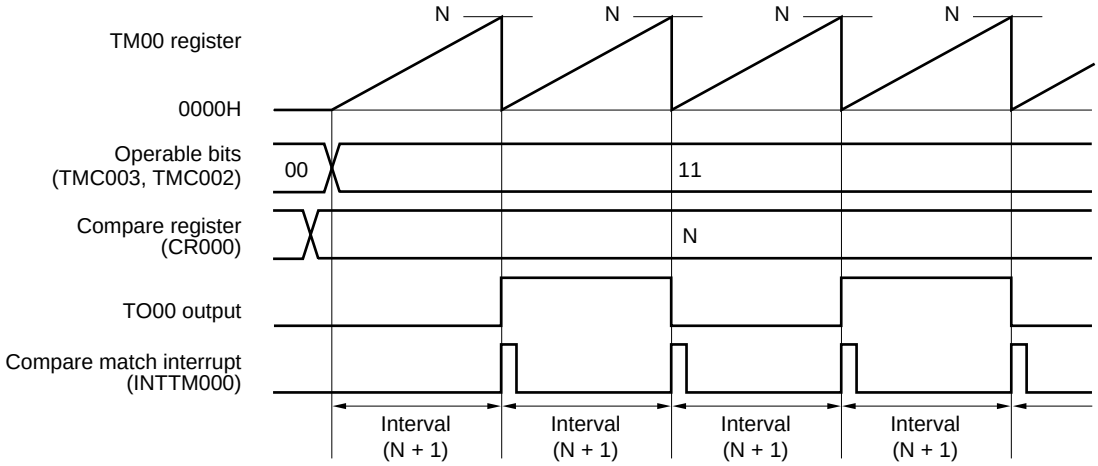
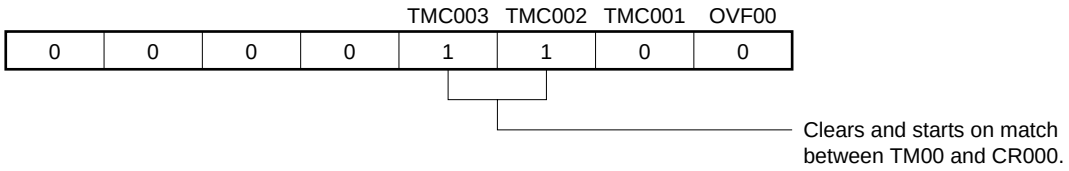
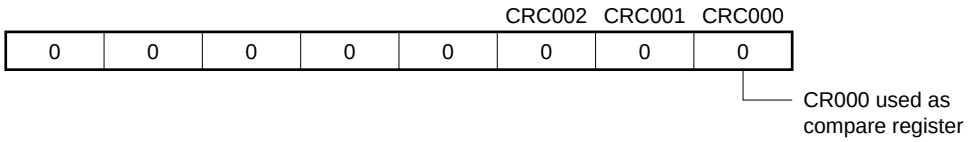


Figure 6-17. Example of Register Settings for Square-Wave Output Operation

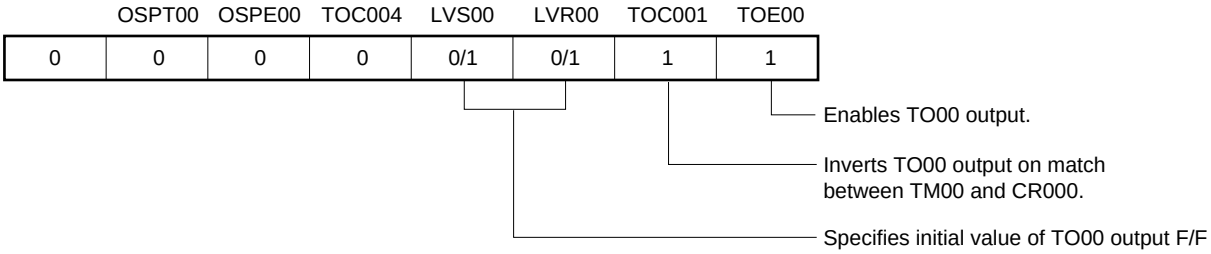
(a) 16-bit timer mode control register 00 (TMC00)



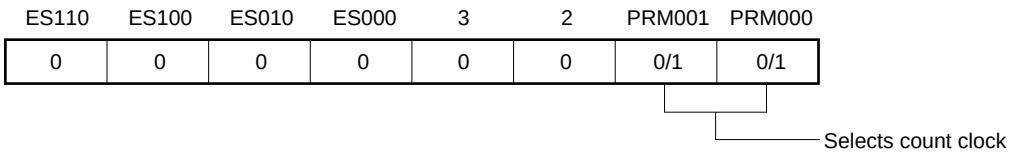
(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



(d) Prescaler mode register 00 (PRM00)



(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

If M is set to CR000, the interval time is as follows.

- Square wave frequency = 1 / [2 × (M + 1) × Count clock cycle]

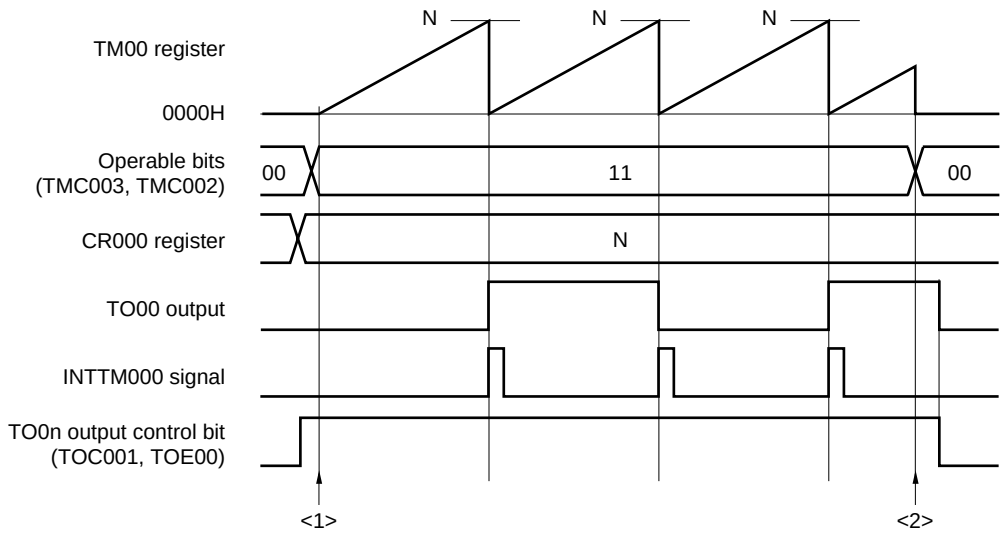
Setting CR000 to 0000H is prohibited.

(g) 16-bit capture/compare register 010 (CR010)

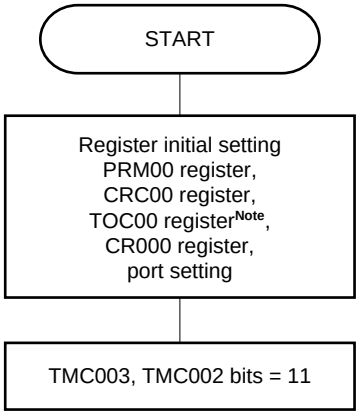
Usually, CR010 is not used for the square-wave output function. However, a compare match interrupt (INTTM010) is generated when the set value of CR010 matches the value of TM00.

Therefore, mask the interrupt request by using the interrupt mask flag (TMMK010).

Figure 6-18. Example of Software Processing for Square-Wave Output Function



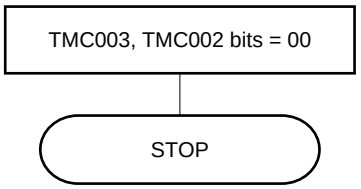
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 11.

Starts count operation

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

Note Care must be exercised when setting TOC00. For details, refer to **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

6.4.3 External event counter operation

When bits 1 and 0 (PRM001 and PRM000) of the prescaler mode register 00 (PRM00) are set to 11 (for counting up with the valid edge of the TI000 pin) and bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 11, the valid edge of an external event input is counted, and a match interrupt signal indicating matching between TM00 and CR000 (INTTM000) is generated.

To input the external event, the TI000 pin is used. Therefore, the timer/event counter cannot be used as an external event counter in the clear & start mode entered by the TI000 pin valid edge input (when TMC003 and TMC002 = 10).

The INTTM000 signal is generated with the following timing.

- Timing of generation of INTTM000 signal (second time or later)
  = Number of times of detection of valid edge of external event × (Set value of CR000 + 1)

However, the first match interrupt immediately after the timer/event counter has started operating is generated with the following timing.

- Timing of generation of INTTM000 signal (first time only)
  = Number of times of detection of valid edge of external event input × (Set value of CR000 + 2)

To detect the valid edge, the signal input to the TI000 pin is sampled during the clock cycle of f_{PRS}. The valid edge is not detected until it is detected two times in a row. Therefore, a noise with a short pulse width can be eliminated.

Remarks 1. For the setting of I/O pins, refer to **6.3 (5) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

Figure 6-19. Block Diagram of External Event Counter Operation

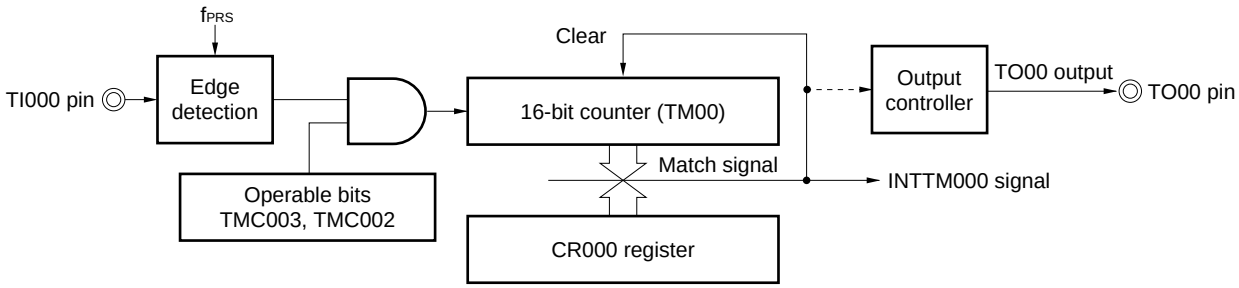
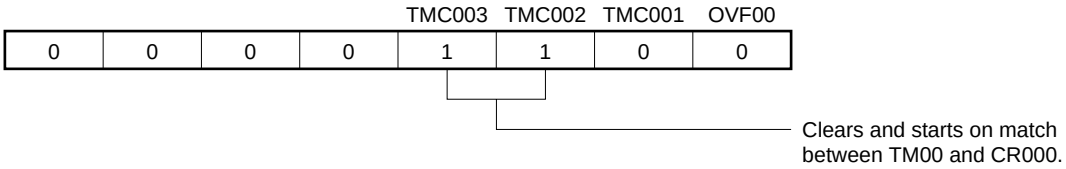
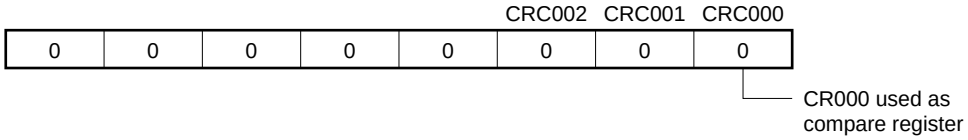


Figure 6-20. Example of Register Settings in External Event Counter Mode (1/2)

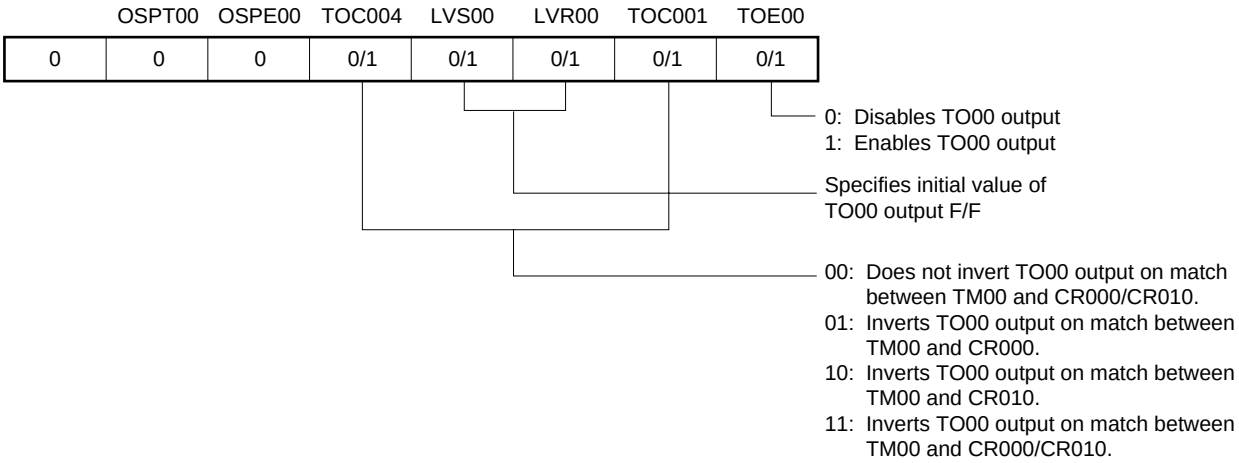
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



(d) Prescaler mode register 00 (PRM00)

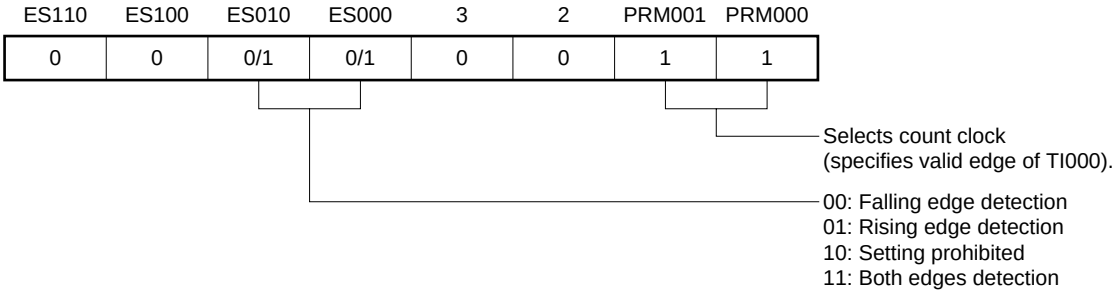


Figure 6-20. Example of Register Settings in External Event Counter Mode (2/2)

(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

If M is set to CR000, the interrupt signal (INTTM000) is generated when the number of external events reaches (M + 1).

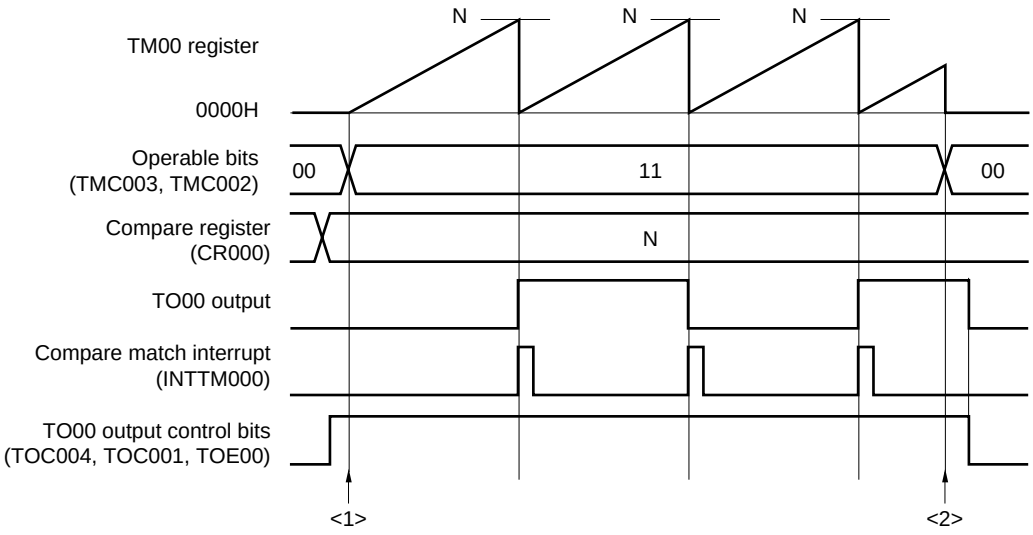
Setting CR000 to 0000H is prohibited.

(g) 16-bit capture/compare register 010 (CR010)

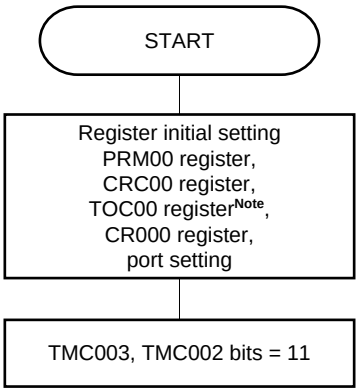
Usually, CR010 is not used in the external event counter mode. However, a compare match interrupt (INTTM010) is generated when the set value of CR010 matches the value of TM00.

Therefore, mask the interrupt request by using the interrupt mask flag (TMMK010).

Figure 6-21. Example of Software Processing in External Event Counter Mode



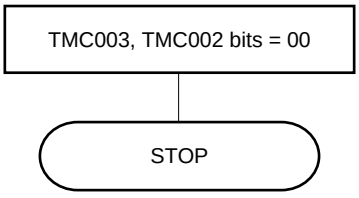
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 11.

Starts count operation

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

Note Care must be exercised when setting TOC00. For details, refer to **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

6.4.4 Operation in clear & start mode entered by TI000 pin valid edge input

When bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 10 (clear & start mode entered by the TI000 pin valid edge input) and the count clock (set by PRM00) is supplied to the timer/event counter, TM00 starts counting up. When the valid edge of the TI000 pin is detected during the counting operation, TM00 is cleared to 0000H and starts counting up again. If the valid edge of the TI000 pin is not detected, TM00 overflows and continues counting.

The valid edge of the TI000 pin is a cause to clear TM00. Starting the counter is not controlled immediately after the start of the operation.

CR000 and CR010 are used as compare registers and capture registers.

(a) When CR000 and CR010 are used as compare registers

Signals INTTM000 and INTTM010 are generated when the value of TM00 matches the value of CR000 and CR010.

(b) When CR000 and CR010 are used as capture registers

The count value of TM00 is captured to CR000 and the INTTM000 signal is generated when the valid edge is input to the TI010 pin (or when the phase reverse to that of the valid edge is input to the TI000 pin).

When the valid edge is input to the TI000 pin, the count value of TM00 is captured to CR010 and the INTTM010 signal is generated. As soon as the count value has been captured, the counter is cleared to 0000H.

Caution Do not set the count clock as the valid edge of the TI000 pin (PRM001 and PRM000 = 11). When PRM001 and PRM000 = 11, TM00 is cleared.

Remarks 1. For the setting of the I/O pins, refer to **6.3 (5) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

(1) Operation in clear & start mode entered by TI000 pin valid edge input (CR000: compare register, CR010: compare register)

Figure 6-22. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Compare Register)

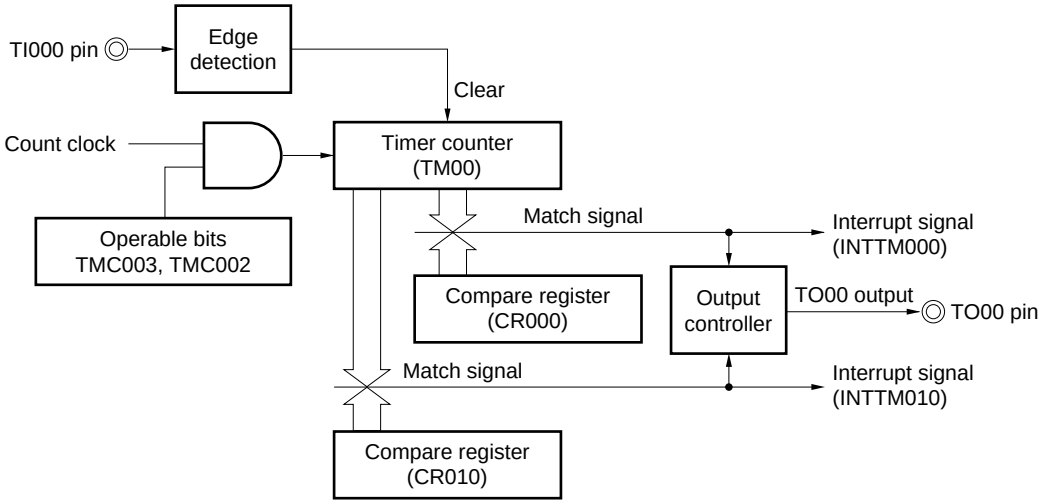
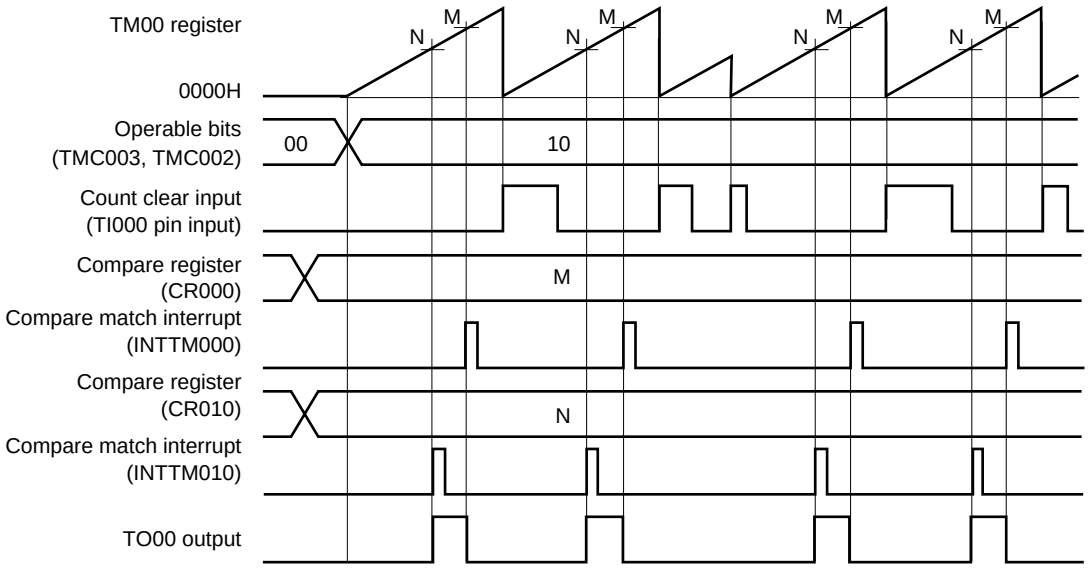
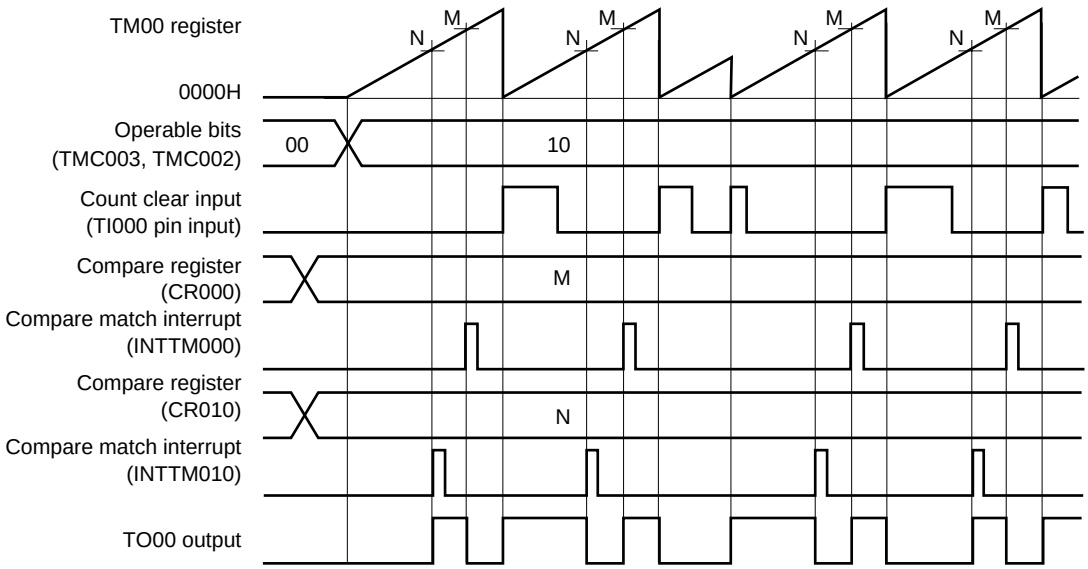


Figure 6-23. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Compare Register)

(a) TOC00 = 13H, PRM00 = 10H, CRC00 = 00H, TMC00 = 08H



(b) TOC00 = 13H, PRM00 = 10H, CRC00 = 00H, TMC00 = 0AH



(a) and (b) differ as follows depending on the setting of bit 1 (TMC001) of the 16-bit timer mode control register 00 (TMC00).

(a) The TO00 output level is inverted when TM00 matches a compare register.

(b) The TO00 output level is inverted when TM00 matches a compare register or when the valid edge of the TI000 pin is detected.

(2) Operation in clear & start mode entered by TI000 pin valid edge input
(CR000: compare register, CR010: capture register)

Figure 6-24. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register)

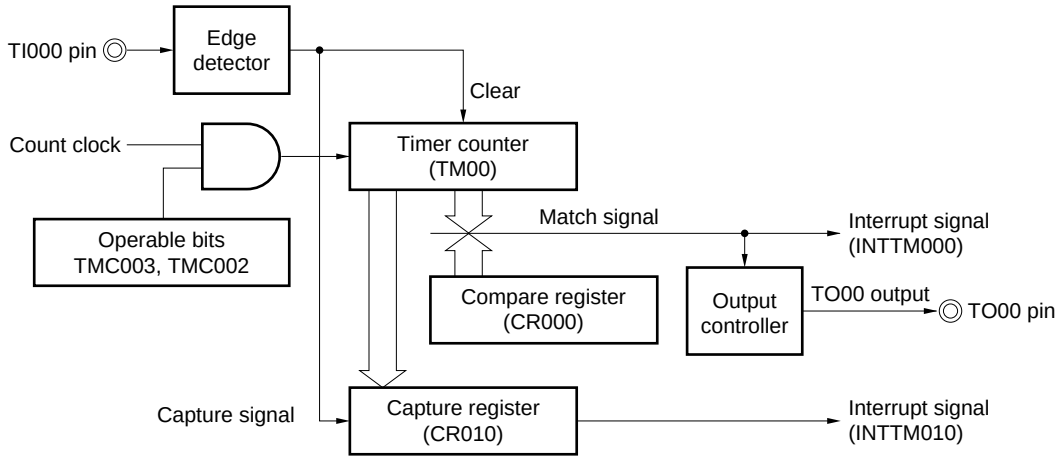
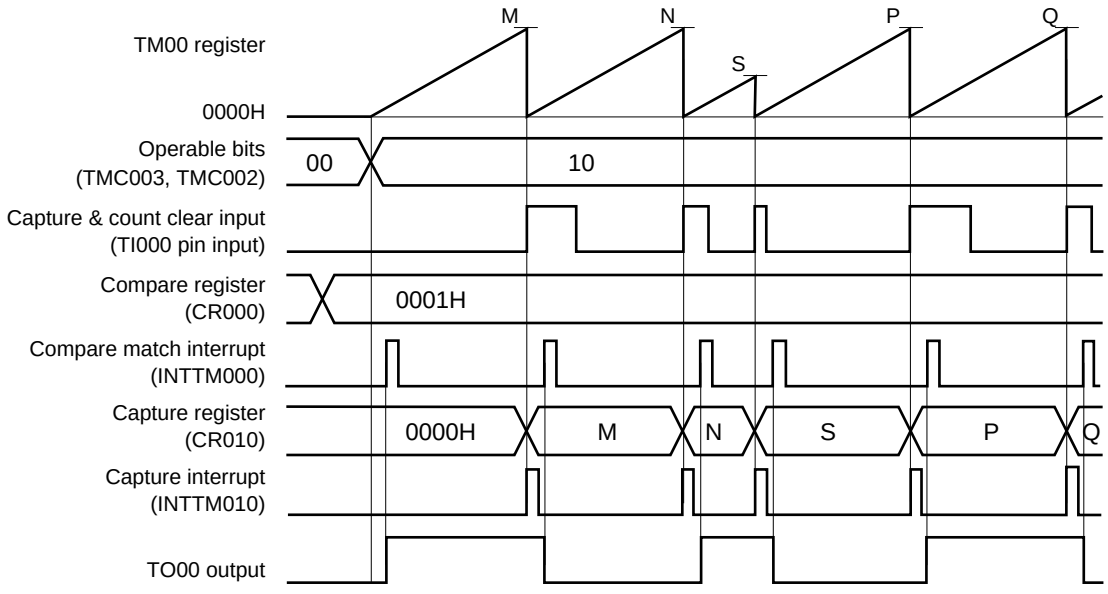


Figure 6-25. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register) (1/2)

(a) TOC00 = 13H, PRM00 = 10H, CRC00 = 04H, TMC00 = 08H, CR000 = 0001H

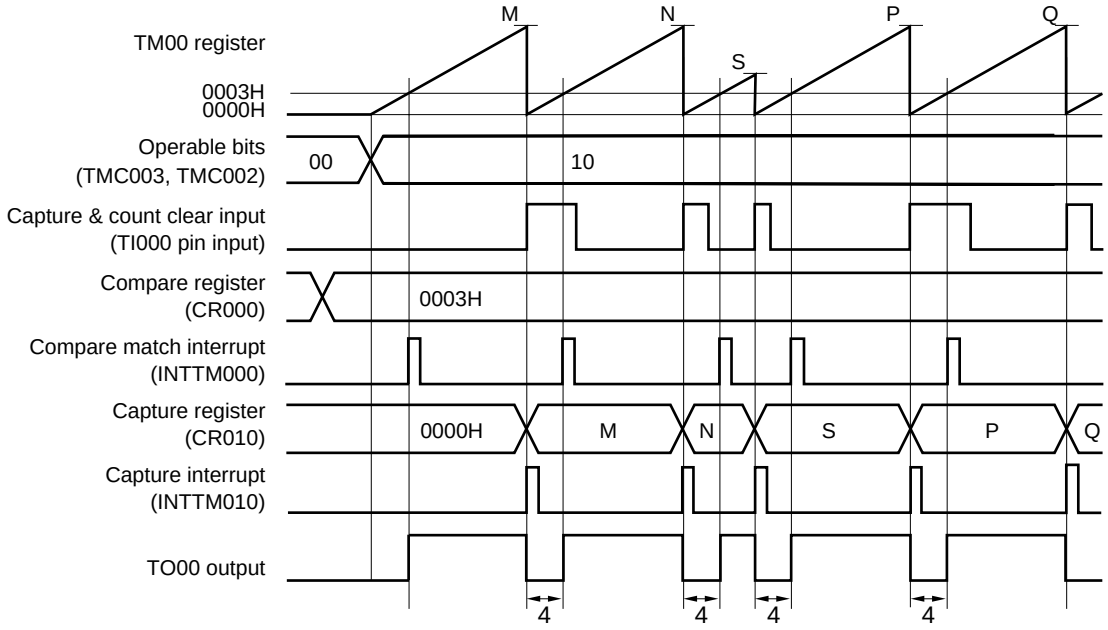


This is an application example where the TO00 output level is inverted when the count value has been captured & cleared.

The count value is captured to CR010 and TM00 is cleared (to 0000H) when the valid edge of the TI000 pin is detected. When the count value of TM00 is 0001H, a compare match interrupt signal (INTTM000) is generated, and the TO00 output level is inverted.

Figure 6-25. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register) (2/2)

(b) TOC00 = 13H, PRM00 = 10H, CRC00 = 04H, TMC00 = 0AH, CR000 = 0003H



This is an application example where the width set to CR000 (4 clocks in this example) is to be output from the TO00 pin when the count value has been captured & cleared.

The count value is captured to CR010, a capture interrupt signal (INTTM010) is generated, TM00 is cleared (to 0000H), and the TO00 output level is inverted when the valid edge of the TI000 pin is detected. When the count value of TM00 is 0003H (four clocks have been counted), a compare match interrupt signal (INTTM000) is generated and the TO00 output level is inverted.

(3) Operation in clear & start mode by entered TI000 pin valid edge input (CR000: capture register, CR010: compare register)

Figure 6-26. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Compare Register)

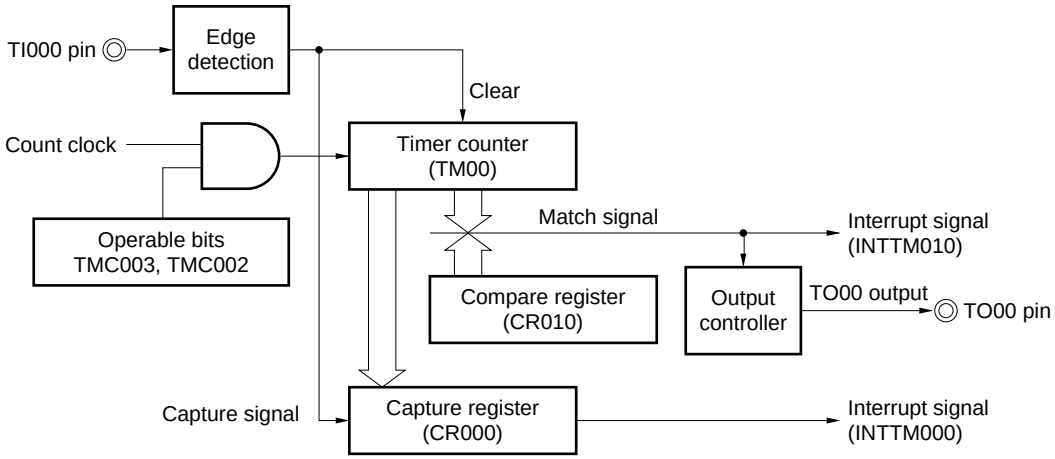
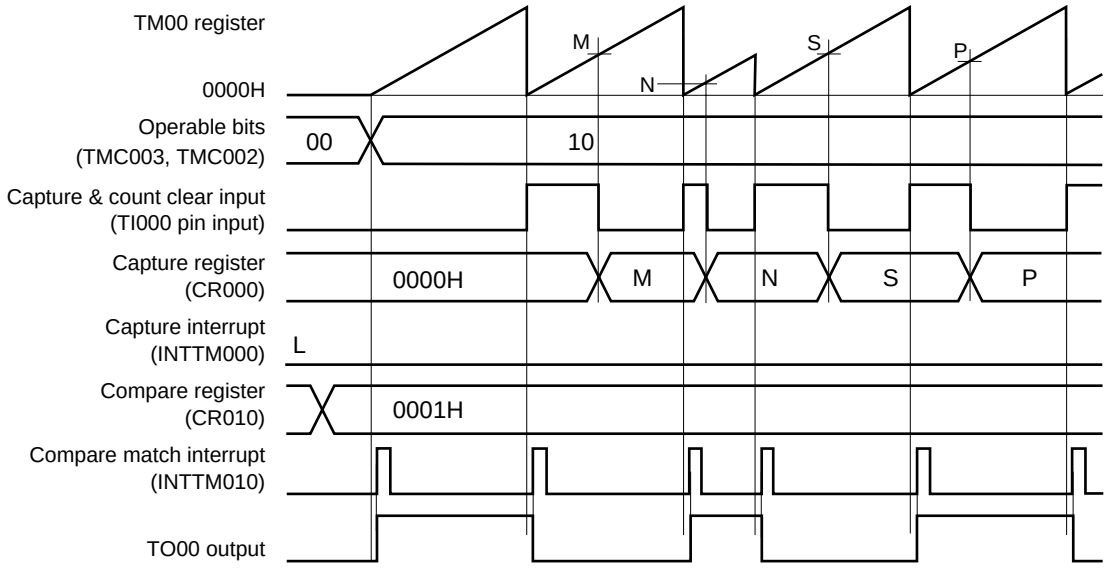


Figure 6-27. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Compare Register) (1/2)

(a) TOC00 = 13H, PRM00 = 10H, CRC00 = 03H, TMC00 = 08H, CR010 = 0001H



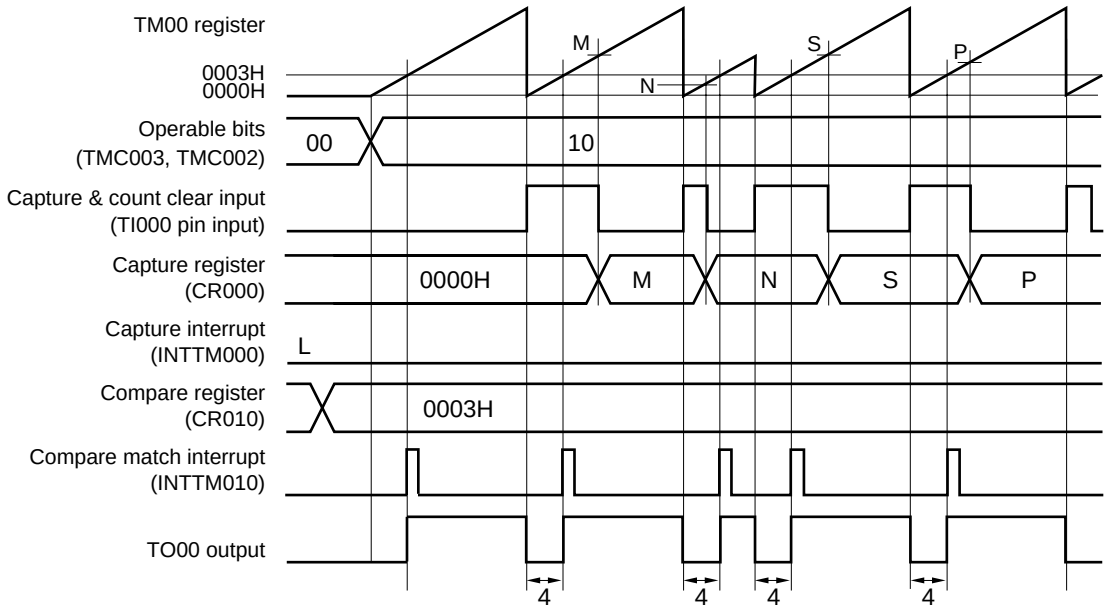
This is an application example where the TO00 output level is to be inverted when the count value has been captured & cleared.

TM00 is cleared at the rising edge detection of the TI000 pin and it is captured to CR000 at the falling edge detection of the TI000 pin.

When bit 1 (CRC001) of capture/compare control register 00 (CRC00) is set to 1, the count value of TM00 is captured to CR000 in the phase reverse to that of the signal input to the TI000 pin, but the capture interrupt signal (INTTM000) is not generated. However, the INTTM000 signal is generated when the valid edge of the TI010 pin is detected. Mask the INTTM000 signal when it is not used.

Figure 6-27. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Compare Register) (2/2)

(b) TOC00 = 13H, PRM00 = 10H, CRC00 = 03H, TMC00 = 0AH, CR010 = 0003H



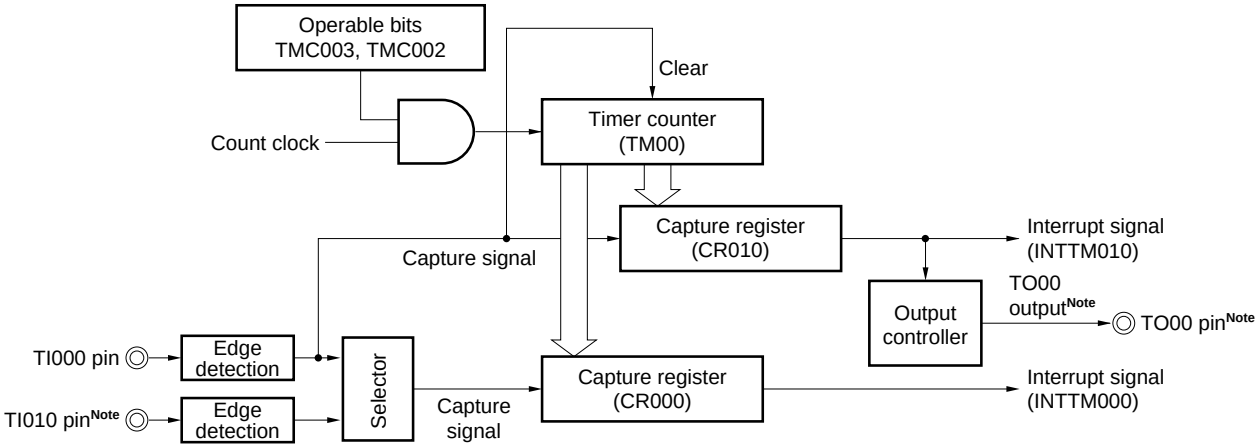
This is an application example where the width set to CR010 (4 clocks in this example) is to be output from the TO00 pin when the count value has been captured & cleared.

TM00 is cleared (to 0000H) at the rising edge detection of the TI000 pin and captured to CR000 at the falling edge detection of the TI000 pin. The TO00 output level is inverted when TM00 is cleared (to 0000H) because the rising edge of the TI000 pin has been detected or when the value of TM00 matches that of a compare register (CR010).

When bit 1 (CRC001) of capture/compare control register 00 (CRC00) is 1, the count value of TM00 is captured to CR000 in the phase reverse to that of the input signal of the TI000 pin, but the capture interrupt signal (INTTM000) is not generated. However, the INTTM000 interrupt is generated when the valid edge of the TI010 pin is detected. Mask the INTTM000 signal when it is not used.

(4) Operation in clear & start mode entered by TI000 pin valid edge input (CR000: capture register, CR010: capture register)

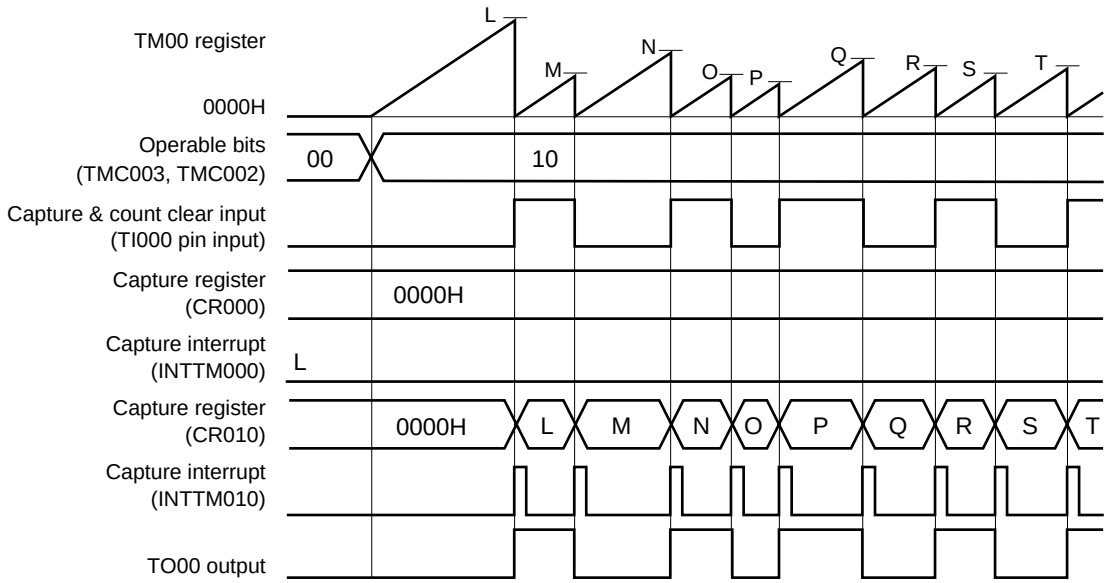
Figure 6-28. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Capture Register)



Note The timer output (TO00) cannot be used when detecting the valid edge of the TI010 pin is used.

Figure 6-29. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Capture Register) (1/3)

(a) TOC00 = 13H, PRM00 = 30H, CRC00 = 05H, TMC00 = 0AH

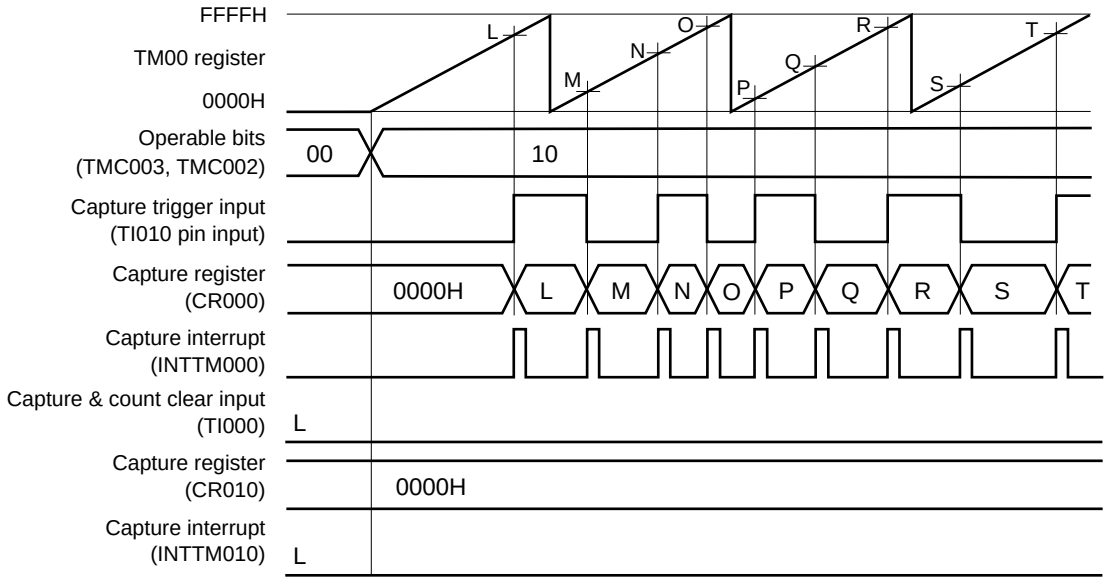


This is an application example where the count value is captured to CR010, TM00 is cleared, and the TO00 output is inverted when the rising or falling edge of the TI000 pin is detected.

When the edge of the TI010 pin is detected, an interrupt signal (INTTM000) is generated. Mask the INTTM000 signal when it is not used.

Figure 6-29. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Capture Register) (2/3)

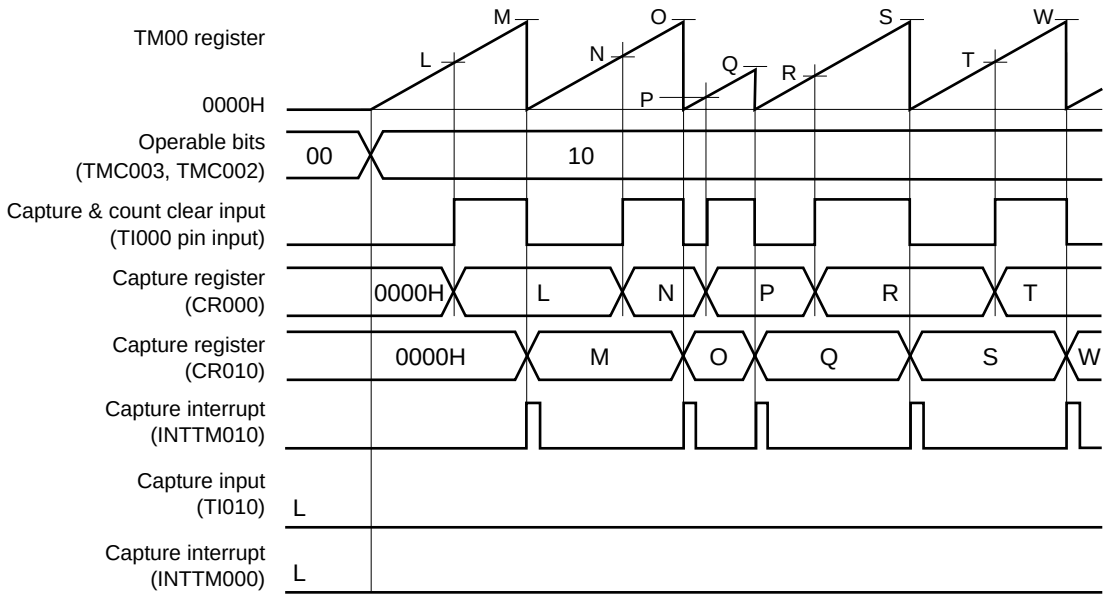
(b) TOC00 = 13H, PRM00 = C0H, CRC00 = 05H, TMC00 = 0AH



This is a timing example where an edge is not input to the TI000 pin, in an application where the count value is captured to CR000 when the rising or falling edge of the TI010 pin is detected.

Figure 6-29. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Capture Register, CR010: Capture Register) (3/3)

(c) TOC00 = 13H, PRM00 = 00H, CRC00 = 07H, TMC00 = 0AH



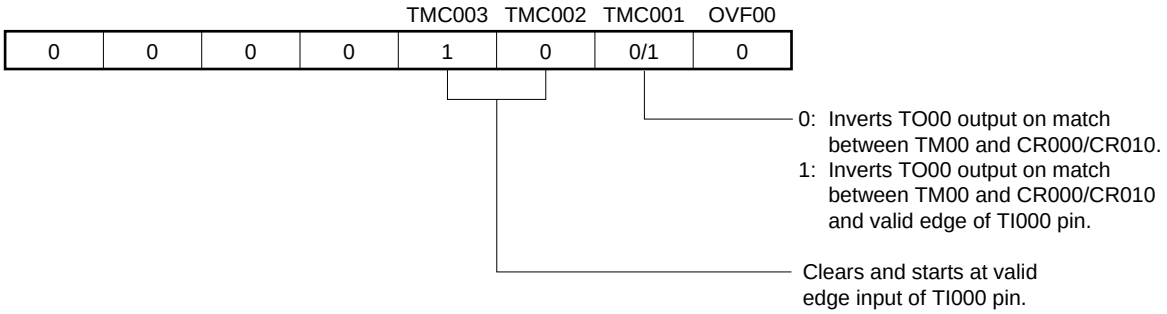
This is an application example where the pulse width of the signal input to the TI000 pin is measured.
By setting CRC00, the count value can be captured to CR000 in the phase reverse to the falling edge of the TI000 pin (i.e., rising edge) and to CR010 at the falling edge of the TI000 pin.
The high- and low-level widths of the input pulse can be calculated by the following expressions.

- High-level width = [CR010 value] – [CR000 value] × [Count clock cycle]
- Low-level width = [CR000 value] × [Count clock cycle]

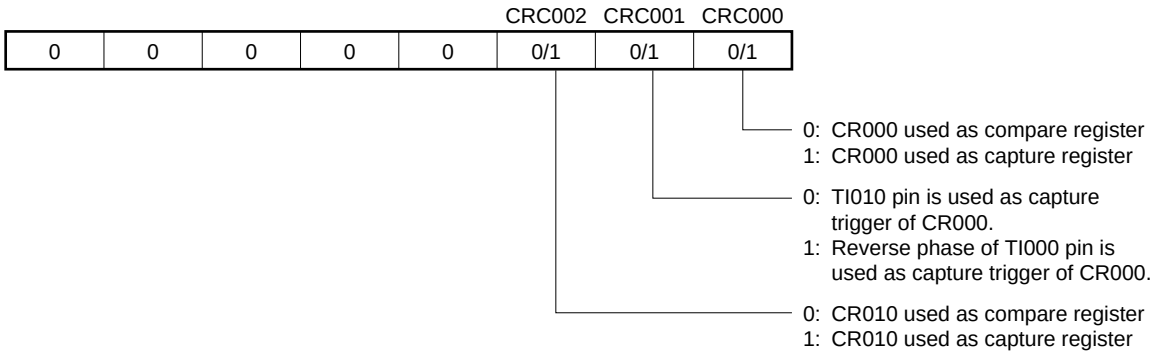
If the reverse phase of the TI000 pin is selected as a trigger to capture the count value to CR000, the INTTM000 signal is not generated. Read the values of CR000 and CR010 to measure the pulse width immediately after the INTTM010 signal is generated.
However, if the valid edge specified by bits 6 and 5 (ES110 and ES100) of prescaler mode register 00 (PRM00) is input to the TI010 pin, the count value is not captured but the INTTM000 signal is generated. To measure the pulse width of the TI000 pin, mask the INTTM000 signal when it is not used.

Figure 6-30. Example of Register Settings in Clear & Start Mode Entered by TI000 Pin Valid Edge Input (1/2)

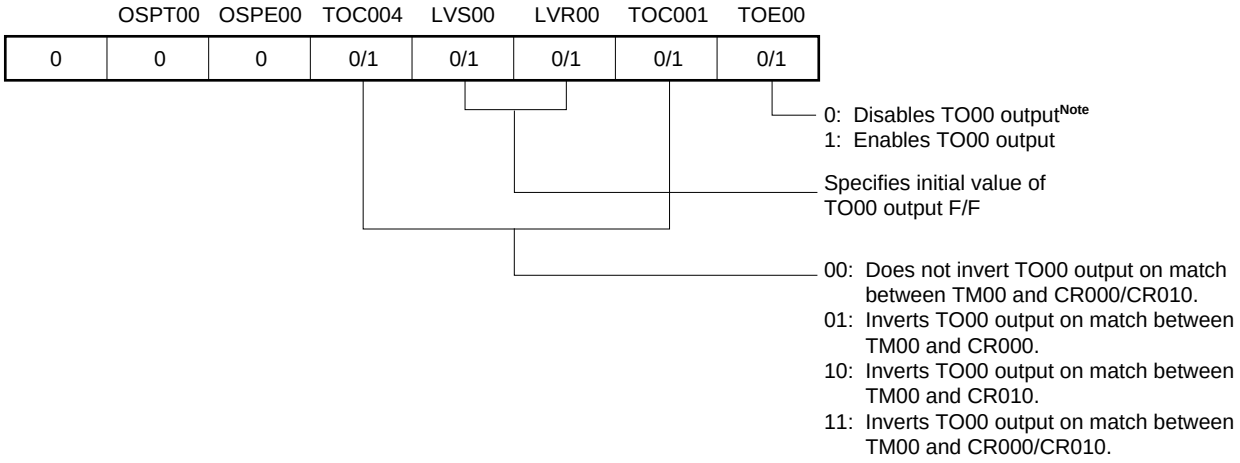
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



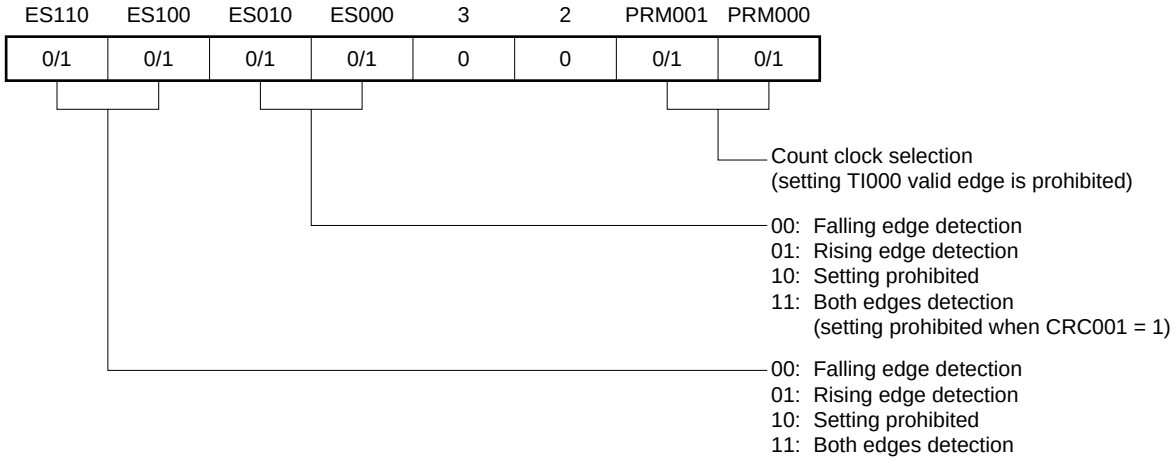
(c) 16-bit timer output control register 00 (TOC00)



Note The timer output (TO00) cannot be used when detecting the valid edge of the TI010 pin is used.

Figure 6-30. Example of Register Settings in Clear & Start Mode Entered by TI000 Pin Valid Edge Input (2/2)

(d) Prescaler mode register 00 (PRM00)



(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM000) is generated. The count value of TM00 is not cleared.

To use this register as a capture register, select either the TI000 or TI010 pin[Note] input as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR000.

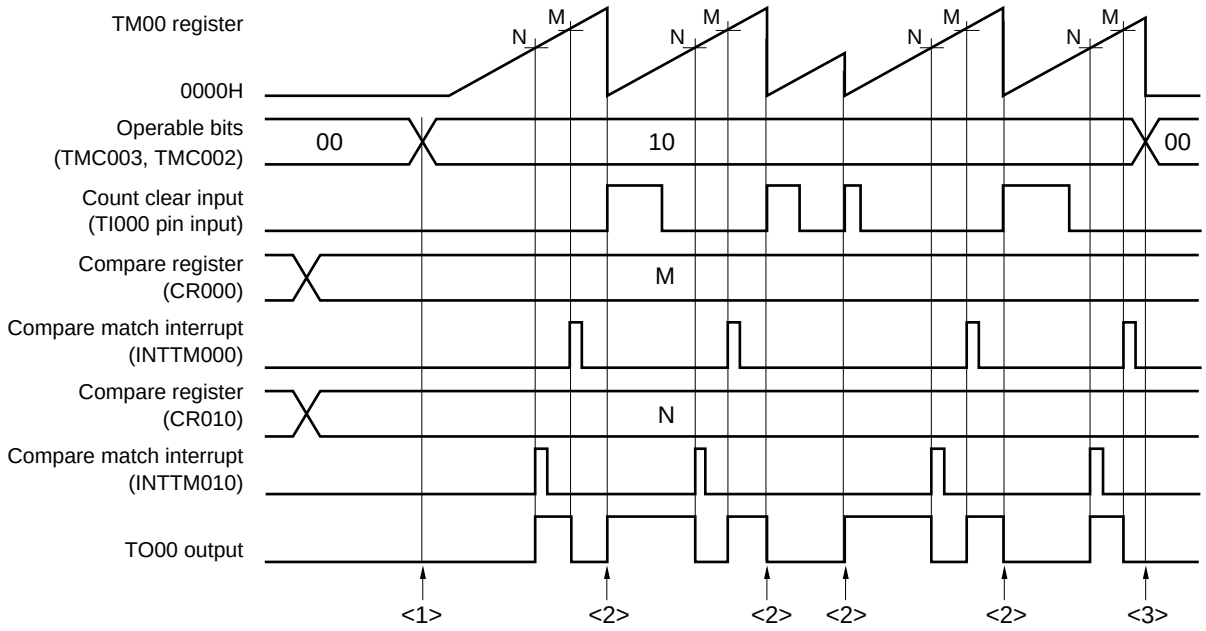
Note The timer output (TO00) cannot be used when detection of the valid edge of the TI010 pin is used.

(g) 16-bit capture/compare register 010 (CR010)

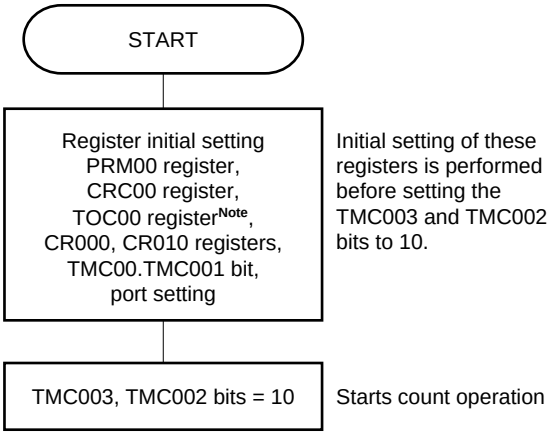
When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM010) is generated. The count value of TM00 is not cleared.

When this register is used as a capture register, the TI000 pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR010.

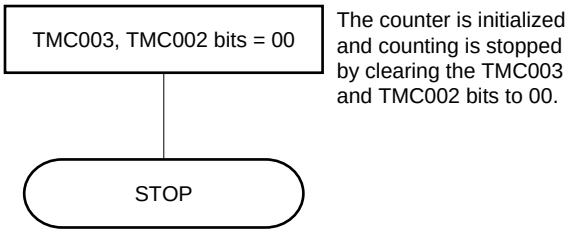
Figure 6-31. Example of Software Processing in Clear & Start Mode Entered by TI000 Pin Valid Edge Input



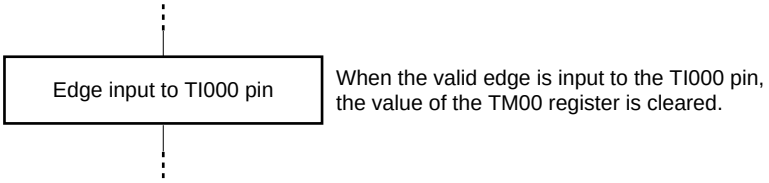
<1> Count operation start flow



<3> Count operation stop flow



<2> TM00 register clear & start flow



Note Care must be exercised when setting TOC00. For details, refer to **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

6.4.5 Free-running timer operation

When bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 01 (free-running timer mode), 16-bit timer/event counter 00 continues counting up in synchronization with the count clock. When it has counted up to FFFFH, the overflow flag (OVF00) is set to 1 at the next clock, and TM00 is cleared (to 0000H) and continues counting. Clear OVF00 to 0 by executing the CLR instruction via software.

The following three types of free-running timer operations are available.

- Both CR000 and CR010 are used as compare registers.
- One of CR000 or CR010 is used as a compare register and the other is used as a capture register.
- Both CR000 and CR010 are used as capture registers.

Remarks 1. For the setting of the I/O pins, refer to **6.3 (5) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

(1) Free-running timer mode operation

(CR000: compare register, CR010: compare register)

Figure 6-32. Block Diagram of Free-Running Timer Mode
(CR000: Compare Register, CR010: Compare Register)

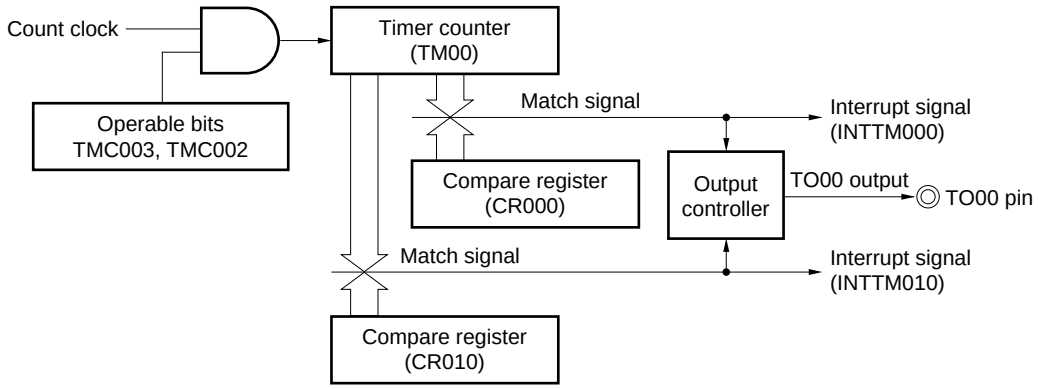
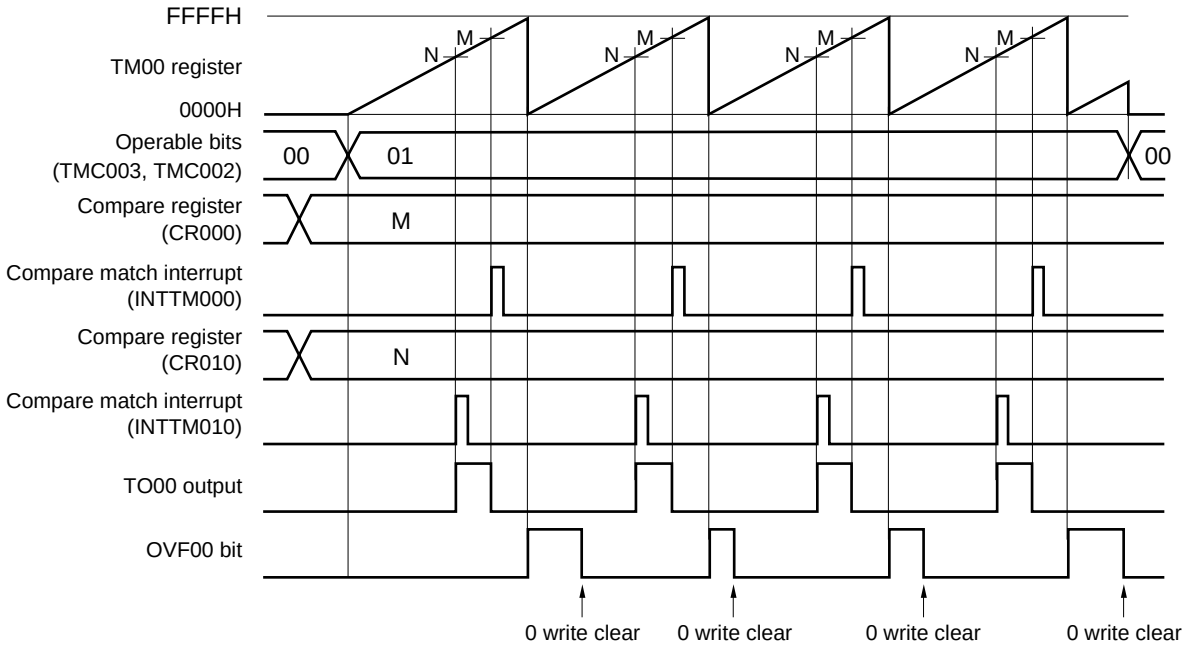


Figure 6-33. Timing Example of Free-Running Timer Mode
(CR000: Compare Register, CR010: Compare Register)

• TOC00 = 13H, PRM00 = 00H, CRC00 = 00H, TMC00 = 04H



This is an application example where two compare registers are used in the free-running timer mode.

The TO00 output level is reversed each time the count value of TM00 matches the set value of CR000 or CR010. When the count value matches the register value, the INTTM000 or INTTM010 signal is generated.

(2) Free-running timer mode operation
(CR000: compare register, CR010: capture register)

Figure 6-34. Block Diagram of Free-Running Timer Mode
(CR000: Compare Register, CR010: Capture Register)

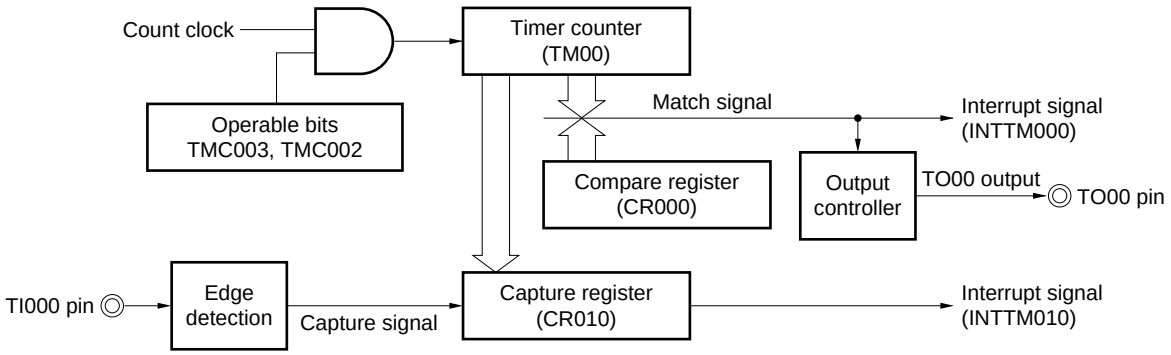
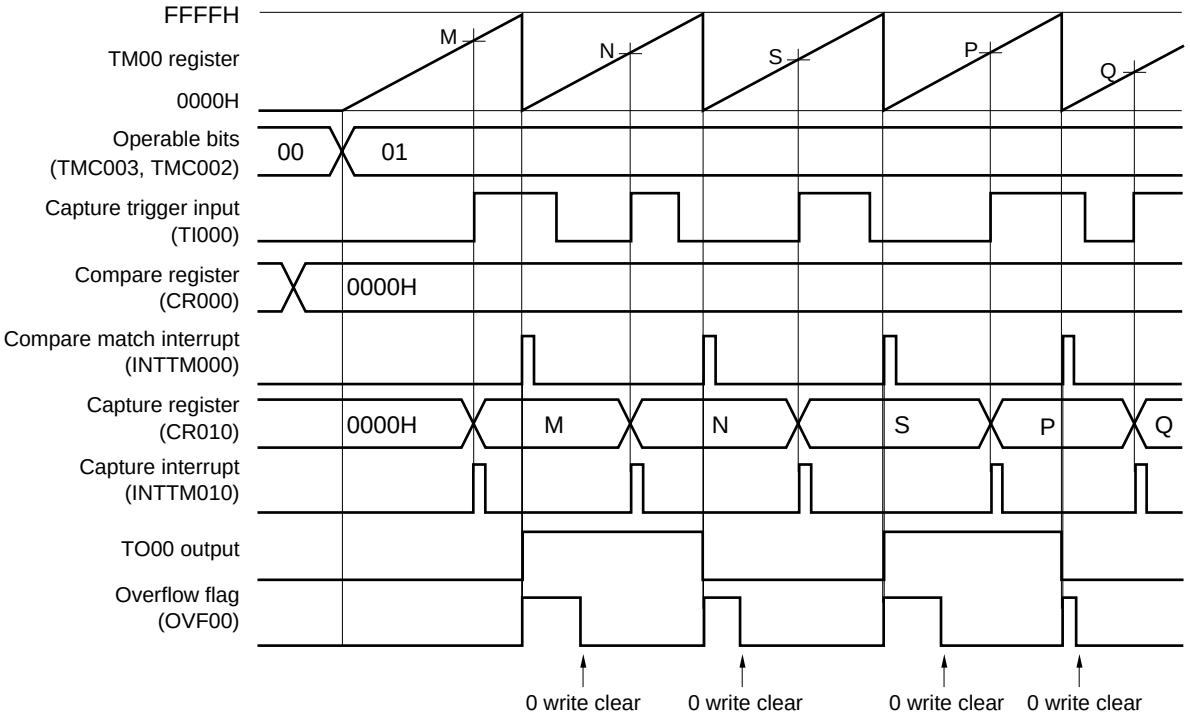


Figure 6-35. Timing Example of Free-Running Timer Mode
(CR000: Compare Register, CR010: Capture Register)

• TOC00 = 13H, PRM00 = 10H, CRC00 = 04H, TMC00 = 04H



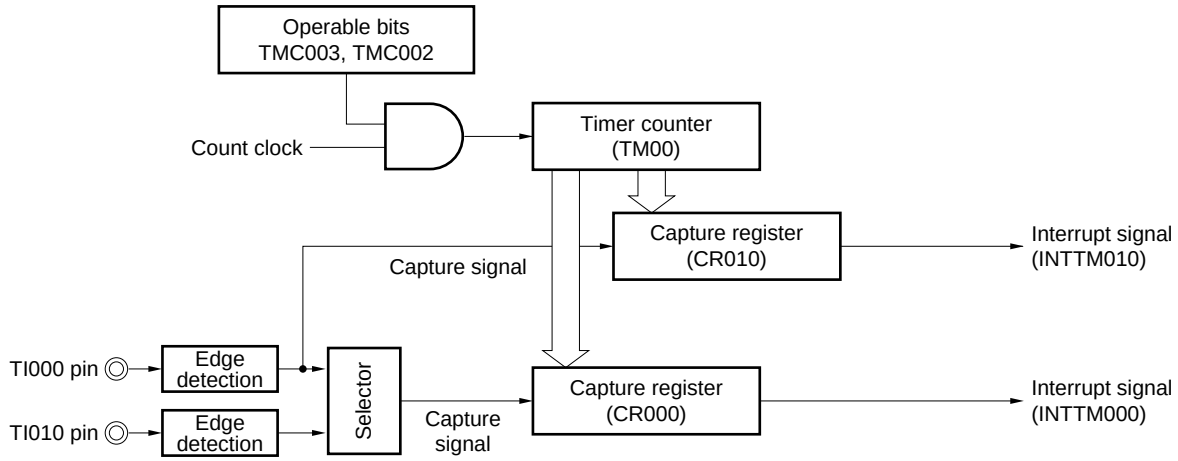
This is an application example where a compare register and a capture register are used at the same time in the free-running timer mode.

In this example, the INTTM000 signal is generated and the TO00 output level is reversed each time the count value of TM00 matches the set value of CR000 (compare register). In addition, the INTTM010 signal is generated and the count value of TM00 is captured to CR010 each time the valid edge of the TI000 pin is detected.

(3) Free-running timer mode operation

(CR000: capture register, CR010: capture register)

Figure 6-36. Block Diagram of Free-Running Timer Mode
(CR000: Capture Register, CR010: Capture Register)

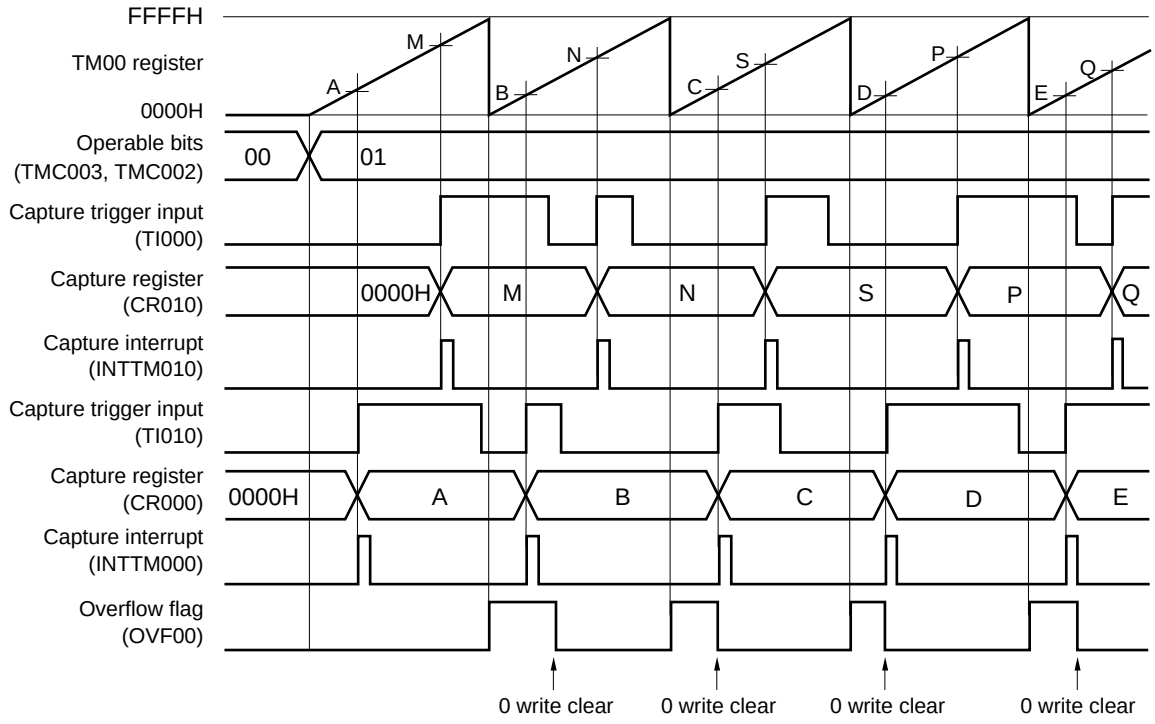


Remark If both CR000 and CR010 are used as capture registers in the free-running timer mode, the TO00 output level is not inverted.

However, it can be inverted each time the valid edge of the TI000 pin is detected if bit 1 (TMC001) of 16-bit timer mode control register 00 (TMC00) is set to 1.

Figure 6-37. Timing Example of Free-Running Timer Mode
(CR000: Capture Register, CR010: Capture Register) (1/2)

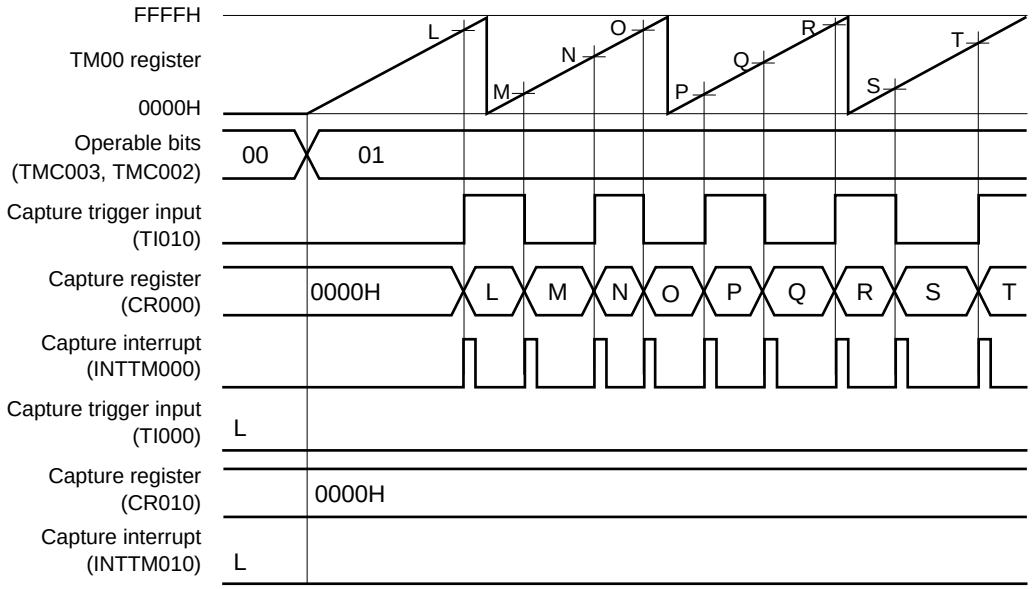
(a) TOC00 = 13H, PRM00 = 50H, CRC00 = 05H, TMC00 = 04H



This is an application example where the count values that have been captured at the valid edges of separate capture trigger signals are stored in separate capture registers in the free-running timer mode.
The count value is captured to CR010 when the valid edge of the TI000 pin input is detected and to CR000 when the valid edge of the TI010 pin input is detected.

Figure 6-37. Timing Example of Free-Running Timer Mode
(CR000: Capture Register, CR010: Capture Register) (2/2)

(b) TOC00 = 13H, PRM00 = C0H, CRC00 = 05H, TMC00 = 04H

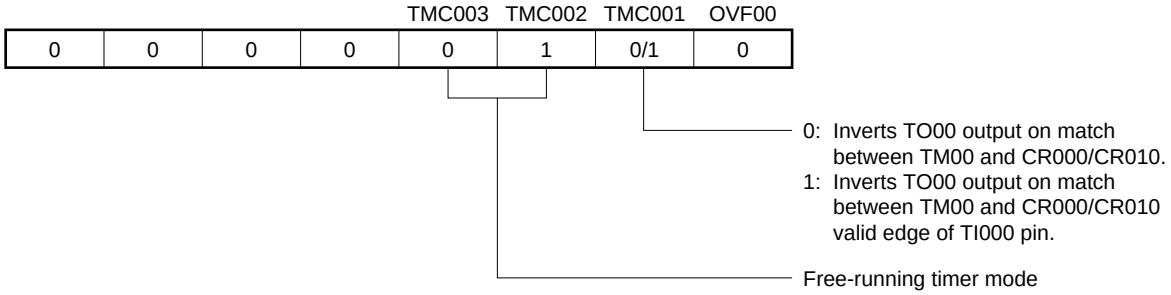


This is an application example where both the edges of the TI010 pin are detected and the count value is captured to CR000 in the free-running timer mode.

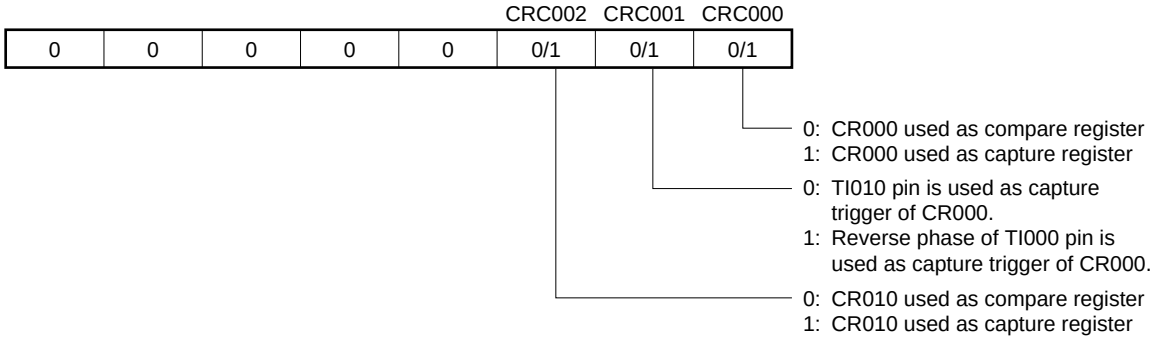
When both CR000 and CR010 are used as capture registers and when the valid edge of only the TI010 pin is to be detected, the count value cannot be captured to CR010.

Figure 6-38. Example of Register Settings in Free-Running Timer Mode (1/2)

(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)

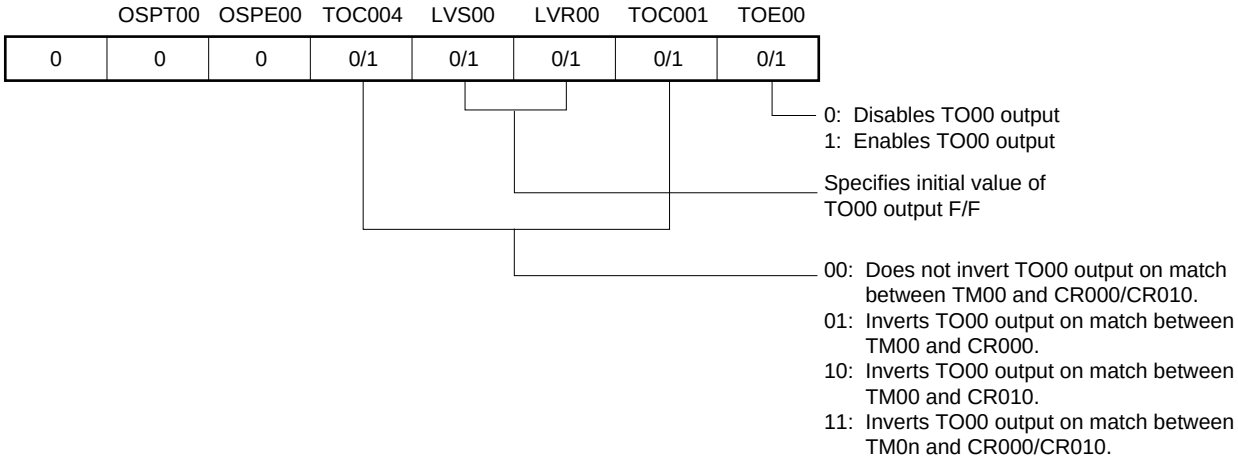
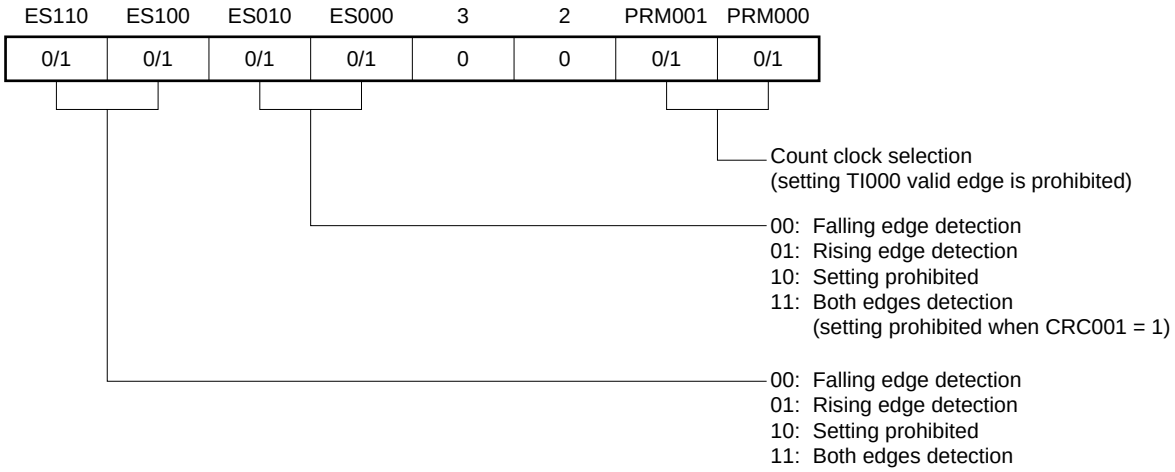


Figure 6-38. Example of Register Settings in Free-Running Timer Mode (2/2)

(d) Prescaler mode register 00 (PRM00)



(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM000) is generated. The count value of TM00 is not cleared.

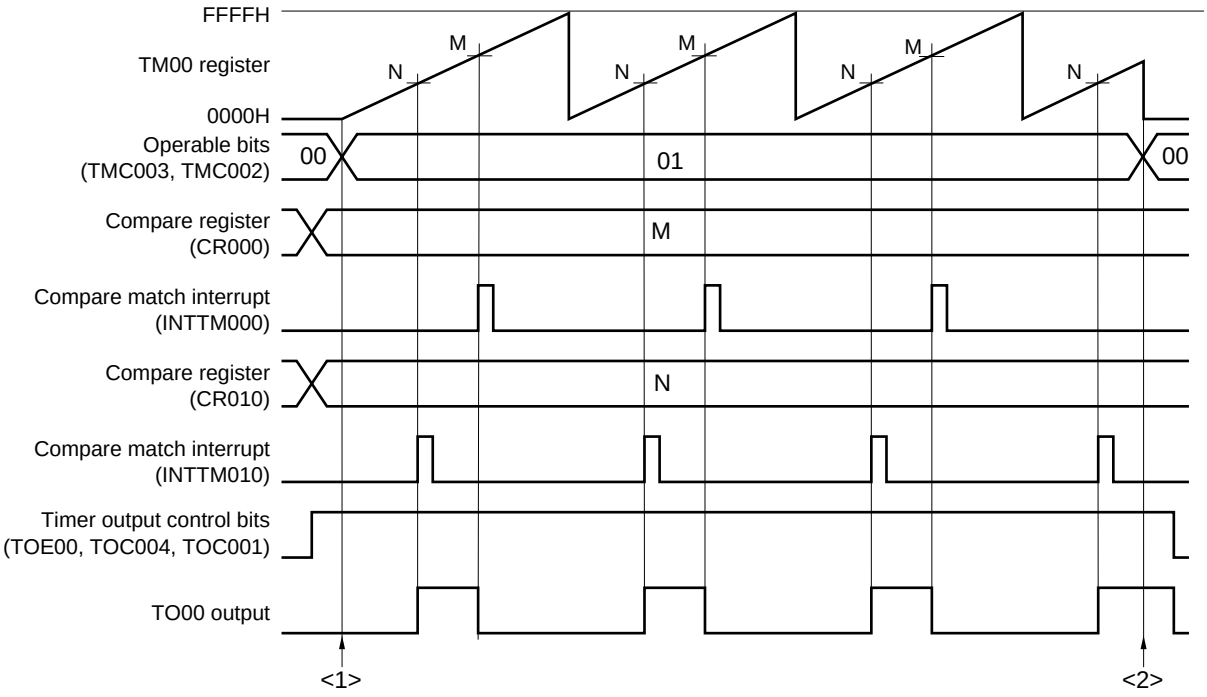
To use this register as a capture register, select either the TI000 or TI010 pin input as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR000.

(g) 16-bit capture/compare register 010 (CR010)

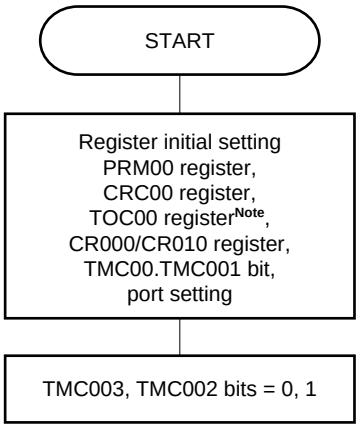
When this register is used as a compare register and when its value matches the count value of TM00, an interrupt signal (INTTM010) is generated. The count value of TM00 is not cleared.

When this register is used as a capture register, the TI000 pin input is used as a capture trigger. When the valid edge of the capture trigger is detected, the count value of TM00 is stored in CR010.

Figure 6-39. Example of Software Processing in Free-Running Timer Mode



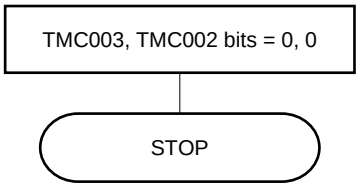
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 01.

Starts count operation

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

Note Care must be exercised when setting TOC00. For details, refer to **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

6.4.6 PPG output operation

A square wave having a pulse width set in advance by CR010 is output from the TO00 pin as a PPG (Programmable Pulse Generator) signal during a cycle set by CR000 when bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 11 (clear & start upon a match between TM00 and CR000).

The pulse cycle and duty factor of the pulse generated as the PPG output are as follows.

- Pulse cycle = (Set value of CR000 + 1) × Count clock cycle
- Duty = (Set value of CR010 + 1) / (Set value of CR000 + 1)

Caution To change the duty factor (value of CR010) during operation, refer to 6.5.1 Rewriting CR010 during TM00 operation.

Remarks 1. For the setting of I/O pins, refer to **6.3 (5) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, refer to **CHAPTER 17 INTERRUPT FUNCTIONS**.

Figure 6-40. Block Diagram of PPG Output Operation

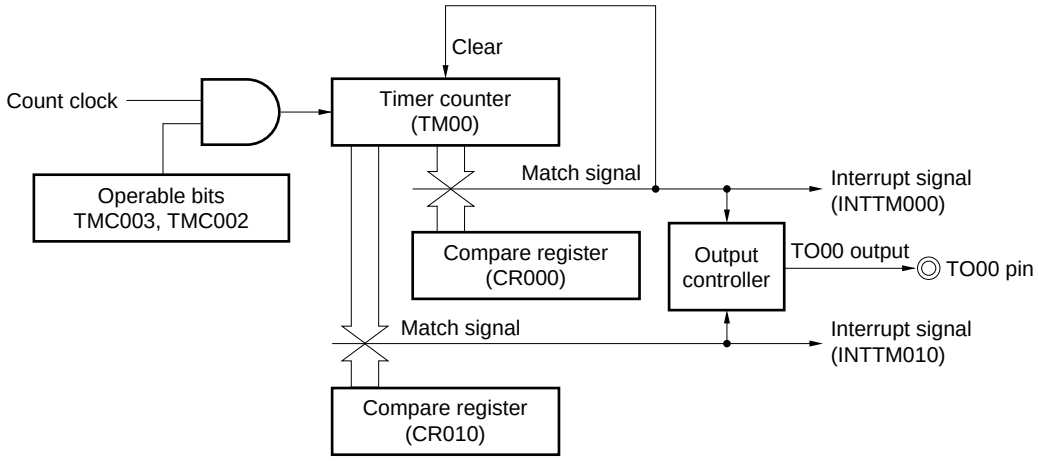
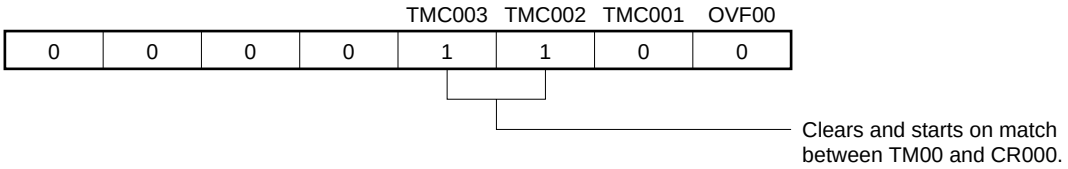
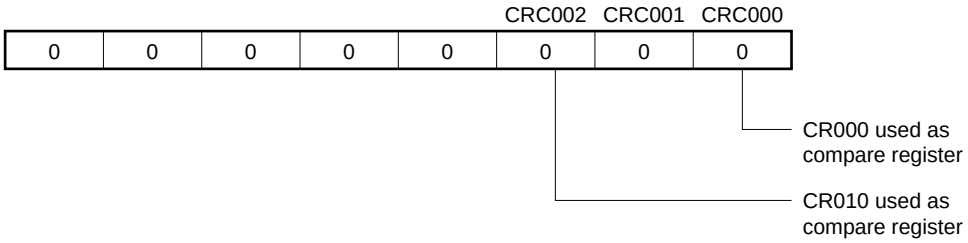


Figure 6-41. Example of Register Settings for PPG Output Operation (1/2)

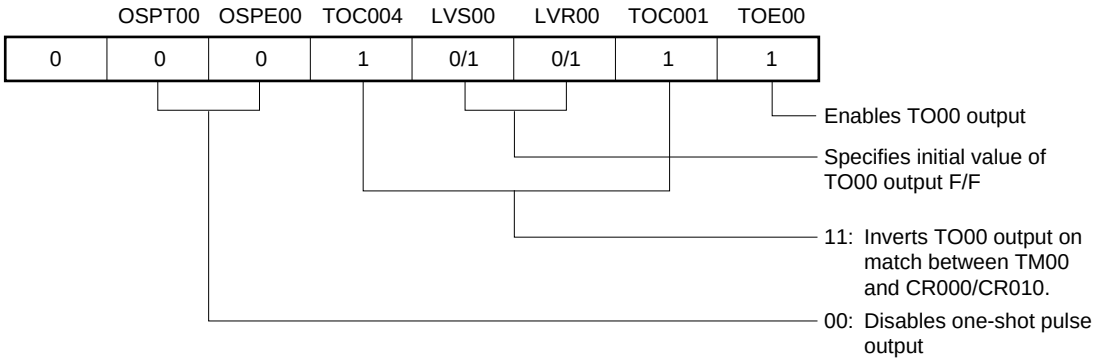
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



(d) Prescaler mode register 00 (PRM00)

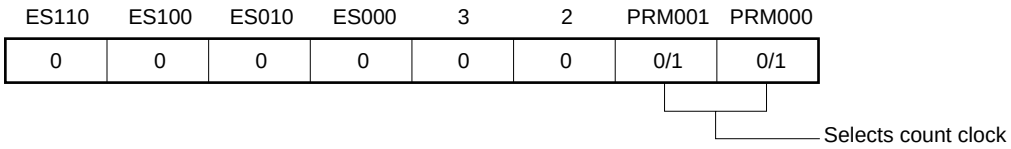


Figure 6-41. Example of Register Settings for PPG Output Operation (2/2)

(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

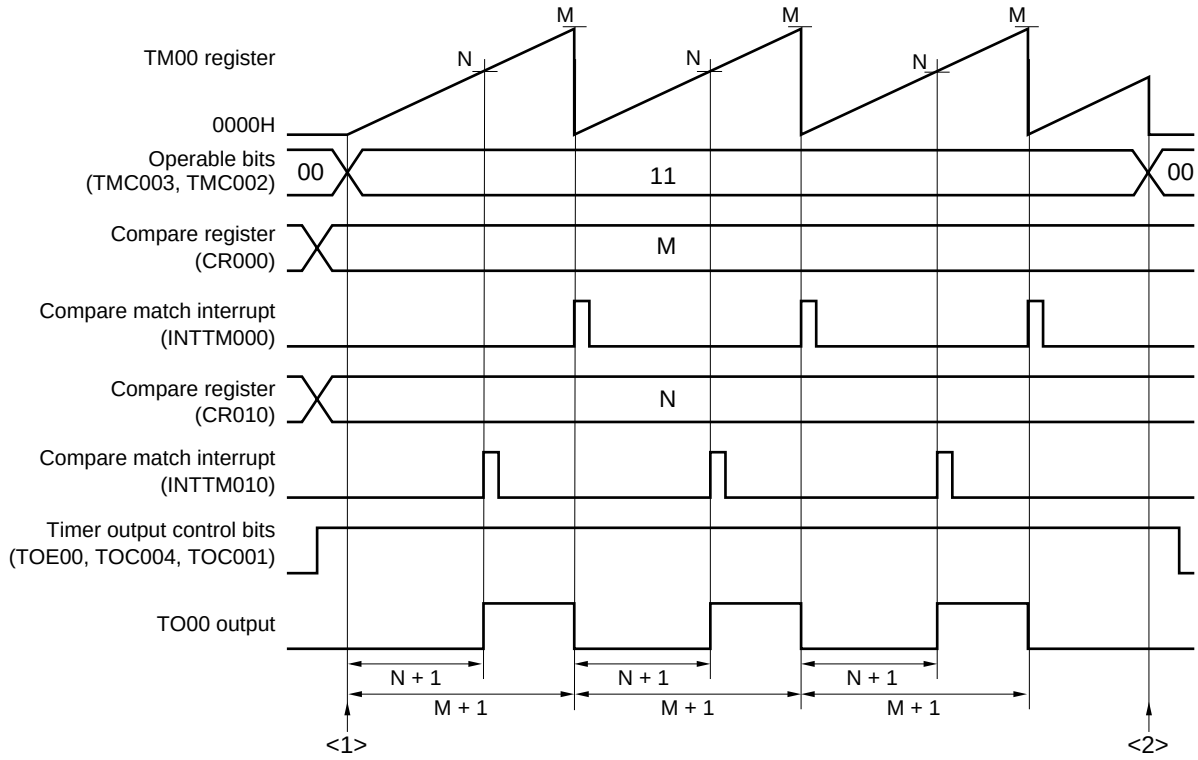
An interrupt signal (INTTM000) is generated when the value of this register matches the count value of TM00. The count value of TM00 is cleared.

(g) 16-bit capture/compare register 010 (CR010)

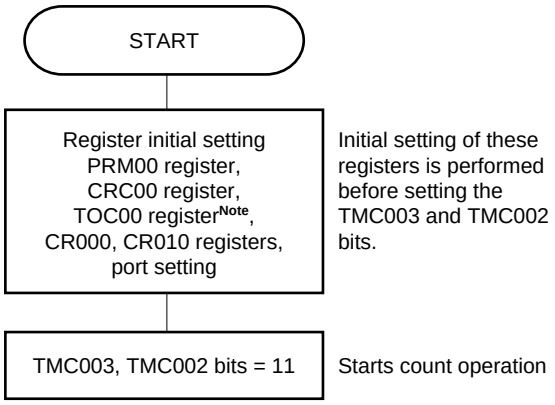
An interrupt signal (INTTM010) is generated when the value of this register matches the count value of TM00. The count value of TM00 is not cleared.

Caution Set values to CR000 and CR010 such that the condition 0000H ≤ CR010 < CR000 ≤ FFFFH is satisfied.

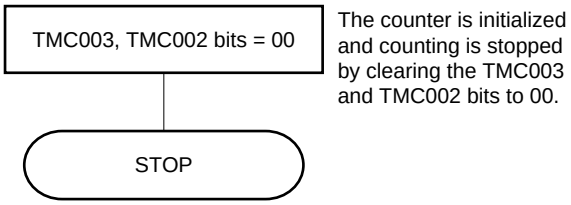
Figure 6-42. Example of Software Processing for PPG Output Operation



<1> Count operation start flow



<2> Count operation stop flow



Note Care must be exercised when setting TOC00. For details, refer to **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

Remark PPG pulse cycle = (M + 1) × Count clock cycle
PPG duty = (N + 1)/(M + 1)

6.4.7 One-shot pulse output operation

A one-shot pulse can be output by setting bits 3 and 2 (TMC003 and TMC002) of the 16-bit timer mode control register 00 (TMC00) to 01 (free-running timer mode) or to 10 (clear & start mode entered by the TI000 pin valid edge) and setting bit 5 (OSPE00) of 16-bit timer output control register 00 (TOC00) to 1.

When bit 6 (OSPT00) of TOC00 is set to 1 or when the valid edge is input to the TI000 pin during timer operation, clearing & starting of TM00 is triggered, and a pulse of the difference between the values of CR000 and CR010 is output only once from the TO00 pin.

Cautions 1. Do not input the trigger again (setting OSPT00 to 1 or detecting the valid edge of the TI000 pin) while the one-shot pulse is output. To output the one-shot pulse again, generate the trigger after the current one-shot pulse output has completed.

2. To use only the setting of OSPT00 to 1 as the trigger of one-shot pulse output, do not change the level of the TI000 pin or its alternate function port pin. Otherwise, the pulse will be unexpectedly output.

Remarks 1. For the setting of the I/O pins, refer to **6.3 (5) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

Figure 6-43. Block Diagram of One-Shot Pulse Output Operation

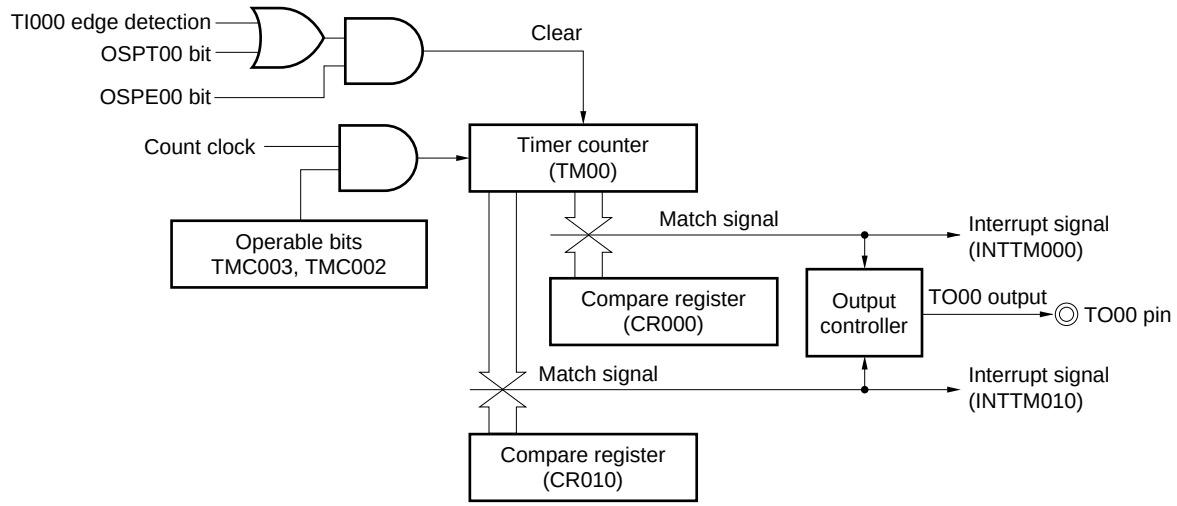
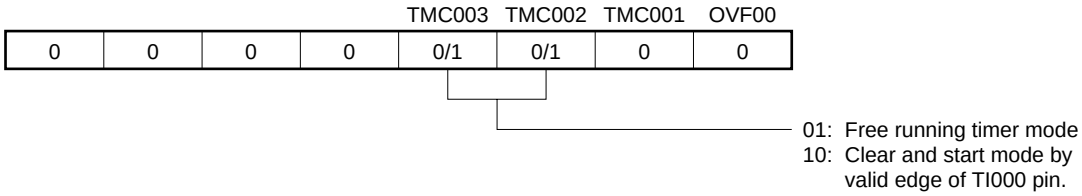
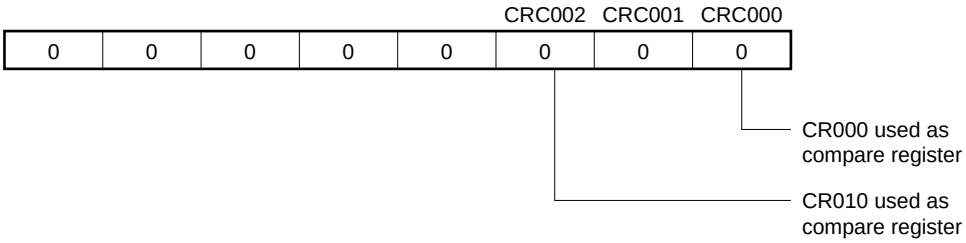


Figure 6-44. Example of Register Settings for One-Shot Pulse Output Operation (1/2)

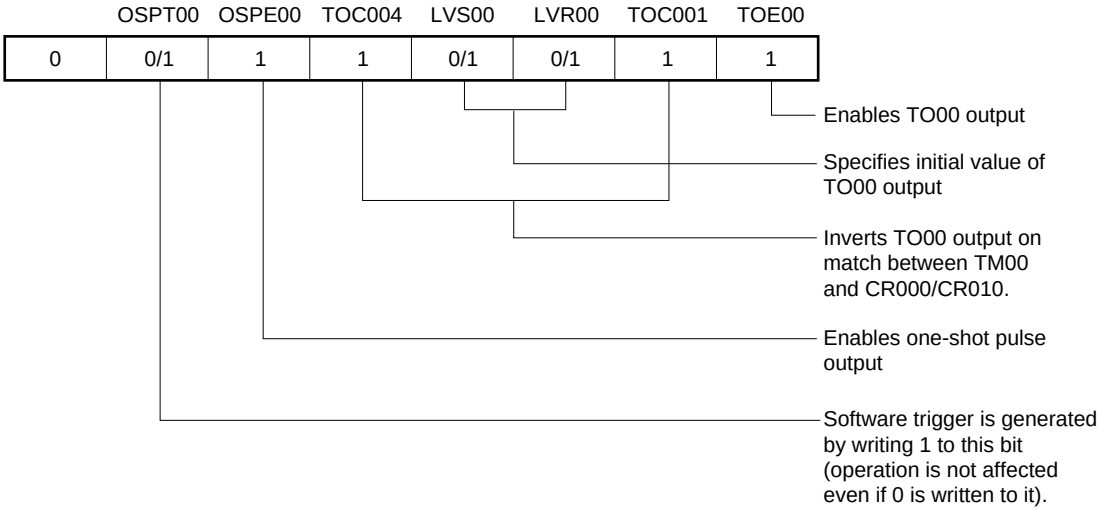
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



(d) Prescaler mode register 00 (PRM00)

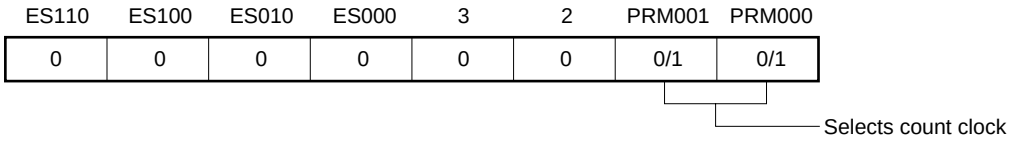


Figure 6-44. Example of Register Settings for One-Shot Pulse Output Operation (2/2)

(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

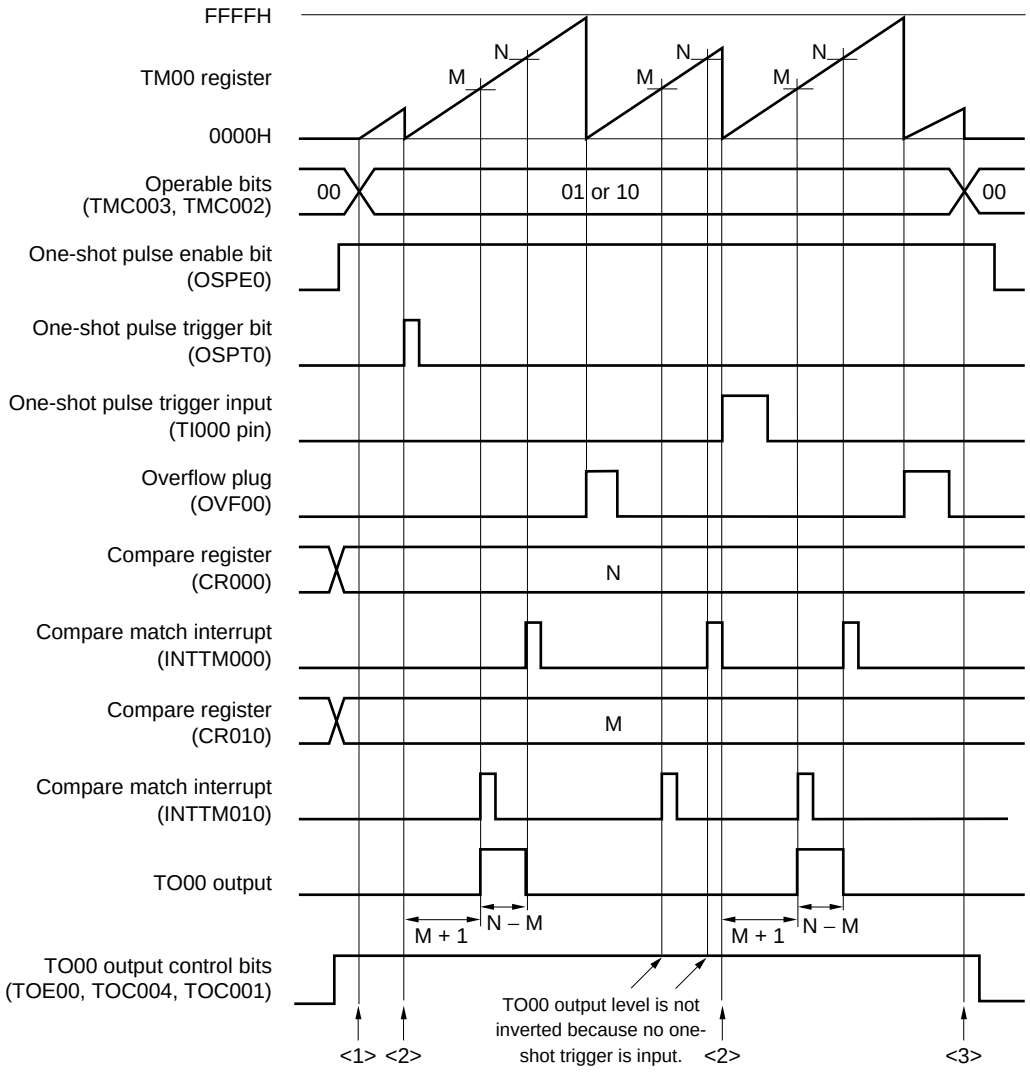
This register is used as a compare register when a one-shot pulse is output. When the value of TM00 matches that of CR000, an interrupt signal (INTTM000) is generated and the TO00 output level is inverted.

(g) 16-bit capture/compare register 010 (CR010)

This register is used as a compare register when a one-shot pulse is output. When the value of TM00 matches that of CR010, an interrupt signal (INTTM010) is generated and the TO00 output level is inverted.

Caution Do not set the same value to CR000 and CR010.

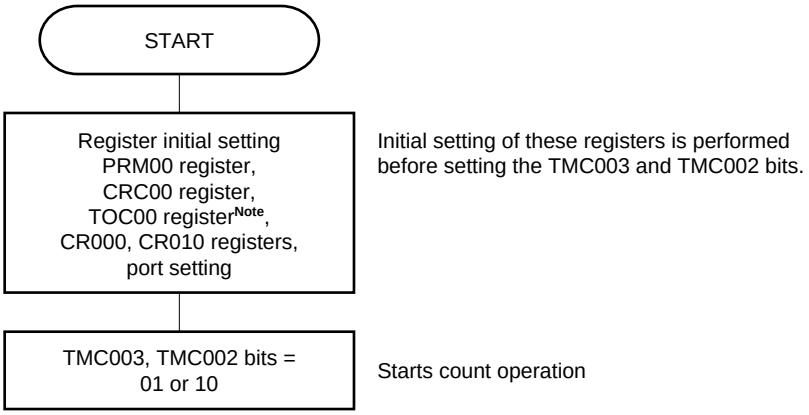
Figure 6-45. Example of Software Processing for One-Shot Pulse Output Operation (1/2)



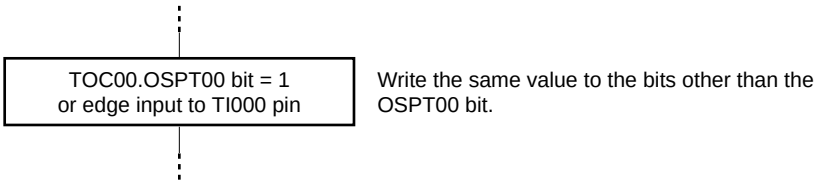
- Time from when the one-shot pulse trigger is input until the one-shot pulse is output
  = (M + 1) × Count clock cycle
- One-shot pulse output active level width
  = (N − M) × Count clock cycle

Figure 6-45. Example of Software Processing for One-Shot Pulse Output Operation (2/2)

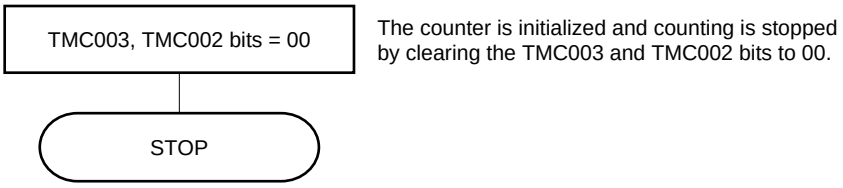
<1> Count operation start flow



<2> One-shot trigger input flow



<3> Count operation stop flow



Note Care must be exercised when setting TOC00. For details, refer to **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

6.4.8 Pulse width measurement operation

TM00 can be used to measure the pulse width of the signal input to the TI000 and TI010 pins.

Measurement can be accomplished by operating the 16-bit timer/event counter 00 in the free-running timer mode or by restarting the timer in synchronization with the signal input to the TI000 pin.

When an interrupt is generated, read the value of the valid capture register and measure the pulse width. Check bit 0 (OVF00) of 16-bit timer mode control register 00 (TMC00). If it is set (to 1), clear it to 0 by software.

Figure 6-46. Block Diagram of Pulse Width Measurement (Free-Running Timer Mode)

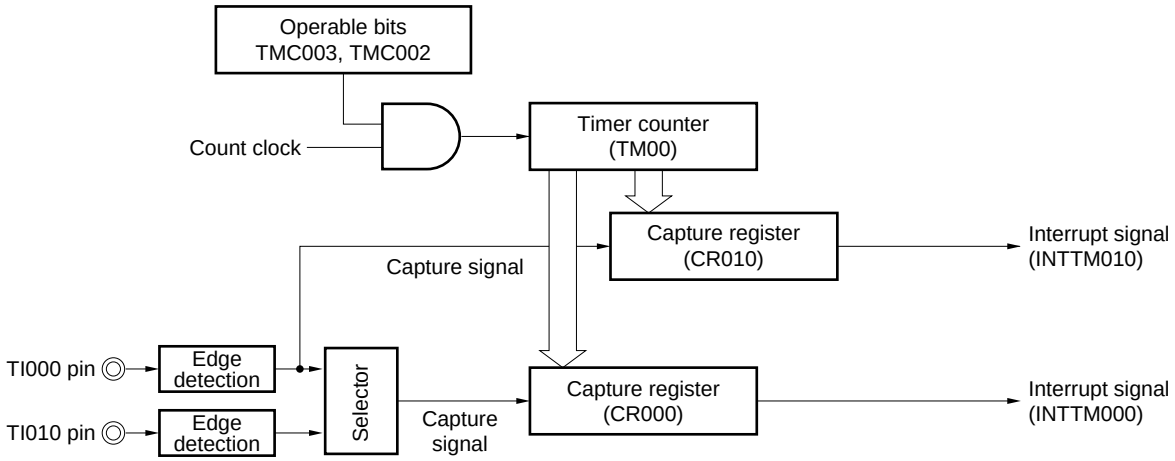
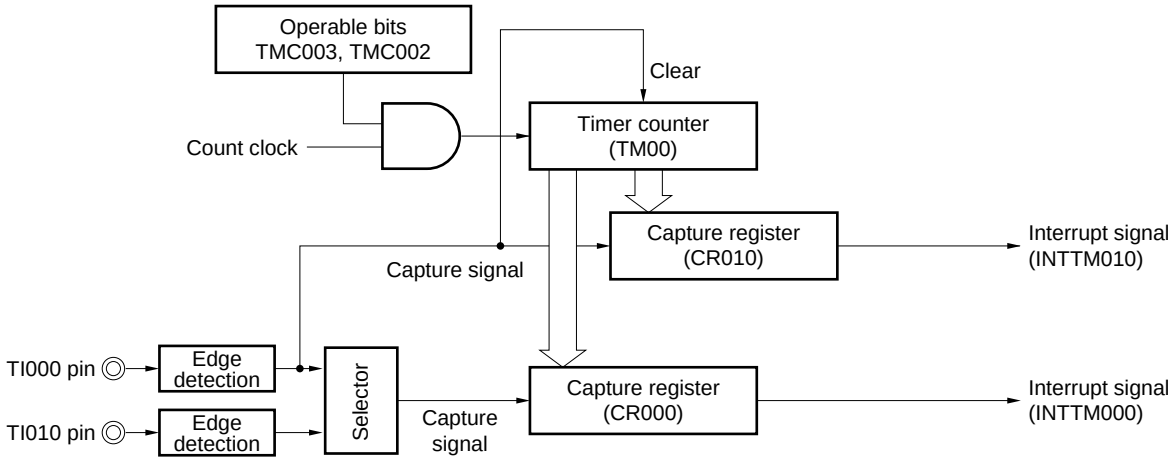


Figure 6-47. Block Diagram of Pulse Width Measurement
(Clear & Start Mode Entered by TI000 Pin Valid Edge Input)



A pulse width can be measured in the following three ways.

- Measuring the pulse width by using two input signals of the TI000 and TI010 pins (free-running timer mode)
- Measuring the pulse width by using one input signal of the TI000 pin (free-running timer mode)
- Measuring the pulse width by using one input signal of the TI000 pin (clear & start mode entered by the TI000 pin valid edge input)

Remarks 1. For the setting of the I/O pins, refer to **6.3 (5) Port mode register 3 (PM3)**.

2. For how to enable the INTTM000 signal interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

(1) Measuring the pulse width by using two input signals of the TI000 and TI010 pins (free-running timer mode)

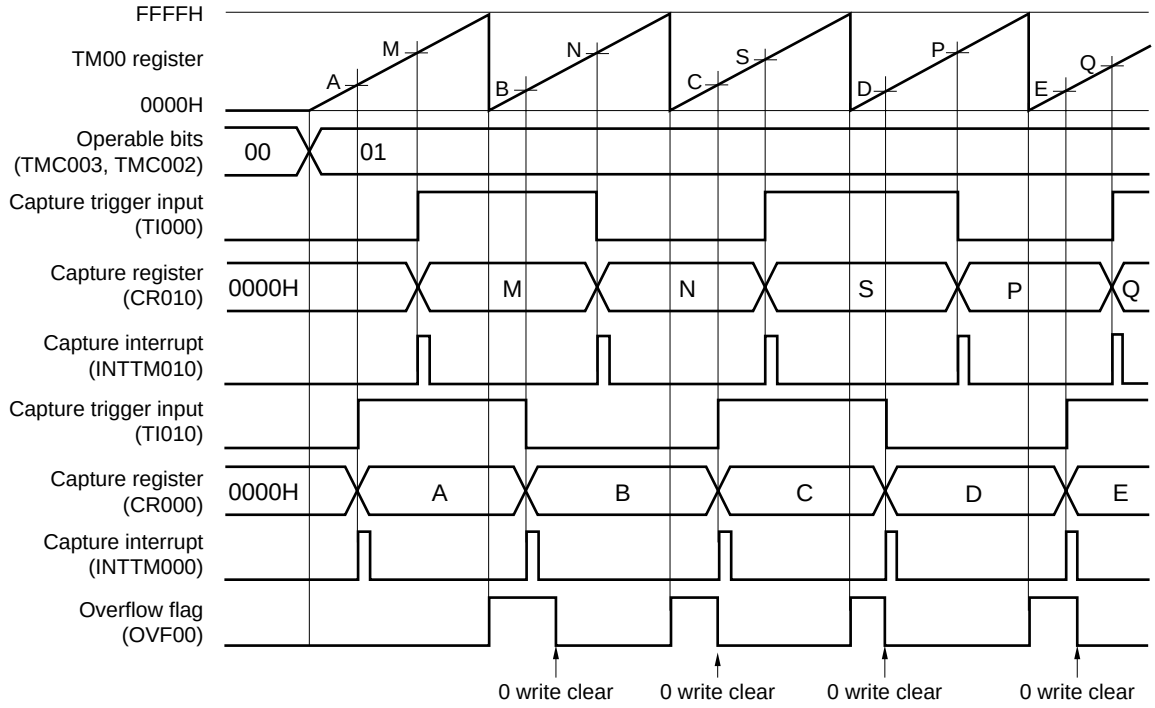
Set the free-running timer mode (TMC003 and TMC002 = 01). When the valid edge of the TI000 pin is detected, the count value of TM00 is captured to CR010. When the valid edge of the TI010 pin is detected, the count value of TM00 is captured to CR000. Specify detection of both the edges of the TI000 and TI010 pins.

By this measurement method, the previous count value is subtracted from the count value captured by the edge of each input signal. Therefore, save the previously captured value to a separate register in advance.

If an overflow occurs, the value becomes negative if the previously captured value is simply subtracted from the current captured value and, therefore, a borrow occurs (bit 0 (CY) of the program status word (PSW) is set to 1). If this happens, ignore CY and take the calculated value as the pulse width. In addition, clear bit 0 (OVF00) of 16-bit timer mode control register 00 (TMC00) to 0.

Figure 6-48. Timing Example of Pulse Width Measurement (1)

• TMC00 = 04H, PRM00 = F0H, CRC00 = 05H



(2) Measuring the pulse width by using one input signal of the TI000 pin (free-running timer mode)

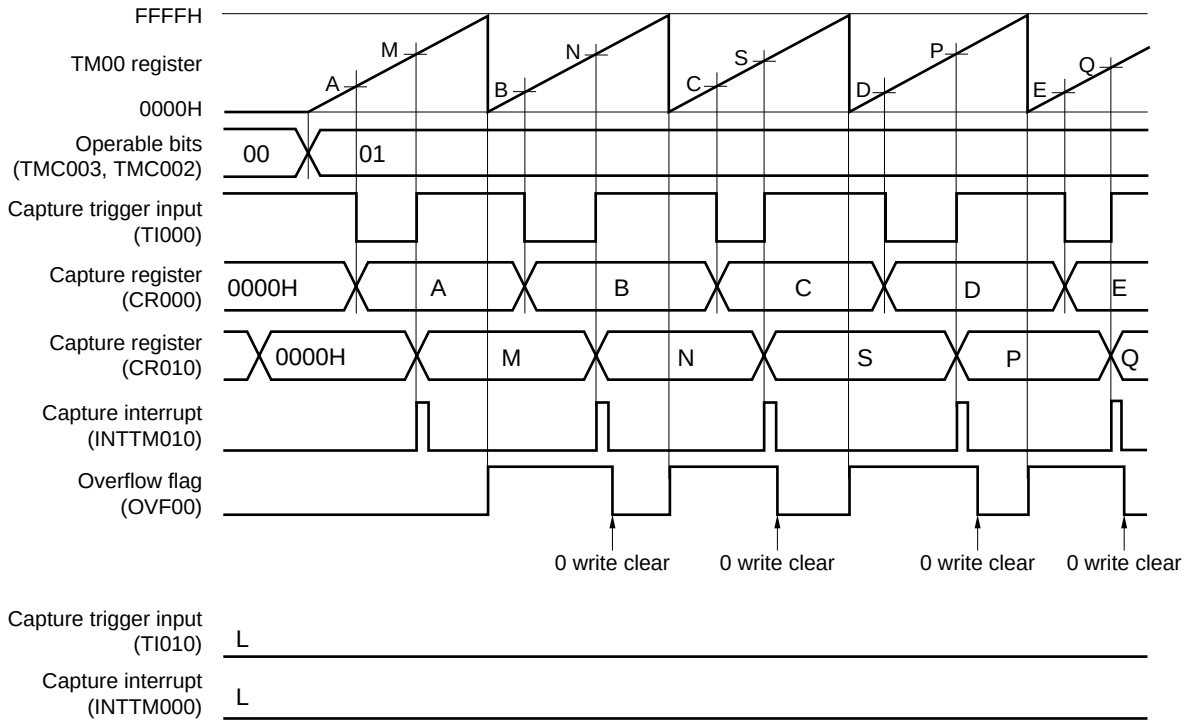
Set the free-running timer mode (TMC003 and TMC002 = 01). The count value of TM00 is captured to CR000 in the phase reverse to the valid edge detected on the TI000 pin. When the valid edge of the TI000 pin is detected, the count value of TM00 is captured to CR010.

By this measurement method, values are stored in separate capture registers when a width from one edge to another is measured. Therefore, the capture values do not have to be saved. By subtracting the value of one capture register from that of another, a high-level width, low-level width, and cycle are calculated.

If an overflow occurs, the value becomes negative if one captured value is simply subtracted from another and, therefore, a borrow occurs (bit 0 (CY) of the program status word (PSW) is set to 1). If this happens, ignore CY and take the calculated value as the pulse width. In addition, clear bit 0 (OVF00) of 16-bit timer mode control register 00 (TMC00) to 0.

Figure 6-49. Timing Example of Pulse Width Measurement (2)

• TMC00 = 04H, PRM00 = 10H, CRC00 = 07H



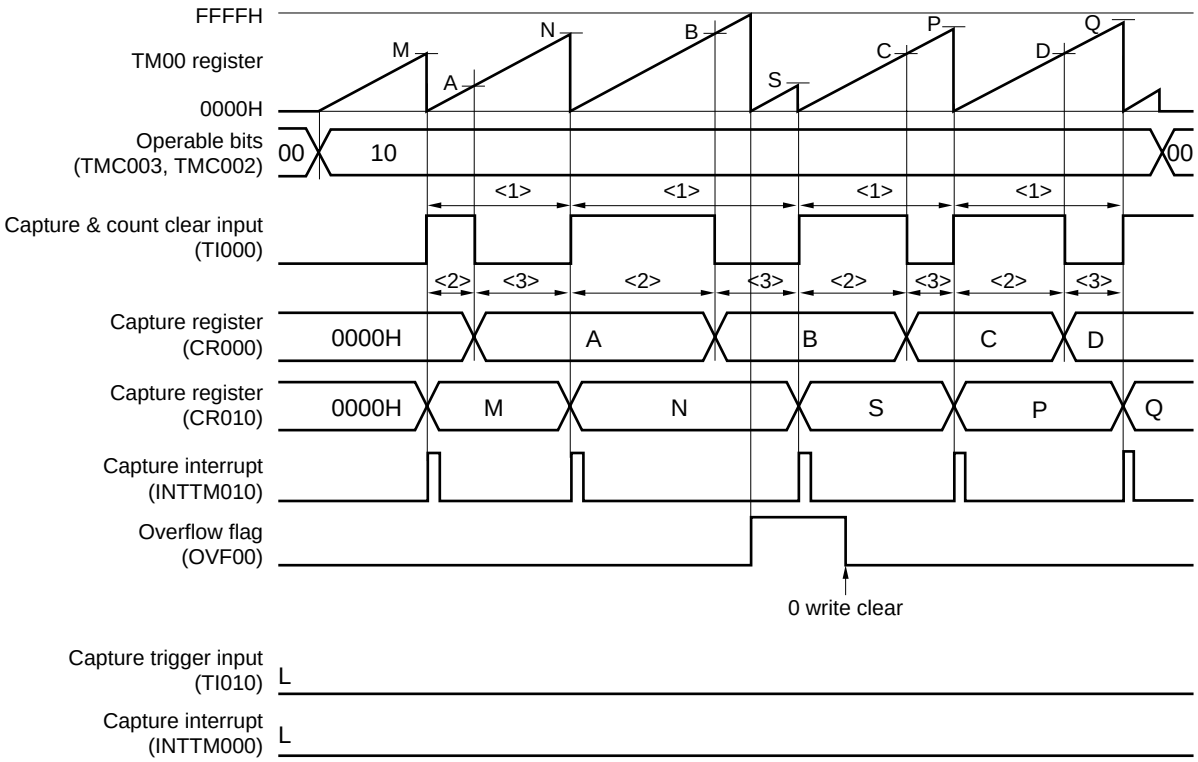
(3) Measuring the pulse width by using one input signal of the TI000 pin (clear & start mode entered by the TI000 pin valid edge input)

Set the clear & start mode entered by the TI000 pin valid edge (TMC003 and TMC002 = 10). The count value of TM00 is captured to CR000 in the phase reverse to the valid edge of the TI000 pin, and the count value of TM00 is captured to CR010 and TM00 is cleared (0000H) when the valid edge of the TI000 pin is detected. Therefore, a cycle is stored in CR010 if TM00 does not overflow.

If an overflow occurs, take the value that results from adding 10000H to the value stored in CR010 as a cycle. Clear bit 0 (OVF00) of 16-bit timer mode control register 00 (TMC00) to 0.

Figure 6-50. Timing Example of Pulse Width Measurement (3)

• TMC00 = 08H, PRM00 = 10H, CRC00 = 07H



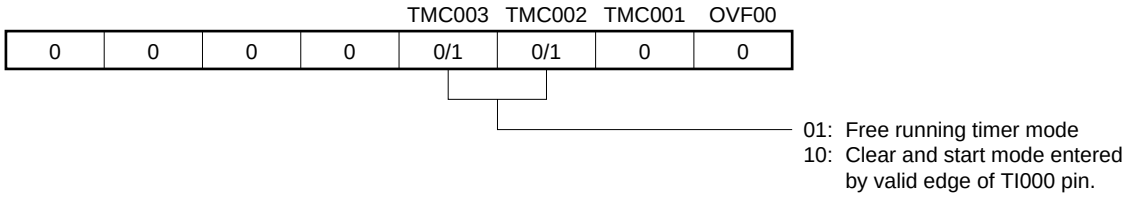
<1> Pulse cycle = (10000H × Number of times OVF00 bit is set to 1 + Captured value of CR010) × Count clock cycle

<2> High-level pulse width = (10000H × Number of times OVF00 bit is set to 1 + Captured value of CR000) × Count clock cycle

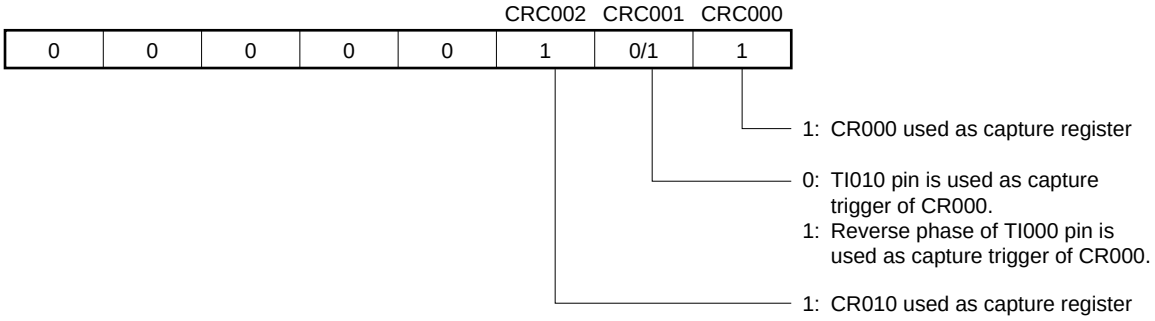
<3> Low-level pulse width = (Pulse cycle − High-level pulse width)

Figure 6-51. Example of Register Settings for Pulse Width Measurement (1/2)

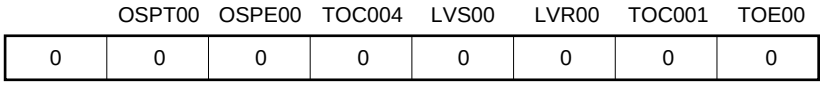
(a) 16-bit timer mode control register 00 (TMC00)



(b) Capture/compare control register 00 (CRC00)



(c) 16-bit timer output control register 00 (TOC00)



(d) Prescaler mode register 00 (PRM00)

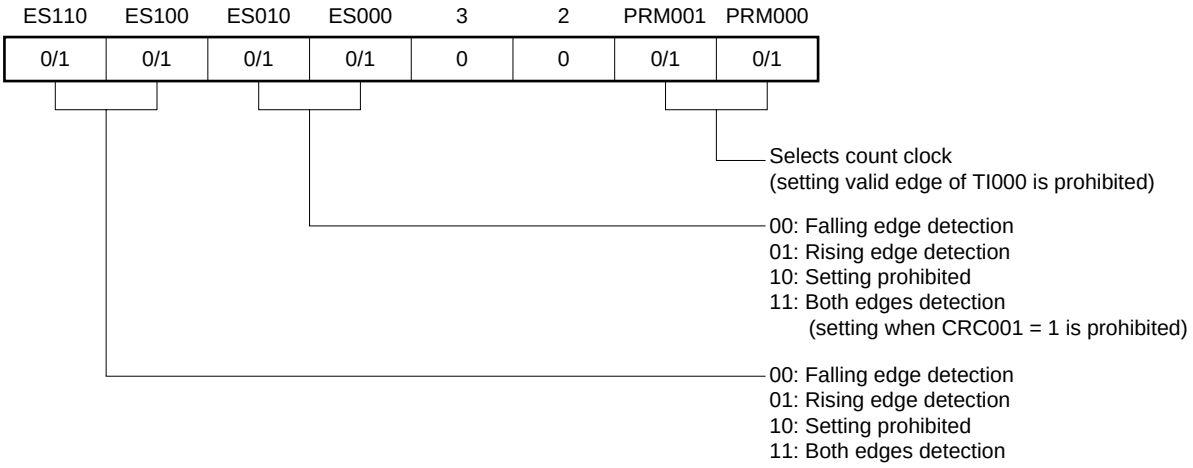


Figure 6-51. Example of Register Settings for Pulse Width Measurement (2/2)

(e) 16-bit timer counter 00 (TM00)

By reading TM00, the count value can be read.

(f) 16-bit capture/compare register 000 (CR000)

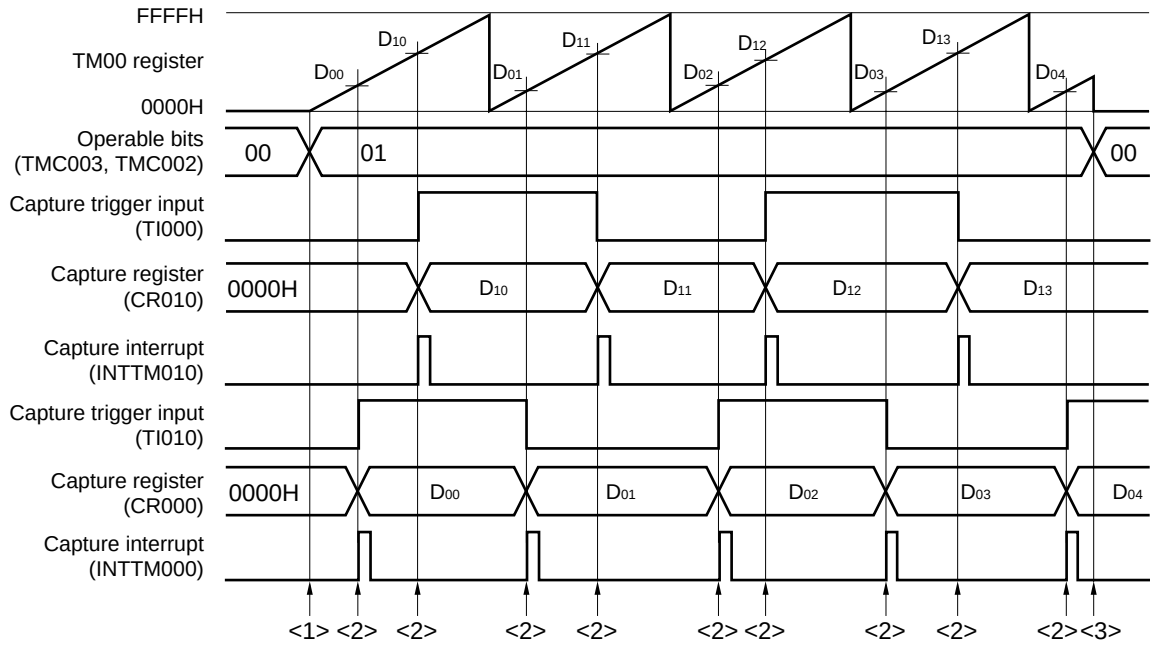
This register is used as a capture register. Either the TI000 or TI010 pin is selected as a capture trigger. When a specified edge of the capture trigger is detected, the count value of TM00 is stored in CR000.

(g) 16-bit capture/compare register 010 (CR010)

This register is used as a capture register. The signal input to the TI000 pin is used as a capture trigger. When the capture trigger is detected, the count value of TM00 is stored in CR010.

Figure 6-52. Example of Software Processing for Pulse Width Measurement (1/2)

(a) Example of free-running timer mode



(b) Example of clear & start mode entered by TI000 pin valid edge

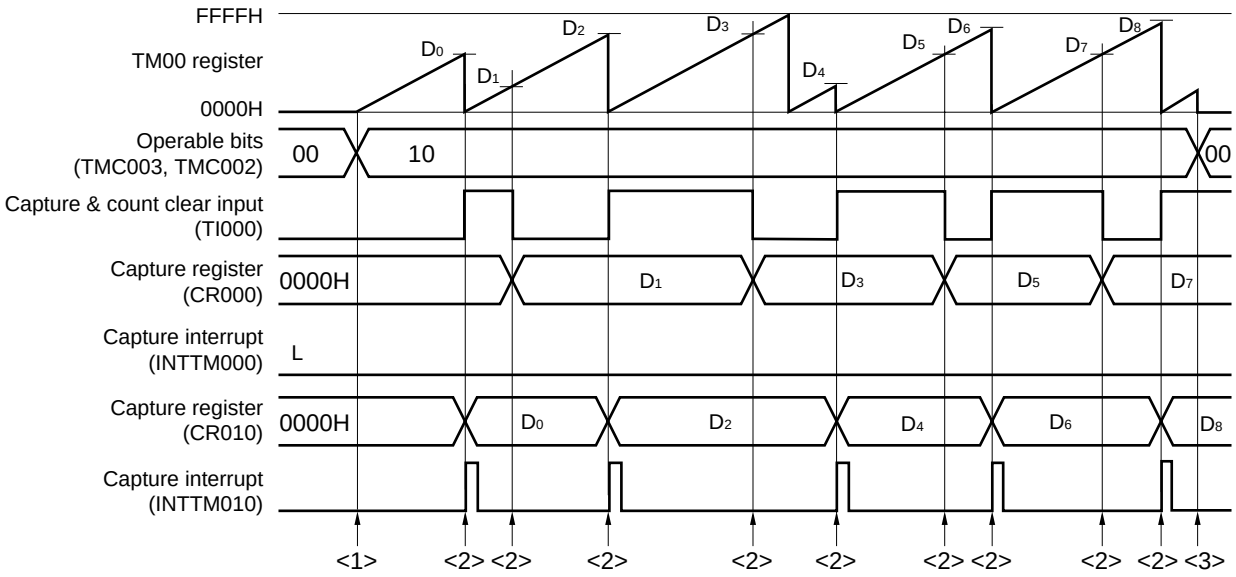
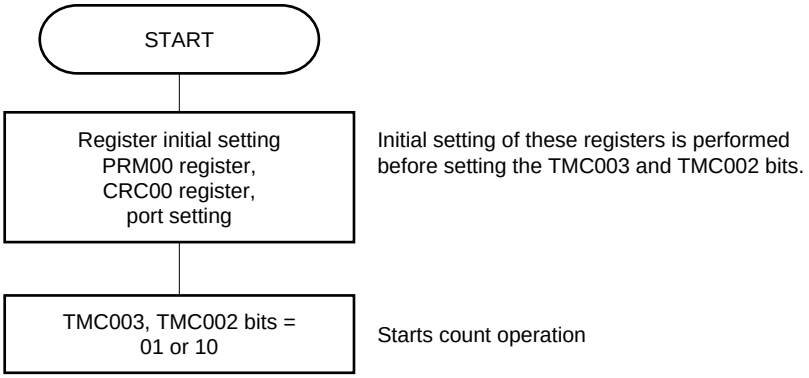
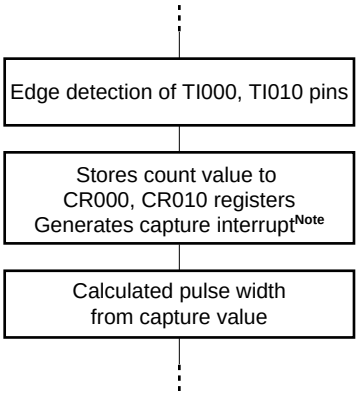


Figure 6-52. Example of Software Processing for Pulse Width Measurement (2/2)

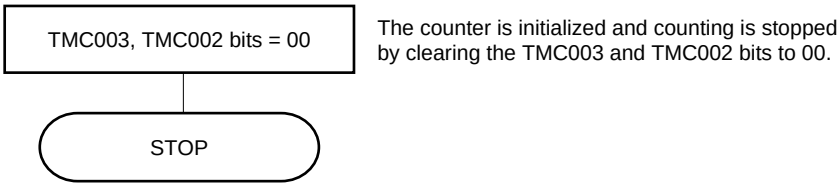
<1> Count operation start flow



<2> Capture trigger input flow



<3> Count operation stop flow



Note The capture interrupt signal (INTTM000) is not generated when the reverse-phase edge of the TI000 pin input is selected to the valid edge of CR000.

6.5 Special Use of TM00

6.5.1 Rewriting CR010 during TM00 operation

In principle, rewriting CR000 and CR010 of the µPD79F7023, 79F7024 microcontrollers when they are used as compare registers is prohibited while TM00 is operating (TMC003 and TMC002 = other than 00).

However, the value of CR010 can be changed, even while TM00 is operating, using the following procedure if CR010 is used for PPG output and the duty factor is changed. (When changing the value of CR010 to a smaller value than the current one, rewrite it immediately after its value matches the value of TM00. When changing the value of CR010 to a larger value than the current one, rewrite it immediately after the values of CR000 and TM00 match. If the value of CR010 is rewritten immediately before a match between CR010 and TM00, or between CR000 and TM00, an unexpected operation may be performed.).

Procedure for changing value of CR010

<1> Disable interrupt INTTM010 (TMMK010 = 1).
<2> Disable reversal of the timer output when the value of TM00 matches that of CR010 (TOC004 = 0).
<3> Change the value of CR010.
<4> Wait for one cycle of the count clock of TM00.
<5> Enable reversal of the timer output when the value of TM00 matches that of CR010 (TOC004 = 1).
<6> Clear the interrupt flag of INTTM010 (TMIF010 = 0) to 0.
<7> Enable interrupt INTTM010 (TMMK010 = 0).

Remark For TMIF010 and TMMK010, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

6.5.2 Setting LVS00 and LVR00

(1) Usage of LVS00 and LVR00

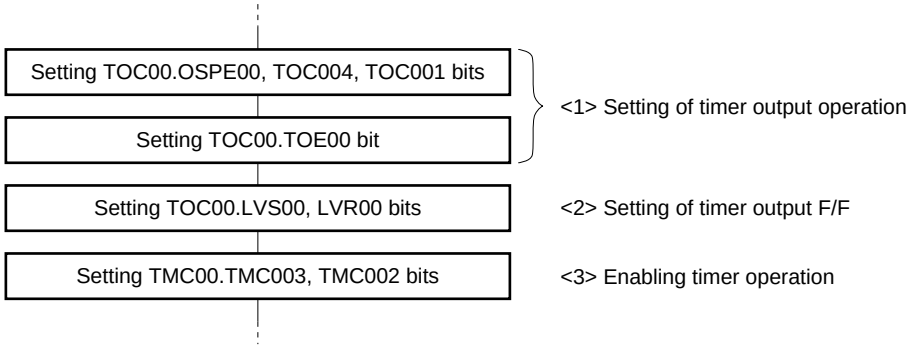
LVS00 and LVR00 are used to set the default value of the TO00 output and to invert the timer output without enabling the timer operation (TMC003 and TMC002 = 00). Clear LVS00 and LVR00 to 00 (default value: low-level output) when software control is unnecessary.

LVS00	LVR00	Timer Output Status
0	0	Not changed (low-level output)
0	1	Cleared (low-level output)
1	0	Set (high-level output)
1	1	Setting prohibited

(2) Setting LVS00 and LVR00

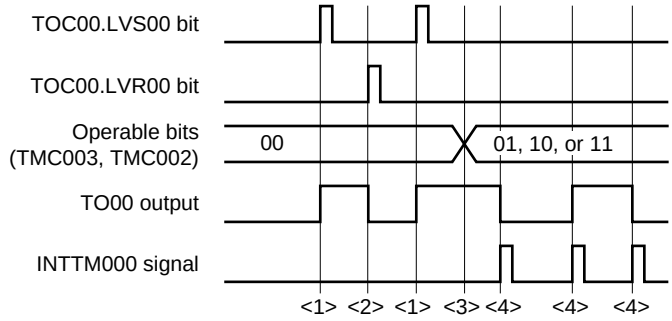
Set LVS00 and LVR00 using the following procedure.

Figure 6-53. Example of Flow for Setting LVS00 and LVR00 Bits



Caution Be sure to set LVS00 and LVR00 following steps <1>, <2>, and <3> above.
Step <2> can be performed after <1> and before <3>.

Figure 6-54. Timing Example of LVR00 and LVS00



<1> The TO00 output goes high when LVS00 and LVR00 = 10.

<2> The TO00 output goes low when LVS00 and LVR00 = 01 (the pin output remains unchanged from the high level even if LVS00 and LVR00 are cleared to 00).

<3> The timer starts operating when TMC003 and TMC002 are set to 01, 10, or 11. Because LVS00 and LVR00 were set to 10 before the operation was started, the TO00 output starts from the high level. After the timer starts operating, setting LVS00 and LVR00 is prohibited until TMC003 and TMC002 = 00 (disabling the timer operation).

<4> The TO00 output level is inverted each time an interrupt signal (INTTM000) is generated.

6.6 Cautions for 16-Bit Timer/Event Counter 00

(1) Restrictions for each channel of 16-bit timer/event counter 00

Table 6-3 shows the restrictions for each channel.

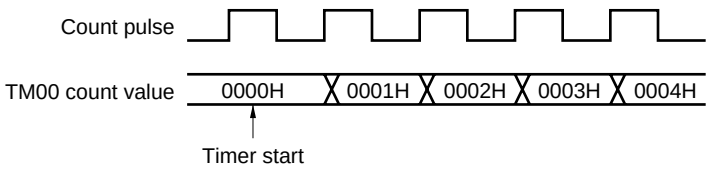
Table 6-3. Restrictions for Each Channel of 16-Bit Timer/Event Counter 00

Operation	Restriction
As interval timer	–
As square-wave output	
As external event counter	
As clear & start mode entered by TI000 pin valid edge input	Using timer output (TO00) is prohibited when detection of the valid edge of the TI010 pin is used. (TOC00 = 00H)
As free-running timer	–
As PPG output	0000H ≤ CP010 < CR000 ≤ FFFFH
As one-shot pulse output	Setting the same value to CR000 and CP010 is prohibited.
As pulse width measurement	Using timer output (TO00) is prohibited (TOC00 = 00H)

(2) Timer start errors

An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because counting TM00 is started asynchronously to the count pulse.

Figure 6-55. Start Timing of TM00 Count



(3) Setting of CR000 and CR010 (clear & start mode entered upon a match between TM00 and CR000)

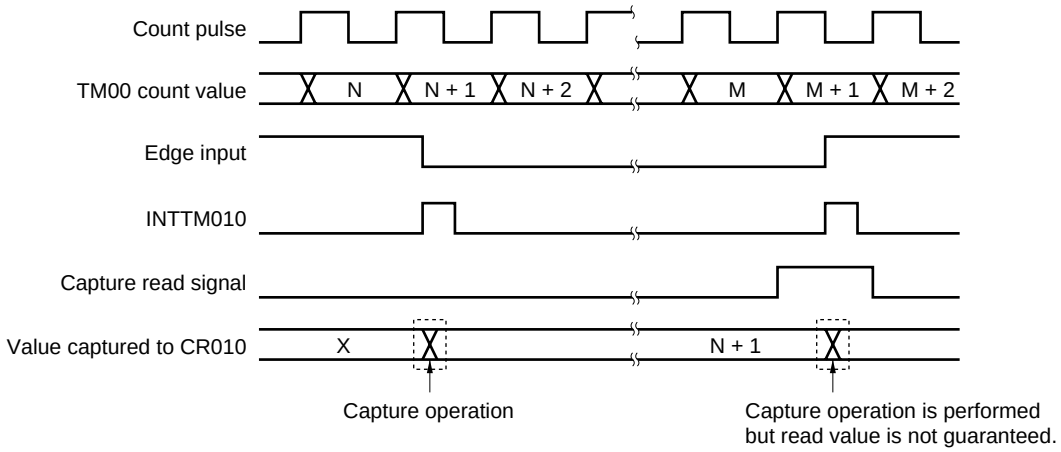
Set a value other than 0000H to CR000 and CR010 (TM00 cannot count one pulse when it is used as an external event counter).

(4) Timing of holding data by capture register

(a) When the valid edge is input to the TI000/TI010 pin and the reverse phase of the TI000 pin is detected while CR000/CR010 is read, CR010 performs a capture operation but the read value of CR000/CR010 is not guaranteed. At this time, an interrupt signal (INTTM000/INTTM010) is generated when the valid edge of the TI000/TI010 pin is detected (the interrupt signal is not generated when the reverse-phase edge of the TI000 pin is detected).

When the count value is captured because the valid edge of the TI000/TI010 pin was detected, read the value of CR000/CR010 after INTTM000/INTTM010 is generated.

Figure 6-56. Timing of Holding Data by Capture Register



(b) The values of CR000 and CR010 are not guaranteed after 16-bit timer/event counter 00 stops.

(5) Setting valid edge

Set the valid edge of the TI000 pin while the timer operation is stopped (TMC003 and TMC002 = 00). Set the valid edge by using ES000 and ES010.

(6) Re-triggering one-shot pulse

Make sure that the trigger is not generated while an active level is being output in the one-shot pulse output mode. Be sure to input the next trigger after the current active level is output.

(7) Operation of OVF00 flag

(a) Setting OVF00 flag (1)

The OVF00 flag is set to 1 in the following case, as well as when TM00 overflows.

Select the clear & start mode entered upon a match between TM00 and CR000.

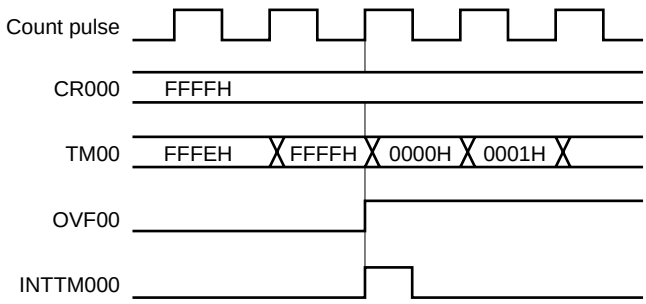
↓

Set CR000 to FFFFH.

↓

When TM00 matches CR000 and TM00 is cleared from FFFFH to 0000H

Figure 6-57. Operation Timing of OVF00 Flag



(b) Clearing OVF00 flag

Even if the OVF00 flag is cleared to 0 after TM00 overflows and before the next count clock is counted (before the value of TM00 becomes 0001H), it is set to 1 again and clearing is invalid.

(8) One-shot pulse output

One-shot pulse output operates correctly in the free-running timer mode or the clear & start mode entered by the TI000 pin valid edge. The one-shot pulse cannot be output in the clear & start mode entered upon a match between TM00 and CR000.

(9) Capture operation

(a) When valid edge of TI000 is specified as count clock

When the valid edge of TI000 is specified as the count clock, the capture register for which TI000 is specified as a trigger does not operate correctly.

(b) Pulse width to accurately capture value by signals input to TI010 and TI000 pins

To accurately capture the count value, the pulse input to the TI000 and TI010 pins as a capture trigger must be wider than two count clocks selected by PRM00 (refer to **Figure 6-7**).

(c) Generation of interrupt signal

The capture operation is performed at the falling edge of the count clock but the interrupt signals (INTTM000 and INTTM010) are generated at the rising edge of the next count clock (refer to **Figure 6-7**).

(d) Note when CRC001 (bit 1 of capture/compare control register 00 (CRC00)) is set to 1

When the count value of the TM00 register is captured to the CR000 register in the phase reverse to the signal input to the TI000 pin, the interrupt signal (INTTM000) is not generated after the count value is captured. If the valid edge is detected on the TI010 pin during this operation, the capture operation is not performed but the INTTM000 signal is generated as an external interrupt signal. Mask the INTTM000 signal when the external interrupt is not used.

(10) Edge detection

(a) Specifying valid edge after reset

If the operation of the 16-bit timer/event counter 00 is enabled after reset and while the TI000 or TI010 pin is at high level and when the rising edge or both the edges are specified as the valid edge of the TI000 or TI010 pin, then the high level of the TI000 or TI010 pin is detected as the rising edge. Note this when the TI000 or TI010 pin is pulled up. However, the rising edge is not detected when the operation is once stopped and then enabled again.

(b) Sampling clock for eliminating noise

The sampling clock for eliminating noise differs depending on whether the valid edge of TI000 is used as the count clock or capture trigger. In the former case, the sampling clock is fixed to f_{PRS}. In the latter, the count clock selected by PRM00 is used for sampling.

When the signal input to the TI000 pin is sampled and the valid level is detected two times in a row, the valid edge is detected. Therefore, noise having a short pulse width can be eliminated (refer to **Figure 6-7**).

(11) Timer operation

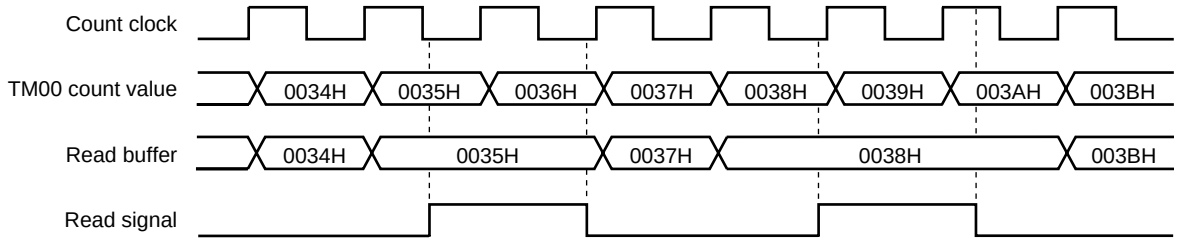
The signal input to the TI000/TI010 pin is not acknowledged while the timer is stopped, regardless of the operation mode of the CPU.

Remark f_{PRS}: Peripheral hardware clock frequency

(12) Reading of 16-bit timer counter 00 (TM00)

TM00 can be read without stopping the actual counter, because the count values captured to the buffer are fixed when it is read. The buffer, however, may not be updated when it is read immediately before the counter counts up, because the buffer is updated at the timing the counter counts up.

Figure 6-58. 16-bit Timer Counter 00 (TM00) Read Timing



CHAPTER 7 8-BIT TIMER/EVENT COUNTER 51

7.1 Functions of 8-Bit Timer/Event Counter 51

8-bit timer/event counter 51 has the following functions.

(1) Interval timer
(2) External event counter
(3) Square-wave output
(4) PWM output

Remark Square-wave output and PWM output are available only as a basic clock for UART0.

7.2 Configuration of 8-Bit Timer/Event Counter 51

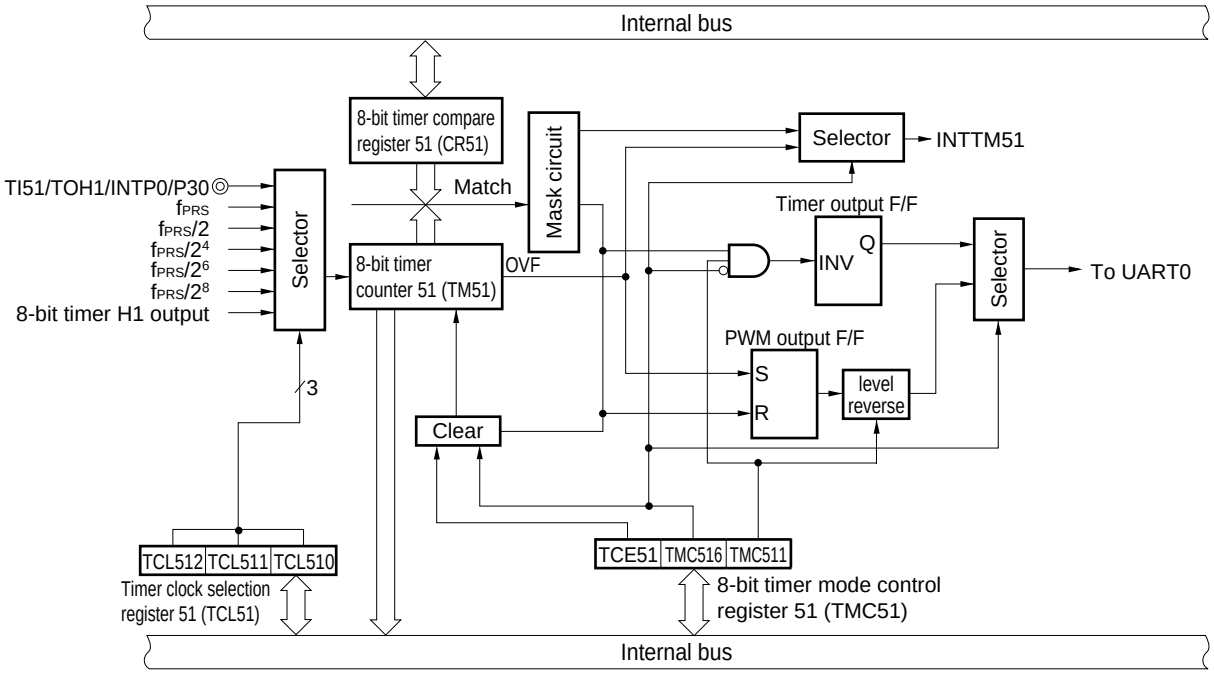
8-bit timer/event counter 51 includes the following hardware.

Table 7-1. Configuration of 8-Bit Timer/Event Counter 51

Item	Configuration
Timer register	8-bit timer counter 51 (TM51)
Timer input	TI51
Register	8-bit timer compare register 51 (CR51)
Control registers	Timer clock selection register 51 (TCL51) 8-bit timer mode control register 51 (TMC51) Port mode register 3 (PM3) Port register 3 (P3)

Figure 7-1 shows the block diagrams of 8-bit timer/event counter 51.

Figure 7-1. Block Diagram of 8-Bit Timer 51



(1) 8-bit timer counter 51 (TM51)

TM51 is an 8-bit register that counts the count pulses and is read-only.

The counter is incremented in synchronization with the rising edge of the count clock.

Figure 7-2. Format of 8-Bit Timer Counter 51 (TM51)

Address: FF1FH After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
TM51								

In the following situations, the count value is cleared to 00H.

<1> Reset signal generation

<2> When TCE51 is cleared

<3> When TM51 and CR51 match in the mode in which clear & start occurs upon a match of the TM51 and CR51.

(2) 8-bit timer compare register 51 (CR51)

CR51 can be read and written by an 8-bit memory manipulation instruction.

The value set in CR51 is constantly compared with the 8-bit timer counter 51 (TM51) count value, and an interrupt request (INTTM51) is generated if they match.

The value of CR51 can be set within 00H to FFH.

Reset signal generation clears CR51 to 00H.

Figure 7-3. Format of 8-Bit Timer Compare Register 51 (CR51)

Address: FFB1H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CR51								

Caution In the mode in which clear & start occurs on a match of TM5n and CR5n (TMC5n6 = 0), do not write other values to CR5n during operation.

7.3 Registers Controlling 8-Bit Timer/Event Counter 51

The following four registers are used to control 8-bit timer/event counter 51.

- Timer clock selection register 51 (TCL51)
- 8-bit timer mode control register 51 (TMC51)
- Port mode register 3 (PM3)
- Port register 3 (P3)

(1) Timer clock selection register 51 (TCL51)

This register sets the count clock of 8-bit timer/event counter 51 and the valid edge of the TI51 pin input.

TCL51 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears TCL51 to 00H.

Figure 7-4. Format of Timer Clock Selection Register 51 (TCL51)

Address: FFB2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
TCL51	0	0	0	0	0	TCL512	TCL511	TCL510

TCL512	TCL511	TCL510	Count clock selection			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	TI51 pin falling edge[Note]			
0	0	1	TI51 pin rising edge[Note]			
0	1	0	f_{PRS}	2 MHz	5 MHz	10 MHz
0	1	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
1	0	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz
1	0	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	1	0	$f_{PRS}/2^8$	7.81 kHz	19.53 kHz	39.06 kHz
1	1	1	TMH1 output			

Note Do not start timer operation with the external clock from the TI51 pin when the internal high-speed oscillation clock and high-speed system clock are stopped while the CPU operates with the subsystem clock, or when in the STOP mode.

Cautions 1. When rewriting TCL51 to other data, stop the timer operation beforehand.

2. Be sure to clear bits 3 to 7 to "0".

Remark f_{PRS}: Peripheral hardware clock frequency

(2) 8-bit timer mode control register 51 (TMC51)

TMC51 is a register that performs 8-bit timer counter 51 (TM51) count operation control.

TMC51 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-5. Format of 8-Bit Timer Mode Control Register 51 (TMC51)

Address: FFB3H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
TMC51	TCE51	TMC516	0	0	0	0	TMC511	0

TCE51	TM51 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

TMC516	TM51 operating mode selection
0	Mode in which clear & start occurs on a match between TM51 and CR51
1	PWM (free-running) mode

TMC511	In other modes (TMC516 = 0)	In PWM mode (TMC516 = 1)
	Timer F/F control	Active level selection
0	Inversion operation disabled	Active-high
1	Inversion operation enabled	Active-low

Cautions 1. Perform <1> to <2> below in the following order, not at the same time.

<1> Set TMC511, TMC516: Operation mode setting

<2> Set TCE51

2. When TCE51 = 1, setting the other bits of TMC51 is prohibited.

Remark In PWM mode, PWM output is made inactive by clearing TCE51 to 0.

(4) Port mode registers 3 (PM3)

This register sets port 3 input/output in 1-bit units.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

When using the P30/TI51/TOH1/INTP0 pin for timer input, set PM30 to 1. The output latches of P30 at this time may be 0 or 1.

Figure 7-6. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

7.4 Operations of 8-Bit Timer/Event Counter 51

7.4.1 Operation as interval timer

8-bit timer/event counter 51 operates as an interval timer that generates interrupt requests repeatedly at intervals of the count value preset to 8-bit timer compare register 51 (CR51).

When the count value of 8-bit timer counter 51 (TM51) matches the value set to CR51, counting continues with the TM51 value cleared to 0 and an interrupt request signal (INTTM51) is generated.

The count clock of TM51 can be selected with bits 0 to 2 (TCL510 to TCL512) of timer clock selection register 51 (TCL51).

Setting

<1> Set the registers.

- TCL51: Select the count clock.
- CR51: Compare value
- TMC51: Stop the count operation, select the mode in which clear & start occurs on a match of TM51 and CR51.
  (TMC51 = 0000×××0B × = Don't care)

<2> After TCE51 = 1 is set, the count operation starts.

<3> If the values of TM51 and CR51 match, INTTM51 is generated (TM51 is cleared to 00H).

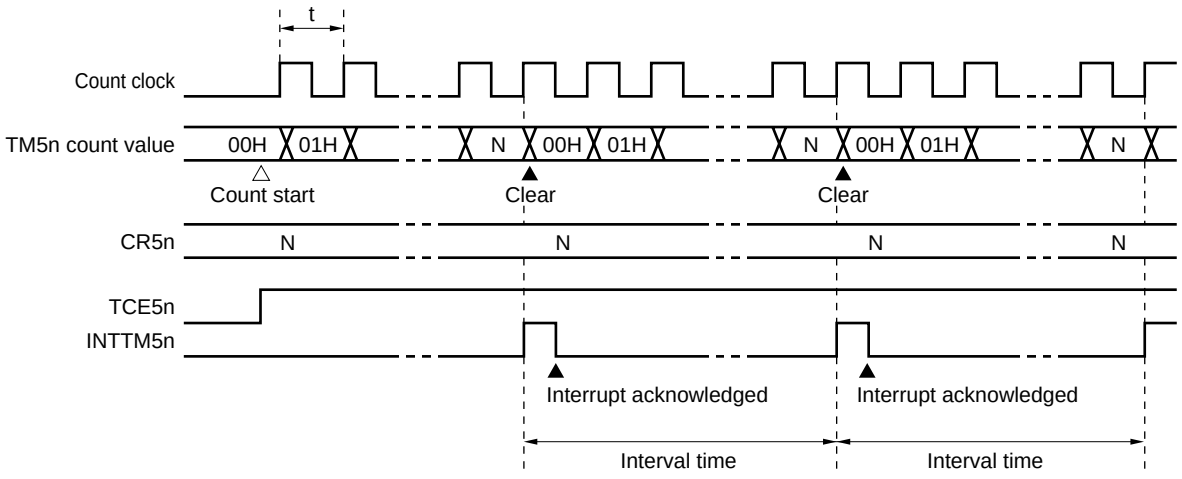
<4> INTTM51 is generated repeatedly at the same interval.
Set TCE51 to 0 to stop the count operation.

Caution Do not write other values to CR51 during operation.

Remark For how to enable the INTTM51 signal interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

Figure 7-7. Interval Timer Operation Timing (1/2)

(a) Basic operation

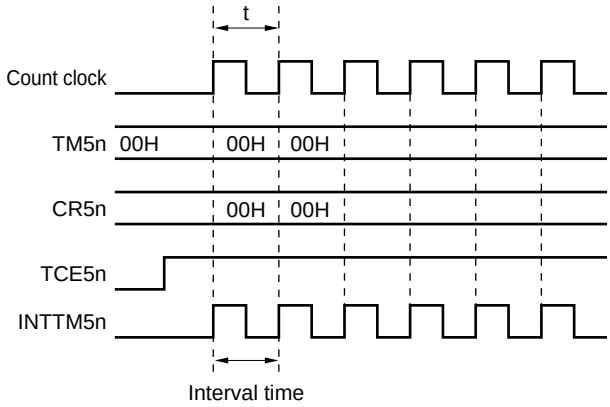


Remarks 1. Interval time = (N + 1) × t, N = 01H to FFH

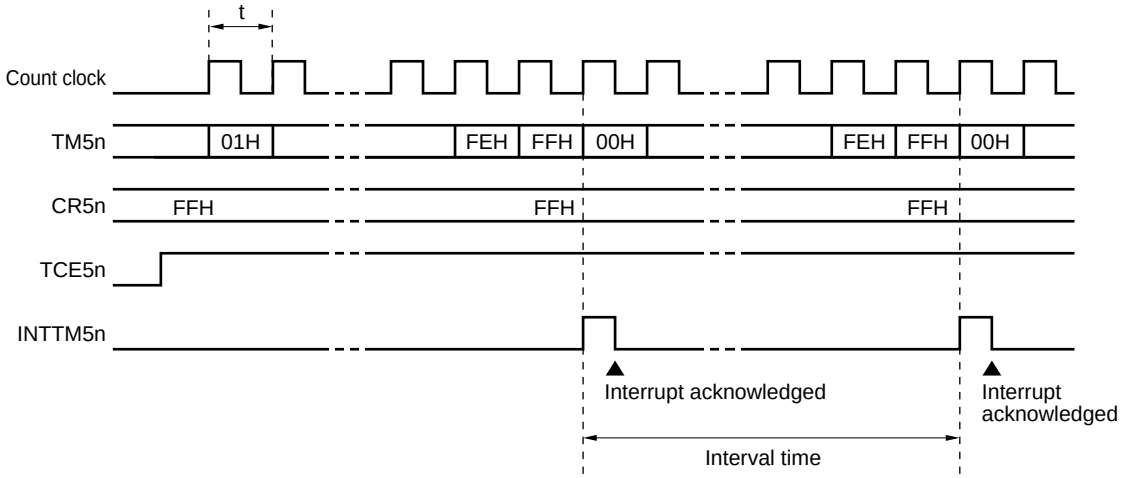
2. n = 1

Figure 7-7. Interval Timer Operation Timing (2/2)

(b) When CR51 = 00H



(c) When CR51 = FFH



Remark n = 1

7.4.2 Operation as external event counter

The external event counter counts the number of external clock pulses to be input to the TI51 pin by 8-bit timer counter 51 (TM51).

TM51 is incremented each time the valid edge specified by timer clock selection register 51 (TCL51) is input. Either the rising or falling edge can be selected.

When the TM51 count value matches the value of 8-bit timer compare register 51 (CR51), TM51 is cleared to 0 and an interrupt request signal (INTTM51) is generated.

Whenever the TM51 value matches the value of CR51, INTTM51 is generated.

Setting

<1> Set each register.

- Set the port mode register (PM30) to 1.
- TCL51: Select TI51 pin input edge.
  TI51 pin falling edge → TCL51 = 00H
  TI51 pin rising edge → TCL51 = 01H
- CR51: Compare value
- TMC51: Stop the count operation, select the mode in which clear & start occurs on match of TM51 and CR51, disable the timer F/F inversion operation, disable timer output.
  (TMC51 = 00000000B)

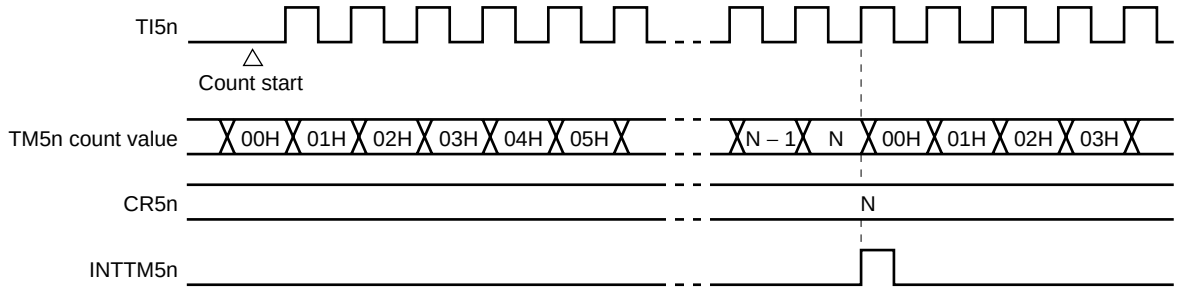
<2> When TCE51 = 1 is set, the number of pulses input from the TI51 pin is counted.

<3> When the values of TM51 and CR51 match, INTTM51 is generated (TM51 is cleared to 00H).

<4> After these settings, INTTM51 is generated each time the values of TM51 and CR51 match.

Remark For how to enable the INTTM51 signal interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

Figure 7-8. External Event Counter Operation Timing (with Rising Edge Specified)



Remarks 1. N = 00H to FFH

2. n = 1

7.4.3 Square-wave output operation

A square wave with any selected frequency is output at intervals determined by the value preset to 8-bit timer compare register 51 (CR51).

The timer 51 output status is inverted at intervals determined by the count value preset to CR51. This enables a square wave with any selected frequency to be output (duty = 50%).

Remark Square-wave output is available only as a basic clock for UART0.

Setting

<1> Set each register.

- Clear the port output latch (P30) and port mode register (PM30) to 0.
- TCL51: Select the count clock.
- CR51: Compare value
- TMC51: Stop the count operation, select the mode in which clear & start occurs on a match of TM51 and CR51. (TMC5n = 00000010B)

<2> After TCE51 = 1 is set, the count operation starts.

<3> The timer output F/F is inverted by a match of TM51 and CR51. After INTTM51 is generated, TM51 is cleared to 00H.

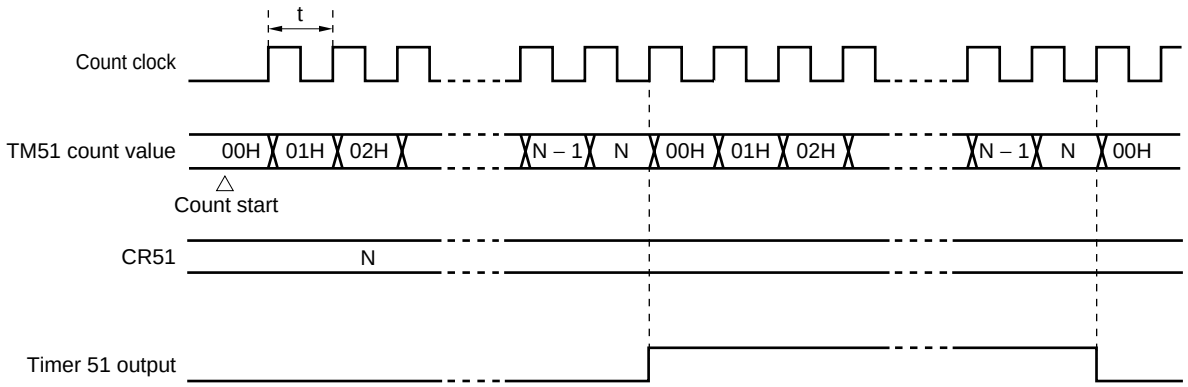
<4> After these settings, the timer output F/F is inverted at the same interval and a square wave is output.
The frequency is as follows.

- Frequency = 1/2t (N + 1)
  (N: 00H to FFH)

Caution Do not write other values to CR51 during operation.

Remark For how to enable the INTTM51 signal interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

Figure 7-9. Square-Wave Output Operation Timing



7.4.4 PWM output operation

8-bit timer/event counter 51 operates as a PWM output when bit 6 (TMC516) of 8-bit timer mode control register 51 (TMC51) is set to 1.

The duty pulse determined by the value set to 8-bit timer compare register 51 (CR51) is output.

Set the active level width of the PWM pulse to CR51; the active level can be selected with bit 1 (TMC511) of TMC51.

The count clock can be selected with bits 0 to 2 (TCL510 to TCL512) of timer clock selection register 51 (TCL51).

Caution In PWM mode, make the CR51 rewrite period 3 count clocks of the count clock (clock selected by TCL51) or more.

Remark PWM output is available only as a basic clock for UART0.

(1) PWM output basic operation

Setting

<1> Set each register.

- Clear the port output latch (P30) and port mode register (PM30) to 0.
- TCL51: Select the count clock.
- CR51: Compare value
- TMC51: Stop the count operation, select PWM mode.

TMC511	Active Level Selection
0	Active-high
1	Active-low

(TMC51 = 01000000B or 01000010B)

<2> The count operation starts when TCE51 = 1.
Clear TCE51 to 0 to stop the count operation.

PWM output operation

<1> PWM output (timer 51 output) outputs an inactive level until an overflow occurs.

<2> When an overflow occurs, the active level is output. The active level is output until CR51 matches the count value of 8-bit timer counter 51 (TM51).

<3> After the CR51 matches the count value, the inactive level is output until an overflow occurs again.

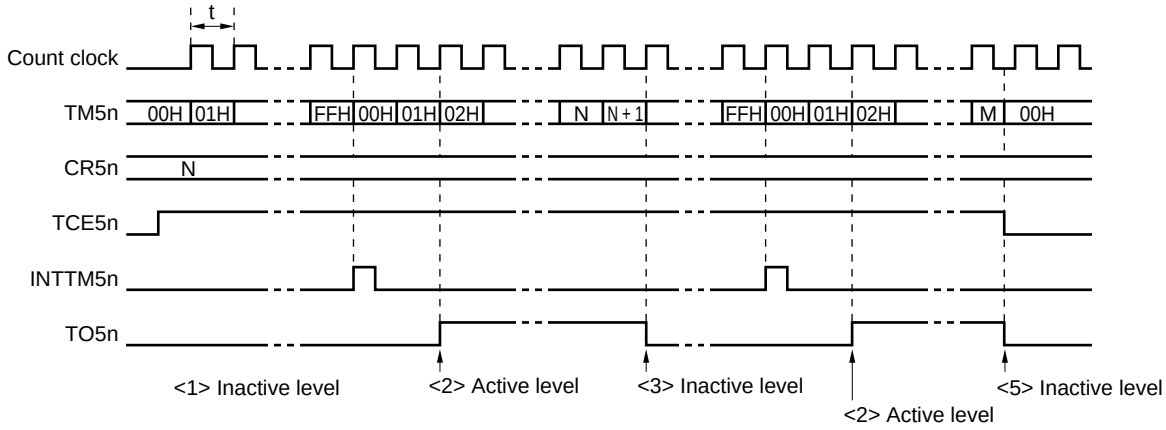
<4> Operations <2> and <3> are repeated until the count operation stops.

<5> When the count operation is stopped with TCE51 = 0, PWM output becomes inactive.
For details of timing, refer to **Figures 7-10** and **7-11**.
The cycle, active-level width, and duty are as follows.

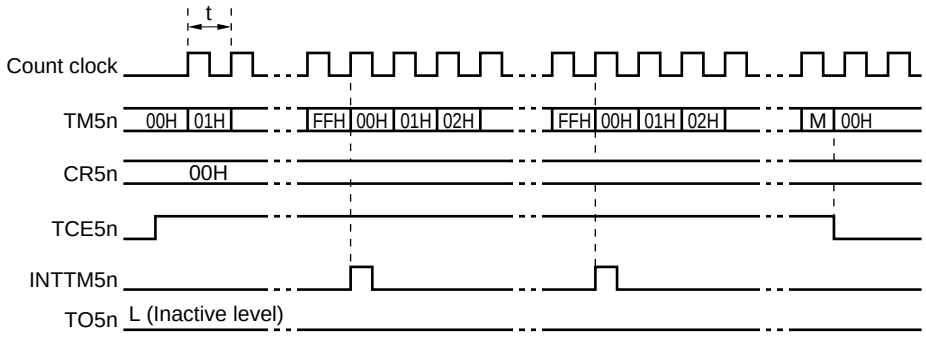
- Cycle = 2^8t
- Active-level width = Nt
- Duty = N/2^8
  (N = 00H to FFH)

Figure 7-10. PWM Output Operation Timing

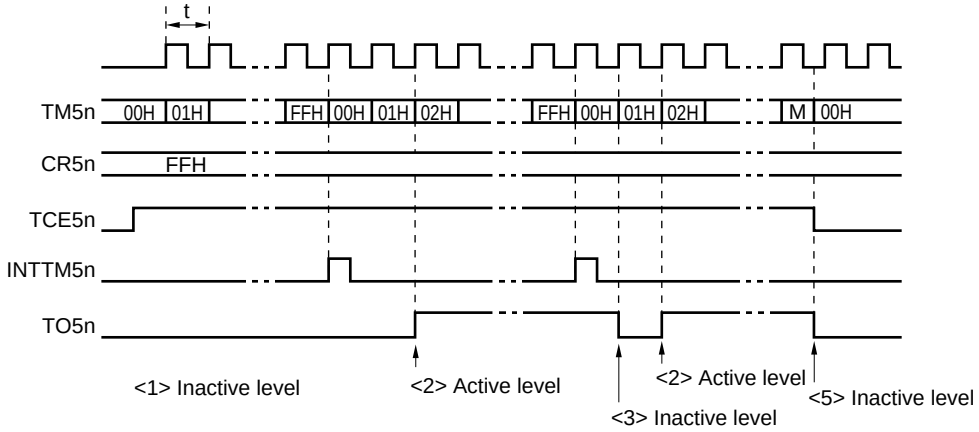
(a) Basic operation (active level = H)



(b) CR5n = 00H



(c) CR5n = FFH



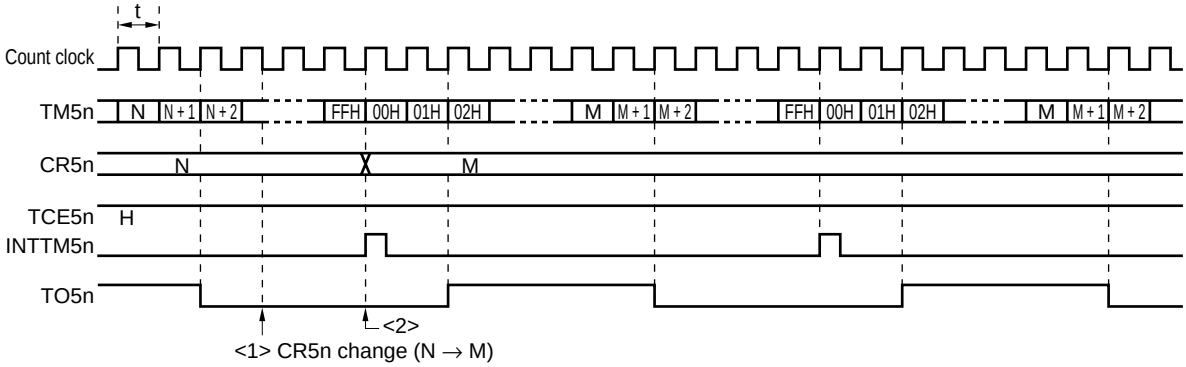
Remarks 1. <1> to <3> and <5> in Figure 7-10 (a) and (c) correspond to <1> to <3> and <5> in PWM output operation in **7.4.4 (1) PWM output basic operation**.

2. n = 1

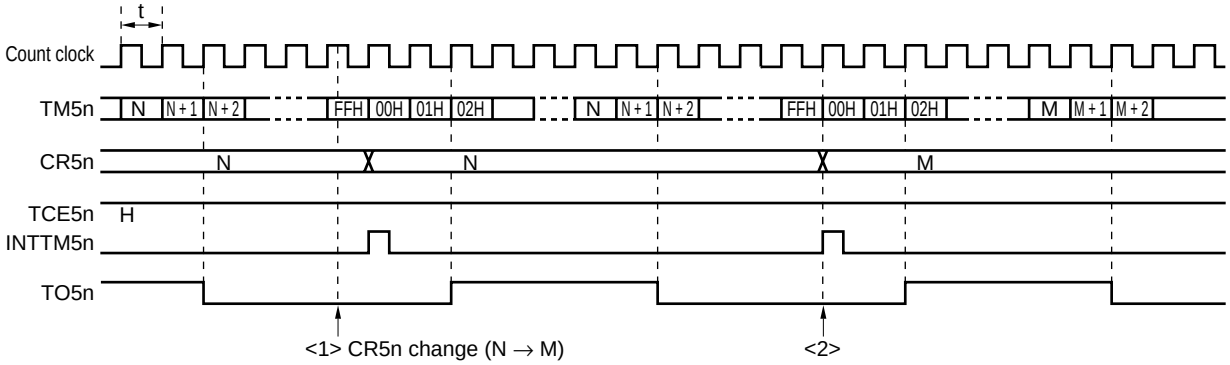
(2) Operation with CR51 changed

Figure 7-11. Timing of Operation with CR51 Changed

(a) CR51 value is changed from N to M before clock rising edge of FFH
→ Value is transferred to CR51 at overflow immediately after change.



(b) CR51 value is changed from N to M after clock rising edge of FFH
→ Value is transferred to CR51 at second overflow.



Caution When reading from CR51 between <1> and <2> in Figure 7-11, the value read differs from the actual value (read value: M, actual value of CR51: N).

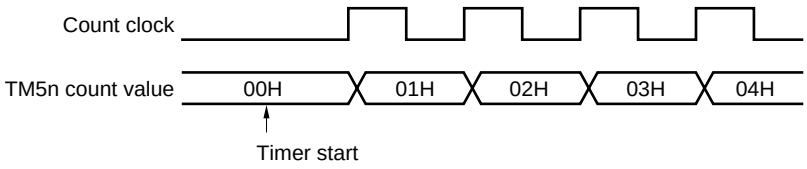
Remark n = 1

7.5 Cautions for 8-Bit Timer/Event Counter 51

(1) Timer start error

An error of up to one clock may occur in the time required for a match signal to be generated after timer start. This is because 8-bit timer counter 51 (TM51) is started asynchronously to the count clock.

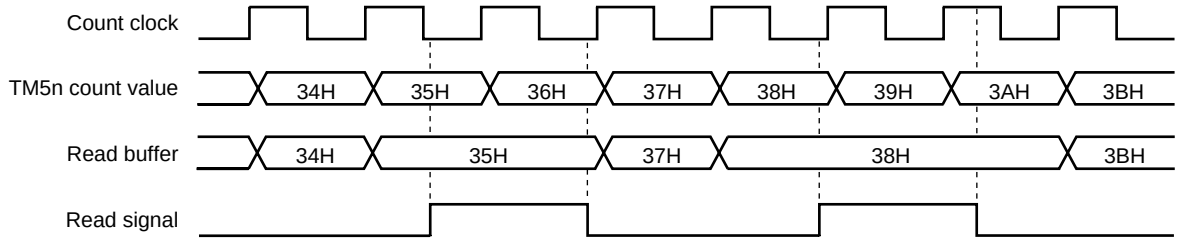
Figure 7-12. 8-Bit Timer Counter 51 (TM51) Start Timing



(2) Reading of 8-bit timer counter 51 (TM51)

TM51 can be read without stopping the actual counter, because the count values captured to the buffer are fixed when it is read. The buffer, however, may not be updated when it is read immediately before the counter counts up, because the buffer is updated at the timing the counter counts up.

Figure 7-13. 8-bit Timer Counter 51 (TM51) Read Timing



Remark n = 1

CHAPTER 8 8-BIT TIMER H1

8.1 Functions of 8-Bit Timer H1

8-bit timer H1 has the following functions.

- Interval timer
- Square-wave output
- PWM output
- Carrier generator

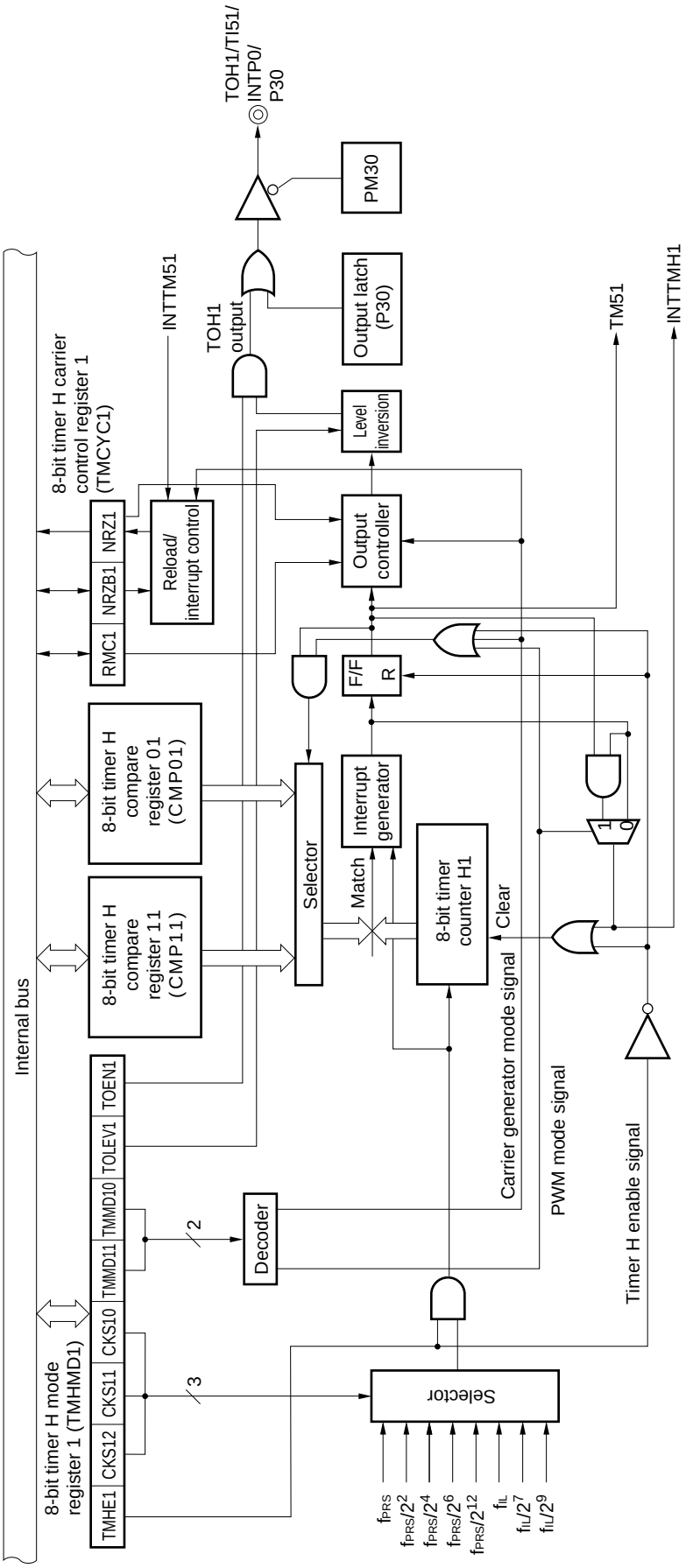
8.2 Configuration of 8-Bit Timer H1

8-bit timer H1 includes the following hardware.

Table 8-1. Configuration of 8-Bit Timer H1

Item	Configuration
Timer register	8-bit timer counter H1
Registers	8-bit timer H compare register 01 (CMP01) 8-bit timer H compare register 11 (CMP11)
Timer output	TOH1, output controller
Control registers	8-bit timer H mode register n (TMHMD1) 8-bit timer H carrier control register 1 (TMCYC1) Port mode register 3 (PM3) Port register 3 (P3)

Figure 8-1. Block Diagram of 8-Bit Timer H1



(1) 8-bit timer H compare register 01 (CMP01)

This register can be read or written by an 8-bit memory manipulation instruction. This register is used in all of the timer operation modes.

This register constantly compares the value set to CMP01 with the count value of the 8-bit timer counter H1 and, when the two values match, generates an interrupt request signal (INTTMH1) and inverts the output level of TOH1.

Rewrite the value of CMP01 while the timer is stopped (TMHE1 = 0).

A reset signal generation clears this register to 00H.

Figure 8-2. Format of 8-Bit Timer H Compare Register 01 (CMP01)

Address: FF1AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMP01								

Caution CMP01 cannot be rewritten during timer count operation. CMP01 can be refreshed (the same value is written) during timer count operation.

(2) 8-bit timer H compare register 11 (CMP11)

This register can be read or written by an 8-bit memory manipulation instruction. This register is used in the PWM output mode and carrier generator mode.

In the PWM output mode, this register constantly compares the value set to CMP11 with the count value of the 8-bit timer counter H1 and, when the two values match, inverts the output level of TOH1. No interrupt request signal is generated.

In the carrier generator mode, the CMP11 register always compares the value set to CMP11 with the count value of the 8-bit timer counter H1 and, when the two values match, generates an interrupt request signal (INTTMH1). At the same time, the count value is cleared.

CMP11 can be refreshed (the same value is written) and rewritten during timer count operation.

If the value of CMP11 is rewritten while the timer is operating, the new value is latched and transferred to CMP11 when the count value of the timer matches the old value of CMP11, and then the value of CMP11 is changed to the new value. If matching of the count value and the CMP11 value and writing a value to CMP11 conflict, the value of CMP11 is not changed.

A reset signal generation clears this register to 00H.

Figure 8-3. Format of 8-Bit Timer H Compare Register 11 (CMP11)

Address: FF1BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CMP11								

Caution In the PWM output mode and carrier generator mode, be sure to set CMP11 when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to CMP11).

8.3 Registers Controlling 8-Bit Timer H1

The following four registers are used to control 8-bit timer H1.

- 8-bit timer H mode register 1 (TMHMD1)
- 8-bit timer H carrier control register 1 (TMCYC1)
- Port mode register 3 (PM3)
- Port register 3 (P3)

(1) 8-bit timer H mode register n (TMHMD1)

This register controls the mode of timer H.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 8-4. Format of 8-Bit Timer H Mode Register 1 (TMHMD1)

Address: FF6CH After reset: 00H R/W

	<7>	6	5	4	3	2	<1>	<0>
TMHMD1	TMHE1	CKS12	CKS11	CKS10	TMMD11	TMMD10	TOLEV1	TOEN1

TMHE1	Timer operation enable
0	Stops timer count operation (counter is cleared to 0)
1	Enables timer count operation (count operation started by inputting clock)

CKS12	CKS11	CKS10	Count clock selection			
				f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	0	f_{PRS}	2 MHz	5 MHz	10 MHz
0	0	1	$f_{PRS}/2^2$	500 kHz	1.25 MHz	2.5 MHz
0	1	0	$f_{PRS}/2^4$	125 kHz	312.5 kHz	625 kHz
0	1	1	$f_{PRS}/2^6$	31.25 kHz	78.13 kHz	156.25 kHz
1	0	0	$f_{PRS}/2^{12}$	0.49 kHz	1.22 kHz	2.44 kHz
1	0	1	$f_{IL}/2^7$	1.88 kHz (TYP.)		
1	1	0	$f_{IL}/2^9$	0.47 kHz (TYP.)		
1	1	1	f_{IL}	240 kHz (TYP.)		

TMMD11	TMMD10	Timer operation mode
0	0	Interval timer mode
0	1	Carrier generator mode
1	0	PWM output mode
1	1	Setting prohibited

TOLEV1	Timer output level control (in default mode)
0	Low level
1	High level

TOEN1	Timer output control
0	Disables output
1	Enables output

Cautions 1. When TMHE1 = 1, setting the other bits of TMHMD1 is prohibited. However, TMHMD1 can be refreshed (the same value is written).

2. In the PWM output mode and carrier generator mode, be sure to set the 8-bit timer H compare register 11 (CMP11) when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to CMP11).

3. When the carrier generator mode is used, set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.

4. The actual TOH1/TI51/INTP0/P30 pin output is determined depending on PM30 and P30, besides TOH1 output.

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. f_{IL}: Internal low-speed oscillation clock frequency

(2) 8-bit timer H carrier control register 1 (TMCYC1)

This register controls the remote control output and carrier pulse output status of 8-bit timer H1.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 8-5. Format of 8-Bit Timer H Carrier Control Register 1 (TMCYC1)

Address: FF71H After reset: 00H R/W[Note]

	7	6	5	4	3	2	1	<0>
TMCYC1	0	0	0	0	0	RMC1	NRZB1	NRZ1

RMC1	NRZB1	Remote control output
0	0	Low-level output
0	1	High-level output at rising edge of INTTM51 signal input
1	0	Low-level output
1	1	Carrier pulse output at rising edge of INTTM51 signal input

NRZ1	Carrier pulse output status flag
0	Carrier output disabled status (low-level status)
1	Carrier output enabled status (RMC1 = 1: Carrier pulse output, RMC1 = 0: High-level status)

Note Bit 0 is read-only.

Caution Do not rewrite RMC1 when TMHE = 1. However, TMCYC1 can be refreshed (the same value is written).

(3) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P30/TOH1/TI51/INTP0 pin for timer output, clear PM30 and the output latches of P30 to 0.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 8-6. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

8.4 Operation of 8-Bit Timer H1

8.4.1 Operation as interval timer/square-wave output

When the 8-bit timer counter H1 and compare register 01 (CMP01) match, an interrupt request signal (INTTMH1) is generated and the 8-bit timer counter H1 is cleared to 00H.

Compare register 11 (CMP11) is not used in interval timer mode. Since a match of the 8-bit timer counter H1 and the CMP11 register is not detected even if the CMP11 register is set, timer output is not affected.

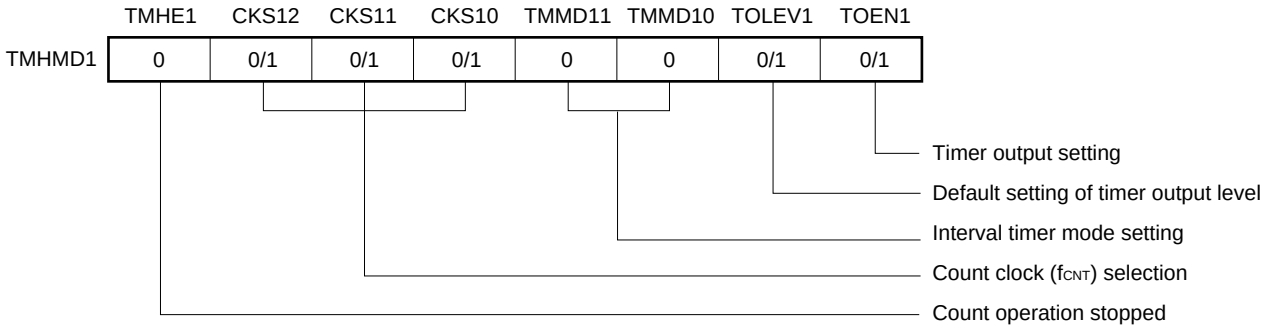
By setting bit 0 (TOEN1) of timer H mode register n (TMHMD1) to 1, a square wave of any frequency (duty = 50%) is output from TOH1.

Setting

<1> Set each register.

Figure 8-7. Register Setting During Interval Timer/Square-Wave Output Operation

(i) Setting timer H mode register 1 (TMHMD1)



(ii) CMP01 register setting

The interval time is as follows if N is set as a comparison value.

- Interval time = (N +1)/f_{CNT}

<2> Count operation starts when TMHE1 = 1.

<3> When the values of the 8-bit timer counter H1 and the CMP01 register match, the INTTMH1 signal is generated and the 8-bit timer counter H1 is cleared to 00H.

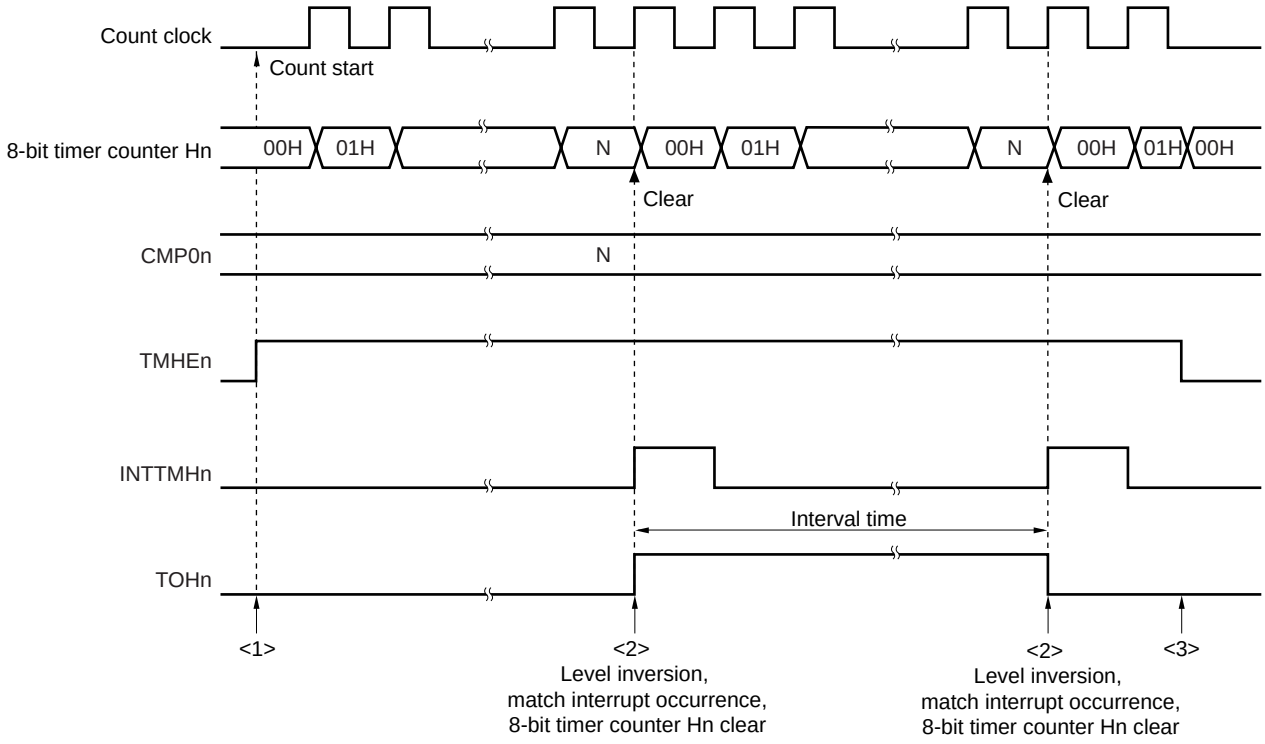
<4> Subsequently, the INTTMH1 signal is generated at the same interval. To stop the count operation, clear TMHE1 to 0.

Remarks 1. For the setting of the output pin, refer to **8.3 (3) Port mode register 3 (PM3)**.

2. For how to enable the INTTMH1 signal interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

Figure 8-8. Timing of Interval Timer/Square-Wave Output Operation (1/2)

(a) Basic operation (Operation When 01H ≤ CMP01 ≤ FEH)



<1> The count operation is enabled by setting the TMHE1 bit to 1. The count clock starts counting no more than 1 clock after the operation is enabled.

<2> When the value of the 8-bit timer counter H1 matches the value of the CMP01 register, the value of the timer counter is cleared, and the level of the TOH1 output is inverted. In addition, the INTTMH1 signal is output at the rising edge of the count clock.

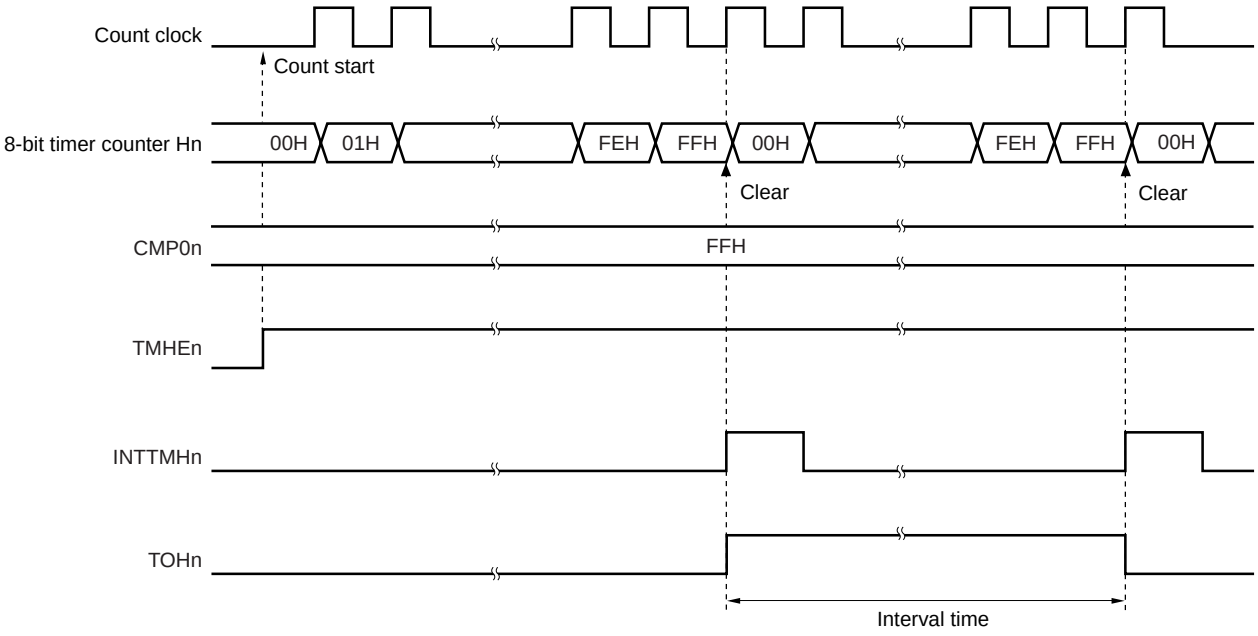
<3> If the TMHE1 bit is cleared to 0 while timer H is operating, the INTTMH1 signal and TOH1 output are set to the default level. If they are already at the default level before the TMHE1 bit is cleared to 0, then that level is maintained.

Remarks 1. 01H ≤ N ≤ FEH

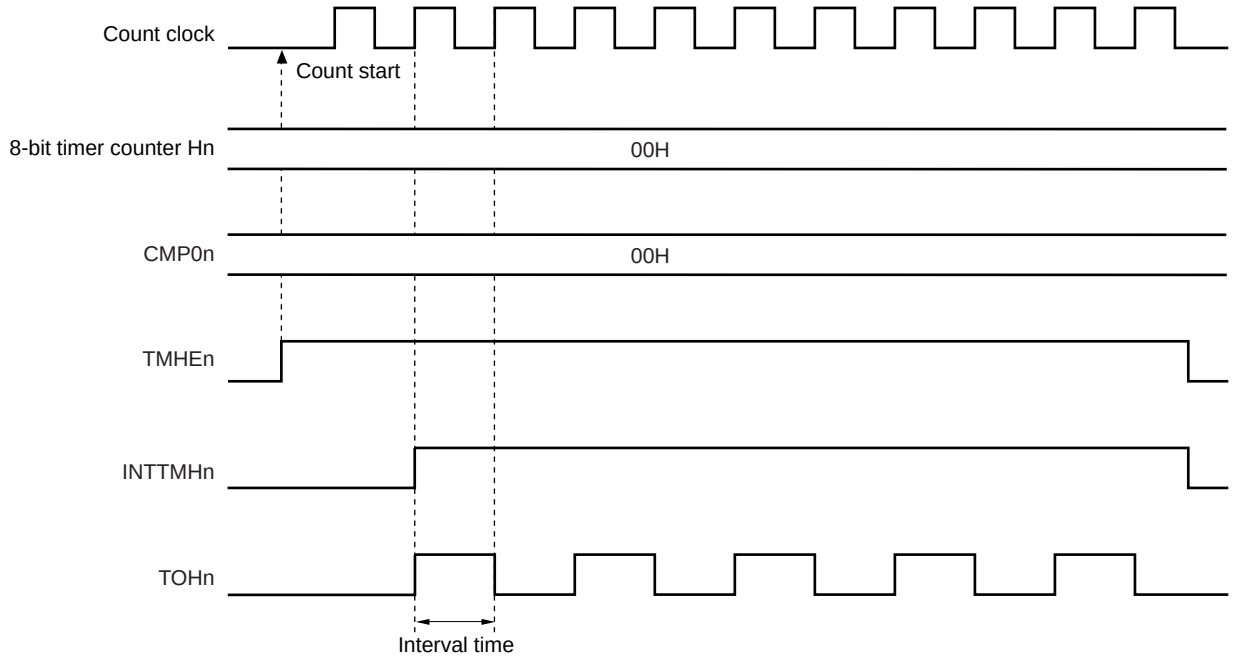
2. n = 1

Figure 8-8. Timing of Interval Timer/Square-Wave Output Operation (2/2)

(b) Operation when CMP01 = FFH



(c) Operation when CMP01 = 00H



Remark n = 1

8.4.2 Operation as PWM output

In PWM output mode, a pulse with an arbitrary duty and arbitrary cycle can be output.

The 8-bit timer compare register 01 (CMP01) controls the cycle of timer output (TOH1). Rewriting the CMP01 register during timer operation is prohibited.

The 8-bit timer compare register 11 (CMP11) controls the duty of timer output (TOH1). Rewriting the CMP11 register during timer operation is possible.

The operation in PWM output mode is as follows.

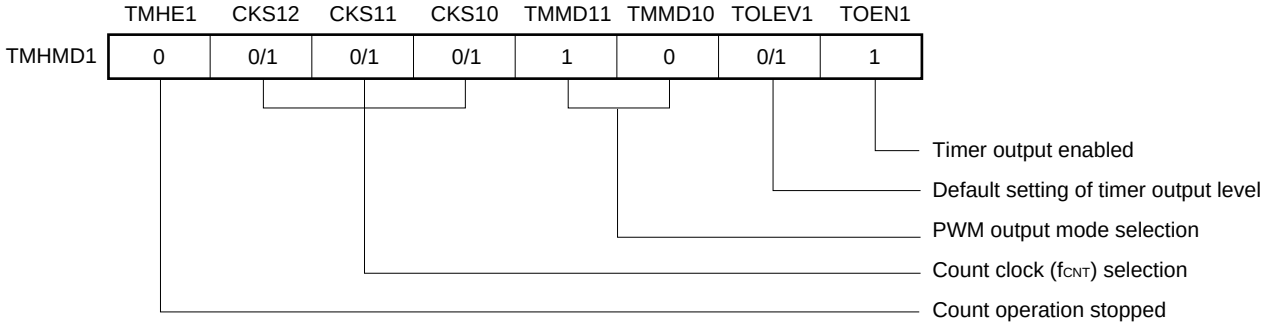
PWM output (TOH1 output) outputs an active level and 8-bit timer counter H1 is cleared to 0 when 8-bit timer counter H1 and the CMP01 register match after the timer count is started. PWM output (TOH1 output) outputs an inactive level when 8-bit timer counter H1 and the CMP11 register match.

Setting

<1> Set each register.

Figure 8-9. Register Setting in PWM Output Mode

(i) Setting timer H mode register 1 (TMHMD1)



(ii) Setting CMP01 register

- Compare value (N): Cycle setting

(iii) Setting CMP11 register

- Compare value (M): Duty setting

Remarks 00H ≤ CMP11 (M) < CMP01 (N) ≤ FFH

<2> The count operation starts when TMHE1 = 1.

<3> The CMP01 register is the compare register that is to be compared first after counter operation is enabled. When the values of the 8-bit timer counter H1 and the CMP01 register match, the 8-bit timer counter H1 is cleared, an interrupt request signal (INTTMH1) is generated, and an active level is output. At the same time, the compare register to be compared with the 8-bit timer counter H1 is changed from the CMP01 register to the CMP11 register.

<4> When the 8-bit timer counter H1 and the CMP11 register match, an inactive level is output and the compare register to be compared with the 8-bit timer counter H1 is changed from the CMP11 register to the CMP01 register. At this time, the 8-bit timer counter H1 is not cleared and the INTTMH1 signal is not generated.

<5> By performing procedures <3> and <4> repeatedly, a pulse with an arbitrary duty can be obtained.

<6> To stop the count operation, set TMHE1 = 0.

If the setting value of the CMP01 register is N, the setting value of the CMP11 register is M, and the count clock frequency is f_{CNT}, the PWM pulse output cycle and duty are as follows.

- PWM pulse output cycle = (N + 1)/f_{CNT}
- Duty = (M + 1)/(N + 1)

Cautions 1. The set value of the CMP11 register can be changed while the timer counter is operating. However, this takes a duration of three operating clocks (signal selected by the CKSn2 to CKSn0 bits of the TMHMD1 register) from when the value of the CMP11 register is changed until the value is transferred to the register.

2. Be sure to set the CMP11 register when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).

3. Make sure that the CMP11 register setting value (M) and CMP01 register setting value (N) are within the following range.

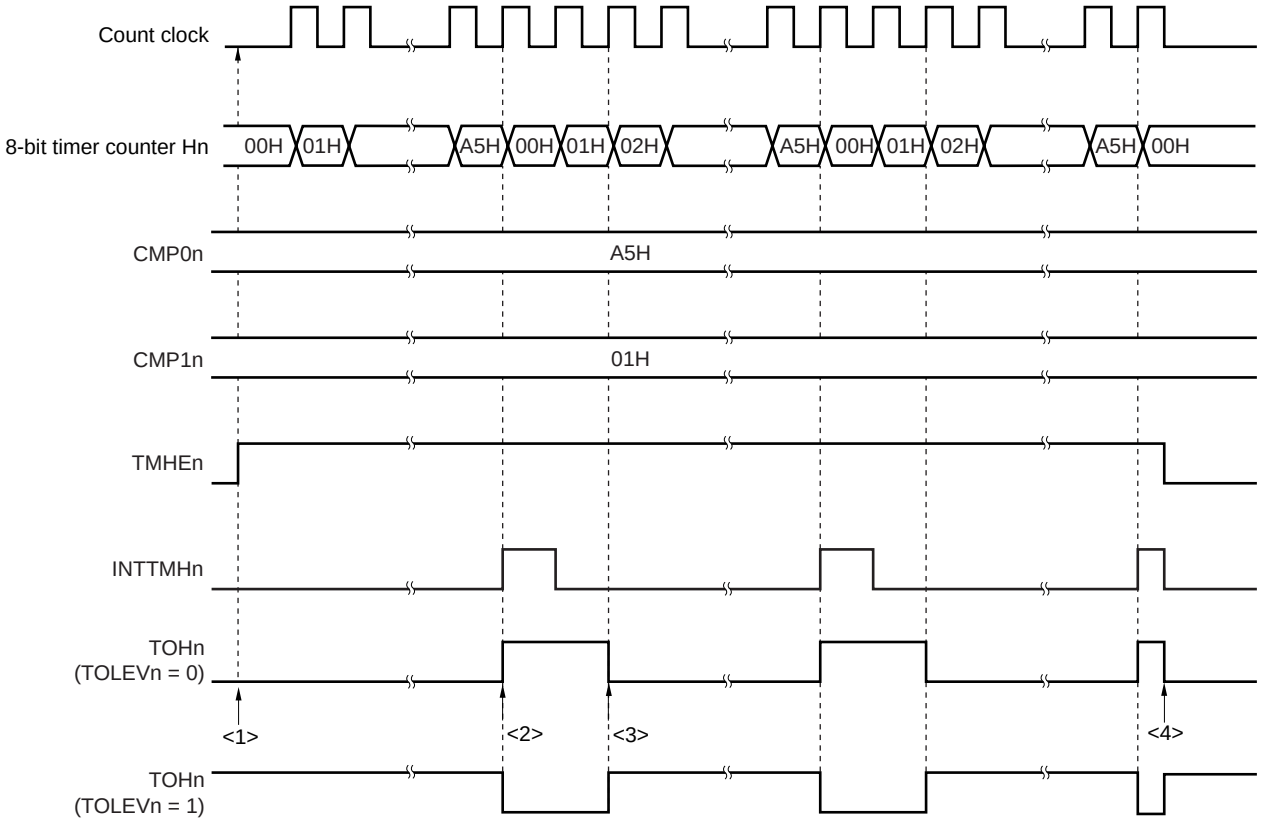
00H ≤ CMP11 (M) < CMP01 (N) ≤ FFH

Remarks 1. For the setting of the output pin, refer to **8.3 (3) Port mode register 3 (PM3)**.

2. For details on how to enable the INTTMH1 signal interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

Figure 8-10. Operation Timing in PWM Output Mode (1/4)

(a) Basic operation



<1> The count operation is enabled by setting the TMHE1 bit to 1. Start the 8-bit timer counter H1 by masking one count clock to count up. At this time, PWM output outputs an inactive level.

<2> When the values of the 8-bit timer counter H1 and the CMP01 register match, an active level is output. At this time, the value of the 8-bit timer counter H1 is cleared, and the INTTMH1 signal is output.

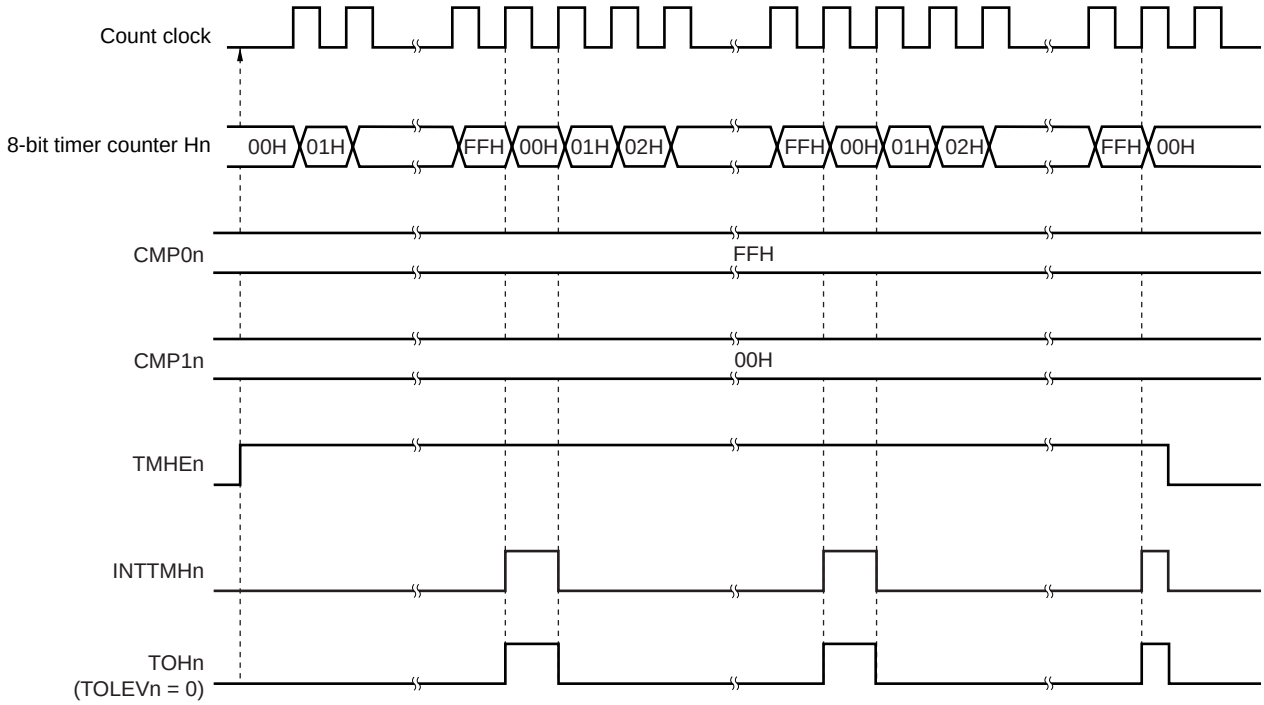
<3> When the values of the 8-bit timer counter H1 and the CMP11 register match, an inactive level is output. At this time, the 8-bit timer counter value is not cleared and the INTTMH1 signal is not output.

<4> Clearing the TMHE1 bit to 0 during timer H1 operation sets the INTTMH1 signal to the default and PWM output to an inactive level.

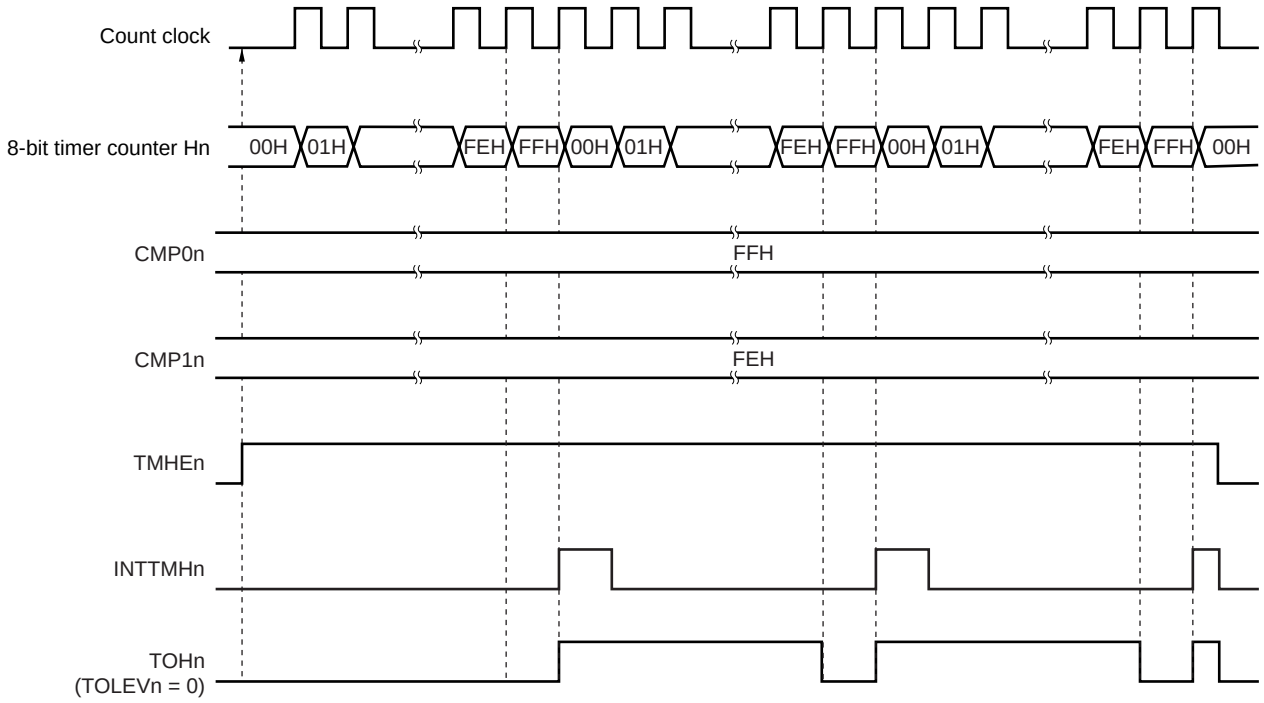
Remark n = 1

Figure 8-10. Operation Timing in PWM Output Mode (2/4)

(b) Operation when CMP01 = FFH, CMP11 = 00H



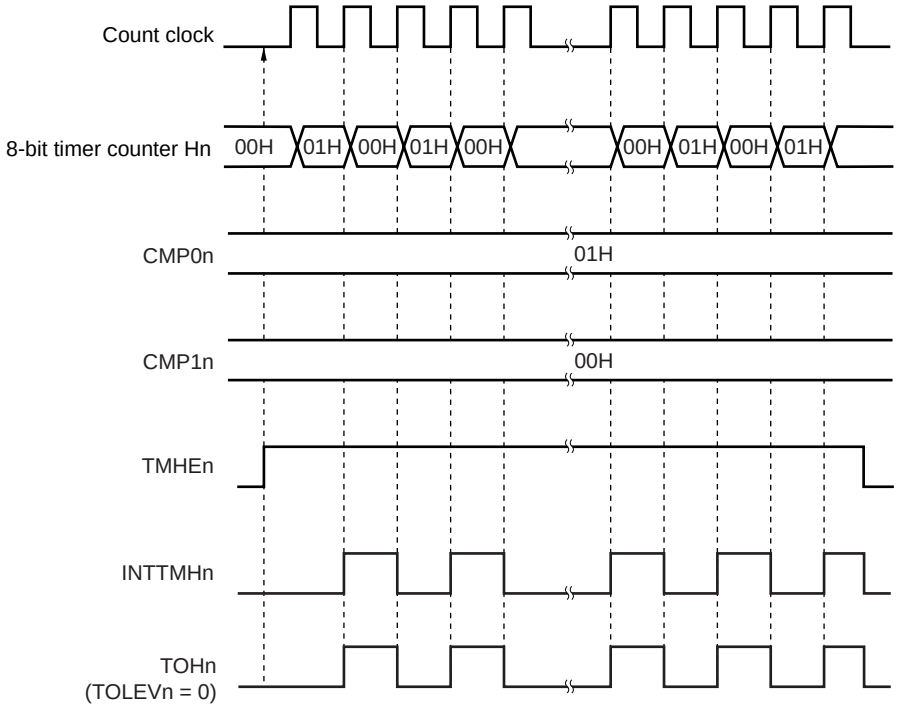
(c) Operation when CMP01 = FFH, CMP11 = FEH



Remark n = 1

Figure 8-10. Operation Timing in PWM Output Mode (3/4)

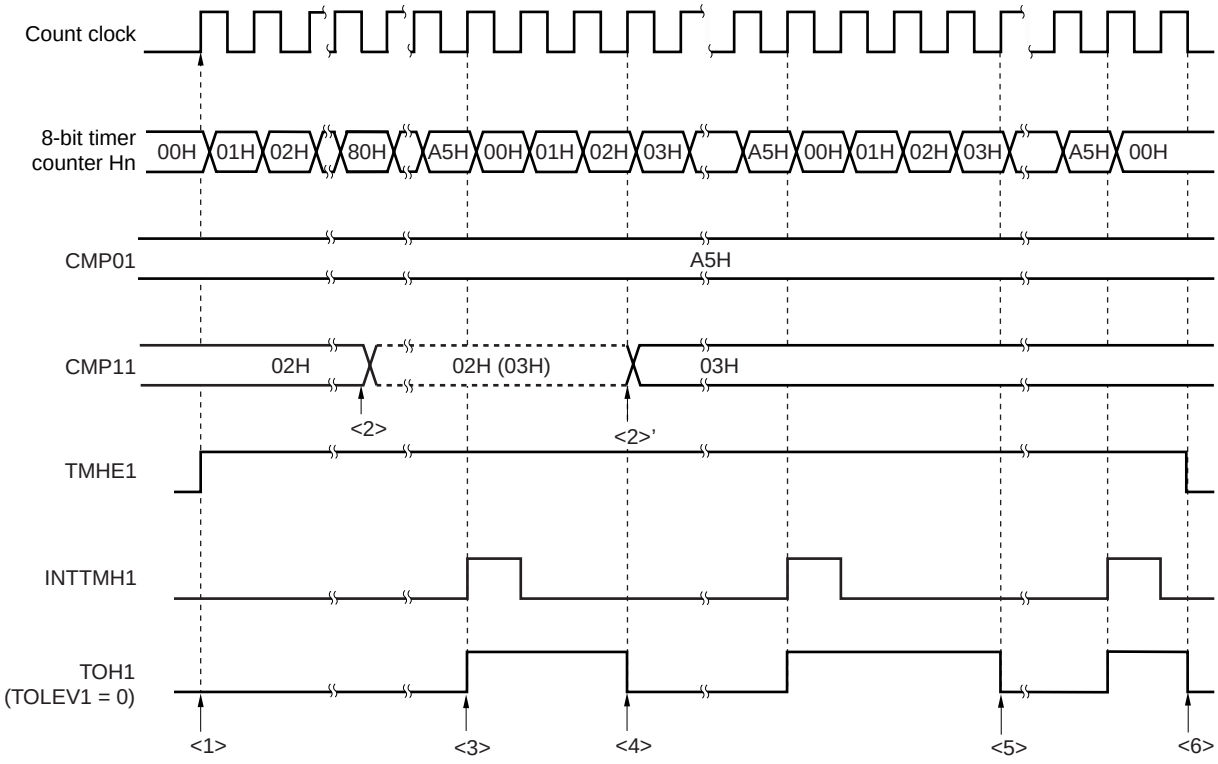
(d) Operation when CMP01 = 01H, CMP11 = 00H



Remark n = 1

Figure 8-10. Operation Timing in PWM Output Mode (4/4)

(e) Operation by changing CMP11 (CMP11 = 02H → 03H, CMP01 = A5H)



<1> The count operation is enabled by setting TMHE1 = 1. Start the 8-bit timer counter H1 by masking one count clock to count up. At this time, PWM output outputs an inactive level.

<2> The CMP11 register value can be changed during timer counter operation. This operation is asynchronous to the count clock.

<3> When the values of the 8-bit timer counter H1 and the CMP01 register match, the value of the 8-bit timer counter H1 is cleared, an active level is output, and the INTTMH1 signal is output.

<4> If the CMP11 register value is changed, the value is latched and not transferred to the register. When the values of the 8-bit timer counter H1 and the CMP11 register before the change match, the value is transferred to the CMP11 register and the CMP11 register value is changed (<2>').

However, three count clocks or more are required from when the CMP11 register value is changed to when the value is transferred to the register. If a match signal is generated within three count clocks, the changed value cannot be transferred to the register.

<5> When the values of the 8-bit timer counter H1 and the CMP11 register after the change match, an inactive level is output. The 8-bit timer counter H1 is not cleared and the INTTMH1 signal is not generated.

<6> Clearing the TMHE1 bit to 0 during timer H1 operation sets the INTTMH1 signal to the default and PWM output to an inactive level.

Remark n = 1

8.4.3 Carrier generator operation

In the carrier generator mode, the 8-bit timer H1 is used to generate the carrier signal of an infrared remote controller, and the 8-bit timer/event counter 51 is used to generate an infrared remote control signal (time count).

The carrier clock generated by the 8-bit timer H1 is output in the cycle set by the 8-bit timer/event counter 51.

In carrier generator mode, the output of the 8-bit timer H1 carrier pulse is controlled by the 8-bit timer/event counter 51, and the carrier pulse is output from the TOH1 output.

(1) Carrier generation

In carrier generator mode, the 8-bit timer H compare register 01 (CMP01) generates a low-level width carrier pulse waveform and the 8-bit timer H compare register 11 (CMP11) generates a high-level width carrier pulse waveform.

Rewriting the CMP11 register during the 8-bit timer H1 operation is possible but rewriting the CMP01 register is prohibited.

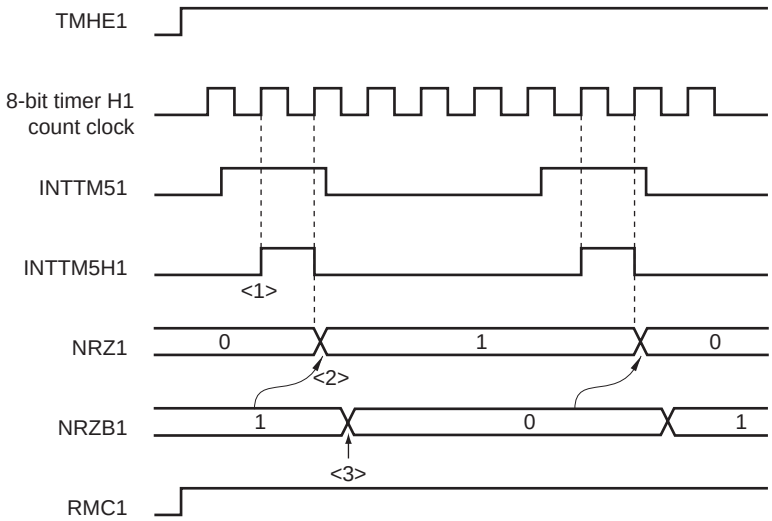
(2) Carrier output control

Carrier output is controlled by the interrupt request signal (INTTM51) of the 8-bit timer/event counter 51 and the NRZB1 and RMC1 bits of the 8-bit timer H carrier control register (TMCYC1). The relationship between the outputs is shown below.

RMC1 Bit	NRZB1 Bit	Output
0	0	Low-level output
0	1	High-level output at rising edge of INTTM51 signal input
1	0	Low-level output
1	1	Carrier pulse output at rising edge of INTTM51 signal input

To control the carrier pulse output during a count operation, the NRZ1 and NRZB1 bits of the TMCYC1 register have a master and slave bit configuration. The NRZ1 bit is read-only but the NRZB1 bit can be read and written. The INTTM51 signal is synchronized with the 8-bit timer H1 count clock and is output as the INTTM5H1 signal. The INTTM5H1 signal becomes the data transfer signal of the NRZ1 bit, and the NRZB1 bit value is transferred to the NRZ1 bit. The timing for transfer from the NRZB1 bit to the NRZ1 bit is as shown below.

Figure 8-11. Transfer Timing



<1> The INTTM51 signal is synchronized with the count clock of the 8-bit timer H1 and is output as the INTTM5H1 signal.

<2> The value of the NRZB1 bit is transferred to the NRZ1 bit at the second clock from the rising edge of the INTTM5H1 signal.

<3> Write the next value to the NRZB1 bit in the interrupt servicing program that has been started by the INTTM5H1 interrupt or after timing has been checked by polling the interrupt request flag. Write data to count the next time to the CR51 register.

Cautions 1. Do not rewrite the NRZB1 bit again until at least the second clock after it has been rewritten, or else the transfer from the NRZB1 bit to the NRZ1 bit is not guaranteed.

2. When the 8-bit timer/event counter 51 is used in the carrier generator mode, an interrupt is generated at the timing of <1>. When the 8-bit timer/event counter 51 is used in a mode other than the carrier generator mode, the timing of the interrupt generation differs.

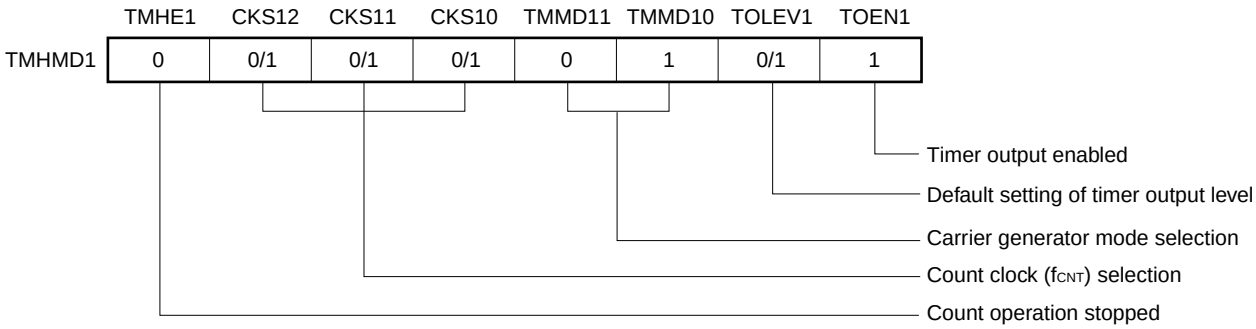
Remark INTTM5H1 is an internal signal and not an interrupt source.

Setting

<1> Set each register.

Figure 8-12. Register Setting in Carrier Generator Mode

(i) Setting 8-bit timer H mode register 1 (TMHMD1)



(ii) CMP01 register setting

- Compare value

(iii) CMP11 register setting

- Compare value

(iv) TMCYC1 register setting

- RMC1 = 1 ... Remote control output enable bit
- NRZB1 = 0/1 ... carrier output enable bit

(v) TCL51 and TMC51 register setting

- Refer to **7.3 Registers Controlling 8-Bit Timer/Event Counter 51**.

<2> When TMHE1 = 1, the 8-bit timer H1 starts counting.

<3> When TCE51 of the 8-bit timer mode control register 51 (TMC51) is set to 1, the 8-bit timer/event counter 51 starts counting.

<4> After the count operation is enabled, the first compare register to be compared is the CMP01 register. When the count value of the 8-bit timer counter H1 and the CMP01 register value match, the INTTMH1 signal is generated, the 8-bit timer counter H1 is cleared. At the same time, the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP01 register to the CMP11 register.

<5> When the count value of the 8-bit timer counter H1 and the CMP11 register value match, the INTTMH1 signal is generated, the 8-bit timer counter H1 is cleared. At the same time, the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP11 register to the CMP01 register.

<6> By performing procedures <4> and <5> repeatedly, a carrier clock is generated.

<7> The INTTM51 signal is synchronized with count clock of the 8-bit timer H1 and output as the INTTM5H1 signal. The INTTM5H1 signal becomes the data transfer signal for the NRZB1 bit, and the NRZB1 bit value is transferred to the NRZ1 bit.

<8> Write the next value to the NRZB1 bit in the interrupt servicing program that has been started by the INTTM5H1 interrupt or after timing has been checked by polling the interrupt request flag. Write data to count the next time to the CR51 register.

<9> When the NRZ1 bit is high level, a carrier clock is output by TOH1 output.

<10> By performing the procedures above, an arbitrary carrier clock is obtained. To stop the count operation, clear TMHE1 to 0.

If the setting value of the CMP01 register is N, the setting value of the CMP11 register is M, and the count clock frequency is f_{CNT}, the carrier clock output cycle and duty are as follows.

- Carrier clock output cycle = (N + M + 2)/f_{CNT}
- Duty = High-level width/carrier clock output width = (M + 1)/(N + M + 2)

Cautions 1. Be sure to set the CMP11 register when starting the timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).

2. Set so that the count clock frequency of TMH1 becomes more than 6 times the count clock frequency of TM51.

3. Set the values of the CMP01 and CMP11 registers in a range of 01H to FFH.

4. The set value of the CMP11 register can be changed while the timer counter is operating. However, it takes the duration of three operating clocks (signal selected by the CKS12 to CKS10 bits of the TMHMD1 register) since the value of the CMP11 register has been changed until the value is transferred to the register.

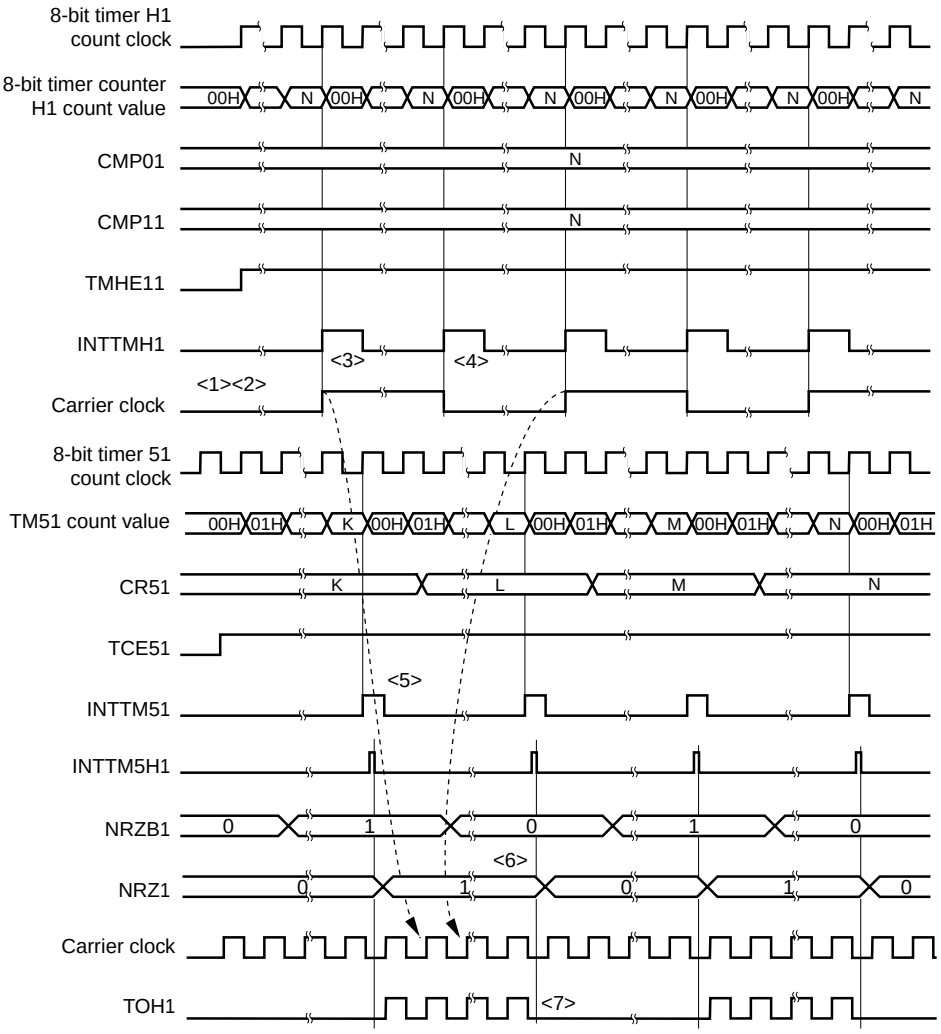
5. Be sure to set the RMC1 bit before the count operation is started.

Remarks 1. For the setting of the output pin, refer to **8.3 (3) Port mode register 3 (PM3)**.

2. For how to enable the INTTMH1 signal interrupt, refer to **CHAPTER 14 INTERRUPT FUNCTIONS**.

Figure 8-13. Carrier Generator Mode Operation Timing (1/3)

(a) Operation when CMP01 = N, CMP11 = N



<1> When TMHE1 = 0 and TCE51 = 0, the 8-bit timer counter H1 operation is stopped.

<2> When TMHE1 = 1 is set, the 8-bit timer counter H1 starts a count operation. At that time, the carrier clock remains default.

<3> When the count value of the 8-bit timer counter H1 matches the CMP01 register value, the first INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP01 register to the CMP11 register. The 8-bit timer counter H1 is cleared to 00H.

<4> When the count value of the 8-bit timer counter H1 matches the CMP11 register value, the INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP11 register to the CMP01 register. The 8-bit timer counter H1 is cleared to 00H. By performing procedures <3> and <4> repeatedly, a carrier clock with duty fixed to 50% is generated.

<5> When the INTTM51 signal is generated, it is synchronized with the 8-bit timer H1 count clock and is output as the INTTM5H1 signal.

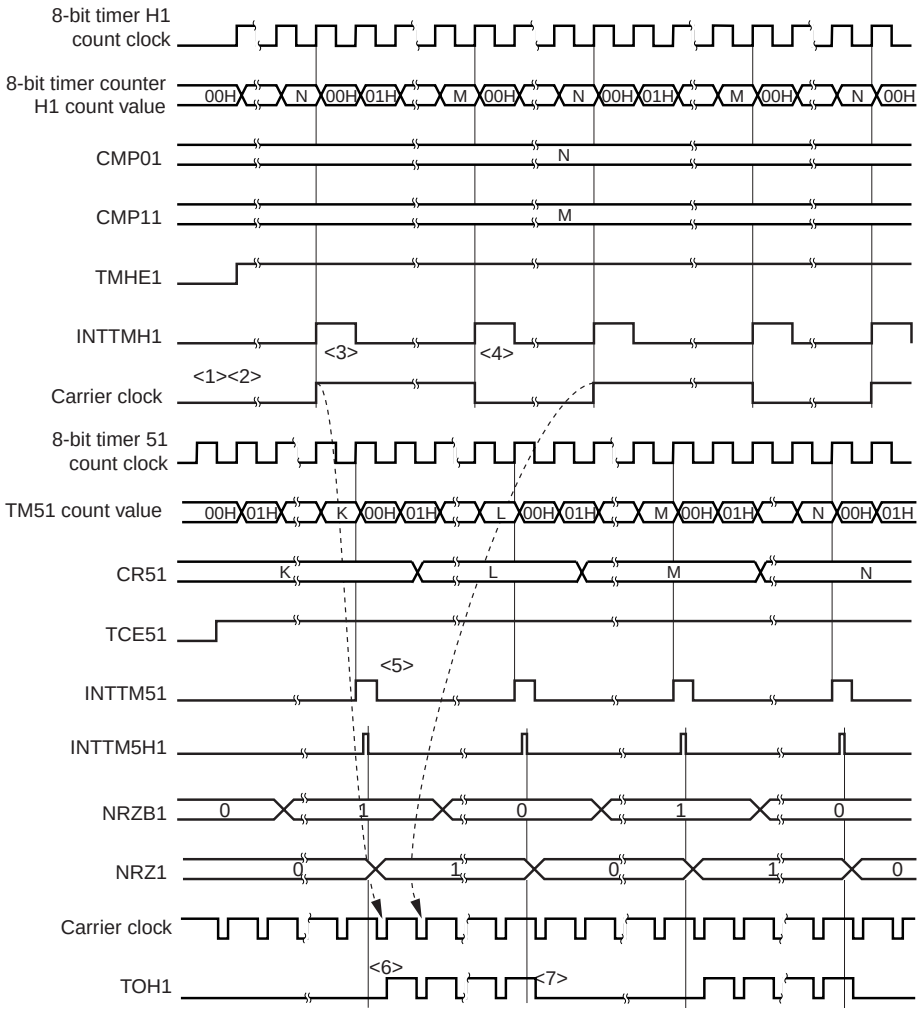
<6> The INTTM5H1 signal becomes the data transfer signal for the NRZB1 bit, and the NRZB1 bit value is transferred to the NRZ1 bit.

<7> When NRZ1 = 0 is set, the TOH1 output becomes low level.

Remark INTTM5H1 is an internal signal and not an interrupt source.

Figure 8-13. Carrier Generator Mode Operation Timing (2/3)

(b) Operation when CMP01 = N, CMP11 = M



<1> When TMHE1 = 0 and TCE51 = 0, the 8-bit timer counter H1 operation is stopped.

<2> When TMHE1 = 1 is set, the 8-bit timer counter H1 starts a count operation. At that time, the carrier clock remains default.

<3> When the count value of the 8-bit timer counter H1 matches the CMP01 register value, the first INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP01 register to the CMP11 register. The 8-bit timer counter H1 is cleared to 00H.

<4> When the count value of the 8-bit timer counter H1 matches the CMP11 register value, the INTTMH1 signal is generated, the carrier clock signal is inverted, and the compare register to be compared with the 8-bit timer counter H1 is switched from the CMP11 register to the CMP01 register. The 8-bit timer counter H1 is cleared to 00H. By performing procedures <3> and <4> repeatedly, a carrier clock with duty fixed to other than 50% is generated.

<5> When the INTTM51 signal is generated, it is synchronized with the 8-bit timer H1 count clock and is output as the INTTM5H1 signal.

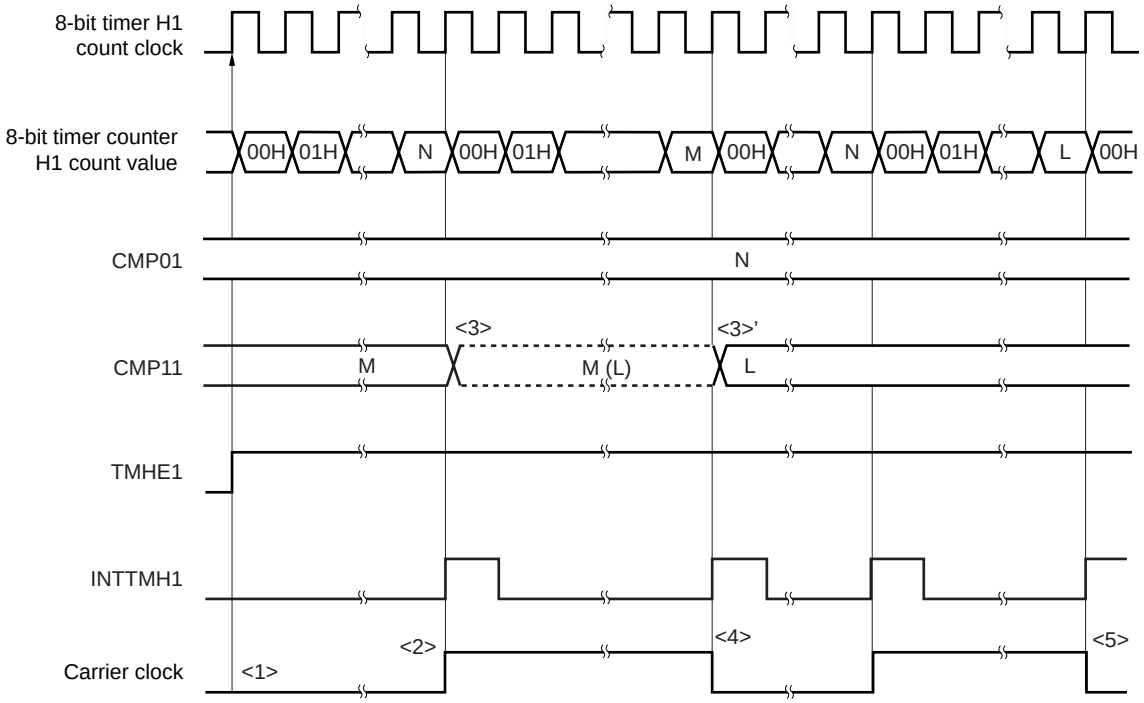
<6> A carrier signal is output at the first rising edge of the carrier clock if NRZ1 is set to 1.

<7> When NRZ1 = 0, the TOH1 output is held at the high level and is not changed to low level while the carrier clock is high level (from <6> and <7>, the high-level width of the carrier clock waveform is guaranteed).

Remark INTTM5H1 is an internal signal and not an interrupt source.

Figure 8-13. Carrier Generator Mode Operation Timing (3/3)

(c) Operation when CMP11 is changed



<1> When TMHE1 = 1 is set, the 8-bit timer H1 starts a count operation. At that time, the carrier clock remains default.

<2> When the count value of the 8-bit timer counter H1 matches the value of the CMP01 register, the INTTMH1 signal is output, the carrier signal is inverted, and the timer counter is cleared to 00H. At the same time, the compare register whose value is to be compared with that of the 8-bit timer counter H1 is changed from the CMP01 register to the CMP11 register.

<3> The CMP11 register is asynchronous to the count clock, and its value can be changed while the 8-bit timer H1 is operating. The new value (L) to which the value of the register is to be changed is latched. When the count value of the 8-bit timer counter H1 matches the value (M) of the CMP11 register before the change, the CMP11 register is changed (<3>').

However, it takes three count clocks or more since the value of the CMP11 register has been changed until the value is transferred to the register. Even if a match signal is generated before the duration of three count clocks elapses, the new value is not transferred to the register.

<4> When the count value of 8-bit timer counter H1 matches the value (M) of the CMP11 register before the change, the INTTMH1 signal is output, the carrier signal is inverted, and the timer counter is cleared to 00H. At the same time, the compare register whose value is to be compared with that of the 8-bit timer counter H1 is changed from the CMP11 register to the CMP01 register.

<5> The timing at which the count value of the 8-bit timer counter H1 and the CMP11 register value match again is indicated by the value after the change (L).

CHAPTER 9 WATCHDOG TIMER

9.1 Functions of Watchdog Timer

The watchdog timer operates on the internal low-speed oscillation clock.

The watchdog timer is used to detect an inadvertent program loop. If a program loop is detected, an internal reset signal is generated.

Program loop is detected in the following cases.

- If the watchdog timer counter overflows
- If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
- If data other than “ACH” is written to WDTE
- If data is written to WDTE during a window close period
- If the instruction is fetched from an area not set by the IMS register (detection of an invalid check while the CPU hangs up)
- If the CPU accesses an area that is not set by the IMS register (excluding FB00H to FFFFH) by executing a read/write instruction (detection of an abnormal access during a CPU program loop)

When a reset occurs due to the watchdog timer, bit 4 (WDTRF) of the reset control flag register (RESF) is set to 1. For details of RESF, refer to **CHAPTER 16 RESET FUNCTION**.

9.2 Configuration of Watchdog Timer

The watchdog timer includes the following hardware.

Table 9-1. Configuration of Watchdog Timer

Item	Configuration
Control register	Watchdog timer enable register (WDTE)

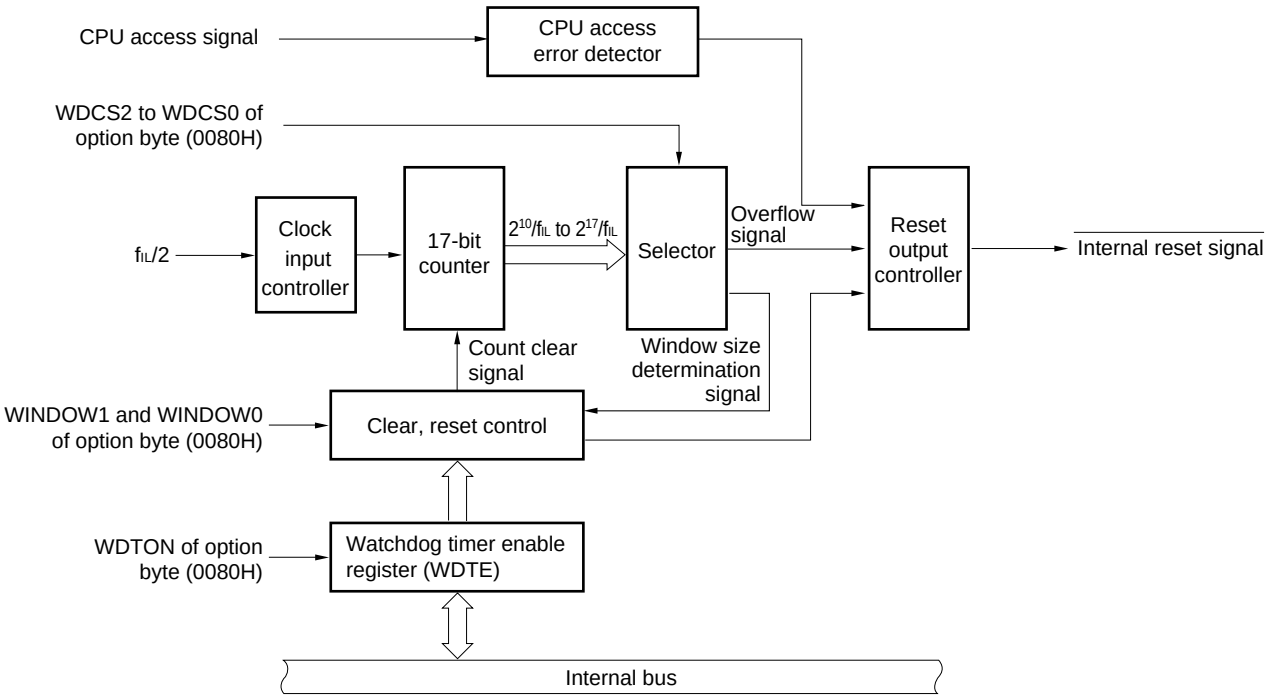
How the counter operation is controlled, overflow time, and window open period are set by the option byte.

Table 9-2. Setting of Option Bytes and Watchdog Timer

Setting of Watchdog Timer	Option Byte (0080H)
Window open period	Bits 6 and 5 (WINDOW1, WINDOW0)
Controlling counter operation of watchdog timer	Bit 4 (WDTON)
Overflow time of watchdog timer	Bits 3 to 1 (WDCS2 to WDCS0)

Remark For the option byte, refer to **CHAPTER 20 OPTION BYTE**.

Figure 9-1. Block Diagram of Watchdog Timer



9.3 Register Controlling Watchdog Timer

The watchdog timer is controlled by the watchdog timer enable register (WDTE).

(1) Watchdog timer enable register (WDTE)

Writing ACH to WDTE clears the watchdog timer counter and starts counting again.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 9AH or 1AH[Note].

Figure 9-2. Format of Watchdog Timer Enable Register (WDTE)

Address: FF99H After reset: 9AH/1AH[Note] R/W

Symbol	7	6	5	4	3	2	1	0
WDTE								

Note The WDTE reset value differs depending on the WDTON setting value of the option byte (0080H). To operate watchdog timer, set WDTON to 1.

WDTON Setting Value	WDTE Reset Value
0 (watchdog timer count operation disabled)	1AH
1 (watchdog timer count operation enabled)	9AH

Cautions 1. If a value other than ACH is written to WDTE, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.

2. If a 1-bit memory manipulation instruction is executed for WDTE, an internal reset signal is generated. If the source clock to the watchdog timer is stopped, however, an internal reset signal is generated when the source clock to the watchdog timer resumes operation.

3. The value read from WDTE is 9AH/1AH (this differs from the written value (ACH)).

9.4 Operation of Watchdog Timer

9.4.1 Controlling operation of watchdog timer

1. When the watchdog timer is used, its operation is specified by the option byte (0080H).

   - Enable counting operation of the watchdog timer by setting bit 4 (WDTON) of the option byte (0080H) to 1 (the counter starts operating after a reset release) (for details, refer to **CHAPTER 20**).

WDTON	Operation Control of Watchdog Timer Counter/Illegal Access Detection
0	Counter operation disabled (counting stopped after reset), illegal access detection operation disabled
1	Counter operation enabled (counting started after reset), illegal access detection operation enabled

   - Set an overflow time by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (0080H) (for details, refer to **9.4.2** and **CHAPTER 20**).
   - Set a window open period by using bits 6 and 5 (WINDOW1 and WINDOW0) of the option byte (0080H) (for details, refer to **9.4.3** and **CHAPTER 20**).

2. After a reset release, the watchdog timer starts counting.
3. By writing “ACH” to WDTE after the watchdog timer starts counting and before the overflow time set by the option byte, the watchdog timer is cleared and starts counting again.
4. After that, write WDTE the second time or later after a reset release during the window open period. If WDTE is written during a window close period, an internal reset signal is generated.
5. If the overflow time expires without “ACH” written to WDTE, an internal reset signal is generated.
   A internal reset signal is generated in the following cases.

   - If a 1-bit manipulation instruction is executed on the watchdog timer enable register (WDTE)
   - If data other than “ACH” is written to WDTE
   - If the instruction is fetched from an area not set by the IMS register (detection of an invalid check during a CPU program loop)
   - If the CPU accesses an area not set by the IMS register (excluding FB00H to FFFFH) by executing a read/write instruction (detection of an abnormal access during a CPU program loop)

Cautions 1. The first writing to WDTE after a reset release clears the watchdog timer, if it is made before the overflow time regardless of the timing of the writing, and the watchdog timer starts counting again.

2. If the watchdog timer is cleared by writing “ACH” to WDTE, the actual overflow time may be different from the overflow time set by the option byte by up to $2/f_{IL}$ seconds.

3. The watchdog timer can be cleared immediately before the count value overflows (FFFFH).

Cautions 4. The operation of the watchdog timer in the HALT and STOP modes differs as follows depending on the set value of bit 0 (LSROSC) of the option byte.

	LSROSC = 0 (Internal Low-Speed Oscillator Can Be Stopped by Software)	LSROSC = 1 (Internal Low-Speed Oscillator Cannot Be Stopped)
In HALT mode	Watchdog timer operation stops.	Watchdog timer operation continues.
In STOP mode		

If LSROSC = 0, the watchdog timer resumes counting after the HALT or STOP mode is released. At this time, the counter is not cleared to 0 but starts counting from the value at which it was stopped.

If oscillation of the internal low-speed oscillator is stopped by setting LSRSTOP (bit 1 of the internal oscillation mode register (RCM) = 1) when LSROSC = 0, the watchdog timer stops operating. At this time, the counter is not cleared to 0.

5. The watchdog timer continues its operation during self-programming of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

9.4.2 Setting overflow time of watchdog timer

Set the overflow time of the watchdog timer by using bits 3 to 1 (WDCS2 to WDCS0) of the option byte (0080H).

If an overflow occurs, an internal reset signal is generated. The present count is cleared and the watchdog timer starts counting again by writing “ACH” to WDTE during the window open period before the overflow time.

The following overflow time is set.

Table 9-3. Setting of Overflow Time of Watchdog Timer

WDCS2	WDCS1	WDCS0	Overflow Time of Watchdog Timer
0	0	0	$2^{10}/f_{IL}$ (3.88 ms)
0	0	1	$2^{11}/f_{IL}$ (7.76 ms)
0	1	0	$2^{12}/f_{IL}$ (15.52 ms)
0	1	1	$2^{13}/f_{IL}$ (31.03 ms)
1	0	0	$2^{14}/f_{IL}$ (62.06 ms)
1	0	1	$2^{15}/f_{IL}$ (124.12 ms)
1	1	0	$2^{16}/f_{IL}$ (248.24 ms)
1	1	1	$2^{17}/f_{IL}$ (496.48 ms)

Cautions 1. The combination of WDCS2 = WDCS1 = WDCS0 = 0 and WINDOW1 = WINDOW0 = 0 is prohibited.

2. The watchdog timer continues its operation during self-programming of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

Remarks 1. f_{IL}: Internal low-speed oscillation clock frequency

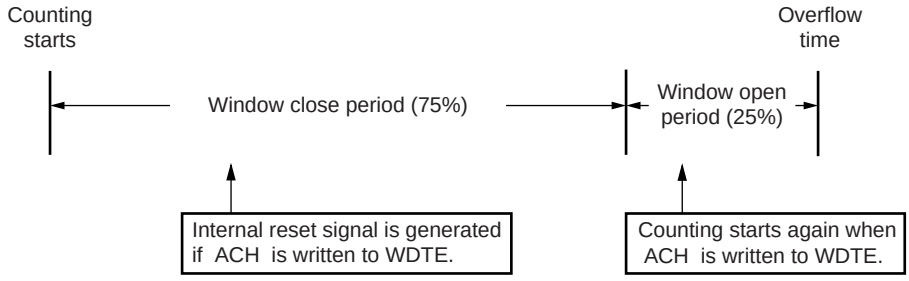
2. ( ): f_{IL} = 33 kHz (MAX.)

9.4.3 Setting window open period of watchdog timer

Set the window open period of the watchdog timer by using bits 6 and 5 (WINDOW1, WINDOW0) of the option byte (0080H). The outline of the window is as follows.

- If “ACH” is written to WDTE during the window open period, the watchdog timer is cleared and starts counting again.
- Even if “ACH” is written to WDTE during the window close period, an abnormality is detected and an internal reset signal is generated.

Example: If the window open period is 25%



Caution The first writing to WDTE after a reset release clears the watchdog timer, if it is made before the overflow time regardless of the timing of the writing, and the watchdog timer starts counting again.

The window open period to be set is as follows.

Table 9-4. Setting Window Open Period of Watchdog Timer

WINDOW1	WINDOW0	Window Open Period of Watchdog Timer
0	0	25%
0	1	50%
1	0	75%
1	1	100%

Cautions 1. The combination of WDCS2 = WDCS1 = WDCS0 = 0 and WINDOW1 = WINDOW0 = 0 is prohibited.

2. The watchdog timer continues its operation during self-programming of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

Remark If the overflow time is set to $2^{11}/f_{IL}$, the window close time and open time are as follows.

	Setting of Window Open Period			
	25%	50%	75%	100%
Window close time	0 to 7.11 ms	0 to 4.74 ms	0 to 2.37 ms	None
Window open time	7.11 to 7.76 ms	4.74 to 7.76 ms	2.37 to 7.76 ms	0 to 7.76 ms

<When window open period is 25%>

- Overflow time:
  $2^{11}/f_{IL}$ (MAX.) = 2^{11}/264 kHz (MAX.) = 7.76 ms
- Window close time:
  0 to $2^{11}/f_{IL}$ (MIN.) × (1 − 0.25) = 0 to 2^{11}/216 kHz (MIN.) × 0.75 = 0 to 7.11 ms
- Window open time:
  $2^{11}/f_{IL}$ (MIN.) × (1 − 0.25) to $2^{11}/f_{IL}$ (MAX.) = 2^{11}/216 kHz (MIN.) × 0.75 to 2^{11}/264 kHz (MAX.) = 7.11 to 7.76 ms

CHAPTER 10 A/D CONVERTER

10.1 Function of A/D Converter

The A/D converter converts an analog input signal into a digital value, and consists of up to 5 channels (ANI0 to ANI4) with a resolution of 8 bits.

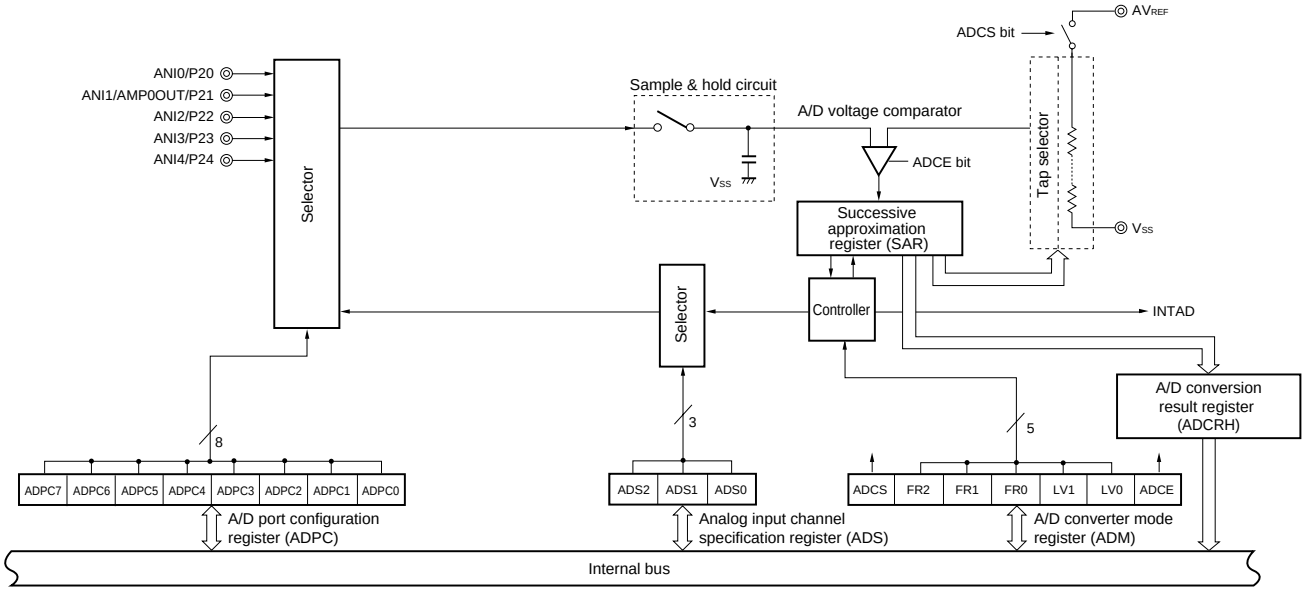
ANI1 function alternately as operational amplifier 0 output (AMP0OUT). This enables using operational amplifier 0 output as an analog input source.

The A/D converter has the following function.

- **8-bit resolution A/D conversion**

  8-bit resolution A/D conversion is carried out repeatedly for one analog input channel selected from ANI0 to ANI4, operational amplifier 0 output. Each time an A/D conversion operation ends, an interrupt request (INTAD) is generated.

Figure 10-1. Block Diagram of A/D Converter



Caution V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

10.2 Configuration of A/D Converter

The A/D converter includes the following hardware.

(1) ANI0 to ANI4 pins

These are the analog input pins of the 5-channel A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins.

(2) AMP0OUT pin

AMP0OUT is the output pin of operational amplifier 0.

This functions alternately as ANI1. The A/D converter can perform A/D conversion by selecting the output signal of operational amplifier 0 as the analog input source.

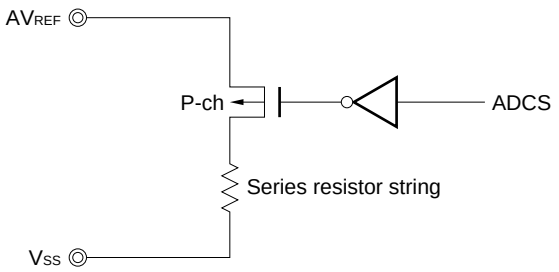
(3) Sample & hold circuit

The sample & hold circuit samples the input voltage of the analog input pin selected by the selector when A/D conversion is started, and holds the sampled voltage value during A/D conversion.

(4) Series resistor string

The series resistor string is connected between AV_{REF} and V_{SS}, and generates a voltage to be compared with the sampled voltage value.

Figure 10-2. Circuit Configuration of Series Resistor String



(5) Voltage comparator

The voltage comparator compares the sampled voltage value and the output voltage of the series resistor string.

(6) Successive approximation register (SAR)

This register converts the result of comparison by the voltage comparator, starting from the most significant bit (MSB). When the voltage value is converted into a digital value down to the least significant bit (LSB) (end of A/D conversion), the contents of the SAR register are transferred to the A/D conversion result register (ADCR).

(7) 8-bit A/D conversion result register H (ADCRH)

The A/D conversion result is loaded from the successive approximation register to this register each time A/D conversion is completed, and the ADCRH register stores the A/D conversion result.

Caution When data is read from ADCRH, a wait cycle is generated. Do not read data from ADCRH when the peripheral hardware clock (f_{PRS}) is stopped. For details, refer to CHAPTER 26 CAUTIONS FOR WAIT.

(8) Controller

This circuit controls the conversion time of an input analog signal that is to be converted into a digital signal, as well as starting and stopping of the conversion operation. When A/D conversion has been completed, this controller generates INTAD.

(9) AV_{REF} pin

This pin inputs an analog power/reference voltage to the A/D converter. Make this pin the same potential as the V_{DD} pin when port 2 is used as a digital port.

The signal input to ANI0 to ANI4 is converted into a digital signal, based on the voltage applied across AV_{REF} and V_{SS}.

(10) V_{SS} pin

This is the ground potential pin. V_{SS} functions alternately as the ground potential of the A/D converter. Be sure to connect V_{SS} to a stabilized GND (= 0 V).

10.3 Registers Used in A/D Converter

The A/D converter uses the following five registers.

- A/D converter mode register (ADM)
- 8-bit A/D conversion result register H (ADCRH)
- Analog input channel specification register (ADS)
- A/D port configuration register (ADPC)
- Port mode register 2 (PM2)

(1) A/D converter mode register (ADM)

This register sets the conversion time for analog input to be A/D converted, and starts/stops conversion.

ADM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-3. Format of A/D Converter Mode Register (ADM)

Address: FF90H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	<0>
ADM	ADCS	0	FR2Note 1	FR1Note 1	FR0Note 1	LV1Note 1	LV0Note 1	ADCE

ADCS	A/D conversion operation control
0	Stops conversion operation
1	Enables conversion operation

ADCE	Voltage comparator operation controlNote 2
0	Stops voltage comparator operation
1	Enables voltage comparator operation

Notes 1. For details of FR2 to FR0, LV1, LV0, and A/D conversion, refer to **Table 10-2 A/D Conversion Time Selection**.

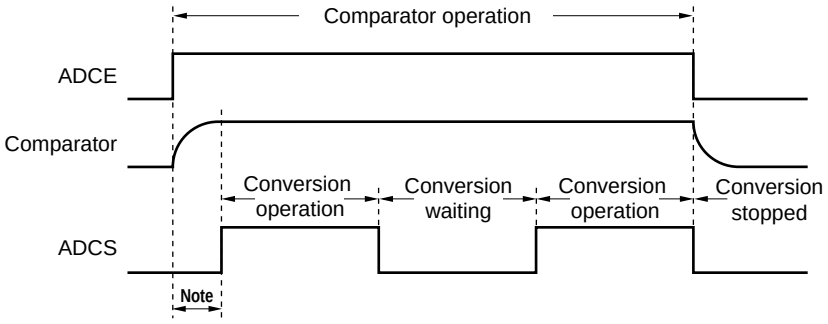
2. The operation of the voltage comparator is controlled by ADCS and ADCE, and it takes 1 µs from operation start to operation stabilization. Therefore, when ADCS is set to 1 after 1 µs or more has elapsed from the time ADCE is set to 1, the conversion result at that time has priority over the first conversion result. Otherwise, ignore data of the first conversion.

Table 10-1. Settings of ADCS and ADCE

ADCS	ADCE	A/D Conversion Operation
0	0	Stop status (DC power consumption path does not exist)
0	1	Conversion waiting mode (only voltage comparator consumes power)
1	0	Conversion mode (comparator operation is stoppedNote)
1	1	Conversion mode (voltage comparator operation)

Note Ignore the first conversion data.

Figure 10-4. Timing Chart When Comparator Is Used



Note To stabilize the internal circuit, the time from setting ADCE to 1 to setting ADCS to 1 must be 1 μs or longer.

Cautions 1. A/D conversion must be stopped before rewriting bits FR0 to FR2, LV1, and LV0 to values other than the identical data.

2. If data is written to ADM, a wait cycle is generated. Do not write data to ADM when the peripheral hardware clock (f_{PRS}) is stopped. For details, refer to CHAPTER 26 CAUTIONS FOR WAIT.

Table 10-2. A/D Conversion Time Selection

(1) 2.7 V ≤ AV_{REF} ≤ 5.5 V (LV0 = 0)

A/D Converter Mode Register (ADM)					Conversion Time Selection			Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{PRS} = 2 MHz	f_{PRS} = 10 MHz	
0	0	0	0	0	264/f_{PRS}	Setting prohibited	26.4 µs	f_{PRS}/12
0	0	1	0	0	176/f_{PRS}		17.6 µs	f_{PRS}/8
0	1	0	0	0	132/f_{PRS}		13.2 µs	f_{PRS}/6
0	1	1	0	0	88/f_{PRS}		8.8 µs Note	f_{PRS}/4
1	0	0	0	0	66/f_{PRS}	33.0 µs	6.6 µs Note	f_{PRS}/3
1	0	1	0	0	44/f_{PRS}	22.0 µs	Setting prohibited	f_{PRS}/2
Other than above								

Note This can only be set when 4.0 V ≤ AV_{REF} ≤ 5.5 V.

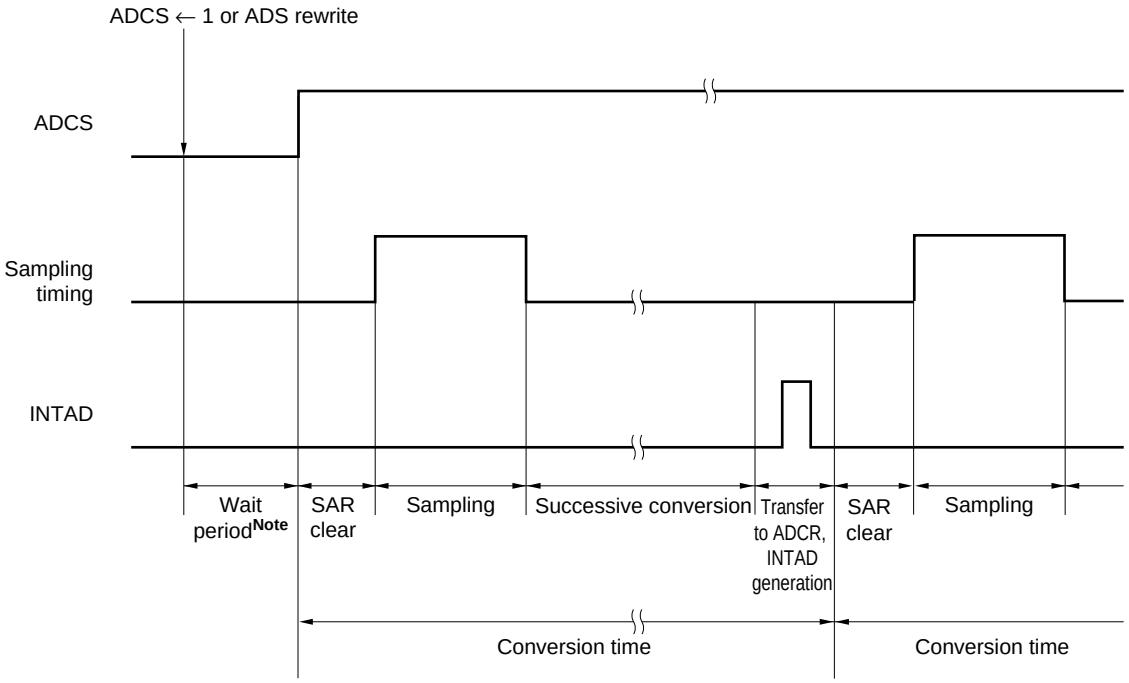
Cautions 1. Specify the conversion time so that the following conditions are satisfied:
When 4.0 V ≤ AV_{REF} ≤ 5.5 V: f_{AD} = 0.6 V to 3.6 MHz
When 2.7 V ≤ AV_{REF} < 4.0 V: f_{AD} = 0.6 V to 1.8 MHz

2. When rewriting FR2 to FR0, LV1, and LV0 to other than the same data, stop A/D conversion once (ADCS = 0) beforehand.

3. The above conversion time does not include clock frequency errors. Select conversion time, taking clock frequency errors into consideration.

Remark f_{PRS}: Peripheral hardware clock frequency

Figure 10-5. A/D Converter Sampling and A/D Conversion Timing



Note For details of wait period, refer to **CHAPTER 26 CAUTIONS FOR WAIT**.

(2) 8-bit A/D conversion result register H (ADCRH)

This register is an 8-bit register that stores the A/D conversion result.

ADCRH can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-6. Format of 8-Bit A/D Conversion Result Register (ADCRH)

Address: FF09H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ADCRH								

Cautions 1. When writing to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using timing other than the above may cause an incorrect conversion result to be read.

2. If data is read from ADCRH, a wait cycle is generated. Do not read data from ADCRH when the peripheral hardware clock (f_{PRS}) is stopped. For details, refer to CHAPTER 26 CAUTIONS FOR WAIT.

(3) Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

ADS can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 10-7. Format of Analog Input Channel Specification Register (ADS)

Address: FF0EH After reset: 00H R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
ADS	0	0	0	0	0	ADS2	ADS1	ADS0

ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	ANI0	P20/ANI0 pin
0	0	1	ANI1	P21/ANI1 pin or operational amplifier 0 output signal
0	1	0	ANI2	P22/ANI2 pin
0	1	1	ANI3	P23/ANI3 pin
1	0	0	ANI4	P24/ANI4 pin
Other than above			Setting prohibited	

Cautions 1. Be sure to clear bits 3 to 7 to "0".

2. Set a channel to be used for A/D conversion in the input mode by using port mode register 2 (PM2).

3. If data is written to ADS, a wait cycle is generated. Do not write data to ADS when the peripheral hardware clock (f_{PRS}) is stopped. For details, refer to CHAPTER 26 CAUTIONS FOR WAIT.

(4) A/D port configuration register (ADPC)

ADPC switches the P20/AMP0-/ANI0 to P24/ANI4 pins to digital I/O or analog I/O of port. Each bit of ADPC corresponds to a pin of port 2 and can be specified in 1-bit units.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears ADPC to 00H.

Figure 10-8. Format of A/D Port Configuration Register (ADPC)

Address: FF97H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	ADPC7	ADPC6	ADPC5	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0

ADPCn	Digital I/O or analog I/O selection (n = 0 to 7)
0	Analog I/O
1	Digital I/O

Cautions 1. Set the pin set to analog I/O to the input mode by using port mode register 2 (PM2).

2. If data is written to ADPC, a wait cycle is generated. Do not write data to ADPC when the peripheral hardware clock is stopped. For details, refer to CHAPTER 26 CAUTIONS FOR WAIT.

(5) Port mode register (PM2)

When using the ANI0/AMP0-/P20 to ANI4/P24 pins for analog input port, set PM20 to PM24 to 1. The output latches of P20 to P24 at this time may be 0 or 1.

If PM20 to PM24 are set to 0, they cannot be used as analog input port pins.

PM2 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 10-9. Format of Port Mode Register 2 (PM2)

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

PM2n	P2n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

When using P20/AMP0-/ANI0 to P24/ANI4, set the registers according to the pin function to be used (refer to **Tables 10-3** to **10-5**).

Table 10-3. Setting Functions of P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins

ADPC Register	PM2 Register	OPAMP0E bit	ADS Register (n = 0, 2)	P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins
Analog input selection	Input mode	0	Selects ANIn.	Analog input (to be converted into digital signals)
			Does not select ANIn.	Analog input (not to be converted into digital signals)
		1	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Operational amplifier 0 input
	Output mode	–	–	Setting prohibited
Digital I/O selection	Input mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital input
	Output mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital output

Remark ADPC: A/D port configuration register
PM2: Port mode register 2
OPAMP0E: Bit 7 of operational amplifier control register (AMPM)
ADS: Analog input channel specification register

Table 10-4. Setting Functions of P21/ANI1/AMP0OUT Pin

ADPC Register	PM2 Register	OPAMP0E bit	ADS Register	P21/ANI1/AMP0OUT Pin
Analog I/O selection	Input mode	0	Selects ANI1.	Analog input (to be converted into digital signals)
			Does not select ANI1.	Analog input (not to be converted into digital signals)
		1	Selects ANI1.	Operational amplifier 0 output (to be converted into digital signals)
			Does not select ANI1.	Operational amplifier 0 output (not to be converted into digital signals)
	Output mode	–		Setting prohibited
Digital I/O selection	Input mode	0	Selects ANI1.	Setting prohibited
			Does not select ANI1.	Digital input
		1	–	Setting prohibited
	Output mode	0	Selects ANI1.	Setting prohibited
			Does not select ANI1.	Digital output
		1	–	Setting prohibited

Table 10-5. Setting Functions of P23/ANI3 to P24/ANI4 Pins

ADPC Register	PM2 Register	ADS Register (n = 3, 4)	P23/ANI3 to P24/ANI4 Pins
Analog input selection	Input mode	Selects ANIn.	Analog input (to be converted into digital signals)
		Does not select ANIn.	Analog input (not to be converted into digital signals)
	Output mode	–	Setting prohibited
Digital I/O selection	Input mode	Selects ANIn.	Setting prohibited
		Does not select ANIn.	Digital input
	Output mode	Selects ANIn.	Setting prohibited
		Does not select ANIn.	Digital output

Remark ADPC: A/D port configuration register
PM2: Port mode register 2
OPAMP0E: Bit 7 of operational amplifier control register (AMPM)
ADS: Analog input channel specification register

10.4 A/D Converter Operations

10.4.1 Basic operations of A/D converter

<1> Set the A/D conversion time and the operation mode by using bits 5 to 1 (FR2 to FR0, LV1, and LV0) of the A/D converter mode register (ADM).

<2> Set bit 0 (ADCE) of ADM to 1 to start the operation of the voltage comparator.

<3> Set channels for A/D conversion to analog I/O by using the A/D port configuration register (ADPC) and set to input mode by using port mode register 2 (PM2).

<4> Select one channel for A/D conversion by using the analog input channel specification register (ADS).

<5> Start the conversion operation by setting bit 7 (ADCS) of ADM to 1.
(<6> to <13> are operations performed by hardware.)

<6> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.

<7> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the sampled voltage is held until the A/D conversion operation has ended.

<8> Bit 7 of the successive approximation register (SAR) is set. The series resistor string voltage tap is set to (1/2) AV_{REF} by the tap selector

<9> The voltage difference between the series resistor string voltage tap and sampled voltage is compared by the voltage comparator. If the analog input is greater than (1/2) AV_{REF}, the MSB of SAR remains set to 1. If the analog input is smaller than (1/2) AV_{REF}, the MSB is reset to 0.

<10> Next, bit 6 of SAR is automatically set to 1, and the operation proceeds to the next comparison. The series resistor string voltage tap is selected according to the preset value of bit 6, as described below.

- Bit 7 = 1: (3/4) AV_{REF}
- Bit 7 = 0: (1/4) AV_{REF}

The voltage tap and sampled voltage are compared and bit 6 of SAR is manipulated as follows.

- Analog input voltage ≥ Voltage tap: Bit 6 = 1
- Analog input voltage < Voltage tap: Bit 6 = 0

<11> Comparison is continued in this way up to bit 0 of SAR.

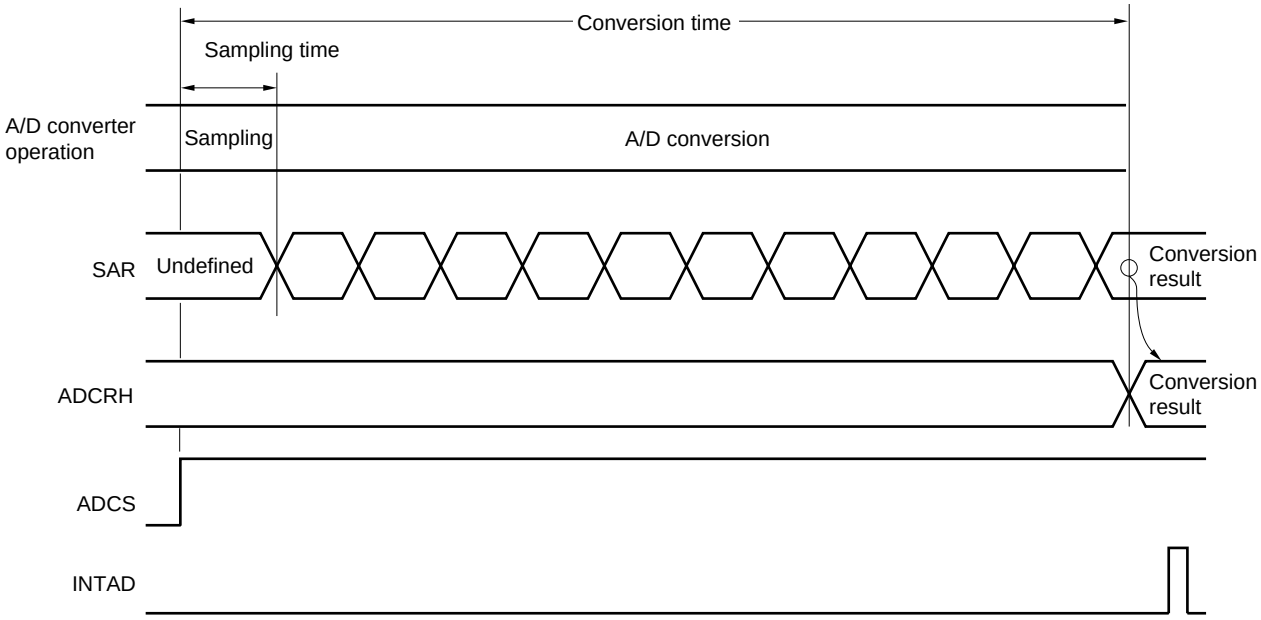
<12> Upon completion of the comparison of 8 bits, an effective digital result value remains in SAR, and the result value is transferred to the A/D conversion result register (ADCRH) and then latched.
At the same time, the A/D conversion end interrupt request (INTAD) can also be generated.

<13> Repeat steps <6> to <12>, until ADCS is cleared to 0.
To stop the A/D converter, clear ADCS to 0.
To restart A/D conversion from the status of ADCE = 1, start from <5>. To start A/D conversion again when ADCE = 0, set ADCE to 1, wait for 1 µs or longer, and start <5>. To change a channel of A/D conversion, start from <4>.

Cautions 1. Make sure the period of <2> to <5> is 1 µs or more.

2. If the timing of <2> is earlier than that of <4>, <2> may be performed any time.

Figure 10-10. Basic Operation of A/D Converter



A/D conversion operations are performed continuously until bit 7 (ADCS) of the A/D converter mode register (ADM) is reset (0) by software.

If a write operation is performed to the analog input channel specification register (ADS) during an A/D conversion operation, the conversion operation is initialized, and if the ADCS bit is set (1), conversion starts again from the beginning.

Reset signal generation clears the A/D conversion result register (ADCRH) to 00H.

10.4.2 Input voltage and conversion results

The relationship between the analog input voltage input to the analog input pins (ANI0 to ANI4) and the theoretical A/D conversion result (stored in the 8-bit A/D conversion result register (ADCRH)) is shown by the following expression.

$$ADCR = INT\left(\frac{V_{AIN}}{AV_{REF}} \times 256 + 0.5\right)$$

or

$$(ADCR - 0.5) \times \frac{AV_{REF}}{256} \leq V_{AIN} < (ADCR + 0.5) \times \frac{AV_{REF}}{256}$$

where, INT( ): Function which returns integer part of value in parentheses

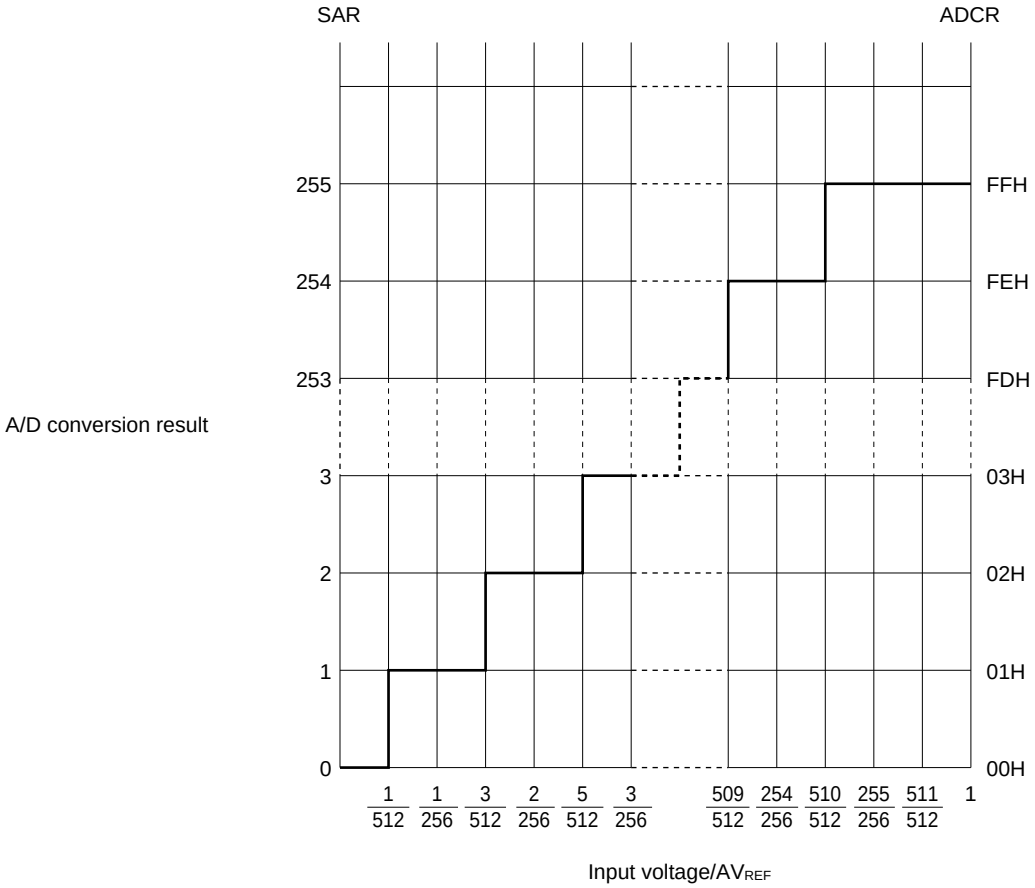
V_{AIN}: Analog input voltage

AV_{REF}: AV_{REF} pin voltage

ADCR: 8-bit A/D conversion result register (ADCRH) value

Figure 10-11 shows the relationship between the analog input voltage and the A/D conversion result.

Figure 10-11. Relationship between Analog Input Voltage and A/D Conversion Result



10.4.3 A/D converter operation mode

One channel of analog input is selected from ANI0 to ANI14 by the analog input channel specification register (ADS) and A/D conversion is executed.

(1) A/D conversion operation

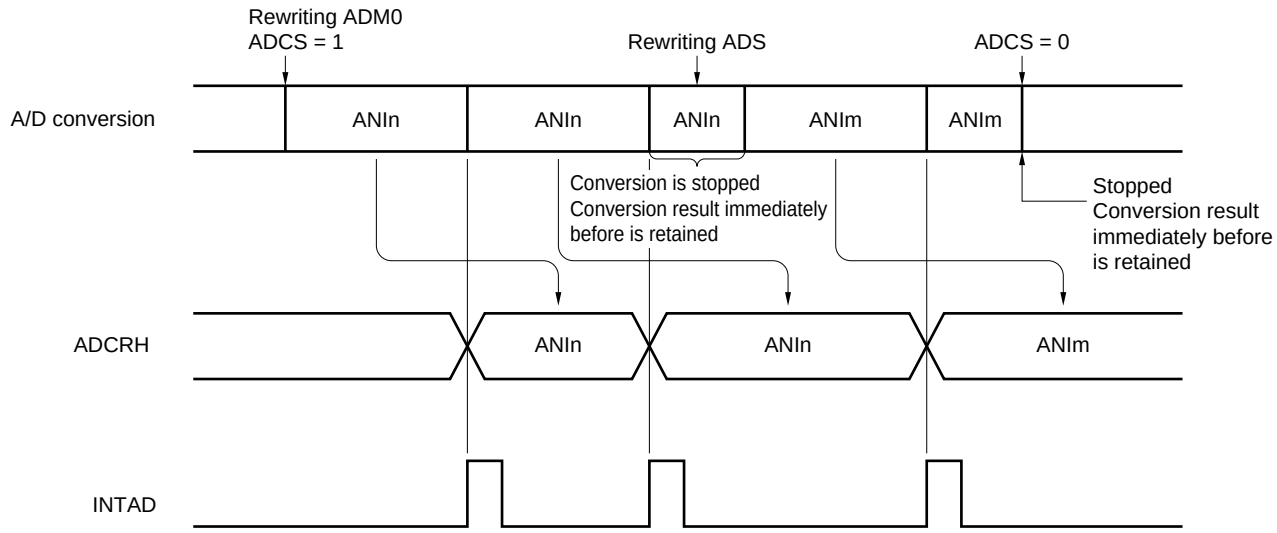
By setting bit 7 (ADCS) of the A/D converter mode register (ADM) to 1, the A/D conversion operation of the voltage, which is applied to the analog input pin specified by the analog input channel specification register (ADS), is started.

When A/D conversion has been completed, the result of the A/D conversion is stored in the A/D conversion result register (ADCRH), and an interrupt request signal (INTAD) is generated. When one A/D conversion has been completed, the next A/D conversion operation is immediately started.

If ADS is rewritten during A/D conversion, the A/D conversion operation under execution is stopped and restarted from the beginning.

If 0 is written to ADCS during A/D conversion, A/D conversion is immediately stopped. At this time, the conversion result immediately before is retained.

Figure 10-12. A/D Conversion Operation



Remarks 1. n = 0 to 4

2. m = 0 to 4

The setting methods are described below.

<1> Set the A/D conversion time and the operation mode by using bits 5 to 1 (FR2 to FR0, LV1, and LV0) of the A/D converter mode register (ADM).
<2> Set bit 0 (ADCE) of ADM to 1.
<3> Set the channel to be used to analog input by using the A/D port configuration register (ADPC) and port mode register 2 (PM2).
<4> Select a channel to be used by using the analog input channel specification register (ADS).
<5> Set bit 7 (ADCS) of ADM to 1 to start A/D conversion.
<6> When one A/D conversion has been completed, an interrupt request signal (INTAD) is generated.
<7> Transfer the A/D conversion data to the A/D conversion result register (ADCRH).

<Change the channel>

<8> Set bit 0 (ADMK) of the interrupt mask flag register 1L (MK1L) to 1[Note].
<9> Change the channel by using ADS to start A/D conversion.
<10> Clear bit 0 (ADIF) of the interrupt request flag register 1L (IF1L) to 0.
<11> Clear ADMK to 0[Note].
<12> When one A/D conversion has been completed, an interrupt request signal (INTAD) is generated.
<13> Transfer the A/D conversion data to the A/D conversion result register (ADCRH).

<Complete A/D conversion>

<14> Clear ADCS to 0.
<15> Clear ADCE to 0.

Note Execute this only if interrupt servicing is used for A/D conversion.

Cautions 1. Make sure the period of <2> to <5> is 1 μs or more.
2. If the timing of <2> is earlier than that of <4>, <2> may be performed any time.
3. <2> can be omitted. However, ignore data of the first conversion after <5> in this case.
4. The period from <6> to <12> differs from the conversion time set using bits 5 to 1 (FR2 to FR0, LV1, LV0) of ADM. The period from <9> to <12> is the conversion time set using FR2 to FR0, LV1, and LV0.

10.5 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1LSB (Least Significant Bit). The percentage of 1LSB with respect to the full scale is expressed by %FSR (Full Scale Range).

1LSB is as follows when the resolution is 8 bits.

$1LSB = 1/2^8 = 1/256$
$= 0.391\%FSR$

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.
Zero-scale error, full-scale error, integral linearity error, and differential linearity errors that are combinations of these express the overall error.
Note that the quantization error is not included in the overall error in the characteristics table.

(3) Quantization error

When analog values are converted to digital values, a ±1/2LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of ±1/2LSB is converted to the same digital code, so a quantization error cannot be avoided.
Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

Figure 10-13. Overall Error

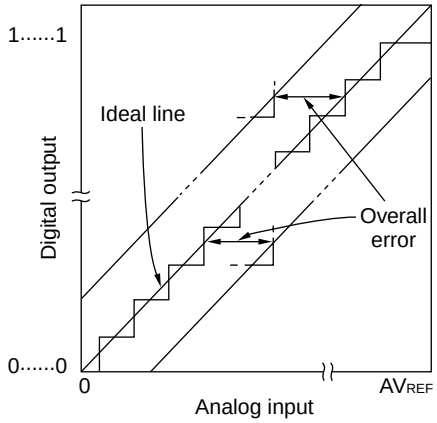
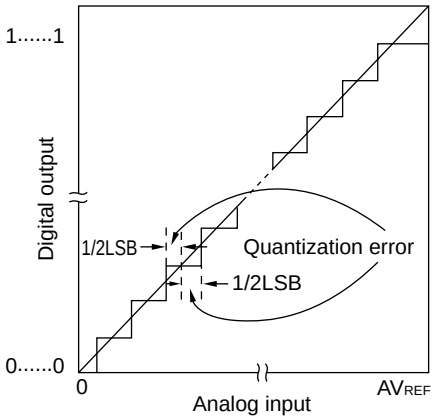


Figure 10-14. Quantization Error



(4) Zero-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (1/2LSB) when the digital output changes from 0.....000 to 0.....001.
If the actual measurement value is greater than the theoretical value, it shows the difference between the actual measurement value of the analog input voltage and the theoretical value (3/2LSB) when the digital output changes from 0……001 to 0……010.

(5) Full-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (Full-scale – 3/2LSB) when the digital output changes from 1.....110 to 1.....111.

(6) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

(7) Differential linearity error

While the ideal width of code output is 1LSB, this indicates the difference between the actual measurement value and the ideal value.

Figure 10-15. Zero-Scale Error

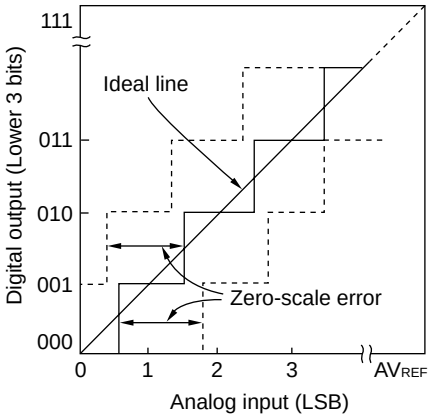


Figure 10-16. Full-Scale Error

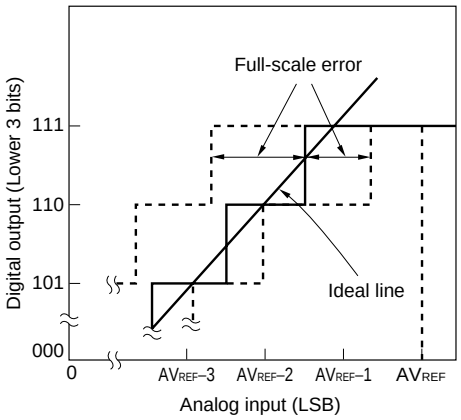


Figure 10-17. Integral Linearity Error

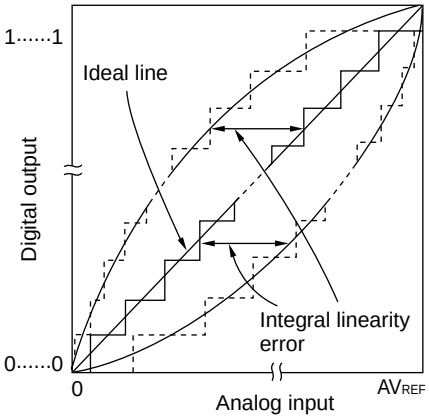
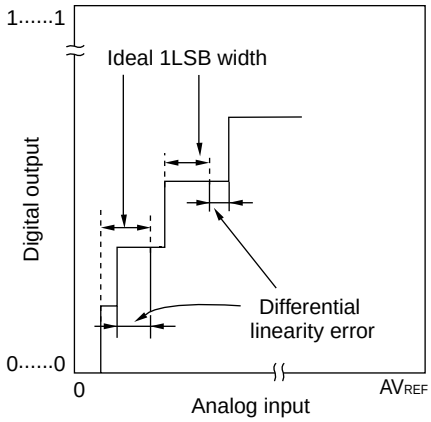


Figure 10-18. Differential Linearity Error



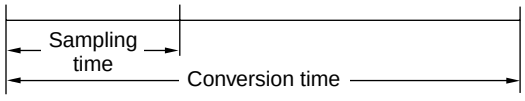
(8) Conversion time

This expresses the time from the start of sampling to when the digital output is obtained.

The sampling time is included in the conversion time in the characteristics table.

(9) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.



10.6 Cautions for A/D Converter

(1) Operating current in STOP mode

To satisfy the DC characteristics of the power supply current in STOP mode, clear bits 7 (ADCS) and 0 (ADCE) of A/D converter mode register (ADM) to 0 before executing a STOP instruction.

To restart from the standby status, clear bit 0 (ADIF) of interrupt request flag register 1L (IF1L) to 0 and start operation.

(2) Input range of ANI0 to ANI4

Observe the rated range of the ANI0 to ANI4 input voltage. If a voltage of AV_{REF} or higher and V_{SS} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

(3) Conflicting operations

<1> Conflict between A/D conversion result register (ADCRH) write and ADCRH read by instruction upon the end of conversion

ADCRH read has priority. After the read operation, the new conversion result is written to ADCRH.

<2> Conflict between ADCRH write and A/D converter mode register (ADM) write, analog input channel specification register (ADS), or A/D port configuration register (ADPC) write upon the end of conversion

ADM, ADS, or ADPC write has priority. ADCRH write is not performed, nor is the conversion end interrupt signal (INTAD) generated.

(4) Noise countermeasures

To maintain the 8-bit resolution, attention must be paid to noise input to the AV_{REF} pin and pins ANI0 to ANI4.

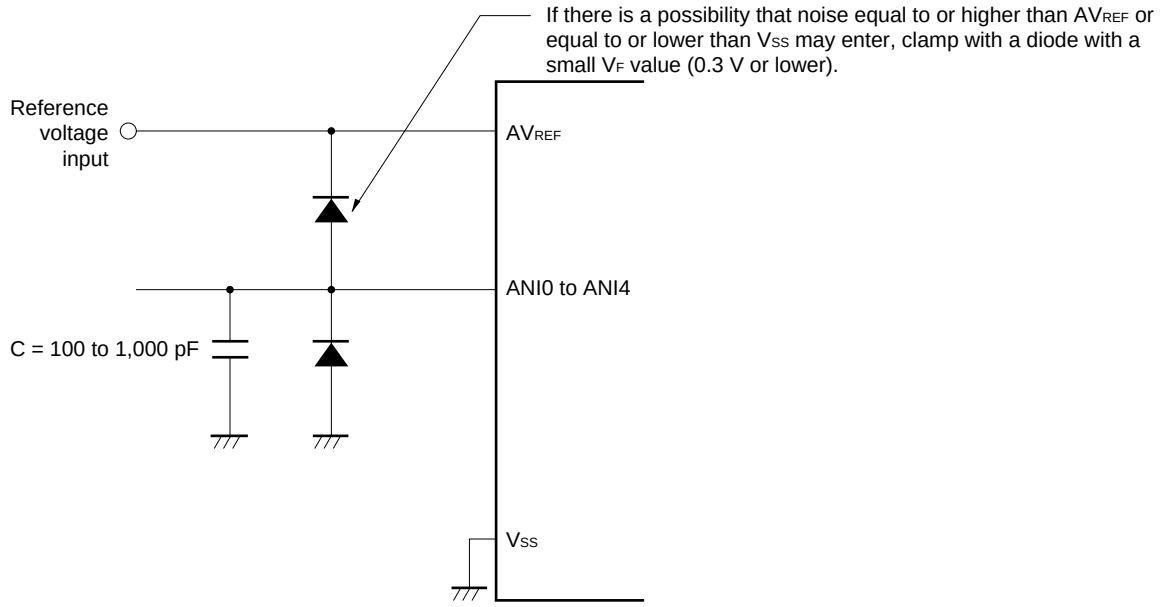
<1> Connect a capacitor with a low equivalent resistance and a good frequency response to the power supply.

<2> The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting external C as shown in Figure 10-19 is recommended.

<3> Do not switch these pins with other pins during conversion.

<4> The accuracy is improved if the HALT mode is set immediately after the start of conversion.

Figure 10-19. Analog Input Pin Connection



(5) ANI0/P20 to ANI4/P24

<1> The analog input pins (ANI0 to ANI4) are also used as digital I/O port pins (P20 to P24). When A/D conversion is performed with any of ANI0 to ANI4 selected, do not access P20 to P24 while conversion is in progress; otherwise the conversion resolution may be degraded.

<2> To use the ANI0/P20 to ANI4/P24 pins for digital I/O port, it is recommended to use starting with the furthest pin from AV_{REF} (ANI4/P24 pin). To use these pins as analog input, it is recommended to use starting with the closest pin to V_{SS} (ANI0/P20 pin).

<3> If a digital pulse is applied to the pins adjacent to the pins currently used for A/D conversion, the expected value of the A/D conversion may not be obtained due to coupling noise. Therefore, do not apply a pulse to the pins adjacent to the pin undergoing A/D conversion.

(6) Input impedance of ANI0 to ANI4 pins

This A/D converter charges a sampling capacitor for sampling during sampling time.

Therefore, only a leakage current flow when sampling is not in progress, and a current that charges the capacitor flows during sampling. Consequently, the input impedance fluctuates depending on whether sampling is in progress, and on the other states.

To make sure that sampling is effective, however, it is recommended to keep the output impedance of the analog input source to within 10 kΩ, and to connect a capacitor of about 100 pF to the ANI0 to ANI4 pins (refer to **Figure 10-19**).

(7) AV_{REF} pin input impedance

A series resistor string of several tens of kΩ is connected between the AV_{REF} and V_{SS} pins.

Therefore, if the output impedance of the reference voltage source is high, this will result in a series connection to the series resistor string between the AV_{REF} and V_{SS} pins, resulting in a large reference voltage error.

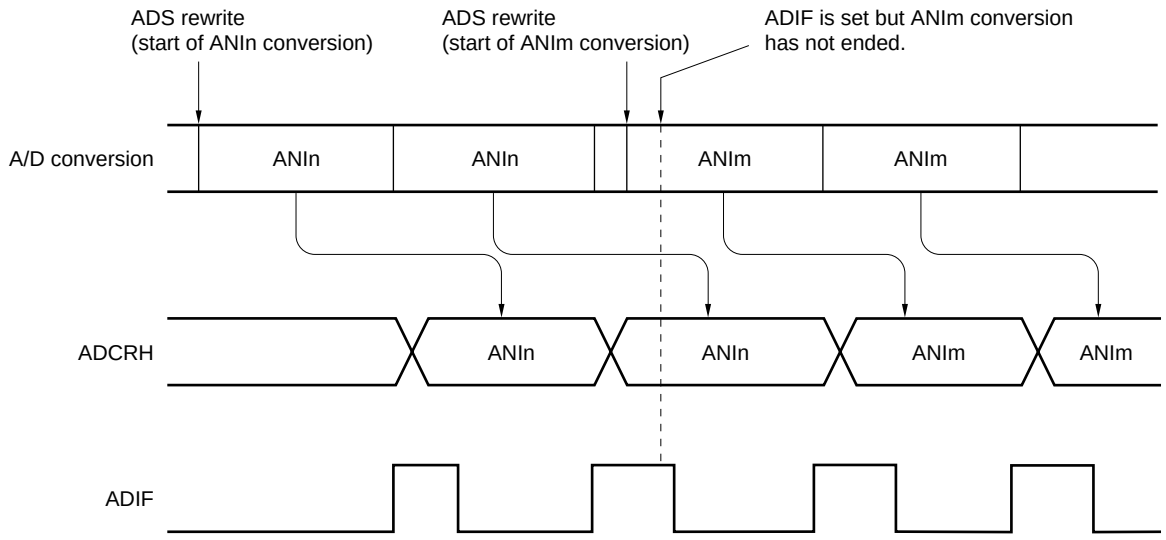
(8) Interrupt request flag (ADIF)

The interrupt request flag (ADIF) is not cleared even if the analog input channel specification register (ADS) is changed.

Therefore, if an analog input pin is changed during A/D conversion, the A/D conversion result and ADIF for the pre-change analog input may be set just before the ADS rewrite. Caution is therefore required since, at this time, when ADIF is read immediately after the ADS rewrite, ADIF is set despite the fact A/D conversion for the post-change analog input has not ended.

When A/D conversion is stopped and then resumed, clear ADIF before the A/D conversion operation is resumed.

Figure 10-20. Timing of A/D Conversion End Interrupt Request Generation



Remarks 1. n = 0 to 4

2. m = 0 to 4

(9) Conversion results just after A/D conversion start

The first A/D conversion value immediately after A/D conversion starts may not fall within the rating range if the ADCS bit is set to 1 within 1 μs after the ADCE bit was set to 1, or if the ADCS bit is set to 1 with the ADCE bit = 0. Take measures such as polling the A/D conversion end interrupt request (INTAD) and removing the first conversion result.

(10) A/D conversion result register (ADCRH) read operation

When a write operation is performed to the A/D converter mode register (ADM), analog input channel specification register (ADS), and A/D port configuration register (ADPC), the contents of ADCRH may become undefined. Read the conversion result following conversion completion before writing to ADM, ADS, and ADPC. Using a timing other than the above may cause an incorrect conversion result to be read.

(11) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 10-21. Internal Equivalent Circuit of ANIn Pin

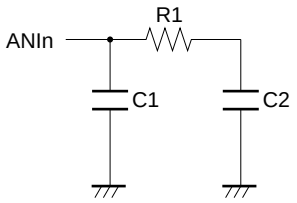


Table 10-6. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

AV_{REF}	R1	C1	C2
$2.7\ V \leq AV_{REF} \leq 5.5\ V$	11.5 kΩ	8.0 pF	8.0 pF

Remarks 1. The resistance and capacitance values shown in Table 10-6 are not guaranteed values.

2. n = 0 to 4

CHAPTER 11 OPERATIONAL AMPLIFIERS

11.1 Function of Operational Amplifier

Operational amplifiers 0 and 1 are mounted onto products with operational amplifier of the μPD79F7023, 79F7024.

Operational amplifiers 0 and 1 both have two input pins (the AMPn- pin and the AMPn+ pin) and one output pin (the AMPnOUT pin), and can be used as single-power supply amplifiers that can be externally connected.

The amplified voltage can be used as an analog input of the A/D converter, because the AMP0OUT pin is alternatively used with analog input pin of the A/D converter.

Remark n = 0, 1

11.2 Configuration of Operational Amplifier

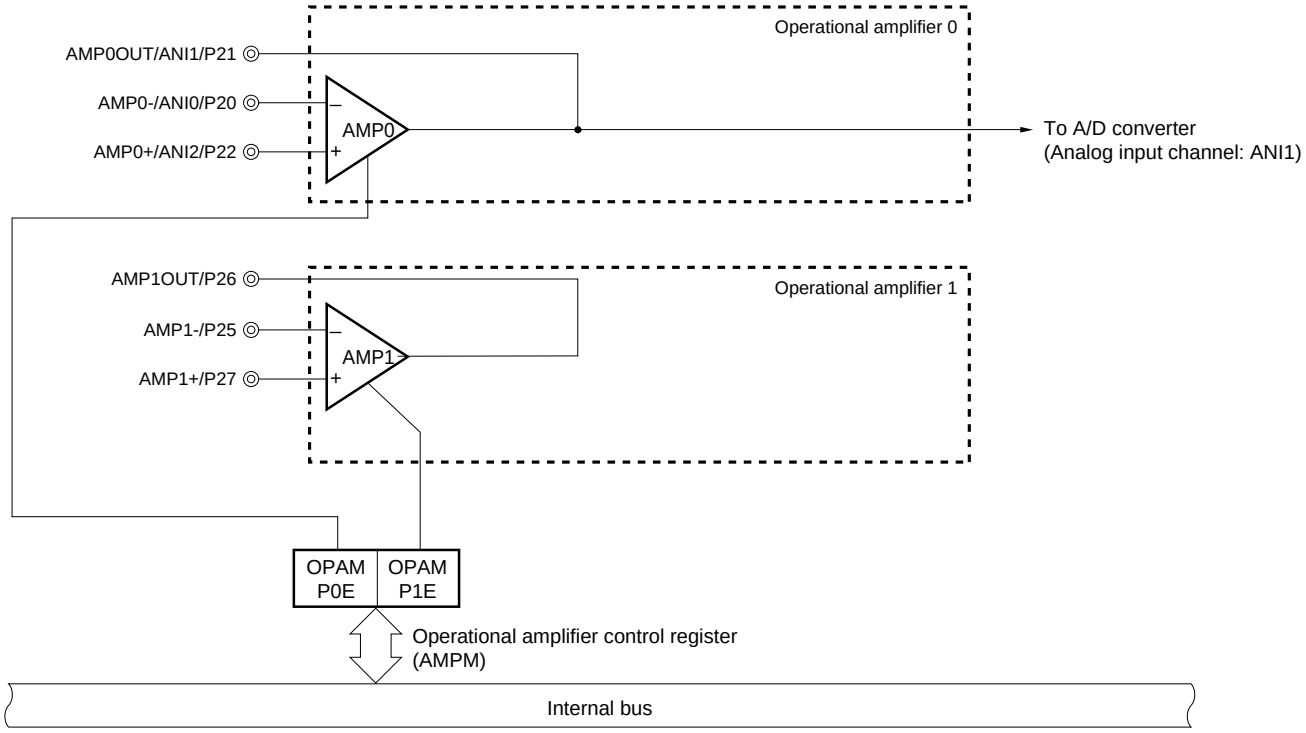
The operational amplifiers consist of the following hardware.

Table 11-1. Configuration of Operational Amplifier

Item	Configuration
Operational amplifier input	AMPn– pin, AMPn+ pin
Operational amplifier output	AMPnOUT pin
Control registers	Operational amplifier control register (AMPM) A/D configuration register (ADPC) Analog input channel specification register (ADS) Port mode register 2 (PM2)

Remark n = 0, 1

Figure 11-1. Block Diagram of Operational Amplifier



11.3 Registers Used in Operational Amplifier

The operational amplifiers use the following four registers.

- Operational amplifier control register (AMPM)
- A/D port configuration register (ADPC)
- Analog input channel specification register (ADS)
- Port mode register 2 (PM2)

(1) Operational amplifier control register (AMPM)

This register controls the operations of operational amplifiers 0 and 1.

AMPM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11-2. Format of Operational Amplifier Control Register (AMPM)

Address: FF60H After reset: 00H R/W

Symbol	<7>	6	5	4	<3>	2	1	0
AMPM	OPAMP0E	0	0	0	OPAMP1E	0	0	0

OPAMP0E	Operational amplifier 0 operation control
0	Stops operational amplifier 0 operation
1	Enables operational amplifier 0 operation

Caution When using as digital inputs the pins of port 2, which are not used with the operational amplifier 0, when the operational amplifier 0 is used, make sure that the input levels of digital input ports are fixed to prevent degradation of the A/D conversion resolution.

OPAMP1E	Operational amplifier 1 operation control
0	Stops operational amplifier 1 operation
1	Enables operational amplifier 1 operation

(2) A/D port configuration register (ADPC)

ADPC switches the P20/AMP0-/ANI0 to P24/ANI4 pins to digital I/O or analog I/O of port. Each bit of ADPC corresponds to a pin of port 2 and can be specified in 1-bit units.

Reset signal generation clears ADPC to 00H.

Figure 11-4. Format of A/D Port Configuration Register (ADPC)

Address: FF97H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	ADPC7	ADPC6	ADPC5	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0

ADPCn	Digital I/O or analog I/O selection (n = 0 to 7)
0	Analog I/O
1	Digital I/O

Cautions 1. Set the pin set to analog I/O to the input mode by using port mode register 2 (PM2).

2. If data is written to ADPC, a wait cycle is generated. Do not write data to ADPC when the peripheral hardware clock is stopped. For details, refer to CHAPTER 26 CAUTIONS FOR WAIT.

(3) Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

ADS can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 11-6. Format of Analog Input Channel Specification Register (ADS)

Address: FF0EH After reset: 00H R/W

Symbol	7	6	5	4	3	<2>	<1>	<0>
ADS	0	0	0	0	0	ADS2	ADS1	ADS0

ADS2	ADS1	ADS0	Analog input channel	Input source
0	0	0	ANI0	P20/ANI0 pin
0	0	1	ANI1	P21/ANI1 pin or operational amplifier 0 output signal
0	1	0	ANI2	P22/ANI2 pin
0	1	1	ANI3	P23/ANI3 pin
1	0	0	ANI4	P24/ANI4 pin
Other than above			Setting prohibited	

Cautions 1. Be sure to clear bits 3 to 7 to "0".

2. Set a channel to be used for A/D conversion in the input mode by using port mode register 2 (PM2).

(4) Port mode register 2 (PM2)

When using AMP0-/ANI0/P20, AMP0OUT/ANI1/P21, and AMP0+/ANI2/P22 pins for the operational amplifier 0, set PM20 to PM22 to 1.

When using AMP1-/P25, AMP1OUT/P26, and AMP1+/P27 pins for the operational amplifier 1, set PM25 to PM27 to 1.

The output latches of P20 to P22 and P25 to P27 at this time may be 0 or 1.

If PM20 to PM22 and PM25 to PM27 are set to 0, they cannot be used as the operational amplifier 0 and 1 pins.

PM2 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 11-5. Format of Port Mode Register 2 (PM2)

Address: FF22H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20

PM2n	P2n pin I/O mode selection (n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

When using P20/ANI0/AMP0-, P21/ANI1/AMP0OUT, and P22/ANI2/AMP0+, set the registers according to the pin function to be used (refer to **Tables 11-2** and **11-3**).

Table 11-2. Setting Functions of P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins

ADPC Register	PM2 Register	OPAMP0E bit	ADS Register (n = 0, 2)	P20/ANI0/AMP0-, P22/ANI2/AMP0+ Pins
Analog input selection	Input mode	0	Selects ANIn.	Analog input (to be converted into digital signals)
			Does not select ANIn.	Analog input (not to be converted into digital signals)
		1	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Operational amplifier input
	Output mode	–	–	Setting prohibited
Digital I/O selection	Input mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital input
	Output mode	–	Selects ANIn.	Setting prohibited
			Does not select ANIn.	Digital output

Table 11-3. Setting Functions of P21/ANI1/AMP0OUT Pin

ADPC Register	PM2 Register	OPAMP0E bit	ADS Register	P21/ANI1/AMP0OUT Pin
Analog I/O selection	Input mode	0	Selects ANI1.	Analog input (to be converted into digital signals)
			Does not select ANI1.	Analog input (not to be converted into digital signals)
		1	Selects ANI1.	Operational amplifier output (to be converted into digital signals)
			Does not select ANI1.	Operational amplifier 0 output (not to be converted into digital signals)
	Output mode	–	–	Setting prohibited
Digital I/O selection	Input mode	0	Selects ANI1.	Setting prohibited
			Does not select ANI1.	Digital input
		1	–	Setting prohibited
	Output mode	0	Selects ANI1.	Setting prohibited
			Does not select ANI1.	Digital output
		1	–	Setting prohibited

Remark ADPC: A/D port configuration register
PM2: Port mode register 2
OPAMP0E: Bit 7 of operational amplifier control register (AMPM)
ADS: Analog input channel specification register

11.4 Operational Amplifier Operations

Operational amplifiers 0 and 1 both have two input pins (the AMPn- pin and the AMPn+ pin) and one output pin (the AMPnOUT pin), and can be used as single-power supply amplifiers that can be externally connected.

The amplified voltage can be used as an analog input of the A/D converter, because the AMP0OUT pin is alternatively used with analog input pin of the A/D converter.

The procedure for starting operation is described below.

<1> Use the ADPC register to set the pins (AMPn−, AMPn+, AMPnOUT) to be used as analog I/O.
<2> Use the PM2 register to set the pins (AMPn−, AMPn+, AMPnOUT) to be used to input mode.
<3> Set (1) the OPAMPnE bit and enable operation.

Caution To use as an input of the A/D converter a voltage that has been amplified, enable operation before selecting an analog input channel by using the ADS register.

Remark n = 0, 1

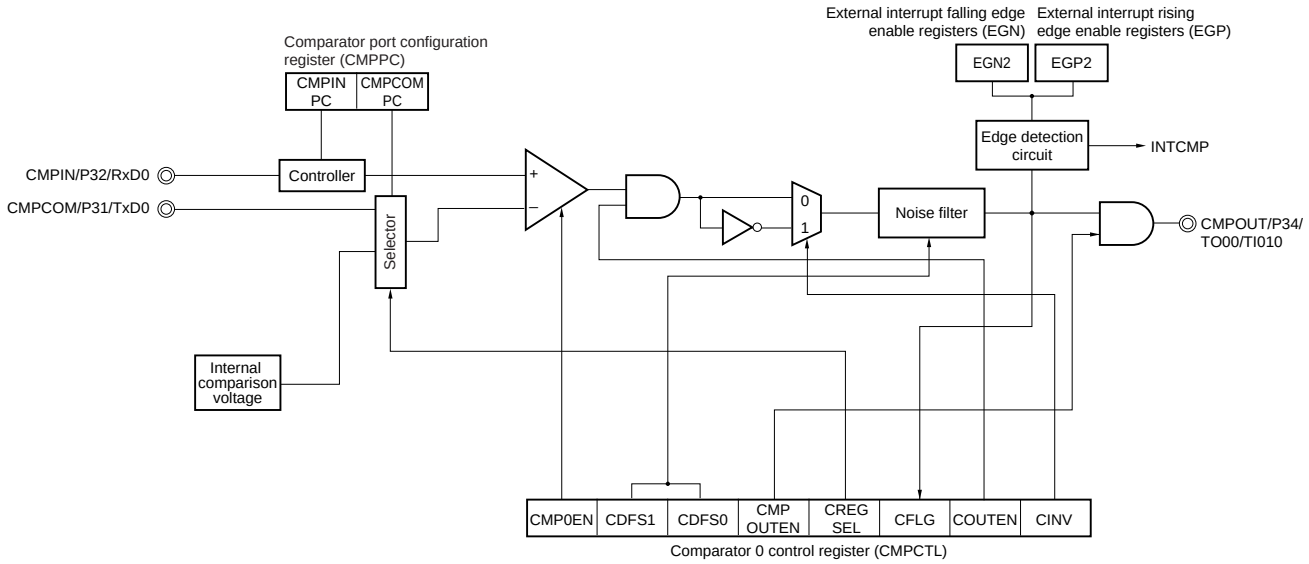
CHAPTER 12 COMPARATOR

12.1 Features of Comparator

Comparator has the following functions.

- The following reference voltages can be selected.
  <1> Internal reference voltage
  <2> Input voltage from comparator common pin (CMPCOM)
- An interrupt signal can be generated by detecting the valid edge of the comparator output. The valid edge can be set by using the EGP2 and EGN2 bits (refer to **CHAPTER 14 INTERRUPT FUNCTIONS**).
- The elimination width of the noise elimination digital filter can be selected.

Figure 12-1. Block Diagram of Comparator



12.2 Configuration of Comparator

The comparator consists of the following hardware.

Table 12-1. Configuration of Comparator

Item	Configuration
Control registers	Comparator control register (CMPCTL)
	Comparator port configuration register (CMPPC)
	Port mode register 3 (PM3)
	Port register 3 (P3)

12.3 Registers Controlling Comparator

The comparator uses the following three registers.

- Comparator control register (CMPCTL)
- Comparator port configuration register (CMPPC)
- Port mode register 3 (PM3)

(1) Comparator control register (CMPCTL)

CMPCTL is used to control the operation of comparator n, enable or disable comparator output, reverse the output, and set the noise elimination width.

CMPCTL can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CMPCTL to 00H.

Figure 12-2. Format of Comparator Control Register (CMPCTL) (1/2)

Address: FF61H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	2	<1>	<0>
CMPCTL	CMP0EN	CDFS1	CDFS0	CMPOUTEN	CREGSEL	CFLG	COUTEN	CINV

CMP0EN	Comparator 0 operation control
0	Stops operation
1	Enables operation Enables input to the external pins (CMPIN) on the positive and negative sides of comparator 0

CDFS1	CDFS0	Noise elimination width setting
0	0	Noise filter unused
0	1	$2/F_{prs}$
1	0	$2^2/F_{prs}$
1	1	$2^3/F_{prs}$

CMPOUTEN	Comparator output pin control
0	Disables comparator output to external pin
1	Enables comparator output to external pin

CREGSEL	Reference voltage selection
0	External reference voltage CMPCOM
1	Internal reference voltage (Regulator voltage: Refer to **CHAPTER 19 REGULATOR**)

CFLG	Comparator output flag monitor
0	Comparator output value is “0”
1	Comparator output value is “1”

COUTEN	Enabling or disabling of comparator output
0	Disables output (output signal = fixed to low level)
1	Enables output

Figure 12-2. Format of Comparator Control Register (CMPCTL) (2/2)

CINV	Output reversal setting
0	Forward
1	Reverse

Cautions 1. Rewrite CDFS1, CDFS0, CMPOUTEN, CREGSEL, COUTEN, CINV after setting the comparator operation to the disabled state (CMP0EN = 0).

2. With the noise elimination width, an extra peripheral hardware clock frequency (f_{PRS}) may be eliminated from the setting value.

3. If the comparator output noise interval is within "set noise elimination width + 1 clock", an illegal waveform may be output.

Remark f_{PRS}: peripheral hardware clock frequency

(2) Comparator port configuration register (CMPPC)

CMPPC switches the comparator input pin to digital I/O or analog input.

CMPPC is read-only by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CMPPC to 00H.

Figure 12-3. Format of Comparator output flag register (CMPPC)

Address: FF62H After reset: 00H R/W

Symbol	7	6	5	4	3	2	<1>	<0>
CMPPC	0	0	0	0	0	0	CMPCOMPC	CMPINPC

CMPCOMPC	Analog (A) or digital (D) selection for P31/TxD0/CMPCOM
0	Analog (A) (Default)
1	Digital (D)

CMPINPC	Analog (A) or digital (D) selection for P32/RxD0/CMPIN
0	Analog (A) (Default)
1	Digital (D)

(3) Port mode register 3 (PM3)

PM3 is used to set port 3 input or output in 1-bit units.

When CMPIN/P32/RxD0 pin, and CMPCOM/P31/TxD0 pin are used for the comparator input and comparator common input respectively, set PM31, PM32 bits to 1.

The output latches of P31, P32 at this time may be 0 or 1.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets PM3 to FFH.

Figure 12-4. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	PM30

Caution Be sure to set bits 5 to 7 of PM3 to 1.

PM3n	P3n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution If the internal reference voltage is used, the port function shared by the CMPCOM pin can be used in input mode. Using the port function in output mode, however, is prohibited. Also, accessing port register 3 (P3) is prohibited.

When using P32/RxD0/CMPIN and P31/TxD0/CMPCOM, set the registers according to the pin function to be used (refer to **Tables 12-2** and **12-3**).

Table 12-2. Setting Functions of P32/RxD0/CMPIN Pin

CMPPC Register	PM3 Register	CMP0EN bit	P32/RxD0/CMPIN Pin
Digital I/O selection	Input mode	0	Digital input
		1	Setting prohibited
	Output mode	0	Digital output
		1	Setting prohibited
Analog input selection	Input mode	0	Comparator input (Disabled)
		1	Comparator input (Enabled)
	Output mode	–	Setting prohibited

Remark CMPPC: Comparator port configuration register
PM3: Port mode register 3
CMP0EN: Bit 7 of comparator control register (CMPCTL)
ADS: Analog input channel specification register

Table 12-3. Setting Functions of P31/TxD0/CMPCOM Pin

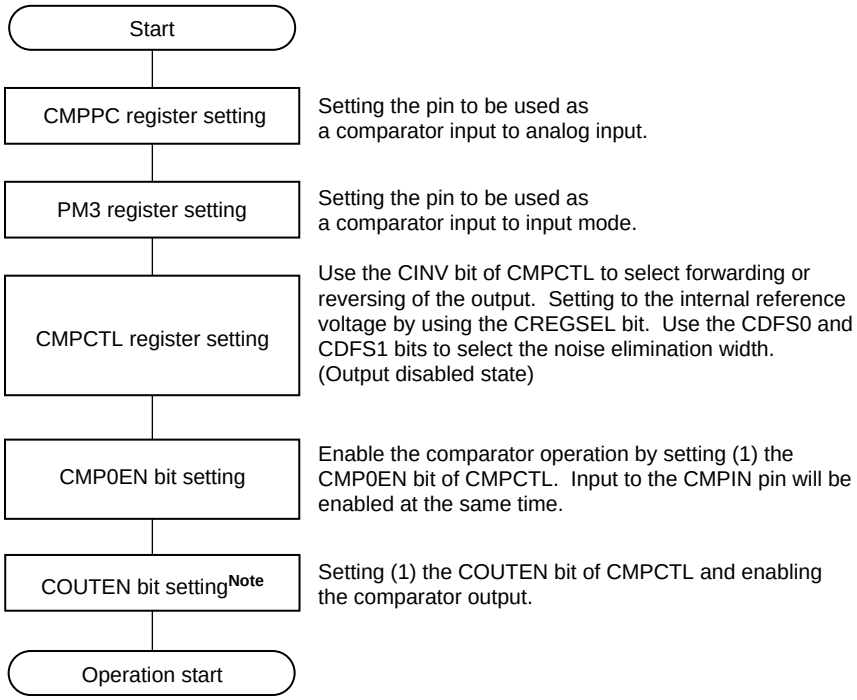
CMPPC Register	PM3 Register	CMP0EN bit	CREGSEL bit	P31/TxD0/CMPCOM Pin
Digital I/O selection	Input mode	0	0	Digital input
			1	
		1	0	Setting prohibited
			1	Digital input / Comparator common input (Disabled)
	Output mode	0	0	Digital output
			1	
		1	0	Setting prohibited
			1	Digital output / Comparator common input (Disabled)
Analog input selection	Input mode	0	0	Comparator common input (Disabled)
			1	
		1	0	Comparator common input (Disabled)
			1	Comparator common input (Enabled)
	Output mode	–		Setting prohibited

Remark CMPPC: Comparator port configuration register
PM3: Port mode register 3
CMP0EN: Bit 7 of comparator control register (CMPCTL)
ADS: Analog input channel specification register

12.4 Operation of Comparator

12.4.1 Starting comparator operation (using internal reference voltage for comparator reference voltage)

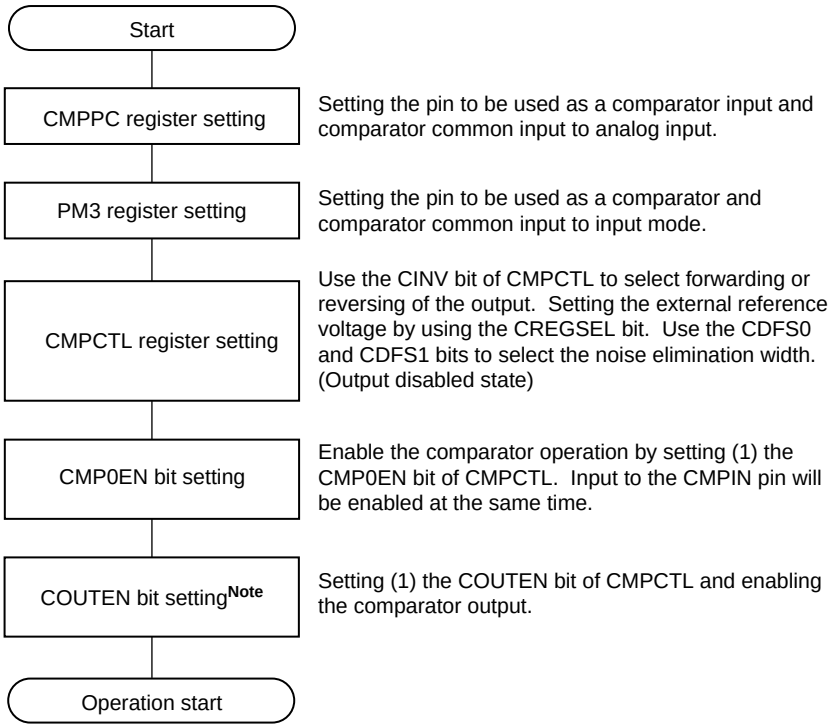
Figure 12-5. Example of Setting Procedure when Starting Comparator Operation (Using Internal Reference Voltage for Comparator Reference Voltage)



Note Set the COUTEN bit to 1 when at least 20 μs have elapsed after having set the CREGSEL bit.

12.4.2 Starting comparator operation (using input voltage from CMPCOM pin for comparator reference voltage)

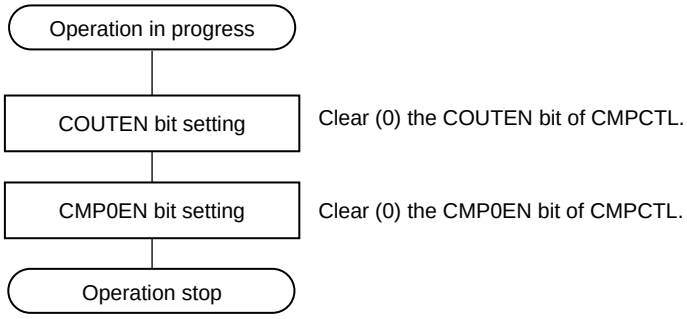
Figure 12-6. Example of Setting Procedure when Starting Comparator Operation (Using Input Voltage from Comparator Common (CMPCOM) Pin for Comparator Reference Voltage)



Note Set the COUTEN bit to 1 when at least 1 μs have elapsed after having set the CMP0EN bit.

12.4.3 Stopping comparator operation

Figure 12-7. Example of Setting Procedure when Stopping Comparator Operation



CHAPTER 13 SERIAL INTERFACE UART0

13.1 Functions of Serial Interface UART0

Serial interface UART0 has the following two modes.

(1) Operation stop mode

This mode is used when serial communication is not executed and can enable a reduction in the power consumption.

For details, see **13.4.1 Operation stop mode**.

(2) Asynchronous serial interface (UART) mode

The functions of this mode are outlined below.

For details, see **13.4.2 Asynchronous serial interface (UART) mode** and **13.4.3 Dedicated baud rate generator**.

- Maximum transfer rate: 625 kbps
- Two-pin configuration TxD0: Transmit data output pin
  RxD0: Receive data input pin
- Length of communication data can be selected from 7 or 8 bits.
- Dedicated on-chip 5-bit baud rate generator allowing any baud rate to be set
- Transmission and reception can be performed independently (full-duplex operation).
- Fixed to LSB-first communication

Cautions 1. If clock supply to serial interface UART0 is not stopped (e.g., in the HALT mode), normal operation continues. If clock supply to serial interface UART0 is stopped (e.g., in the STOP mode), each register stops operating, and holds the value immediately before clock supply was stopped. The TxD0 pin also holds the value immediately before clock supply was stopped and outputs it. However, the operation is not guaranteed after clock supply is resumed. Therefore, reset the circuit so that POWER0 = 0, RXE0 = 0, and TXE0 = 0.

2. Set POWER0 = 1 and then set TXE0 = 1 (transmission) or RXE0 = 1 (reception) to start communication.

3. TXE0 and RXE0 are synchronized by the base clock (f_{XCLK0}) set by BRGC0. To enable transmission or reception again, set TXE0 or RXE0 to 1 at least two clocks of base clock after TXE0 or RXE0 has been cleared to 0. If TXE0 or RXE0 is set within two clocks of base clock, the transmission circuit or reception circuit may not be initialized.

4. Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.

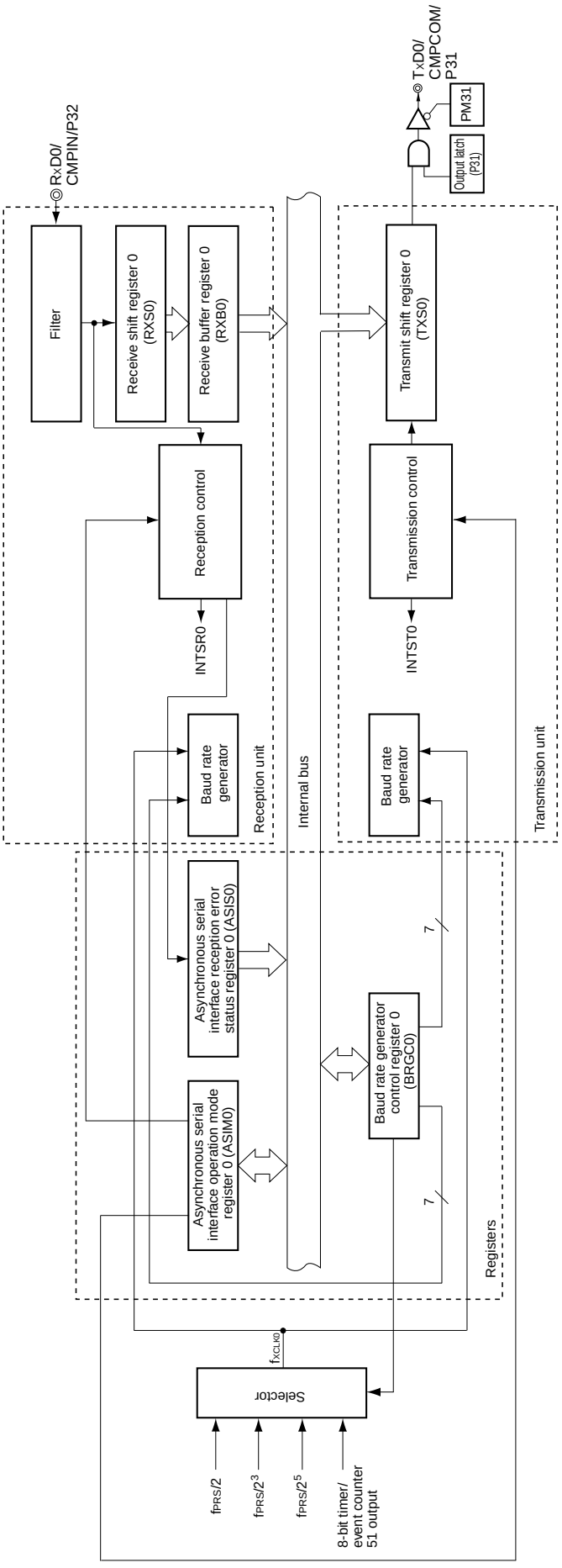
13.2 Configuration of Serial Interface UART0

Serial interface UART0 includes the following hardware.

Table 13-1. Configuration of Serial Interface UART0

Item	Configuration
Registers	Receive buffer register 0 (RXB0) Receive shift register 0 (RXS0) Transmit shift register 0 (TXS0)
Control registers	Asynchronous serial interface operation mode register 0 (ASIM0) Asynchronous serial interface reception error status register 0 (ASIS0) Baud rate generator control register 0 (BRGC0) Port mode register 3 (PM3) Port register 3 (P3)

Figure 13-1. Block Diagram of Serial Interface UART0



(1) Receive buffer register 0 (RXB0)

This 8-bit register stores parallel data converted by receive shift register 0 (RXS0).

Each time 1 byte of data has been received, new receive data is transferred to this register from receive shift register 0 (RXS0).

If the data length is set to 7 bits the receive data is transferred to bits 0 to 6 of RXB0 and the MSB of RXB0 is always 0.

If an overrun error (OVE0) occurs, the receive data is not transferred to RXB0.

RXB0 can be read by an 8-bit memory manipulation instruction. No data can be written to this register.

Reset signal generation and POWER0 = 0 set this register to FFH.

(2) Receive shift register 0 (RXS0)

This register converts the serial data input to the RxD0 pin into parallel data.

RXS0 cannot be directly manipulated by a program.

(3) Transmit shift register 0 (TXS0)

This register is used to set transmit data. Transmission is started when data is written to TXS0, and serial data is transmitted from the TxD0 pins.

TXS0 can be written by an 8-bit memory manipulation instruction. This register cannot be read.

Reset signal generation, POWER0 = 0, and TXE0 = 0 set this register to FFH.

Cautions 1. Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.

2. Do not write the next transmit data to TXS0 before the transmission completion interrupt signal (INTST0) is generated.

13.3 Registers Controlling Serial Interface UART0

Serial interface UART0 is controlled by the following five registers.

- Asynchronous serial interface operation mode register 0 (ASIM0)
- Asynchronous serial interface reception error status register 0 (ASIS0)
- Baud rate generator control register 0 (BRGC0)
- Port mode register 3 (PM3)
- Port register 3 (P3)

(1) Asynchronous serial interface operation mode register 0 (ASIM0)

This 8-bit register controls the serial communication operations of serial interface UART0.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Figure 13-2. Format of Asynchronous Serial Interface Operation Mode Register 0 (ASIM0) (1/2)

Address: FF50H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM0	POWER0	TXE0	RXE0	PS01	PS00	CL0	SL0	1

POWER0	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].
1	Enables operation of the internal operation clock.

TXE0	Enables/disables transmission
0	Disables transmission (synchronously resets the transmission circuit).
1	Enables transmission.

RXE0	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).
1	Enables reception.

Notes 1. The input from the RxD0 pin is fixed to high level when POWER0 = 0.

2. Asynchronous serial interface reception error status register 0 (ASIS0), transmit shift register 0 (TXS0), and receive buffer register 0 (RXB0) are reset.

Figure 13-2. Format of Asynchronous Serial Interface Operation Mode Register 0 (ASIM0) (2/2)

PS01	PS00	Transmission operation	Reception operation
0	0	Does not output parity bit.	Reception without parity
0	1	Outputs 0 parity.	Reception as 0 parity[Note]
1	0	Outputs odd parity.	Judges as odd parity.
1	1	Outputs even parity.	Judges as even parity.

CL0	Specifies character length of transmit/receive data
0	Character length of data = 7 bits
1	Character length of data = 8 bits

SL0	Specifies number of stop bits of transmit data
0	Number of stop bits = 1
1	Number of stop bits = 2

Note If “reception as 0 parity” is selected, the parity is not judged. Therefore, bit 2 (PE0) of asynchronous serial interface reception error status register 0 (ASIS0) is not set and the error interrupt does not occur.

Cautions
1. **To start the transmission, set POWER0 to 1 and then set TXE0 to 1. To stop the transmission, clear TXE0 to 0, and then clear POWER0 to 0.**
2. **To start the reception, set POWER0 to 1 and then set RXE0 to 1. To stop the reception, clear RXE0 to 0, and then clear POWER0 to 0.**
3. **Set POWER0 to 1 and then set RXE0 to 1 while a high level is input to the RxD0 pin. If POWER0 is set to 1 and RXE0 is set to 1 while a low level is input, reception is started.**
4. **TXE0 and RXE0 are synchronized by the base clock (f_{XCLK0}) set by BRGC0. To enable transmission or reception again, set TXE0 or RXE0 to 1 at least two clocks of base clock after TXE0 or RXE0 has been cleared to 0. If TXE0 or RXE0 is set within two clocks of base clock, the transmission circuit or reception circuit may not be initialized.**
5. **Set transmit data to TXS0 at least one base clock (f_{XCLK0}) after setting TXE0 = 1.**
6. **Clear the TXE0 and RXE0 bits to 0 before rewriting the PS01, PS00, and CL0 bits.**
7. **Make sure that TXE0 = 0 when rewriting the SL0 bit. Reception is always performed with “number of stop bits = 1”, and therefore, is not affected by the set value of the SL0 bit.**
8. **Be sure to set bit 0 to 1.**

(2) Asynchronous serial interface reception error status register 0 (ASIS0)

This register indicates an error status on completion of reception by serial interface UART0. It includes three error flag bits (PE0, FE0, OVE0).

This register is read-only by an 8-bit memory manipulation instruction.

Reset signal generation, or clearing bit 7 (POWER0) or bit 5 (RXE0) of ASIM0 to 0 clears this register to 00H. 00H is read when this register is read. If a reception error occurs, read ASIS0 and then read receive buffer register 0 (RXB0) to clear the error flag.

Figure 13-3. Format of Asynchronous Serial Interface Reception Error Status Register 0 (ASIS0)

Address: FF53H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ASIS0	0	0	0	0	0	PE0	FE0	OVE0

PE0	Status flag indicating parity error
0	If POWER0 = 0 or RXE0 = 0, or if ASIS0 register is read.
1	If the parity of transmit data does not match the parity bit on completion of reception.

FE0	Status flag indicating framing error
0	If POWER0 = 0 or RXE0 = 0, or if ASIS0 register is read.
1	If the stop bit is not detected on completion of reception.

OVE0	Status flag indicating overrun error
0	If POWER0 = 0 and RXE0 = 0, or if ASIS0 register is read.
1	If receive data is set to the RXB0 register and the next reception operation is completed before the data is read.

Cautions 1. The operation of the PE0 bit differs depending on the set values of the PS01 and PS00 bits of asynchronous serial interface operation mode register 0 (ASIM0).

2. Only the first bit of the receive data is checked as the stop bit, regardless of the number of stop bits.

3. If an overrun error occurs, the next receive data is not written to receive buffer register 0 (RXB0) but discarded.

4. If data is read from ASIS0, a wait cycle is generated. Do not read data from ASIS0 when the peripheral hardware clock (f_{PRS}) is stopped. For details, see CHAPTER 26 CAUTIONS FOR WAIT.

(3) Baud rate generator control register 0 (BRGC0)

This register selects the base clock of serial interface UART0 and the division value of the 5-bit counter.

BRGC0 can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 1FH.

Figure 13-4. Format of Baud Rate Generator Control Register 0 (BRGC0)

Address: FF51H After reset: 1FH R/W

Symbol	7	6	5	4	3	2	1	0
BRGC0	TPS01	TPS00	0	MDL04	MDL03	MDL02	MDL01	MDL00

TPS01	TPS00	Base clock (f_{XCLK0}) selection			
			f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	TM51 output[Note]			
0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
1	0	$f_{PRS}/2^3$	250 kHz	625 kHz	1.25 MHz
1	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	312.5 kHz

MDL04	MDL03	MDL02	MDL01	MDL00	k	Selection of 5-bit counter output clock
0	0	×	×	×	×	Setting prohibited
0	1	0	0	0	8	$f_{XCLK0}/8$
0	1	0	0	1	9	$f_{XCLK0}/9$
0	1	0	1	0	10	$f_{XCLK0}/10$
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
1	1	0	1	0	26	$f_{XCLK0}/26$
1	1	0	1	1	27	$f_{XCLK0}/27$
1	1	1	0	0	28	$f_{XCLK0}/28$
1	1	1	0	1	29	$f_{XCLK0}/29$
1	1	1	1	0	30	$f_{XCLK0}/30$
1	1	1	1	1	31	$f_{XCLK0}/31$

Note Note the following points when selecting the TM51 output as the base clock.

- Mode in which the count clock is cleared and started upon a match of TM51 and CR51 (TMC516 = 0)
  Start the operation of 8-bit timer/event counter 51 first and then enable the timer F/F inversion operation (TMC511 = 1).
- PWM mode (TMC516 = 1)
  Start the operation of 8-bit timer/event counter 51 first and then set the count clock to make the duty = 50%.

Cautions 1. Make sure that bit 6 (TXE0) and bit 5 (RXE0) of the ASIM0 register = 0 when rewriting the MDL04 to MDL00 bits.

2. Make sure that bit 7 (POWER0) of the ASIM0 register = 0 when rewriting the TPS01 and TPS00 bits.

3. The baud rate value is the output clock of the 5-bit counter divided by 2.

Remarks 1. f_{XCLK0}: Frequency of base clock selected by the TPS01 and TPS00 bits
2. f_{PRS}: Peripheral hardware clock frequency
3. k: Value set by the MDL04 to MDL00 bits (k = 8, 9, 10, ..., 31)
4. ×: Don't care
5. TMC516: Bit 6 of 8-bit timer mode control register 51 (TMC51)
TMC511: Bit 1 of TMC51

(4) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P31/TxD0/CMPCOM pin for serial interface data output, clear PM31 to 0 and set the output latch of P31 to 1.

When using the P32/RxD0/CMPIN pin for serial interface data input, set PM32 to 1. The output latch of P32 at this time may be 0 or 1.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

Figure 13-5. Format of Port Mode Register 3 (PM3)

Address: FF23H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

13.4 Operation of Serial Interface UART0

Serial interface UART0 has the following two modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode

13.4.1 Operation stop mode

In this mode, serial communication cannot be executed, thus reducing the power consumption. In addition, the pins can be used as ordinary port pins in this mode. To set the operation stop mode, clear bits 7, 6, and 5 (POWER0, TXE0, and RXE0) of ASIM0 to 0.

(1) Register used

The operation stop mode is set by asynchronous serial interface operation mode register 0 (ASIM0).

ASIM0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Address: FF50H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM0	POWER0	TXE0	RXE0	PS01	PS00	CL0	SL0	1

POWER0	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].

TXE0	Enables/disables transmission
0	Disables transmission (synchronously resets the transmission circuit).

RXE0	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).

Notes 1. The input from the RxD0 pin is fixed to high level when POWER0 = 0.

2. Asynchronous serial interface reception error status register 0 (ASIS0), transmit shift register 0 (TXS0), and receive buffer register 0 (RXB0) are reset.

Caution Clear POWER0 to 0 after clearing TXE0 and RXE0 to 0 to set the operation stop mode. To start the communication, set POWER0 to 1, and then set TXE0 or RXE0 to 1.

Remark To use the RxD0/CMPIN/P32 and TxD0/CMPCOM/P31 pins as general-purpose port pins, see **CHAPTER 4 PORT FUNCTIONS**.

13.4.2 Asynchronous serial interface (UART) mode

In this mode, 1-byte data is transmitted/received following a start bit, and a full-duplex operation can be performed.

A dedicated UART baud rate generator is incorporated, so that communication can be executed at a wide range of baud rates.

(1) Registers used

- Asynchronous serial interface operation mode register 0 (ASIM0)
- Asynchronous serial interface reception error status register 0 (ASIS0)
- Baud rate generator control register 0 (BRGC0)
- Port mode register 3 (PM3)
- Port register 3 (P3)

The basic procedure of setting an operation in the UART mode is as follows.

<1> Set the BRGC0 register (see **Figure 13-4**).
<2> Set bits 1 to 4 (SL0, CL0, PS00, and PS01) of the ASIM0 register (see **Figure 13-2**).
<3> Set bit 7 (POWER0) of the ASIM0 register to 1.
<4> Set bit 6 (TXE0) of the ASIM0 register to 1. → Transmission is enabled.
Set bit 5 (RXE0) of the ASIM0 register to 1. → Reception is enabled.
<5> Write data to the TXS0 register. → Data transmission is started.

Caution Take relationship with the other party of communication when setting the port mode register and port register.

The relationship between the register settings and pins is shown below.

Table 13-2. Relationship Between Register Settings and Pins

POWER0	TXE0	RXE0	PM31	P31	PM32	P32	UART0 Operation	Pin Function	
								TxD0/CMPCOM/P31	RxD0/CMPIN/P32
0	0	0	×Note	×Note	×Note	×Note	Stop	CMPCOM/P31	CMPIN/P32
1	0	1	×Note	×Note	1	×	Reception	CMPCOM/P31	RxD0
	1	0	0	1	×Note	×Note	Transmission	TxD0	CMPIN/P32
	1	1	0	1	1	×	Transmission/ reception	TxD0	RxD0

Note Can be set as port function or comparator.

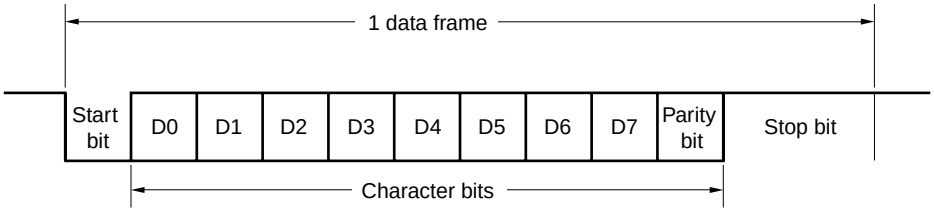
Remark ×: don't care
POWER0: Bit 7 of asynchronous serial interface operation mode register 0 (ASIM0)
TXE0: Bit 6 of ASIM0
RXE0: Bit 5 of ASIM0
PM3×: Port mode register
P3×: Port output latch

(2) Communication operation

(a) Format and waveform example of normal transmit/receive data

Figures 13-6 and 13-7 show the format and waveform example of the normal transmit/receive data.

Figure 13-6. Format of Normal UART Transmit/Receive Data



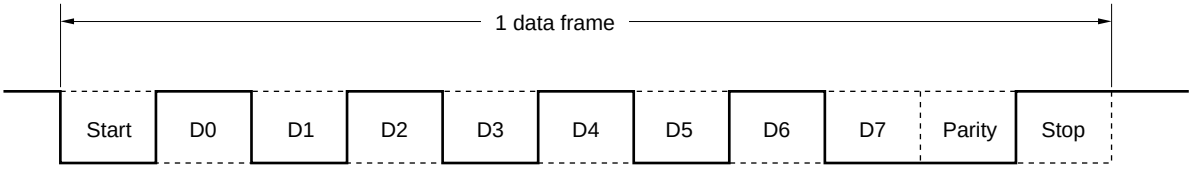
One data frame consists of the following bits.

- Start bit ... 1 bit
- Character bits ... 7 or 8 bits (LSB first)
- Parity bit ... Even parity, odd parity, 0 parity, or no parity
- Stop bit ... 1 or 2 bits

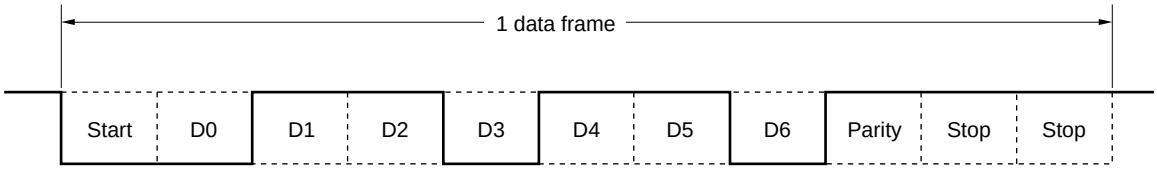
The character bit length, parity, and stop bit length in one data frame are specified by asynchronous serial interface operation mode register 0 (ASIM0).

Figure 13-7. Example of Normal UART Transmit/Receive Data Waveform

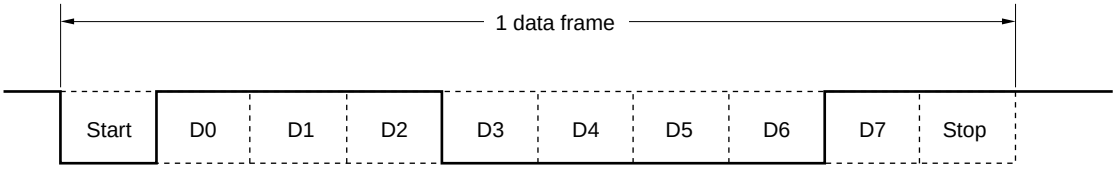
1. Data length: 8 bits, Parity: Even parity, Stop bit: 1 bit, Communication data: 55H



2. Data length: 7 bits, Parity: Odd parity, Stop bit: 2 bits, Communication data: 36H



3. Data length: 8 bits, Parity: None, Stop bit: 1 bit, Communication data: 87H



(b) Parity types and operation

The parity bit is used to detect a bit error in communication data. Usually, the same type of parity bit is used on both the transmission and reception sides. With even parity and odd parity, a 1-bit (odd number) error can be detected. With zero parity and no parity, an error cannot be detected.

(i) Even parity

- Transmission

  Transmit data, including the parity bit, is controlled so that the number of bits that are “1” is even.
  The value of the parity bit is as follows.

  If transmit data has an odd number of bits that are “1”: 1
  If transmit data has an even number of bits that are “1”: 0

- Reception

  The number of bits that are “1” in the receive data, including the parity bit, is counted. If it is odd, a parity error occurs.

(ii) Odd parity

- Transmission

  Unlike even parity, transmit data, including the parity bit, is controlled so that the number of bits that are “1” is odd.

  If transmit data has an odd number of bits that are “1”: 0
  If transmit data has an even number of bits that are “1”: 1

- Reception

  The number of bits that are “1” in the receive data, including the parity bit, is counted. If it is even, a parity error occurs.

(iii) 0 parity

The parity bit is cleared to 0 when data is transmitted, regardless of the transmit data.
The parity bit is not detected when the data is received. Therefore, a parity error does not occur regardless of whether the parity bit is “0” or “1”.

(iv) No parity

No parity bit is appended to the transmit data.
Reception is performed assuming that there is no parity bit when data is received. Because there is no parity bit, a parity error does not occur.

(c) Transmission

If bit 7 (POWER0) of asynchronous serial interface operation mode register 0 (ASIM0) is set to 1 and bit 6 (TXE0) of ASIM0 is then set to 1, transmission is enabled. Transmission can be started by writing transmit data to transmit shift register 0 (TXS0). The start bit, parity bit, and stop bit are automatically appended to the data.

When transmission is started, the start bit is output from the TxD0 pin, and the transmit data is output followed by the rest of the data in order starting from the LSB. When transmission is completed, the parity and stop bits set by ASIM0 are appended and a transmission completion interrupt request (INTST0) is generated.

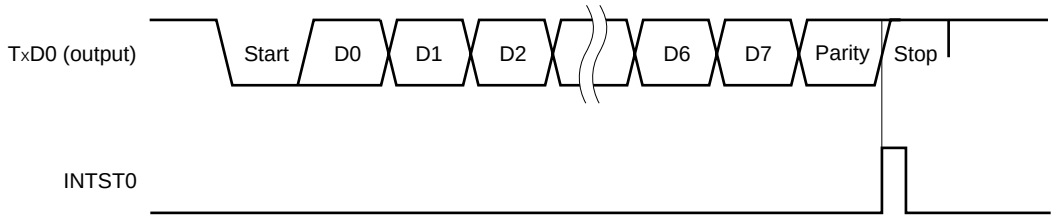
Transmission is stopped until the data to be transmitted next is written to TXS0.

Figure 13-8 shows the timing of the transmission completion interrupt request (INTST0). This interrupt occurs as soon as the last stop bit has been output.

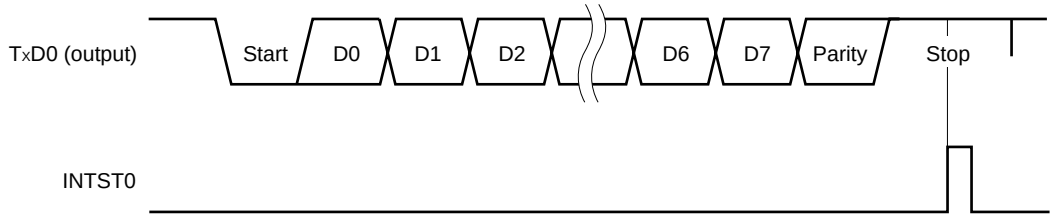
Caution After transmit data is written to TXS0, do not write the next transmit data before the transmission completion interrupt signal (INTST0) is generated.

Figure 13-8. Transmission Completion Interrupt Request Timing

1. Stop bit length: 1



2. Stop bit length: 2



(d) Reception

Reception is enabled and the RxD0 pin input is sampled when bit 7 (POWER0) of asynchronous serial interface operation mode register 0 (ASIM0) is set to 1 and then bit 5 (RXE0) of ASIM0 is set to 1.

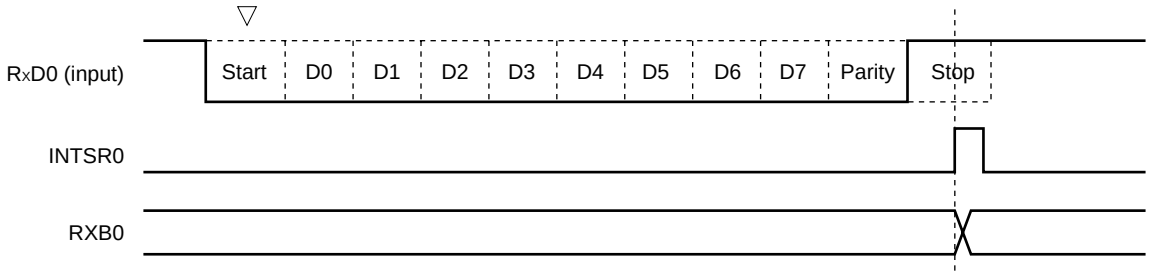
The 5-bit counter of the baud rate generator starts counting when the falling edge of the RxD0 pin input is detected. When the set value of baud rate generator control register 0 (BRGC0) has been counted, the RxD0 pin input is sampled again (▽ in Figure 13-9). If the RxD0 pin is low level at this time, it is recognized as a start bit.

When the start bit is detected, reception is started, and serial data is sequentially stored in receive shift register 0 (RXS0) at the set baud rate. When the stop bit has been received, the reception completion interrupt (INTSR0) is generated and the data of RXS0 is written to receive buffer register 0 (RXB0). If an overrun error (OVE0) occurs, however, the receive data is not written to RXB0.

Even if a parity error (PE0) occurs while reception is in progress, reception continues to the reception position of the stop bit, and an reception error interrupt (INTSR0) is generated after completion of reception.

INTSR0 occurs upon completion of reception and in case of a reception error.

Figure 13-9. Reception Completion Interrupt Request Timing



Cautions 1. If a reception error occurs, read asynchronous serial interface reception error status register 0 (ASIS0) and then read receive buffer register 0 (RXB0) to clear the error flag. Otherwise, an overrun error will occur when the next data is received, and the reception error status will persist.

2. Reception is always performed with the "number of stop bits = 1". The second stop bit is ignored.

(e) Reception error

Three types of errors may occur during reception: a parity error, framing error, or overrun error. If the error flag of asynchronous serial interface reception error status register 0 (ASIS0) is set as a result of data reception, a reception error interrupt (INTSR0) is generated.

Which error has occurred during reception can be identified by reading the contents of ASIS0 in the reception error interrupt (INTSR0) servicing (see **Figure 13-3**).

The contents of ASIS0 are cleared to 0 when ASIS0 is read.

Table 13-3. Cause of Reception Error

Reception Error	Cause
Parity error	The parity specified for transmission does not match the parity of the receive data.
Framing error	Stop bit is not detected.
Overrun error	Reception of the next data is completed before data is read from receive buffer register 0 (RXB0).

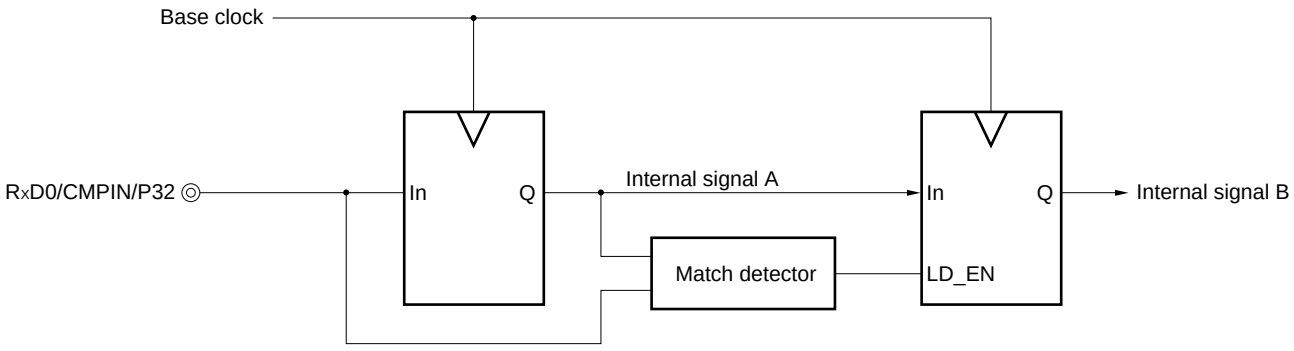
(f) Noise filter of receive data

The RxD0 signal is sampled using the base clock output by the prescaler block.

If two sampled values are the same, the output of the match detector changes, and the data is sampled as input data.

Because the circuit is configured as shown in Figure 13-10, the internal processing of the reception operation is delayed by two clocks from the external signal status.

Figure 13-10. Noise Filter Circuit



13.4.3 Dedicated baud rate generator

The dedicated baud rate generator consists of a source clock selector and a 5-bit programmable counter, and generates a serial clock for transmission/reception of UART0.

Separate 5-bit counters are provided for transmission and reception.

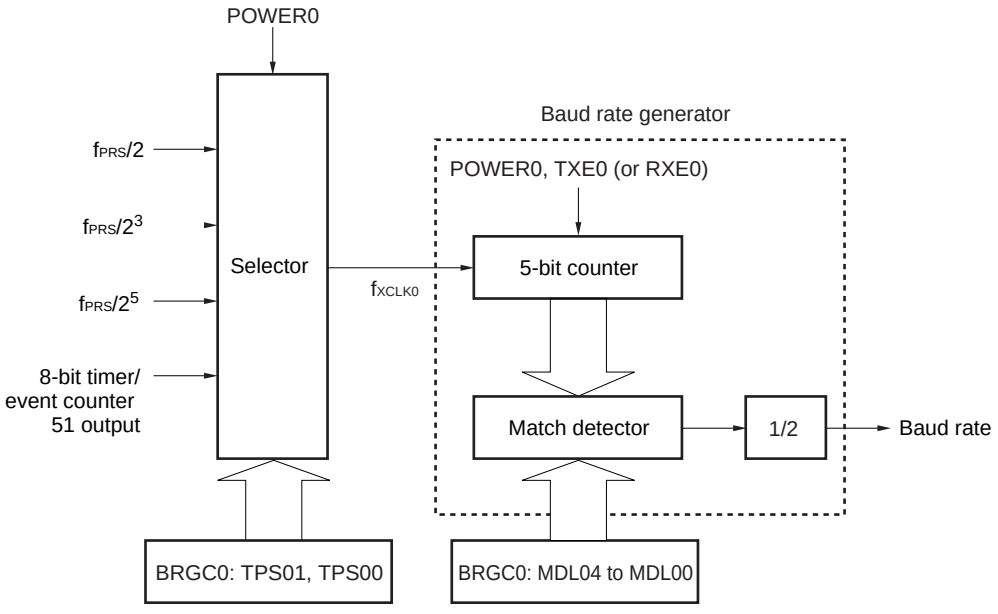
(1) Configuration of baud rate generator

- Base clock
  The clock selected by bits 7 and 6 (TPS01 and TPS00) of baud rate generator control register 0 (BRGC0) is supplied to each module when bit 7 (POWER0) of asynchronous serial interface operation mode register 0 (ASIM0) is 1. This clock is called the base clock and its frequency is called f_{XCLK0}. The base clock is fixed to low level when POWER0 = 0.

- Transmission counter
  This counter stops operation, cleared to 0, when bit 7 (POWER0) or bit 6 (TXE0) of asynchronous serial interface operation mode register 0 (ASIM0) is 0.
  It starts counting when POWER0 = 1 and TXE0 = 1.
  The counter is cleared to 0 when the first data transmitted is written to transmit shift register 0 (TXS0).

- Reception counter
  This counter stops operation, cleared to 0, when bit 7 (POWER0) or bit 5 (RXE0) of asynchronous serial interface operation mode register 0 (ASIM0) is 0.
  It starts counting when the start bit has been detected.
  The counter stops operation after one frame has been received, until the next start bit is detected.

Figure 13-11. Configuration of Baud Rate Generator



Remark POWER0: Bit 7 of asynchronous serial interface operation mode register 0 (ASIM0)
TXE0: Bit 6 of ASIM0
RXE0: Bit 5 of ASIM0
BRGC0: Baud rate generator control register 0

(2) Generation of serial clock

A serial clock to be generated can be specified by using baud rate generator control register 0 (BRGC0).

Select the clock to be input to the 5-bit counter by using bits 7 and 6 (TPS01 and TPS00) of BRGC0.

Bits 4 to 0 (MDL04 to MDL00) of BRGC0 can be used to select the division value ($f_{XCLK0}/8$ to $f_{XCLK0}/31$) of the 5-bit counter.

13.4.4 Calculation of baud rate

(1) Baud rate calculation expression

The baud rate can be calculated by the following expression.

- Baud rate = $\frac{f_{XCLK0}}{2 \times k}$ [bps]

f_{XCLK0}: Frequency of base clock selected by the TPS01 and TPS00 bits of the BRGC0 register

k: Value set by the MDL04 to MDL00 bits of the BRGC0 register (k = 8, 9, 10, ..., 31)

Table 13-4. Set Value of TPS01 and TPS00

TPS01	TPS00	Base clock (f_{XCLK0}) selection			
			f_{PRS} = 2 MHz	f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	TM51 output[Note]			
0	1	$f_{PRS}/2$	1 MHz	2.5 MHz	5 MHz
1	0	$f_{PRS}/2^3$	250 kHz	625 kHz	1.25 MHz
1	1	$f_{PRS}/2^5$	62.5 kHz	156.25 kHz	312.5 kHz

Note Note the following points when selecting the TM51 output as the base clock.

- Mode in which the count clock is cleared and started upon a match of TM51 and CR51 (TMC516 = 0)
  Start the operation of 8-bit timer/event counter 51 first and then enable the timer F/F inversion operation (TMC511 = 1).
- PWM mode (TMC516 = 1)
  Start the operation of 8-bit timer/event counter 51 first and then set the count clock to make the duty = 50%.

(2) Error of baud rate

The baud rate error can be calculated by the following expression.

- $\text{Error (\%)} = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (correct baud rate)}} - 1 \right) \times 100 \text{ [\%]}$

Cautions 1. Keep the baud rate error during transmission to within the permissible error range at the reception destination.

2. Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.

Example: Frequency of base clock = 2.5 MHz = 2,500,000 Hz
Set value of MDL04 to MDL00 bits of BRGC0 register = 10000B (k = 16)
Target baud rate = 76,800 bps

Baud rate = 2.5 M/(2 × 16)
= 2,500,000/(2 × 16) = 78,125 [bps]

Error = (78,125/76,800 − 1) × 100
= 1.725 [%]

(3) Example of setting baud rate

Table 13-5. Set Data of Baud Rate Generator

Baud Rate [bps]	f_{PRS} = 2.0 MHz				f_{PRS} = 5.0 MHz				f_{PRS} = 10.0 MHz			
	TPS01, TPS00	k	Calculated Value	ERR [%]	TPS01, TPS00	k	Calculated Value	ERR [%]	TPS01, TPS00	k	Calculated Value	ERR [%]
4800	2H	26	4808	0.16	3H	16	4883	1.73	–	–	–	–
9600	2H	13	9615	0.16	3H	8	9766	1.73	3H	16	9766	1.73
10400	2H	12	10417	0.16	2H	30	10417	0.16	3H	15	10417	0.16
19200	1H	26	19231	0.16	2H	16	19531	1.73	3H	8	19531	1.73
24000	1H	21	23810	−0.79	2H	13	24038	0.16	2H	26	24038	0.16
31250	1H	16	31250	0	2H	10	31250	0	2H	20	31250	0
33600	1H	15	33333	−0.79	2H	9	34722	3.34	2H	19	32895	−2.1
38400	1H	13	38462	0.16	2H	8	39063	1.73	2H	16	39063	1.73
56000	1H	9	55556	−0.79	1H	22	56818	1.46	2H	11	56818	1.46
62500	1H	8	62500	0	1H	20	62500	0	2H	10	62500	0
76800	–	–	–	–	1H	16	78125	1.73	2H	8	78125	1.73
115200	–	–	–	–	1H	11	113636	−1.36	1H	22	113636	−1.36
153600	–	–	–	–	1H	8	156250	1.73	1H	16	156250	1.73
312500	–	–	–	–	–	–	–	–	1H	8	312500	0
625000	–	–	–	–	–	–	–	–	–	–	–	–

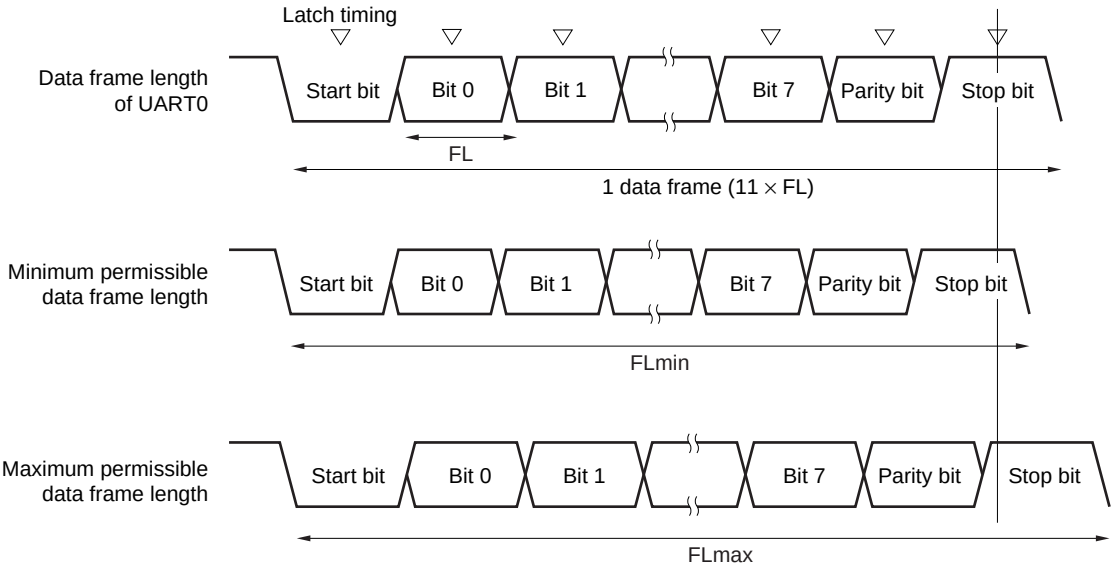
Remark TPS01, TPS00: Bits 7 and 6 of baud rate generator control register 0 (BRGC0) (setting of base clock (f_{XCLK0}))
k: Value set by the MDL04 to MDL00 bits of BRGC0 (k = 8, 9, 10, ..., 31)
f_{PRS}: Peripheral hardware clock frequency
ERR: Baud rate error

(4) Permissible baud rate range during reception

The permissible error from the baud rate at the transmission destination during reception is shown below.

Caution Make sure that the baud rate error during reception is within the permissible error range, by using the calculation expression shown below.

Figure 13-12. Permissible Baud Rate Range During Reception



As shown in Figure 13-12, the latch timing of the receive data is determined by the counter set by baud rate generator control register 0 (BRGC0) after the start bit has been detected. If the last data (stop bit) meets this latch timing, the data can be correctly received.

Assuming that 11-bit data is received, the theoretical values can be calculated as follows.

$FL = (Brate)^{-1}$

Brate: Baud rate of UART0

k: Set value of BRGC0

FL: 1-bit data length

Margin of latch timing: 2 clocks

Minimum permissible data frame length: $FLmin = 11 \times FL - \frac{k-2}{2k} \times FL = \frac{21k+2}{2k} FL$

Therefore, the maximum receivable baud rate at the transmission destination is as follows.

$$BRmax = (FLmin/11)^{-1} = \frac{22k}{21k+2} Brate$$

Similarly, the maximum permissible data frame length can be calculated as follows.

$$\frac{10}{11} \times FLmax = 11 \times FL - \frac{k+2}{2 \times k} \times FL = \frac{21k-2}{2 \times k} FL$$

$$FLmax = \frac{21k-2}{20k} FL \times 11$$

Therefore, the minimum receivable baud rate at the transmission destination is as follows.

$$BRmin = (FLmax/11)^{-1} = \frac{20k}{21k-2} Brate$$

The permissible baud rate error between UART0 and the transmission destination can be calculated from the above minimum and maximum baud rate expressions, as follows.

Table 13-6. Maximum/Minimum Permissible Baud Rate Error

Division Ratio (k)	Maximum Permissible Baud Rate Error	Minimum Permissible Baud Rate Error
8	+3.53%	–3.61%
16	+4.14%	–4.19%
24	+4.34%	–4.38%
31	+4.44%	–4.47%

Remarks 1. The permissible error of reception depends on the number of bits in one frame, input clock frequency, and division ratio (k). The higher the input clock frequency and the higher the division ratio (k), the higher the permissible error.

2. k: Set value of BRGC0

CHAPTER 14 INTERRUPT FUNCTIONS

14.1 Interrupt Function Types

The following two types of interrupt functions are used.

(1) Maskable interrupts

These interrupts undergo mask control. Maskable interrupts can be divided into a high interrupt priority group and a low interrupt priority group by setting the priority specification flag registers (PR0L, PR0H, PR1L).

Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the priority of vectored interrupt servicing. For the priority order, refer to **Table 14-1**.

A standby release signal is generated and STOP and HALT modes are released.

External interrupt requests and internal interrupt requests are provided as maskable interrupts.

(2) Software interrupt

This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

14.2 Interrupt Sources and Configuration

The interrupt sources consist of maskable interrupts and software interrupts. In addition, they also have up to four reset sources (refer to **Table 14-1**).

Table 14-1. Interrupt Source List (1/2)

Interrupt Type	Internal/ External	Basic Configuration Type Note 1	Default Priority Note 2	Interrupt Source		Vector Table Address
				Name	Trigger	
Maskable	Internal	(A)	0	INTLVI	Low-voltage detection Note 3	0004H
	External	(B)	1	INTP0	Pin input edge detection	0006H
			2	INTP1		0008H
			3	INTCMP	Comparator edge detection	000AH
	-	-	4	-	-	000CH
			5	-		000EH
			6	-		0010H
			7	-		0012H
	Internal	(A)	8	INTSR0	End of UART0 reception/reception error generation	0014H
			9	INTST0	End of UART0 transmission	0016H
	-	-	10	-	-	0018H
	Internal	(A)	11	INTTMH1	Match between TMH1 and CMP01 (when compare register is specified)	001AH
	-	-	12	-	-	001CH
			13			001EH
	Internal	(A)	14	INTTM000	Match between TM00 and CR000 (when compare register is specified), TI010 pin valid edge detection (when capture register is specified)	0020H
			15	INTTM010	Match between TM00 and CR010 (when compare register is specified), TI000 pin valid edge detection (when capture register is specified)	0022H
			16	INTAD	End of A/D conversion	0024H
	-	-	17	-	-	0026H
			18			0028H
	Internal	(A)	19	INTTM51 Note 4	Match between TM51 and CR51 (when compare register is specified)	002AH
	-	-	20	-	-	002CH

Notes 1. Basic configuration types (A) to (C) correspond to (A) to (C) in **Figure 14-1**.

2. The default priority determines the sequence of processing vectored interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 28 indicates the lowest priority.

3. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is cleared to 0.

4. When 8-bit timer/event counter 51 is used in the carrier generator mode, an interrupt is generated upon the timing when the INTTM5H1 signal is generated (refer to **Figure 8-11 Transfer Timing**).

Table 14-1. Interrupt Source List (2/2)

Interrupt Type	Internal/ External	Basic Configuration Type Note 1	Default Priority Note 2	Interrupt Source		Vector Table Address
				Name	Trigger	
Maskable	-	-	21	-	-	002EH
			22			0030H
			23			0032H
			24			0034H
			25			0036H
			26			0038H
			27			003AH
			28			003CH
Software	–	(C)	–	BRK	BRK instruction execution	003EH
Reset	–	–	–	RESET	Reset input	0000H
				POC	Power-on clear	
				LVI	Low-voltage detection Note 3	
				WDT	WDT overflow	

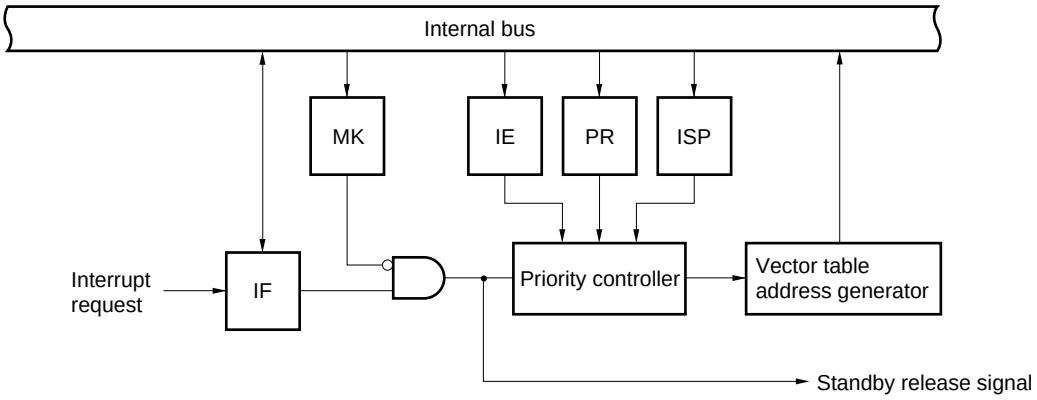
Notes 1. Basic configuration types (A) to (C) correspond to (A) to (C) in **Figure 14-1**.

2. The default priority determines the sequence of processing vectored interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 28 indicates the lowest priority.

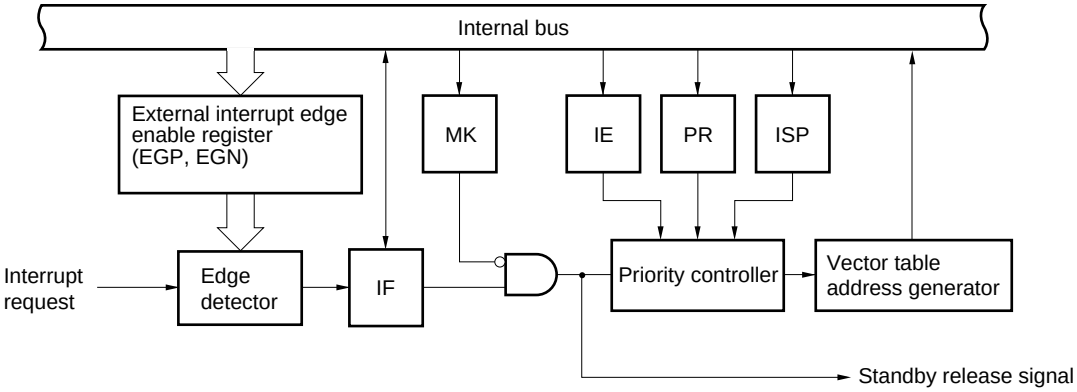
3. When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is set to 1.

Figure 14-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal maskable interrupt



(B) External maskable interrupt (INTPn, INTCMP)

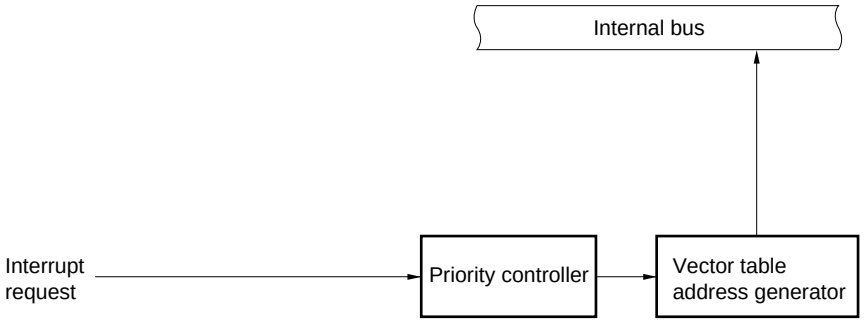


Remark n = 0, 1

IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

Figure 14-1. Basic Configuration of Interrupt Function (2/2)

(C) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

14.3 Registers Controlling Interrupt Functions

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag registers (IF0L, IF0H, IF1L)
- Interrupt mask flag registers (MK0L, MK0H, MK1L)
- Priority specification flag registers (PR0L, PR0H, PR1L)
- External interrupt rising edge enable registers (EGP)
- External interrupt falling edge enable registers (EGN)
- Program status word (PSW)

Table 14-2 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 14-2. Flags Corresponding to Interrupt Request Sources

Interrupt Source	Interrupt Request Flag	Register	Interrupt Mask Flag	Register	Priority Specification Flag	Register
INTLVI	LVIIF	IF0L	LVIMK	MK0L	LVIPR	PR0L
INTP0	PIF0		PMK0		PPR0	
INTP1	PIF1		PMK1		PPR1	
INTCMP	CMPIF		CMPMK		CMPPR	
INTSR6	SRIF0	IF0H	SRMK0	MK0H	SRPR0	PR0H
INTST0	STIF0		STMK0		STPR0	
INTTMH1	TMIFH1		TMMKH1		TMPRH1	
INTTM000	TMIF000		TMMK000		TMPR000	
INTTM010	TMIF010		TMMK010		TMPR010	
INTAD	ADIF	IF1L	ADMK	MK1L	ADPR	PR1L
INTTM51[Note]	TMIF51		TMMK51		TMPR51	

Note When 8-bit timer/event counter 51 is used in the carrier generator mode, an interrupt is generated upon the timing when the INTTM5H1 signal is generated (refer to **Figure 8-11 Transfer Timing**).

(1) Interrupt request flag registers (IF0L, IF0H, IF1L)

The interrupt request flags are set to 1 when the corresponding interrupt request is generated or an instruction is executed. They are cleared to 0 when an instruction is executed upon acknowledgment of an interrupt request or upon reset signal generation.

When an interrupt is acknowledged, the interrupt request flag is automatically cleared and then the interrupt routine is entered.

IF0L, IF0H, and IF1L are set by a 1-bit or 8-bit memory manipulation instruction. When IF0L and IF0H are combined to form 16-bit register IF0, they are set by a 16-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Cautions 1. When operating a timer, serial interface, or A/D converter after standby release, operate it once after clearing the interrupt request flag. An interrupt request flag may be set by noise.

2. When manipulating a flag of the interrupt request flag register, use a 1-bit memory manipulation instruction (CLR1). When describing in C language, use a bit manipulation instruction such as "IF0L.0 = 0;" or "_asm("clr1 IF0L, 0");" because the compiled assembler must be a 1-bit memory manipulation instruction (CLR1).

If a program is described in C language using an 8-bit memory manipulation instruction such as "IF0L &= 0xfe;" and compiled, it becomes the assembler of three instructions.

```
mov a, IF0L
and a, #0FEH
mov IF0L, a
```

In this case, even if the request flag of another bit of the same interrupt request flag register (IF0L) is set to 1 at the timing between "mov a, IF0L" and "mov IF0L, a", the flag is cleared to 0 at "mov IF0L, a". Therefore, care must be exercised when using an 8-bit memory manipulation instruction in C language.

Figure 14-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L)

Address: FFE0H After reset: 00H R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
IF0L	0	0	0	0	CMPIF	PIF1	PIF0	LVIIF

Address: FFE1H After reset: 00H R/W

Symbol	<7>	<6>	5	4	<3>	2	<1>	<0>
IF0H	TMIF010	TMIF000	0	0	TMIFH1	0	STIF0	SRIF0

Address: FFE2H After reset: 00H R/W

Symbol	7	6	5	4	<3>	2	1	<0>
IF1L	0	0	0	0	TMIF51	0	0	ADIF

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Caution Be sure to clear bits 4 and 7 of IF0L, bits 2, 4 and 5 of IF0H, and bits 1, 2, 4 to 7 of IF1L to 0.

(2) Interrupt mask flag registers (MK0L, MK0H, MK1L)

The interrupt mask flags are used to enable/disable the corresponding maskable interrupt servicing.

MK0L, MK0H, and MK1L are set by a 1-bit or 8-bit memory manipulation instruction. When MK0L and MK0H are combined to form 16-bit register MK0, they are set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 14-3. Format of Interrupt Mask Flag Registers (MK0L, MK0H, MK1L)

Address: FFE4H After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
MK0L	1	1	1	1	CMPMK	PMK1	PMK0	LVIMK

Address: FFE5H After reset: FFH R/W

Symbol	<7>	<6>	5	4	<3>	2	<1>	<0>
MK0H	TMMK010	TMMK000	1	1	TMMKH1	1	STMK0	SRMK0

Address: FFE6H After reset: FFH R/W

Symbol	7	6	5	4	<3>	2	1	<0>
MK1L	1	1	1	1	TMMK51	1	1	ADMK

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Caution Be sure to set bits 4 to 7 of MK0L, bits 2, 4 and 5 of MK0H, and bits 1, 2, 4 to 7 of MK1L to 1.

(3) Priority specification flag registers (PR0L, PR0H, PR1L)

The priority specification flag registers are used to set the corresponding maskable interrupt priority order.

PR0L, PR0H, and PR1L are set by a 1-bit or 8-bit memory manipulation instruction. If PR0L and PR0H are combined to form 16-bit register PR0, they are set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 14-4. Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L)

Address: FFE8H After reset: FFH R/W

Symbol	7	6	5	4	<3>	<2>	<1>	<0>
PR0L	1	1	1	1	CMPPR	PPR1	PPR0	LVIPR

Address: FFE9H After reset: FFH R/W

Symbol	<7>	<6>	5	4	<3>	2	<1>	<0>
PR0H	TMPR010	TMPR000	1	1	TMPRH1	1	STPR0	SRPR0

Address: FFEAH After reset: FFH R/W

Symbol	7	6	5	4	<3>	2	1	<0>
PR1L	1	1	1	1	TMPR51	1	1	ADPR

XXPRX	Priority level selection
0	High priority level
1	Low priority level

Caution Be sure to set bits 4 to 7 of PR0L, bits 2, 4 and 5 of PR0H, and bits 1, 2, 4 to 7 of PR1L to 1.

(4) External interrupt rising edge enable registers (EGP), external interrupt falling edge enable registers (EGN)

These registers specify the valid edge for INTPn.

EGP and EGN are set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 14-5. Format of External Interrupt Rising Edge Enable Registers (EGP) and External Interrupt Falling Edge Enable Registers (EGN)

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	0	0	0	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	0	0	0	0	EGN2	EGN1	EGN0

EGPn	EGNn	INTPn pin valid edge selection
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Caution Be sure to clear bits 3 to 7 of EGP and EGN to 0.

Remark n = 0 to 2

Table 14-3 shows the ports corresponding to EGPn and EGNn.

Table 14-3. Ports Corresponding to EGPn and EGNn

Detection Enable Register		Edge Detection Port	Interrupt Request Signal
EGP0	EGN0	P30	INTP0
EGP1	EGN1	P33	INTP1
EGP2	EGN2	-	INTCMP

Caution Select the port mode by clearing EGPn and EGNn to 0 because an edge may be detected when the external interrupt function is switched to the port function.

Remark n = 0 to 2

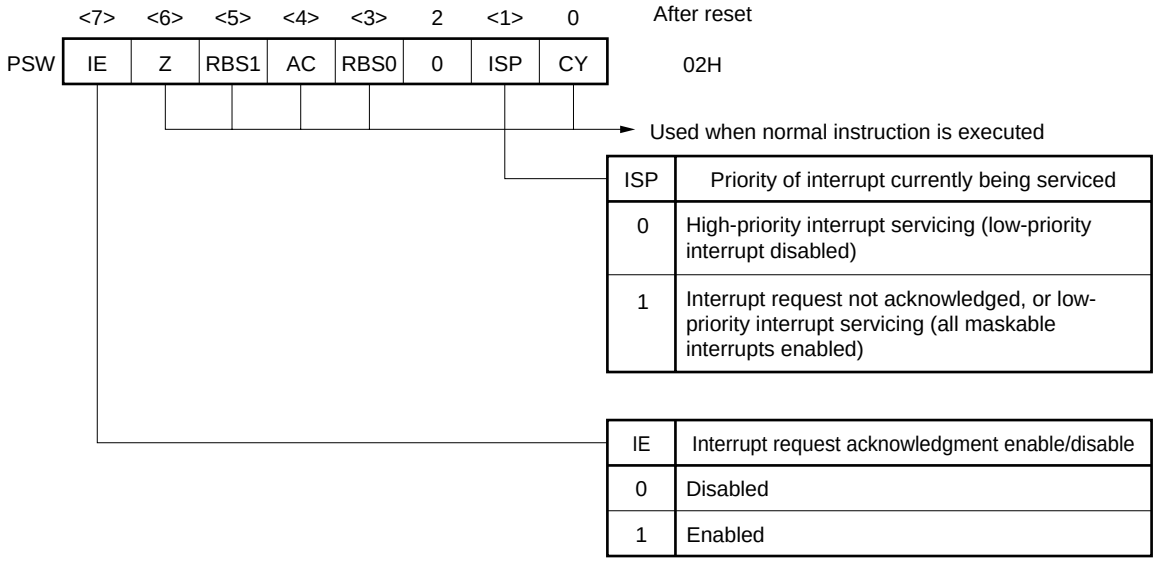
(5) Program status word (PSW)

The program status word is a register used to hold the instruction execution result and the current status for an interrupt request. The IE flag that sets maskable interrupt enable/disable and the ISP flag that controls multiple interrupt servicing are mapped to the PSW.

Besides 8-bit read/write, this register can carry out operations using bit manipulation instructions and dedicated instructions (EI and DI). When a vectored interrupt request is acknowledged, if the BRK instruction is executed, the contents of the PSW are automatically saved into a stack and the IE flag is reset to 0. If a maskable interrupt request is acknowledged, the contents of the priority specification flag of the acknowledged interrupt are transferred to the ISP flag. The PSW contents are also saved into the stack with the PUSH PSW instruction. They are restored from the stack with the RETI, RETB, and POP PSW instructions.

Reset signal generation sets PSW to 02H.

Figure 14-6. Format of Program Status Word



ISP	Priority of interrupt currently being serviced
0	High-priority interrupt servicing (low-priority interrupt disabled)
1	Interrupt request not acknowledged, or low-priority interrupt servicing (all maskable interrupts enabled)

IE	Interrupt request acknowledgment enable/disable
0	Disabled
1	Enabled

14.4 Interrupt Servicing Operations

14.4.1 Maskable interrupt acknowledgment

A maskable interrupt becomes acknowledgeable when the interrupt request flag is set to 1 and the mask (MK) flag corresponding to that interrupt request is cleared to 0. A vectored interrupt request is acknowledged if interrupts are in the interrupt enabled state (when the IE flag is set to 1). However, a low-priority interrupt request is not acknowledged during servicing of a higher priority interrupt request (when the ISP flag is reset to 0).

The times from generation of a maskable interrupt request until vectored interrupt servicing is performed are listed in Table 17-4 below.

For the interrupt request acknowledgment timing, refer to **Figures 14-8** and **14-9**.

Table 14-4. Time from Generation of Maskable Interrupt Until Servicing

	Minimum Time	Maximum Time[Note]
When ××PR = 0	7 clocks	32 clocks
When ××PR = 1	8 clocks	33 clocks

Note If an interrupt request is generated just before a divide instruction, the wait time becomes longer.

Remark 1 clock: $1/f_{CPU}$ (f_{CPU}: CPU clock)

If two or more maskable interrupt requests are generated simultaneously, the request with a higher priority level specified in the priority specification flag is acknowledged first. If two or more interrupts requests have the same priority level, the request with the highest default priority is acknowledged first.

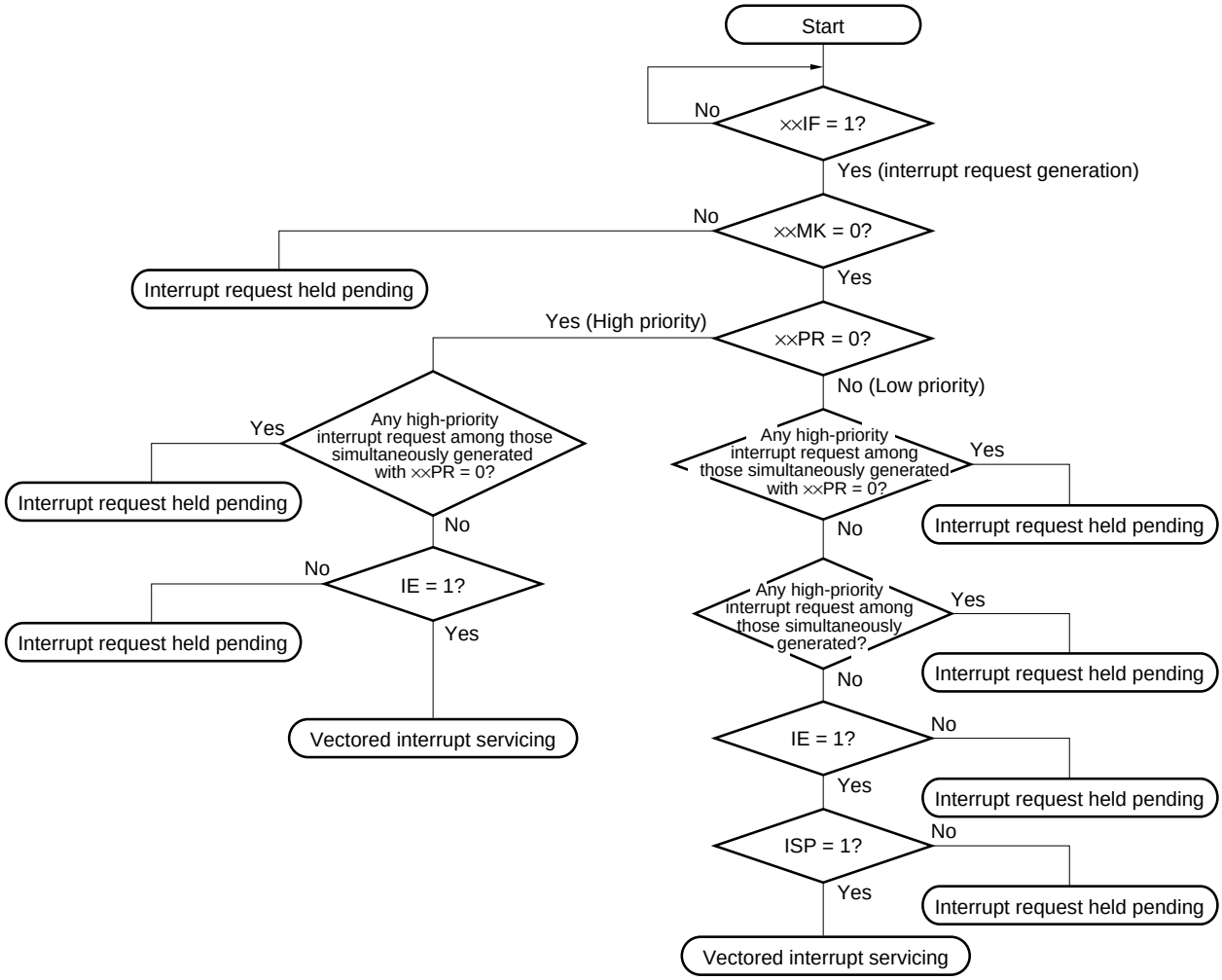
An interrupt request that is held pending is acknowledged when it becomes acknowledgeable.

Figure 14-7 shows the interrupt request acknowledgment algorithm.

If a maskable interrupt request is acknowledged, the contents are saved into the stacks in the order of PSW, then PC, the IE flag is reset (0), and the contents of the priority specification flag corresponding to the acknowledged interrupt are transferred to the ISP flag. The vector table data determined for each interrupt request is the loaded into the PC and branched.

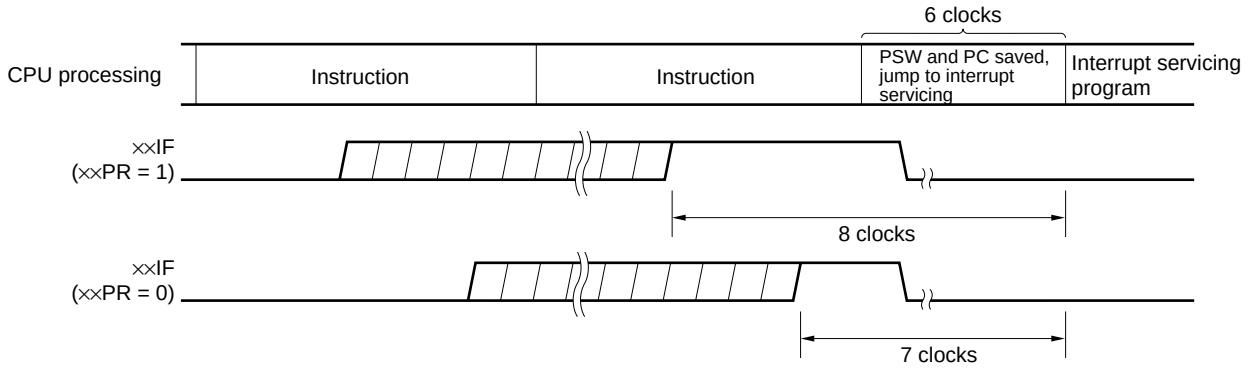
Restoring from an interrupt is possible by using the RETI instruction.

Figure 14-7. Interrupt Request Acknowledgment Processing Algorithm



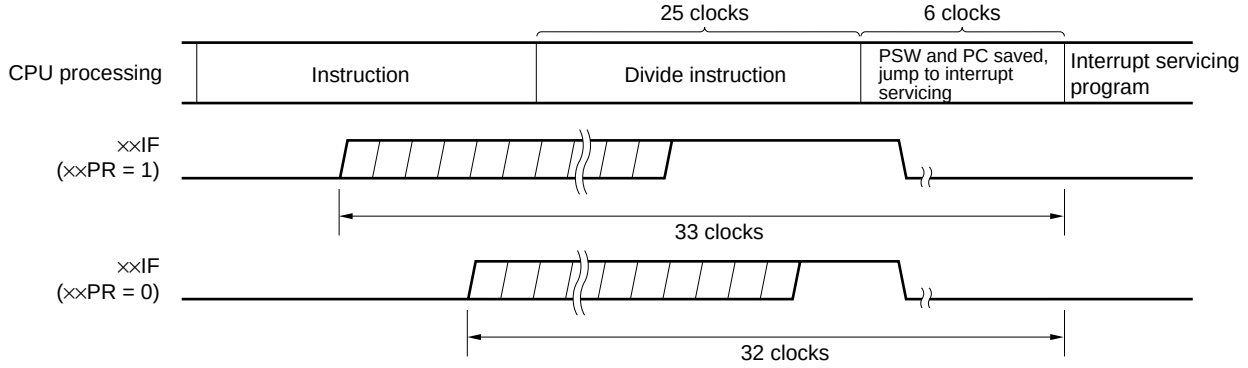
××IF: Interrupt request flag
××MK: Interrupt mask flag
××PR: Priority specification flag
IE: Flag that controls acknowledgment of maskable interrupt request (1 = Enable, 0 = Disable)
ISP: Flag that indicates the priority level of the interrupt currently being serviced (0 = high-priority interrupt servicing, 1 = No interrupt request acknowledged, or low-priority interrupt servicing)

Figure 14-8. Interrupt Request Acknowledgment Timing (Minimum Time)



Remark 1 clock: 1/f_{CPU} (f_{CPU}: CPU clock)

Figure 14-9. Interrupt Request Acknowledgment Timing (Maximum Time)



Remark 1 clock: 1/f_{CPU} (f_{CPU}: CPU clock)

14.4.2 Software interrupt request acknowledgment

A software interrupt acknowledge is acknowledged by BRK instruction execution. Software interrupts cannot be disabled.

If a software interrupt request is acknowledged, the contents are saved into the stacks in the order of the program status word (PSW), then program counter (PC), the IE flag is reset (0), and the contents of the vector table (003EH, 003FH) are loaded into the PC and branched.

Restoring from a software interrupt is possible by using the RETB instruction.

Caution Do not use the RETI instruction for restoring from the software interrupt.

14.4.3 Multiple interrupt servicing

Multiple interrupt servicing occurs when another interrupt request is acknowledged during execution of an interrupt.

Multiple interrupt servicing does not occur unless the interrupt request acknowledgment enabled state is selected (IE = 1). When an interrupt request is acknowledged, interrupt request acknowledgment becomes disabled (IE = 0). Therefore, to enable multiple interrupt servicing, it is necessary to set (1) the IE flag with the EI instruction during interrupt servicing to enable interrupt acknowledgment.

Moreover, even if interrupts are enabled, multiple interrupt servicing may not be enabled, this being subject to interrupt priority control. Two types of priority control are available: default priority control and programmable priority control. Programmable priority control is used for multiple interrupt servicing.

In the interrupt enabled state, if an interrupt request with a priority equal to or higher than that of the interrupt currently being serviced is generated, it is acknowledged for multiple interrupt servicing. If an interrupt with a priority lower than that of the interrupt currently being serviced is generated during interrupt servicing, it is not acknowledged for multiple interrupt servicing. Interrupt requests that are not enabled because interrupts are in the interrupt disabled state or because they have a lower priority are held pending. When servicing of the current interrupt ends, the pending interrupt request is acknowledged following execution of at least one main processing instruction execution.

Table 14-5 shows relationship between interrupt requests enabled for multiple interrupt servicing and Figure 14-10 shows multiple interrupt servicing examples.

Table 14-5. Relationship Between Interrupt Requests Enabled for Multiple Interrupt Servicing During Interrupt Servicing

Multiple Interrupt Request / Interrupt Being Serviced		Maskable Interrupt Request				Software Interrupt Request
		PR = 0		PR = 1		
		IE = 1	IE = 0	IE = 1	IE = 0	
Maskable interrupt	ISP = 0	○	×	×	×	○
	ISP = 1	○	×	○	×	○
Software interrupt		○	×	○	×	○

Remarks 1. ○: Multiple interrupt servicing enabled

2. ×: Multiple interrupt servicing disabled

3. ISP and IE are flags contained in the PSW.

ISP = 0: An interrupt with higher priority is being serviced.

ISP = 1: No interrupt request has been acknowledged, or an interrupt with a lower priority is being serviced.

IE = 0: Interrupt request acknowledgment is disabled.

IE = 1: Interrupt request acknowledgment is enabled.

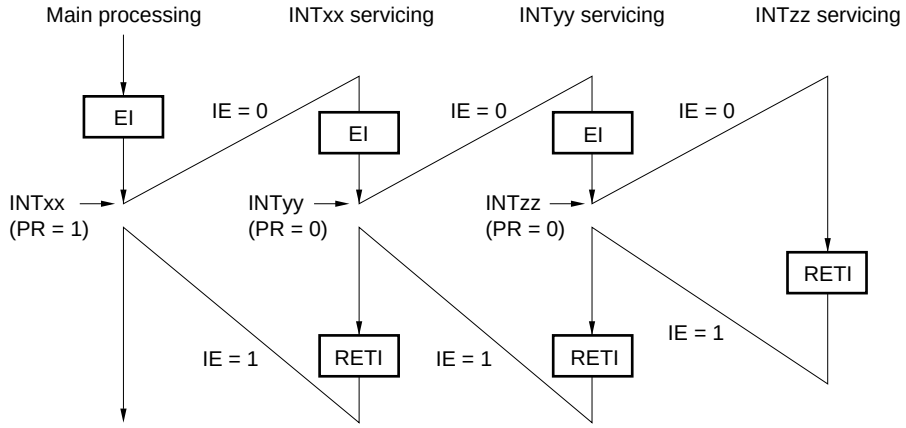
4. PR is a flag contained in PR0L, PR0H, and PR1L.

PR = 0: Higher priority level

PR = 1: Lower priority level

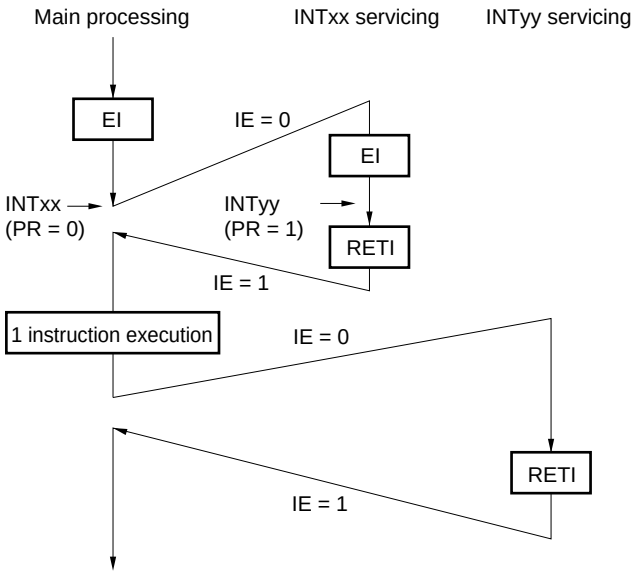
Figure 14-10. Examples of Multiple Interrupt Servicing (1/2)

Example 1. Multiple interrupt servicing occurs twice



During servicing of interrupt INTxx, two interrupt requests, INTyy and INTzz, are acknowledged, and multiple interrupt servicing takes place. Before each interrupt request is acknowledged, the EI instruction must always be issued to enable interrupt request acknowledgment.

Example 2. Multiple interrupt servicing does not occur due to priority control

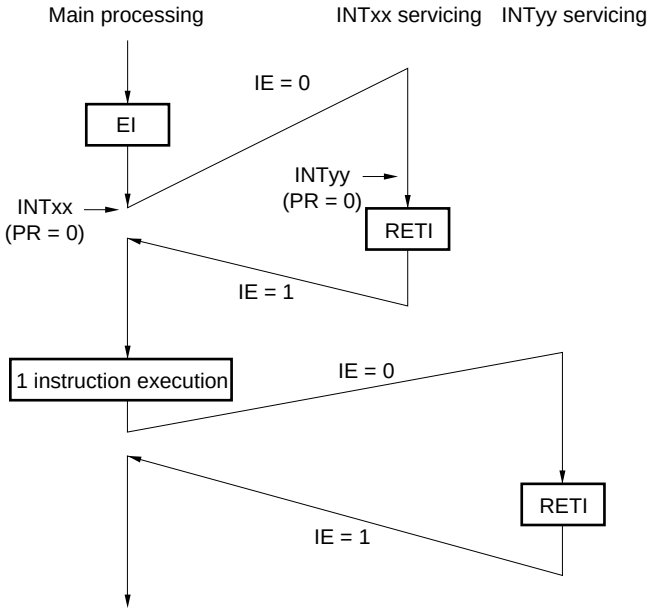


Interrupt request INTyy issued during servicing of interrupt INTxx is not acknowledged because its priority is lower than that of INTxx, and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 0: Higher priority level
PR = 1: Lower priority level
IE = 0: Interrupt request acknowledgment disabled

Figure 14-10. Examples of Multiple Interrupt Servicing (2/2)

Example 3. Multiple interrupt servicing does not occur because interrupts are not enabled



Interrupts are not enabled during servicing of interrupt INTxx (EI instruction is not issued), therefore, interrupt request INTyy is not acknowledged and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 0: Higher priority level
IE = 0: Interrupt request acknowledgment disabled

14.4.4 Interrupt request hold

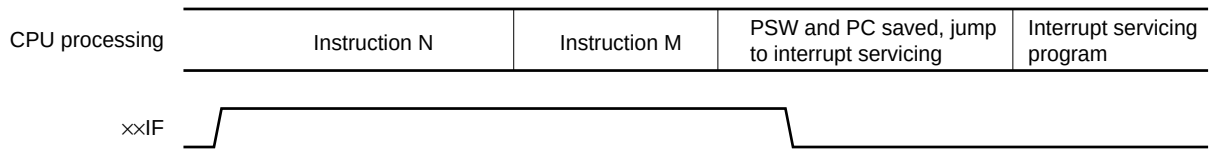
There are instructions where, even if an interrupt request is issued for them while another instruction is being executed, request acknowledgment is held pending until the end of execution of the next instruction. These instructions (interrupt request hold instructions) are listed below.

- MOV PSW, #byte
- MOV A, PSW
- MOV PSW, A
- MOV1 PSW. bit, CY
- MOV1 CY, PSW. bit
- AND1 CY, PSW. bit
- OR1 CY, PSW. bit
- XOR1 CY, PSW. bit
- SET1 PSW. bit
- CLR1 PSW. bit
- RETB
- RETI
- PUSH PSW
- POP PSW
- BT PSW. bit, $addr16
- BF PSW. bit, $addr16
- BTCLR PSW. bit, $addr16
- EI
- DI
- Manipulation instructions for the IF0L, IF0H, IF1L, MK0L, MK0H, MK1L, PR0L, PR0H, and PR1L registers.

Caution The BRK instruction is not one of the above-listed interrupt request hold instructions. However, the software interrupt activated by executing the BRK instruction causes the IE flag to be cleared. Therefore, even if a maskable interrupt request is generated during execution of the BRK instruction, the interrupt request is not acknowledged.

Figure 14-11 shows the timing at which interrupt requests are held pending.

Figure 14-11. Interrupt Request Hold



Remarks 1. Instruction N: Interrupt request hold instruction

2. Instruction M: Instruction other than interrupt request hold instruction

3. The ××PR (priority level) values do not affect the operation of ××IF (interrupt request).

CHAPTER 15 STANDBY FUNCTION

15.1 Standby Function and Configuration

15.1.1 Standby function

The standby function is designed to reduce the operating current of the system. The following two modes are available.

(1) HALT mode

HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the high-speed system clock oscillator, internal high-speed oscillator, or internal low-speed oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.

(2) STOP mode

STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and internal high-speed oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current.

Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

In either of these two modes, all the contents of registers, flags and data memory just before the standby mode is set are held. The I/O port output latches and output buffer statuses are also held.

Cautions

1. **When shifting to the STOP mode, be sure to stop the peripheral hardware operation operating with main system clock before executing STOP instruction.**
2. **The following sequence is recommended for operating current reduction of the A/D converter when the standby function is used: First clear bit 7 (ADCS) and bit 0 (ADCE) of the A/D converter mode register 0 (ADM0) to 0 to stop the A/D conversion operation, and then execute the STOP instruction.**
3. **Stop the operational amplifier before executing the STOP instruction.**

15.1.2 Registers controlling standby function

The standby function is controlled by the following two registers.

- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)

Remark For the registers that start, stop, or select the clock, refer to **CHAPTER 5 CLOCK GENERATOR**.

(1) Oscillation stabilization time counter status register (OSTC)

This is the register that indicates the count status of the X1 clock oscillation stabilization time counter. When X1 clock oscillation starts with the internal high-speed oscillation clock used as the CPU clock, the X1 clock oscillation stabilization time can be checked.

OSTC can be read by a 1-bit or 8-bit memory manipulation instruction.

When reset is released (reset by $\overline{\text{RESET}}$ input, POC, LVI, and WDT), the STOP instruction and MSTOP (bit 7 of MOC register) = 1, clear OSTC to 00H.

Figure 15-1. Format of Oscillation Stabilization Time Counter Status Register (OSTC)

Address: FFA3H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	0	0	0	MOST11	MOST13	MOST14	MOST15	MOST16

MOST11	MOST13	MOST14	MOST15	MOST16	Oscillation stabilization time status	
						f_X = 10 MHz
1	0	0	0	0	$2^{11}/f_X$ min.	204.8 μs min.
1	1	0	0	0	$2^{13}/f_X$ min.	819.2 μs min.
1	1	1	0	0	$2^{14}/f_X$ min.	1.64 ms min.
1	1	1	1	0	$2^{15}/f_X$ min.	3.27 ms min.
1	1	1	1	1	$2^{16}/f_X$ min.	6.55 ms min.

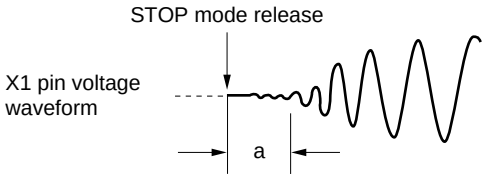
Cautions 1. After the above time has elapsed, the bits are set to 1 in order from MOST11 and remain 1.

2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts (“a” below).



Remark f_X: X1 clock oscillation frequency

(2) Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation waits for the time set using OSTS after the STOP mode is released.

When the internal high-speed oscillation clock is selected as the CPU clock, confirm with OSTC that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using OSTC.

OSTS can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets OSTS to 05H.

Figure 15-2. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection	
				f_X = 10 MHz
0	0	1	$2^{11}/f_X$	204.8 µs
0	1	0	$2^{13}/f_X$	819.2 µs
0	1	1	$2^{14}/f_X$	1.64 ms
1	0	0	$2^{15}/f_X$	3.27 ms
1	0	1	$2^{16}/f_X$	6.55 ms
Other than above			Setting prohibited	

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

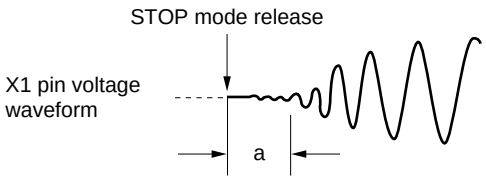
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts (“a” below).



Remark f_X: X1 clock oscillation frequency

15.2 Standby Function Operation

15.2.1 HALT mode

(1) HALT mode

The HALT mode is set by executing the HALT instruction. HALT mode can be set regardless of whether the CPU clock before the setting was the high-speed system clock, or internal high-speed oscillation clock.

The operating statuses in the HALT mode are shown below.

Table 15-1. Operating Statuses in HALT Mode

HALT Mode Setting / Item			When HALT Instruction Is Executed While CPU Is Operating on Main System Clock		
			When CPU Is Operating on Internal High-Speed Oscillation Clock (f_{IH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EXCLK})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{IH}	Operation continues (cannot be stopped)	Status before HALT mode was set is retained	
		f_X	Status before HALT mode was set is retained	Operation continues (cannot be stopped)	Status before HALT mode was set is retained
		f_{EXCLK}	Operates or stops by external clock input		Operation continues (cannot be stopped)
	f_{IL}		Status before HALT mode was set is retained		
CPU			Operation stopped		
Flash memory					
RAM			Status before HALT mode was set is retained		
Port (latch)					
16-bit timer/event counter 00			Operable		
8-bit timer/event counter51					
8-bit timer H1					
Watchdog timer			Operable. Clock supply to watchdog timer stops when “internal low-speed oscillator can be stopped by software” is set by option byte.		
A/D converter			Operable		
Operational amplifiers 0, 1					
Comparator					
Serial interface UART0					
Power-on-clear function					
Low-voltage detection function					
External interrupt					

Remark f_{IH}: Internal high-speed oscillation clock, f_X: X1 clock
f_{EXCLK}: External main system clock, f_{IL}: Internal low-speed oscillation clock

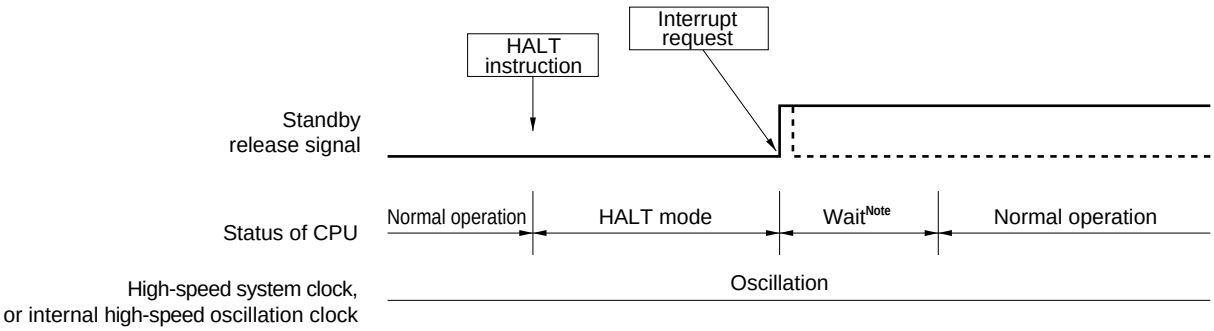
(2) HALT mode release

The HALT mode can be released by the following two sources.

(a) Release by unmasked interrupt request

When an unmasked interrupt request is generated, the HALT mode is released. If interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 15-3. HALT Mode Release by Interrupt Request Generation



Note The wait time is as follows:

- When vectored interrupt servicing is carried out: 11 or 12 clocks
- When vectored interrupt servicing is not carried out: 4 or 5 clocks

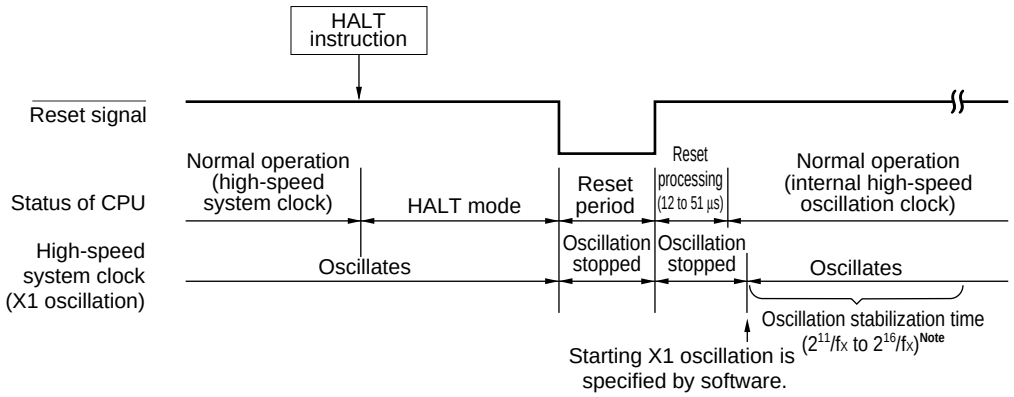
Remark The broken lines indicate the case when the interrupt request which has released the standby mode is acknowledged.

(b) Release by reset signal generation

When the reset signal is generated, HALT mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

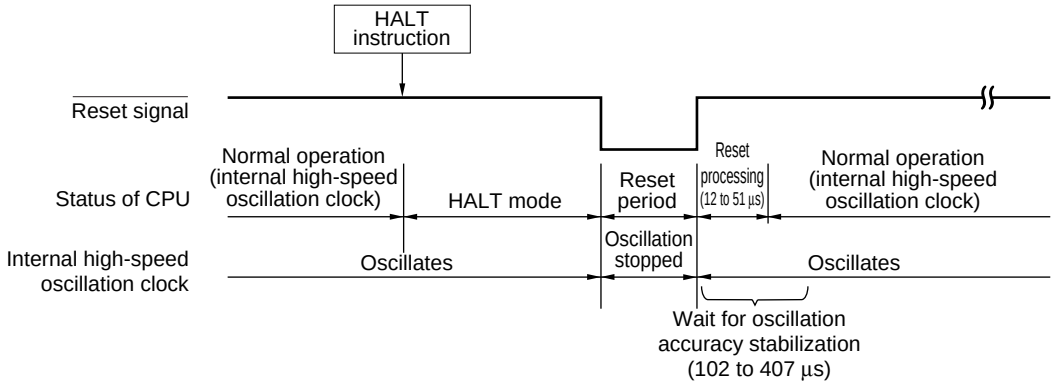
Figure 15-4. HALT Mode Release by Reset

(1) When high-speed system clock is used as CPU clock



Note Oscillation stabilization time is not required when using the external main system clock (f_{EXCLK}) as the high-speed system clock.

(2) When internal high-speed oscillation clock is used as CPU clock



Remark f_X: X1 clock oscillation frequency

Table 15-2. Operation in Response to Interrupt Request in HALT Mode

Release Source	MK××	PR××	IE	ISP	Operation
Maskable interrupt request	0	0	0	×	Next address instruction execution
	0	0	1	×	Interrupt servicing execution
	0	1	0	1	Next address instruction execution
	0	1	×	0	
	0	1	1	1	Interrupt servicing execution
	1	×	×	×	HALT mode held
Reset	–	–	×	×	Reset processing

×: don't care

15.2.2 STOP mode

(1) STOP mode setting and operating statuses

The STOP mode is set by executing the STOP instruction, and it can be set only when the CPU clock before the setting was the main system clock.

Caution Because the interrupt request signal is used to clear the standby mode, if there is an interrupt source with the interrupt request flag set and the interrupt mask flag reset, the standby mode is immediately cleared if set. Thus, the STOP mode is reset to the HALT mode immediately after execution of the STOP instruction and the system returns to the operating mode as soon as the wait time set using the oscillation stabilization time select register (OSTS) has elapsed.

The operating statuses in the STOP mode are shown below.

Table 15-3. Operating Statuses in STOP Mode

STOP Mode Setting / Item			When STOP Instruction Is Executed While CPU Is Operating on Main System Clock		
			When CPU Is Operating on Internal High-Speed Oscillation Clock (f_{IH})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EXCLK})
System clock			Clock supply to the CPU is stopped		
	Main system clock	f_{IH}	Stopped		
		f_X			
		f_{EXCLK}	Input invalid		
	f_{IL}		Status before STOP mode was set is retained		
CPU			Operation stopped		
Flash memory					
RAM			Status before STOP mode was set is retained		
Port (latch)					
16-bit timer/event counter 00			Operation stopped		
8-bit timer/event counter51			Operable only when TI51 is selected as the count clock		
8-bit timer H1			Operable only when f_{IL}, $f_{IL}/2^7$, $f_{IL}/2^9$ is selected as the count clock		
Watchdog timer			Operable. Clock supply to watchdog timer stops when “internal low-speed oscillator can be stopped by software” is set by option byte.		
A/D converter			Operation stopped		
Operational amplifiers 0, 1			Operable		
Comparator			Operation prohibited		
Serial interface UART0			Operable only when TM51 output is selected as the serial clock during 8-bit timer/event counter 51 operation		
Power-on-clear function			Operable		
Low-voltage detection function					
External interrupt					

Remark f_{IH}: Internal high-speed oscillation clock, f_X: X1 clock
f_{EXCLK}: External main system clock, f_{IL}: Internal low-speed oscillation clock

Cautions 1. To use the peripheral hardware that stops operation in the STOP mode, and the peripheral hardware for which the clock that stops oscillating in the STOP mode after the STOP mode is released, restart the peripheral hardware.

2. Even if "internal low-speed oscillator can be stopped by software" is selected by the option byte, the internal low-speed oscillation clock continues in the STOP mode in the status before the STOP mode is set. To stop the internal low-speed oscillator's oscillation in the STOP mode, stop it by software and then execute the STOP instruction.

3. To shorten oscillation stabilization time after the STOP mode is released when the CPU operates with the high-speed system clock (X1 oscillation), switch the CPU clock to the internal high-speed oscillation clock before the execution of the STOP instruction using the following procedure.

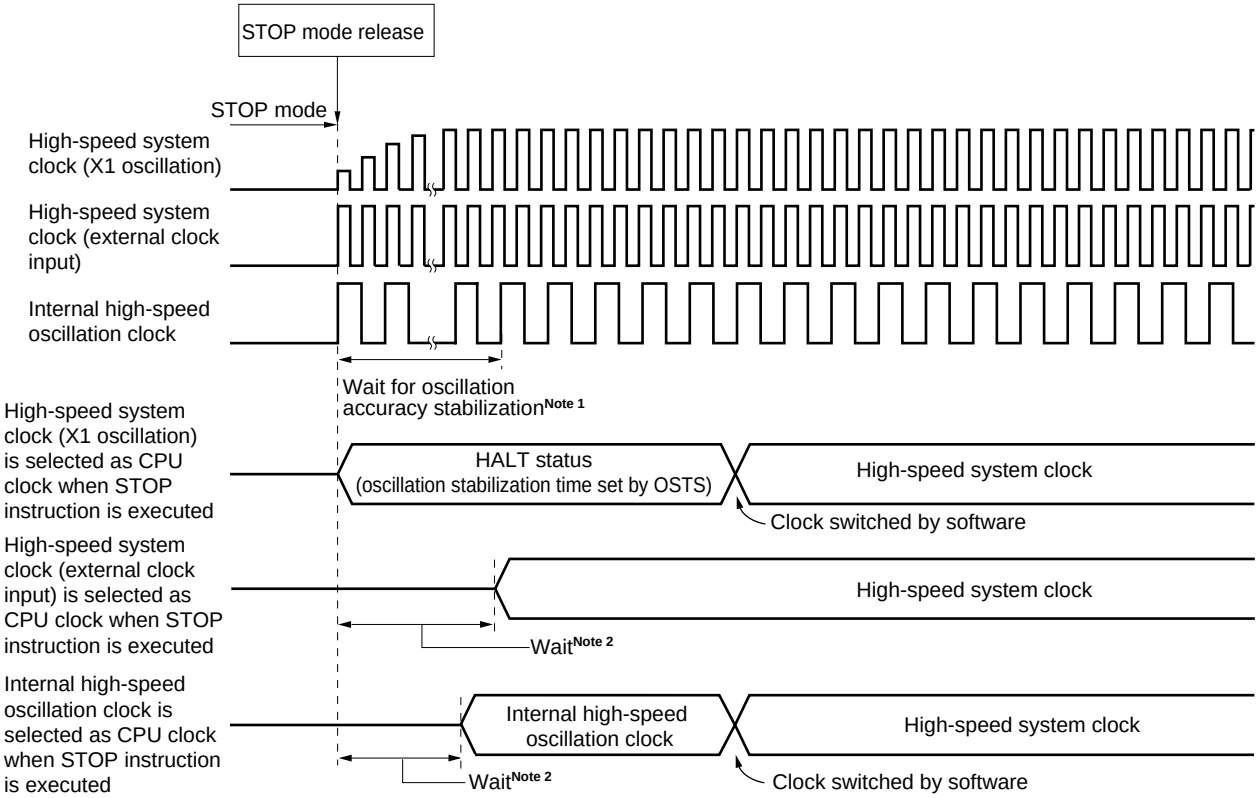
<1> Set RSTOP to 0 (starting oscillation of the internal high-speed oscillator) → <2> Set MCM0 to 0 (switching the CPU from X1 oscillation to internal high-speed oscillation) → <3> Check that MCS is 0 (checking the CPU clock) → <4> Check that RSTS is 1 (checking internal high-speed oscillation operation) → <5> Execute the STOP instruction

Before changing the CPU clock from the internal high-speed oscillation clock to the high-speed system clock (X1 oscillation) after the STOP mode is released, check the oscillation stabilization time with the oscillation stabilization time counter status register (OSTC).

4. Execute the STOP instruction after having confirmed that the internal high-speed oscillator is operating stably (RSTS = 1).

(2) STOP mode release

Figure 15-5. Operation Timing When STOP Mode Is Released (When Unmasked Interrupt Request Is Generated)



Notes 1. The wait time for oscillation accuracy stabilization is as follows:

- RMC register = 00H: 102 to 407 μs
- RMC register = 56H/59H: 120 to 481 μs

2. The wait time is as follows:

- When vectored interrupt servicing is carried out: 17 or 18 clocks
- When vectored interrupt servicing is not carried out: 11 or 12 clocks

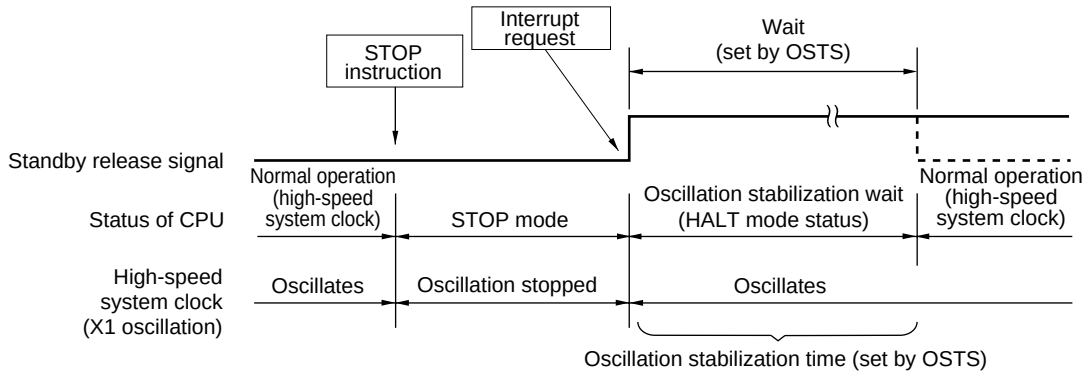
The STOP mode can be released by the following two sources.

(a) Release by unmasked interrupt request

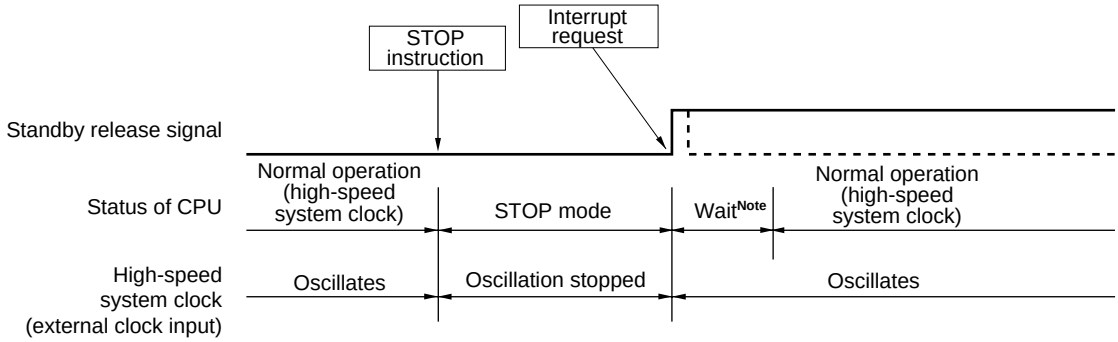
When an unmasked interrupt request is generated, the STOP mode is released. After the oscillation stabilization time has elapsed, if interrupt acknowledgment is enabled, vectored interrupt servicing is carried out. If interrupt acknowledgment is disabled, the next address instruction is executed.

Figure 15-6. STOP Mode Release by Interrupt Request Generation (1/2)

(1) When high-speed system clock (X1 oscillation) is used as CPU clock



(2) When high-speed system clock (external clock input) is used as CPU clock



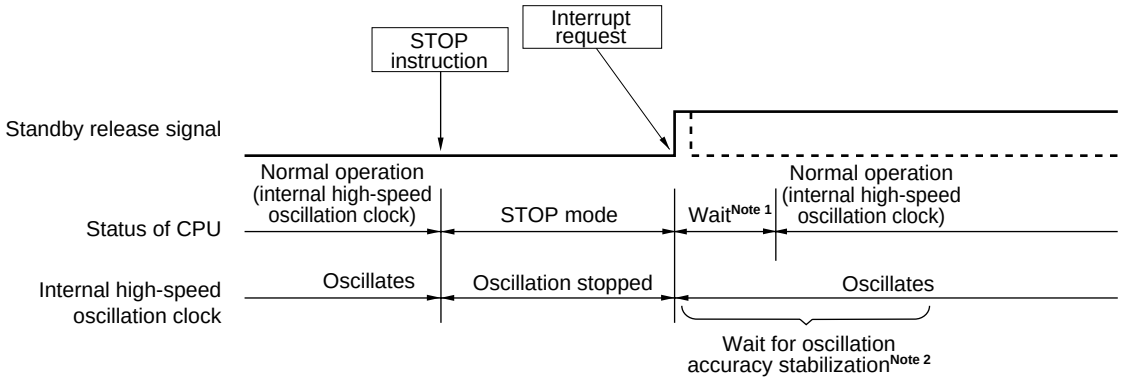
Note The wait time is as follows:

- When vectored interrupt servicing is carried out: 17 or 18 clocks
- When vectored interrupt servicing is not carried out: 11 or 12 clocks

Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

Figure 15-6. STOP Mode Release by Interrupt Request Generation (2/2)

(3) When internal high-speed oscillation clock is used as CPU clock



Notes 1. The wait time is as follows:

- When vectored interrupt servicing is carried out: 17 or 18 clocks
- When vectored interrupt servicing is not carried out: 11 or 12 clocks

2. The wait time for oscillation accuracy stabilization is as follows:

- RMC register = 00H: 102 to 407 µs
- RMC register = 56H/59H: 120 to 481 µs

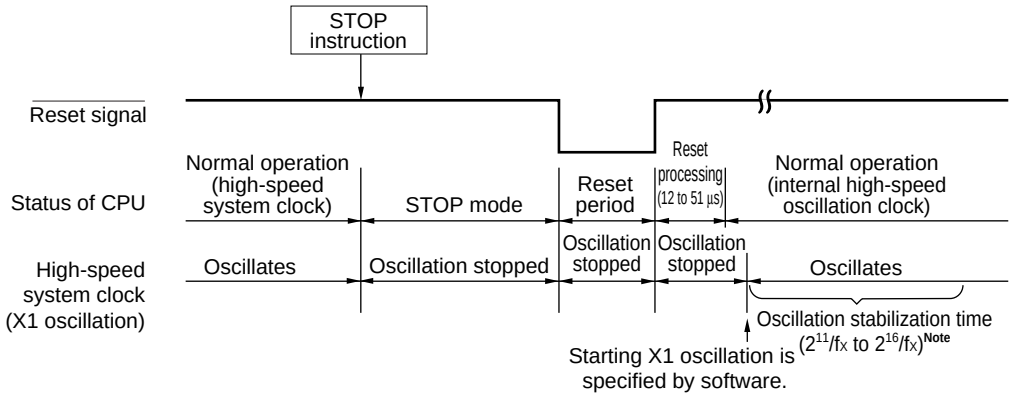
Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

(b) Release by reset signal generation

When the reset signal is generated, STOP mode is released, and then, as in the case with a normal reset operation, the program is executed after branching to the reset vector address.

Figure 15-7. STOP Mode Release by Reset

(1) When high-speed system clock is used as CPU clock



Note Oscillation stabilization time is not required when using the external main system clock (f_{EXCLK}) as the high-speed system clock.

Remark f_X: X1 clock oscillation frequency

(2) When internal high-speed oscillation clock is used as CPU clock

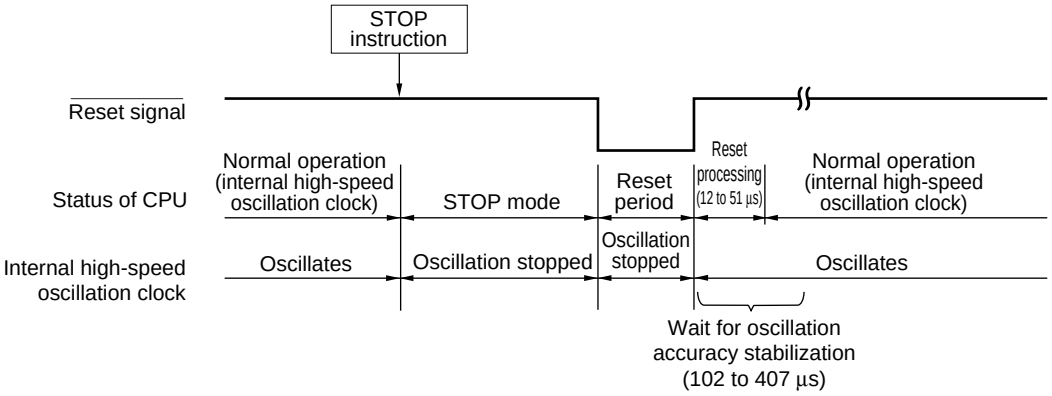


Table 15-4. Operation in Response to Interrupt Request in STOP Mode

Release Source	MK××	PR××	IE	ISP	Operation
Maskable interrupt request	0	0	0	×	Next address instruction execution
	0	0	1	×	Interrupt servicing execution
	0	1	0	1	Next address instruction execution
	0	1	×	0	
	0	1	1	1	Interrupt servicing execution
	1	×	×	×	STOP mode held
Reset	–	–	×	×	Reset processing

×: don't care

CHAPTER 16 RESET FUNCTION

The following four operations are available to generate a reset signal.

(1) External reset input via $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer program loop detection
(3) Internal reset by comparison of supply voltage and detection voltage of power-on-clear (POC) circuit
(4) Internal reset by comparison of supply voltage of the low-voltage detector (LVI) and detection voltage

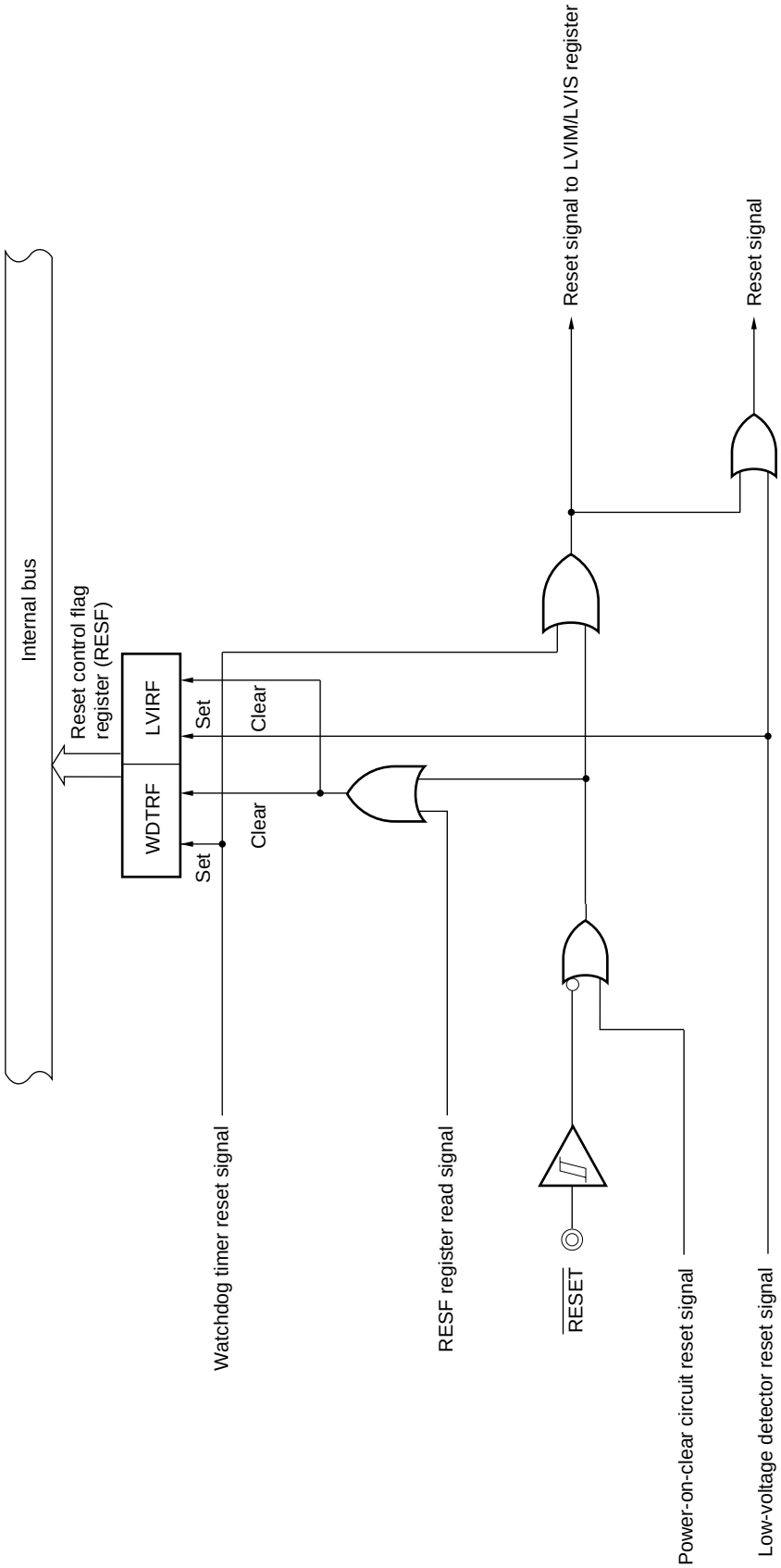
External and internal resets start program execution from the address at 0000H and 0001H when the reset signal is generated.

A reset is applied when a low level is input to the $\overline{\text{RESET}}$ pin, the watchdog timer overflows, or by POC and LVI circuit voltage detection, and each item of hardware is set to the status shown in Tables 16-1 and 16-2. Each pin is high impedance during reset signal generation or during the oscillation stabilization time just after a reset release.

When a low level is input to the $\overline{\text{RESET}}$ pin, the device is reset. It is released from the reset status when a high level is input to the $\overline{\text{RESET}}$ pin and program execution is started with the internal high-speed oscillation clock after reset processing. A reset by the watchdog timer is automatically released, and program execution starts using the internal high-speed oscillation clock (refer to **Figures 16-2** to **16-4**) after reset processing. Reset by POC and LVI circuit power supply detection is automatically released when $V_{DD} \geq V_{POR}$ or $V_{DD} \geq V_{LVI}$ after the reset, and program execution starts using the internal high-speed oscillation clock (refer to **CHAPTER 17 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 18 LOW-VOLTAGE DETECTOR**) after reset processing.

Cautions 1. For an external reset, input a low level for 10 µs or more to the $\overline{\text{RESET}}$ pin.
(If an external reset is effected upon power application, the period during which the supply voltage is outside the operating range (V_{DD} < 1.8 V) is not counted in the 10 µs. However, the low-level input may be continued before POC is released.)
2. During reset signal generation, the X1 clock, internal high-speed oscillation clock, and internal low-speed oscillation clock stop oscillating. External main system clock input becomes invalid.
3. When the STOP mode is released by a reset, the RAM contents in the STOP mode are held during reset input. However, because SFR is initialized, the port pins become high-impedance.

Figure 16-1. Block Diagram of Reset Function



Caution An LVI circuit internal reset does not reset the LVI circuit.

Remarks 1. LVIM: Low-voltage detection register

2. LVIS: Low-voltage detection level selection register

Figure 16-2. Timing of Reset by $\overline{\text{RESET}}$ Input

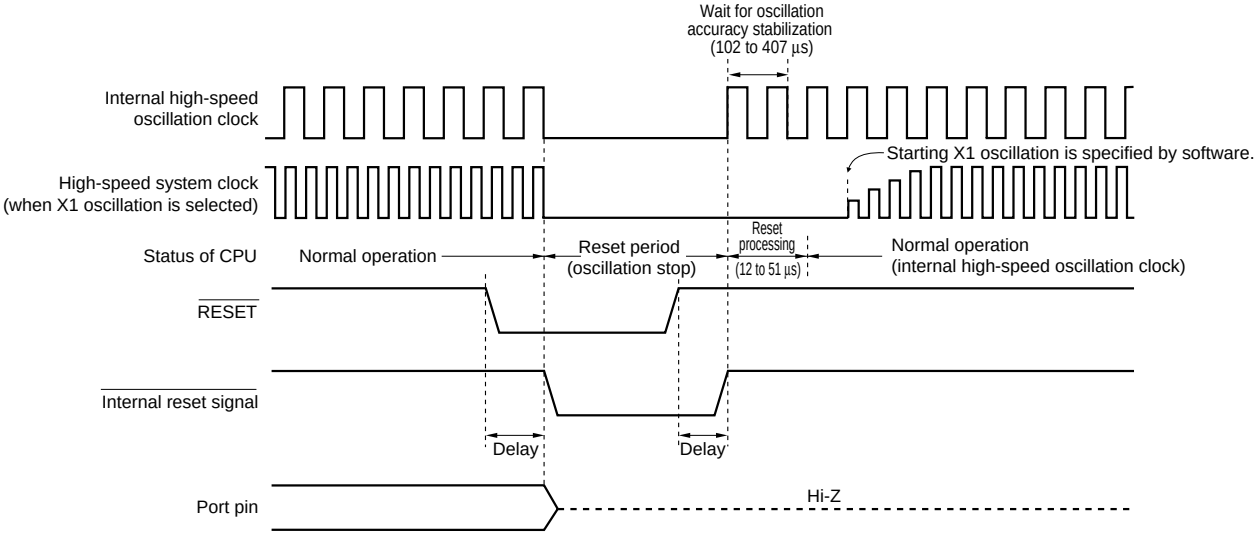
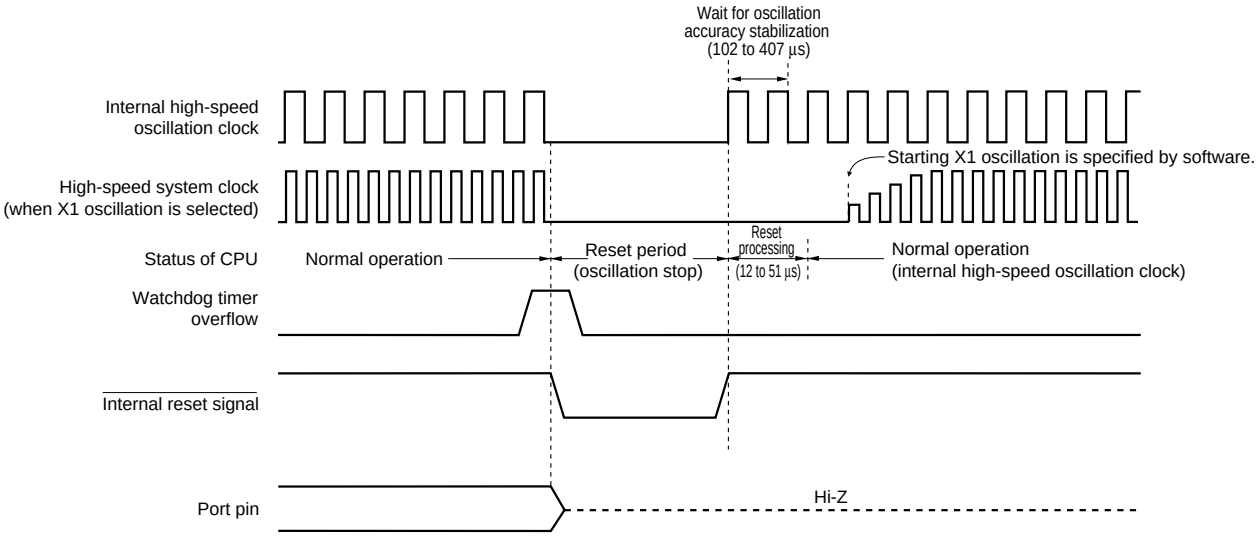
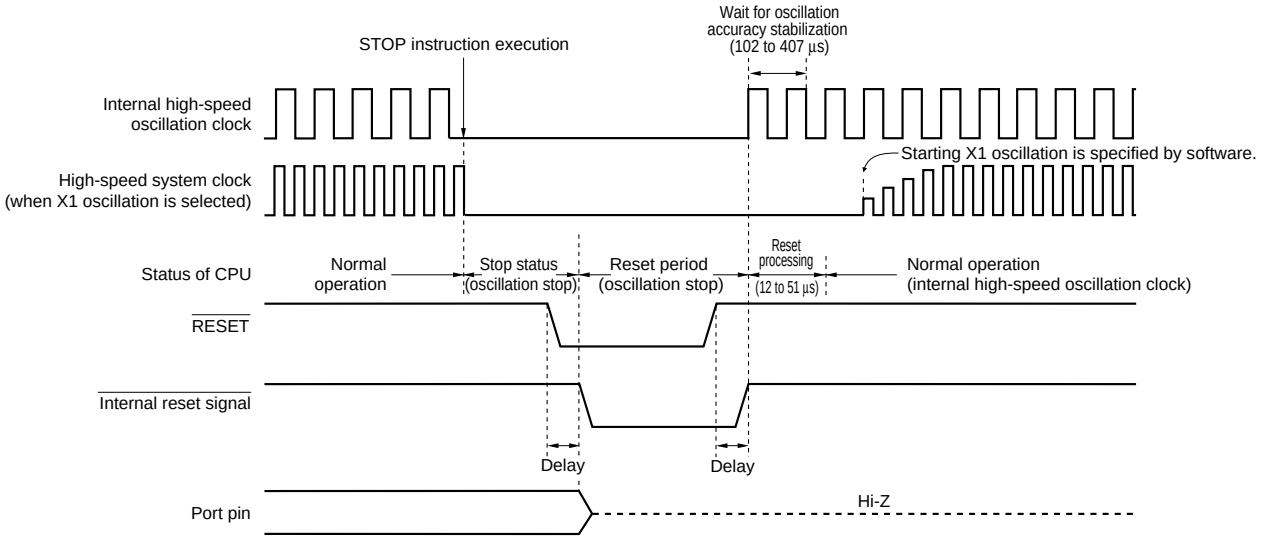


Figure 16-3. Timing of Reset Due to Watchdog Timer Overflow



Caution A watchdog timer internal reset resets the watchdog timer.

Figure 16-4. Timing of Reset in STOP Mode by $\overline{\text{RESET}}$ Input



Remark For the reset timing of the power-on-clear circuit and low-voltage detector, refer to **CHAPTER 17 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 18 LOW-VOLTAGE DETECTOR**.

Table 16-1. Operation Statuses During Reset Period

Item			During Reset Period
System clock			Clock supply to the CPU is stopped.
	Main system clock	f_{IH}	Operation stopped
		f_X	Operation stopped (X1 and X2 pins are input port mode)
		f_{EXCLK}	Clock input invalid (EXCLK pin is input port mode)
	f_{IL}		Operation stopped
CPU			
Flash memory			
RAM			Operation stopped (The value, however, is retained when the voltage is at least the power-onclear detection voltage.)
Port (latch)			Operation stopped
16-bit timer/event counter 00			
8-bit timer/event counter51			
8-bit timer H1			
Watchdog timer			
A/D converter			
Operational amplifier 0 (AMP0)			
Operational amplifier 1 (AMP1)			
Comparator			
Serial interface UART0			
External interrupt			
Power-on-clear function			Operable
Low-voltage detection function			Operation stopped (however, operation continues at LVI reset)
On-chip debug function			Operation stopped

Remark f_{IH}: Internal high-speed oscillation clock, f_X: X1 clock
f_{EXCLK}: External main system clock, f_{IL}: Internal low-speed oscillation clock

Table 16-2. Hardware Statuses After Reset Acknowledgment (1/3)

Hardware		After Reset Acknowledgment[Note 1]
Program counter (PC)		The contents of the reset vector table (0000H, 0001H) are set.
Stack pointer (SP)		Undefined
Program status word (PSW)		02H
RAM	Data memory	Undefined[Note 2]
	General-purpose registers	Undefined[Note 2]
Port registers 2, 3, 12 (P2, P3, P12) (output latches)		00H
Port mode registers 2, 3, 12 (PM2, PM3, PM12)		FFH
Pull-up resistor option registers 3 (PU3)		00H
Pull-up resistor option register 12 (PU12)		20H
Reset pin mode register (RSTMASK)		00H
Internal memory size switching register (IMS)		CFH[Note 3]

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. When a reset is executed in the standby mode, the pre-reset status is held even after reset.

3. Reset signal generation makes the setting of the ROM area undefined. Therefore, set the value corresponding to each product as indicated below after release of reset.

Products	IMS	ROM Capacity	Internal High-Speed RAM Capacity
µPD79F7023	42H	8 KB	512 bytes
µPD79F7024	04H	16 KB	768 bytes

Table 16-2. Hardware Statuses After Reset Acknowledgment (2/3)

Hardware		Status After Reset Acknowledgment[Note 1]
Clock operation mode select register (OSCCTL)		00H
Processor clock control register (PCC)		01H
Internal oscillation mode register (RCM)		80H
Main OSC control register (MOC)		80H
Main clock mode register (MCM)		00H
Oscillation stabilization time counter status register (OSTC)		00H
Oscillation stabilization time select register (OSTS)		05H
16-bit timer/event counter 00	Timer counter 00 (TM00)	0000H
	Capture/compare registers 000, 010 (CR000, CR010)	0000H
	Mode control register 00 (TMC00)	00H
	Prescaler mode register 00 (PRM00)	00H
	Capture/compare control register 00 (CRC00)	00H
	Timer output control register 00 (TOC00)	00H
8-bit timer/event counter 51	Timer counter 51 (TM51)	00H
	Compare register 51 (CR51)	00H
	Timer clock selection register 51 (TCL51)	00H
	Mode control register 51 (TMC51)	00H
8-bit timer H1	Compare registers 01, 11 (CMP01, CMP11)	00H
	Mode register (TMHMD1)	00H
	Carrier control register 1 (TMCYC1)	00H
Watchdog timer	Enable register (WDTE)	1AH/9AH[Note 2]
A/D converter	8-bit A/D conversion result register H (ADCRH)	00H
	Mode register (ADM)	00H
	Analog input channel specification register (ADS)	00H
	A/D port configuration register (ADPC)	00H
Operational amplifier 0 (AMP0)	Operational amplifier control register (AMPM)	00H
Operational amplifier 1 (AMP1)		
Comparator	Comparator control register (CMPCTL)	00H
	Comparator port cofiguration register (CMPPC)	00H
Serial interface UART0	Receive buffer register 0 (RXB0)	FFH
	Transmit buffer register 0 (TXS0)	FFH
	Asynchronous serial interface operation mode register 0 (ASIM0)	01H
	Asynchronous serial interface reception error status register 0 (ASIS0)	00H
	Baud rate generator control register 0 (BRGC0)	1FH

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. The reset value of WDTE is determined by the option byte setting.

Table 16-2. Hardware Statuses After Reset Acknowledgment (3/3)

Hardware		Status After Reset Acknowledgment[Note 1]
Reset function	Reset control flag register (RESF)	00H[Note 2]
Low-voltage detector	Low-voltage detection register (LVIM)	00H[Note 2]
	Low-voltage detection level selection register (LVIS)	00H[Note 2]
Interrupt	Request flag registers 0L, 0H, 1L (IF0L, IF0H, IF1L)	00H
	Mask flag registers 0L, 0H, 1L (MK0L, MK0H, MK1L)	FFH
	Priority specification flag registers 0L, 0H, 1L (PR0L, PR0H, PR1L)	FFH
	External interrupt rising edge enable register (EGP)	00H
	External interrupt falling edge enable register (EGN)	00H
Regulator	Regulator mode control register (RMC)	00H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. These values vary depending on the reset source.

Register \ Reset Source		$\overline{\text{RESET}}$ Input	Reset by POC	Reset by WDT	Reset by LVI (Except Reset by LVI Default Start Function)	Reset by LVI Default Start Function
RESF	WDTRF flag	Cleared (0)	Cleared (0)	Set (1)	Held	Cleared (0)
	LVIRF flag			Held	Set (1)	
LVIM		Cleared (00H)	Cleared (00H)	Cleared (00H)	Held	Cleared (00H)
LVIS						

16.1 Register for Confirming Reset Source

Many internal reset generation sources exist in the µPD79F7023, 79F7024 microcontrollers. The reset control flag register (RESF) is used to store which source has generated the reset request.

RESF can be read by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input, reset by power-on-clear (POC) circuit, and reading RESF set RESF to 00H.

Figure 16-5. Format of Reset Control Flag Register (RESF)

Address: FFACH After reset: 00H[Note] R

Symbol	7	6	5	4	3	2	1	0
RESF	0	0	0	WDTRF	0	0	0	LVIRF

WDTRF	Internal reset request by watchdog timer (WDT)
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

LVIRF	Internal reset request by low-voltage detector (LVI)
0	Internal reset request is not generated, or RESF is cleared.
1	Internal reset request is generated.

Note The value after reset varies depending on the reset source.

Caution Do not read data by a 1-bit memory manipulation instruction.

The status of RESF when a reset request is generated is shown in Table 16-3.

Table 16-3. RESF Status When Reset Request Is Generated

Flag \ Reset Source	$\overline{\text{RESET}}$ Input	Reset by POC	Reset by WDT	Reset by LVI (Except Reset by LVI Default Start Function)	Reset by LVI Default Start Function
WDTRF	Cleared (0)	Cleared (0)	Set (1)	Held	Cleared (0)
LVIRF			Held	Set (1)	

CHAPTER 17 POWER-ON-CLEAR CIRCUIT

17.1 Functions of Power-on-Clear Circuit

The power-on-clear circuit (POC) has the following functions.

(1) In 1.59 V POC mode (option byte: LVISTART = 0)

- An internal reset signal is generated on power application. When the supply voltage (V_{DD}) exceeds the detection voltage (V_{POC} = 1.59 V ±0.15 V), the reset status is released.
- The supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.15 V) are compared. When $V_{DD} < V_{POC}$, the internal reset signal is generated. It is released when $V_{DD} \geq V_{POC}$.

(2) In 2.7 V/1.59 V POC mode (option byte: LVISTART = 1)

- An internal reset signal is generated on power application. When the supply voltage (V_{DD}) exceeds the detection voltage (V_{DDPOC} = 2.7 V ±0.2 V), the reset status is released.
- The supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.15 V) are compared. When $V_{DD} < V_{POC}$, the internal reset signal is generated. It is released when $V_{DD} \geq V_{DDPOC}$.

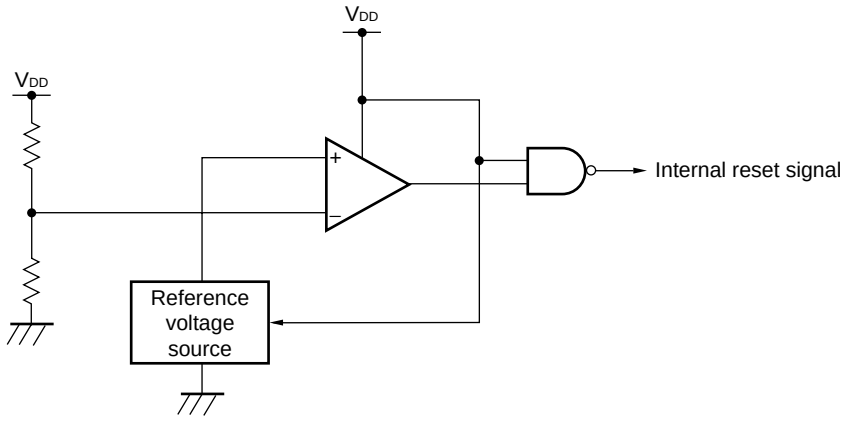
Caution If an internal reset signal is generated in the POC circuit, the reset control flag register (RESF) is cleared to 00H.

Remark The µPD79F7023, 79F7024 microcontrollers incorporate multiple hardware functions that generate an internal reset signal. A flag that indicates the reset source is located in the reset control flag register (RESF) for when an internal reset signal is generated by the watchdog timer (WDT) and low-voltage-detector (LVI). RESF is not cleared to 00H and the flag is set to 1 when an internal reset signal is generated by WDT or LVI. For details of RESF, refer to **CHAPTER 16 RESET FUNCTION**.

17.2 Configuration of Power-on-Clear Circuit

The block diagram of the power-on-clear circuit is shown in Figure 17-1.

Figure 17-1. Block Diagram of Power-on-Clear Circuit



17.3 Operation of Power-on-Clear Circuit

- An internal reset signal is generated on power application. When the supply voltage (V_{DD}) exceeds detection voltage (V_{POC} = 1.59 V ±0.15 V), the reset status is released.

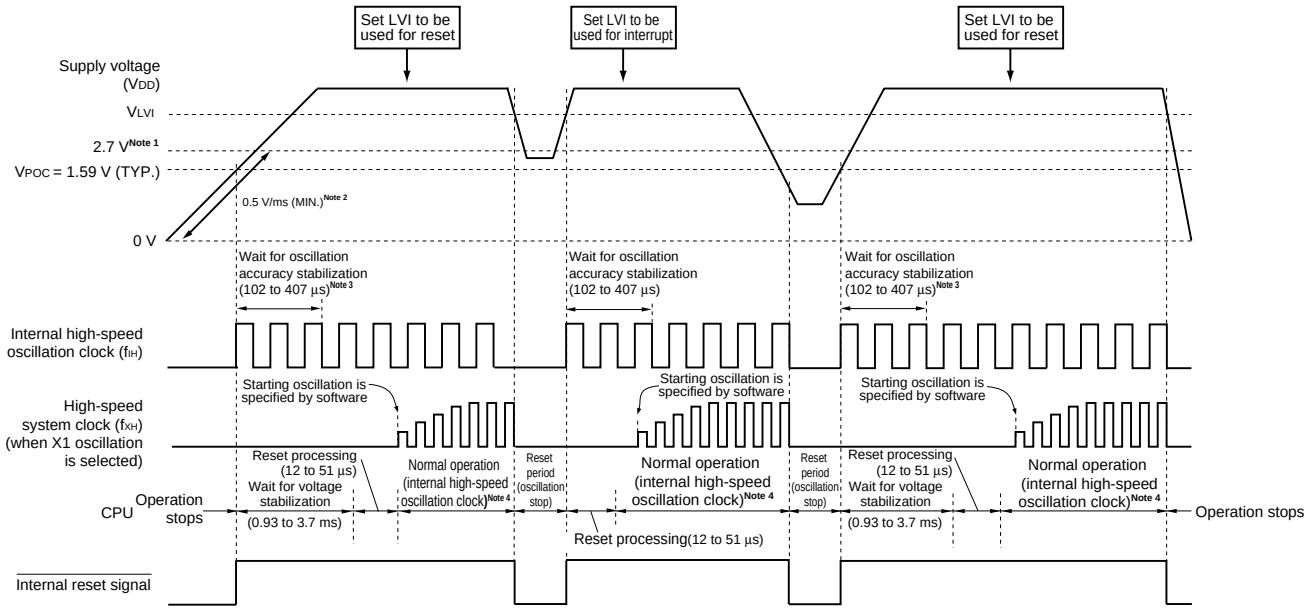
Caution If the LVI default function enabled is set by using an option byte, the reset signal is not released until the supply voltage (V_{DD}) exceeds 2.7 V ±0.1 V.

- The supply voltage (V_{DD}) and detection voltage (V_{POC} = 1.59 V ±0.15 V) are compared. When $V_{DD} < V_{PDR}$, the internal reset signal is generated.

The timing of generation of the internal reset signal by the power-on-clear circuit and low-voltage detector is shown below.

Figure 17-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (1/2)

(1) In 1.59 V POC mode (option byte: LVISTART = 0)



Notes 1. The operation guaranteed range is 2.7 V ≤ V_{DD} ≤ 5.5 V. To make the state at lower than 2.7 V reset state when the supply voltage falls, use the reset function of the low-voltage detector, or input the low level to the $\overline{\text{RESET}}$ pin.

2. If the rate at which the voltage rises to 2.7 V after power application is slower than 0.5 V/ms (MIN.), input a low level to the $\overline{\text{RESET}}$ pin before the voltage reaches to 2.7 V.

3. The internal voltage stabilization wait time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

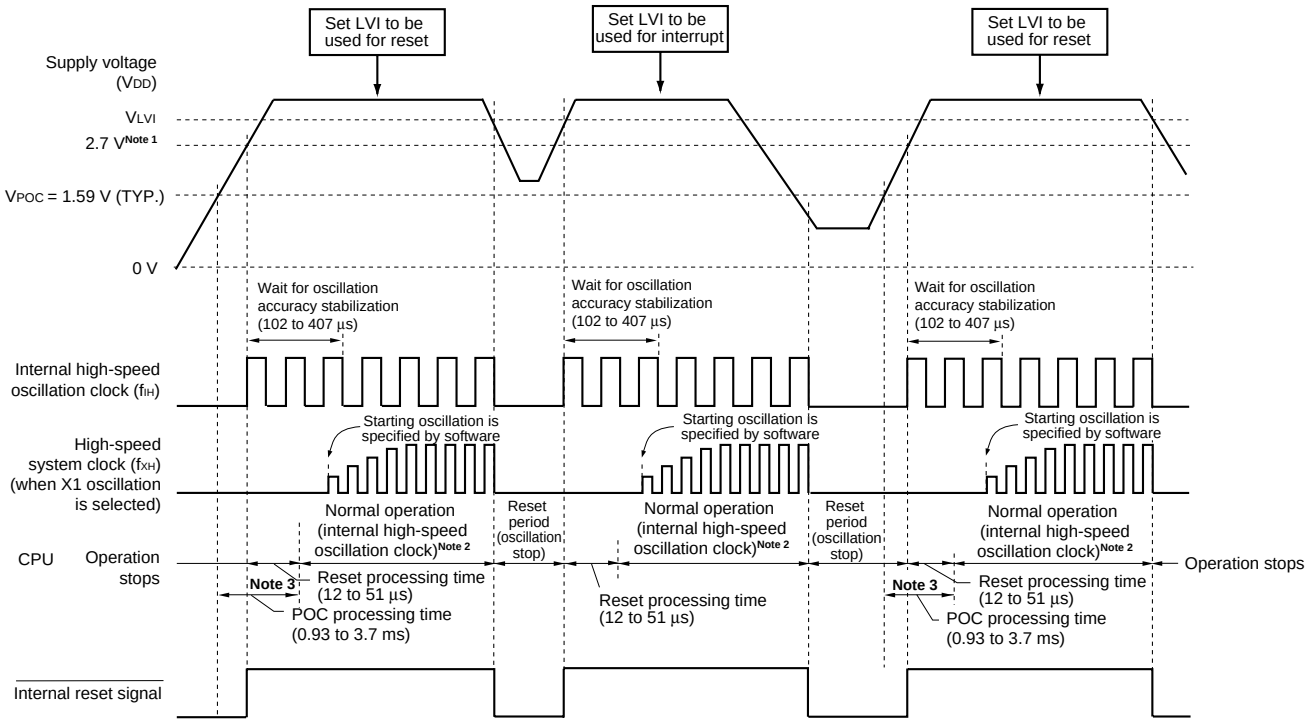
4. The internal high-speed oscillation clock or high-speed system clock can be selected as the CPU clock. To use the X1 clock, use the OSTC register to confirm the lapse of the oscillation stabilization time.

Caution Set the low-voltage detector by software after the reset status is released (refer to CHAPTER 18 LOW-VOLTAGE DETECTOR).

Remark V_{LVI}: LVI detection voltage
V_{POC}: Detection voltage

Figure 17-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (2/2)

(2) In 2.7 V/1.59 V POC mode (option byte: LVISTART = 1)



Notes 1. The operation guaranteed range is 2.7 V ≤ V_{DD} ≤ 5.5 V. To make the state at lower than 2.7 V reset state when the supply voltage falls, use the reset function of the low-voltage detector, or input the low level to the $\overline{\text{RESET}}$ pin.

2. The internal high-speed oscillation clock or high-speed system clock can be selected as the CPU clock. To use the X1 clock, use the OSTC register to confirm the lapse of the oscillation stabilization time.

3. The following times are required between reaching the POC detection voltage (1.59 V (TYP.)) and starting normal operation.

- When the time to reach 2.7 V (TYP.) from 1.59 V (TYP.) is less than 3.7 ms:
  A processing time of about 1.0 to 3.8 ms is required between reaching 1.59 V (TYP.) and starting normal operation.
- When the time to reach 2.7 V (TYP.) from 1.59 V (TYP.) is greater than 3.7 ms:
  A reset processing time of about 12 to 51 µs is required between reaching 2.7 V (TYP.) and starting normal operation.

Caution Set the low-voltage detector by software after the reset status is released (refer to CHAPTER 18 LOW-VOLTAGE DETECTOR).

Remark V_{LVI}: LVI detection voltage
V_{POC}: Detection voltage

17.4 Cautions for Power-on-Clear Circuit

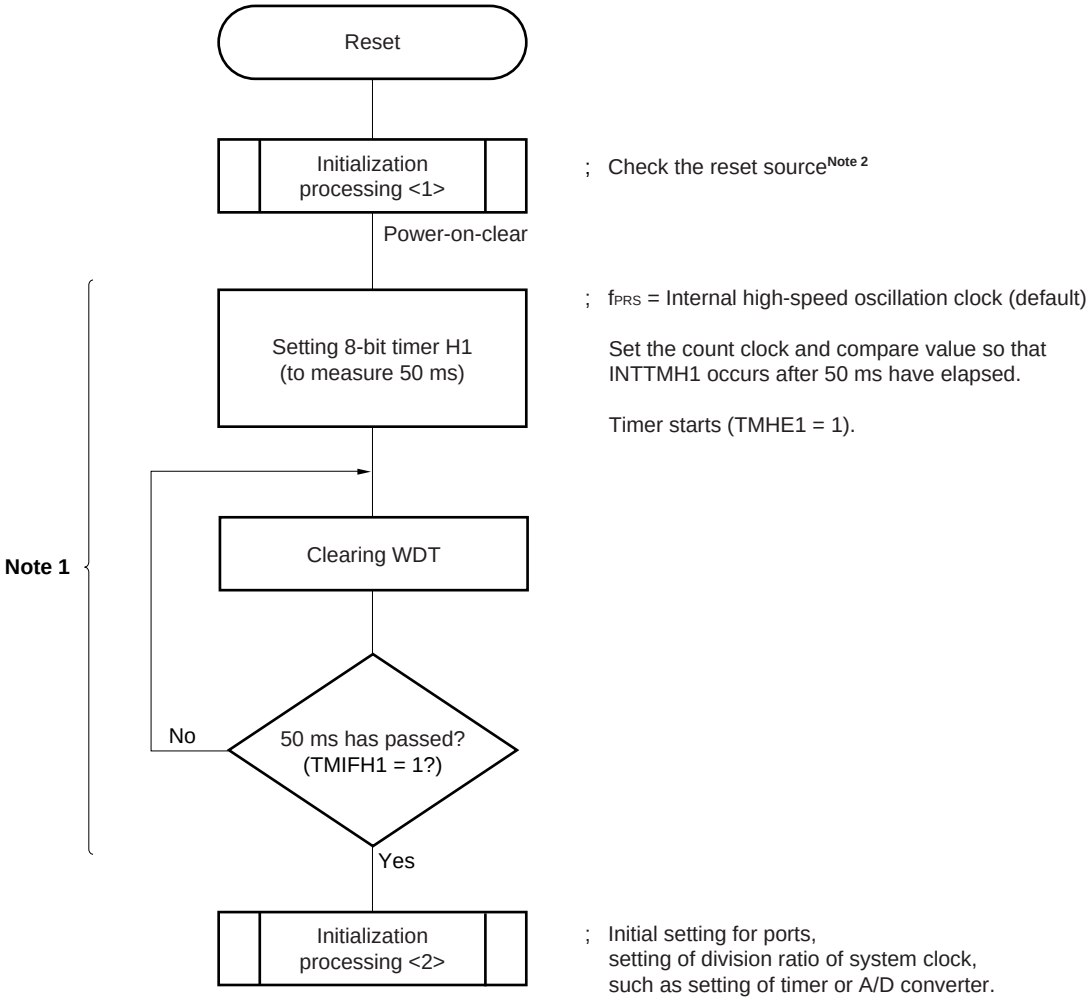
In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the detection voltage (V_{POC}), the system may be repeatedly reset and released from the reset status. In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking the following action.

<Action>

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports.

Figure 17-3. Example of Software Processing After Reset Release (1/2)

- If supply voltage fluctuation is 50 ms or less in vicinity of detection voltage

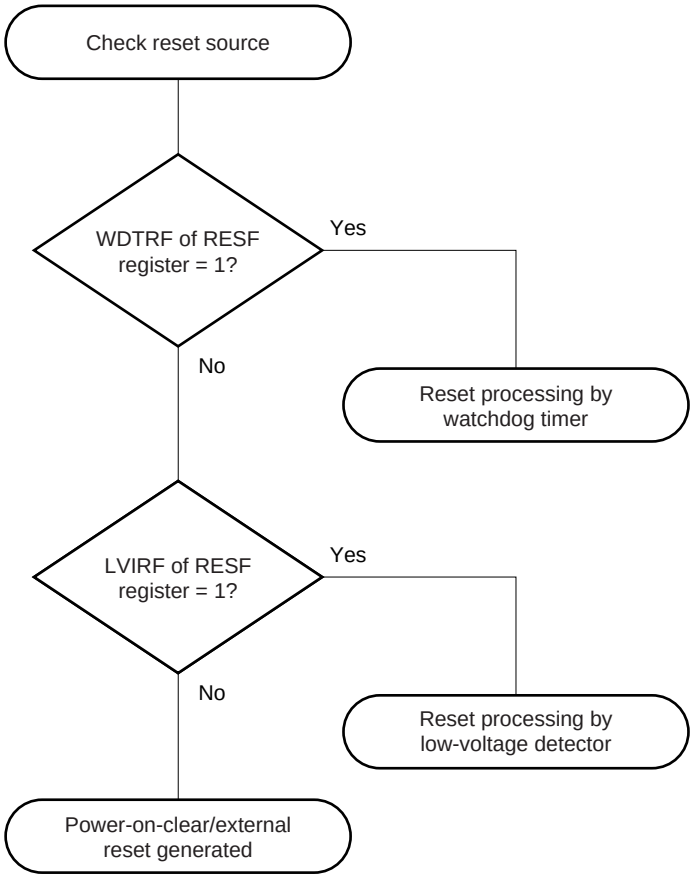


Notes 1. If reset is generated again during this period, initialization processing <2> is not started.

2. A flowchart is shown on the next page.

Figure 17-3. Example of Software Processing After Reset Release (2/2)

• Checking reset source



CHAPTER 18 LOW-VOLTAGE DETECTOR

18.1 Functions of Low-Voltage Detector

The low-voltage detector has the following functions.

- The LVI circuit compares the supply voltage (V_{DD}) with the LVI detection voltage (V_{LVI}) and generates an internal reset or internal interrupt signal.
- The low-voltage detector (LVI) can be set to ON by an option byte by default. If it is set to ON to raise the power supply from the detection voltage (V_{POC} = 1.59 V (TYP.)) or lower, the internal reset signal is generated when the supply voltage (V_{DD}) < the LVI detection voltage (V_{LVI} = 2.7 V ±0.1 V). After that, the internal reset signal is generated when the supply voltage (V_{DD}) < the LVI detection voltage (V_{LVI} = 2.7 V ±0.1 V).
- A reset or an interrupt can be selected to be generated after detection by software.
- Detection levels (V_{LVI},11 levels) of supply voltage can be changed by software.
- Operable in STOP mode.

The reset and interrupt signals are generated as follows depending on selection by software.

Selects reset (LVIMD = 1).	Selects interrupt (LVIMD = 0).
Generates an internal reset signal when $V_{DD} < V_{LVI}$ and releases the reset signal when $V_{DD} \geq V_{LVI}$.	Generates an internal interrupt signal when V_{DD} drops lower than V_{LVI} ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$).

Remark LVISEL: Bit 2 of low-voltage detection register (LVIM)
LVIMD: Bit 1 of LVIM

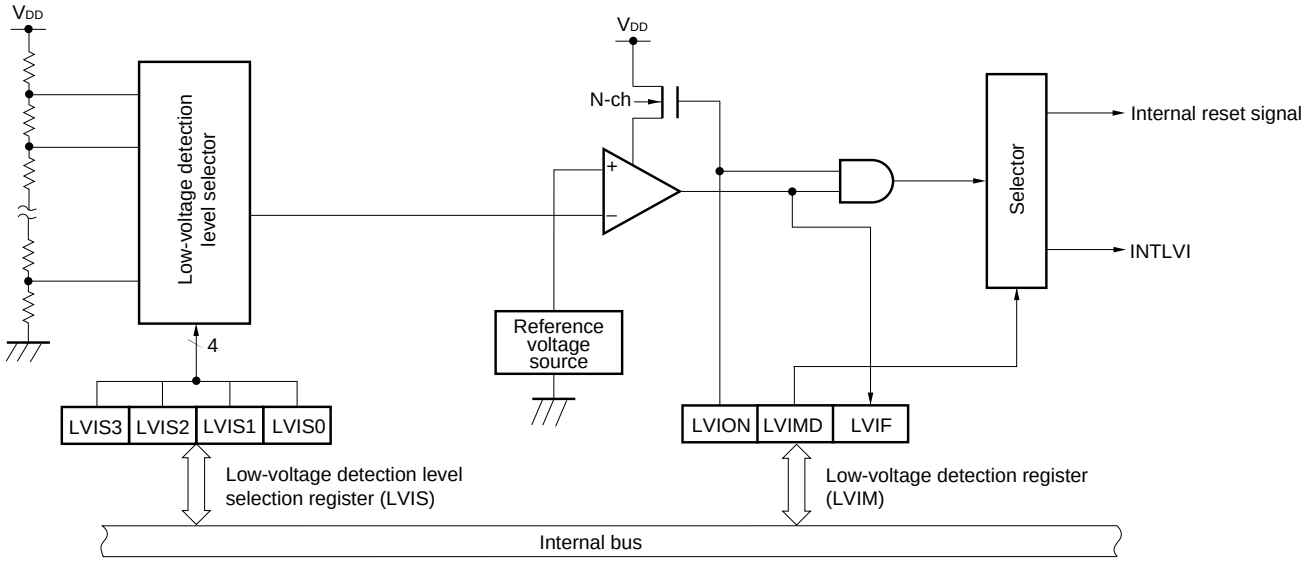
While the low-voltage detector is operating, whether the supply voltage or the input voltage from an external input pin is more than or less than the detection level can be checked by reading the low-voltage detection flag (LVIF: bit 0 of LVIM).

When the low-voltage detector is used to reset, bit 0 (LVIRF) of the reset control flag register (RESF) is set to 1 if reset occurs. For details of RESF, refer to **CHAPTER 16 RESET FUNCTION**.

18.2 Configuration of Low-Voltage Detector

The block diagram of the low-voltage detector is shown in Figure 18-1.

Figure 18-1. Block Diagram of Low-Voltage Detector



18.3 Registers Controlling Low-Voltage Detector

The low-voltage detector is controlled by the following registers.

- Low-voltage detection register (LVIM)
- Low-voltage detection level select register (LVIS)

(1) Low-voltage detection register (LVIM)

This register sets low-voltage detection and the operation mode.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

The generation of a reset signal other than an LVI reset clears this register to 00H.

Figure 18-2. Format of Low-Voltage Detection Register (LVIM)

Address: FFBEH After reset: 00H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	2	<1>	<0>
LVIM	LVION	0	0	0	0	0	LVIMD	LVIF

LVION[Notes 3, 4]	Enables low-voltage detection operation
0	Disables operation
1	Enables operation

LVIMD[Note 3]	Low-voltage detection operation mode (interrupt/reset) selection
0	Generates an internal interrupt signal when the supply voltage (V_{DD}) drops lower than the LVI detection voltage (V_{LVI}) ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$).
1	Generates an internal reset signal when the supply voltage (V_{DD}) < the LVI detection voltage (V_{LVI}) and releases the reset signal when $V_{DD} \geq V_{LVI}$.

LVIF	Low-voltage detection flag
0	Supply voltage (V_{DD}) ≥ LVI detection voltage (V_{LVI}), or when LVI operation is disabled
1	Supply voltage (V_{DD}) < LVI detection voltage (V_{LVI})

Notes 1. The reset value changes depending on the reset source and the setting of the option byte.
This register is not cleared (00H) by LVI resets (except resets by the LVI default start function).
The value of this register is reset to “00H” by other resets.

2. Bit 0 is read-only.

3. LVION and LVIMD are cleared to 0 in the case of a reset other than an LVI reset. These are not cleared to 0 in the case of an LVI reset.

4. When LVION is set to 1, operation of the comparator in the LVI circuit is started. Use software to wait for an operation stabilization time (10 µs (MAX.)) from when LVION is set to 1 until operation is stabilized. After the operation stabilizes, an external input (minimum pulse width: 200 µs) of 200 µs or more is required until LVIF is set (1) after the voltage drops to the LVI detection voltage or less.

Cautions 1. To stop LVI, follow either of the procedures below.
- **When using 8-bit memory manipulation instruction: Write 00H to LVIM.**
- **When using 1-bit memory manipulation instruction: Clear LVION to 0.**

2. If LVI operation is disabled (clears LVION) when LVI is used in interrupt mode (LVIMD = 0) and the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}), an interrupt request signal (INTLVI) is generated and LVIIF may be set to 1.

(2) Low-voltage detection level select register (LVIS)

This register selects the low-voltage detection level.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation input sets this register to 00H.

Figure 18-3. Format of Low-Voltage Detection Level Select Register (LVIS)

Address: FFBFH After reset: 00H[Note] R/W

Symbol	7	6	5	4	3	2	1	0
LVIS	0	0	0	0	LVIS3	LVIS2	LVIS1	LVIS0

LVIS3	LVIS2	LVIS1	LVIS0	Detection level
0	0	0	0	V_{LVI0} (4.24 ±0.1 V)
0	0	0	1	V_{LVI1} (4.09 ±0.1 V)
0	0	1	0	V_{LVI2} (3.93 ±0.1 V)
0	0	1	1	V_{LVI3} (3.78 ±0.1 V)
0	1	0	0	V_{LVI4} (3.62 ±0.1 V)
0	1	0	1	V_{LVI5} (3.47 ±0.1 V)
0	1	1	0	V_{LVI6} (3.32 ±0.1 V)
0	1	1	1	V_{LVI7} (3.16 ±0.1 V)
1	0	0	0	V_{LVI8} (3.01 ±0.1 V)
1	0	0	1	V_{LVI9} (2.85 ±0.1 V)
1	0	1	0	V_{LVI10} (2.70 ±0.1 V)

Note The reset value changes depending on the reset source.
If the LVIS register is reset by LVI resets (except resets by the LVI default start function), it is not reset but holds the current value. The value of this register is reset to “00H” by other resets.

Cautions 1. Be sure to clear bits 4 to 7 to 0.

2. Do not change the value of LVIS during LVI operation.

18.4 Operation of Low-Voltage Detector

The low-voltage detector can be used in the following two modes.

(1) Used as reset (LVIMD = 1)

- Compares the supply voltage (V_{DD}) and LVI detection voltage (V_{LVI}), generates an internal reset signal when $V_{DD} < V_{LVI}$, and releases internal reset when $V_{DD} \geq V_{LVI}$.

Remark The low-voltage detector (LVI) can be set to ON by an option byte by default. If it is set to ON to raise the power supply from the detection voltage (V_{POC} = 1.59 V (TYP.)) or lower, the internal reset signal is generated when the supply voltage (V_{DD}) < detection voltage (V_{LVI} = 2.70 V ±0.1 V).

(2) Used as interrupt (LVIMD = 0)

- Compares the supply voltage (V_{DD}) and LVI detection voltage (V_{LVI}). When V_{DD} drops lower than V_{LVI} ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$), generates an interrupt signal (INTLVI).

While the low-voltage detector is operating, whether the supply voltage is more than or less than the detection level can be checked by reading the low-voltage detection flag (LVIF: bit 0 of LVIM).

Remark LVIMD: Bit 1 of low-voltage detection register (LVIM)

18.4.1 When used as reset

(1) In 1.59 V POC mode (LVISTART = 0)

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Set the LVI detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level selection register (LVIS).
  - <3> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
  - <4> Use software to wait for an operation stabilization time (10 μs (MAX.)).
  - <5> Wait until it is checked that (supply voltage (V_{DD}) ≥ LVI detection voltage (V_{LVI})) by bit 0 (LVIF) of LVIM.
  - <6> Set bit 1 (LVIMD) of LVIM to 1 (generates reset when the level is detected).

  Figure 18-4 shows the timing of the internal reset signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <6> above.

  Cautions 1. Be sure to execute <1>. When LVIMK = 0, an interrupt may occur immediately after the processing in <3>.
  2. If supply voltage (V_{DD}) ≥ LVI detection voltage (V_{LVI}) when LVIMD is set to 1, an internal reset signal is not generated.

- When stopping operation

  Either of the following procedures must be executed.

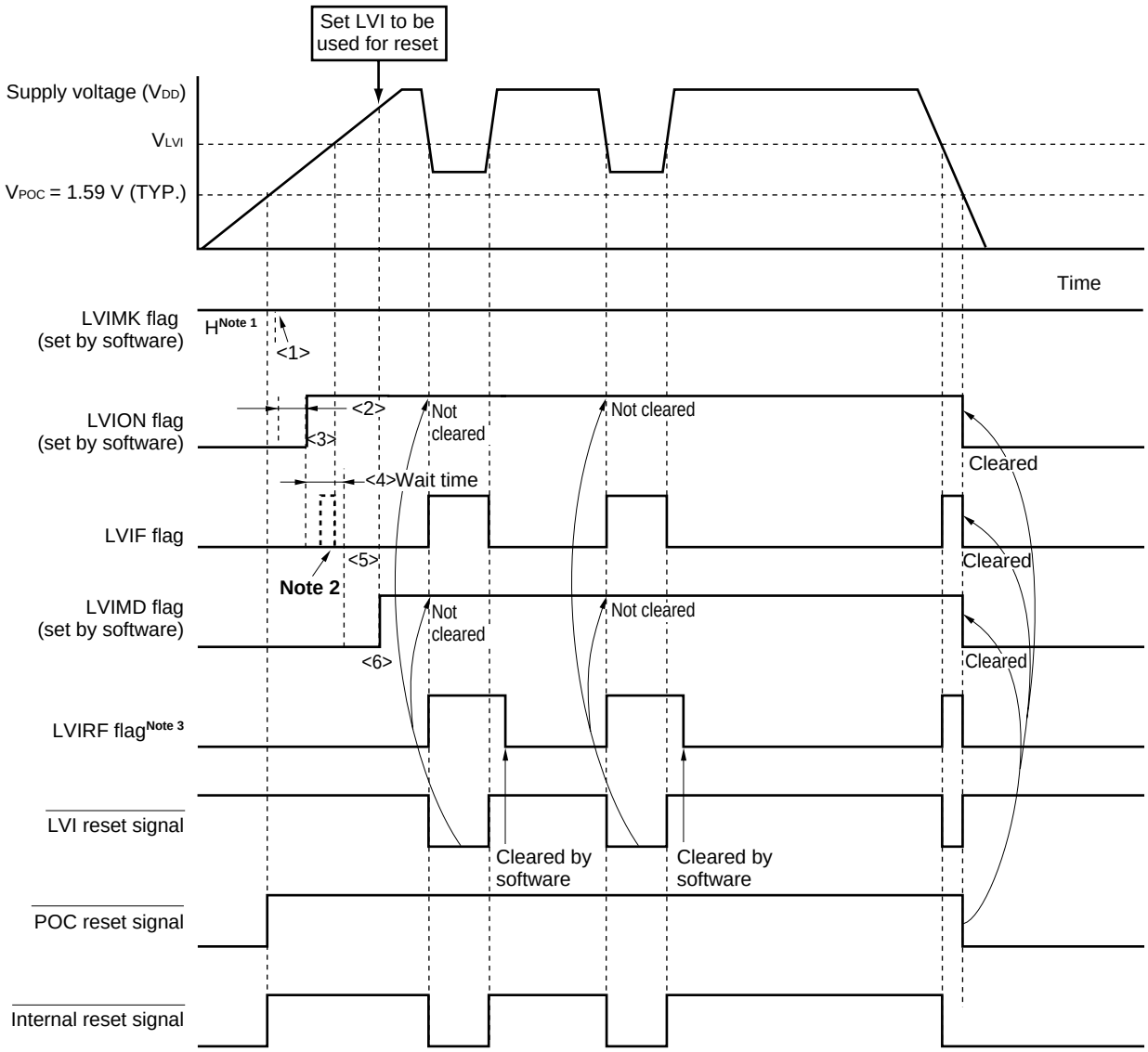
  • When using 8-bit memory manipulation instruction:

  Write 00H to LVIM.

  • When using 1-bit memory manipulation instruction:

  Clear LVIMD to 0 and then LVION to 0.

Figure 18-4. Timing of Low-Voltage Detector Internal Reset Signal Generation (LVISTART = 0)



Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. The LVIIF flag of the interrupt request flag registers and the LVIF flag may be set (1).

3. LVIRF is bit 0 of the reset control flag register (RESF). For details of RESF, refer to **CHAPTER 16 RESET FUNCTION**.

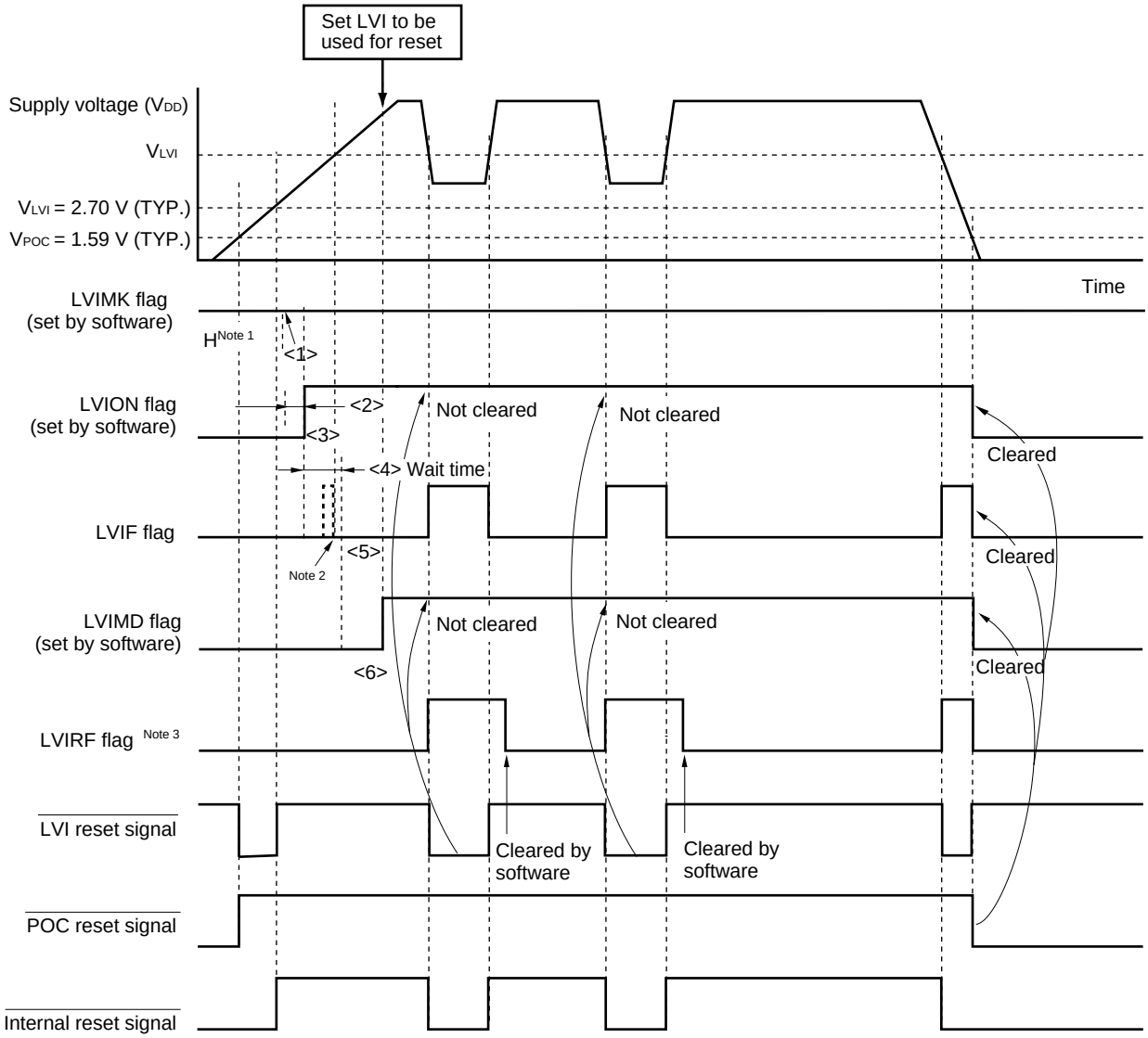
Remarks 1. <1> to <6> in Figure 18-4 above correspond to <1> to <6> in the description of “When starting operation” in **18.4.1 (1) When LVI default start function stopped is set (LVISTART = 0).**

2. VPOC: Detection voltage

(2) In 2.7 V/1.59 V POC mode (LVISTART = 1)

The setting when operation starts and when operation stops is the same as that described in **18.4.1 (1) When LVI default start function stopped is set (LVISTART = 0)**.

Figure 18-5. Timing of Low-Voltage Detector Internal Reset Signal Generation (LVISTART = 1)



Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. The LVIIF flag of the interrupt request flag registers and the LVIF flag may be set (1).

3. LVIRF is bit 0 of the reset control flag register (RESF).
For details of RESF, refer to **CHAPTER 16 RESET FUNCTION**.

Remarks 1. <1> to <6> in Figure 18-5 above correspond to <1> to <6> in the description of “When starting operation” in **18.4.1 (1) When LVI default start function stopped is set (LVISTART = 0)**.

2. VPOC: Detection voltage

18.4.2 When used as interrupt

(1) When LVI default start function stopped is set (LVISTART = 0)

- When starting operation
  - <1> Mask the LVI interrupt (LVIMK = 1).
  - <2> Set the LVI detection voltage using bits 3 to 0 (LVIS3 to LVIS0) of the low-voltage detection level selection register (LVIS).
  - <3> Clear bit 1 (LVIMD) of LVIM to 0 (generates interrupt signal when the level is detected) (default value).
  - <4> Set bit 7 (LVION) of LVIM to 1 (enables LVI operation).
  - <5> Use software to wait for an operation stabilization time (10 μs (MAX.)).
  - <6> Confirm that "supply voltage (V_{DD}) ≥ LVI detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < LVI detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, at bit 0 (LVIF) of LVIM.
  - <7> Clear the interrupt request flag of LVI (LVIIF) to 0.
  - <8> Release the interrupt mask flag of LVI (LVIMK).
  - <9> Execute the EI instruction (when vector interrupts are used).

Figure 18-6 shows the timing of the interrupt signal generated by the low-voltage detector. The numbers in this timing chart correspond to <1> to <8> above.

- When stopping operation

Either of the following procedures must be executed.

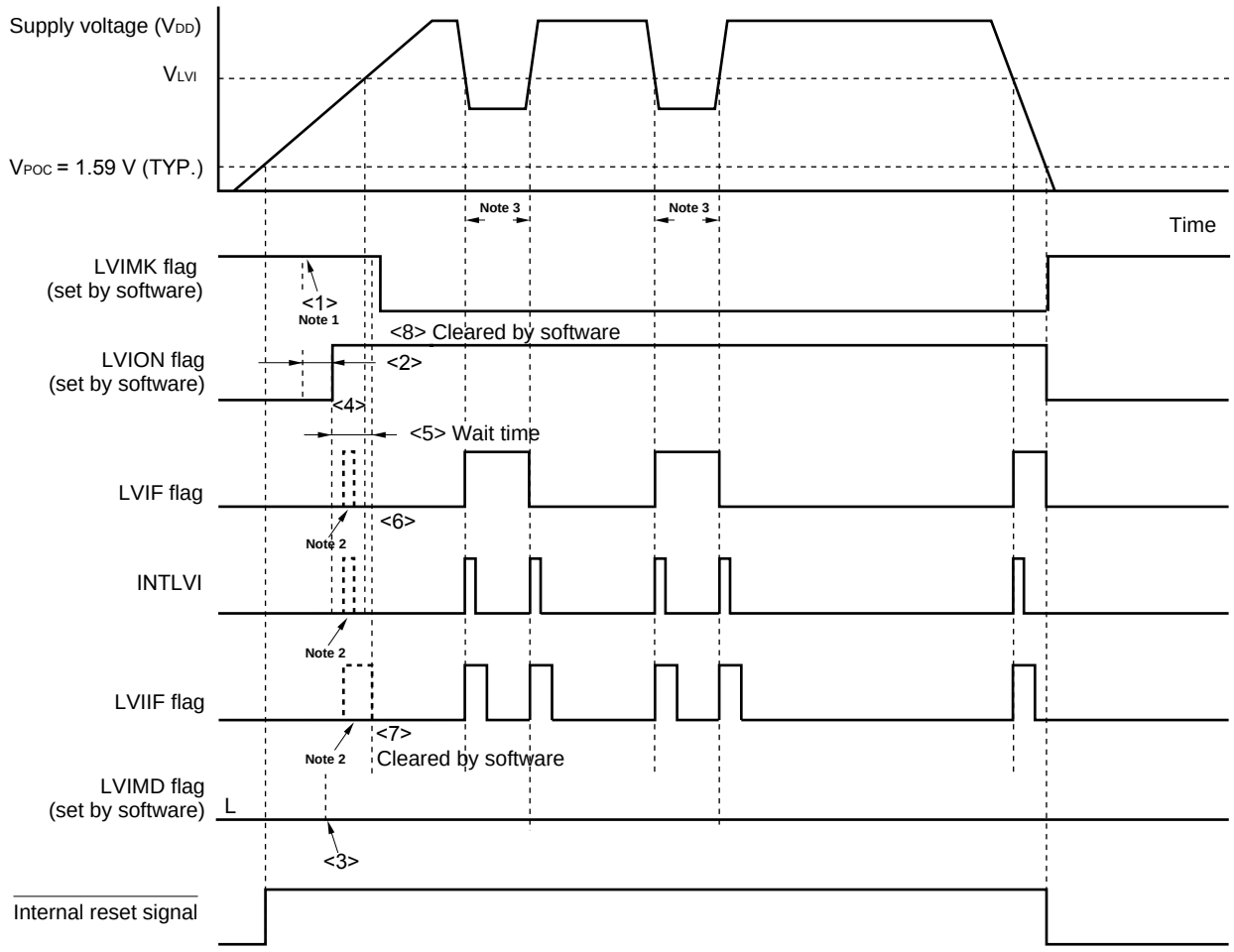
- When using 8-bit memory manipulation instruction:

Write 00H to LVIM.

- When using 1-bit memory manipulation instruction:

Clear LVION to 0.

Figure 18-6. Timing of Low-Voltage Detector Interrupt Signal Generation (LVISTART = 0)



Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVI operation is disabled (clears LVION) when the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}), an interrupt request signal (INTLVI) is generated and LVIIF may be set to 1.

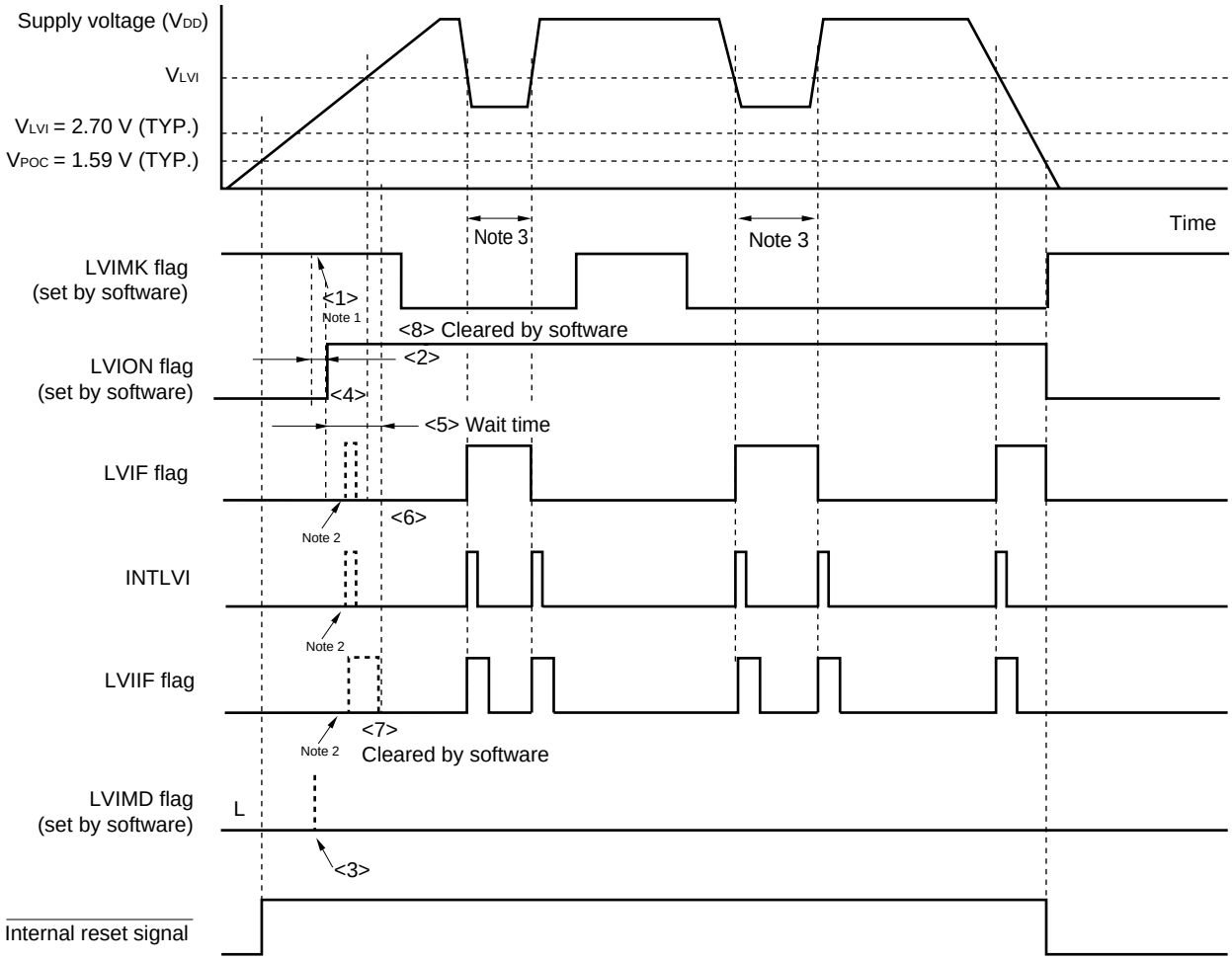
Remarks 1. <1> to <8> in Figure 18-6 above correspond to <1> to <8> in the description of “When starting operation” in **18.4.2 (1) When LVI default start function stopped is set (LVISTART = 0).**

2. V_{POC}: Detection voltage

(2) When LVI default start function enabled is set (LVISTART = 1)

The setting when operation starts and when operation stops is the same as that described in **18.4.2 (1) When LVI default start function stopped is set (LVISTART = 0)**.

Figure 18-7. Timing of Low-Voltage Detector Interrupt Signal Generation (LVISTART = 1)



Notes 1. The LVIMK flag is set to “1” by reset signal generation.

2. The LVIIF flag of the interrupt request flag registers and the LVIF flag may be set (1).

3. If LVI operation is disabled (clears LVION) when the supply voltage (V_{DD}) is less than or equal to the detection voltage (V_{LVI}), an interrupt request signal (INTLVI) is generated and LVIIF may be set to 1.

Remarks 1. <1> to <8> in Figure 18-7 above correspond to <1> to <8> in the description of “When starting operation” in **18.4.2 (1) When LVI default start function enabled is set (LVISTART = 1).**

2. V_{POC}: Detection voltage

18.5 Cautions for Low-Voltage Detector

In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the LVI detection voltage (V_{LVI}), the operation is as follows depending on how the low-voltage detector is used.

Operation example 1: When used as reset

The system may be repeatedly reset and released from the reset status.

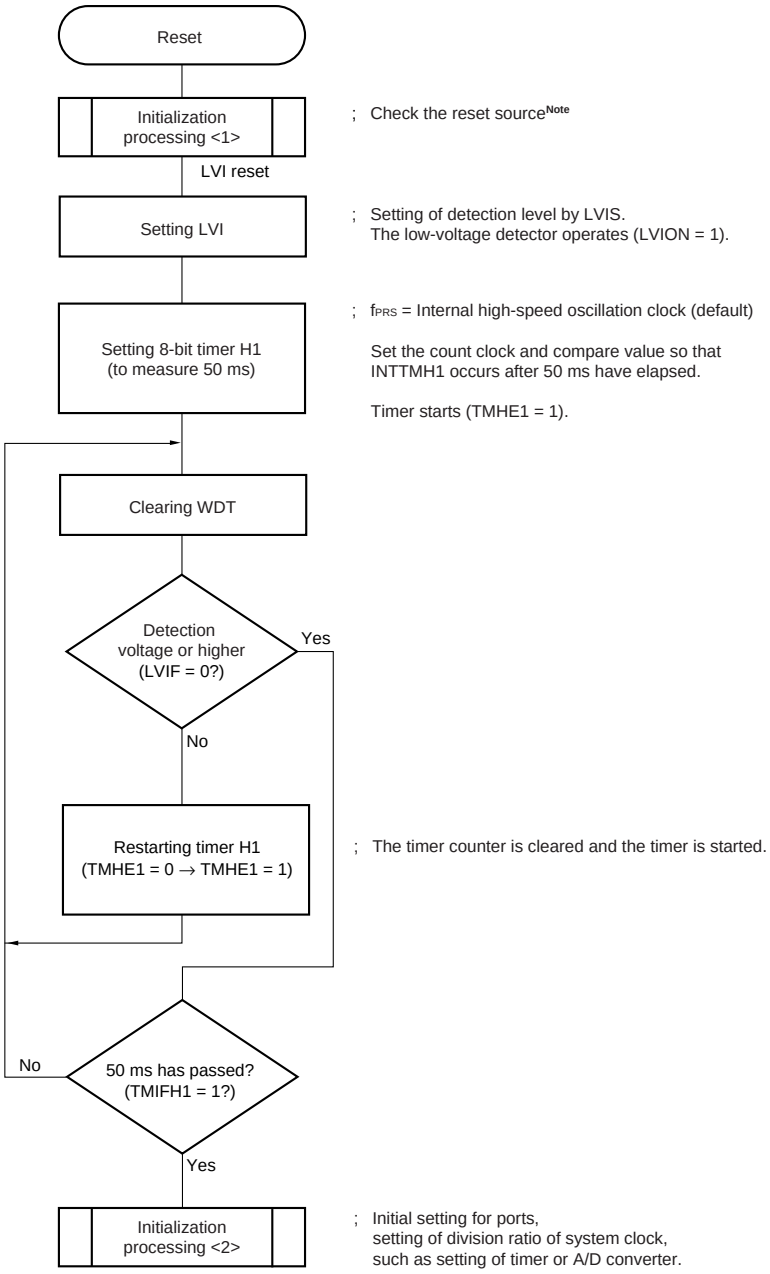
The time from reset release through microcontroller operation start can be set arbitrarily by the following action.

<Action>

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports (refer to **Figure 18-8**).

Figure 18-8. Example of Software Processing After Reset Release (1/2)

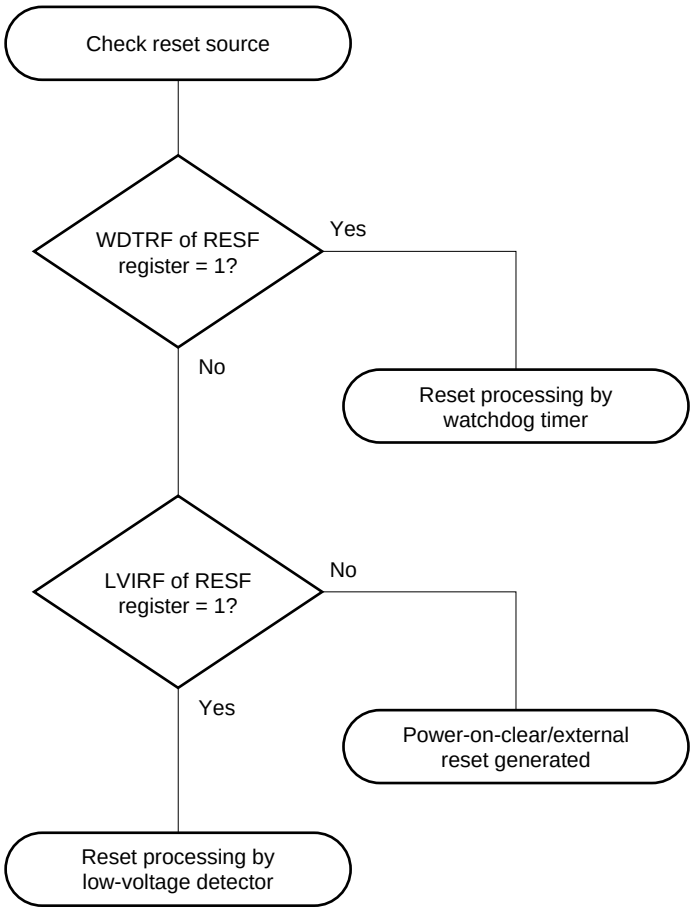
• If supply voltage fluctuation is 50 ms or less in vicinity of LVI detection voltage



Note A flowchart is shown on the next page.

Figure 18-8. Example of Software Processing After Reset Release (2/2)

• Checking reset source



Operation example 2: When used as interrupt

Interrupt requests may be generated frequently.

Take the following action.

<Action>

Confirm that "supply voltage (V_{DD}) ≥ LVI detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < LVI detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, in the servicing routine of the LVI interrupt by using bit 0 (LVIF) of the low-voltage detection register (LVIM). Clear bit 1 (LVIIF) of interrupt request flag register 0L (IF0L) to 0.

For a system with a long supply voltage fluctuation period near the LVI detection voltage, take the above action after waiting for the supply voltage fluctuation time.

CHAPTER 19 REGULATOR

19.1 Regulator Overview

The µPD79F7023, 79F7024 microcontrollers contain a circuit for operating the device with a constant voltage. At this time, in order to stabilize the regulator output voltage, connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 µF: target). However, when using the STOP mode that has been entered since operation of the internal high-speed oscillation clock and external main system clock, 0.47 µF is recommended. Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

The regulator output voltage is normally 2.5 V (TYP.), and in the low power consumption mode, 1.9 V (TYP.).

19.2 Register Controlling Regulator

(1) Regulator mode control register (RMC)

This register sets the output voltage of the regulator.

RMC is set with an 8-bit memory manipulation instruction.

Reset input sets this register to 00H.

Figure 19-1. Format of Regulator Mode Control Register (RMC)

Address: FF3DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
RMC								

RMC[7:0]	Control of output voltage of regulator
59H	Low power consumption mode (fixed to 1.9 V) When CPU clock (f_{CPU}) ≤ 4 MHz, can be set.
56H	Low power consumption mode (fixed to 1.9 V) When the internal high-speed oscillation clock is selected as the CPU clock, f_{CPU} ≤ 1 MHz, or high-speed system clock is stopped, can be set to 56H.
00H	Normal power mode (fixed to 2.5 V)
Other than above	Setting prohibited

Cautions 1. To change the RMC register setting value from 56H/59H to 00H and use a CPU operating frequency of 4 MHz or more, change the PCC and RCM registers when 22 µs or more has elapsed after the RMC register was set.

2. When using the setting fixed to the low power consumption mode, the RMC register can be used in the following cases.

<When the high-speed internal oscillation clock is selected for the CPU clock, and high-speed system clock is stopped> f_{CPU} ≤ 1 MHz

19.3 Cautions for Self Programming

1. Make sure that the regulator output voltage mode is fixed when executing self programming.
2. The power supply voltage range in which the flash memory can be rewritten in normal power mode is $V_{DD} \geq 2.5$ V. Note that program area can be rewritten by using the self programming library in normal power mode.
3. Rewriting the flash memory is prohibited in low power consumption mode.

Remark For details of the self-programming function and the self programming library, refer to **"78K0 Microcontrollers User's Manual Self Programming Library Type 01 (U18274E)"** and **"78K0 Microcontrollers Self Programming Library Type 01 Ver. 3.10 Operating Precautions (notification document) (ZUD-CD-09-0122)"**.

CHAPTER 20 OPTION BYTE

20.1 Functions of Option Bytes

The flash memory at 0080H, 0081H, and 0084H of the µPD79F7023, 79F7024 is an option byte area. When power is turned on or when the device is restarted from the reset status, the device automatically references the option bytes and sets specified functions. When using the product, be sure to set the following functions by using the option bytes.

When the boot swap operation is used during self-programming, 0080H, 0081H, and 0084H are switched to 1080H, 1081H, and 1084H. Therefore, set values that are the same as those of 0080H, 0081H, and 0084H to 1080H, 1081H, and 1084H in advance.

(1) 0080H/1080H

- Internal low-speed oscillator operation
  - Can be stopped by software
  - Cannot be stopped
- Watchdog timer interval time setting
- Watchdog timer counter operation
  - Enabled counter operation
  - Disabled counter operation
- Watchdog timer window open period setting

Caution Set a value that is the same as that of 0080H to 1080H because 0080H and 1080H are switched during the boot swap operation.

(2) 0081H/1081H

- LVI default start operation control
  - During LVI default start function enabled (LVISTART = 1)
    The device is in the reset state after reset release or upon power application and until the supply voltage reaches 2.7 V (TYP.). It is released from the reset state when the voltage exceeds 2.7 V (TYP.).
    If the supply voltage rises to 2.7 V after reset release or power application at a rate slower than 0.5 V/ms (MIN.), LVI default start function operation is recommended.
  - During LVI default start function stopped (LVISTART = 0)
    The device is in the reset state after reset release or upon power application and until the supply voltage reaches 1.59 V (TYP.). It is released from the reset state when the voltage exceeds 1.59 V (TYP.).

Caution LVISTART can only be written by using a dedicated flash memory programmer. It cannot be set or change during self-programming or boot swap operation during self-programming. However, because 0080H and 1080H are switched during the boot swap operation, set a value that is the same as that of 0080H to 1080H.

(3) 0082H/1082H

Be sure to set to 01H.

Caution Set a 01H to 1082H because 0082H and 1082H are switched during the boot swap operation.

(4) 0083H/1083H

○ On-chip debug mode

- Disabling on-chip debug mode
- Forcibly setting to on-chip debug mode

○ Clock supply to UART0 when STOP instruction is executed

- Supply
- Stop

Caution Set a value that is the same as that of 0083H to 1083H because 0083H and 1083H are switched during the boot swap operation.

(5) 0084H/1084H

○ On-chip debug operation control

- Disabling on-chip debug operation
- Enabling on-chip debug operation and erasing data of the flash memory in case authentication of the on-chip debug security ID fails
- Enabling on-chip debug operation and not erasing data of the flash memory even in case authentication of the on-chip debug security ID fails

Caution Set a value that is the same as that of 0084H to 1084H because 0084H and 1084H are switched during the boot swap operation.

20.2 Format of Option Byte

The format of the option byte is shown below.

Figure 20-1. Format of Option Byte (1/3)

Address: 0080H/1080H[Note]

7	6	5	4	3	2	1	0
0	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	LSROSC

WINDOW1	WINDOW0	Watchdog timer window open period
0	0	25%
0	1	50%
1	0	75%
1	1	100%

WDTON	Operation control of watchdog timer counter/illegal access detection
0	Counter operation disabled (counting stopped after reset), illegal access detection operation disabled
1	Counter operation enabled (counting started after reset), illegal access detection operation enabled

WDCS2	WDCS1	WDCS0	Watchdog timer overflow time
0	0	0	$2^{10}/f_{IL}$ (4.27 ms)
0	0	1	$2^{11}/f_{IL}$ (8.53 ms)
0	1	0	$2^{12}/f_{IL}$ (17.07 ms)
0	1	1	$2^{13}/f_{IL}$ (34.13 ms)
1	0	0	$2^{14}/f_{IL}$ (68.27 ms)
1	0	1	$2^{15}/f_{IL}$ (136.53 ms)
1	1	0	$2^{16}/f_{IL}$ (273.07 ms)
1	1	1	$2^{17}/f_{IL}$ (546.13 ms)

LSROSC	Internal low-speed oscillator operation
0	Can be stopped by software (stopped when 1 is written to bit 1 (LSRSTOP) of RCM register)
1	Cannot be stopped (not stopped even if 1 is written to LSRSTOP bit)

Note Set a value that is the same as that of 0080H to 1080H because 0080H and 1080H are switched during the boot swap operation.

Cautions 1. The combination of WDCS2 = WDCS1 = WDCS0 = 0 and WINDOW1 = WINDOW0 = 0 is prohibited.

2. The watchdog timer continues its operation during self-programming of the flash memory. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

3. If LSROSC = 0 (oscillation can be stopped by software), the count clock is not supplied to the watchdog timer in the HALT and STOP modes, regardless of the setting of bit 0 (LSRSTOP) of the internal oscillation mode register (RCM).

When 8-bit timer H1 operates with the internal low-speed oscillation clock, the count clock is supplied to 8-bit timer H1 even in the HALT/STOP mode.

4. Be sure to clear bit 7 to 0.

Remarks 1. f_{IL}: Internal low-speed oscillation clock frequency

2. ( ): f_{IL} = 240 kHz (TYP.)

Figure 20-1. Format of Option Byte (2/3)

Address: 0081H/1081H[Notes 1, 2]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	LVISTART

LVISTART	LVI default start operation control
0	LVI is OFF by default upon power application (LVI default start function stopped)
1	LVI is ON by default upon power application (LVI default start function enabled)

Notes 1. LVISTART can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming. However, because 0080H and 1080H are switched during the boot swap operation, set a value that is the same as that of 0080H to 1080H.

2. To change the setting for the LVI default start, set the value to 0081H again after batch erasure (chip erasure) of the flash memory. The setting cannot be changed after the memory of the specified block is erased.

Caution Be sure to clear bits 7 to 1 to "0".

Address: 0082H/1082H[Note]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1

Note Set a 01H to 1082H because 0082H and 1082H are switched during the boot swap operation.

Caution Be sure to set to "01H".

Address: 0083H/1083H[Note]

7	6	5	4	3	2	1	0
0	0	0	OCDCKSTP	1	1	1	OCDONB

OCDCKSTP	Clock supply to UART0 when STOP instruction is executed in on-chip debug mode
0	If STOP instruction is executed, internal oscillator is not stopped, and clock supply to UART0 is continued. CPU and peripheral circuits are stopped.
1	Internal oscillator is stopped and clock supply to UART0 is stopped.

OCDONB	On-chip debug mode
0	Disables on-chip debug mode
1	Forcibly sets to on-chip debug mode

Note Set a value that is the same as that of 0083H to 1083H because 0083H and 1083H are switched during the boot swap operation.

Caution Be sure to clear bits 7 to 5 and 0 to "0" and set bits 4 to 2 to "1".

Figure 20-1. Format of Option Byte (3/3)

Address: 0084H/1084H[Note]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	OCDEN1	OCDEN0

OCDEN1	OCDEN0	On-chip debug operation control
0	0	Operation disabled
0	1	Setting prohibited
1	0	Operation enabled. Does not erase data of the flash memory in case authentication of the on-chip debug security ID fails.
1	1	Operation enabled. Erases data of the flash memory in case authentication of the on-chip debug security ID fails.

Note Set a value that is the same as that of 0084H to 1084H because 0084H and 1084H are switched during the boot swap operation.

Caution Be sure to clear bits 7 to 2 to "0".

Remark For the on-chip debug security ID, refer to **CHAPTER 22 ON-CHIP DEBUG FUNCTION**.

Here is an example of description of the software for setting the option bytes.

```
OPT      CSEG   AT 0080H
OPTION:  DB     30H      ; Enables watchdog timer operation (illegal access detection operation),
                         ; Window open period of watchdog timer: 50%,
                         ; Overflow time of watchdog timer: 2^10/fIL,
                         ; Internal low-speed oscillator can be stopped by software.
         DB     00H      ; LVI default start function stopped
         DB     01H      ; Internal high-speed oscillation clock frequency 4 MHz (TYP.)
         DB     1EH      ; Use the TOOLC0/X1, TOOLD0/X2 pins
         DB     02H      ; Operation enabled.  Does not erase data of the flash memory in case
                         ; authentication of the on-chip debug security ID fails.
```

Remark Referencing of the option byte is performed during reset processing. For the reset processing timing, refer to **CHAPTER 16 RESET FUNCTION**.

CHAPTER 21 FLASH MEMORY

The μPD79F7023, 79F7024 incorporates the flash memory to which a program can be written, erased, and overwritten while mounted on the board.

21.1 Internal Memory Size Switching Register

Select the internal memory capacity using the internal memory size switching register (IMS).
IMS is set by an 8-bit memory manipulation instruction.
Reset signal generation sets IMS to CFH.

Caution Reset signal generation makes the setting of the ROM area undefined. Therefore, set the value corresponding to each product as indicated Table 21-1 after release of reset.

Figure 21-1. Format of Internal Memory Size Switching Register (IMS)

Address: FFF0H After reset: CFH R/W

Symbol	7	6	5	4	3	2	1	0
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0

RAM2	RAM1	RAM0	Internal high-speed RAM capacity selection
0	0	0	768 bytes
0	1	0	512 bytes
1	1	0	(Default value)
Other than above			Setting prohibited

ROM3	ROM2	ROM1	ROM0	Internal ROM capacity selection
0	0	1	0	8 KB
0	1	0	0	16 KB
1	1	1	1	(Default value)
Other than above				Setting prohibited

Table 21-1. Set Values of Internal Memory Size Switching Register

Products	IMS Setting
μPD79F7023	42H
μPD79F7024	04H

21.2 Writing with Flash Memory Programmer

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the μPD79F7023, 79F7024 have been mounted on the target system. The connectors that connect the dedicated flash memory programmer must be mounted on the target system.

(2) Off-board programming

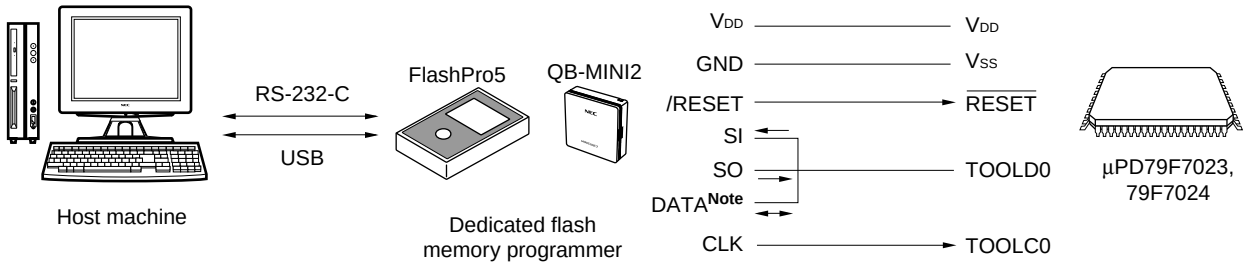
Data can be written to the flash memory with a dedicated program adapter (FA series) before the μPD79F7023, 79F7024 are mounted on the target system.

Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

21.3 Programming Environment

The environment required for writing a program to the flash memory of the µPD79F7023, 79F7024 are illustrated below.

Figure 21-2. Environment for Writing Program to Flash Memory



Note QB-MINI2 only

A host machine that controls the dedicated flash memory programmer is necessary.

To interface between the dedicated flash memory programmer and the µPD79F7023, 79F7024, the TOOLD0 pins is used for manipulation such as writing and erasing via a dedicated single-line UART. To write the flash memory off-board, a dedicated program adapter (FA series) is necessary.

Table 21-2. Pin Connection

Dedicated Flash memory programmer			µPD79F7023, 79F7024 microcontrollers
Signal Name	I/O	Pin Function	Pin Name
CLK	Output	Clock output to µPD79F7023, 79F7024 microcontrollers	TOOLC0/
SI	Input	Receive signal	TOOLD0
SO	Output	Transmit signal	
DATA[Note]	I/O	Input/output signal for data communication during debugging	
/RESET	Output	Reset signal	$\overline{\text{RESET}}$
V_{DD}	I/O	V_{DD} voltage generation/power monitoring	V_{DD}
GND	–	Ground	V_{SS}

Note QB-MINI2 only

21.4 Connection of Pins on Board

To write the flash memory on-board, connectors that connect the dedicated flash memory programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be handled as described below.

21.4.1 TOOL pins

The pins used for communication in flash memory programming mode are shown in the table below.

Table 21-3. Pins Used for Communication in Flash Memory Programming Mode

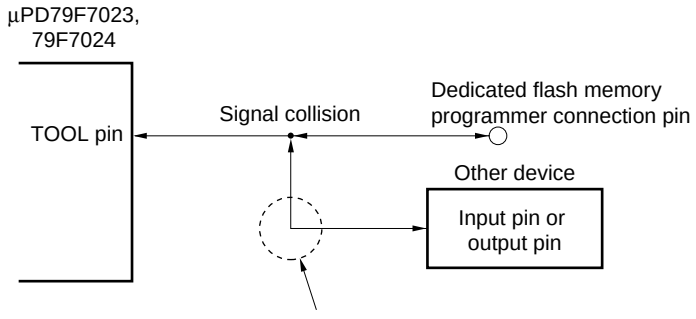
Pin Name	Connection of Pins
TOOLC0	Connect this pin directly to the dedicated flash memory programmer or pull it down by connecting it to V_{SS} via a resistor (10 kΩ)
TOOLD0	Connect this pin directly to the dedicated flash memory programmer or pull it up by connecting it to V_{DD} via a resistor (3 k to 10 kΩ)

To connect the dedicated flash memory programmer to the pins of a serial interface that is connected to another device on the board, care must be exercised so that signals do not collide or that the other device does not malfunction.

(1) Signal collision

If the dedicated flash memory programmer is connected to the TOOL pin that is connected to another device, signal collision takes place. To avoid this collision, either isolate the connection with the other device, or make the other device go into a high-impedance state.

Figure 21-3. Signal Collision (TOOL Pin)



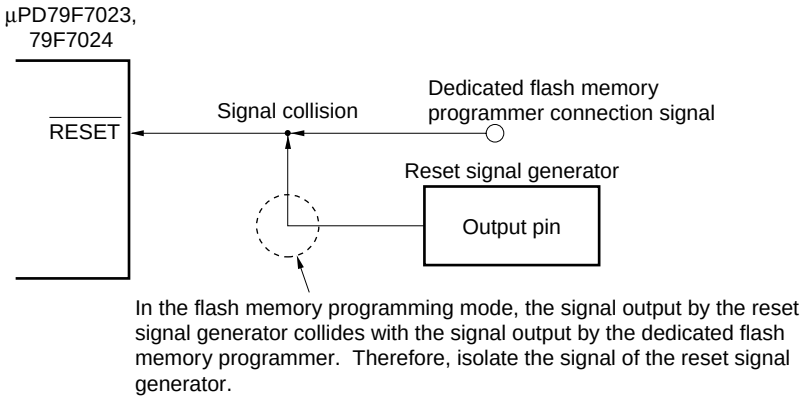
In the flash memory programming mode, the signal of the other device collides with the signal of the dedicated flash programmer. Therefore, isolate the signal of the other device.

21.4.2 $\overline{\text{RESET}}$ pin

If the reset signal of the dedicated flash memory programmer is connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board, signal collision takes place. To prevent this collision, isolate the connection with the reset signal generator.

If the reset signal is input from the user system while the flash memory programming mode is set, the flash memory will not be correctly programmed. Do not input any signal other than the reset signal of the dedicated flash memory programmer.

Figure 21-4. Signal Collision ($\overline{\text{RESET}}$ Pin)



21.4.3 Port pins

When the flash memory programming mode is set, all the pins not used for flash memory programming enter the same status as that immediately after reset. If external devices connected to the ports do not recognize the port status immediately after reset, the port pin must be connected to V_{DD} or V_{SS} via a resistor.

21.4.4 REGC pin

Connect the REGC pin to GND via a capacitor (0.47 to 1 μF) in the same manner as during normal operation. However, when using the STOP mode that has been entered since operation of the internal high-speed oscillation clock and external main system clock, 0.47 μF is recommended. Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

21.4.5 Other signal pins

Connect X1, X2 in the same status as in the normal operation mode.

Remark In the flash memory programming mode, the internal high-speed oscillation clock (f_{IH}) is used.

21.4.6 Power supply

To use the supply voltage output of the flash memory programmer, connect the V_{DD} pin to V_{DD} of the flash memory programmer, and the V_{SS} pin to GND of the flash memory programmer.

To use the on-board supply voltage, connect in compliance with the normal operation mode.

However, be sure to connect the V_{DD} and V_{SS} pins to V_{DD} and GND of the flash memory programmer to use the power monitor function with the flash memory programmer, even when using the on-board supply voltage.

Supply the same other power supplies (AV_{REF}, V_{SS}) as those in the normal operation mode.

21.4.7 On-board writing when connecting crystal/ceramic resonator

To write the flash memory on-board, connectors that connect the dedicated flash memory programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be processed as described below.

The state of the pins in the self programming mode is the same as that in the HALT mode.

When using the X1 (TOOLC0) and X2 (TOOLD0) pins as the serial interface for flash memory programming, signals will collide if an external device is connected. To prevent the conflict of signals, isolate the connection with the external device.

Similarly, when a capacitor is connected to the X1 and X2 pins, the waveform during communication is changed, and thus communication may be disabled depending on the capacitor capacitance. Make sure to isolate the connection with the capacitor during flash programming.

In cases when a crystal or ceramic resonator has been selected to generate the system clock, and the decision has been made to execute on-board flash programming with the resonator mounted on the device because it is difficult to isolate the resonator, be sure to thoroughly evaluate the flash memory programming with the resonator mounted on the device before executing the processing described next.

- Mount the minimum-possible test pads between the device and the resonator, and connect the programmer via the test pad. Keep the wiring as short as possible (refer to **Figure 21-5** and **Table 21-4**).

Figure 21-5. Example of Mounting Test Pads

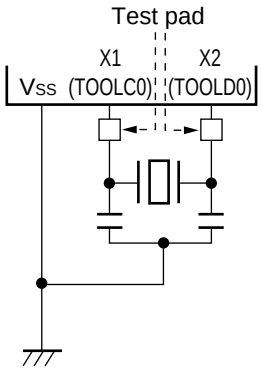


Table 21-4. Clock to Be Used and Mounting of Test Pads

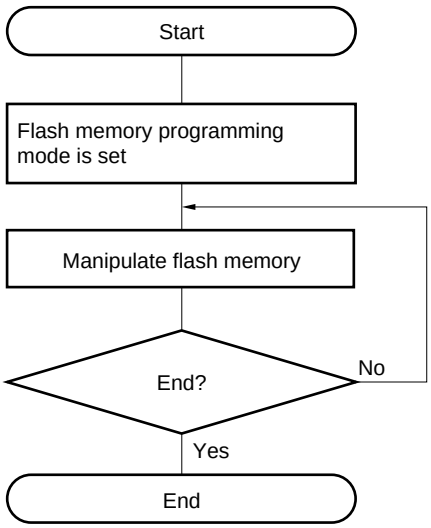
Clock to Be Used		Mounting of Test Pads
High-speed internal oscillation clock		Not required
External clock		
Crystal/ceramic oscillation clock	Before resonator is mounted	
	After resonator is mounted	Required

21.5 Programming Method

21.5.1 Controlling flash memory

The following figure illustrates the procedure to manipulate the flash memory.

Figure 21-6. Flash Memory Manipulation Procedure



21.5.2 Flash memory programming mode

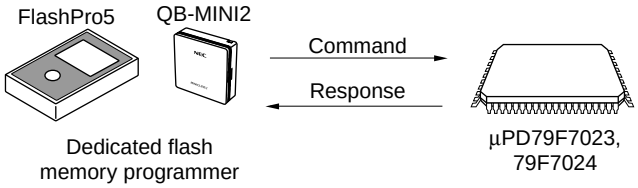
To rewrite the contents of the flash memory by using the dedicated flash memory programmer, set the µPD79F7023, 79F7024 in the flash memory programming mode. The system switches to the flash memory programming mode once the dedicated flash memory programmer is connected and communication starts.

Change the mode by using a jumper when writing the flash memory on-board.

21.5.3 Communication commands

The µPD79F7023, 79F7024 communicate with the dedicated flash memory programmer by using commands. The signals sent from the flash memory programmer to the µPD79F7023, 79F7024 are called commands, and the signals sent from the µPD79F7023, 79F7024 to the dedicated flash memory programmer are called response.

Figure 21-7. Communication Commands



The flash memory control commands of the µPD79F7023, 79F7024 are listed in the table below. All these commands are issued from the programmer and the µPD79F7023, 79F7024 perform processing corresponding to the respective commands.

Table 21-5. Flash Memory Control Commands

Classification	Command Name	Function
Verify	Verify	Compares the contents of a specified area of the flash memory with data transmitted from the programmer.
Erase	Chip Erase	Erases the entire flash memory.
	Block Erase	Erases a specified area in the flash memory.
Blank check	Block Blank Check	Checks if a specified block in the flash memory has been correctly erased.
Write	Programming	Writes data to a specified area in the flash memory.
Getting information	Silicon Signature	Gets μPD79F7023, 79F7024 information (such as the part number and flash memory configuration).
	Version Get	Gets the μPD79F7023, 79F7024 version and firmware version.
	Checksum	Gets the checksum data for a specified area.
Security	Security Set	Sets security information.
Others	Reset	Used to detect synchronization status of communication.
	Baud Rate Set	Sets baud rate when UART communication mode is selected.

The μPD79F7023, 79F7024 return a response for the command issued by the dedicated flash memory programmer. The response names sent from the μPD79F7023, 79F7024 are listed below.

Table 21-6. Response Names

Response Name	Function
ACK	Acknowledges command/data.
NAK	Acknowledges illegal command/data.

21.6 Security Settings

The μPD79F7023, 79F7024 support a security function that prohibits rewriting the user program written to the internal flash memory, so that the program cannot be changed by an unauthorized person.

The operations shown below can be performed using the Security Set command. The security setting is valid when the programming mode is set next.

- Disabling batch erase (chip erase)
  Execution of the block erase and batch erase (chip erase) commands for entire blocks in the flash memory is prohibited by this setting during on-board/off-board programming. Once execution of the batch erase (chip erase) command is prohibited, all of the prohibition settings (including prohibition of batch erase (chip erase)) can no longer be cancelled.

  Caution After the security setting for the batch erase is set, erasure cannot be performed for the device. In addition, even if a write command is executed, data different from that which has already been written to the flash memory cannot be written, because the erase command is disabled.

- Disabling block erase
  Execution of the block erase command for a specific block in the flash memory is prohibited during on-board/off-board programming. However, blocks can be erased by means of self programming.

- Disabling write
  Execution of the write and block erase commands for entire blocks in the flash memory is prohibited during on-board/off-board programming. However, blocks can be written by means of self programming.

- Disabling rewriting boot cluster 0
  Execution of the block erase command and write command on boot cluster 0 (0000H to 0FFFH) in the flash memory is prohibited by this setting. Execution of the batch erase (chip erase) command is also prohibited by this setting.

The batch erase (chip erase), block erase, write commands, and rewriting boot cluster 0 are enabled by the default setting when the flash memory is shipped. Security can be set by on-board/off-board programming and self programming. Each security setting can be used in combination.

All the security settings are cleared by executing the batch erase (chip erase) command.

Table 21-7 shows the relationship between the erase and write commands when the μPD79F7023, 79F7024 security function is enabled.

Table 21-7. Relationship Between Enabling Security Function and Command

(1) During on-board/off-board programming

Valid Security	Executed Command		
	Batch Erase (Chip Erase)	Block Erase	Write
Prohibition of batch erase (chip erase)	Cannot be erased in batch	Blocks cannot be erased.	Can be performed[Note].
Prohibition of block erase	Can be erased in batch.		Can be performed.
Prohibition of writing			Cannot be performed.
Prohibition of rewriting boot cluster 0	Cannot be erased in batch	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Note Confirm that no data has been written to the write area. Because data cannot be erased after batch erase (chip erase) is prohibited, do not write data if the data has not been erased.

(2) During self programming

Valid Security	Executed Command	
	Block Erase	Write
Prohibition of batch erase (chip erase)	Blocks can be erased.	Can be performed.
Prohibition of block erase		
Prohibition of writing		
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Table 21-8 shows how to perform security settings in each programming mode.

Table 21-8. Setting Security in Each Programming Mode

(1) On-board/off-board programming

Security	Security Setting	How to Disable Security Setting
Prohibition of batch erase (chip erase)	Set via GUI of dedicated flash memory programmer, etc.	Cannot be disabled after set.
Prohibition of block erase		Execute batch erase (chip erase) command
Prohibition of writing		
Prohibition of rewriting boot cluster 0		Cannot be disabled after set.

(2) Self programming

Security	Security Setting	How to Disable Security Setting
Prohibition of batch erase (chip erase)	Set by using information library.	Cannot be disabled after set.
Prohibition of block erase		Execute batch erase (chip erase) command during on-board/off-board programming (cannot be disabled during self programming)
Prohibition of writing		
Prohibition of rewriting boot cluster 0		

21.7 Flash Memory Programming by Self Programming

The μPD79F7023, 79F7024 support a self programming function that can be used to rewrite the flash memory via a user program. Because this function allows a user application to rewrite the flash memory by using the μPD79F7023, 79F7024 self programming library, it can be used to upgrade the program in the field.

If an interrupt occurs during self programming, self programming can be temporarily stopped and interrupt servicing can be executed. If an unmasked interrupt request is generated in the EI state, the request branches directly from the self programming library to the interrupt routine. After the self programming mode is later restored, self programming can be resumed. However, the interrupt response time is different from that of the normal operation mode.

Cautions 1. To prohibit an interrupt during self programming, in the same way as in the normal operation mode, execute the self programming library in the state where the IE flag is cleared (0) by the DI instruction. To enable an interrupt, clear (0) the interrupt mask flag to accept in the state where the IE flag is set (1) by the EI instruction, and then execute the self programming library.

2. Make sure that the regulator output voltage mode is fixed when executing self programming.

3. The power supply voltage range in which the flash memory can be rewritten in normal power mode is V_{DD} ≥ 2.5 V. Note that program area can be rewritten by using the self programming library in normal power mode.

4. Rewriting the flash memory is prohibited in low power consumption mode.

Remark For details of the self programming function and the self programming library, refer to **"78K0 Microcontrollers User's Manual Self Programming Library Type 01 (U18274E)"** and **"78K0 Microcontrollers Self Programming Library Type 01 Ver. 3.10 Operating Precautions (notification document) (ZUD-CD-09-0122)"**.

21.7.1 Register controlling self programming mode

The self programming mode is controlled by the self programming mode control register (FPCTL).

FPCTL can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears FPCTL to 00H.

Figure 21-8. Format of Self Programming Mode Control Register (FPCTL)

Address: FF2BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
FPCTL	0	0	0	0	0	0	0	FLMDPUP Note

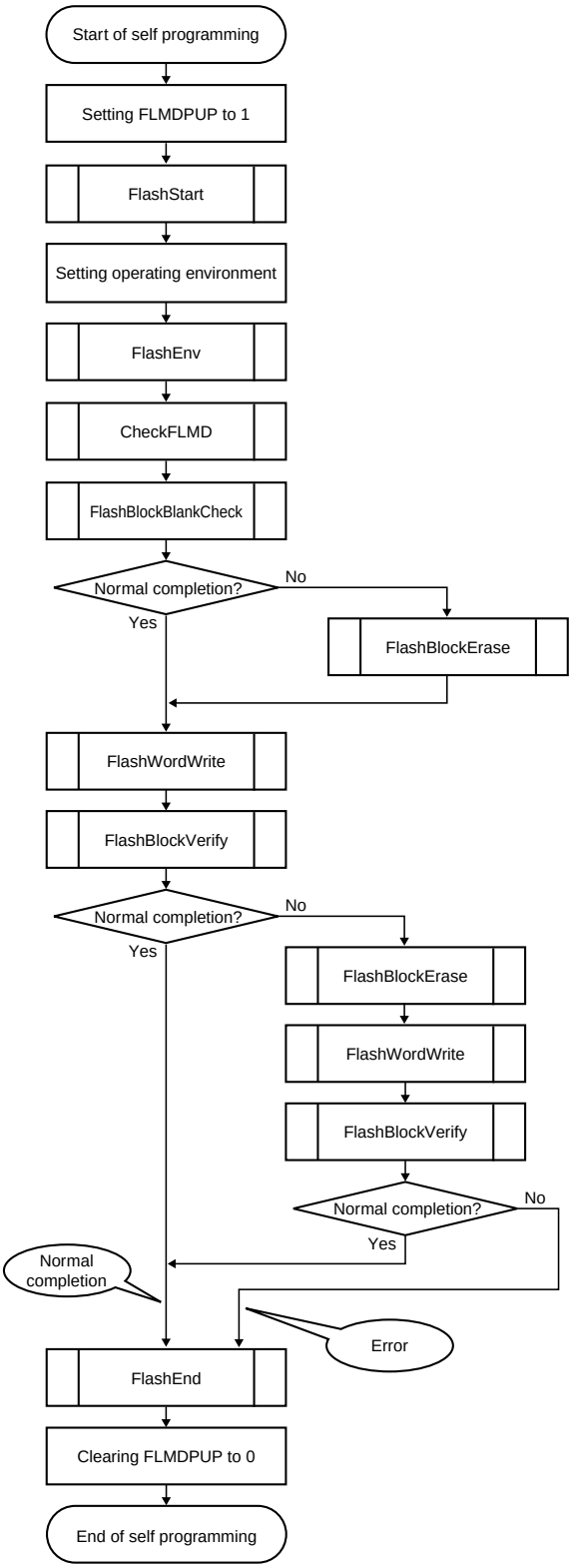
FLMDPUP Note	Self programming mode control
0	Normal operation mode
1	Self programming mode

Note The FLMDPUP bit must be set to 0 (normal operation mode) while the regular user program is being executed, and set to 1 (self programming mode) while self programming is being executed. The flash memory rewrite circuit does not operate in normal operation mode, so even though the firmware and software for rewriting will work, no actual rewriting will take place.

21.7.2 Flow of self programming (Rewriting Flash Memory)

The following figure illustrates a flow of rewriting the flash memory by using a self programming library.

Figure 21-9. Flow of Self Programming (Rewriting Flash Memory)



Remark For details of the self programming function and the self programming library, refer to **"78K0 Microcontrollers User's Manual Self Programming Library Type 01 (U18274E)"** and **"78K0 Microcontrollers Self Programming Library Type 01 Ver. 3.10 Operating Precautions (notification document) (ZUD-CD-09-0122)"**.

21.7.3 Boot swap function

If rewriting the boot area failed by temporary power failure or other reasons, restarting a program by resetting or overwriting is disabled due to data destruction in the boot area.

The boot swap function is used to avoid this problem.

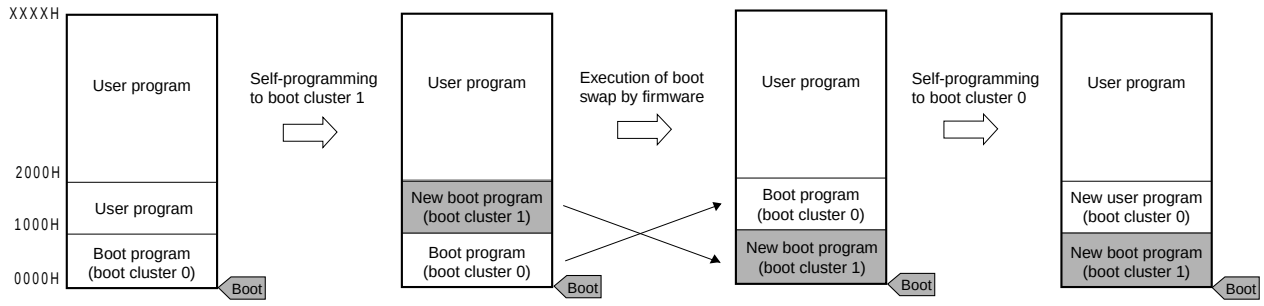
Before erasing boot cluster 0[Note], which is a boot program area, by self programming, write a new boot program to boot cluster 1 in advance. When the program has been correctly written to boot cluster 1, swap this boot cluster 1 and boot cluster 0 by using the set information function of the firmware of the µPD79F7023, 79F7024 microcontrollers, so that boot cluster 1 is used as a boot area. After that, erase or write the original boot program area, boot cluster 0.

As a result, even if a power failure occurs while the boot programming area is being rewritten, the program is executed correctly because it is booted from boot cluster 1 to be swapped when the program is reset and started next.

Note A boot cluster is a 4 KB area and boot clusters 0 and 1 are swapped by the boot swap function.

Caution The products whose ROM size is 4 KB can not use the boot swap function.

Figure 21-10. Boot Swap Function

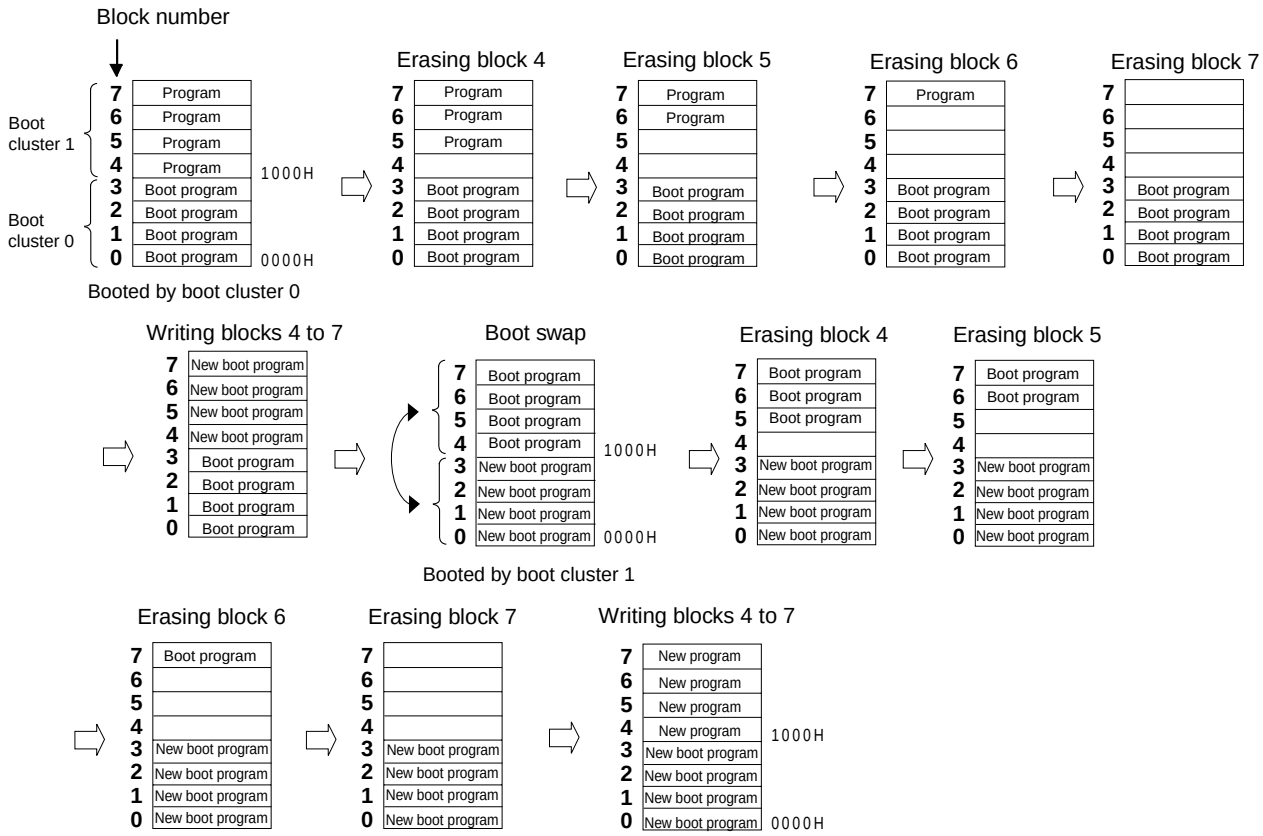


In an example of above figure, it is as follows.

Boot cluster 0: Boot program area before boot swap

Boot cluster 1: Boot program area after boot swap

Figure 21-11. Example of Executing Boot Swapping



CHAPTER 22 ON-CHIP DEBUG FUNCTION

22.1 Connecting QB-MINI2 to µPD79F7023, 79F7024

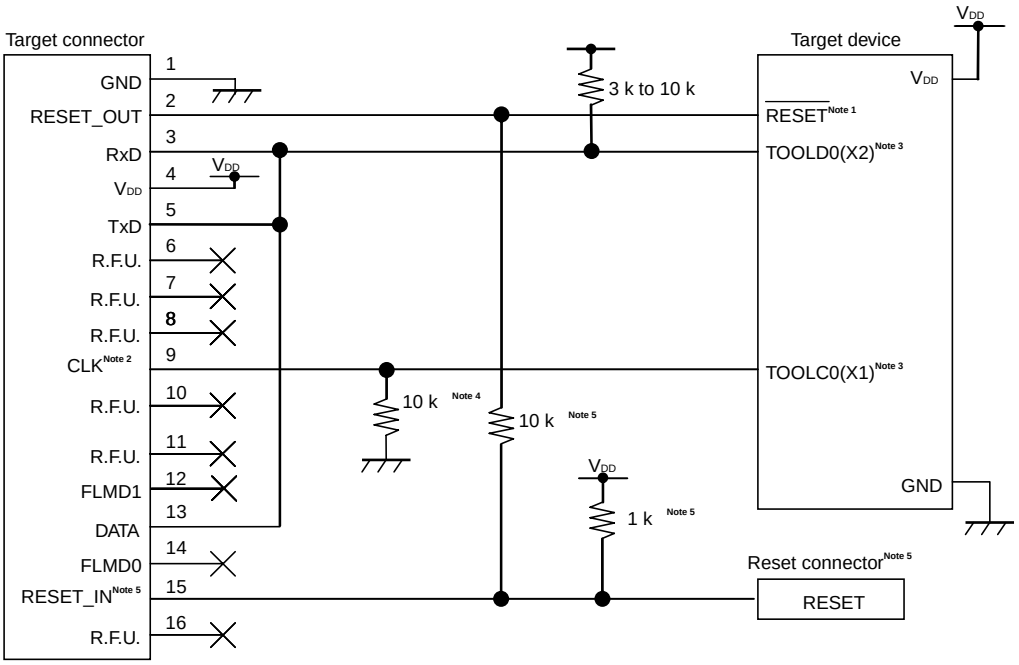
The µPD79F7023, 79F7024 use the V_{DD}, $\overline{RESET}$, TOOLC0/X1, TOOLD0/X2, and V_{SS} pins to communicate with the host machine via an on-chip debug emulator (QB-MINI2).

Cautions 1. The µPD79F7023, 79F7024 have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. When transitioning to STOP mode during on-chip debugging, oscillation of the internal high-speed oscillator continues, but the on-chip debug operation is not affected.

Figure 22-1. Connection Example of QB-MINI2 and µPD79F7023, 79F7024 (1/2)

(1) When using the TOOLC0 and TOOLD0 pins (X1 oscillator or EXCLK input clock is not used, both debugging and programming are performed)



Notes 1. If there are capacitance elements such as capacitors, on-chip debugging might not operate normally.

2. A clock signal provided on the 78K0-OCD board, a 4 or 8 MHz clock signal generated in QB-MINI2, or the clock signal generated by the internal high-speed oscillator of the device can be used for the clock signal of the target device during on-chip debugging.
Only the internal high-speed oscillator of the device can be used during flash programming.

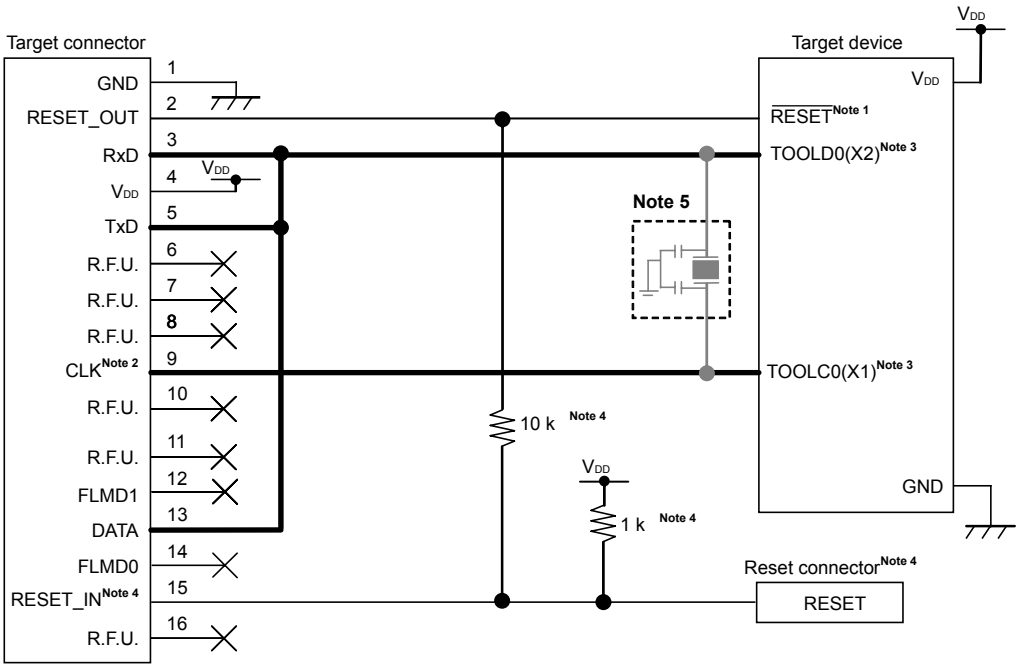
3. During on-chip debugging, the settings specified by the user program are ignored, because these pins are used as pins dedicated to on-chip debugging. However, if the pins are specified as input pins, the pins must be processed (because they are left open when QB-MINI2 is not connected.)

4. This is the processing for the pin that is unused (the input is left open) when the target device operates (when QB-MINI2 is not connected). (This processing is not required if an oscillator circuit is used.)

5. This connection is designed assuming that the reset signal is output from the N-ch open-drain buffer (output resistance: 100 Ω or less).

Figure 22-1. Connection Example of QB-MINI2 and µPD79F7023, 79F7024 (2/2)

(2) When using the TOOLC0 and TOOLD0 pins (with X1/X2 oscillator is used, both debugging and programming are performed)



Notes 1. If there are capacitance elements such as capacitors, on-chip debugging might not operate normally.

2. A clock signal provided on the 78K0-OCD board, a 4 or 8 MHz clock signal generated in QB-MINI2, or the clock signal generated by the internal high-speed oscillator of the device can be used for the clock signal of the target device during on-chip debugging.
Only the internal high-speed oscillator of the device can be used during flash programming.

3. During on-chip debugging, the settings specified by the user program are ignored, because these pins are used as pins dedicated to on-chip debugging. However, if the pins are specified as input pins, the pins must be processed (because they are left open when QB-MINI2 is not connected.)

4. This connection is designed assuming that the reset signal is output from the N-ch open-drain buffer (output resistance: 100 Ω or less). For details, refer to **4.1.3 Connection of reset pin** of QB-MINI2 On-Chip Debug Emulator with Programming Function (18371E).

5. Never connect an oscillation circuit to the 78K0-OCD board during on-chip debugging and flash programming.
To prevent an oscillation circuit from not oscillating due to wiring capacitance when the target device operates (when QB-MINI2 is not connected), also consider countermeasures such as disconnecting the oscillation circuit from the target connectors by setting the jumpers.
A program that was downloaded using the debugger does not operate when QB-MINI2 is not connected.

Caution The bold lines in the figure (TOOLD0 and TOOLC0) must be designed so that the device pins are less than 30 mm from the QB-MINI2 connectors or the paths must be shielded by connecting them to GND.

22.2 On-Chip Debug Security ID

The µPD79F7023, 79F7024 have an on-chip debug operation control bit in the flash memory at 0084H (refer to **CHAPTER 20 OPTION BYTE**) and an on-chip debug security ID setting area at 0085H to 008EH, to prevent third parties from reading memory content.

When the boot swap function is used, also set a value that is the same as that of 1084H and 1085H to 108EH in advance, because 0084H, 0085H to 008EH and 1083H, and 1085H to 108EH are switched.

For details on the on-chip debug security ID, refer to the **QB-MINI2 On-Chip Debug Emulator with Programming Function User's Manual (U18371E)**.

Table 22-1. On-Chip Debug Security ID

Address	On-Chip Debug Security ID
0085H to 008EH	Any ID code of 10 bytes
1085H to 108EH	

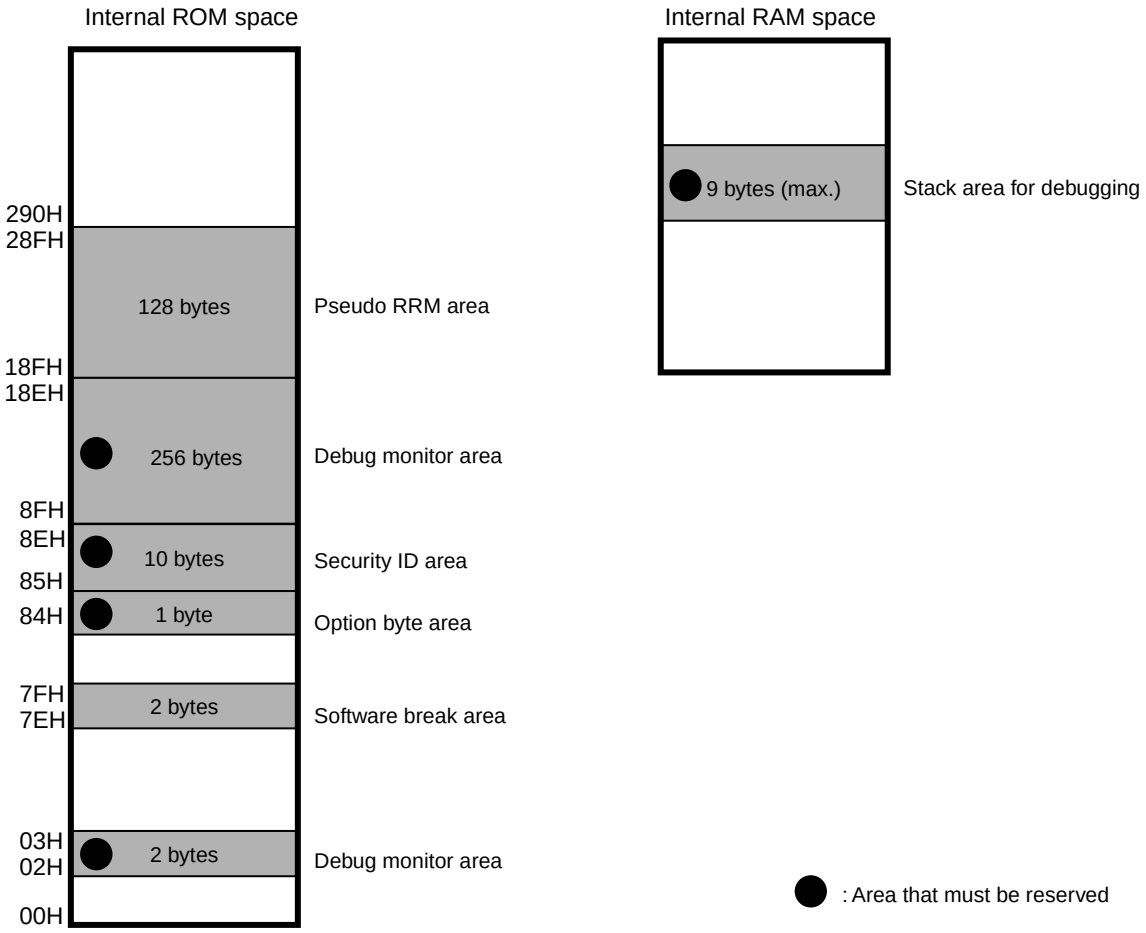
22.3 Securing of User Resources

QB-MINI2 uses the user memory spaces (shaded portions in Figure 22-2) to implement communication with the target device, or each debug functions. The areas marked with a dot (•) are always used for debugging, and other areas are used for each debug function used.

These areas can be secured by using user programs or the linker option.

For details on the securing of these areas, refer to the **QB-MINI2 On-Chip Debug Emulator with Programming Function User's Manual (U18371E)**.

Figure 22-2. Reserved Area Used by QB-MINI2



CHAPTER 23 INSTRUCTION SET

This chapter lists each instruction set of the µPD79F7023, 79F7024 in table form. For details of each operation and operation code, refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

23.1 Conventions Used in Operation List

23.1.1 Operand identifiers and specification methods

Operands are written in the "Operand" column of each instruction in accordance with the specification method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more methods, select one of them. Uppercase letters and the symbols #, !, $ and [ ] are keywords and must be written as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to write the #, !, $, and [ ] symbols.

For operand register identifiers r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for specification.

Table 27-1. Operand Identifiers and Specification Methods

Identifier	Specification Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol[Note]
sfrp	Special function register symbol (16-bit manipulatable register even addresses only)[Note]
saddr	FE20H to FF1FH Immediate data or labels
saddrp	FE20H to FF1FH Immediate data or labels (even address only)
addr16	0000H to FFFFH Immediate data or labels (Only even addresses for 16-bit data transfer instructions)
addr11	0800H to 0FFFH Immediate data or labels
addr5	0040H to 007FH Immediate data or labels (even address only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label
RBn	RB0 to RB3

Note Addresses from FFD0H to FFDFH cannot be accessed with these operands.

Remark For special function register symbols, refer to **Table 3-6 Special Function Register List**.

23.1.2 Description of operation column

A: A register; 8-bit accumulator
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair; 16-bit accumulator
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
RBS: Register bank select flag
IE: Interrupt request enable flag
( ): Memory contents indicated by address or register contents in parentheses
X_H, X_L: Higher 8 bits and lower 8 bits of 16-bit register
∧: Logical product (AND)
∨: Logical sum (OR)
$\veebar$: Exclusive logical sum (exclusive OR)
$\overline{\ \ }$: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

23.1.3 Description of flag operation column

(Blank): Not affected
0: Cleared to 0
1: Set to 1
×: Set/cleared according to the result
R: Previously saved value is restored

23.2 Operation List

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit data transfer	**MOV**	r, #byte	2	4	–	r ← byte	
		saddr, #byte	3	6	7	(saddr) ← byte	
		sfr, #byte	3	–	7	sfr ← byte	
		A, r Note 3	1	2	–	A ← r	
		r, A Note 3	1	2	–	r ← A	
		A, saddr	2	4	5	A ← (saddr)	
		saddr, A	2	4	5	(saddr) ← A	
		A, sfr	2	–	5	A ← sfr	
		sfr, A	2	–	5	sfr ← A	
		A, !addr16	3	8	9	A ← (addr16)	
		!addr16, A	3	8	9	(addr16) ← A	
		PSW, #byte	3	–	7	PSW ← byte	× × ×
		A, PSW	2	–	5	A ← PSW	
		PSW, A	2	–	5	PSW ← A	× × ×
		A, [DE]	1	4	5	A ← (DE)	
		[DE], A	1	4	5	(DE) ← A	
		A, [HL]	1	4	5	A ← (HL)	
		[HL], A	1	4	5	(HL) ← A	
		A, [HL + byte]	2	8	9	A ← (HL + byte)	
		[HL + byte], A	2	8	9	(HL + byte) ← A	
		A, [HL + B]	1	6	7	A ← (HL + B)	
		[HL + B], A	1	6	7	(HL + B) ← A	
		A, [HL + C]	1	6	7	A ← (HL + C)	
		[HL + C], A	1	6	7	(HL + C) ← A	
	XCH	A, r Note 3	1	2	–	A ↔ r	
		A, saddr	2	4	6	A ↔ (saddr)	
		A, sfr	2	–	6	A ↔ (sfr)	
		A, !addr16	3	8	10	A ↔ (addr16)	
		A, [DE]	1	4	6	A ↔ (DE)	
		A, [HL]	1	4	6	A ↔ (HL)	
		A, [HL + byte]	2	8	10	A ↔ (HL + byte)	
		A, [HL + B]	2	8	10	A ↔ (HL + B)	
		A, [HL + C]	2	8	10	A ↔ (HL + C)	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
16-bit data transfer	**MOVW**	rp, #word	3	6	–	rp ← word	
		saddrp, #word	4	8	10	(saddrp) ← word	
		sfrp, #word	4	–	10	sfrp ← word	
		AX, saddrp	2	6	8	AX ← (saddrp)	
		saddrp, AX	2	6	8	(saddrp) ← AX	
		AX, sfrp	2	–	8	AX ← sfrp	
		sfrp, AX	2	–	8	sfrp ← AX	
		AX, rp Note 3	1	4	–	AX ← rp	
		rp, AX Note 3	1	4	–	rp ← AX	
		AX, !addr16	3	10	12	AX ← (addr16)	
		!addr16, AX	3	10	12	(addr16) ← AX	
	XCHW	AX, rp Note 3	1	4	–	AX ↔ rp	
8-bit operation	**ADD**	A, #byte	2	4	–	A, CY ← A + byte	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte	× × ×
		A, r Note 4	2	4	–	A, CY ← A + r	× × ×
		r, A	2	4	–	r, CY ← r + A	× × ×
		A, saddr	2	4	5	A, CY ← A + (saddr)	× × ×
		A, !addr16	3	8	9	A, CY ← A + (addr16)	× × ×
		A, [HL]	1	4	5	A, CY ← A + (HL)	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A + (HL + byte)	× × ×
		A, [HL + B]	2	8	9	A, CY ← A + (HL + B)	× × ×
		A, [HL + C]	2	8	9	A, CY ← A + (HL + C)	× × ×
	ADDC	A, #byte	2	4	–	A, CY ← A + byte + CY	× × ×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) + byte + CY	× × ×
		A, r Note 4	2	4	–	A, CY ← A + r + CY	× × ×
		r, A	2	4	–	r, CY ← r + A + CY	× × ×
		A, saddr	2	4	5	A, CY ← A + (saddr) + CY	× × ×
		A, !addr16	3	8	9	A, CY ← A + (addr16) + C	× × ×
		A, [HL]	1	4	5	A, CY ← A + (HL) + CY	× × ×
		A, [HL + byte]	2	8	9	A, CY ← A + (HL + byte) + CY	× × ×
		A, [HL + B]	2	8	9	A, CY ← A + (HL + B) + CY	× × ×
		A, [HL + C]	2	8	9	A, CY ← A + (HL + C) + CY	× × ×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Only when rp = BC, DE or HL

4. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit operation	**SUB**	A, #byte	2	4	–	A, CY ← A – byte	×	×	×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte	×	×	×
		A, r Note 3	2	4	–	A, CY ← A – r	×	×	×
		r, A	2	4	–	r, CY ← r – A	×	×	×
		A, saddr	2	4	5	A, CY ← A – (saddr)	×	×	×
		A, !addr16	3	8	9	A, CY ← A – (addr16)	×	×	×
		A, [HL]	1	4	5	A, CY ← A – (HL)	×	×	×
		A, [HL + byte]	2	8	9	A, CY ← A – (HL + byte)	×	×	×
		A, [HL + B]	2	8	9	A, CY ← A – (HL + B)	×	×	×
		A, [HL + C]	2	8	9	A, CY ← A – (HL + C)	×	×	×
	SUBC	A, #byte	2	4	–	A, CY ← A – byte – CY	×	×	×
		saddr, #byte	3	6	8	(saddr), CY ← (saddr) – byte – CY	×	×	×
		A, r Note 3	2	4	–	A, CY ← A – r – CY	×	×	×
		r, A	2	4	–	r, CY ← r – A – CY	×	×	×
		A, saddr	2	4	5	A, CY ← A – (saddr) – CY	×	×	×
		A, !addr16	3	8	9	A, CY ← A – (addr16) – CY	×	×	×
		A, [HL]	1	4	5	A, CY ← A – (HL) – CY	×	×	×
		A, [HL + byte]	2	8	9	A, CY ← A – (HL + byte) – CY	×	×	×
		A, [HL + B]	2	8	9	A, CY ← A – (HL + B) – CY	×	×	×
		A, [HL + C]	2	8	9	A, CY ← A – (HL + C) – CY	×	×	×
	AND	A, #byte	2	4	–	A ← A ∧ byte	×		
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∧ byte	×		
		A, r Note 3	2	4	–	A ← A ∧ r	×		
		r, A	2	4	–	r ← r ∧ A	×		
		A, saddr	2	4	5	A ← A ∧ (saddr)	×		
		A, !addr16	3	8	9	A ← A ∧ (addr16)	×		
		A, [HL]	1	4	5	A ← A ∧ (HL)	×		
		A, [HL + byte]	2	8	9	A ← A ∧ (HL + byte)	×		
		A, [HL + B]	2	8	9	A ← A ∧ (HL + B)	×		
		A, [HL + C]	2	8	9	A ← A ∧ (HL + C)	×		

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
8-bit operation	**OR**	A, #byte	2	4	–	A ← A ∨ byte	×
		saddr, #byte	3	6	8	(saddr) ← (saddr) ∨ byte	×
		A, r Note 3	2	4	–	A ← A ∨ r	×
		r, A	2	4	–	r ← r ∨ A	×
		A, saddr	2	4	5	A ← A ∨ (saddr)	×
		A, !addr16	3	8	9	A ← A ∨ (addr16)	×
		A, [HL]	1	4	5	A ← A ∨ (HL)	×
		A, [HL + byte]	2	8	9	A ← A ∨ (HL + byte)	×
		A, [HL + B]	2	8	9	A ← A ∨ (HL + B)	×
		A, [HL + C]	2	8	9	A ← A ∨ (HL + C)	×
	XOR	A, #byte	2	4	–	A ← A ⊻ byte	×
		saddr, #byte	3	6	8	(saddr) ← (saddr) ⊻ byte	×
		A, r Note 3	2	4	–	A ← A ⊻ r	×
		r, A	2	4	–	r ← r ⊻ A	×
		A, saddr	2	4	5	A ← A ⊻ (saddr)	×
		A, !addr16	3	8	9	A ← A ⊻ (addr16)	×
		A, [HL]	1	4	5	A ← A ⊻ (HL)	×
		A, [HL + byte]	2	8	9	A ← A ⊻ (HL + byte)	×
		A, [HL + B]	2	8	9	A ← A ⊻ (HL + B)	×
		A, [HL + C]	2	8	9	A ← A ⊻ (HL + C)	×
	CMP	A, #byte	2	4	–	A – byte	× × ×
		saddr, #byte	3	6	8	(saddr) – byte	× × ×
		A, r Note 3	2	4	–	A – r	× × ×
		r, A	2	4	–	r – A	× × ×
		A, saddr	2	4	5	A – (saddr)	× × ×
		A, !addr16	3	8	9	A – (addr16)	× × ×
		A, [HL]	1	4	5	A – (HL)	× × ×
		A, [HL + byte]	2	8	9	A – (HL + byte)	× × ×
		A, [HL + B]	2	8	9	A – (HL + B)	× × ×
		A, [HL + C]	2	8	9	A – (HL + C)	× × ×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

3. Except “r = A”

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
16-bit operation	**ADDW**	AX, #word	3	6	–	AX, CY ← AX + word	×	×	×
	SUBW	AX, #word	3	6	–	AX, CY ← AX – word	×	×	×
	CMPW	AX, #word	3	6	–	AX – word	×	×	×
Multiply/ divide	**MULU**	X	2	16	–	AX ← A × X			
	DIVUW	C	2	25	–	AX (Quotient), C (Remainder) ← AX ÷ C			
Increment/ decrement	**INC**	r	1	2	–	r ← r + 1	×	×	
		saddr	2	4	6	(saddr) ← (saddr) + 1	×	×	
	DEC	r	1	2	–	r ← r – 1	×	×	
		saddr	2	4	6	(saddr) ← (saddr) – 1	×	×	
	INCW	rp	1	4	–	rp ← rp + 1			
	DECW	rp	1	4	–	rp ← rp – 1			
Rotate	**ROR**	A, 1	1	2	–	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1 time			×
	ROL	A, 1	1	2	–	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1 time			×
	RORC	A, 1	1	2	–	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1 time			×
	ROLC	A, 1	1	2	–	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1 time			×
	ROR4	[HL]	2	10	12	A_{3-0} ← $(HL)_{3-0}$, $(HL)_{7-4}$ ← A_{3-0}, $(HL)_{3-0}$ ← $(HL)_{7-4}$			
	ROL4	[HL]	2	10	12	A_{3-0} ← $(HL)_{7-4}$, $(HL)_{3-0}$ ← A_{3-0}, $(HL)_{7-4}$ ← $(HL)_{3-0}$			
BCD adjustment	**ADJBA**		2	4	–	Decimal Adjust Accumulator after Addition	×	×	×
	ADJBS		2	4	–	Decimal Adjust Accumulator after Subtract	×	×	×
Bit manipulate	**MOV1**	CY, saddr.bit	3	6	7	CY ← (saddr.bit)			×
		CY, sfr.bit	3	–	7	CY ← sfr.bit			×
		CY, A.bit	2	4	–	CY ← A.bit			×
		CY, PSW.bit	3	–	7	CY ← PSW.bit			×
		CY, [HL].bit	2	6	7	CY ← (HL).bit			×
		saddr.bit, CY	3	6	8	(saddr.bit) ← CY			
		sfr.bit, CY	3	–	8	sfr.bit ← CY			
		A.bit, CY	2	4	–	A.bit ← CY			
		PSW.bit, CY	3	–	8	PSW.bit ← CY	×	×	
		[HL].bit, CY	2	6	8	(HL).bit ← CY			

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
Bit manipulate	**AND1**	CY, saddr.bit	3	6	7	CY ← CY ∧ (saddr.bit)	×
		CY, sfr.bit	3	–	7	CY ← CY ∧ sfr.bit	×
		CY, A.bit	2	4	–	CY ← CY ∧ A.bit	×
		CY, PSW.bit	3	–	7	CY ← CY ∧ PSW.bit	×
		CY, [HL].bit	2	6	7	CY ← CY ∧ (HL).bit	×
	OR1	CY, saddr.bit	3	6	7	CY ← CY ∨ (saddr.bit)	×
		CY, sfr.bit	3	–	7	CY ← CY ∨ sfr.bit	×
		CY, A.bit	2	4	–	CY ← CY ∨ A.bit	×
		CY, PSW.bit	3	–	7	CY ← CY ∨ PSW.bit	×
		CY, [HL].bit	2	6	7	CY ← CY ∨ (HL).bit	×
	XOR1	CY, saddr.bit	3	6	7	CY ← CY ⊻ (saddr.bit)	×
		CY, sfr.bit	3	–	7	CY ← CY ⊻ sfr.bit	×
		CY, A.bit	2	4	–	CY ← CY ⊻ A.bit	×
		CY, PSW. bit	3	–	7	CY ← CY ⊻ PSW.bit	×
		CY, [HL].bit	2	6	7	CY ← CY ⊻ (HL).bit	×
	SET1	saddr.bit	2	4	6	(saddr.bit) ← 1	
		sfr.bit	3	–	8	sfr.bit ← 1	
		A.bit	2	4	–	A.bit ← 1	
		PSW.bit	2	–	6	PSW.bit ← 1	× × ×
		[HL].bit	2	6	8	(HL).bit ← 1	
	CLR1	saddr.bit	2	4	6	(saddr.bit) ← 0	
		sfr.bit	3	–	8	sfr.bit ← 0	
		A.bit	2	4	–	A.bit ← 0	
		PSW.bit	2	–	6	PSW.bit ← 0	× × ×
		[HL].bit	2	6	8	(HL).bit ← 0	
	SET1	CY	1	2	–	CY ← 1	1
	CLR1	CY	1	2	–	CY ← 0	0
	NOT1	CY	1	2	–	CY ← $\overline{CY}$	×

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
Call/return	**CALL**	!addr16	3	7	–	(SP – 1) ← (PC + 3)H, (SP – 2) ← (PC + 3)L, PC ← addr16, SP ← SP – 2	
	CALLF	!addr11	2	5	–	(SP – 1) ← (PC + 2)H, (SP – 2) ← (PC + 2)L, PC15 – 11 ← 00001, PC10 – 0 ← addr11, SP ← SP – 2	
	CALLT	[addr5]	1	6	–	(SP – 1) ← (PC + 1)H, (SP – 2) ← (PC + 1)L, PCH ← (addr5 + 1), PCL ← (addr5), SP ← SP – 2	
	BRK		1	6	–	(SP – 1) ← PSW, (SP – 2) ← (PC + 1)H, (SP – 3) ← (PC + 1)L, PCH ← (003FH), PCL ← (003EH), SP ← SP – 3, IE ← 0	
	RET		1	6	–	PCH ← (SP + 1), PCL ← (SP), SP ← SP + 2	
	RETI		1	6	–	PCH ← (SP + 1), PCL ← (SP), PSW ← (SP + 2), SP ← SP + 3	R R R
	RETB		1	6	–	PCH ← (SP + 1), PCL ← (SP), PSW ← (SP + 2), SP ← SP + 3	R R R
Stack manipulate	**PUSH**	PSW	1	2	–	(SP – 1) ← PSW, SP ← SP – 1	
		rp	1	4	–	(SP – 1) ← rpH, (SP – 2) ← rpL, SP ← SP – 2	
	POP	PSW	1	2	–	PSW ← (SP), SP ← SP + 1	R R R
		rp	1	4	–	rpH ← (SP + 1), rpL ← (SP), SP ← SP + 2	
	MOVW	SP, #word	4	–	10	SP ← word	
		SP, AX	2	–	8	SP ← AX	
		AX, SP	2	–	8	AX ← SP	
Unconditional branch	**BR**	!addr16	3	6	–	PC ← addr16	
		$addr16	2	6	–	PC ← PC + 2 + jdisp8	
		AX	2	8	–	PCH ← A, PCL ← X	
Conditional branch	**BC**	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if CY = 1	
	BNC	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if CY = 0	
	BZ	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if Z = 1	
	BNZ	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if Z = 0	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
Conditional branch	**BT**	saddr.bit, $addr16	3	8	9	PC ← PC + 3 + jdisp8 if (saddr.bit) = 1	
		sfr.bit, $addr16	4	–	11	PC ← PC + 4 + jdisp8 if sfr.bit = 1	
		A.bit, $addr16	3	8	–	PC ← PC + 3 + jdisp8 if A.bit = 1	
		PSW.bit, $addr16	3	–	9	PC ← PC + 3 + jdisp8 if PSW.bit = 1	
		[HL].bit, $addr16	3	10	11	PC ← PC + 3 + jdisp8 if (HL).bit = 1	
	BF	saddr.bit, $addr16	4	10	11	PC ← PC + 4 + jdisp8 if (saddr.bit) = 0	
		sfr.bit, $addr16	4	–	11	PC ← PC + 4 + jdisp8 if sfr.bit = 0	
		A.bit, $addr16	3	8	–	PC ← PC + 3 + jdisp8 if A.bit = 0	
		PSW.bit, $addr16	4	–	11	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
		[HL].bit, $addr16	3	10	11	PC ← PC + 3 + jdisp8 if (HL).bit = 0	
	BTCLR	saddr.bit, $addr16	4	10	12	PC ← PC + 4 + jdisp8 if (saddr.bit) = 1 then reset (saddr.bit)	
		sfr.bit, $addr16	4	–	12	PC ← PC + 4 + jdisp8 if sfr.bit = 1 then reset sfr.bit	
		A.bit, $addr16	3	8	–	PC ← PC + 3 + jdisp8 if A.bit = 1 then reset A.bit	
		PSW.bit, $addr16	4	–	12	PC ← PC + 4 + jdisp8 if PSW.bit = 1 then reset PSW.bit	× × ×
		[HL].bit, $addr16	3	10	12	PC ← PC + 3 + jdisp8 if (HL).bit = 1 then reset (HL).bit	
	DBNZ	B, $addr16	2	6	–	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
		C, $addr16	2	6	–	C ← C –1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
		saddr, $addr16	3	8	10	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
CPU control	**SEL**	RBn	2	4	–	RBS1, 0 ← n	
	NOP		1	2	–	No Operation	
	EI		2	–	6	IE ← 1 (Enable Interrupt)	
	DI		2	–	6	IE ← 0 (Disable Interrupt)	
	HALT		2	6	–	Set HALT Mode	
	STOP		2	6	–	Set STOP Mode	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

23.3 Instructions Listed by Addressing Type

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

First Operand \ Second Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except “r = A”

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

Second Operand / First Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Second Operand / First Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Second Operand / First Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound instruction					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

CHAPTER 24 ELECTRICAL SPECIFICATIONS

Cautions The µPD79F7023, 79F7024 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to + 6.5	V
	V_{SS}		−0.5 to + 0.3	V
	AV_{REF}		−0.5 to V_{DD} + 0.3 Note 1	V
REGC pin input voltage Note 2	V_{IREGC}		−0.5 to + 3.6 and −0.5 to V_{DD} + 0.3	V
Input voltage	V_{I1}	P30 to P34, P121, P122, P125, X1, X2, $\overline{\text{RESET}}$	−0.3 to V_{DD} + 0.3 Note 1	V
	V_{I2}	P20 to P27	−0.3 to AV_{REF} + 0.3 Note 1 and −0.3 to V_{DD} + 0.3 Note 1	V
Output voltage	V_{O1}	P30 to P34, P121, P122	−0.3 to V_{DD} + 0.3 Note 1	V
	V_{O2}	P20 to P27	−0.3 to AV_{REF} + 0.3 Note 1	V

Notes 1. Must be 6.5 V or lower.

2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 µF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P31 to P34	−10	mA
		Total of all pins		−25	mA
	I_{OH2}	Per pin	P30	−10	mA
		Total of all pins		−10	mA
	I_{OH3}	Per pin	P20 to P27	−0.5	mA
		Total of all pins		−2	mA
	I_{OH4}	Per pin	P121, P122	−1	mA
		Total of all pins		−4	mA
Output current, low	I_{OL1}	Per pin	P31 to P34	30	mA
		Total of all pins		55	mA
	I_{OL2}	Per pin	P30	30	mA
		Total of all pins		30	mA
	I_{OL3}	Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
	I_{OH4}	Per pin	P121, P122	4	mA
		Total of all pins		10	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

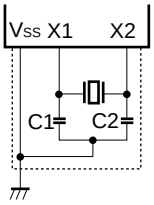
Cautions 1. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

2. The value of the current that can be run per pin must satisfy the value of the current per pin and the total value of the currents of all pins.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

X1 Oscillator Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator, crystal resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		10.0	MHz

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Internal High-speed Oscillator Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Parameter	Conditions		MIN.	TYP.	MAX.	Unit
Internal high-speed oscillator	Oscillation frequency (f_{IH} = 4 MHz) Note	RSTS = 1	T_A = –20 to +70°C	3.92	4	4.08	MHz
			T_A = –40 to +85°C	3.88	4	4.12	MHz

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Internal Low-speed Oscillator Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Resonator	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Internal low-speed oscillator	Oscillation frequency (f_{IL})	CREG = 2.5 V mode	216	240	264	kHz
		CREG = 1.9 V mode	192	240	264	kHz

DC Characteristics (1/5)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P31 to P34	4.0 V ≤ V_{DD} ≤ 5.5 V			–3.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–2.5	mA
		Total of P31 to P34[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			–6.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–4.5	mA
	I_{OH2}	Per pin for P30	4.0 V ≤ V_{DD} ≤ 5.5 V			–3.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–2.5	mA
	I_{OH3}	Per pin for P20 to P27	AV_{REF} = V_{DD}			–100	µA
		Per pin for P121, P122				–100	µA
Output current, low[Note 2]	I_{OL1}	Per pin for P31 to P34	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			5.0	mA
		Total of P31 to P34[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			15.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			10.0	mA
	I_{OH2}	Per pin for P30	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			5.0	mA
	I_{OH3}	Per pin for P122	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5	mA
			2.7 V ≤ V_{DD} < 4.0 V			5.0	mA
	I_{OL4}	Per pin for P20 to P27	AV_{REF} = V_{DD}			400	µA
		Per pin for P121				400	µA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from V_{DD} to an output pin.

2. Value of current at which the device operation is guaranteed even if the current flows from an output pin to GND.

3. Specification under conditions where the duty factor is 70% (time for which current is output is 0.7 × t and time for which current is not output is 0.3 × t, where t is a specific time). The total output current of the pins at a duty factor of other than 70% can be calculated by the following expression.

- Where the duty factor of I_{OH} is n%: Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where the duty factor is 50%, I_{OH} = –20.0 mA

Total output current of pins = (–20.0 × 0.7)/(50 × 0.01) = –28.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (2/5)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P122 Note, P31		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P20 to P27	AV_{REF} = V_{DD}	0.7AV_{REF}		AV_{REF}	V
	V_{IH3}	P121, P125		0.7V_{DD}		V_{DD}	V
	V_{IH4}	P30, P32 to P34, $\overline{\text{RESET}}$, EXCLK		0.8V_{DD}		V_{DD}	V
	V_{IH5}	X1, X2		V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P122 Note, P31		0		0.3V_{DD}	V
	V_{IL2}	P20 to P27	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
	V_{IL3}	P121, P125		0		0.3V_{DD}	V
	V_{IL4}	P30, P32 to P34, $\overline{\text{RESET}}$, EXCLK		0		0.2V_{DD}	V
	V_{IL5}	X1, X2		0		0.1	V
Output voltage, high	V_{OH1}	P30 to P34	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	V_{DD} – 0.7			V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OH1} = –2.5 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P27	AV_{REF} = V_{DD}, I_{OH2} = –100 µA	V_{DD} – 0.5			V
		P121, P122	I_{OH2} = –100 µA	V_{DD} – 0.5			V
Output voltage, low	V_{OH1}	P30 to P34, P122	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.8	V
			2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 5.0 mA			0.7	V
	V_{OH2}	P20 to P27	AV_{REF} = V_{DD}, I_{OL2} = 400 µA			0.4	V
		P121	I_{OL2} = 400 µA			0.4	V

Note V_{IH} and V_{IL} of P122/EXCLK differ between the input port mode and external clock mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (3/5)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P30 to P34, P125/$\overline{\text{RESET}}$	$V_I = V_{DD}$				3	µA
	I_{LIH2}	P20 to P27	$V_I = AV_{REF} = V_{DD}$				3	µA
	I_{LIH3}	P121, P122	$V_I = V_{DD}$	I/O port mode			3	µA
		X1, X2		OSC mode			20	µA
Input leakage current, low	I_{LIL1}	P30 to P34, P125/$\overline{\text{RESET}}$	$V_I = V_{SS}$				–3	µA
	I_{LIL2}	P20 to P27	$V_I = V_{SS}$, $AV_{REF} = V_{DD}$				–3	µA
	I_{LIL3}	P121, P122	$V_I = V_{SS}$	I/O port mode			–3	µA
		X1, X2		OSC mode			–20	µA
Pull-up resistor	R_{PLU1}	P30 to P34	$V_I = V_{SS}$		10	20	100	kΩ
	R_{PLU2}	P125/$\overline{\text{RESET}}$			75	150	300	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (4/5)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current[Note]	I_{DD1}	Operating mode	f_{XH} = 10 MHz, RMC = 00H	Square wave input		1.1	2.7	mA
				Resonator connection		1.3	3.2	mA
			f_{XH} = 5 MHz, RMC = 00H	Square wave input		0.63	1.6	mA
				Resonator connection		0.8	2.0	mA
			f_{IH} = 4 MHz, RMC = 59H	CPU operation only		0.37	0.74	mA
				CPU and peripheral operation		0.42	0.84	mA
			f_{IH} = 4 MHz, f_{CPU} = 1 MHz V_{DD} = 3.0 V, RMC = 56H	CPU operation only		0.14	0.25	mA
				CPU and peripheral operation		0.18	0.36	mA
	I_{DD2}	HALT mode	f_{XH} = 10 MHz, RMC = 00H	Square wave input		0.13	1.3	mA
				Resonator connection		0.36	2.4	mA
			f_{XH} = 5 MHz, RMC = 00H	Square wave input		0.09	0.65	mA
				Resonator connection		0.27	1.1	mA
			f_{IH} = 4 MHz, RMC = 59H			0.12	0.5	mA
	I_{DD3}	STOP mode	V_{DD} = 5.0 V, CREG+POC only	RMC = 00H		1.2	10	µA
				RMC = 56H/59H		2	10	µA

Note Total current flowing into the internal power supply (V_{DD}, AV_{REF}), including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. However, the current flowing into the pull-up resistors, the pull-down resistors and the output current of the port are not included. Below the TYP. column are the values when V_{DD} = 3.0 V and the CPU is operating. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the ADC, WWDT, LVI, AMP, and CMP.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (5/5)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{REF} ≤ V_{DD}, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Watchdog timer operating current[Note 1]	I_{WDT}	V_{DD} = 5.0 V	In 240 kHz internal low-speed oscillation clock operation		5	10	µA
LVI operating current[Note 2]	I_{LVI}				9	18	µA
A/D converter operating current[Note 3]	I_{ADC}				0.86	1.9	mA
Operational amplifier operating current[Note 3]	I_{AMP}	With 1 operational amplifier operating	AV_{REF} = V_{DD} = 5.0 V		250	380	µA
			AV_{REF} = V_{DD} = 3.0 V		230	321	µA
Comparator operating current[Note 3]	I_{CMP}	AV_{REF} = V_{DD} = 5.0 V			80	240	µA
		AV_{REF} = V_{DD} = 3.0 V			70	200	µA

Notes 1. Current flowing only to the watchdog timer (including the operating current of the 240 kHz internal oscillator). The current value of the µPD79F7023, 79F7024 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

2. Current flowing only to the LVI circuit. The current value of the µPD79F7023, 79F7024 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVI circuit operates.

3. Current flowing only to the A/D converter (AV_{REF}).

AC Characteristics

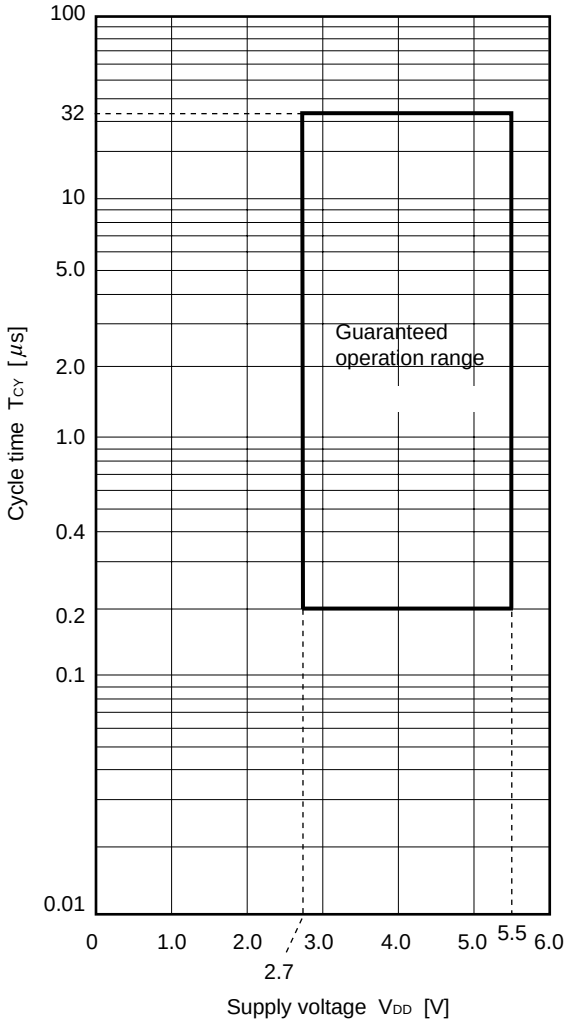
(1) Basic operation

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

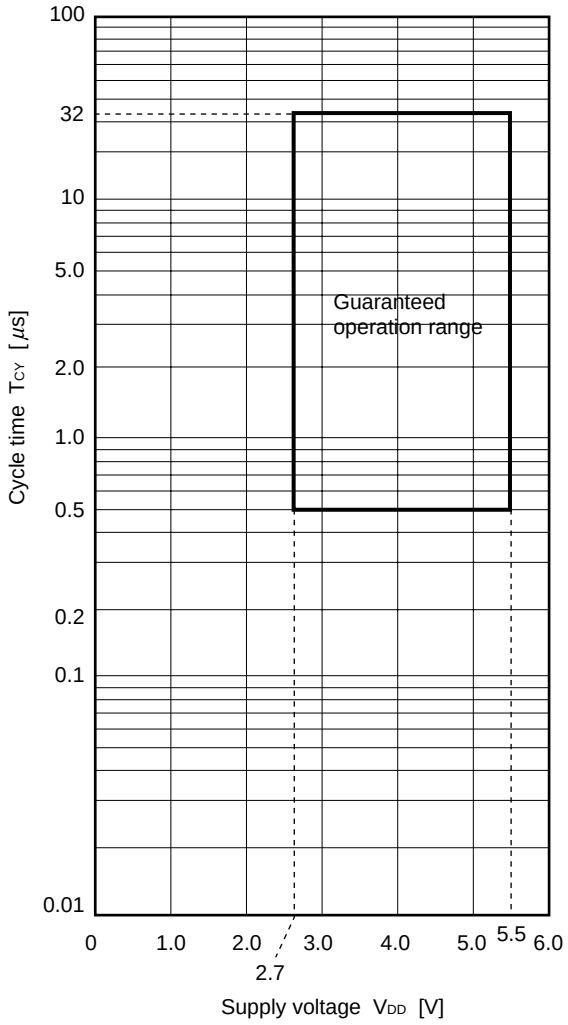
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{XP}) operation	CREG = 2.5 V mode	0.2		32	µs
			CREG = 1.9 V mode	0.5		32	µs
Peripheral hardware clock frequency	f_{PRS}	$f_{PRS} = f_{XP}$				10	MHz
		$f_{PRS} = f_{IH}$		3.8		4.2	MHz
External main system clock frequency	f_{EXCLK}	2.7 V ≤ V_{DD} ≤ 5.5 V		1.0		10.0	MHz
External main system clock input high-level width, low-level width	t_{EXCLKH}, t_{EXCLKL}			$(1/f_{EXCLK} \times 1/2) - 1$			ns
TI000, TI010 input high-level width, low-level width	t_{TIH0}, t_{TIL0}	2.7 V ≤ V_{DD} < 4.0 V		$2/f_{sam}+0.2$ Note			µs
TI51 input frequency	f_{TI5}	2.7 V ≤ V_{DD} ≤ 5.5 V				10.0	MHz
TI51 input high-level width, low-level width	t_{TIH5}	2.7 V ≤ V_{DD} ≤ 5.5 V		50			ns
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}			1			µs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			µs

Note Selection of f_{sam} = f_{PRS}, $f_{PRS}/4$, $f_{PRS}/256$ is possible using bits 0 and 1 (PRM000, PRM001) of prescaler mode register 00 (PRM00). Note that when selecting the TI000 valid edge as the count clock, f_{sam} = f_{PRS}.

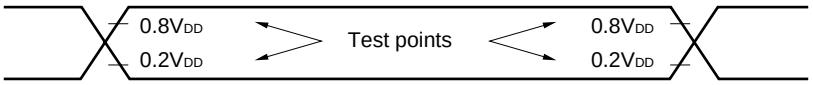
T_{CY} vs. V_{DD} (Main System Clock Operation, CREG = 2.5 V mode)



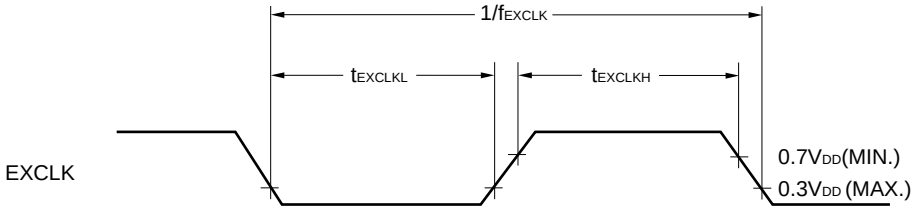
T_{CY} vs. V_{DD} (Main System Clock Operation, CREG = 1.9 V mode)



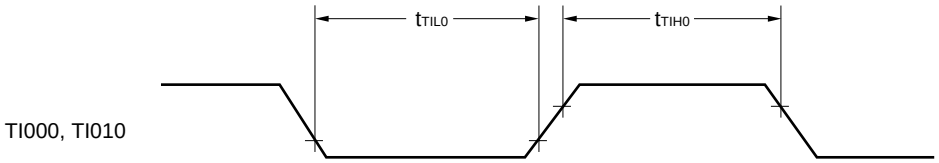
AC Timing Test Points

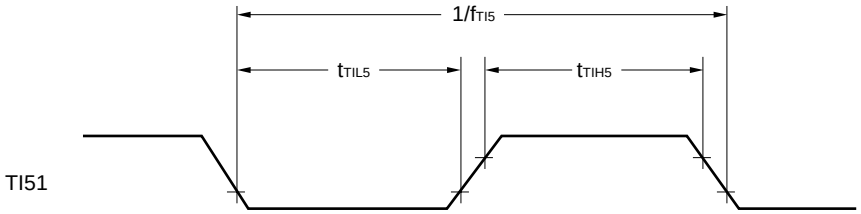


External Main System Clock Timing

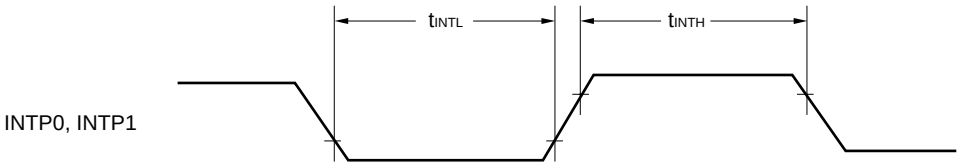


TI Timing

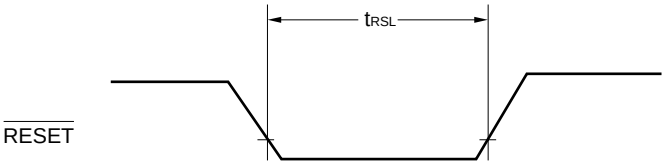




Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



(2) Serial interface

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

(a) UART0 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					312.5	kbps

(b) OCD (UART0)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate			f_{CLK}/32		f_{CLK}/8	bps
		In OCD mode (f_{CLK} = 4 M, V_{DD} ≥ 2.7 V, C_b = 50 pF)	125/250/500			kbps
		In Writer mode (f_{CLK} = 4 M, V_{DD} ≥ 2.7 V, C_b = 50 pF)	125/250/500			kbps
X2/output frequency	f_{OCDB}	V_{DD} ≥ 2.7 V			10	MHz

Analog Characteristics

(1) A/D Converter

(T_A = –40 to +85°C, 2.7 V ≤ AV_{REF} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				8	bit
Overall error[Notes 1, 2]	A_{INL}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.6	%FSR
		2.7 V ≤ AV_{REF} ≤ 5.5 V			±0.8	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	6.1		36.7	µs
		2.7 V ≤ AV_{REF} ≤ 5.5 V	6.1		36.7	µs
Zero-scale error[Notes 1, 2]	E_{ZS}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.6	%FSR
		2.7 V ≤ AV_{REF} ≤ 5.5 V			±0.8	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.6	%FSR
		2.7 V ≤ AV_{REF} ≤ 5.5 V			±0.8	%FSR
Analog input voltage	V_{AIN}		V_{SS}		AV_{REF}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(2) Operational amplifier 0, 1

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ AV_{REF} ≤ 5.5 V, V_{SS} = 0 V, Output load: R_L = 47 kΩ, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage [Note 1]	V_{IOP0}	V_{BIAS} = 1/2 V_{DD}, AV_{REF} = 3.0 V			±3	mV
Power supply voltage rejection ratio	$PSRR_{OP0}$	AV_{REF} = 3.0 V		70		dB
Output voltage, high	V_{OHOP0}	AV_{REF} = 3.0 V, I_{OH} = –500 µA	AV_{REF}–0.2			V
Output voltage, low	V_{OLOP0}	AV_{REF} = 3.0 V, I_{OL} = 500 µA			0.1	V
Common-mode input voltage	V_{ICMOP0}	AV_{REF} = 3.0 V	0		AV_{REF}–0.6	V
Slew rate	SR_{OP0}	AV_{REF} = 3.0 V		1.8		V/µs
		AV_{REF} = 5.0 V		2.0		V/µs
Input noise spectral density (Inoise)		AV_{REF} = 3.0 V, V_{IN} = 0.1 V, f = 1 kHz		73		nV / √Hz
		AV_{REF} = 3.0 V, V_{IN} = AV_{REF}/2 V, f = 1 kHz		60		
		AV_{REF} = 3.0 V, V_{IN} = AV_{REF} –0.6 V, f = 1 kHz		55		
Phase margin		AV_{REF} = 3.0 V		40		deg
Large-amplitude voltage gain	AV_{OP0}	AV_{REF} = 3.0 V		100		dB
Gain-bandwidth product	GBW_{OP0}	AV_{REF} = 5.0 V/3.0 V		3.0		MHz
Operation stabilization wait time [Note 2]	t_{OP0}	AV_{REF} = 3.0 V		10		µs

Notes 1. Data based on characterization results, not tested in production.

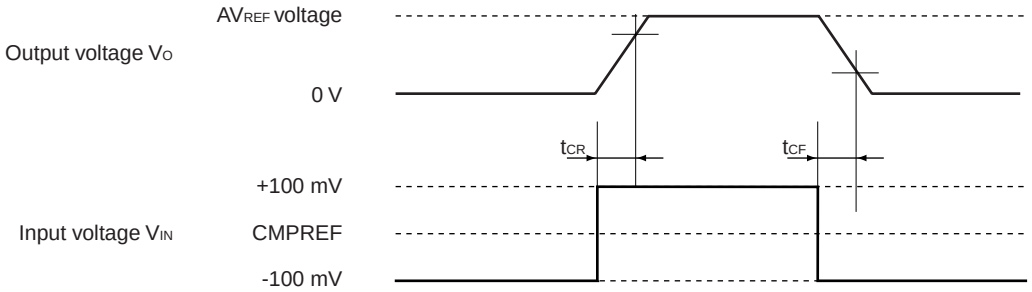
2. Time required until a state is entered where the DC and AC specifications of the operational amplifier 0 are satisfied after the operational amplifier operation has been enabled (OPAMP0E/OPAMP1E = 1).

(3) CMP

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = V_{SS} = 0 V, Output load: R_L = 47 kΩ, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IOCMP}			±5	±40	mV
Input voltage range	V_{ICMP}	CMPIN	0		AV_{REF}	V
		CMPCOM	0.045		$0.9AV_{REF}$	V
Response time	t_{CR}, t_{CF}	Input amplitude ±100 mV		70	150	ns
Operation stabilization wait time[Note]	t_{CMP}				1	µs
Comparator input high-level width, low-level width	t_{CMPL}		125			ns

Note Time required until a state is entered where the DC and AC specifications of the comparator are satisfied after the comparator operation has been enabled (CMP0EN bit = 1).

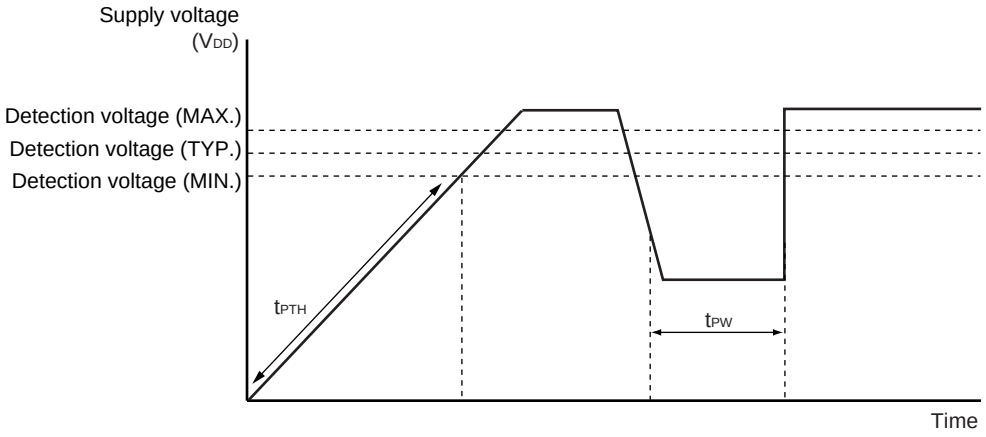


(4) POC

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC0}		1.44	1.59	1.74	V
Power supply voltage rise inclination	t_{PTH}	Change inclination of V_{DD}: 0 V → V_{POC0}	0.5			V/ms
Minimum pulse width	t_{PW}	When the voltage drops	200			µs

POC Circuit Timing



(5) Supply Voltage Rise Time

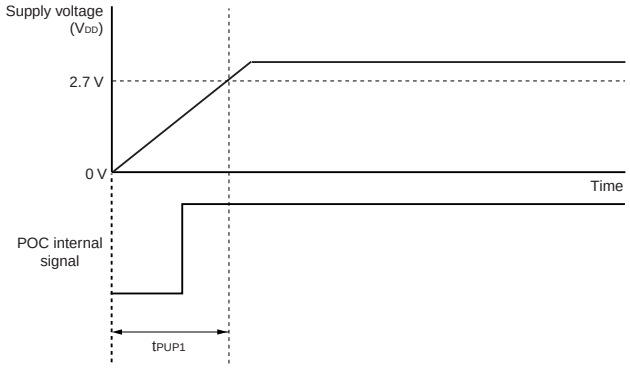
(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 2.7 V (V_{DD} (MIN.))[Note] (V_{DD}: 0 V → 2.7 V)	t_{PUP1}	LVI default start function stopped is set (LVISTART (Option Byte) = 0), when $\overline{\text{RESET}}$ input is not used			5.4	ms
Maximum time to rise to 2.7 V (V_{DD} (MIN.))[Note] (releasing $\overline{\text{RESET}}$ input → V_{DD}: 2.7 V)	t_{PUP2}	LVI default start function stopped is set (LVISTART (Option Byte) = 0), when $\overline{\text{RESET}}$ input is used			1.9	ms

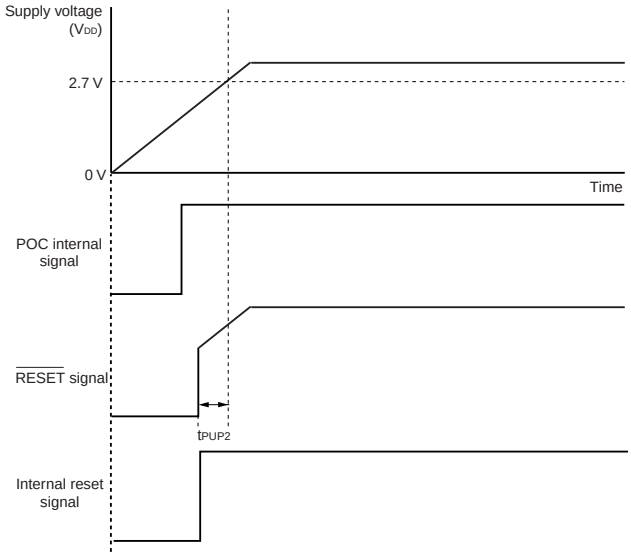
Note Make sure to raise the power supply in a shorter time than this.

Supply Voltage Rise Time Timing

- When $\overline{\text{RESET}}$ pin input is not used



- When $\overline{\text{RESET}}$ pin input is used (when external reset is released by the $\overline{\text{RESET}}$ pin, after POC has been released)



(6) Secondary Supply Voltage Output

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CREG output voltage	V_{REGC}	2.7 V ≤ V_{DD} ≤ 5.5 V	NV mode	2.3	2.5	2.7	V
			LV mode	1.7	1.9	2.1	V

(7) LVI

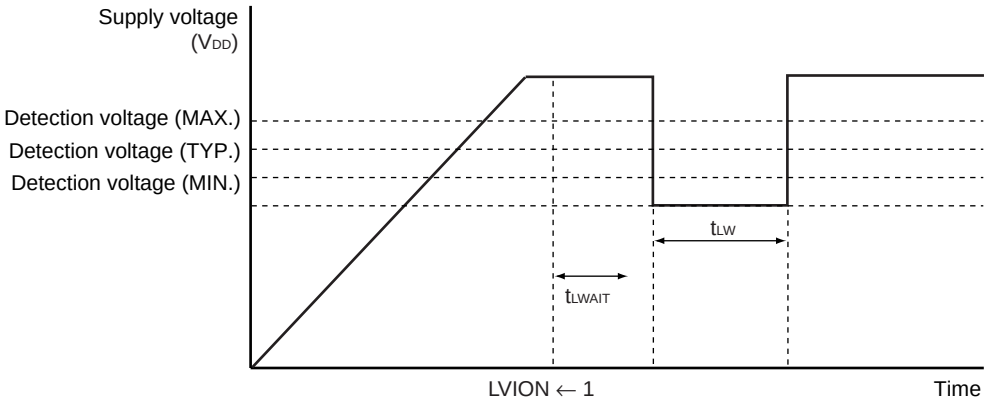
(T_A = –40 to +85°C, $V_{PDR} \le V_{DD} \le$ 5.5 V, V_{SS} =0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}			4.24±0.1		V
		V_{LVI1}			4.09±0.1		V
		V_{LVI2}			3.93±0.1		V
		V_{LVI3}			3.78±0.1		V
		V_{LVI4}			3.62±0.1		V
		V_{LVI5}			3.47±0.1		V
		V_{LVI6}			3.32±0.1		V
		V_{LVI7}			3.16±0.1		V
		V_{LVI8}			3.01±0.1		V
		V_{LVI9}			2.85±0.1		V
		V_{LVI10}			2.70±0.1		V
	Supply voltage when power supply voltage is turned on	V_{DDLVI}	When LVI default start function enabled is set (LVISTART = 1)	2.5	2.7	2.9	V
Minimum pulse width		t_{LW}		200			μs
Operation stabilization wait time[Note]		t_{LWAIT}				10	μs

Note Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 10

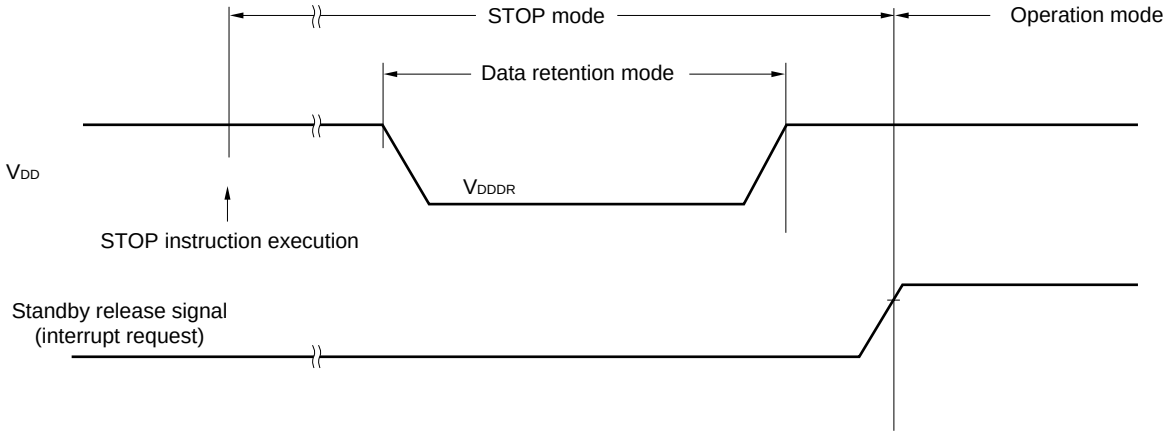
LVI Circuit Timing



Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44[Note]		5.5	V

Note The value depends on the POC detection voltage. When the voltage drops, the data is retained until a POC reset is effected, but data is not retained when a POC reset is effected.



Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

• Basic characteristics

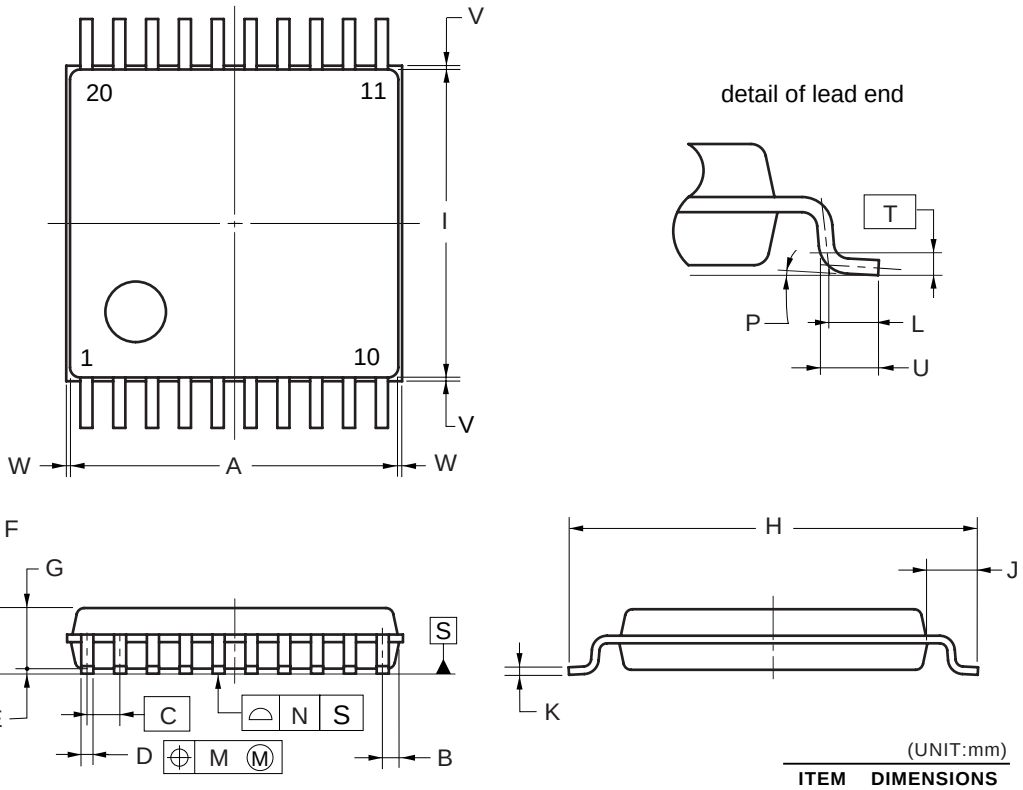
Parameter		Symbol	Conditions			MIN.	TYP.	MAX.	Unit
V_{DD} supply current		I_{DD}					4.5	11.0	mA
Erase time	per chip	t_{eraca}					20	200	ms
	per sector	t_{erasa}					20	200	ms
Write time (in unit of 8 bit)		t_{wrwa}					10	100	µs
Number of rewrites per chip[Note]		C_{erwr}	1 erase + 1 write after erase = 1 rewrite	When a flash memory programmer is used, and the self-programming libraries provided by Renesas Electronics are used	Retention: 15 years	1000			Times
Operating temperature			When a flash memory programmer is used: 10 to 40 °C, during self-programming: –40 to +85 °C						
Operating voltage range			In normal power mode (RMC = other than 56/59H)	When a flash memory programmer is used		2.7 to 5.5 V@8 MHz (MAX.)			
				During self-programming					

Note When a product is first written after shipment, “erase → write” and “write only” are both taken as one rewrite.

CHAPTER 25 PACKAGE DRAWINGS

• μPD79F7023MC-CAA-AX, 79F7024MC-CAA-AX

20-PIN PLASTIC SSOP (7.62 mm (300))



(UNIT:mm)

ITEM	DIMENSIONS
A	6.50±0.10
B	0.325
C	0.65 (T.P.)
D	$0.22^{+0.10}_{-0.05}$
E	0.10±0.05
F	1.30±0.10
G	1.20
H	8.10±0.20
I	6.10±0.10
J	1.00±0.20
K	$0.15^{+0.05}_{-0.01}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25(T.P)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

P20MC-65-CAA

NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

CHAPTER 26 CAUTIONS FOR WAIT

26.1 Cautions for Wait

This product has two internal system buses.

One is a CPU bus and the other is a peripheral bus that interfaces with the low-speed peripheral hardware.

Because the clock of the CPU bus and the clock of the peripheral bus are asynchronous, unexpected illegal data may be passed if an access to the CPU conflicts with an access to the peripheral hardware.

When accessing the peripheral hardware that may cause a conflict, therefore, the CPU repeatedly executes processing, until the correct data is passed.

As a result, the CPU does not start the next instruction processing but waits. If this happens, the number of execution clocks of an instruction increases by the number of wait clocks (for the number of wait clocks, refer to **Table 26-1**). This must be noted when real-time processing is performed.

26.2 Peripheral Hardware That Generates Wait

Table 26-1 lists the registers that issue a wait request when accessed by the CPU, and the number of CPU wait clocks.

Table 26-1. Registers That Generate Wait and Number of CPU Wait Clocks

Peripheral Hardware	Register	Access	Number of Wait Clocks
Serial interface UART0	ASIS0	Read	1 clock (fixed)
A/D converter	ADM0	Write	1 to 5 clocks (when $f_{AD} = f_{PRS}/2$ is selected) 1 to 7 clocks (when $f_{AD} = f_{PRS}/3$ is selected) 1 to 9 clocks (when $f_{AD} = f_{PRS}/4$ is selected) 2 to 13 clocks (when $f_{AD} = f_{PRS}/6$ is selected) 2 to 17 clocks (when $f_{AD} = f_{PRS}/8$ is selected) 2 to 25 clocks (when $f_{AD} = f_{PRS}/12$ is selected)
	ADS	Write	
	ADPC	Write	
	ADCRH	Read	
	The above number of clocks is when the same source clock is selected for f_{CPU} and f_{PRS}. The number of wait clocks can be calculated by the following expression and under the following conditions. <Calculating number of wait clocks> • Number of wait clocks = $\frac{2 f_{CPU}}{f_{AD}} + 1$ * Fraction is truncated if the number of wait clocks ≤ 0.5 and rounded up if the number of wait clocks > 0.5. f_{AD}: A/D conversion clock frequency (f_{PRS} to $f_{PRS}/12$) f_{CPU}: CPU clock frequency f_{PRS}: Peripheral hardware clock frequency f_{XP}: Main system clock frequency <Conditions for maximum/minimum number of wait clocks> • Maximum number of times: Maximum speed of CPU (f_{XP}), lowest speed of A/D conversion clock ($f_{PRS}/12$) • Minimum number of times: Minimum speed of CPU (f_{SUB}), highest speed of A/D conversion clock (f_{PRS})		

Caution When the peripheral hardware clock (f_{PRS}) is stopped, do not access the registers listed above using an access method in which a wait request is issued.

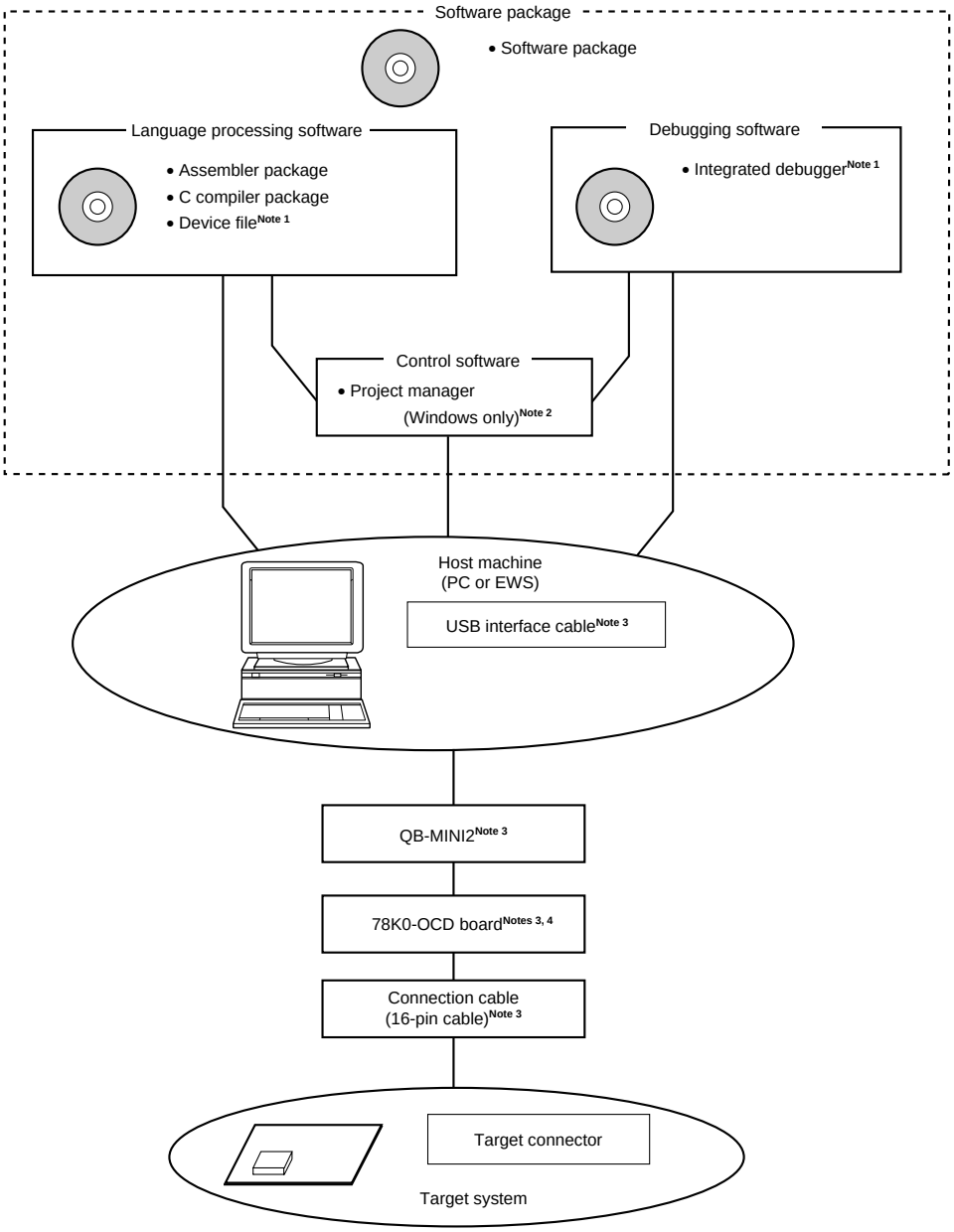
Remark The clock is the CPU clock (f_{CPU}).

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for the development of systems that employ the µPD79F7023, 79F7024 microcontrollers.

Figure A-1 shows the development tool configuration.

Figure A-1. Development Tool Configuration



Notes 1. Download the device file for µPD79F7023, 79F7024 microcontrollers (Under development) and the integrated debugger ID78K0-QB from the download site for development tools (http://www2.renesas.com/micro/en/ods/index.html).

2. The project manager PM+ is included in the assembler package.
The PM+ is only used for Windows.

3. On-chip debug emulator QB-MINI2 is supplied with USB interface cable, connection cables (10-pin cable and 16-pin cable), and 78K0-OCD board. In addition, download the software for operating the QB-MINI2 from the download site for development tools (http://www2.renesas.com/micro/en/ods/index.html).

4. This is used only when using QB-MINI2 as an on-chip debug emulator.

A.1 Software Package

SP78K0 78K0 microcontroller software package	Development tools (software) common to the 78K0 microcontrollers are combined in this package.

A.2 Language Processing Software

RA78K0[Note] Assembler package	This assembler converts programs written in mnemonics into object codes executable with a microcontroller. This assembler is also provided with functions capable of automatically creating symbol tables and branch instruction optimization. This assembler should be used in combination with a device file (Under development). **<Precaution when using RA78K0 in PC environment>** This assembler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (PM+) on Windows. PM+ is included in assembler package.
CC78K0[Note] C compiler package	This compiler converts programs written in C language into object codes executable with a microcontroller. This compiler should be used in combination with an assembler package and device file (Under development). **<Precaution when using CC78K0 in PC environment>** This C compiler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (PM+) on Windows. PM+ is included in assembler package.
Device file (Under development)	This file contains information peculiar to the device. This device file should be used in combination with a tool (RA78K0, CC78K0, and ID78K0-QB). The corresponding OS and host machine differ depending on the tool to be used.

Note If the versions of RA78K0 and CC78K0 are Ver.4.00 or later, different versions of RA78K0 and CC78K0 can be installed on the same machine.

A.3 Flash Memory Programming Tools

A.3.1 When using flash memory programmer PG-FP5 and FL-PR5

PG-FP5, FL-PR5 Flash memory programmer	Flash memory programmer dedicated to microcontrollers with on-chip flash memory.
FA-78F0567MC-CAA-RX Flash memory programming adapter	Flash memory programming adapter used connected to the flash memory programmer for use.

Remarks 1. FL-PR5 and FA-78F0567MC-CAA-RX are products of Naito Densei Machida Mfg. Co., Ltd.
TEL: +81-42-750-4172 Naito Densei Machida Mfg. Co., Ltd.

2. Use the latest version of the flash memory programming adapter.

A.3.2 When using on-chip debug emulator with programming function QB-MINI2

QB-MINI2 On-chip debug emulator with programming function	This is a flash memory programmer dedicated to microcontrollers with on-chip flash memory. It is available also as on-chip debug emulator which serves to debug hardware and software when developing application systems using the µPD79F7023, 79F7024 microcontrollers. When using this as flash memory programmer, it should be used in combination with a connection cable (16-pin cable) and a USB interface cable that is used to connect the host machine.
Target connector specifications	16-pin general-purpose connector (2.54 mm pitch)

Remark Download the software for operating the QB-MINI2 from the download site for development tools (http://www2.renesas.com/micro/en/ods/index.html).

A.4 Debugging Tools (Hardware)

QB-MINI2 On-chip debug emulator with programming function	This on-chip debug emulator serves to debug hardware and software when developing application systems using the µPD79F7023, 79F7024. It is available also as flash memory programmer dedicated to microcontrollers with on-chip flash memory. When using this as on-chip debug emulator, it should be used in combination with a connection cable (16-pin cable), a USB interface cable that is used to connect the host machine, and the 78K0-OCD board.
Target connector specifications	16-pin general-purpose connector (2.54 mm pitch)

Remark Download the software for operating the QB-MINI2 from the download site for development tools (http://www2.renesas.com/micro/en/ods/index.html).

A.5 Debugging Tools (Software)

ID78K0-QB Integrated debugger	This debugger supports the in-circuit emulators for the 78K0 microcontrollers. The ID78K0-QB is Windows-based software. It has improved C-compatible debugging functions and can display the results of tracing with the source program using an integrating window function that associates the source program, disassemble display, and memory display with the trace result. It should be used in combination with the device file (Under development).

REVISION HISTORY	μPD79F7023, 79F7024 User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.00	Mar 7, 2012	—	First Edition issued.
1.10	Nov 29, 2013	—	Modification of Caution on cover.

μPD79F7023, 79F7024 User's Manual: Hardware

Publication Date: Rev.1.10 Nov 29, 2013

Published by: Renesas Electronics Corporation

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 1.3

µPD79F7023, 79F7024

Renesas Electronics Corporation

R01UH0312EJ0110