QCIOT-CCE4503POCZ

CCE4503 IO-Link Transceiver (QCIOT-5)

The QCIOT-5 IO-Link device transceiver board demonstrates the functionality and performance of the CCE4503. The CCE4503 is an easy-to-use device-side IO-Link compliant transceiver. It combines IO-Link compliant communication capability with advanced protection circuitry and additional features while keeping the application small and simple.

Controlled by a UART interface (TXD, RXD, TXEN), the output drivers can be configured as PNP, NPN or Push-pull. Three LDO options and an automatic wake-up detection simplify the overall system requirements and reduce the need for additional external circuitry. The integrated protection features such as reverse-polarity protection, overcurrent protection, undervoltage detection, and thermal protection ensure robust functionality and communication.

The board provides a standard Pmod™ Type 3A (expanded UART) connection for the onboard device to plug into any required MCU evaluation kit with a matching connector.

The software support included with the Renesas IDE (e2 studio) allows for code generation to connect the device and the MCU so that development time is significantly reduced. With its standard connector and software support, the QCIOT-5 board is ideal for the Renesas Quick-Connect IoT to rapidly create an IoT system.

Features

- IO-Link compliant transceiver
- One IO-Link channel with up to 250mA permanent driving current
- Configurable PNP-, NPN- and Push-pull mode
- Configurable slew rate limitation
- Configurable current limit
- Automatic recovery function
- Wake-up detection
- Three LDO options with up to 20mA
- Reverse-polarity protection
- Overcurrent detection
- Undervoltage detection
- Over-temperature detection
- Small 3 × 3 mm DFN-10 package

Board Contents

- CCE4503 IO-Link device transceiver
- RAA2116054 DC/DC step-down regulator

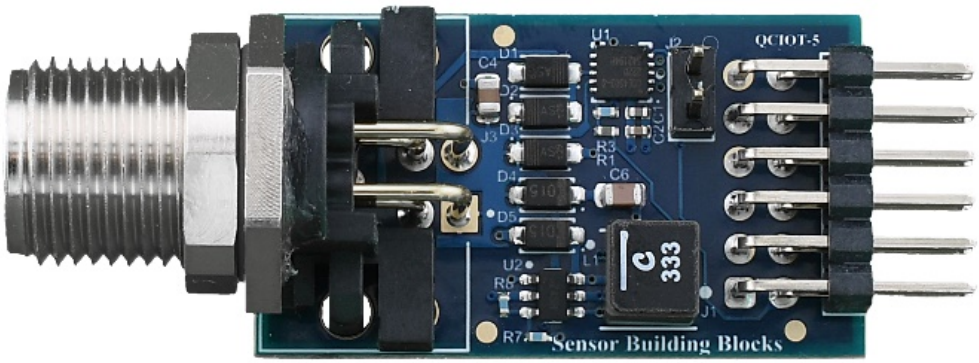

Figure 1. QCIOT-5 IO-Link Device Transceiver Board Image

Contents

Figures

1. Functional Description

The QCIOT-CCE4503POCZ board is used as a quick connect prototyping solution for an IO-Link device interface, enabling fast, simple and cost-effective applications evaluation for an IO-Link device interface. This board can be used with any Renesas evaluation or fast prototyping MCU board.

Figure 2 highlights the main parts of the system.

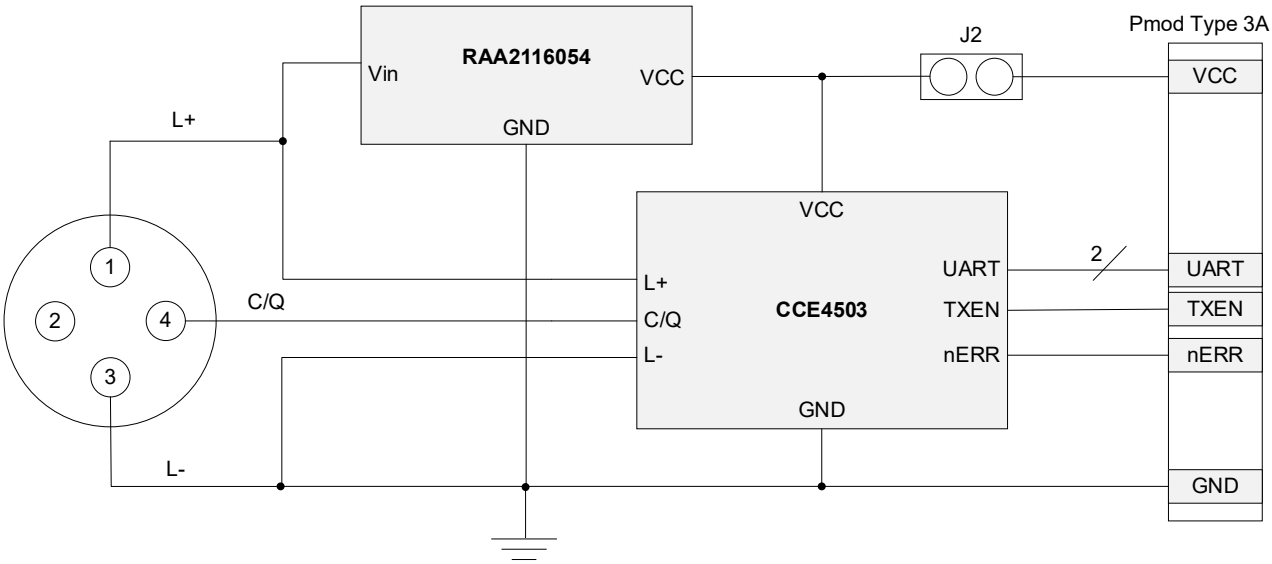

Figure 2. QCIOT-5 IO-Link Device Transceiver Board Block Diagram

The building block of the QCIOT-5 IO-Link board and its functionality are as follows:

- RA2116054 – 60V 0.5A DC/DC step-down regulator with 450kHz switching frequency
- CCE4503 IO-Link device transceiver with cost-optimized feature set

1.1 Operational Characteristics

The QCIOT-5 board can be used as a starting point for IO-Link capable sensors and actuators testing/development in industrial applications.

The board is designed with following characteristics:

- Input voltage: 30V
- 3.3V 500mA for the IO-Link device application

1.1.1 Standalone or IO-Link Bus-Powered Applications

The QCIOT-5 board design allows powering the board directly from the IO-Link master or using an external power supply. For standalone or bus-powered applications, a 2.54mm or 0.1’’ pitch jumper on J2 pin header is required on the top of the board. If an external power supply is used, the J2 header must be left open. See Figure 6 for connection diagram schematics.

1.2 Setup and Configuration

The following hardware and software are required for setup and configuration:

Hardware:

- Renesas evaluation kit EK-RA4M2
- Renesas CCE4503 IO-Link device Pmod board QCIOT-CCE4503POCZ
- Renesas HS4001 temperature and humidity sensor Pmod board US082-HS4001EVZ

- Renesas interposer board US082-INTERPEVZ
- PEPPERL+FUCHS USB IO-Link Master (02-USB 30407 – sold by third party)
- USB micro-B cable (provided with evaluation kit board)
- PC running Windows 10/11 with at least one USB port
- M12-4 or M12-5 IO-Link cable
- USB mini-B cable (needed for PEPPERL+FUCHS master)
- DC Power supply (5V, 1A output)

Software:

- Renesas Flexible Software Package v5.2.0 platform
  - e2 studio 2024-01.1 (24.1.1) or later
  - FSP 5.2.0 or later
  - GCC Arm Embedded 10.3.1 (10 2021.10) or later
- Sample code files (available on the webpage for this device)

1.2.1 Software Installation

Install the FSP v5.2.0 version (supporting the QCIOT-5 board) and the latest version of the e2 studio installer.

1.2.2 Hardware Connections

Refer to Figure 3 and use the following procedures to setup the kit.

1. Connect the QCIOT-CCE4503 Pmod to the PMOD2 connector on the evaluation kit.
   a. Mount the J2 jumper if it is bus-powered. If the USB power is not sufficient to fully power the IO-Link-USB master, use an external power supply.
2. Connect the HS4001 Pmod to PMOD1 through an interposer board.
   a. For kits other than the EK-RA4M2, an I^2C sensor board can be connected directly to the dedicated Type 6A Pmod connector (if a Type 6A Pmod is available). Otherwise, ensure that the kit can use the US082-INTERPEVZ interposer board. Insert the interposer board into the MCU connector before adding any sensor boards.
3. Ensure that pin 12 of the Pmod is 3.3V (this is requested by the US082-HS4001EVZ).
   a. For some evaluation boards, the pin 12 of the Pmod is 3.3V by default, thus, no change is required. Check the user manual before prior to usage.
   b. Only one set of I^2C pull-up resistors should be used on the bus. If multiple Pmod connected boards are used, only one board should have the jumpers present.
   c. If multiple modules use the IRQ# line on the PMOD, only one pull-up jumper should be present.
   d. MCU kits typically do not have pull-up resistors present on the bus lines. Ensure to check if any are present.
4. Connect the IO-Link master with the QCIOT-CCE4503POCZ using a standard M12 4- or 5-pin cable.
5. Connect the evaluation kit with a computer using a USB micro-B cable. This is required for programming the board, debugging or for power if the J2 jumper on CQIOT-CCE4503POCZ is off.
6. Connect the IO-Link master to the USB converter with a computer using USB mini-B cable.
7. The device is now ready to be used in the system. For board testing, see section 4 “Board Testing” of the Quick Start Guide.

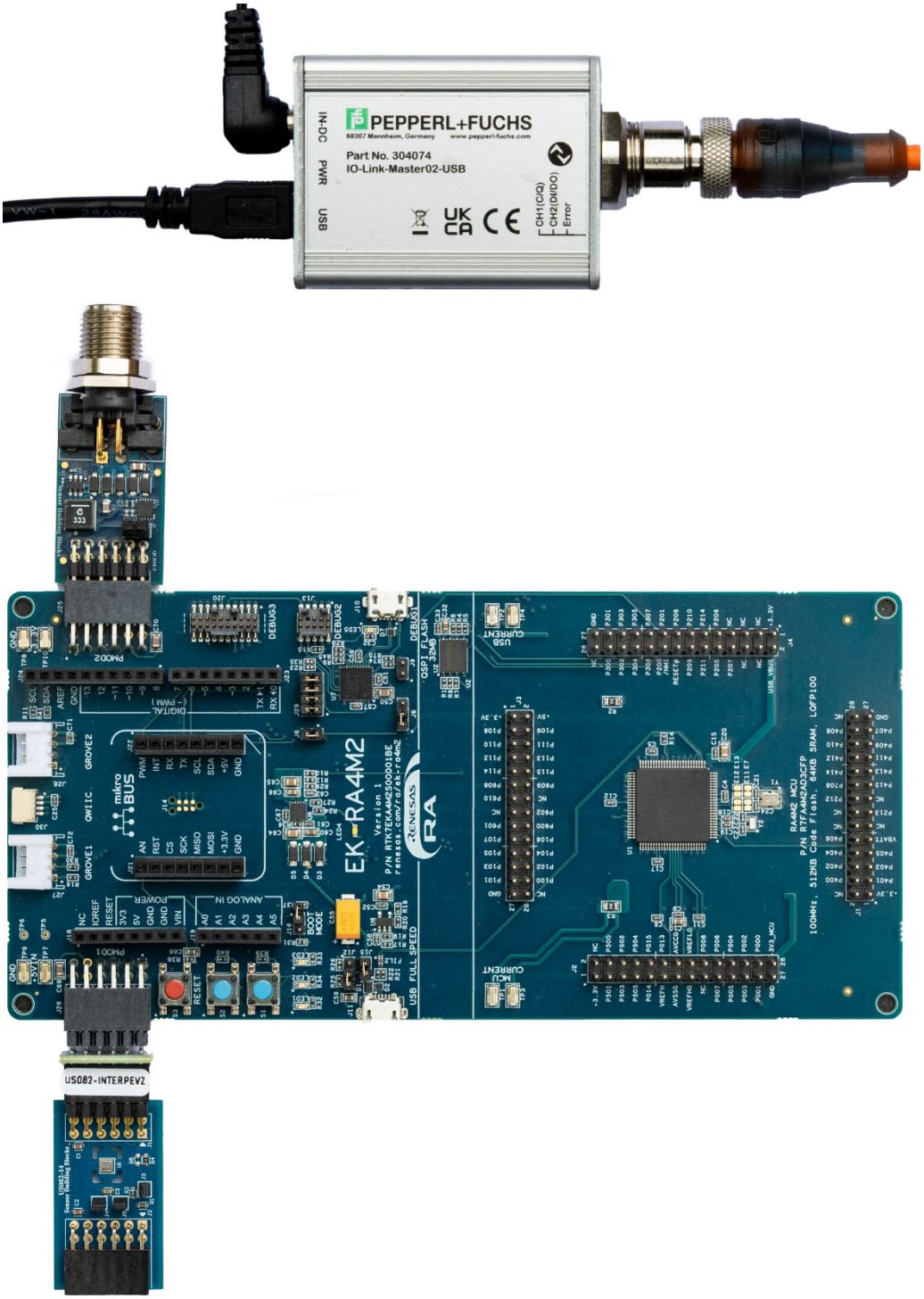

Figure 3. QCIOT-5 IO-Link Device CCE4503 Test Setup

2. Board Design

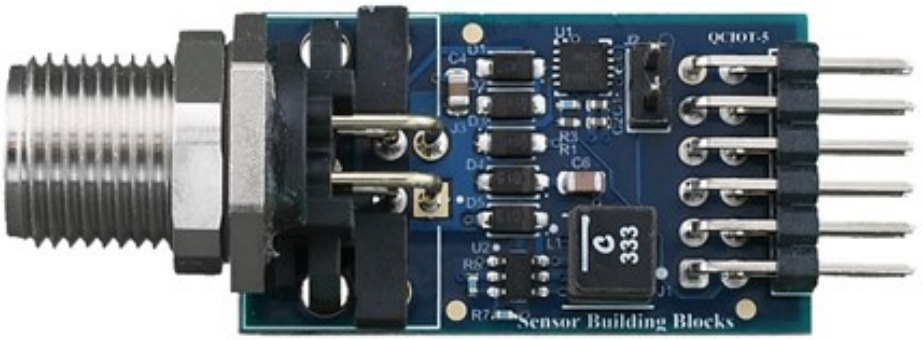

Figure 4. QCIOT-5 IO-Link Device Transceiver Board (Top)

Figure 5. QCIOT-5 IO-Link Device Transceiver Board (Bottom)

2.1 Schematic Diagrams

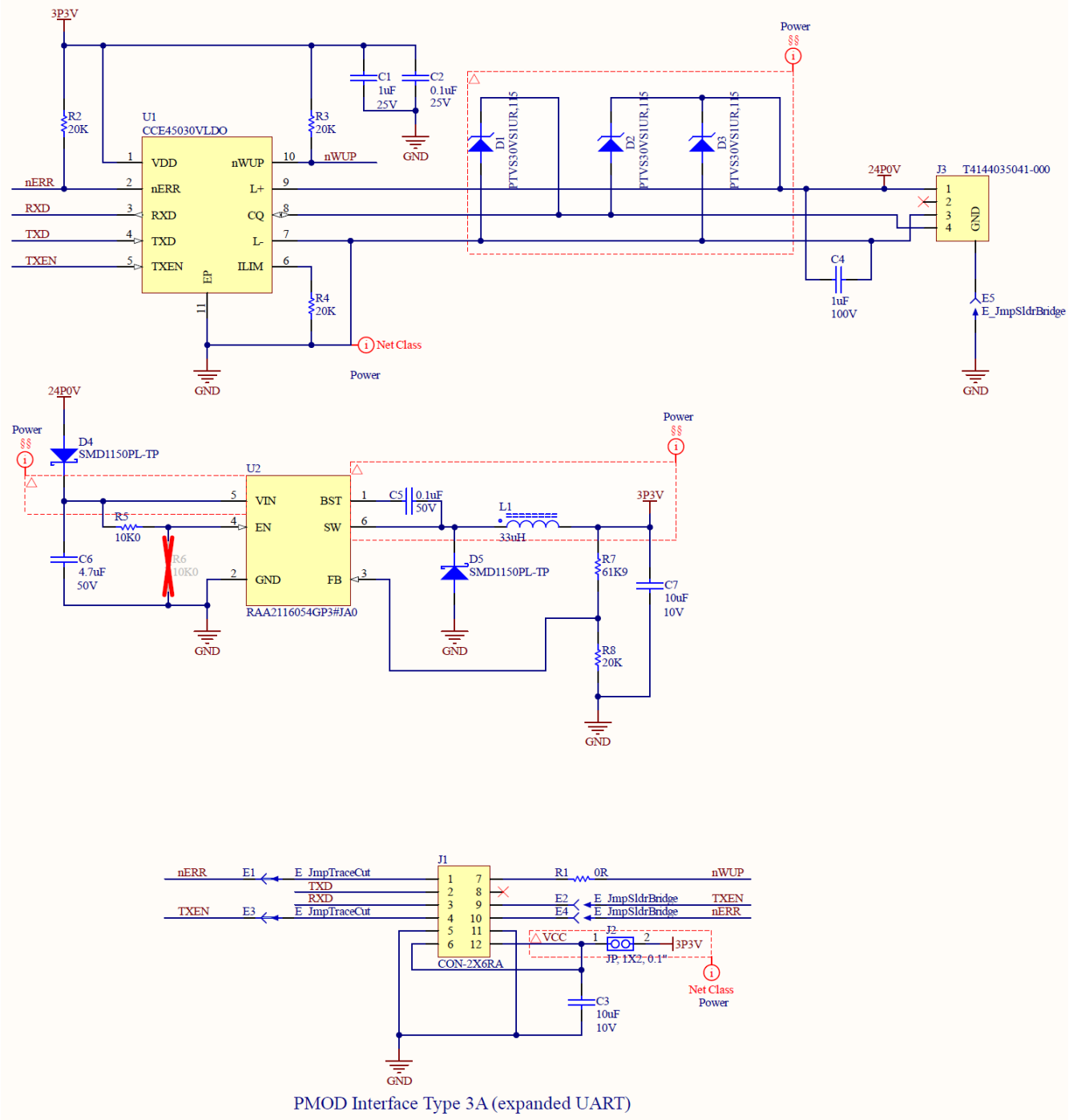

Figure 6. QCIOT-5 IO-Link Device Transceiver Schematics

2.2 Bill of Materials

Quantity	Designator	Description	Manufacturer	Manufacturer Part Number
1	C1	Capacitor, 1µF, 25V, SM	Taiyo Yuden	TMK105BJ105KV-F
1	C2	Capacitor, 0.1µF, 25V, SM	Taiyo Yuden	TMK105B7104KVHF
2	C3, C7	Capacitor, 10µF, 10V, SM	Murata	GRM188R61A106KE69D
1	C4	Capacitor, 1µF, 100V, SM	Kyocera AVX	08051C105K4Z2A
1	C5	Capacitor, 0.1µF, 50V, SM	Yageo	CC0603KRX7R9BB104
1	C6	Capacitor, 4.7µF, 50V, SM	TDK	C2012X7R1H475K125AC
3	D1, D2, D3	Diode, TVS, 30V, Uni-directional, 400W, SM	Nexperia	PTVS30VS1UR,115
2	D4, D5	Diode, 1A, 150V, Schottky, SM	Micro Commercial Co	SMD1150PL-TP
1	FOOT1	Foot, Rubber, Self-adhesive, Black, 6.4mm diameter, 2.1mm tall	Bumper Specialties Inc.	BS25BL07X30RP
1	J1	Connector, 2×6, 0.1", Right Angle, Unshrouded	Würth Elektronik	732-5354-ND
1	J2	Jumper, 1×2, 0.1" Pitch	Sullins	PBC02SAAN
1	J3	Connector, 4 Pin, Circular, M12, Plug, A-Code	TE Connectivity	T4144035041-000
1	L1	Inductor, 33µH, 3.2A, 107mΩ, SM	Coilcraft	XGL5050-333MEC
1	R1	Resistor, 0 ohms, 1/10W, 1%, SM	KOA Speer	RK73Z1ETTP
4	R2, R3, R4, R8	Resistor, 20kΩ, 1/10W, 1%, SM	KOA Speer	RK73H1ETTP2002F
1	R5	Resistor, 10kΩ, 1/10W, 1%, SM	KOA Speer	RK73H1ETTP1002F
1	R7	Resistor, 61.9kΩ, 1/10W, 1%, SM	KOA Speer	RK73H1ETTP6192F
1	U1	Transceiver, IO-Link, No LDO, SM	Renesas	CCE45030VLDO
1	U2	Switching Regulator, Buck, 500mA, 60V Switch	Renesas	RAA2116054GP3#JA0

2.3 Board Layout

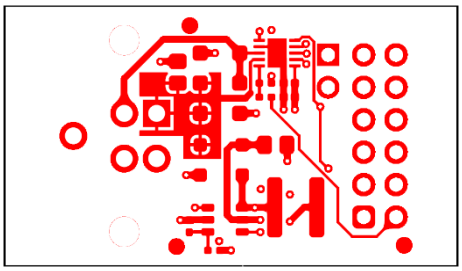

Figure 7. Top Layer

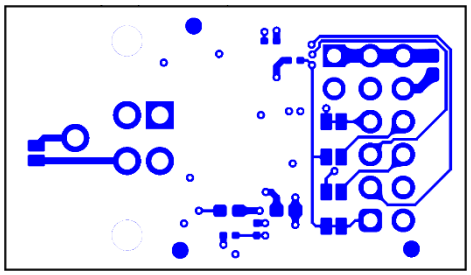

Figure 8. Bottom Layer

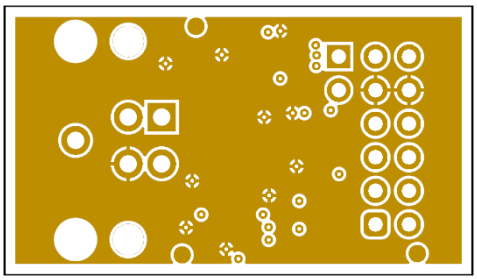

Figure 9. Layer 2 (GND)

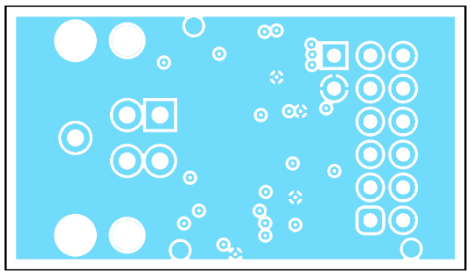

Figure 10. Layer 3 (PWR)

3. Software Design

This section gives a brief overview of the software implementation for the QCIOT-5 IO-Link device board which is based on the Renesas RA Family's Flexible Software Package (FSP) and third-party library for the Cortex M33 core. The following sub-sections describe the project's code structure, the system's software modules, and the main system flow. The application-level code is based on bare metal concept that does not use any RTOS and periodically serves all processes in a main loop.

3.1 Project Code Structure

The Quick Connect IO-Link project is designed to be highly modular in terms of sensors and simple realization. Solutions can be easily configured independently of other modules (if required) or ported to different end-applications.

The project is split into three main parts:

- **Sensor driver** – device driver code for sensor control, data readout and I^2C communications driver
- **IO-Link device driver** – device driver code for CCE4503 and IO-Link device side implementation
- **Application code** – main system code that enables processes requests from IO-Link master and gathers data from the sensors and puts them into predefined structures to be sent when required

Figure 11 shows the e2 studio folder project structure.

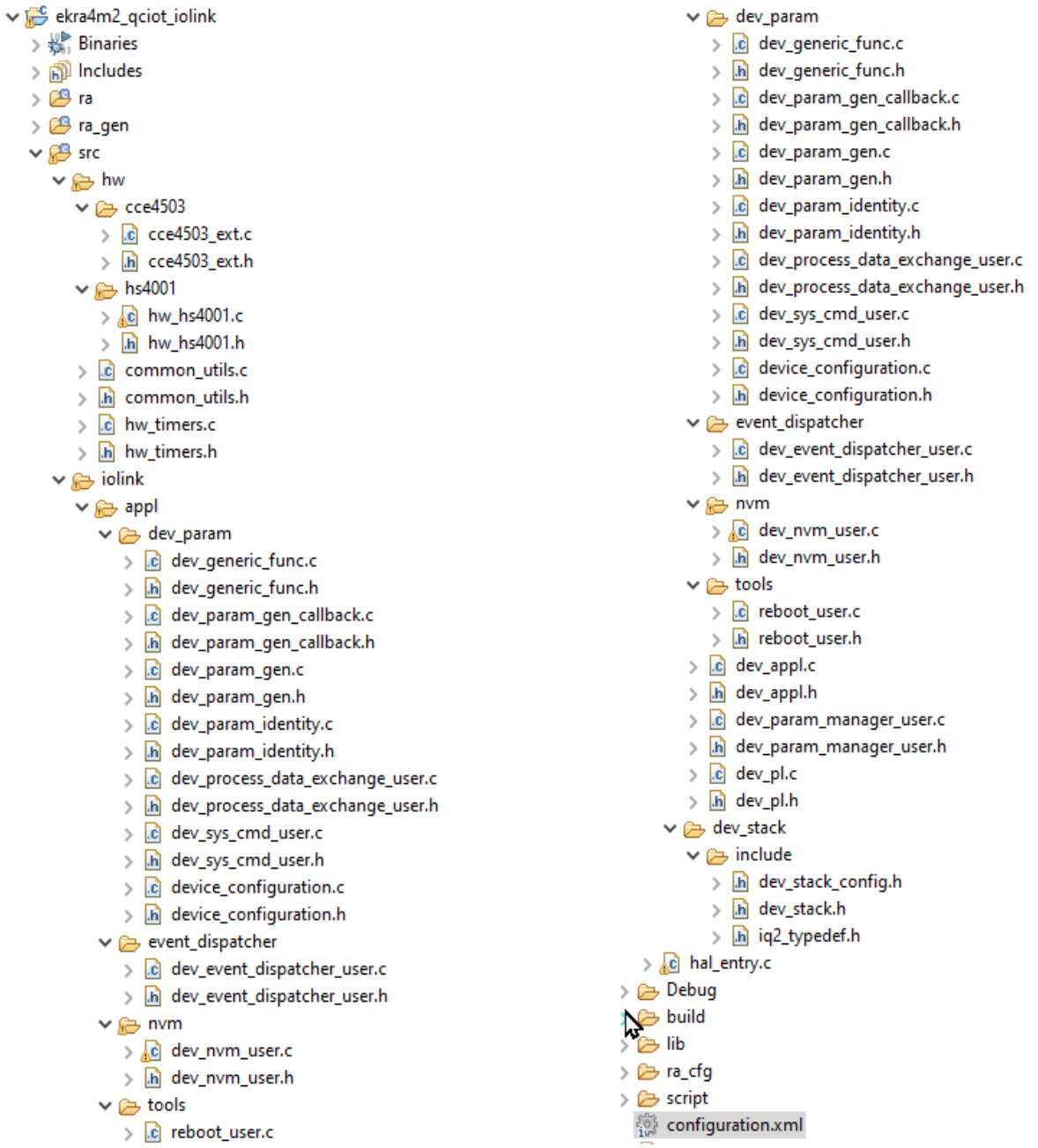

Figure 11. CCE4503-RA4M2 e2Studio Project Folder Structure

e2 studio folder structure:

- **ra** – automatically generated files for FSP drivers and is28022 driver source code and header file
- **ra_gen** – generated files by FSP configuration
- **src** – application code that consists of:
  - **hw** – folder containing low level drivers and control procedures for the hardware used in this project
  - **Iolink** – folder containing procedures and routines for the application layer
  - **lib** – IO-Link device binary library for RA4 microcontroller

Click on **configuration.xml** in the project and open the Stack Tab to see the FSP packages configuration (see Figure 12).

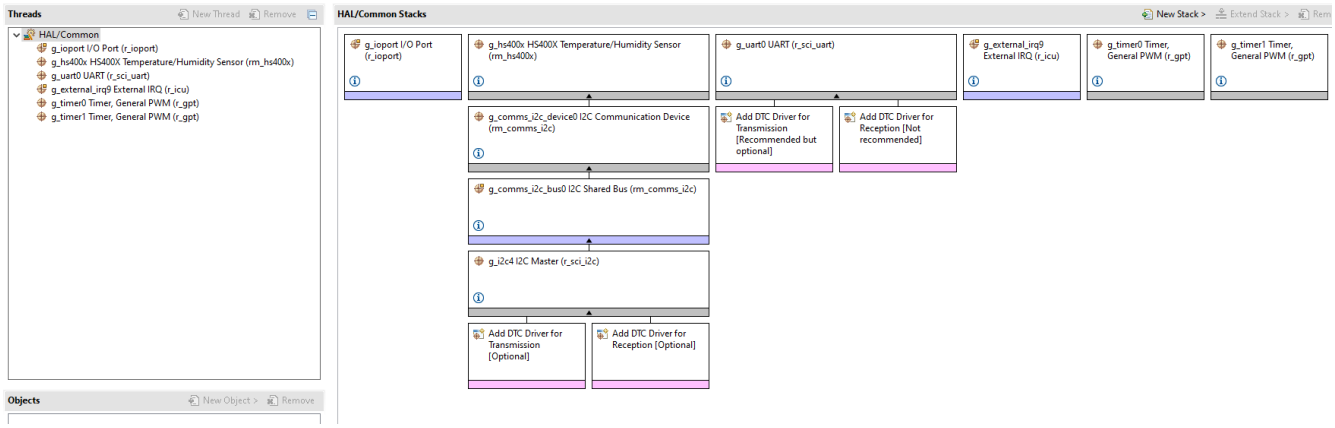

Figure 12. Stack Configuration – Hal/Common

3.2 Application Structure

The application is running bare metal and starts in the **hal_entry()** function. FSP configuration is already setup and shown in Figure 12. The user application starts with initialization and then is split into two parts. The application flow diagram is shown in Figure 13.

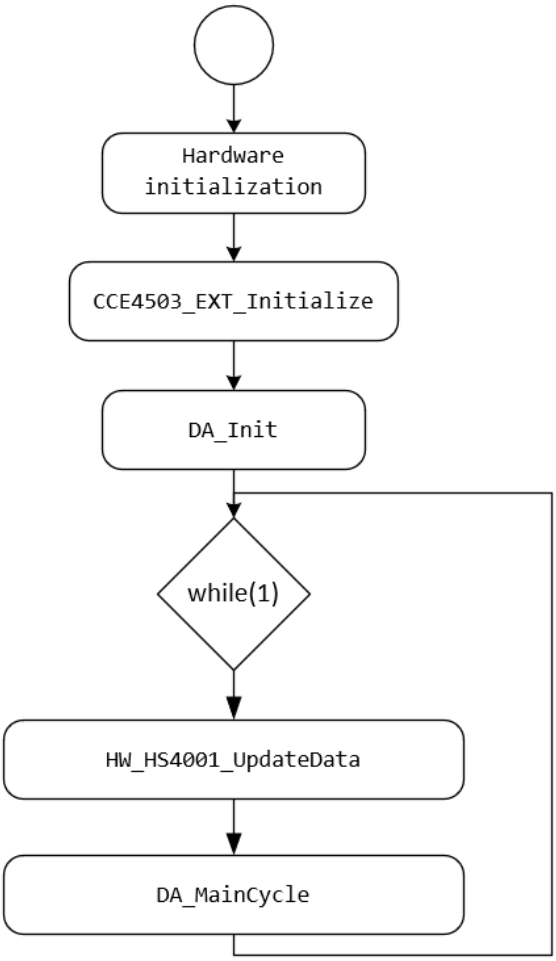

Figure 13. Application Flow Diagram

3.3 Initialization

Initialization consists of four steps:

1. Hardware from FSP configuration setup is initialized (sensor, timers, interrupts, etc).
2. Hardware dedicated for CCE4503 is started.
3. Initialization of the IO-Link library. At this step, the IO-Link device identification and buffers for data exchange are set.

   Important:

   - Identification parameters should correspond to the IODD used by the IO-LINK master
   - **lengthPDIn** and **lengthPDOut** should not be smaller than corresponding data records in **dev_process_data_exchange_usr.c**
   - These settings are kept in the library and are set in function void **DA_InitDSM**(**BooleanT isHoldRevisionId**) in **dev_apl.c** file
4. Perform initial sensor readout and data processing. The library interacts with the user through callbacks and application data is kept in global variables.

3.4 Main Loop

In the sample application, the HS4001 sensor is used and read every 10ms in the main loop. After every readout, it updates the global variable retaining the sensor values. The IO-Link device library is called in every main loop.

3.5 Data Exchange

All data is exchanged using IO-Link library callbacks. Functions that are processing callbacks are kept in the **src/iolink/appl/dev_param** folder.

The sensor's data is kept in a global variable defined as **I_process_data_in**. The data is sent to the master by placing them into a send buffer during library callback in function **DEV_PDE_USER_CopyProccessDataInToIoLink** in the **dev_process_data_exchange_usr.c** file.

Important: The data record cannot be smaller than the buffer size defined in the **DA_InitDSM** function, and it should correspond with the IODD used by the IO-Link master.

4. Quick Start Guide – Board Testing

See section 1.2 for the list of required hardware.

4.1 Setting Up the Boards and Cables

Connect the boards and cables as described below and in Figure 14.

1. QCIOT-CCE4503POCZ to PMOD2 on EK-RA4M2
2. US082-HS4001EVZ to PMOD1 on EK-RA4M2 through interposer board.
3. Micro USB cable to J10 Debug port on EK-RA4M2 board.

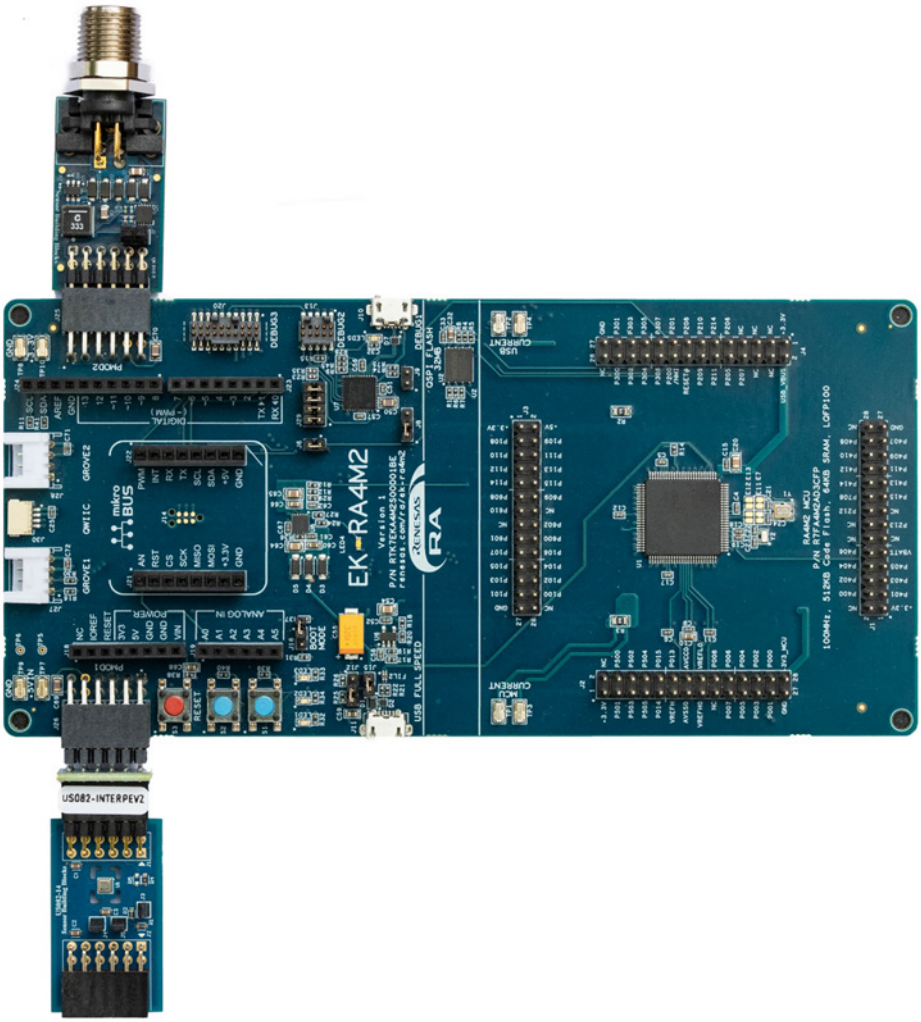

Figure 14. QCIOT-5 IO-Link Device Pmod Test Setup

Note: Ensure that the interposer board is placed in between the sensor and EK board, and the silkscreen **MCU Side** is facing the EK board.

4.2 Programming the EK Board and Running the Example Code

Download the sample project from QCIOT-CCE4503 Renesas website and import it into e2 Studio. The procedure is shown below and in Figure 15:

1. Click on *File* menu in e2 Studio.
2. Select *Import*.
3. Choose Existing Projects into Workspace.
4. Click *Next*.
5. Click on the radio button for *Select archive file*.
6. Click on *Browse* to locate the sample project.
7. Click on the *Finish* button

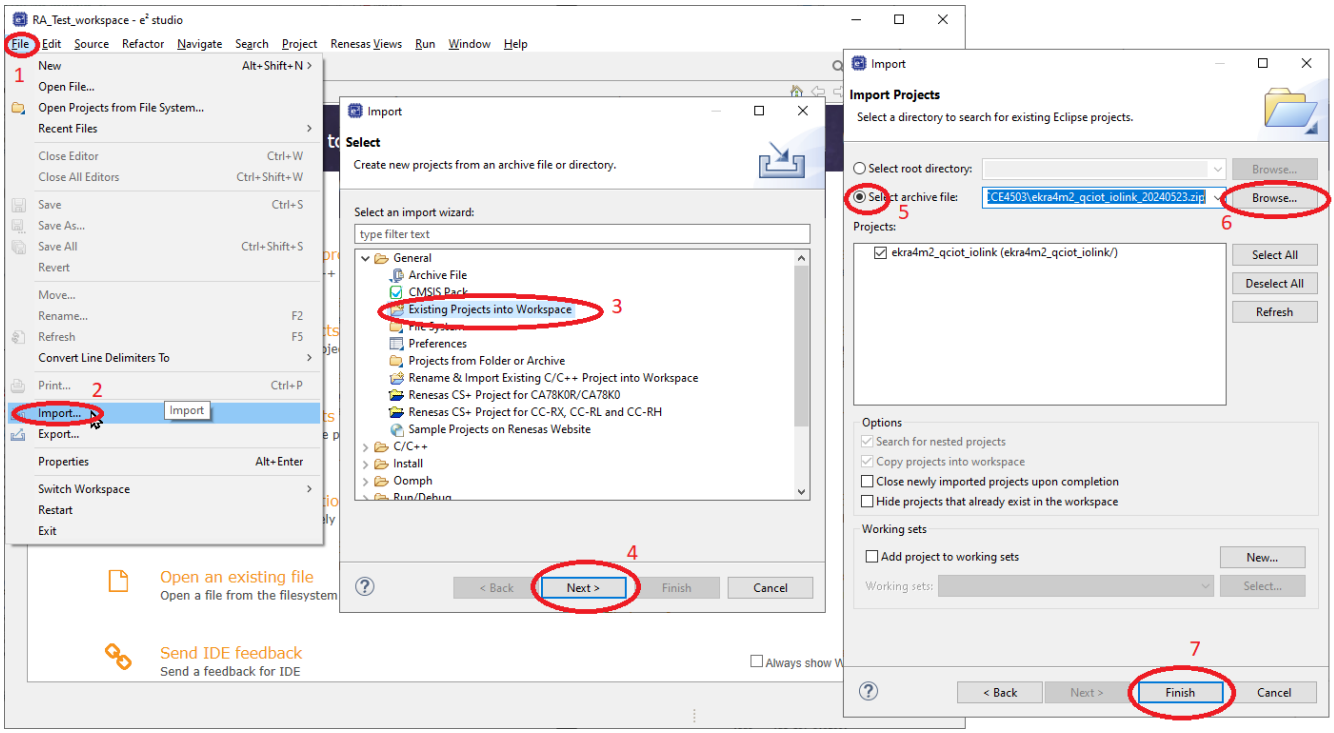

Figure 15. Import the Sample Project

8. After successfully importing the project, build it by pressing the Hammer icon button (see Figure 16).

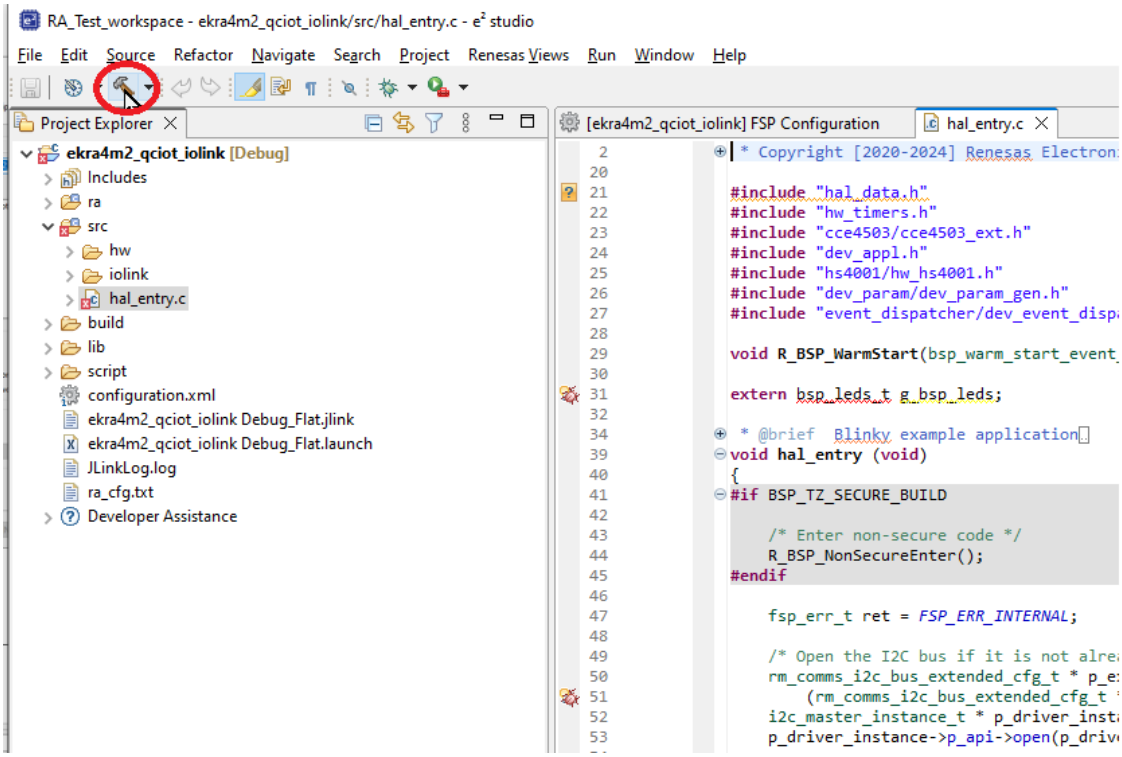

Figure 16. Build the Sample Project

The project should be built without any errors. Ignore any warnings might appear. The build result appears at the bottom of the window.

9. Debug the project by clicking on the Bug icon (see Figure 17).

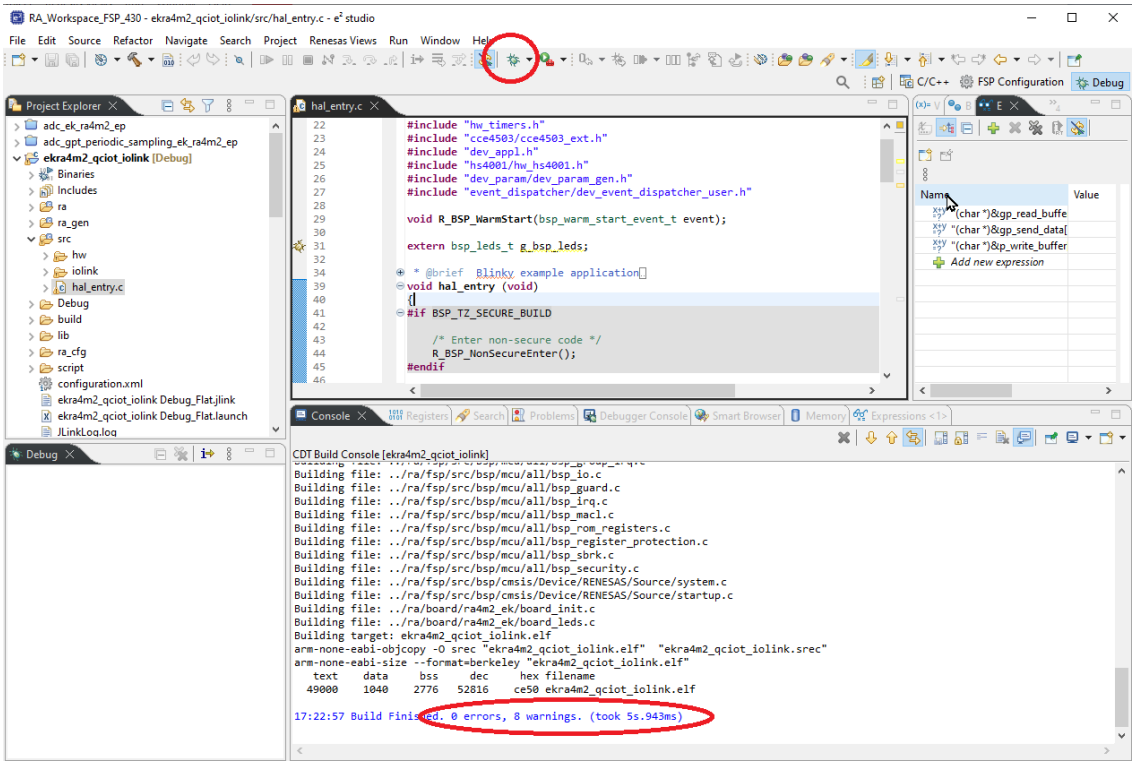

Figure 17. Flash and Debug the Sample Project

10. After the code has been flashed, click on the *Run* icon (see Figure 18).

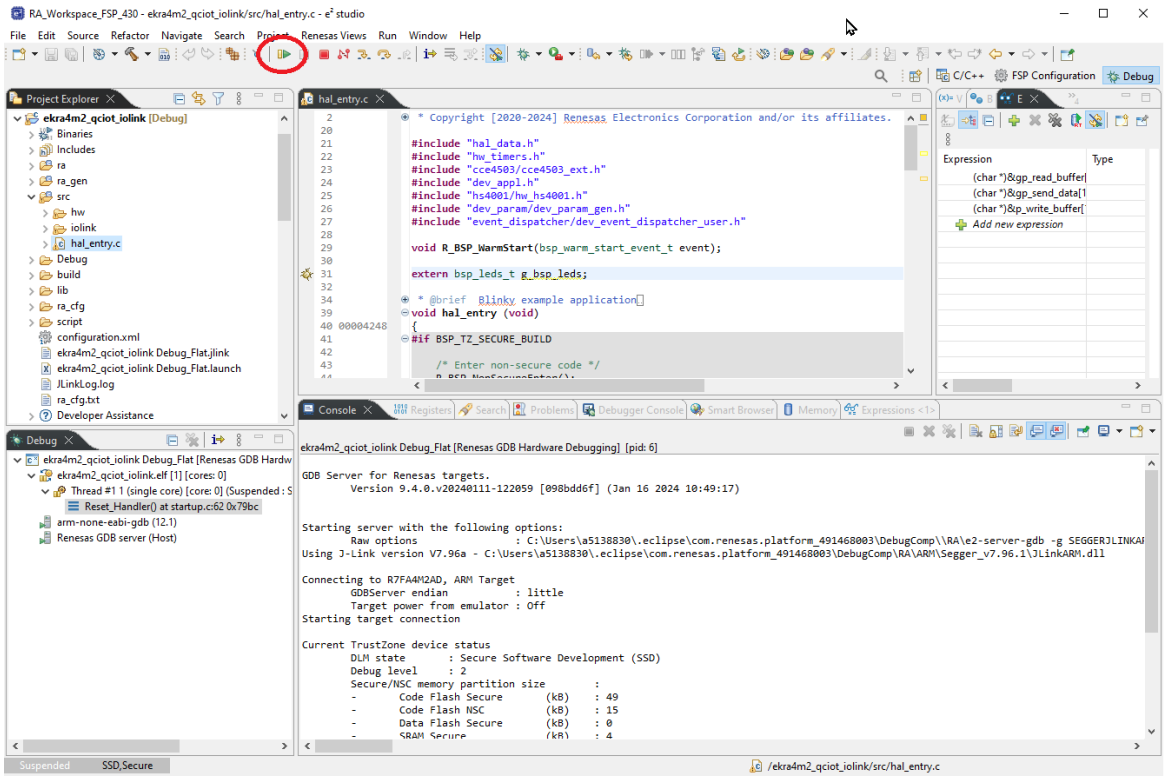

Figure 18. Run Sample Project

11. Configure the tool on a PC (see section 4.3).

4.3 Configure the IODD DTM

Data using IO-Link is sent in structures. It is required to add **Renesas CCE4503EvaKit3 IODD.xml**. Download this from the Renesas website.

For this example, we have been using PEPPERL+FUCHS IO-Link master to USB converter together with their complete software package. Download this from their website.

New IODD can be added using the IODD DTM Configurator (see Figure 19):

1. Click on *Add IODD*.
2. Browse and select Renesas CCE4503EvaKit3 IODD.xml file.
3. Click *Open*.

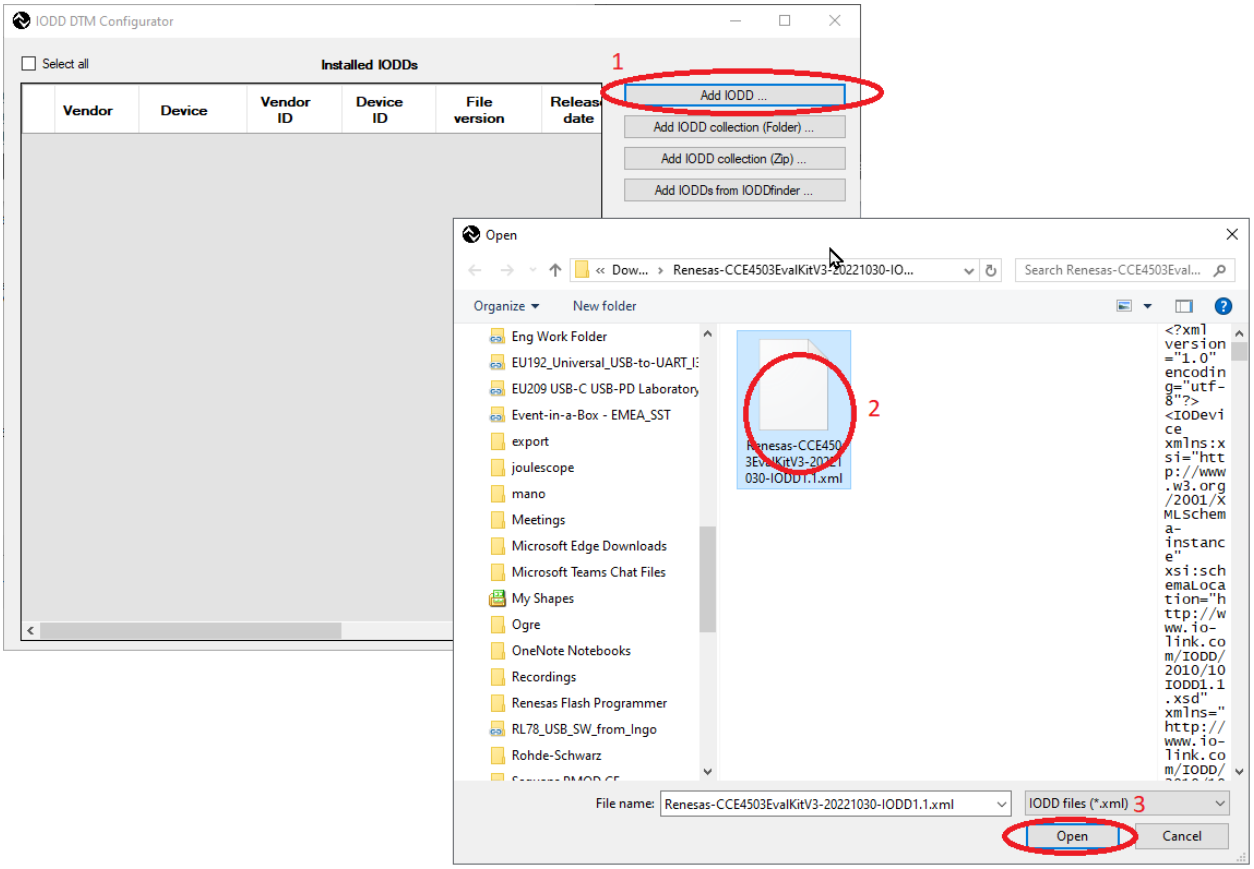

Figure 19. IODD DTM Configurator – Adding a New IODD

After IODD has been successfully added, the Renesas CCE4503EvalKitV3 device appears in the list (see Figure 20).

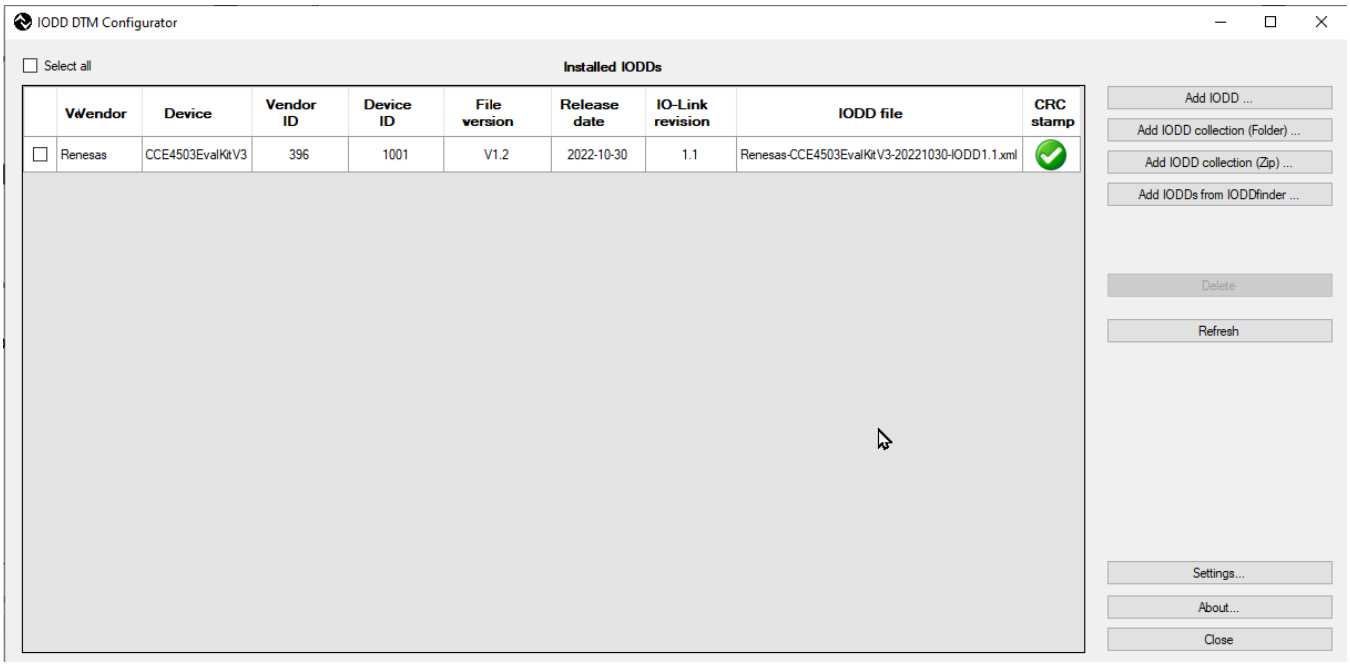

Figure 20. IODD DTM Configurator with Added Renesas CCE4503EvaKit3 IODD

4.4 Reading Parameters with PACTWare Application

When the board is flashed and IODD has been added, the temperature and humidity values can be read on the computer using the PACTware tool (downloadable from the PEPPRL+FUCHS website). This section explains how to read sensor values from the EK.

After starting PACTWare, scan the IO-Link USB master and select IO-Link Protocol. Follow the steps below and refer to Figure 21:

1. Click on *Start*.
2. Select Search new device.
3. Under **Select Communication**, select *IO-Link USB Master 2.0*.

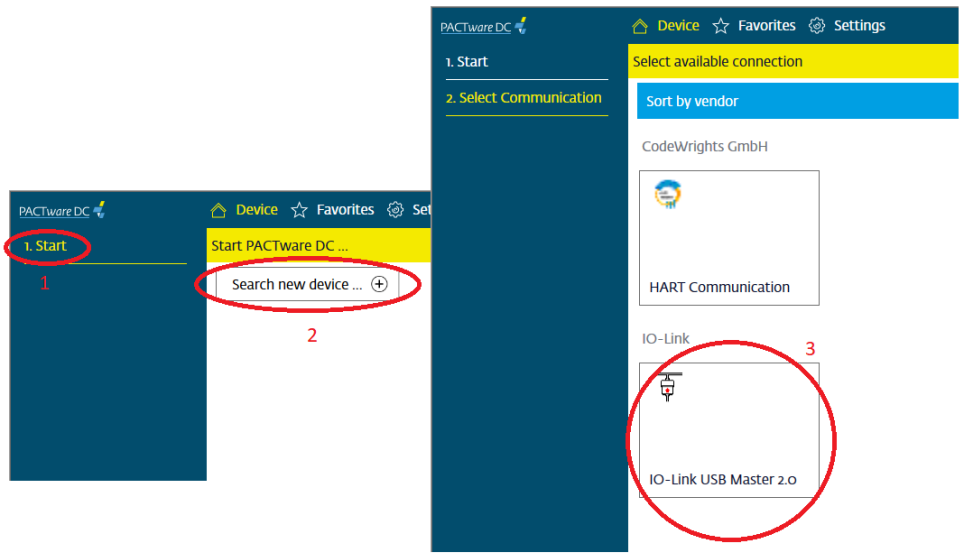

Figure 21. Setting Up the Device on PACTWare

When the connection has been successfully established, a prompt to read data from the device appears (see Figure 22). Click on *Yes*.

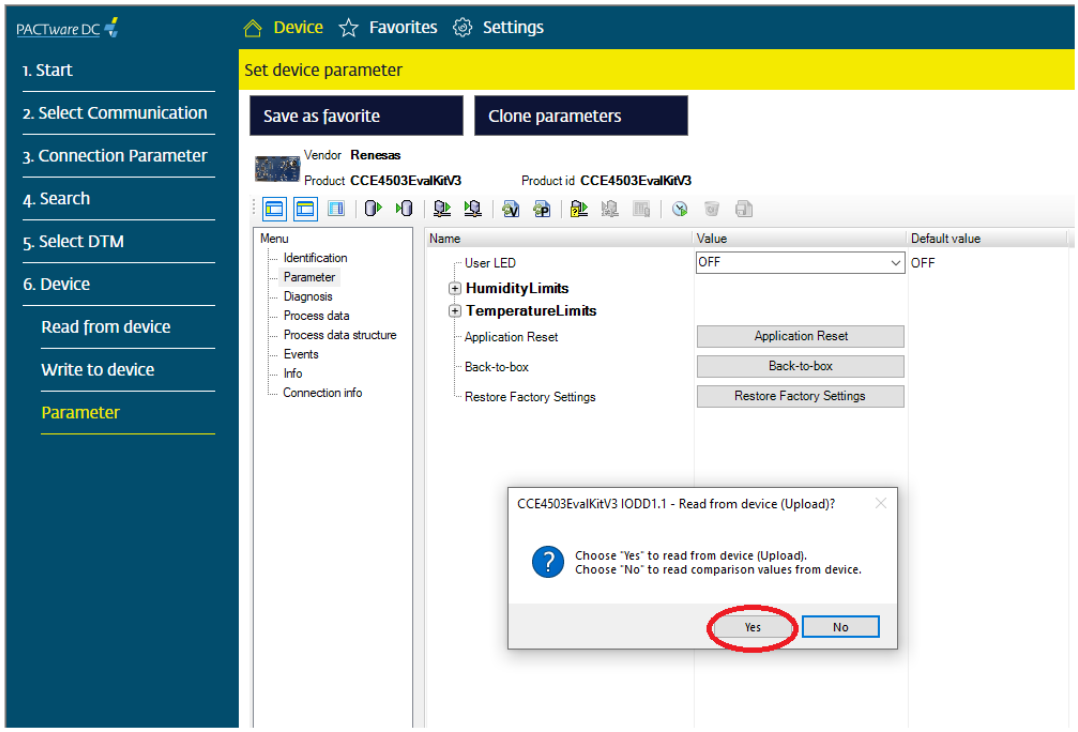

Figure 22. Read Data from Device

To enable cyclic reading of the data values, open the **Parameter** window and:

1. Click on *Process data*.
2. Enable cyclic read from the device by clicking on the icon shown in Figure 23 (labeled “2”).
3. The results are shown in the **Values** column.

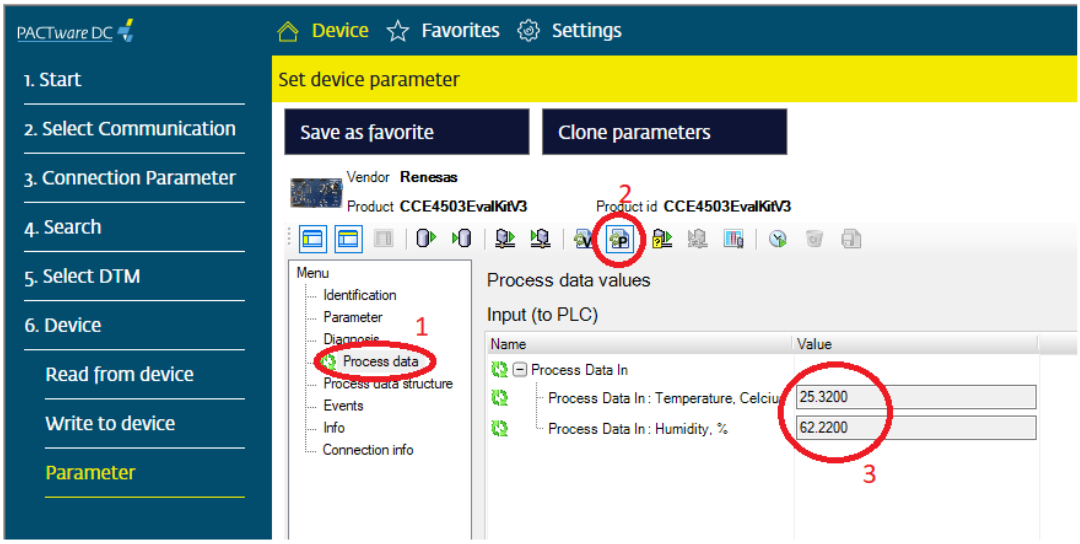

Figure 23. Cyclic Reading of the Data Values

5. Ordering Information

Part Number	Description
QCIOT-CCE4503POCZ	IO-Link Device CCE4503 Transceiver Pmod™ Board
EK-RA4M2	Evaluation Kit for RA4M2 MCU Group
US082-HS4001EVZ	Relative Humidity and Temperature Sensor Pmod™ Board
US082-INTERPEVZ	Interposer Board for Pmod™ Type 2A/3A to 6A

6. Revision History

Revision	Date	Description
1.00	Jul 30, 2024	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.