User's Manual

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R8C/M13B Group

User's Manual: Hardware

RENESAS MCU
R8C Family / R8C/Mx Series

Renesas Electronics
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. For details, see the text of the manual.

The following documents apply to the R8C/M13B Group. Make sure to see the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview and electrical characteristics	R8C/M13B Group Datasheet	R01DS0005EJ0100
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: For details on using peripheral functions, see the application notes.	R8C/M13B Group User's Manual: Hardware	This User's manual
User's manual: Software	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names
Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.
Examples the SRST bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers
The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.
Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX Register (Symbol)

Address XXXXXh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	XXX7	XXX6	XXX5	—	—	—	XXX1	XXX0
After Reset	0	0	0	0	0	0	0	0

*1

Bit	Symbol	Bit Name	Function	R/W
b0	XXX0	XXX bit	b1 b0 0 0: XXX 0 1: XXX 1 0: Do not set. 1 1: XXX	R/W
b1	XXX1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is undefined.		—
b3	—	Reserved	Set to 0.	W
b4	—			
b5	XXX5	XXX bits	Function varies depending on the operating mode.	R/W
b6	XXX6			R/W
b7	XXX7	XXX bit	0: XXX 1: XXX	R

*2 *3

*1
R/W: Read and write.
R: Read only.
W: Write only.
—: Nothing is assigned.

*2
• Reserved
Reserved bits. Set to the specified value.

*3
• Nothing is assigned.
Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
• Do not set.
Operation is not guaranteed when a value is set.
• Function varies depending on the operating mode.
The function of the bit varies with the peripheral function mode. For information on the individual modes, see the register diagram.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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Note:

1. The blank areas are reserved. No access is allowed.

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Note:
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Note:

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001A4h			
001A5h			
001A6h			
001A7h			
001A8h			
001A9h	Flash Memory Status Register	FST	481
001AAh	Flash Memory Control Register 0	FMR0	484
001ABh	Flash Memory Control Register 1	FMR1	486
001ACh	Flash Memory Control Register 2	FMR2	488
001ADh	Flash Memory Refresh Control Register	FREFR	490
001AEh			
001AFh			
001B0h			
001B1h			
001B2h			
001B3h			
001B4h			
001B5h			
001B6h			
001B7h			
001B8h			
001B9h			
001BAh			
001BBh			
001BCh			
001BDh			
001BEh			
001BFh			

Note:
1. The blank areas are reserved. No access is allowed.

Address	Register Name	Symbol	Page
001C0h	Address Match Interrupt Register 0	AIADR0L	122
001C1h		AIADR0M	
001C2h		AIADR0H	
001C3h	Address Match Interrupt Enable Register 0	AIEN0	122
001C4h	Address Match Interrupt Register 1	AIADR1L	122
001C5h		AIADR1M	
001C6h		AIADR1H	
001C7h	Address Match Interrupt Enable Register 1	AIEN1	122
001C8h			
001C9h			
001CAh			
001CBh			
001CCh			
001CDh			
001CEh			
001CFh			
001D0h			
001D1h			
001D2h			
001D3h			
001D4h			
001D5h			
001D6h			
001D7h			
001D8h			
001D9h			
001DAh			
001DBh			
001DCh			
001DDh			
001DEh			
001DFh			
001E0h			
001E1h			
001E2h			
001E3h			
001E4h			
001E5h			
001E6h			
001E7h			
001E8h			
001E9h			
001EAh			
001EBh			
001ECh			
001EDh			
001EEh			
001EFh			
001F0h			
001F1h			
001F2h			
001F3h			
001F4h			
001F5h			
001F6h			
001F7h			
001F8h			
001F9h			
001FAh			
001FBh			
001FCh			
001FDh			
001FEh			
001FFh			
:			
0FFDBh	Option Function Select Register 2	OFS2	31, 40
:			
0FFFFh	Option Function Select Register	OFS	32, 41

1. Overview

1.1 Features

The R8C/M13B Group of single-chip microcontrollers (MCUs) incorporates the R8C CPU core, which provides sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, the CPU core is capable of executing instructions at high speed. In addition, it features a multiplier for high-speed arithmetic processing.
Power consumption is low, and the supported operating modes allow additional power control. These MCUs are designed to maximize EMI/EMS performance.
Integration of many peripheral functions on the same chip, including multifunction timer and serial interface, reduces the number of system components.
The R8C/M13B Group includes data flash (1 KB × 2 blocks).

1.1.1 Applications

Home appliances, office equipment, audio equipment, consumer products, etc.

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications.

Table 1.1 Specifications (1)

Item	Function	Description
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 V to 5.5 V) 200 ns (f(XIN) = 5 MHz, VCC = 1.8 V to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, data flash	See **Table 1.3 Product List**.
Reset sources		• Hardware reset by $\overline{\text{RESET}}$ • Power-on reset • Watchdog timer reset • Software reset • Reset by voltage detection 0
Voltage detection	Voltage detection circuit	Voltage detection with two check points: Voltage detection 0, voltage detection 1 (detection levels selectable)
Watchdog timer		• 14 bits × 1 (with prescaler) • Reset start function selectable • Count source protection function selectable • Periodic timer function selectable
Clock	Clock generation circuits	• 4 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit, high-speed on-chip oscillator (with frequency adjustment function), low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Clock frequency divider circuit integrated
Power control		• Standard operating mode • Wait mode (CPU stopped, peripheral functions in operation) • Stop mode (CPU and peripheral functions stopped)
Interrupts		• Number of interrupt vectors: 69 • External interrupt inputs: 8 ($\overline{\text{INT}}$ × 4, key input × 4) • Priority levels: 2
I/O ports	Programmable I/O ports	• CMOS I/O: 29 (pull-up resistor selectable) • High-current drive ports: 8
Timer	Timer RJ2	16 bits × 1 Timer mode, pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB2	8 bits × 1 (with 8-bit prescaler) or 16 bits × 1 (selectable) Timer mode, programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (output compare function, input capture function), PWM mode (3 outputs), PWM2 mode (1 PWM output)
	Timer RK	8 bits × 1 Interval mode, pulse output mode, output compare mode
	Timer RE2	8 bits × 1 Real-time clock mode, compare match timer mode
Serial interface	UART0	Clock synchronous serial I/O. Also used for asynchronous serial I/O.
	UART1	
Clock synchronous serial interface		• Synchronous serial communication unit (SSU) × 1 channel • I^2C bus interface × 1 channel

Table 1.2 Specifications (2)

Item	Function	Description
IrDA interface		1 channel (UART0 and UART1 can be switched)
A/D converter		• Resolution: 10 bits × 8 channels • Sample and hold function, sweep mode
Comparator B		2 circuits
Flash memory		• Program/erase voltage for program ROM: VCC = 1.8 V to 5.5 V • Program/erase voltage for data flash: VCC = 1.8 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 10,000 times (program ROM) • Program security: ID code check, protection enabled by lock bit • Debug functions: On-chip debug, on-board flash rewrite function
Operating frequency/ Power supply voltage		f(XIN) = 20 MHz (VCC = 2.7 V to 5.5 V) f(XIN) = 5 MHz (VCC = 1.8 V to 5.5 V)
Temperature range		-20 °C to 85 °C (N version) -40 °C to 85 °C (D version) (1)
Package		32-pin LQFP: [Package code] PLQP0032GB-A

Note:
1. Specify the D version if its functions are to be used.

1.2 Product List

Table 1.3 lists the Product List. Figure 1.1 shows the Product Part Number Structure.

Table 1.3 Product List **Current of Mar 2012**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F2M131BNFP	4 Kbytes	1 Kbyte × 2	384 bytes	PLQP0032GB-A	N version
R5F2M132BNFP	8 Kbytes	1 Kbyte × 2	512 bytes		
R5F2M134BNFP	16 Kbytes	1 Kbyte × 2	1 Kbyte		
R5F2M131BDFP	4 Kbytes	1 Kbyte × 2	384 bytes		D version
R5F2M132BDFP	8 Kbytes	1 Kbyte × 2	512 bytes		
R5F2M134BDFP	16 Kbytes	1 Kbyte × 2	1 Kbyte		

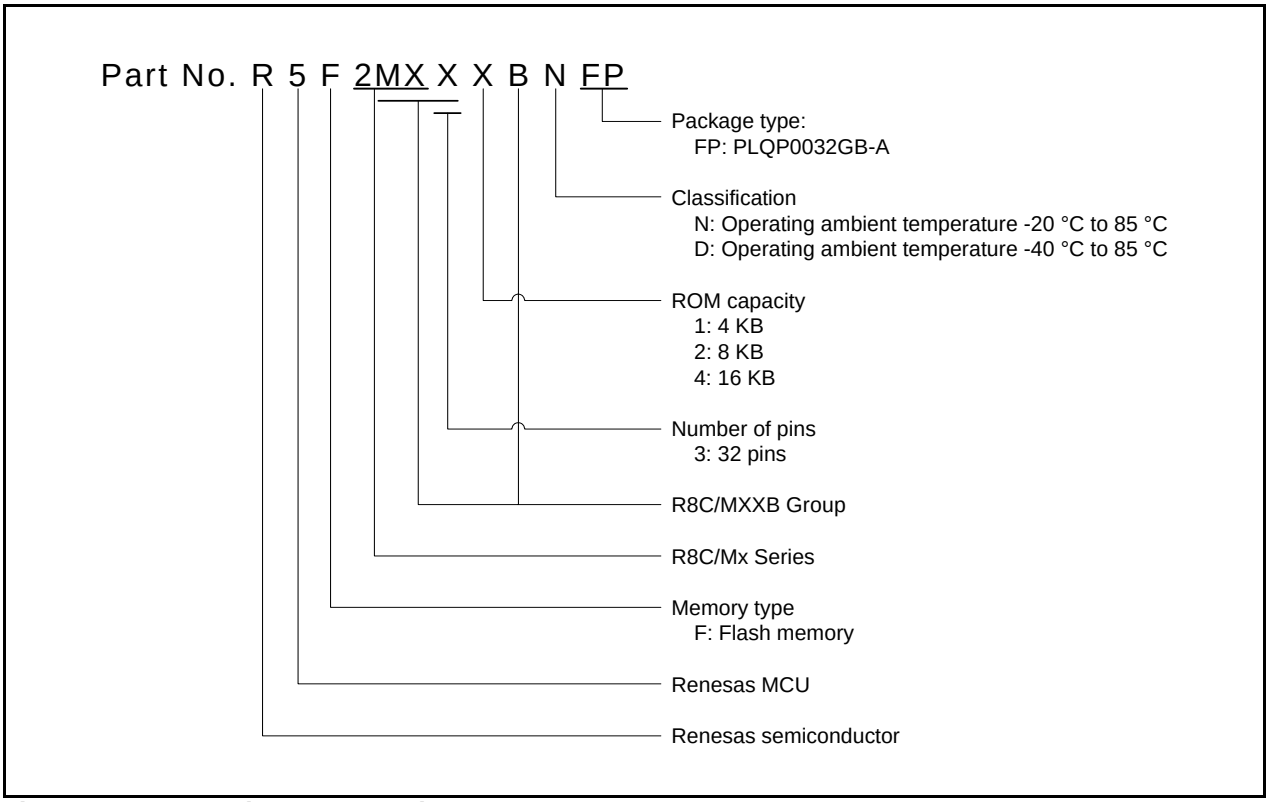


Figure 1.1 Product Part Number Structure

1.3 Block Diagram

Figure 1.2 shows the Block Diagram.

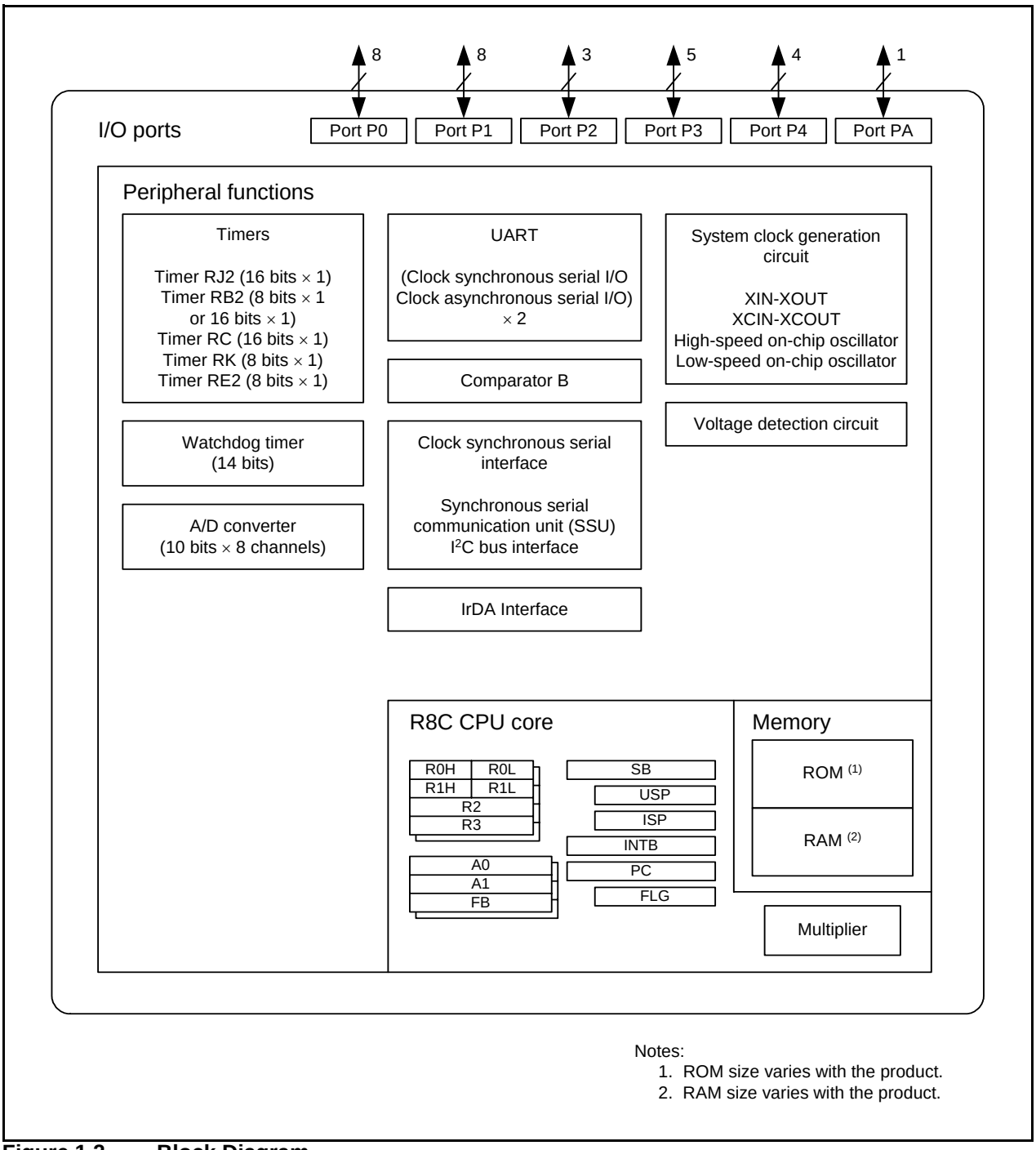
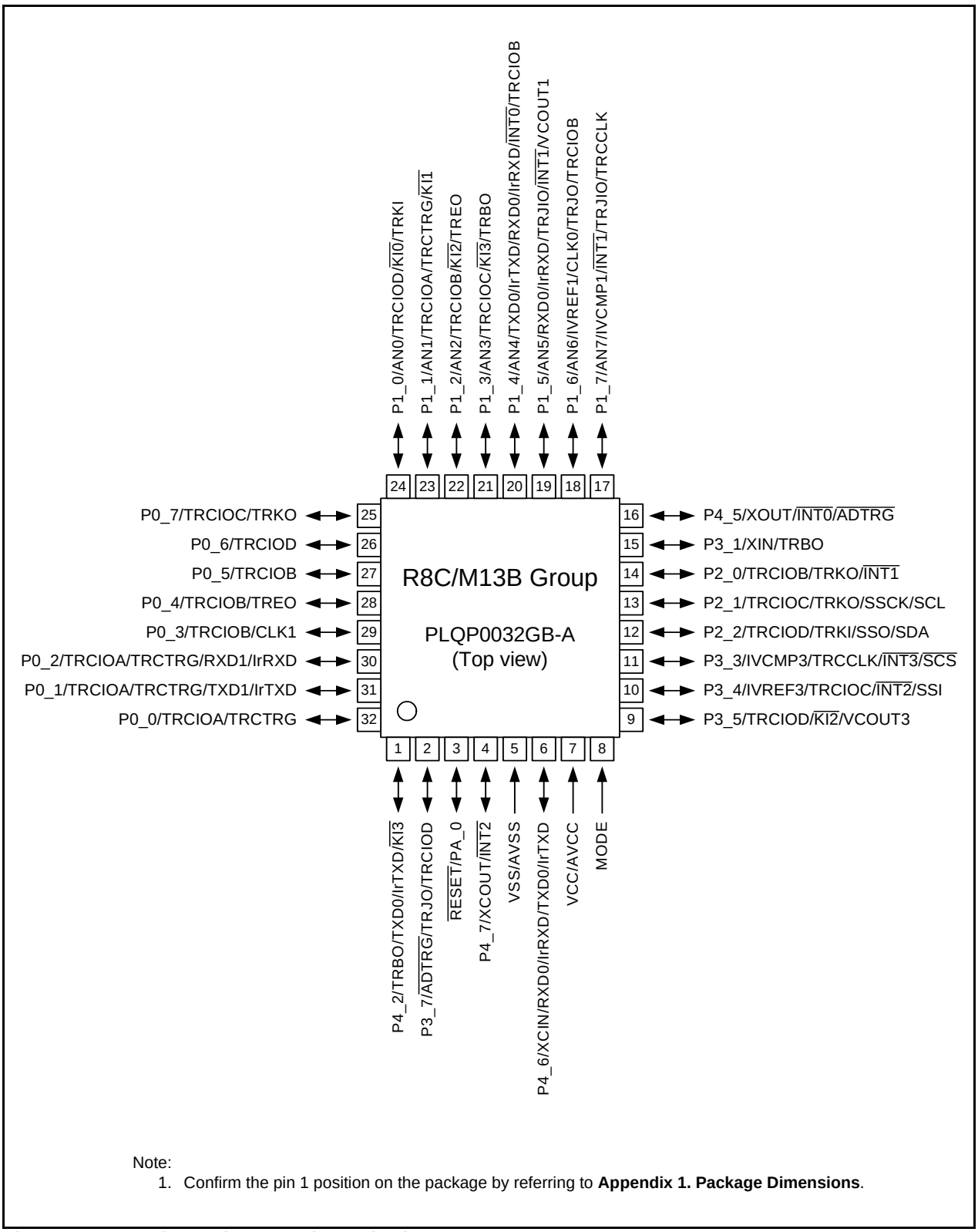


Figure 1.2 Block Diagram

1.4 Pin Assignment

Figure 1.3 shows the Pin Assignment (Top View). Table 1.4 lists the Pin Name Information by Pin Number.



Note:
1. Confirm the pin 1 position on the package by referring to **Appendix 1. Package Dimensions**.

Figure 1.3 Pin Assignment (Top View)

Table 1.4 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pins for Peripheral Functions						
			Interrupt	Timer	Serial Interface	IrDA	SSU	I^2C bus	A/D Converter, Comparator B
1		P4_2	$\overline{KI3}$	TRBO	TXD0	IrTXD			
2		P3_7		TRJO/TRCIOD					$\overline{ADTRG}$
3	$\overline{RESET}$	PA_0							
4	XCOUT	P4_7	$\overline{INT2}$						
5	VSS/AVSS								
6	XCIN	P4_6			RXD0/TXD0	IrRXD/ IrTXD			
7	VCC/AVCC								
8	MODE								
9		P3_5	$\overline{KI2}$	TRCIOD					VCOUT3
10		P3_4	$\overline{INT2}$	TRCIOC			SSI		IVREF3
11		P3_3	$\overline{INT3}$	TRCCLK			$\overline{SCS}$		IVCMP3
12		P2_2		TRCIOD/TRKI			SSO	SDA	
13		P2_1		TRCIOC/TRKO			SSCK	SCL	
14		P2_0	$\overline{INT1}$	TRCIOB/TRKO					
15	XIN	P3_1		TRBO					
16	XOUT	P4_5	$\overline{INT0}$						$\overline{ADTRG}$
17		P1_7	$\overline{INT1}$	TRJIO/TRCCLK					AN7/IVCMP1
18		P1_6		TRJO/TRCIOB	CLK0				AN6/IVREF1
19		P1_5	$\overline{INT1}$	TRJIO	RXD0	IrRXD			AN5/VCOUT1
20		P1_4	$\overline{INT0}$	TRCIOB	RXD0/TXD0	IrRXD/ IrTXD			AN4
21		P1_3	$\overline{KI3}$	TRBO/TRCIOC					AN3
22		P1_2	$\overline{KI2}$	TRCIOB/TREO					AN2
23		P1_1	$\overline{KI1}$	TRCIOA/TRCTRG					AN1
24		P1_0	$\overline{KI0}$	TRCIOD/TRKI					AN0
25		P0_7		TRCIOC/TRKO					
26		P0_6		TRCIOD					
27		P0_5		TRCIOB					
28		P0_4		TRCIOB/TREO					
29		P0_3		TRCIOB	CLK1				
30		P0_2		TRCIOA/TRCTRG	RXD1	IrRXD			
31		P0_1		TRCIOA/TRCTRG	TXD1	IrTXD			
32		P0_0		TRCIOA/TRCTRG					

1.5 Pin Functions

Tables 1.5 and 1.6 list Pin Functions.

Table 1.5 Pin Functions (1)

Item	Pin Name	I/O	Description
Power supply input	VCC, VSS	—	Apply 1.8 V through 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	—	Power supply input for the A/D converter. Connect a capacitor between pins AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Applying a low level to this pin resets the MCU.
MODE	MODE	I	Connect this pin to the VCC pin via a resistor.
XIN clock input	XIN	I	I/O for the XIN clock generation circuit. Connect a ceramic resonator or a crystal oscillator between pins XIN and XOUT. (1) To use an external clock, input it to the XIN pin. P4_5 can be used as an I/O port at this time.
XIN clock output	XOUT	O	
XCIN clock input	XCIN	I	I/O for the XCIN clock generation circuit. Connect a crystal oscillator between pins XCIN and XCOUT. (1) To use an external clock, input it to the XCIN pin. P4_7 can be used as an I/O port at this time.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input.
I/O ports	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_2, P3_1, P3_3 to P3_5, P3_7, P4_2, P4_5 to P4_7, PA_0	I/O	CMOS I/O ports. Each port has an I/O select direction register, enabling switching input and output for each port. For input ports other than PA_0, the presence or absence of a pull-up resistor can be selected by a program. P1_2 to P1_5, P3_3 to P3_5, and P3_7 can be used as LED drive ports.
Timer RJ2	TRJIO	I/O	Timer RJ2 I/O.
	TRJO	O	Timer RJ2 output.
Timer RB2	TRBO	O	Timer RB2 output.
Timer RC	TRCCLK	I	External clock input.
	TRCTRG	I	External trigger input.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O.
Timer RK	TRKI	I	Timer RK external input.
	TRKO	O	Timer RK output.
Timer RE2	TREO	O	Timer RE2 output.
Serial interface	CLK0, CLK1	I/O	Transfer clock I/O.
	RXD0, RXD1	I	Serial data input.
	TXD0, TXD1	O	Serial data output.
Synchronous serial communication unit (SSU)	SSI	I/O	Data I/O.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O.
	SSO	I/O	Data I/O.
	SSCK	I/O	Clock I/O.
I^2C bus interface	SDA	I/O	Data I/O.
	SCL	I/O	Clock I/O.
IrDA Interface	IrRXD	I	Data input.
	IrTXD	O	Data output.
A/D converter	AN0 to AN7	I	Analog input for the A/D converter.
	$\overline{\text{ADTRG}}$	I	External trigger input for the A/D converter.

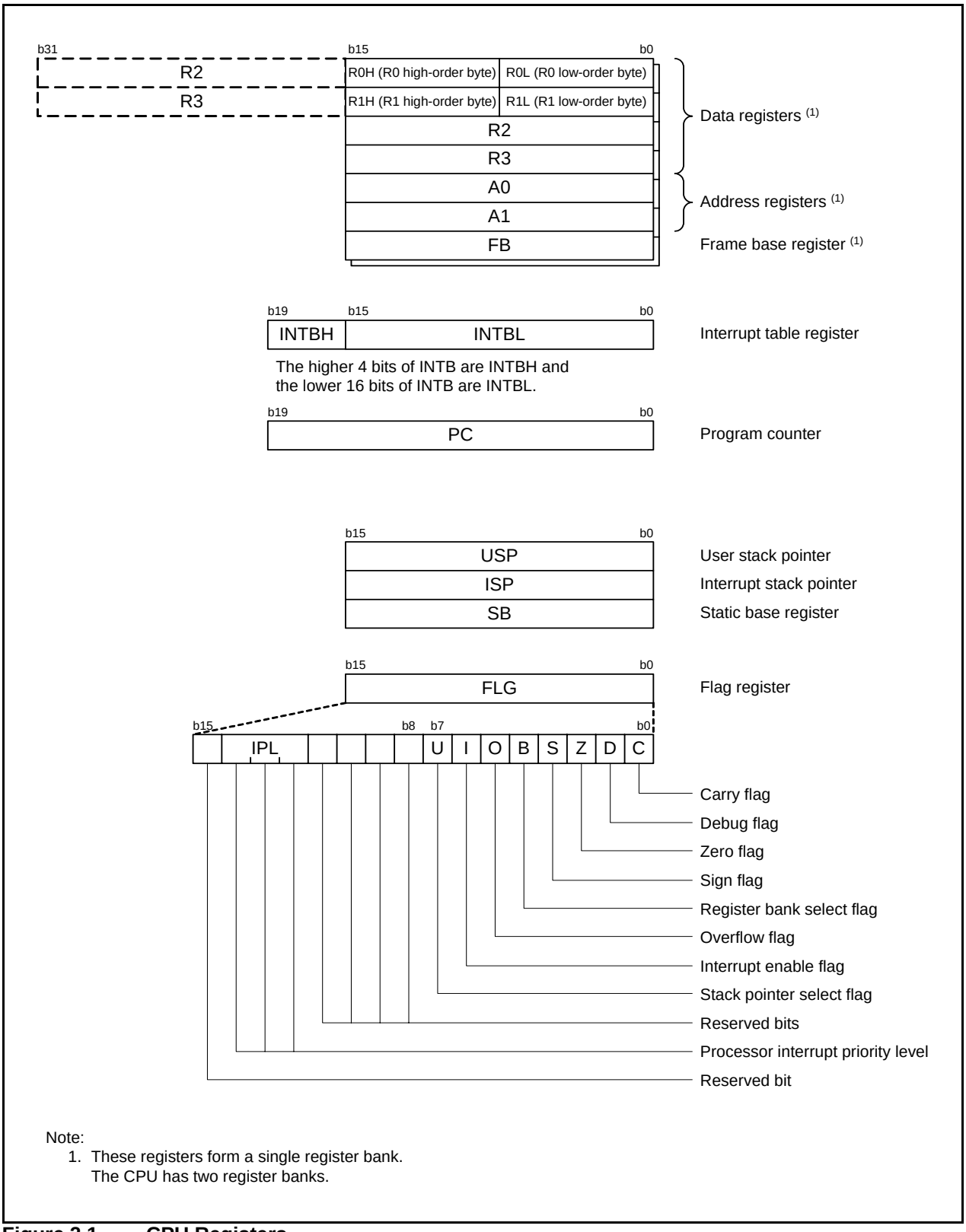
Note:
1. Contact the oscillator manufacturer for oscillation characteristics.

Table 1.6 Pin Functions (2)

Item	Pin Name	I/O	Description
Comparator B	IVCMP1, IVCMP3	I	Analog voltage input for comparator B.
	IVREF1, IVREF3	I	Reference voltage input for comparator B.
	VCOUT1, VCOUT3	O	Comparison result output for comparator B.

2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers, R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.



Note:
1. These registers form a single register bank. The CPU has two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3.
R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). In the same way as with R0 and R2, R3 and R1 can be used as a 32-bit data register (R3R1).

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled. If IPL is set to levels from 2 to 7, all maskable interrupt requests are disabled.

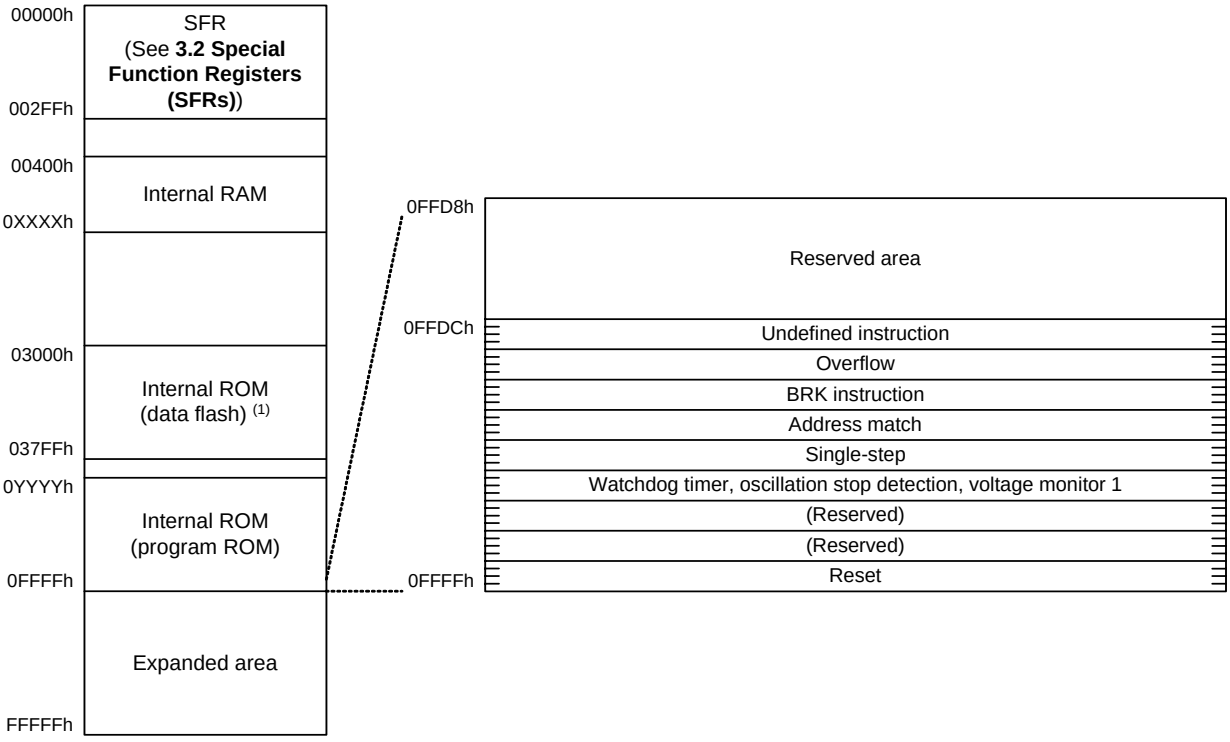
2.8.10 Reserved Bit

The write value must be 0. The read value is undefined.

3. Address Space

3.1 Memory Map

Figure 3.1 shows the Memory Map. The R8C/M13B Group have a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated at lower addresses, beginning with address 0FFFFh. For example, an 8-Kbyte internal ROM area is allocated at addresses 0E000h to 0FFFFh.
The fixed interrupt vector table is allocated at addresses 0FFDCh to 0FFFFh. The start address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated at addresses 03000h to 037FFh.
The internal RAM is allocated at higher addresses, beginning with address 00400h. For example, a 512-byte internal RAM area is allocated at addresses 00400h to 005FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated at addresses 00000h to 002FFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (1 Kbyte) and block B (1 Kbyte).
2. The blank areas are reserved. No access is allowed.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F2M131BNFP, R5F2M131BDFP	4 Kbytes	0F000h	384 bytes	0057Fh
R5F2M132BNFP, R5F2M132BDFP	8 Kbytes	0E000h	512 bytes	005FFh
R5F2M134BNFP, R5F2M134BDFP	16 Kbytes	0C000h	1 Kbytes	007FFh

Figure 3.1 Memory Map

3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.8 list the SFR Information. Table 3.9 lists the ID Code Area and Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Register Name	Symbol	After Reset
00000h			
00001h			
00002h			
00003h			
00004h			
00005h			
00006h			
00007h			
00008h			
00009h			
0000Ah			
0000Bh			
0000Ch			
0000Dh			
0000Eh			
0000Fh			
00010h	Processor Mode Register 0	PM0	00h
00011h			
00012h	Module Standby Control Register	MSTCR	00h (2) 01110111b (3)
00013h	Protect Register	PRCR	00h
00014h			
00015h			
00016h	Hardware Reset Protect Register	HRPR	00h
00017h	Module Standby Control Register 1	MSTCR1	00h (2) FFh (3)
00018h			
00019h			
0001Ah			
0001Bh			
0001Ch			
0001Dh			
0001Eh			
0001Fh			
00020h	External Clock Control Register	EXCKCR	00h
00021h	High-Speed/Low-Speed On-Chip Oscillator Control Register	OCOCR	00h
00022h	System Clock f Control Register	SCKCR	00h
00023h	System Clock f Select Register	PHISEL	00h
00024h	Clock Stop Control Register	CKSTPR	00h
00025h	Clock Control Register When Returning	CKRSCR	00h
00026h	Oscillation Stop Detection Register	BAKCR	00h
00027h			
00028h			
00029h			
0002Ah			
0002Bh			
0002Ch			
0002Dh			
0002Eh			
0002Fh			
00030h	Watchdog Timer Function Register	RISR	10000000b (4) 00h (5)
00031h	Watchdog Timer Reset Register	WDTR	XXh
00032h	Watchdog Timer Start Register	WDTS	XXh
00033h	Watchdog Timer Control Register	WDTC	01XXXXXXb
00034h	Count Source Protection Mode Register	CSPR	10000000b (4) 00h (5)
00035h	Periodic Timer Interrupt Control Register	WDTIR	00h
00036h			
00037h			
00038h	External Input Enable Register	INTEN	00h
00039h			

Notes:
1. The blank areas are reserved. No access is allowed.
2. The MSTINI bit in the OFS2 register is 0.
3. The MSTINI bit in the OFS2 register is 1.
4. The CSPROINI bit in the OFS register is 0.
5. The CSPROINI bit in the OFS register is 1.

Table 3.2 SFR Information (2) (1)

Address	Register Name	Symbol	After Reset
0003Ah	INT Input Filter Select Register 0	INTF0	00h
0003Bh			
0003Ch	INT Input Edge Select Register 0	ISCR0	00h
0003Dh			
0003Eh	Key Input Enable Register	KIEN	00h
0003Fh			
00040h	Interrupt Priority Level Register 0	ILVL0	00h
00041h	Interrupt Priority Level Register 1	ILVL1	00h
00042h	Interrupt Priority Level Register 2	ILVL2	00h
00043h	Interrupt Priority Level Register 3	ILVL3	00h
00044h	Interrupt Priority Level Register 4	ILVL4	00h
00045h	Interrupt Priority Level Register 5	ILVL5	00h
00046h	Interrupt Priority Level Register 6	ILVL6	00h
00047h	Interrupt Priority Level Register 7	ILVL7	00h
00048h	Interrupt Priority Level Register 8	ILVL8	00h
00049h	Interrupt Priority Level Register 9	ILVL9	00h
0004Ah	Interrupt Priority Level Register A	ILVLA	00h
0004Bh	Interrupt Priority Level Register B	ILVLB	00h
0004Ch	Interrupt Priority Level Register C	ILVLC	00h
0004Dh	Interrupt Priority Level Register D	ILVLD	00h
0004Eh	Interrupt Priority Level Register E	ILVLE	00h
0004Fh			
00050h	Interrupt Monitor Flag Register 0	IRR0	00h
00051h	Interrupt Monitor Flag Register 1	IRR1	00h
00052h	Interrupt Monitor Flag Register 2	IRR2	00h
00053h	External Interrupt Flag Register	IRR3	00h
00054h			
00055h			
00056h			
00057h			
00058h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
00059h			
0005Ah	Voltage Detect Register 2	VCA2	00100100b (2) 00000100b (3)
0005Bh	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0005Ch	Voltage Monitor 0 Circuit Control Register	VW0C	1100X011b (2) 1100X010b (3)
0005Dh	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b
0005Eh			
0005Fh	Reset Source Determination Register	RSTFR	0000XXXXb (4)
00060h			
00061h			
00062h			
00063h			
00064h	High-Speed On-Chip Oscillator 18.432 MHz Control Register 0	FR18S0	Value when shipped
00065h	High-Speed On-Chip Oscillator 18.432 MHz Control Register 1	FR18S1	Value when shipped
00066h			
00067h	High-Speed On-Chip Oscillator Control Register 1	FRV1	Value when shipped
00068h	High-Speed On-Chip Oscillator Control Register 2	FRV2	Value when shipped
00069h			
0006Ah			
0006Bh			
0006Ch			
0006Dh			
0006Eh			
0006Fh			
00070h			
00071h			
00072h			
00073h			
00074h			
00075h			
00076h			
00077h			
00078h			
00079h			

X: Undefined

Notes:

1. The blank areas are reserved. No access is allowed.
2. The LVDAS bit in the OFS register is 0.
3. The LVDAS bit in the OFS register is 1.
4. The value after a reset differs depending on the reset source.

Table 3.3 SFR Information (3) (1)

Address	Register Name	Symbol	After Reset
0007Ah			
0007Bh			
0007Ch			
0007Dh			
0007Eh			
0007Fh			
00080h	UART0 Transmit/Receive Mode Register	U0MR	00h
00081h	UART0 Bit Rate Register	U0BRG	XXh
00082h	UART0 Transmit Buffer Register	U0TBL	XXh
00083h		U0TBH	XXh
00084h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00085h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00086h	UART0 Receive Buffer Register	U0RBL	XXh
00087h		U0RBH	XXh
00088h	UART0 Interrupt Flag and Enable Register	U0IR	00h
00089h			
0008Ah			
0008Bh			
0008Ch			
0008Dh			
0008Eh			
0008Fh			
00090h			
00091h			
00092h			
00093h			
00094h			
00095h			
00096h			
00097h			
00098h	A/D Register 0	AD0L	XXh
00099h		AD0H	000000XXb
0009Ah	A/D Register 1	AD1L	XXh
0009Bh		AD1H	000000XXb
0009Ch	A/D Mode Register	ADMOD	00h
0009Dh	A/D Input Select Register	ADINSEL	00h
0009Eh	A/D Control Register 0	ADCON0	00h
0009Fh	A/D Interrupt Control Status Register	ADICSR	00h
000A0h			
000A1h			
000A2h			
000A3h			
000A4h			
000A5h			
000A6h			
000A7h			
000A8h	Port P0 Direction Register	PD0	00h
000A9h	Port P1 Direction Register	PD1	00h
000AAh	Port P2 Direction Register	PD2	00h
000ABh	Port P3 Direction Register	PD3	00h
000ACh	Port P4 Direction Register	PD4	00h
000ADh	Port PA Direction Register	PDA	00h
000AEh	Port P0 Register	P0	00h
000AFh	Port P1 Register	P1	00h
000B0h	Port P2 Register	P2	00h
000B1h	Port P3 Register	P3	00h
000B2h	Port P4 Register	P4	00h
000B3h	Port PA Register	PA	00h
000B4h	Pull-Up Control Register 0	PUR0	00h
000B5h	Pull-Up Control Register 1	PUR1	00h
000B6h	Pull-Up Control Register 2	PUR2	00h
000B7h	Pull-Up Control Register 3	PUR3	00h
000B8h	Pull-Up Control Register 4	PUR4	00h
000B9h	Port I/O Function Control Register	PINSR	00h
000BAh			
000BBh	Drive Capacity Control Register 1	DRR1	00h
000BCh			
000BDh	Drive Capacity Control Register 3	DRR3	00h
000BEh			
000BFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.4 SFR Information (4) (1)

Address	Register Name	Symbol	After Reset
000C0h	Open-Drain Control Register 0	POD0	00h
000C1h	Open-Drain Control Register 1	POD1	00h
000C2h	Open-Drain Control Register 2	POD2	00h
000C3h	Open-Drain Control Register 3	POD3	00h
000C4h	Open-Drain Control Register 4	POD4	00h
000C5h	Port PA Mode Control Register	PAMCR	11h
000C6h	Port 0 Function Mapping Register 0	PML0	00h
000C7h	Port 0 Function Mapping Register 1	PMH0	00h
000C8h	Port 1 Function Mapping Register 0	PML1	00h
000C9h	Port 1 Function Mapping Register 1	PMH1	00h
000CAh	Port 2 Function Mapping Register 0	PML2	00h
000CBh			
000CCh	Port 3 Function Mapping Register 0	PML3	00h
000CDh	Port 3 Function Mapping Register 1	PMH3	00h
000CEh	Port 4 Function Mapping Register 0	PML4	00h
000CFh	Port 4 Function Mapping Register 1	PMH4	00h
000D0h			
000D1h	Port 1 Function Mapping Expansion Register	PMH1E	00h
000D2h			
000D3h			
000D4h			
000D5h			
000D6h			
000D7h			
000D8h	Timer RJ Counter Register	TRJ	FFh
000D9h			FFh
000DAh	Timer RJ Control Register	TRJCR	00h
000DBh	Timer RJ I/O Control Register	TRJIOC	00h
000DCh	Timer RJ Mode Register	TRJMR	00h
000DDh	Timer RJ Event Select Register	TRJISR	00h
000DEh	Timer RJ Interrupt Control Register	TRJIR	00h
000DFh			
000E0h	Timer RB Control Register	TRBCR	00h
000E1h	Timer RB One-Shot Control Register	TRBOCR	00h
000E2h	Timer RB I/O Control Register	TRBIOC	00h
000E3h	Timer RB Mode Register	TRBMR	00h
000E4h	Timer RB Prescaler Register (2) Timer RB Primary/Secondary Register (Lower 8 Bits) (3)	TRBPRE	FFh
000E5h	Timer RB Primary Register (2) Timer RB Primary Register (Higher 8 Bits) (3)	TRBPR	FFh
000E6h	Timer RB Secondary Register (2) Timer RB Secondary Register (Higher 8 Bits) (3)	TRBSC	FFh
000E7h	Timer RB Interrupt Control Register	TRBIR	00h
000E8h	Timer RC Counter	TRCCNT	00h
000E9h			00h
000EAh	Timer RC General Register A	TRCGRA	FFh
000EBh			FFh
000ECh	Timer RC General Register B	TRCGRB	FFh
000EDh			FFh
000EEh	Timer RC General Register C	TRCGRC	FFh
000EFh			FFh
000F0h	Timer RC General Register D	TRCGRD	FFh
000F1h			FFh
000F2h	Timer RC Mode Register	TRCMR	01001000b
000F3h	Timer RC Control Register 1	TRCCR1	00h
000F4h	Timer RC Interrupt Enable Register	TRCIER	01110000b
000F5h	Timer RC Status Register	TRCSR	01110000b
000F6h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
000F7h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
000F8h	Timer RC Control Register 2	TRCCR2	00011000b
000F9h	Timer RC Digital Filter Function Select Register	TRCDF	00h
000FAh	Timer RC Output Enable Register	TRCOER	01111111b
000FBh	Timer RC A/D Conversion Trigger Control Register	TRCADCR	11110000b
000FCh	Timer RC Waveform Output Manipulation Register	TRCOPR	00h
000FDh			
000FEh			
000FFh			

Notes:
1. The blank areas are reserved. No access is allowed.
2. The TCNT16 bit in the TRBMR register is 0.
3. The TCNT16 bit in the TRBMR register is 1.

Table 3.5 SFR Information (5) (1)

Address	Register Name	Symbol	After Reset
00100h			
00101h			
00102h			
00103h			
00104h			
00105h			
00106h			
00107h			
00108h			
00109h			
0010Ah			
0010Bh			
0010Ch			
0010Dh			
0010Eh			
0010Fh			
00110h			
00111h			
00112h			
00113h			
00114h			
00115h			
00116h			
00117h			
00118h			
00119h			
0011Ah			
0011Bh			
0011Ch			
0011Dh			
0011Eh			
0011Fh			
00120h			
00121h			
00122h			
00123h			
00124h			
00125h			
00126h			
00127h			
00128h			
00129h			
0012Ah			
0012Bh			
0012Ch			
0012Dh			
0012Eh			
0012Fh			
00130h	Timer RE Second Data Register	TRESEC	XXXXXXXXb
	Timer RE Counter Data Register	TRECNT	
00131h	Timer RE Minute Data Register	TREMIN	XXXXXXXXb
	Timer RE Compare Data Register		
00132h	Timer RE Hour Data Register	TREHR	00XXXXXXb
00133h	Timer RE Day-of-the-Week Data Register	TREWK	00000XXXb
00134h	Timer RE Day Data Register	TREDY	00XXXXXXb
00135h	Timer RE Month Data Register	TREMON	000XXXXXb
00136h	Timer RE Year Data Register	TREYR	XXXXXXXXb
00137h	Timer RE Control Register	TRECR	XXX00X0Xb
00138h	Timer RE Count Source Select Register	TRECSR	X0001000b
00139h	Timer RE Clock Error Correction Register	TREADJ	XXXXXXXXb
0013Ah	Timer RE Interrupt Flag Register	TREIFR	00000XXXb
0013Bh	Timer RE Interrupt Enable Register	TREIER	XXXXXXXXb
0013Ch	Timer RE Alarm Minute Register	TREAMN	XXXXXXXXb
0013Dh	Timer RE Alarm Hour Register	TREAHR	XXXXXXXXb
0013Eh	Timer RE Alarm Day-of-the-Week Register	TREAWK	X0000XXXb
0013Fh	Timer RE Protect Register	TREPRC	00000000b

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.6 SFR Information (6) (1)

Address	Register Name	Symbol	After Reset
00140h			
00141h			
00142h			
00143h			
00144h			
00145h			
00146h			
00147h			
00148h			
00149h			
0014Ah			
0014Bh			
0014Ch			
0014Dh			
0014Eh			
0014Fh			
00150h			
00151h			
00152h			
00153h			
00154h			
00155h			
00156h			
00157h			
00158h			
00159h			
0015Ah			
0015Bh			
0015Ch			
0015Dh			
0015Eh			
0015Fh			
00160h	IIC Control Register	IICCR	00001110b
00161h	SS Bit Counter Register	SSBR	11111000b
00162h	SI Transmit Data Register	SITDR	FFh
00163h			FFh
00164h	SI Receive Data Register	SIRDR	FFh
00165h			FFh
00166h	SI Control Register 1	SICR1	00h
00167h	SI Control Register 2	SICR2	01111101b
00168h	SI Mode Register 1	SIMR1	00010000b (2) 00011000b (3)
00169h	SI Interrupt Enable Register	SIER	00h
0016Ah	SI Status Register	SISR	00h
0016Bh	SI Mode Register 2	SIMR2	00h
0016Ch			
0016Dh			
0016Eh			
0016Fh			
00170h			
00171h			
00172h			
00173h			
00174h			
00175h			
00176h			
00177h			
00178h			
00179h			
0017Ah			
0017Bh			
0017Ch			
0017Dh			
0017Eh			
0017Fh			

Notes:
1. The blank areas are reserved. No access is allowed.
2. When the SSU function is used.
3. When the I^2C bus function is used.

Table 3.7 SFR Information (7) (1)

Address	Register Name	Symbol	After Reset
00180h	Comparator B Control Register	WCMPR	00h
00181h	Comparator B1 Interrupt Control Register	WCB1INTR	00h
00182h	Comparator B3 Interrupt Control Register	WCB3INTR	00h
00183h			
00184h			
00185h			
00186h			
00187h			
00188h	Timer RK Mode Register	TMKM	00h
00189h	Timer RK Control Register	TMKCR	00h
0018Ah	Timer RK Load Register	TMKLD (TMKCNT)	00h
0018Bh	Timer RK Compare Match Data Register	TMKCMP	00h
0018Ch	Timer RK Interrupt Request and Status Register	TMKIR	00h
0018Dh			
0018Eh			
0018Fh			
00190h	UART1 Transmit/Receive Mode Register	U1MR	00h
00191h	UART1 Bit Rate Register	U1BRG	XXh
00192h	UART1 Transmit Buffer Register	U1TBL	XXh
00193h		U1TBH	XXh
00194h	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00195h	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00196h	UART1 Receive Buffer Register	U1RBL	XXh
00197h		U1RBH	XXh
00198h	UART1 Interrupt Flag and Enable Register	U1IR	00h
00199h			
0019Ah			
0019Bh			
0019Ch	IrDA Control Register	IRCR	00h
0019Dh			
0019Eh			
0019Fh			
001A0h			
001A1h			
001A2h			
001A3h			
001A4h			
001A5h			
001A6h			
001A7h			
001A8h			
001A9h	Flash Memory Status Register	FST	10000000b
001AAh	Flash Memory Control Register 0	FMR0	00h
001ABh	Flash Memory Control Register 1	FMR1	00h
001ACh	Flash Memory Control Register 2	FMR2	00h
001ADh	Flash Memory Refresh Control Register	FREFR	00h
001AEh			
001AFh			
001B0h			
001B1h			
001B2h			
001B3h			
001B4h			
001B5h			
001B6h			
001B7h			
001B8h			
001B9h			
001BAh			
001BBh			
001BCh			
001BDh			
001BEh			
001BFh			

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.8 SFR Information (8) (1)

Address	Register Name	Symbol	After Reset
001C0h	Address Match Interrupt Register 0	AIADR0L	00h
001C1h		AIADR0M	00h
001C2h		AIADR0H	00h
001C3h	Address Match Interrupt Enable Register 0	AIEN0	00h
001C4h	Address Match Interrupt Register 1	AIADR1L	00h
001C5h		AIADR1M	00h
001C6h		AIADR1H	00h
001C7h	Address Match Interrupt Enable Register 1	AIEN1	00h
001C8h			
001C9h			
001CAh			
001CBh			
001CCh			
001CDh			
001CEh			
001CFh			
001D0h			
001D1h			
001D2h			
001D3h			
001D4h			
001D5h			
001D6h			
001D7h			
001D8h			
001D9h			
001DAh			
001DBh			
001DCh			
001DDh			
001DEh			
001DFh			
001E0h			
001E1h			
001E2h			
001E3h			
001E4h			
001E5h			
001E6h			
001E7h			
001E8h			
001E9h			
001EAh			
001EBh			
001ECh			
001EDh			
001EEh			
001EFh			
001F0h			
001F1h			
001F2h			
001F3h			
001F4h			
001F5h			
001F6h			
001F7h			
001F8h			
001F9h			
001FAh			
001FBh			
001FCh			
001FDh			
001FEh			
001FFh			

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.9 ID Code Area and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
0FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
0FFDFh	ID1		(Note 2)
:			
0FFE3h	ID2		(Note 2)
:			
0FFEBh	ID3		(Note 2)
:			
0FFEFh	ID4		(Note 2)
:			
0FFF3h	ID5		(Note 2)
:			
0FFF7h	ID6		(Note 2)
:			
0FFFBh	ID7		(Note 2)
:			
0FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the option function select area. Erasure of the block including the option function select area causes the option function select area to be set to FFh.
   When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the ID code area. Erasure of the block including the ID code area causes the ID code area to be set to FFh.
   When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
   When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

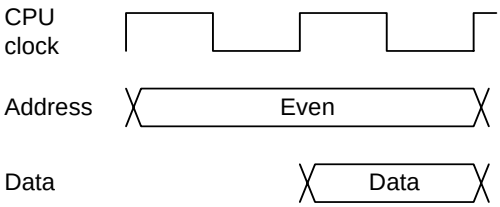
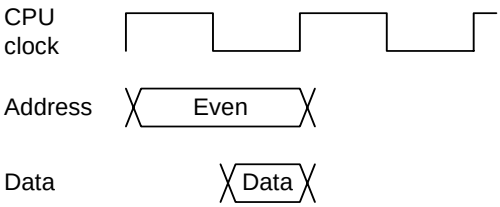
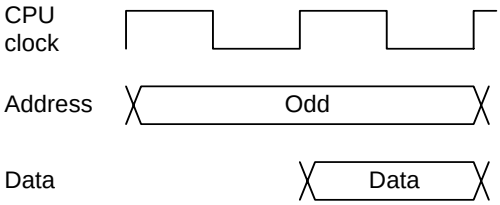
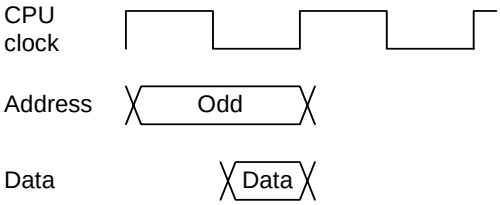
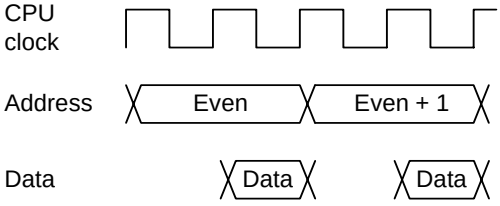
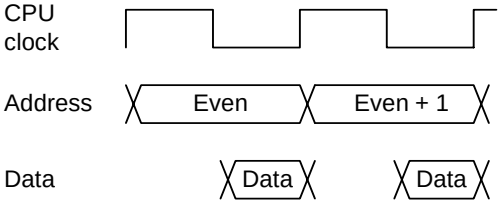
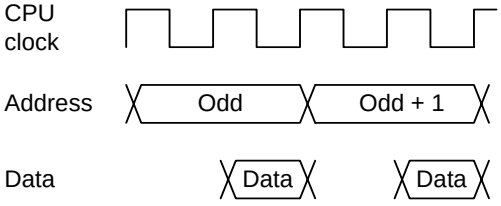
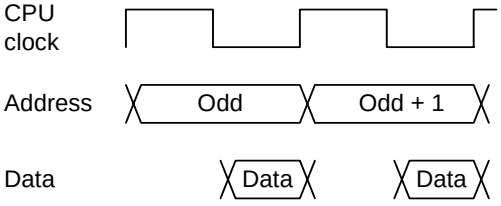
4. Bus Control

The number of bus cycles differ depending on the area accessed: ROM, RAM, or SFR.
Table 4.1 lists the Number of Bus Cycles for Accessing Different Areas. Table 4.2 lists the Access Units and Bus Operations.
The units for SFR access are specified as “Access Size” in the register configuration table in each chapter.
The peripheral function modules are connected to the CPU via an 8-bit bus. Thus, when these areas are accessed as word (16-bit) units, they are accessed twice in 8-bit units.

Table 4.1 Number of Bus Cycles for Accessing Different Areas

Access Area	Bus Cycle
ROM (data flash)	2 cycles of CPU clock
SFR (other than FMR2 register)	
SFR (FMR2 register)	6 cycles of CPU clock
ROM (program ROM)	1 cycle of CPU clock
RAM	

Table 4.2 Access Units and Bus Operations

Area	ROM (data flash), SFR	ROM (program ROM), RAM
Even address byte access		
Odd address byte access		
Even address word access		
Odd address word access		

5. System Control

5.1 Overview

This chapter describes system control functions, such as ID code checking, register access protection, and option functions.

5.2 Registers

Table 5.1 lists the Register Configuration for System Control.

Table 5.1 Register Configuration for System Control

Register Name	Symbol	After Reset	Address	Access Size
Processor Mode Register 0	PM0	00h	00010h	8
Module Standby Control Register	MSTCR	(Note 1)	00012h	8
Protect Register	PRCR	00h	00013h	8
Hardware Reset Protect Register	HRPR	00h	00016h	8
Module Standby Control Register 1	MSTCR1	(Note 1)	00017h	8
Reset Source Determination Register	RSTFR	(Note 2)	0005Fh	8
Option Function Select Register 2	OFS2	(Note 3)	0FFDBh	8
Option Function Select Register	OFS	(Note 4)	0FFFFh	8

Notes:
1. See the description of the individual registers.
2. The value of the RSTFR register after a reset differs depending on the reset source. For details, see **5.2.6 Reset Source Determination Register (RSTFR)**.
3. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS2 register. Erasure of the block including the OFS2 register causes the OFS2 register to be set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.
4. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS register. Erasure of the block including the OFS register causes the OFS register to be set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.

5.2.1 Processor Mode Register 0 (PM0)

Address 00010h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	SRST	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	SRST	Software reset bit	0: State is retained 1: Reset is generated	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

SRST Bit (Software reset bit)

When the SRST bit is set to 1, the entire MCU is reset. The read value is 0. For details, see **6. Resets**.

5.2.2 Module Standby Control Register (MSTCR)

Address 00012h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	MSTUART0	MSTTRC	MSTAD	—	MSTTRE	MSTTRB	MSTTRJ
After Reset	0	0	0	0	0	0	0	0

The above applies when the MSTINI bit in the OFS2 register is 0.

After Reset	0	1	1	1	0	1	1	1

The above applies when the MSTINI bit in the OFS2 register is 1.

Bit	Symbol	Bit Name	Function	R/W
b0	MSTTRJ	Timer RJ2 standby bit	0: Active 1: Standby (1)	R/W
b1	MSTTRB	Timer RB2 standby bit	0: Active 1: Standby (2)	R/W
b2	MSTTRE	Timer RE2 standby bit	0: Active 1: Standby (3)	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	MSTAD	A/D converter standby bit	0: Active 1: Standby (4)	R/W
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (5)	R/W
b6	MSTUART0	UART0 standby bit	0: Active 1: Standby (6)	R/W
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

Notes:

1. When the MSTTRJ bit is set to 1 (standby), access to the registers associated with timer RJ2 (addresses 000D8h to 000DEh) is disabled.
2. When the MSTTRB bit is set to 1 (standby), access to the registers associated with timer RB2 (addresses 000E0h to 000E7h) is disabled.
3. When the MSTTRE bit is set to 1 (standby), access to the registers associated with timer RE2 (addresses 00130h to 0013Fh) is disabled.
4. When the MSTAD bit is set to 1 (standby), access to the registers associated with the A/D converter (addresses 00098h to 0009Fh) is disabled.
5. When the MSTTRC bit is set to 1 (standby), access to the registers associated with timer RC (addresses 000E8h to 000FCh) is disabled.
6. When the MSTUART0 bit is set to 1 (standby), access to the registers associated with UART0 (addresses 00080h to 00088h) is disabled.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand.

5.2.3 Protect Register (PRCR)

Address 00013h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	PRC4	PRC3	—	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Writing to registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2 0: Disabled 1: Enabled (1)	R/W
b1	PRC1	Protect bit 1	Writing to registers PM0 and RISR 0: Disabled 1: Enabled (1)	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	PRC3	Protect bit 3	Writing to registers VCA2, VD1LS, VW0C, and VW1C 0: Disabled 1: Enabled (1)	R/W
b4	PRC4	Protect bit 4	Writing to the PINSR register 0: Disabled 1: Enabled (1)	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

Note:
1. Once this bit is set to 1, writing remains enabled until it is set to 0 by a program.

5.2.4 Hardware Reset Protect Register (HRPR)

Address 00016h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	PAMCRE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PAMCRE	PAMCR register write enable bit (1)	0: Write disabled 1: Write enabled	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. To set this bit to 1, first write 0 and then write 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.

PAMCRE Bit (PAMCR register write enable bit)

[Condition for setting to 0]
• When 0 is written to this bit.
[Condition for setting to 1]
• When 0 and then 1 is written to this bit.

5.2.5 Module Standby Control Register 1 (MSTCR1)

Address 00017h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	MSTUART1	MSTTRK	—	MSTICSU	MSTIRDA
After Reset	0	0	0	0	0	0	0	0

The above applies when the MSTINT bit in the OFS2 register is 0.

After Reset	1	1	1	1	1	1	1	1

The above applies when the MSTINT bit in the OFS2 register is 1.

Bit	Symbol	Bit Name	Function	R/W
b0	MSTIRDA	IrDA standby bit	0: Active 1: Standby (1)	R/W
b1	MSTICSU	SSU/I^{2}C bus standby bit	0: Active 1: Standby (2)	R/W
b2	—	Reserved	Set to 1. The read value is undefined.	R/W
b3	MSTTRK	Timer RK standby bit	0: Active 1: Standby (3)	R/W
b4	MSTUART1	UART1 standby bit	0: Active 1: Standby (4)	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

Notes:
1. When the MSTIRDA bit is set to 1 (standby), access to the register associated with IrDA (address 0019Ch) is disabled.
2. When the MSTICSU bit is set to 1 (standby), access to the registers associated with SSU/I^{2}C bus (addresses 00160h to 0016Bh) is disabled.
3. When the MSTTRK bit is set to 1 (standby), access to the registers associated with timer RK (addresses 00188h to 0018Ch) is disabled.
4. When the MSTUART1 bit is set to 1 (standby), access to the registers associated with UART1 (addresses 00190h to 00198h) is disabled.

When changing each standby bit to standby, stop the corresponding peripheral function beforehand.

5.2.6 Reset Source Determination Register (RSTFR)

Address 0005Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDR	SWR	HWR	CWR
After Reset	0	0	0	0	(Note 1)	(Note 1)	(Note 1)	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. The value after a reset differs depending on the reset source.

CWR Bit (Cold start-up/warm start-up determine flag)

This flag indicates whether a cold start-up or warm start-up has occurred. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.
The CWR bit is set to 1 by writing 1 by a program, but writing 0 to this bit has no effect.

[Condition for setting to 0]
• When a reset occurs after power-on or voltage detection 0.
[Condition for setting to 1]
• When 1 is written to this bit by a program.

HWR Bit (Hardware reset detect flag)

This flag indicates that a hardware reset has occurred.

[Condition for setting to 0]
• When a software reset, watchdog timer reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a hardware reset occurs.

SWR Bit (Software reset detect flag)

This flag indicates that a reset has been generated by software.

[Condition for setting to 0]
• When a watchdog timer reset, hardware reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a software reset occurs.

WDR Bit (Watchdog timer reset detect flag)

This flag indicates that a reset has been generated by the watchdog timer.

[Condition for setting to 0]
• When a software reset, hardware reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a watchdog timer reset occurs.

5.2.7 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTINI	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period setting bits	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acceptance period setting bits	b3 b2 0 0: 25 % 0 1: 50 % 1 0: 75 % 1 1: 100 %	R/W
b3	WDTRCS1			R/W
b4	—	Reserved	Set to 1.	R/W
b5	MSTINI	MSTCR register initial value select bit	0: MSTCR register is set to 00h and MSTCR1 register is set to 00h after reset 1: MSTCR register is set to 77h and MSTCR1 register is set to FFh after reset	R/W
b6	—	Reserved	Set to 1.	R/W
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS2 register. Erasure of the block including the OFS2 register causes the OFS2 register to be set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For an example of the OFS2 register settings, see **5.6.1 Option Function Select Area Setting Example**.

Bits WDTUFS0 to WDTUFS1 (Watchdog timer underflow period setting bits)

These bits are used to select the underflow period for the watchdog timer.

Bits WDTRCS0 to WDTRCS1 (Watchdog timer refresh acceptance period setting bits)

These bits are used to select the refresh acceptance period as a percentage. Note that the period from the start of counting to underflow is 100 %.
For details, see **8.3.1.1 Refresh Acceptance Period**.

5.2.8 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer is automatically started after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bits	b5 b4 0 0: 3.80 V (typ.) selected (Vdet0_3) 0 1: 2.85 V (typ.) selected (Vdet0_2) 1 0: 2.35 V (typ.) selected (Vdet0_1) 1 1: 1.90 V (typ.) selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Note:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS register. Erasure of the block including the OFS register causes the OFS register to be set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.

   For an example of the OFS register settings, see **5.6.1 Option Function Select Area Setting Example**.

WDTON Bit (Watchdog timer start select bit)

This bit is used to select whether the watchdog timer is automatically started after a reset is cleared.

Bits VDSEL0 to VDSEL1 (Voltage detection 0 level select bits)

These bits are used to select the detection level (Vdet0) for voltage monitor 0 reset. The same level of the voltage detection 0 level selected by bits VDSEL0 to VDSEL1 is set in both the voltage monitor 0 reset and power-on reset functions.

LVDAS Bit (Voltage detection 0 circuit start bit)

This bit is used to select whether voltage monitor 0 reset is enabled. Set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset) to use the power-on reset.

CSPROINI Bit (Count source protection mode after reset select bit)

This bit is used to select whether to protect the count source for the watchdog timer from being changed.

5.3 ID Code Check Function

The ID code check function prevents the flash memory from being read, rewritten, or erased when standard serial I/O mode is used. This function is realized by examination of the ID codes written in the ID code area.
For details, see **23.3 ID Code Check Function**.

5.4 Register Access Protect Function

The protection function protects important registers from being easily rewritten if a program runs out of control.
Table 5.2 lists the PRCR Register Bits and Registers Protected.
For details on each bit, see **5.2.3 Protect Register (PRCR)**.

Table 5.2 PRCR Register Bits and Registers Protected

Bit	Registers Protected
PRC0	Registers EXCKCR, OCOCR, SCKCR, PHISEL, CKSTPR, CKRSCR, BAKCR, FRV1, and FRV2
PRC1	Registers PM0 and RISR
PRC3	Registers VCA2, VD1LS, VW0C, and VW1C
PRC4	PINSR register

Table 5.3 lists the HRPR Register Bit and Register Protected.
For details on each bit, see **5.2.4 Hardware Reset Protect Register (HRPR)**.

Table 5.3 HRPR Register Bit and Register Protected

Bit	Registers Protected
PAMCRE	PAMCR register

5.5 Option Functions

The option functions allow the user to select the MCU state after a reset is cleared. Table 5.4 lists the Option Functions.

The option functions can be selected by registers OFS2 and OFS. These registers are allocated at the addresses 0FFFFh (highest of the reset vector) and 0FFDBh, as shown in Figure 5.1.

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

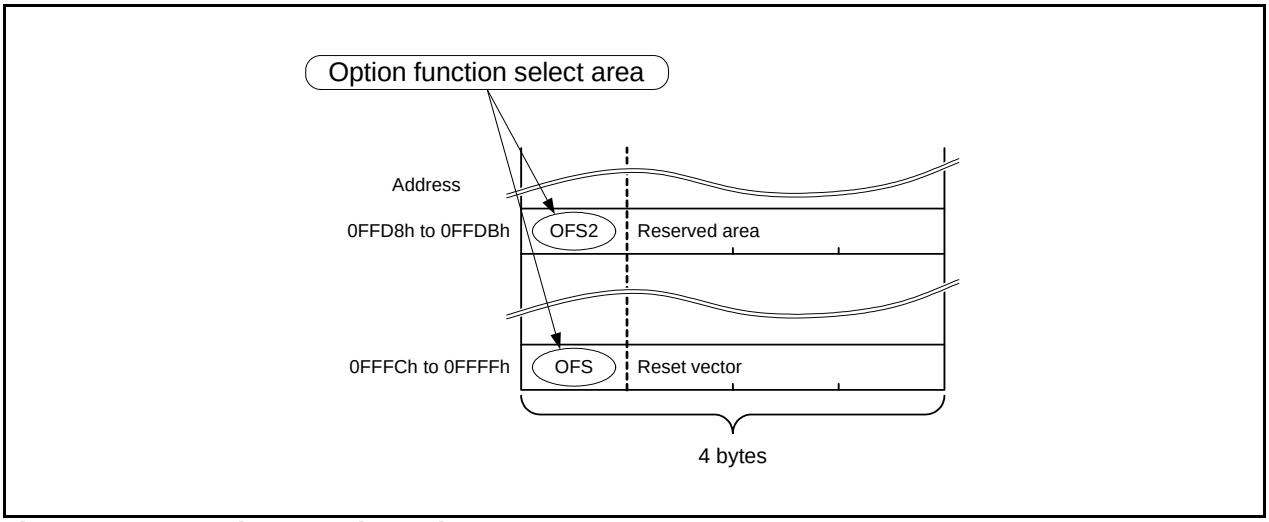


Figure 5.1 Option Function Select Area

Table 5.4 Option Functions

Option Function Name		Register Name	Bit Name	Reference
Watchdog timer	Start select function	OFS register	WDTON bit	8. Watchdog Timer
	Count source protection select function		CSPROINI bit	
	Underflow period select function	OFS2 register	Bits WDTUFS0 to WDTUFS1	
	Refresh acceptance period select function		Bits WDTRCS0 to WDTRCS1	
Voltage detection circuit	Voltage monitor 0 reset level function	OFS register	Bits VDSEL0 to VDSEL1	6. Resets 7. Voltage Detection Circuit
	Voltage monitor 0 reset start select function		LVDAS bit	
Flash memory	ROM code protection function		Bits ROMCR to ROMCP1	23. Flash Memory

5.6 Notes on System Control

5.6.1 Option Function Select Area Setting Example

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

• To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

Programming formats vary depending on the compiler. Check the compiler manual.

• To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)          ; RESET
```

Programming formats vary depending on the compiler. Check the compiler manual.

6. Resets

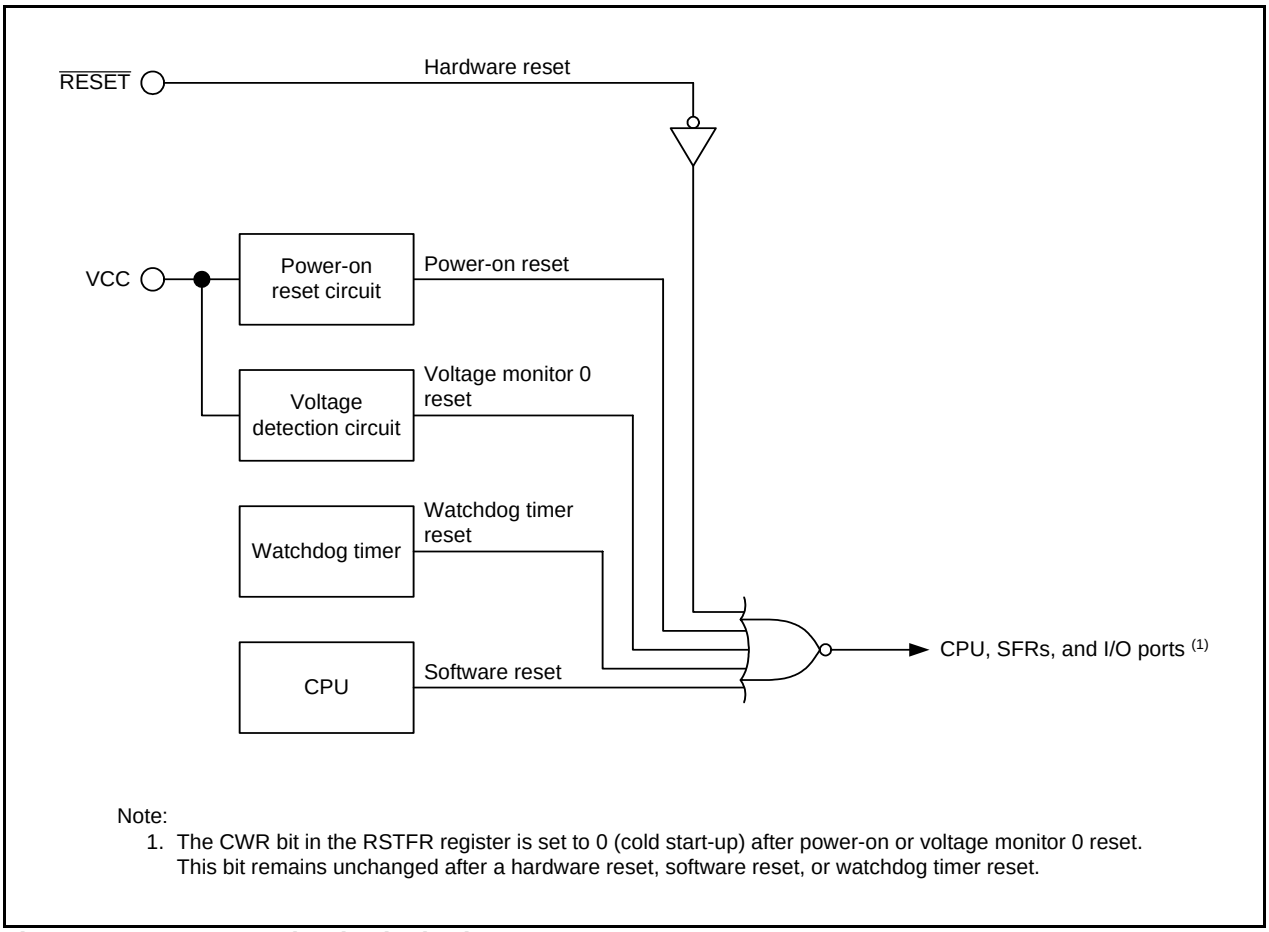
The following resets are provided: hardware reset, power-on reset, voltage monitor 0 reset triggered by the voltage detection circuit, watchdog timer reset, and software reset.

6.1 Overview

Table 6.1 lists the Reset Names and Sources. Figure 6.1 shows the Reset Circuit Block Diagram.

Table 6.1 Reset Names and Sources

Reset Name	Source
Hardware reset	When a low level is input to the $\overline{\text{RESET}}$ pin.
Power-on reset	When VCC is turned on.
Voltage monitor 0 reset	When VCC decreases below Vdet0, which is detected by voltage detection circuit 0.
Watchdog timer reset	When the watchdog timer underflows.
Software reset	When 1 is written to the SRST bit in the PM0 register by a program.



Note:
1. The CWR bit in the RSTFR register is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.

Figure 6.1 Reset Circuit Block Diagram

6.2 Registers

Table 6.2 lists the Register Configuration for Reset.

Table 6.2 Register Configuration for Reset

Register Name	Symbol	After Reset	Address	Access Size
Processor Mode Register 0	PM0	00h	00010h	8
Reset Source Determination Register	RSTFR	(Note 1)	0005Fh	8
Option Function Select Register 2	OFS2	(Note 2)	0FFDBh	8
Option Function Select Register	OFS	(Note 3)	0FFFFh	8

Notes:
1. The value of the RSTFR register after a reset differs depending on the reset source. For details, see **6.2.2 Reset Source Determination Register (RSTFR)**.
2. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS2 register. Erasure of the block including the OFS2 register causes the OFS2 register to be set to FFh.
   The value of the OFS2 register is FFh at shipment of blank products. After programming, the value is the same as that programmed by the user.
   At shipment of factory-programmed products, the value of the OFS2 register is the same as that set in a program by the user.
3. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS register. Erasure of the block including the OFS register causes the OFS register to be set to FFh.
   The value of the OFS register is FFh at shipment of blank products. After programming, the value is the same as that programmed by the user.
   At shipment of factory-programmed products, the value of the OFS register is the same as that set in a program by the user.

6.2.1 Processor Mode Register 0 (PM0)

Address 00010h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	SRST	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	SRST	Software reset bit	0: State is retained 1: Reset is generated	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

SRST Bit (Software reset bit)

When the SRST bit is set to 1, the entire MCU is reset. The read value is 0. For details, see **6. Resets**.

6.2.2 Reset Source Determination Register (RSTFR)

Address 0005Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDR	SWR	HWR	CWR
After Reset	0	0	0	0	(Note 1)	(Note 1)	(Note 1)	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. The value after a reset differs depending on the reset source.

CWR Bit (Cold start-up/warm start-up determine flag)

This flag indicates whether a cold start-up or warm start-up has occurred. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.
The CWR bit is set to 1 by writing 1 by a program, but writing 0 to this bit has no effect.

[Condition for setting to 0]
• When a reset occurs after power-on or voltage detection 0.
[Condition for setting to 1]
• When 1 is written to this bit by a program.

HWR Bit (Hardware reset detect flag)

This flag indicates that a hardware reset has occurred.

[Condition for setting to 0]
• When a software reset, watchdog timer reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a hardware reset occurs.

SWR Bit (Software reset detect flag)

This flag indicates that a reset has been generated by software.

[Condition for setting to 0]
• When a watchdog timer reset, hardware reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a software reset occurs.

WDR Bit (Watchdog timer reset detect flag)

This flag indicates that a reset has been generated by the watchdog timer.

[Condition for setting to 0]
• When a software reset, hardware reset, power-on reset, or voltage monitor 0 reset occurs.
[Condition for setting to 1]
• When a watchdog timer reset occurs.

6.2.3 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTINI	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period setting bits	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acceptance period setting bits	b3 b2 0 0: 25 % 0 1: 50 % 1 0: 75 % 1 1: 100 %	R/W
b3	WDTRCS1			R/W
b4	—	Reserved	Set to 1.	R/W
b5	MSTINI	MSTCR register initial value select bit	0: MSTCR register is set to 00h and MSTCR1 register is set to 00h after reset 1: MSTCR register is set to 77h and MSTCR1 register is set to FFh after reset	R/W
b6	—	Reserved	Set to 1.	R/W
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS2 register. Erasure of the block including the OFS2 register causes the OFS2 register to be set to FFh.
   When blank products are shipped, the OFS2 register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS2 register is the value programmed by the user.

   For an example of the OFS2 register settings, see **5.6.1 Option Function Select Area Setting Example**.

Bits WDTUFS0 to WDTUFS1 (Watchdog timer underflow period setting bits)

These bits are used to select the underflow period for the watchdog timer.

Bits WDTRCS0 to WDTRCS1 (Watchdog timer refresh acceptance period setting bits)

These bits are used to select the refresh acceptance period as a percentage. Note that the period from the start of counting to underflow is 100 %.
For details, see **8.3.1.1 Refresh Acceptance Period**.

6.2.4 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer is automatically started after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bits	b5 b4 0 0: 3.80 V (typ.) selected (Vdet0_3) 0 1: 2.85 V (typ.) selected (Vdet0_2) 1 0: 2.35 V (typ.) selected (Vdet0_1) 1 1: 1.90 V (typ.) selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Note:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not perform an additional write to the OFS register. Erasure of the block including the OFS register causes the OFS register to be set to FFh.
   When blank products are shipped, the OFS register is set to FFh. It is set to the written value after written by the user.
   When factory-programming products are shipped, the value of the OFS register is the value programmed by the user.

   For an example of the OFS register settings, see **5.6.1 Option Function Select Area Setting Example**.

WDTON Bit (Watchdog timer start select bit)

This bit is used to select whether the watchdog timer is automatically started after a reset is cleared.

Bits VDSEL0 to VDSEL1 (Voltage detection 0 level select bits)

These bits are used to select the detection level (Vdet0) for voltage monitor 0 reset. The same level of the voltage detection 0 level selected by bits VDSEL0 to VDSEL1 is set in both the voltage monitor 0 reset and power-on reset functions.

LVDAS Bit (Voltage detection 0 circuit start bit)

This bit is used to select whether voltage monitor 0 reset is enabled. Set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset) to use the power-on reset.

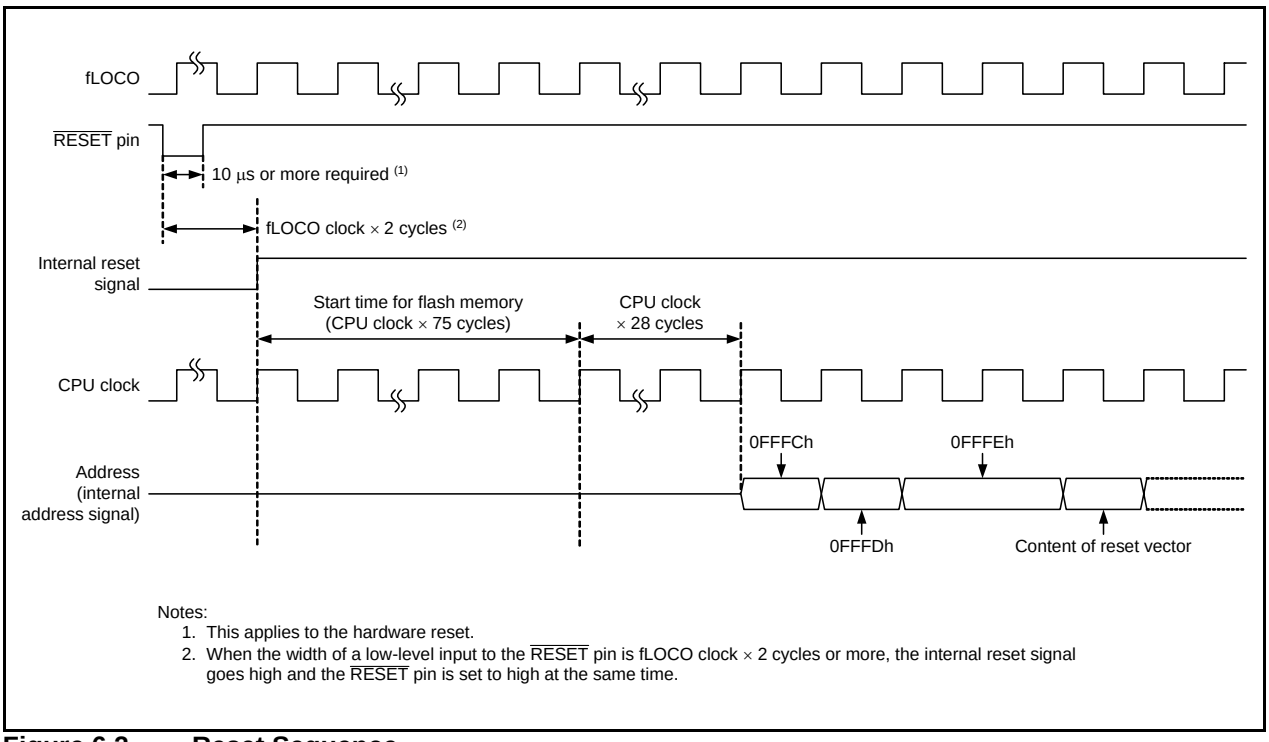
CSPROINI Bit (Count source protection mode after reset select bit)

This bit is used to select whether to protect the count source for the watchdog timer from being changed.

6.3 Operation

6.3.1 Reset Sequence

Figure 6.2 shows the Reset Sequence using a hardware reset as an example. When the internal reset signal is cleared, the CPU starts operation from the reset vector (addresses 0FFFCh to 0FFFEh) after a predetermined time has elapsed.



Notes:
1. This applies to the hardware reset.
2. When the width of a low-level input to the RESET pin is fLOCO clock × 2 cycles or more, the internal reset signal goes high and the RESET pin is set to high at the same time.

Figure 6.2 Reset Sequence

6.3.2 Hardware Reset

The hardware reset is the reset that is caused by the $\overline{\text{RESET}}$ pin. When a low level is input to the $\overline{\text{RESET}}$ pin under the condition that the power supply voltage meets the recommended operating conditions, the CPU, SFRs, and I/O ports are initialized. See **3.2 Special Function Registers (SFRs)** for the states of the SFRs after a reset, and **Table 6.3 Pin States** for the states of I/O ports.

The internal RAM is not initialized. If the $\overline{\text{RESET}}$ pin is set to low while writing to the internal RAM, the RAM values will be undefined.

When the $\overline{\text{RESET}}$ pin is changed from low to high, a program is executed starting at the address indicated by the reset vector. The low-speed on-chip oscillator clock (no division) is automatically selected as the CPU clock after a reset.

Figure 6.3 shows the Hardware Reset Circuit Example (Using External Power Supply Voltage Detection Circuit) and Operation.

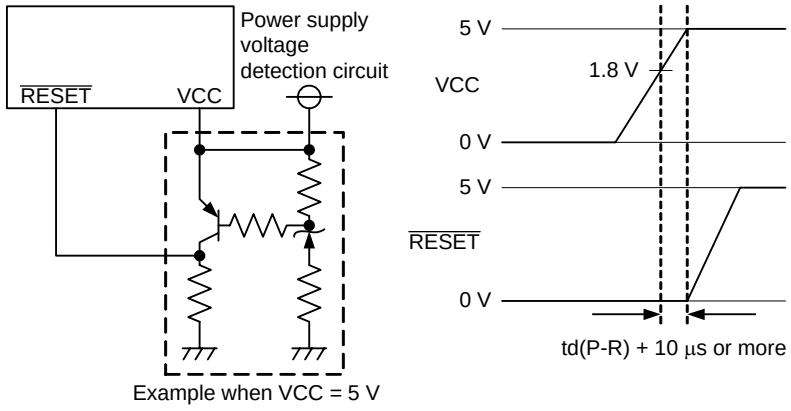
The $\overline{\text{RESET}}$ pin is multiplexed with port PA_0, so it can be used as general-purpose I/O ports when not used for a hardware reset. For details, see **12.13.1 Notes on RESET/PA_0 Pin**.

6.3.2.1 When Power Supply is Stable

(1) Input a low level to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10 µs.
(3) Input a high level to the $\overline{\text{RESET}}$ pin.

6.3.2.2 When Power Supply is Turned on

(1) Input a low level to the $\overline{\text{RESET}}$ pin.
(2) Let the power supply voltage increase until it meets the recommended operating conditions.
(3) Wait for td(P-R) until the internal power supply is stabilized (see **24. Electrical Characteristics**).
(4) Wait for 10 µs.
(5) Input a high level to the $\overline{\text{RESET}}$ pin.



Note:
1. See **24. Electrical Characteristics**.

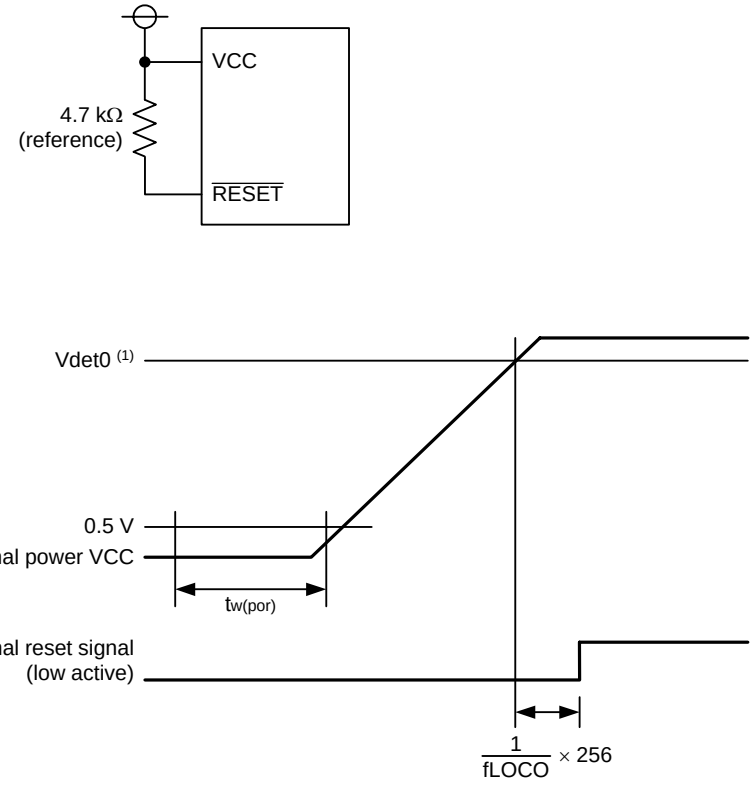
Figure 6.3 Hardware Reset Circuit Example (Using External Power Supply Voltage Detection Circuit) and Operation

6.3.3 Power-On Reset

When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a resistor and the VCC pin voltage level rises, the power-on reset is activated and the CPU, SFRs, and I/O ports are initialized. The internal RAM values will be undefined. In addition, when a capacitor is connected to the $\overline{\text{RESET}}$ pin, assure that the voltage applied to the $\overline{\text{RESET}}$ pin is always 0.8 VCC or more. When using the $\overline{\text{RESET}}$ pin as an I/O port, see **12.13.1 Notes on $\overline{\text{RESET}}$/PA_0 Pin**.

When the input voltage to the VCC pin reaches Vdet0 or above, counting of the low-speed on-chip oscillator clock starts. When the low-speed on-chip oscillator clock count reaches 256, the internal reset signal goes high and the MCU proceeds to the reset sequence (see Figure 6.2). The low-speed on-chip oscillator clock (no division) is automatically selected as the CPU clock after a reset. For the states of the SFRs after a power-on reset, see **3.2 Special Function Registers (SFRs)**. To use the power-on reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled) and enable the voltage monitor 0 reset.

Figure 6.4 shows the Power-On Reset Circuit Example and Operation.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. For details, see **7. Voltage Detection Circuit**.
2. For details on the electrical characteristics, see **24. Electrical Characteristics**.
3. To use the power-on reset, enable the voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 6.4 Power-On Reset Circuit Example and Operation

6.3.4 Voltage Monitor 0 Reset

The voltage monitor 0 reset is due to the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the voltage applied to the VCC pin. Vdet0 is the detection level. The Vdet0 level is set with bits VDSEL0 to VDSEL1 in the OFS register.

When the input voltage to the VCC pin falls to the Vdet0 level or lower, the CPU, SFRs and I/O ports are initialized. The internal RAM is not initialized. If the supply voltage falls to Vdet0 or lower while writing to the internal RAM, the RAM values will be undefined.

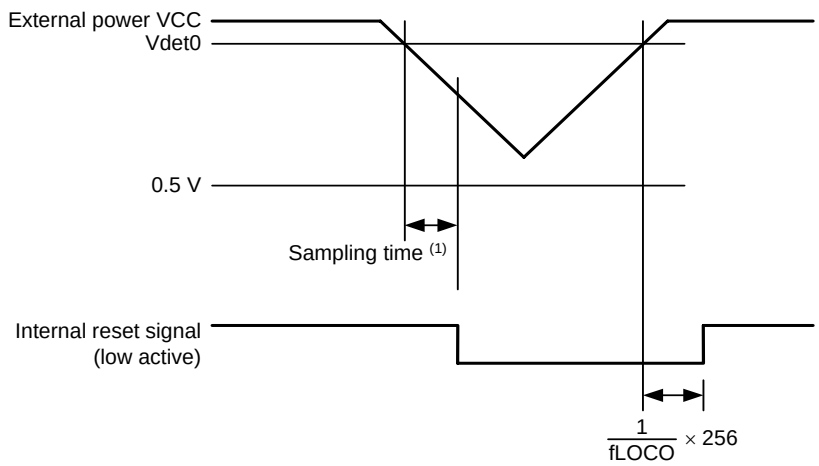
When the voltage applied to the VCC pin next rises to the Vdet0 level or higher, counting of the low-speed on-chip oscillator clock starts. When the low-speed on-chip oscillator clock count reaches 256, the internal reset signal goes high and the MCU proceeds to the reset sequence (see Figure 6.2). The low-speed on-chip oscillator clock (no division) is automatically selected as the CPU clock after a reset.

The LVDAS bit in the OFS register can be used to enable or disable the voltage monitor 0 reset after a reset. The setting of the LVDAS bit is valid at all resets.

Bits VDSEL0 to VDSEL1, and LVDAS cannot be changed by a program. To change these bits, write values to b4 to b6 at address 0FFFFh using a flash programmer. For details on the OFS register, see **6.2.4 Option Function Select Register (OFS)**.

For details on the voltage monitor 0 reset, see **7. Voltage Detection Circuit**.

Figure 6.5 shows an Example of Voltage Monitor 0 Reset Operation.



Note:
1. The voltage monitor 0 digital filter samples VCC to monitor the voltage. If VCC falls below the operating voltage range (1.8 V or more), the voltage cannot be correctly measured. This factor should be considered when selecting the sampling clock for the digital filter. For details, see **7. Voltage Detection Circuit**.

Figure 6.5 Example of Voltage Monitor 0 Reset Operation

6.3.5 Watchdog Timer Reset

When the RIS bit in the RISR register is 1 (watchdog timer reset enabled), if the watchdog timer underflows or if the WDTR register is written at a time other than the refresh acceptance period, a watchdog timer reset is generated. This reset initializes the CPU, SFRs, and I/O ports. The internal reset signal goes high and the watchdog timer reset is cleared at the same time. The MCU then proceeds to the reset sequence (see Figure 6.2).
The low-speed on-chip oscillator clock (no division) is automatically selected as the CPU clock after a reset.
The internal RAM is not initialized. When the watchdog timer underflows, the RAM values will be undefined.
The underflow period and refresh acceptance period for the watchdog timer are set by bits WDTUFS0 to WDTUFS1 and WDTRCS0 to WDTRCS1 in the OFS2 register, respectively.
For details on the watchdog timer, see **8. Watchdog Timer**.

6.3.6 Software Reset

When the SRST bit in the PM0 register is 1 (reset is generated), the CPU, SFRs, and I/O ports are initialized. Next, the program located at the address indicated by the reset vector is executed. The low-speed on-chip oscillator clock (no division) is automatically selected as the CPU clock after the reset is cleared.
For the states of the SFRs after a software reset, see **3.2 Special Function Registers (SFRs)**.
The internal RAM is not initialized.

6.3.7 Cold Start-Up/Warm Start-Up Determination Function

The CWR bit in the RSTFR register is used to determine whether a cold start-up reset process was initiated at power-on, or whether a warm start-up reset process was initiated during operation.
The CWR bit is set to 0 (cold start-up) at power-on and also set to 0 by a voltage monitor 0 reset. If 1 is written to the CWR bit by a program, it is set to 1. This bit remains unchanged after a hardware reset, software reset, or watchdog timer reset.
The cold start-up/warm stat-up determination function uses the voltage monitor 0 reset.
For the bit settings associated with the voltage monitor 0 reset, see **Table 7.3 Procedure for Setting Bits Associated with Voltage Monitor 0 Reset**.
Figure 6.6 shows an Example of Cold Start-Up/Warm Start-Up Function Operation.

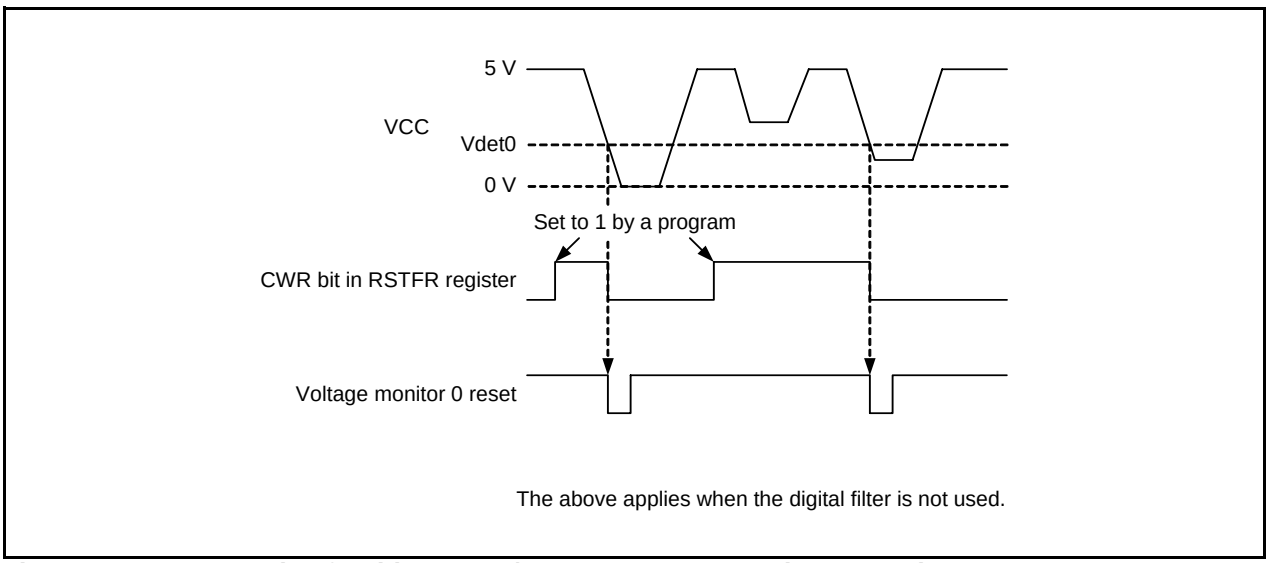


Figure 6.6 Example of Cold Start-Up/Warm Start-Up Function Operation

6.3.8 Reset Source Determination Function

The RSTFR register can be used to detect whether a hardware reset, software reset, or watchdog timer reset has occurred.
If a hardware reset occurs, the HWR bit is set to 1 (detected). If a software reset occurs, the SWR bit is set to 1 (detected). If a watchdog timer reset occurs, the WDR bit is set to 1 (detected).

6.4 States during Reset

6.4.1 Pin States While $\overline{\text{RESET}}$ Pin Level is Low

Table 6.3 lists the Pin States.

Table 6.3 Pin States

Pin Name	Pin Function
P0_0 to P0_7	Input port
P1_0 to P1_7	Input port
P2_0 to P2_2	Input port
P3_1, P3_3 to P3_5, P3_7	Input port
P4_2, P4_5 to P4_7	Input port
PA_0	Input port

6.4.2 CPU Register States After Reset

Figure 6.7 shows the CPU Register States After Reset.

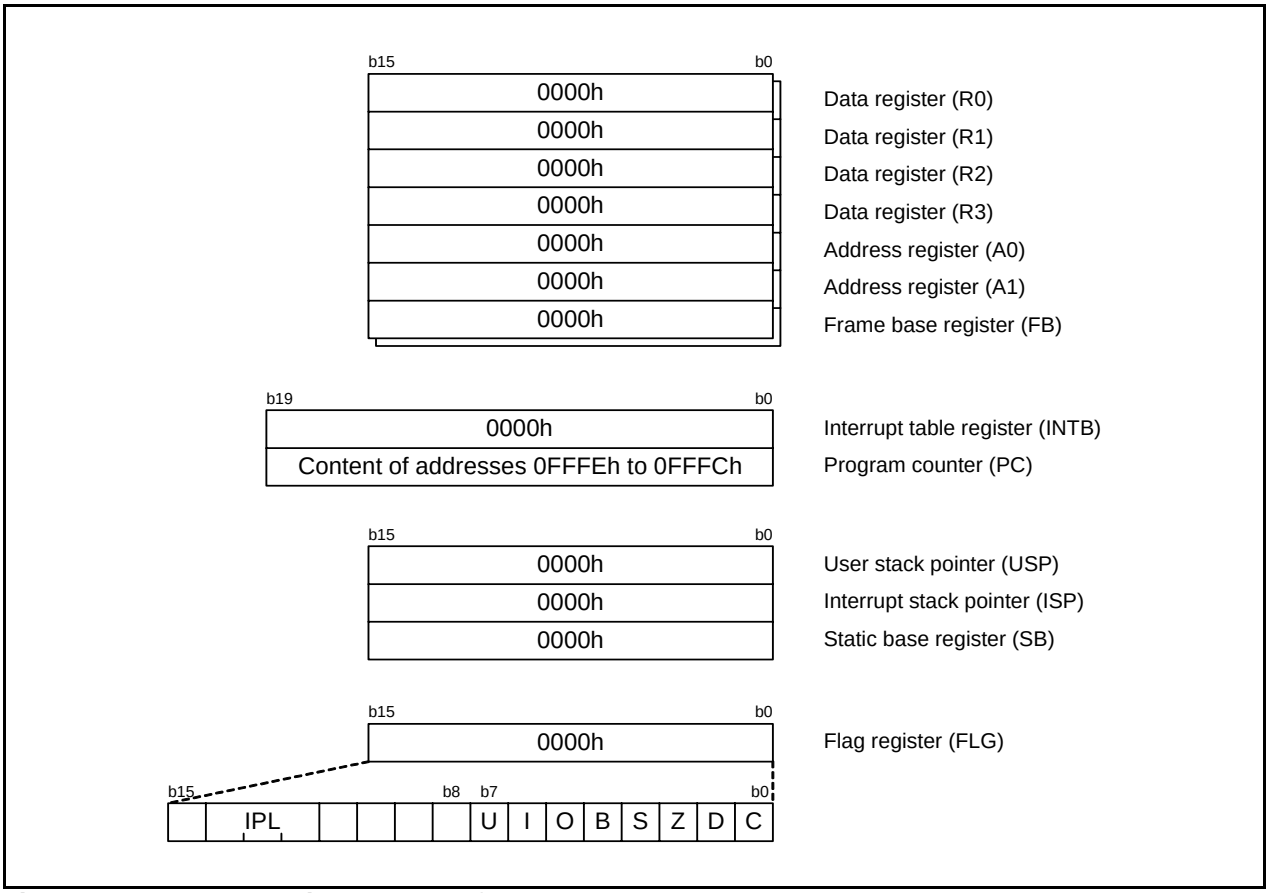


Figure 6.7 CPU Register States After Reset

7. Voltage Detection Circuit

The voltage detection circuit is used to monitor the voltage applied to the VCC pin. The VCC input voltage can be monitored by a program.

7.1 Overview

The detection voltage for voltage detection 0 can be selected from four levels with the OFS register. For details on the OFS register, see **5. System Control**.
The detection voltage for voltage detection 1 can be selected from eight levels with the VD1LS register.
The voltage monitor 0 reset, and voltage monitor 1 interrupt can be used.
Table 7.1 lists the Voltage Detection Circuit Specifications. Figure 7.1 shows the Voltage Detection Circuit Block Diagram. Figure 7.2 shows the Voltage Monitor 0 Reset Generation Circuit Block Diagram. Figure 7.3 shows the Voltage Monitor 1 Interrupt Generation Circuit Block Diagram.

Table 7.1 Voltage Detection Circuit Specifications

Item		Voltage Monitor 0	Voltage Monitor 1
VCC monitor	Voltage to be monitored	Vdet0	Vdet1
	Detection target	Detection by passing down through Vdet0	Detection by passing up or down through Vdet1
	Detection voltage	Selectable from 4 levels with the OFS register	Selectable from 8 levels with the VD1LS register
	Monitor	None	The VW1C3 bit in the VW1C register
			Higher or lower than Vdet1
Process at voltage detection	Reset	Voltage monitor 0 reset	None
		Reset at Vdet0 > VCC, CPU operation is restarted at VCC > Vdet0	
	Interrupts	None	Voltage monitor 1 interrupt
			Interrupt request at Vdet1 > VCC and/or VCC > Vdet1
Digital filter	Switching enable/disable	Available	Available
	Sampling time	(Division of fLOCO by n) × 2 n: 1, 2, 4, or 8	(Division of fLOCO by n) × 2 n: 1, 2, 4, or 8

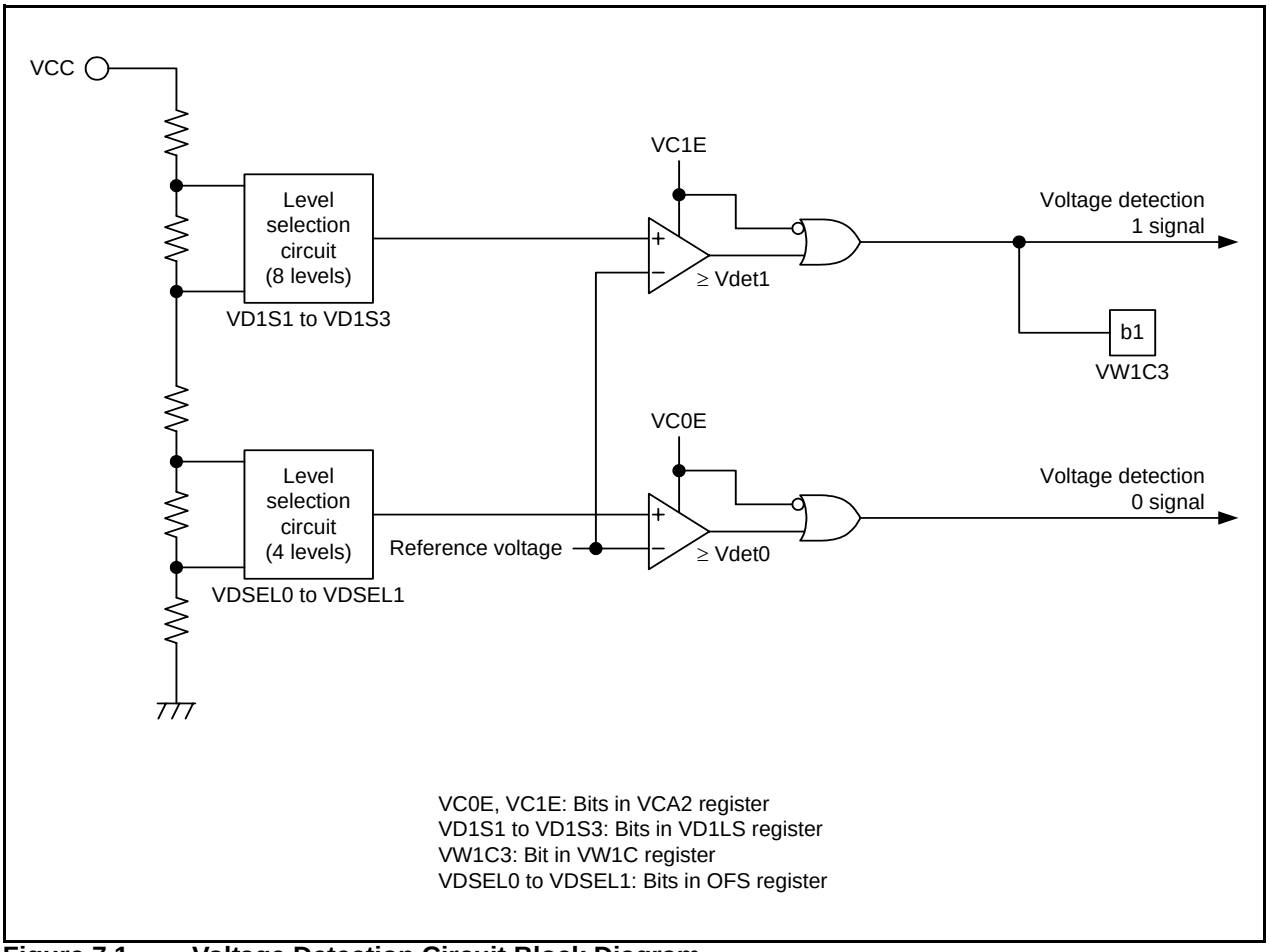
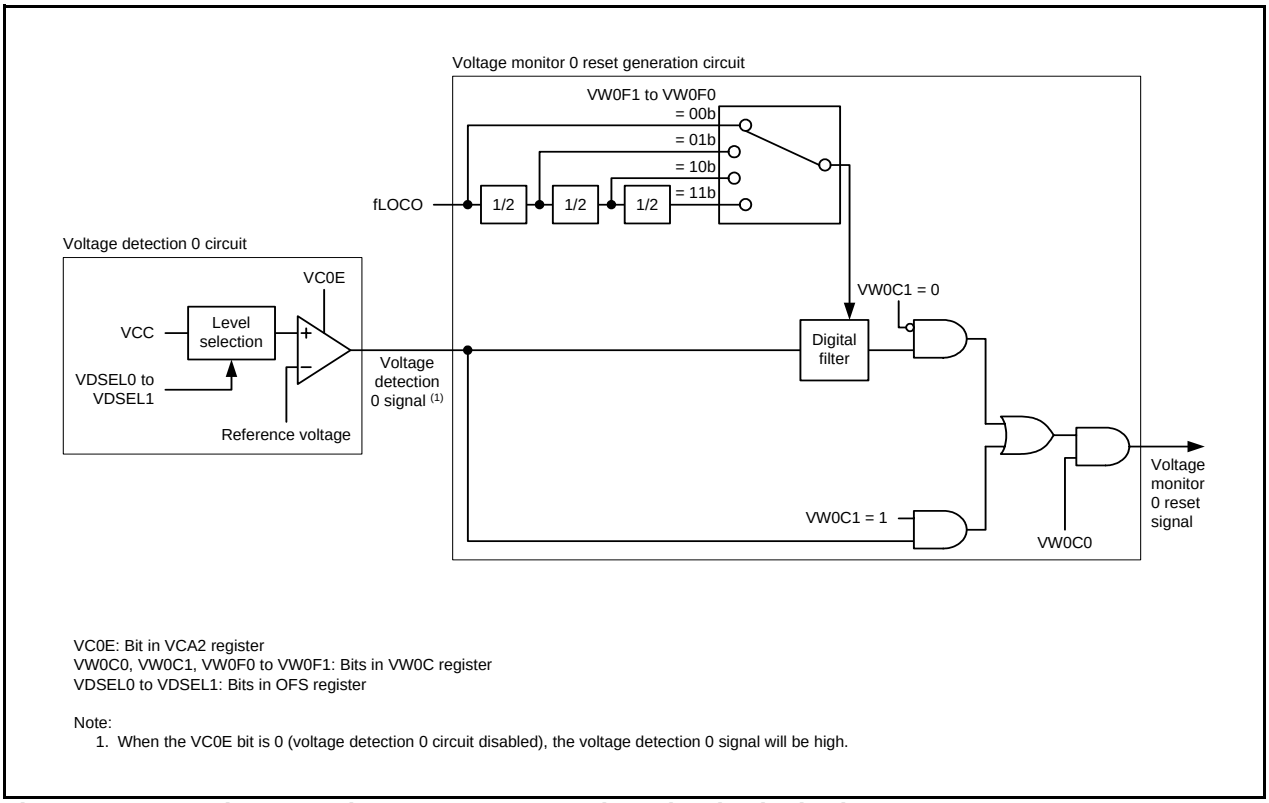


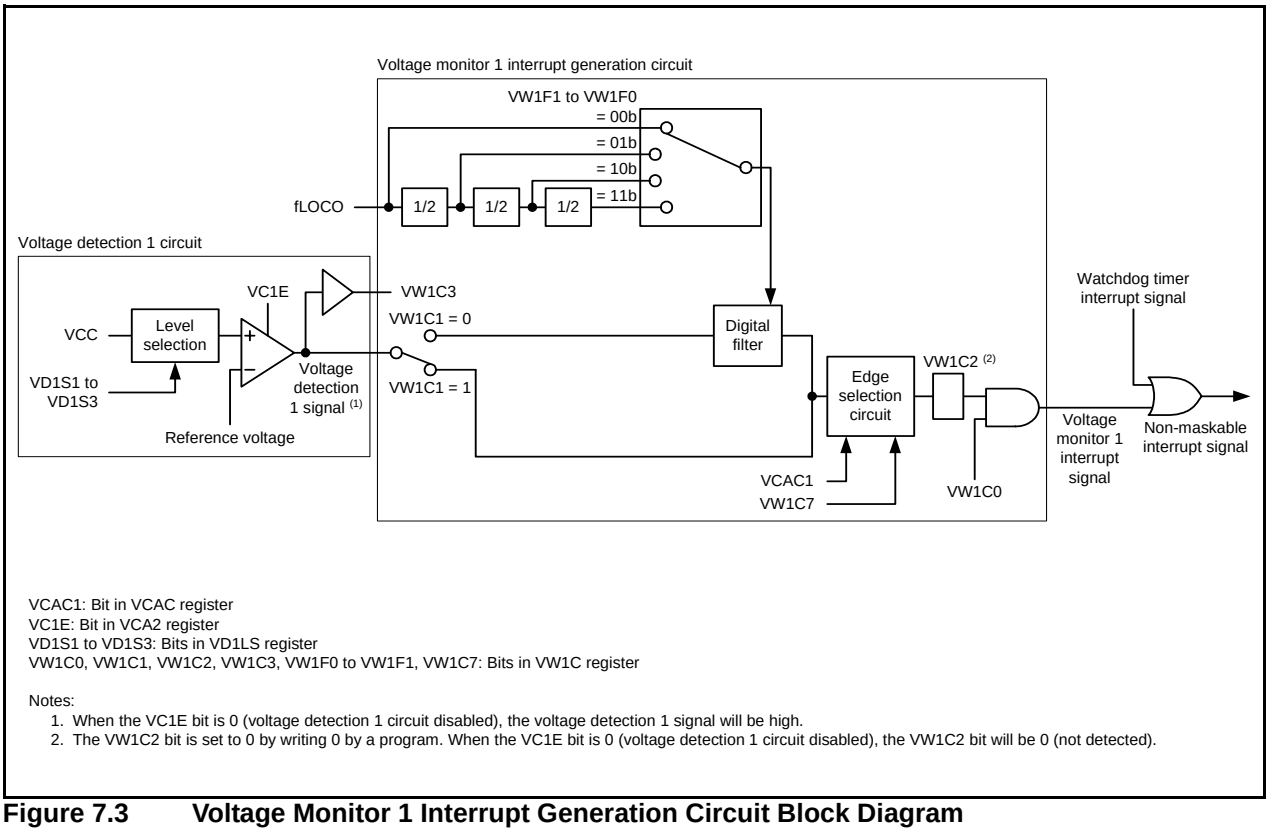
Figure 7.1 Voltage Detection Circuit Block Diagram



VC0E: Bit in VCA2 register
VW0C0, VW0C1, VW0F0 to VW0F1: Bits in VW0C register
VDSEL0 to VDSEL1: Bits in OFS register

Note:
1. When the VC0E bit is 0 (voltage detection 0 circuit disabled), the voltage detection 0 signal will be high.

Figure 7.2 Voltage Monitor 0 Reset Generation Circuit Block Diagram



VCAC1: Bit in VCAC register
VC1E: Bit in VCA2 register
VD1S1 to VD1S3: Bits in VD1LS register
VW1C0, VW1C1, VW1C2, VW1C3, VW1F0 to VW1F1, VW1C7: Bits in VW1C register

Notes:
1. When the VC1E bit is 0 (voltage detection 1 circuit disabled), the voltage detection 1 signal will be high.
2. The VW1C2 bit is set to 0 by writing 0 by a program. When the VC1E bit is 0 (voltage detection 1 circuit disabled), the VW1C2 bit will be 0 (not detected).

Figure 7.3 Voltage Monitor 1 Interrupt Generation Circuit Block Diagram

7.2 Registers

Table 7.2 lists the Voltage Detection Circuit Register Configuration.

Table 7.2 Voltage Detection Circuit Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Voltage Monitor Circuit Edge Select Register	VCAC	00h	00058h	8
Voltage Detect Register 2	VCA2	(Note 1)	0005Ah	8
Voltage Detection 1 Level Select Register	VD1LS	00000111b	0005Bh	8
Voltage Monitor 0 Circuit Control Register	VW0C	(Note 1)	0005Ch	8
Voltage Monitor 1 Circuit Control Register	VW1C	10001010b	0005Dh	8

Note:
1. See the description of the individual registers.

7.2.1 Voltage Monitor Circuit Edge Select Register (VCAC)

Address 00058h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	VCAC1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	VCAC1	Voltage monitor 1 circuit edge select bit (1)	0: One-way edge 1: Two-way edge	R/W
b2	—	Reserved	Set to 0.	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When the VCAC1 bit is 0 (one-way edge), the VW1C7 bit in the VW1C register can be used to select an interrupt generated when the voltage increases or decreases. Set the VCAC1 bit to 0 before setting the VW1C7 bit.

7.2.2 Voltage Detect Register 2 (VCA2)

Address 0005Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	VC1E	VC0E	—	—	—	—	LPE
After Reset	0	0	1	0	0	1	0	0

The above applies when the LVDAS bit in the OFS register is 0.

After Reset	0	0	0	0	0	1	0	0

The above applies when the LVDAS bit in the OFS register is 1.

Bit	Symbol	Bit Name	Function	R/W
b0	LPE	Internal low-power-consumption enable bit (1)	0: Low-power-consumption wait mode disabled 1: Low-power-consumption wait mode enabled	R/W
b1	—	Reserved	Set to 0.	R/W
b2	—	Reserved	Set to 1.	R/W
b3	—	Reserved	Set to 0.	R/W
b4	—			
b5	VC0E	Voltage detection 0 enable bit (2)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VC1E	Voltage detection 1 enable bit (3)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	—	Reserved	Set to 0.	R/W

Notes:

1. Use the LPE bit only when entering wait mode. To set the LPE bit, see **Figure 10.5 Procedure for Reducing Internal Power Consumption by Using LPE Bit**. When the LPE bit is 1 (low-power-consumption wait mode), do not set the STPM bit in the CKSTPR register to 1 (all clocks are stopped (stop mode)).
2. When voltage monitor 0 reset is used, set the VC0E bit to 1 (voltage detection 0 circuit enabled). Set the VC0E bit from 0 to 1 and wait for td(E-A). After that, the voltage detection 0 circuit operates. For details on td(E-A), see **24. Electrical Characteristics**.
3. When a voltage detection 1 interrupt or the VW1C3 bit in the VW1C register is used, set the VC1E bit to 1 (voltage detection 1 circuit enabled). Set the VC1E bit from 0 to 1 and wait for td(E-A). After that, the voltage detection 1 circuit operates. For details on td(E-A), see **24. Electrical Characteristics**.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

7.2.3 Voltage Detection 1 Level Select Register (VD1LS)

Address 0005Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VD1S3	VD1S2	VD1S1	—
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 1.	R/W
b1	VD1S1	Voltage detection 1 level select bits	b3 b2 b1 0 0 0: 2.35 V (Vdet1_1) 0 0 1: 2.65 V (Vdet1_3) 0 1 0: 2.95 V (Vdet1_5) 0 1 1: 3.25 V (Vdet1_7) 1 0 0: 3.55 V (Vdet1_9) 1 0 1: 3.85 V (Vdet1_B) 1 1 0: 4.15 V (Vdet1_D) 1 1 1: 4.45 V (Vdet1_F)	R/W
b2	VD1S2			R/W
b3	VD1S3			R/W
b4	—	Reserved	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VD1LS register.

7.2.4 Voltage Monitor 0 Circuit Control Register (VW0C)

Address 0005Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	VW0F1	VW0F0	—	—	VW0C1	VW0C0
After Reset	1	1	0	0	X	0	1	1
	The above applies when the LVDAS bit in the OFS register is 0.							
After Reset	1	1	0	0	X	0	1	0
	The above applies when the LVDAS bit in the OFS register is 1.							

Bit	Symbol	Bit Name	Function	R/W
b0	VW0C0	Voltage monitor 0 reset enable bit (1)	0: Voltage monitor 0 reset disabled 1: Voltage monitor 0 reset enabled	R/W
b1	VW0C1	Voltage monitor 0 digital filter mode select bit (2, 3)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disabled mode (digital filter circuit disabled)	R/W
b2	—	Reserved	Set to 0.	R/W
b3	—	Reserved	The read value is undefined.	R
b4	VW0F0	Sampling clock select bits (3)	b5 b4 0 0: Division of fLOCO by 1 (no division) 0 1: Division of fLOCO by 2 1 0: Division of fLOCO by 4 1 1: Division of fLOCO by 8	R/W
b5	VW0F1			R/W
b6	—	Reserved	Set to 1.	R/W
b7	—			

Notes:

1. The VW0C0 bit is enabled when the VC0E bit in the VCA2 register is 1 (voltage detection 0 circuit enabled). When the VC0E bit is 0 (voltage detection 0 circuit disabled), set the VW0C0 bit to 0 (voltage monitor 0 reset disabled). To set the VW0C0 bit to 1 (voltage monitor 0 reset enabled), see **Table 7.3 Procedure for Setting Bits Associated with Voltage Monitor 0 Reset**.
2. When the digital filter is used (while the VW0C1 bit is 0), set the LOCODIS bit in the OCOCR register to 0 (low-speed on-chip oscillator on).
   When the voltage monitor 0 reset is used to return from stop mode, set the VW0C1 bit to 1 (digital filter disabled mode).
3. When the VW0C0 bit is 1 (voltage monitor 0 reset enabled), do not set bits VW0C1 and VW0F0 to VW0F1 at the same time (with one instruction).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW0C register.

7.2.5 Voltage Monitor 1 Circuit Control Register (VW1C)

Address 0005Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW1C7	—	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW1C0	Voltage monitor 1 interrupt enable bit (1)	0: Voltage monitor 1 interrupt disabled 1: Voltage monitor 1 interrupt enabled	R/W
b1	VW1C1	Voltage monitor 1 digital filter mode select bit (2, 5)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disabled mode (digital filter circuit disabled)	R/W
b2	VW1C2	Voltage change detection flag (3, 4)	0: Not detected 1: Detected by passing through Vdet1	R/W
b3	VW1C3	Voltage detection 1 signal monitor flag (3)	0: VCC < Vdet1 1: VCC ≥ Vdet1 or voltage detection 1 circuit disabled	R
b4	VW1F0	Sampling clock select bits (5)	b5 b4 0 0: Division of fLOCO by 1 (no division) 0 1: Division of fLOCO by 2 1 0: Division of fLOCO by 4 1 1: Division of fLOCO by 8	R/W
b5	VW1F1			R/W
b6	—	Reserved	Set to 0.	R/W
b7	VW1C7	Voltage monitor 1 interrupt generation condition select bit (6)	0: VCC reaches Vdet1 or above 1: VCC reaches Vdet1 or below	R/W

Notes:

1. The VW1C0 bit is enabled when the VC1E bit in the VCA2 register is 1 (voltage detection 1 circuit enabled). When the VC1E bit is 0 (voltage detection 1 circuit disabled), set the VW1C0 bit to 0 (voltage monitor 1 interrupt disabled). To set the VW1C0 bit to 1 (voltage monitor 1 interrupt enabled), see **Table 7.4 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt**.
2. When the digital filter is used (the VW1C1 bit is 0), set the LOCODIS bit in the OCOCR register to 0 (low-speed on-chip oscillator on).
   When the voltage monitor 1 interrupt is used to return from stop mode, set the VW1C1 bit to 1 (digital filter disabled mode).
3. Bits VW1C2 and VW1C3 are enabled when the VC1E bit in the VCA2 register is 1 (voltage detection 1 circuit enabled).
4. Set this bit to 0 by a program. The VW1C2 bit can be set to 0 by writing 0 by a program, but writing 1 to this bit has no effect.
5. When the VW1C0 bit is 1 (voltage monitor 1 interrupt enabled), do not set bits VW1C1 and VW1F0 to VW1F1 at the same time (with one instruction).
6. The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is 0 (one-way edge). Set the VCAC1 bit to 0 before setting the VW1C7 bit.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW1C register. Rewriting the the VW1C register may set the VW1C2 bit to 1 (Vdet1 passing detected). Rewrite this register before setting the VW1C2 bit to 0 (not detected).

7.3 Monitoring VCC Input Voltage

7.3.1 Monitoring Vdet0

Vdet0 cannot be monitored.

7.3.2 Monitoring Vdet1

Make the following settings and wait for td(E-A) (see **24. Electrical Characteristics**). After that, the comparison result from voltage monitor 1 can be monitored with the VW1C3 bit in the VW1C register.

(1) Set bits VD1S1 to VD1S3 in the VD1LS register to select the detection voltage for voltage detection 1.
(2) Set the VC1E bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).

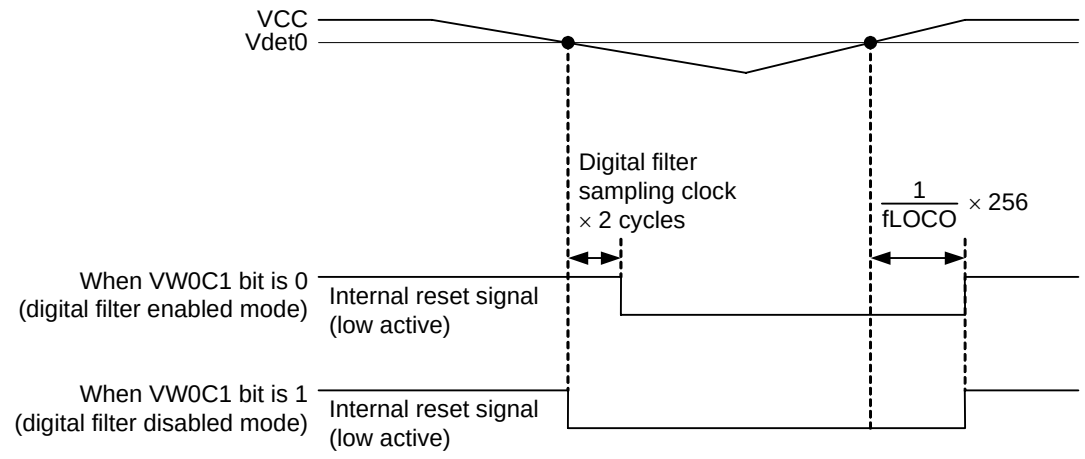
7.4 Voltage Monitor 0 Reset

Table 7.3 lists the Procedure for Setting Bits Associated with Voltage Monitor 0 Reset. Figure 7.4 shows an Example of Voltage Monitor 0 Reset Operation.
Set the VW0C1 bit in the VW0C register to 1 (digital filter disabled mode) to use the voltage monitor 0 interrupt to clear stop mode.

Table 7.3 Procedure for Setting Bits Associated with Voltage Monitor 0 Reset

Step	When the Digital Filter is Used	When the Digital Filter is Not Used
1	Set bits VDSEL0 to VDSEL1 in the OFS register to select the detection voltage for voltage detection 0.	
2	Set the VC0E bit in the VCA2 register to 1 (voltage detection 0 circuit enabled).	
3	Wait for td(E-A).	
4 (1)	Set VW0F0 to VW0F1 in the VW0C register to select the sampling clock for the digital filter.	—
5 (1)	Set the VW0C1 bit in the VW0C register to 0 (digital filter enabled mode).	Set the VW0C1 bit in the VW0C register to 1 (digital filter disabled mode).
6	Set the LOCODIS bit in the OCOCR register to 0 (low-speed on-chip oscillator on).	—
7	Wait for 2 cycles of the digital filter sampling clock.	No wait time
8	Set the VW0C0 bit in the VW0C register to 1 (voltage monitor 0 reset enabled).	

Note:
1. When the VW0C0 bit in the VW0C register is 0 (voltage monitor 0 reset disabled), steps 4 and 5 can be executed at the same time (with one instruction).



VW0C1: Bit in VW0C register

The above diagram applies under the following conditions:
- VC0E bit in VCA2 register = 1 (voltage detection 0 circuit enabled)
- VW0C0 bit in VW0C register = 1 (voltage monitor 0 reset enabled)

When the internal reset signal goes low, the CPU, SFRs, and I/O ports are initialized.
When the internal reset signal changes from low to high, program execution starts from the address indicated by the reset vector.
For the states of the SFRs, see **3.2 Special Function Registers (SFRs)**.

Figure 7.4 Example of Voltage Monitor 0 Reset Operation

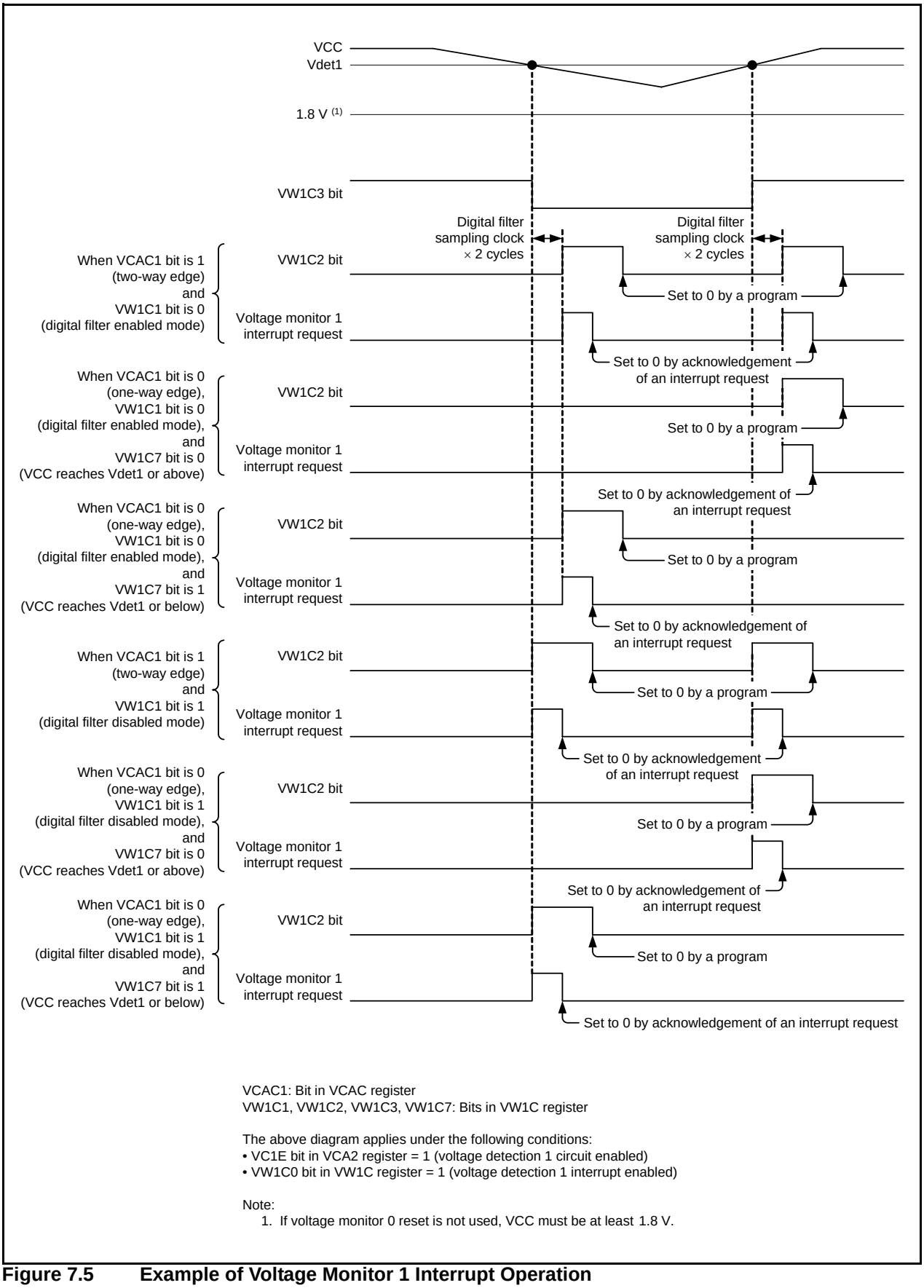
7.5 Voltage Monitor 1 Interrupt

Table 7.4 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt. Figure 7.5 shows an Example of Voltage Monitor 1 Interrupt Operation.
Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled mode) to use the voltage monitor 1 interrupt to clear stop mode.

Table 7.4 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt

Step	When the Digital Filter is Used	When the Digital Filter is Not Used
1	Set bits VD1S1 to VD1S3 in the VD1LS register to select the detection voltage for voltage detection 1.	
2	Set the VC1E bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).	
3	Wait for td(E-A).	
4 (1)	Set bits VW1F0 to VW1F1 in the VW1C register to select the sampling clock for the digital filter.	—
5 (1)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled mode).	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled mode).
6	Set the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register to select the timing for an interrupt request.	
7	Set the VW1C2 bit in the VW1C register to 0 (not detected).	
8	Set the LOCODIS bit in the OCOCR register to 0 (low-speed on-chip oscillator on).	—
9	Wait for 2 cycles of the digital filter sampling clock.	No wait time
10	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled).	

Note:
1. When the VW1C0 bit in the VW1C register is 0 (voltage monitor 1 interrupt disabled), steps 4 and 5 can be executed at the same time (with one instruction).



VCAC1: Bit in VCAC register
VW1C1, VW1C2, VW1C3, VW1C7: Bits in VW1C register

The above diagram applies under the following conditions:
- VC1E bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage detection 1 interrupt enabled)

Note:
1. If voltage monitor 0 reset is not used, VCC must be at least 1.8 V.

Figure 7.5 Example of Voltage Monitor 1 Interrupt Operation

7.6 Digital Filter for Voltage Detection Circuits 0 and 1

Figure 7.6 shows a Block Diagram of Voltage Detection Circuit Digital Filter. In digital filter enabled mode, the voltage detection signal from the voltage detection circuit is used to generate a voltage monitor 0 reset signal and a voltage monitor 1 interrupt signal individually through the digital filter circuit. The filter width of the digital filter circuit is the sampling clock × 2.

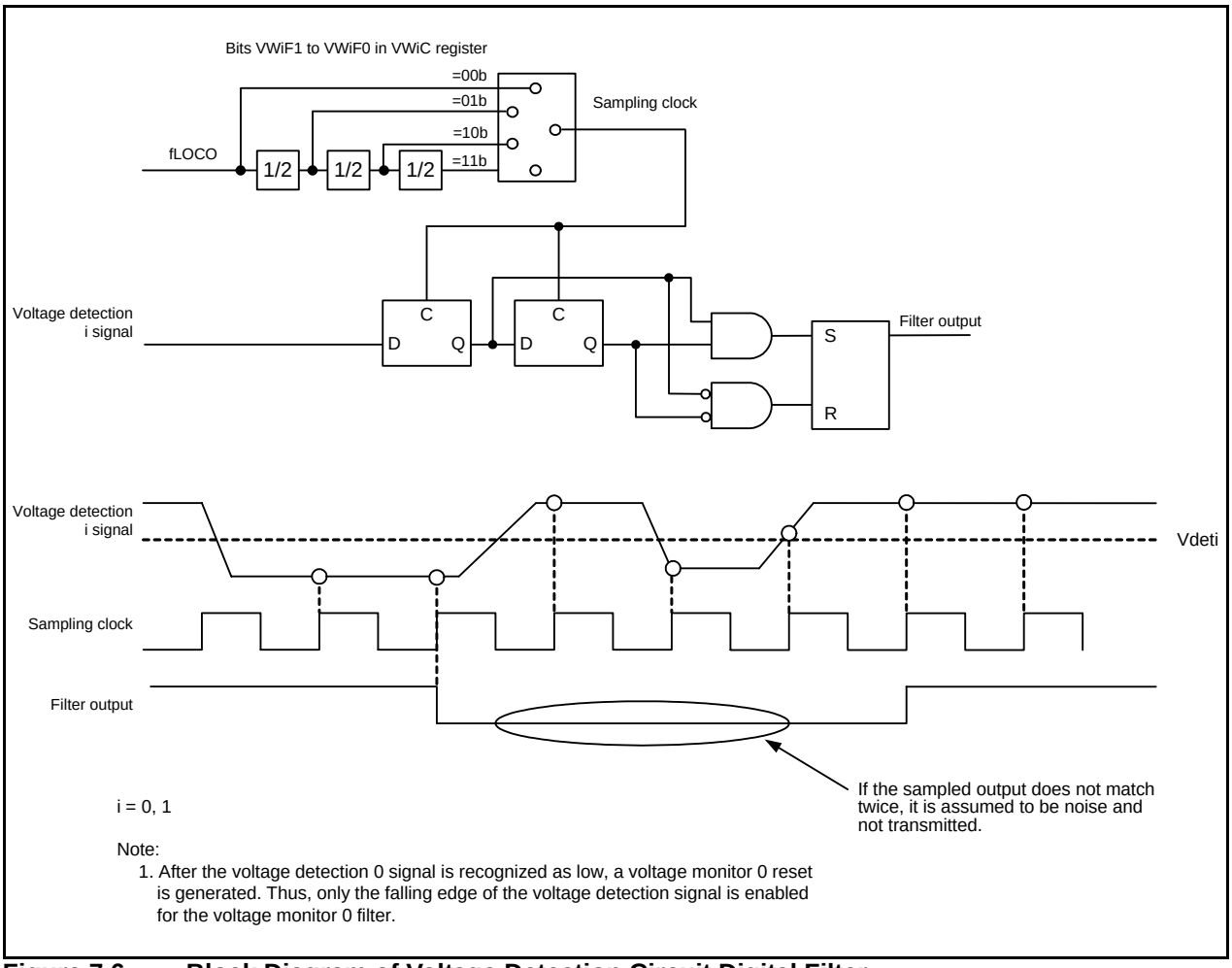


Figure 7.6 Block Diagram of Voltage Detection Circuit Digital Filter

8. Watchdog Timer

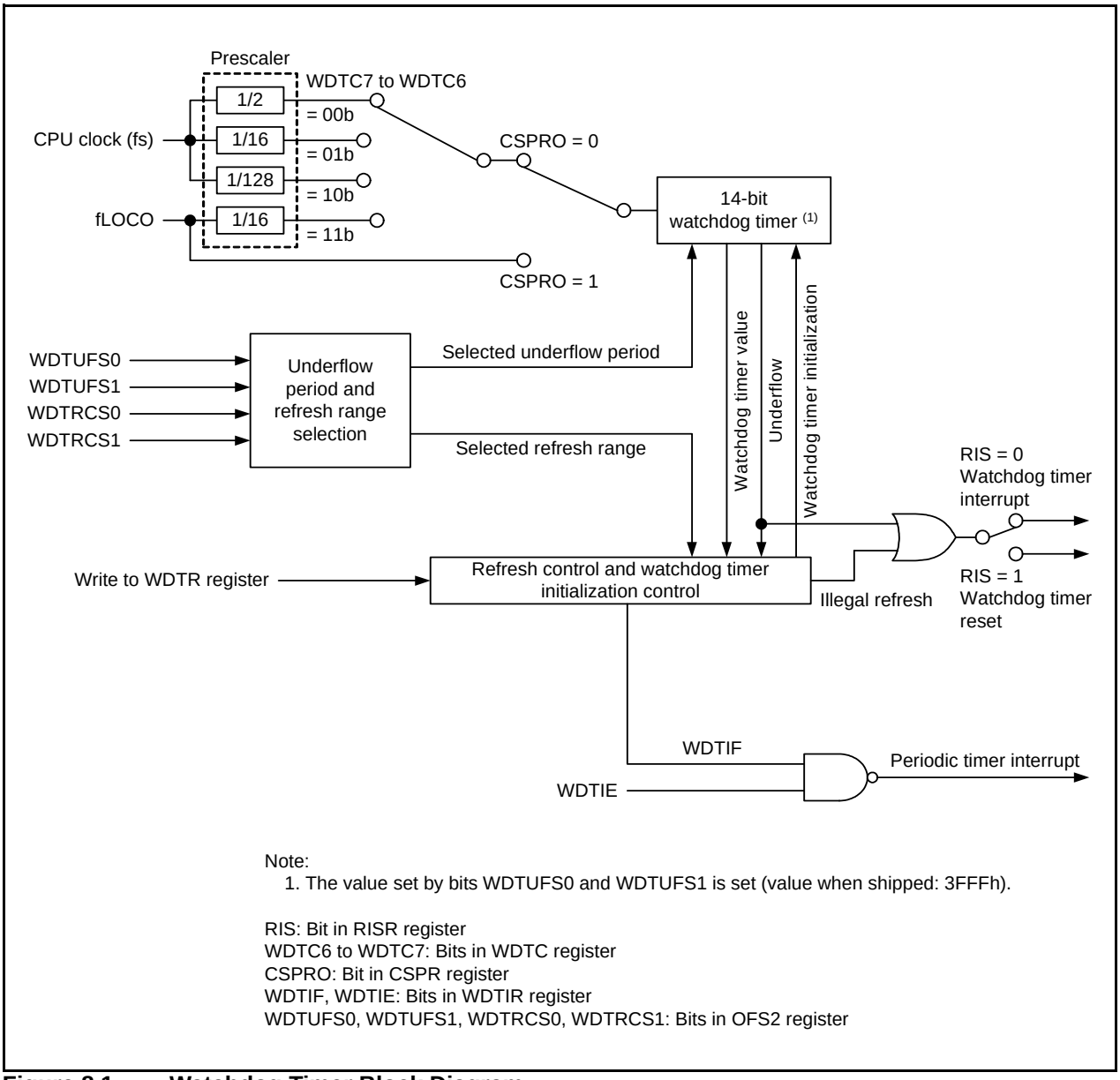
The watchdog timer is a function for detecting program malfunctions. Using this function is recommended, since it can improve system reliability.
The watchdog timer also has a function that can be used as a periodic timer.

8.1 Overview

The watchdog timer has a 14-bit down counter, and count source protection mode can be enabled or disabled.
Table 8.1 lists the Watchdog Timer Specifications.
For details on the watchdog timer reset, see **6.3.5 Watchdog Timer Reset**.
For details on the periodic timer, see **8.3.4 Periodic Timer Function**.
Figure 8.1 shows the Watchdog Timer Block Diagram.

Table 8.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock or low-speed on-chip oscillator clock (1/16)	Low-speed on-chip oscillator clock
Count operation	Decrement	
Count start condition	Either of the following can be selected: • The count is automatically started after a reset. • The count is started by writing to the WDTS register.	
Count stop conditions	When wait mode or stop mode is entered while the count source is the CPU clock	None
Watchdog timer initialization conditions	• Reset • 00h and then FFh are written to the WDTR register during the acceptance period (An acceptance period is set.) • Underflow	
Operation at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Selection of the count source Selected by bits WDTC6 to WDTC7 in the WDTC register. • Count source protection mode - Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register. - If count source protection mode is disabled, whether count source protection mode is enabled or disabled is selected by the CSPRO bit in the CSPR register. • Start or stop of the watchdog timer after a reset Selected by the WDTON bit in the OFS register. • Initial value of the watchdog timer Selected by bits WDTUFS0 to WDTUFS1 in the OFS2 register. • Refresh acceptance period for the watchdog timer Selected by bits WDTRCS0 to WDTRCS1 in the OFS2 register.	



Note:
1. The value set by bits WDTUFS0 and WDTUFS1 is set (value when shipped: 3FFFh).

RIS: Bit in RISR register
WDTC6 to WDTC7: Bits in WDTC register
CSPRO: Bit in CSPR register
WDTIF, WDTIE: Bits in WDTIR register
WDTUFS0, WDTUFS1, WDTRCS0, WDTRCS1: Bits in OFS2 register

Figure 8.1 Watchdog Timer Block Diagram

8.2 Registers

Table 8.2 lists the Watchdog Timer Register Configuration.

Table 8.2 Watchdog Timer Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Watchdog Timer Function Register	RISR	(Note 1)	00030h	8
Watchdog Timer Reset Register	WDTR	XXh	00031h	8
Watchdog Timer Start Register	WDTS	XXh	00032h	8
Watchdog Timer Control Register	WDTC	01XXXXXXb	00033h	8
Count Source Protection Mode Register	CSPR	(Note 1)	00034h	8
Periodic Timer Interrupt Control Register	WDTIR	00h	00035h	8

Note:
1. See the description of the individual registers.

8.2.1 Watchdog Timer Function Register (RISR)

Address 00030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RIS	UFIF	—	—	—	—	—	—
After Reset	1	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 0.							
After Reset	0	0	0	0	0	0	0	0
	The above applies when the CSPROINI bit in the OFS register is 1.							

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	UFIF	WDT underflow detection flag	0: No watchdog timer underflow 1: Watchdog timer underflow (1)	R/W
b7	RIS	WDT interrupt/reset switch bit	0: Watchdog timer interrupt 1: Watchdog timer reset (2)	R/W

Notes:
1. After reading this bit as 1, wait at least one cycle of the count source before writing 0 to it.
2. The RIS bit is set to 1 by writing 1 by a program, but writing 0 to this bit has no effect.
   When the CSPRO bit in the CSPR register is 1 (count source protection mode enabled), the RIS bit is automatically set to 1.

   Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the RISR register.

UFIF Bit (WDT underflow detection flag)

[Condition for setting to 0]
• When 0 is written to this bit.
[Conditions for setting to 1]
• When the watchdog timer underflows while the RIS bit is 0 (watchdog timer interrupt).
• When a refresh is executed during the period other than the acceptance period (illegal refresh) while the RIS bit is 0 (watchdog timer interrupt).

8.2.2 Watchdog Timer Reset Register (WDTR)

Address 00031h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	The watchdog timer is initialized by writing 00h and then writing FFh during the acceptance period. When 00h and then FFh is written during a non-acceptable period, a watchdog timer reset or a watchdog timer interrupt is generated. If a watchdog timer interrupt is selected, the counter is not initialized. The initial value of the watchdog timer is specified by bits WDTUFS0 to WDTUFS1 in the OFS2 register. (1)	W

Note:
1. Only write to the WDTR register when the watchdog timer is counting.

8.2.3 Watchdog Timer Start Register (WDTS)

Address 00032h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	The watchdog timer is started by executing a write instruction to this register.	W

8.2.4 Watchdog Timer Control Register (WDTC)

Address 00033h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTC7	WDTC6	—	—	—	—	—	—
After Reset	0	1	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is undefined.	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	WDTC6	Watchdog timer count source select bits	b7 b6 0 0: Division of CPU clock by 2 0 1: Division of CPU clock by 16 1 0: Division of CPU clock by 128 1 1: Division of low-speed on-chip oscillator by 16	R/W
b7	WDTC7			R/W

8.2.5 Count Source Protection Mode Register (CSPR)

Address 00034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPRO	—	—	—	—	—	—	—
After Reset	1	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is 0.

After Reset	0	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is 1.

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CSPRO	Count source protection mode select bit (1)	0: Count source protection mode disabled 1: Count source protection mode enabled	R/W

Note:
1. To set the CSPRO bit to 1, first write 0 and then write 1 to it. This bit cannot be set to 0 by a program. Do not write to any register other than the CSPR register between writing 0 and then writing 1.

8.2.6 Periodic Timer Interrupt Control Register (WDTIR)

Address 00035h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTIE	WDTIF	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	WDTIF	Periodic timer interrupt request flag	0: No periodic timer interrupt requested 1: Periodic timer interrupt requested	R/W
b7	WDTIE	Periodic timer interrupt enable bit (1)	0: Periodic timer interrupt disabled 1: Periodic timer interrupt enabled	R/W

Note:
1. When bits WDTRCS1 to WDTRCS0 in the OFS2 register is 11b (100%), set the WDTIE bit to 0 (periodic timer interrupt disabled).

WDTIF Bit (Periodic timer interrupt request flag)

[Condition for setting to 0]
• When 0 is written to this bit after reading it as 1.
[Condition for setting to 1]
• When the watchdog timer completes counting an illegal write range.

8.3 Operation

8.3.1 Items Common to Multiple Modes

8.3.1.1 Refresh Acceptance Period

The period for accepting a refresh operation to the watchdog timer (a write to the WDTR register) can be selected by bits WDTRCS0 to WDTRCS1 in the OFS2 register. Figure 8.2 shows the Watchdog Timer Refresh Acceptance Period.

When the period from the start of counting to underflow is 100%, a refresh operation executed during the acceptance period is accepted as shown below. A refresh operation executed during a period other than the acceptance period is processed as an illegal refresh, generating a watchdog timer interrupt or watchdog timer reset (selected by the RIS bit in the RISR register). In addition, the UFIF bit in the RISR register is set to 1.

Do not perform a refresh operation when the watchdog timer is stopped.

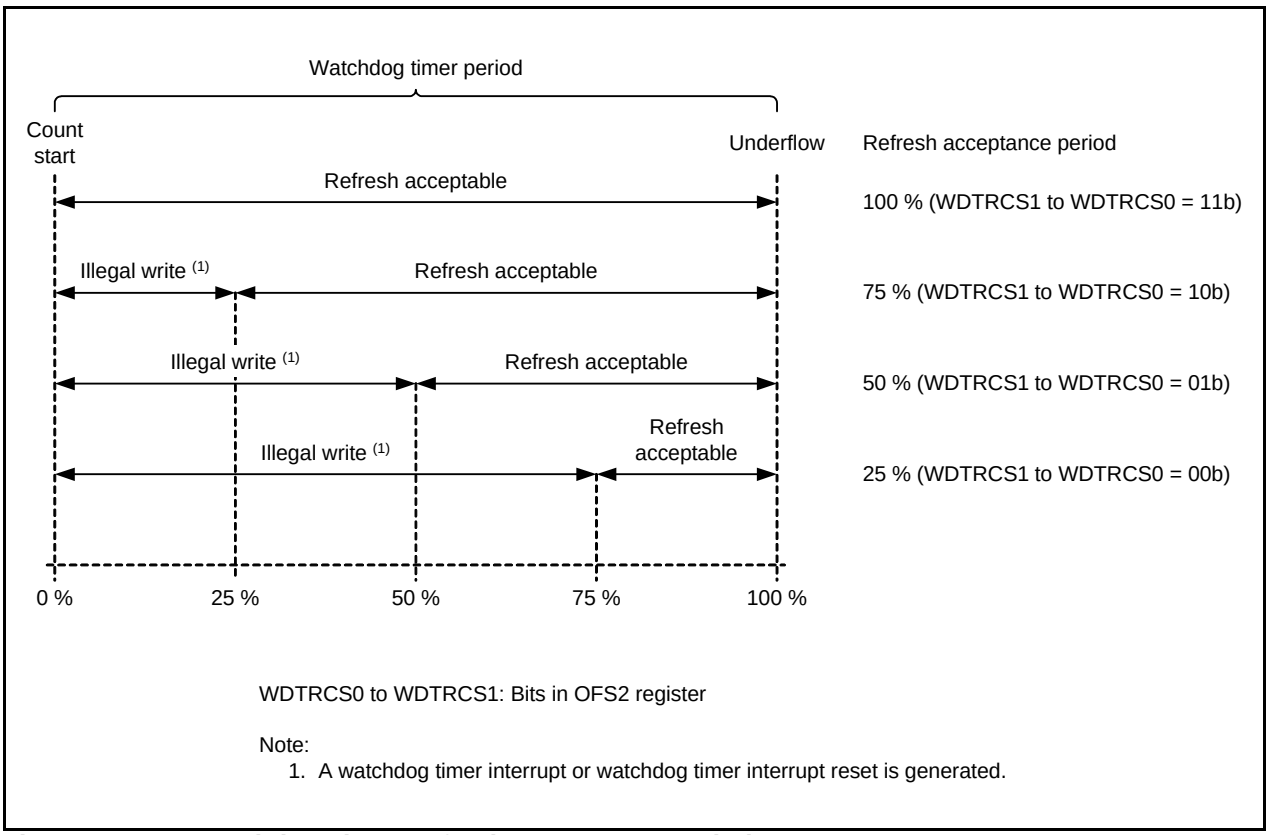


Figure 8.2 Watchdog Timer Refresh Acceptance Period

8.3.2 When Count Source Protection Mode is Disabled

When count source protection mode is disabled, the count source for the watchdog timer is the CPU clock or low-speed on-chip oscillator clock.
Table 8.3 lists the Watchdog Timer Specifications When Count Source Protection Mode is Disabled.

Table 8.3 Watchdog Timer Specifications When Count Source Protection Mode is Disabled

Item	Specification
Count source	CPU clock or low-speed on-chip oscillator clock (1/16)
Count operation	Decrement
Period	$\frac{\text{Prescaler division ratio (n)} \times \text{Count value in the watchdog timer (m)}}{\text{Count source}}$ (1) n: 2, 16, or 128 (selected by bits WDTC6 to WDTC7 in the WDTC register) However, when bits WDTC7 to WDTC6 are 11b (count source is low-speed on-chip oscillator), n is 16. m: Value set by bits WDTUFS0 to WDTUFS1 in the OFS2 register Ex.: When the prescaler divides a CPU clock of 20 MHz by 16, and bits WDTUFS1 to WDTUFS0 are 11b (3FFFh), the period is approx. 13.1 ms.
Watchdog timer initialization conditions	• Reset • 00h and then FFh are written to the WDTR register • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit in the OFS register (address 0FFFFh). • When the WDTON bit is 1 (watchdog timer is stopped after reset) The watchdog timer and the prescaler are stopped after a reset, and only start counting when the WDTS register is written. • When the WDTON bit is 0 (watchdog timer is automatically started after reset) The watchdog timer and the prescaler automatically start counting after a reset.
Count stop conditions	When wait mode or stop mode is entered while the count source is the CPU clock
Operation at underflow	• When the RIS bit in the RISR register is 0 Watchdog timer interrupt • When the RIS bit in the RISR register is 1 Watchdog timer reset (See **6.3.5 Watchdog Timer Reset**.)

Note:
1. The watchdog timer is initialized by writing 00h and then writing FFh to the WDTR register. The prescaler is initialized after a reset. This results in discrepancies in the watchdog timer period due to the prescaler.

8.3.3 When Count Source Protection Mode is Enabled

When count source protection mode is enabled, the count source for the watchdog timer is the low-speed on-chip oscillator clock. If the CPU clock is stopped when a program runs out of control, a clock will still be supplied to the watchdog timer.
Table 8.4 lists the Watchdog Timer Specifications When Count Source Protection Mode is Enabled.

Table 8.4 Watchdog Timer Specifications When Count Source Protection Mode is Enabled

Item	Specification
Count source	Low-speed on-chip oscillator clock
Count operation	Decrement
Period	$\frac{\text{Count value in the watchdog timer (m)}}{\text{Low-speed on-chip oscillator clock}}$ m: Value set by WDTUFS0 to WDTUFS1 in the OFS2 register Ex.: When the low-speed on-chip oscillator clock is 125 kHz and bits WDTUFS1 to WDTUFS0 are 00b (03FFh), the period is approx. 8.2 ms.
Watchdog timer initialization conditions	• Reset • 00h and then FFh are written to the WDTR register • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit in the OFS register (address 0FFFFh). • When the WDTON bit is 1 (watchdog timer is stopped after reset) The watchdog timer is stopped after a reset, and only starts counting when the WDTS register is written. • When the WDTON bit is 0 (watchdog timer is automatically started after reset) The watchdog timer automatically starts counting after a reset.
Count stop condition	None (The count is not stopped even in wait mode or stop mode once it is started.)
Operation at underflow	Watchdog timer reset (See **6.3.5 Watchdog Timer Reset**.)
Registers, bits	When the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled), the following are automatically set: • The low-speed on-chip oscillator oscillates. • The RIS bit in the RISR register is set to 1 (watchdog timer reset).

8.3.4 Periodic Timer Function

The count range is determined by the underflow period setting (bits WDTUFS0 to WDTUFS1 in the OFS2 register) and the refresh acceptance period setting (bits WDTRCS0 to WDTRCS1 in the OFS2 register). The periodic timer cannot be used in stop mode.
Table 8.5 lists the Periodic Timer Settings. Figure 8.3 shows the Timing of Periodic Timer Function.
When the periodic timer runs beyond the count range in Table 8.5, the WDTIF bit in the WDTIR register is set to 1 (periodic timer interrupt requested).

Table 8.5 Periodic Timer Settings

Initial Value Set by Bits WDTUFS1 to WDTUFS0 in OFS2 Register	Refresh Range Set by Bits WDTRCS1 to WDTRCS0 in OFS2 Register (1)	Range Counted by Periodic Timer
11b	10b	3FFFh → 2FFFh
	01b	3FFFh → 1FFFh
	00b	3FFFh → 0FFFh
10b	10b	1FFFh → 17FFh
	01b	1FFFh → 0FFFh
	00b	1FFFh → 07FFh
01b	10b	0FFFh → 0BFFh
	01b	0FFFh → 07FFh
	00b	0FFFh → 03FFh
00b	10b	03FFh → 02FFh
	01b	03FFh → 01FFh
	00b	03FFh → 00FFh

Note:
1. When bits WDTRCS1 to WDTRCS0 in the OFS2 register is 11b (100%), set the WDTIE bit to 0 (periodic timer interrupt disabled).

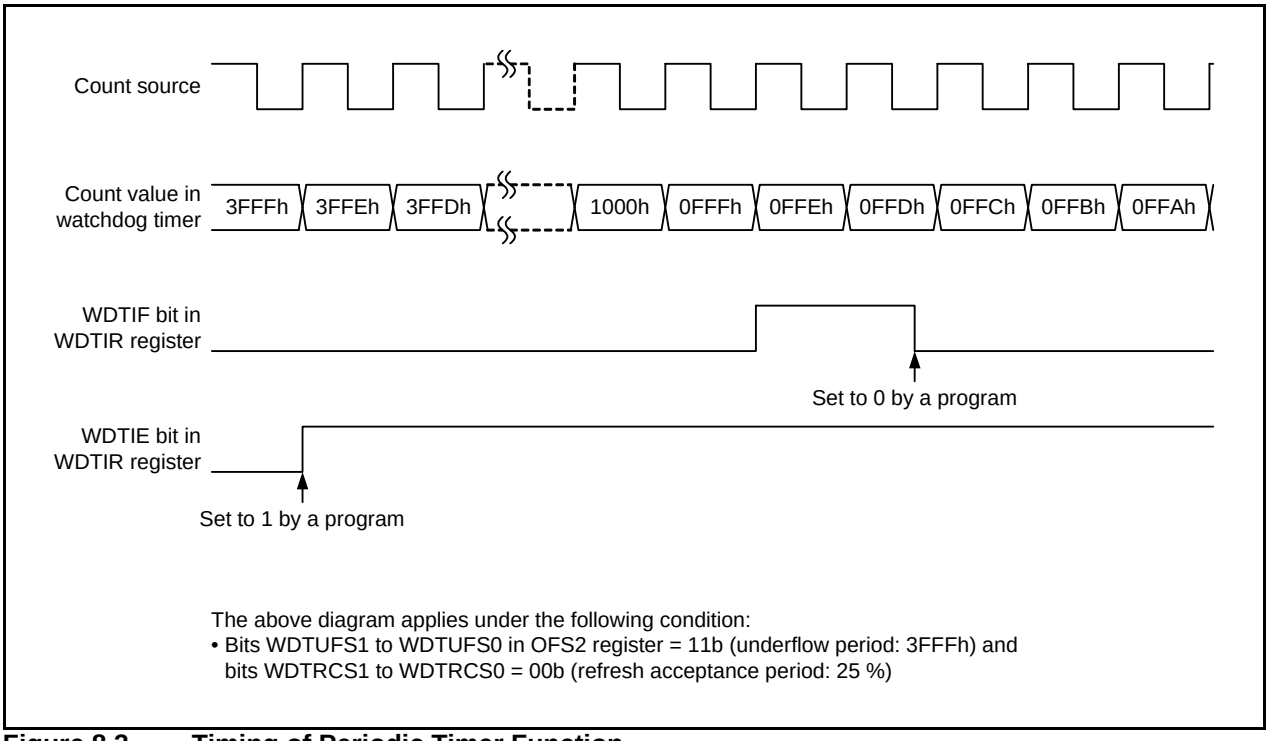


Figure 8.3 Timing of Periodic Timer Function

8.4 Notes on Watchdog Timer

- Do not switch the count sources during watchdog timer operation.
- There is a delay of two cycles of the count source from a write to the WDTR register until the initialization of the watchdog timer.
- Allow at least three cycles of the count source between the previous and the next initialization of the watchdog timer.

9. Clock Generation Circuit

9.1 Overview

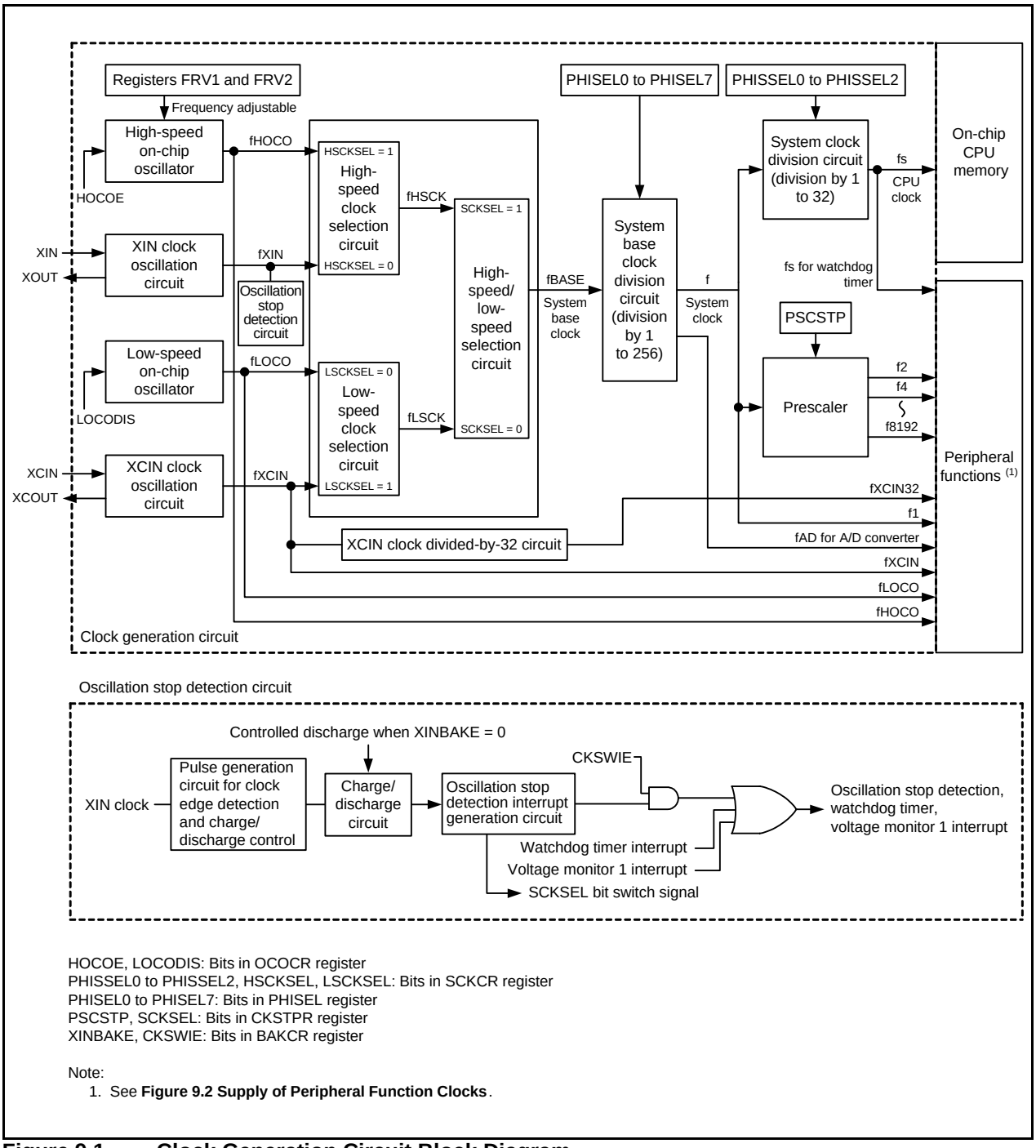
The following four circuits are included in the clock generation circuit:
- XIN clock oscillation circuit
- XCIN clock oscillation circuit
- High-speed on-chip oscillator
- Low-speed on-chip oscillator

Table 9.1 lists the Clock Generation Circuit Specifications. Figure 9.1 shows the Clock Generation Circuit Block Diagram. Figure 9.2 shows the Supply of Peripheral Function Clocks. Table 9.2 lists the Clock Generation Circuit Pin Configuration.

Table 9.1 Clock Generation Circuit Specifications

Item	XIN Clock Oscillation Circuit	XCIN Clock Oscillation Circuit	High-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator
Clock frequency	0 MHz to 20 MHz (2 MHz to 20 MHz when an oscillator is used)	32.768 kHz	Approx. 20 MHz	Approx. 125 kHz
Connectable oscillator	• Ceramic resonator • Crystal oscillator	Crystal oscillator	—	—
Oscillator connect pins	XIN, XOUT (1)	XCIN, XCOUT (2)	—	—
Oscillation start and stop	Usable	Usable	Usable	Usable
State after reset	Stopped	Stopped	Stopped	Oscillates
Others	• An externally generated clock can be input. • A feed-back resistor is included (connected or not connected can be selected).	• An externally generated clock can be input. • A feed-back resistor is included (connected or not connected can be selected).	The system clock can be output from P4_5.	The system clock can be output from P4_5.

Notes:
1. When the on-chip oscillator clock instead of the XIN clock oscillation circuit is used as the CPU clock, these pins can be used as P3_1 and P4_5.
2. When the on-chip oscillator clock instead of the XCIN clock oscillation circuit is used as the CPU clock, these pins can be used as P4_6 and P4_7.



HOCOE, LOCODIS: Bits in OCOCR register
PHISSEL0 to PHISSEL2, HSCKSEL, LSCKSEL: Bits in SCKCR register
PHISEL0 to PHISEL7: Bits in PHISEL register
PSCSTP, SCKSEL: Bits in CKSTPR register
XINBAKE, CKSWIE: Bits in BAKCR register

Note:
1. See **Figure 9.2 Supply of Peripheral Function Clocks**.

Figure 9.1 Clock Generation Circuit Block Diagram

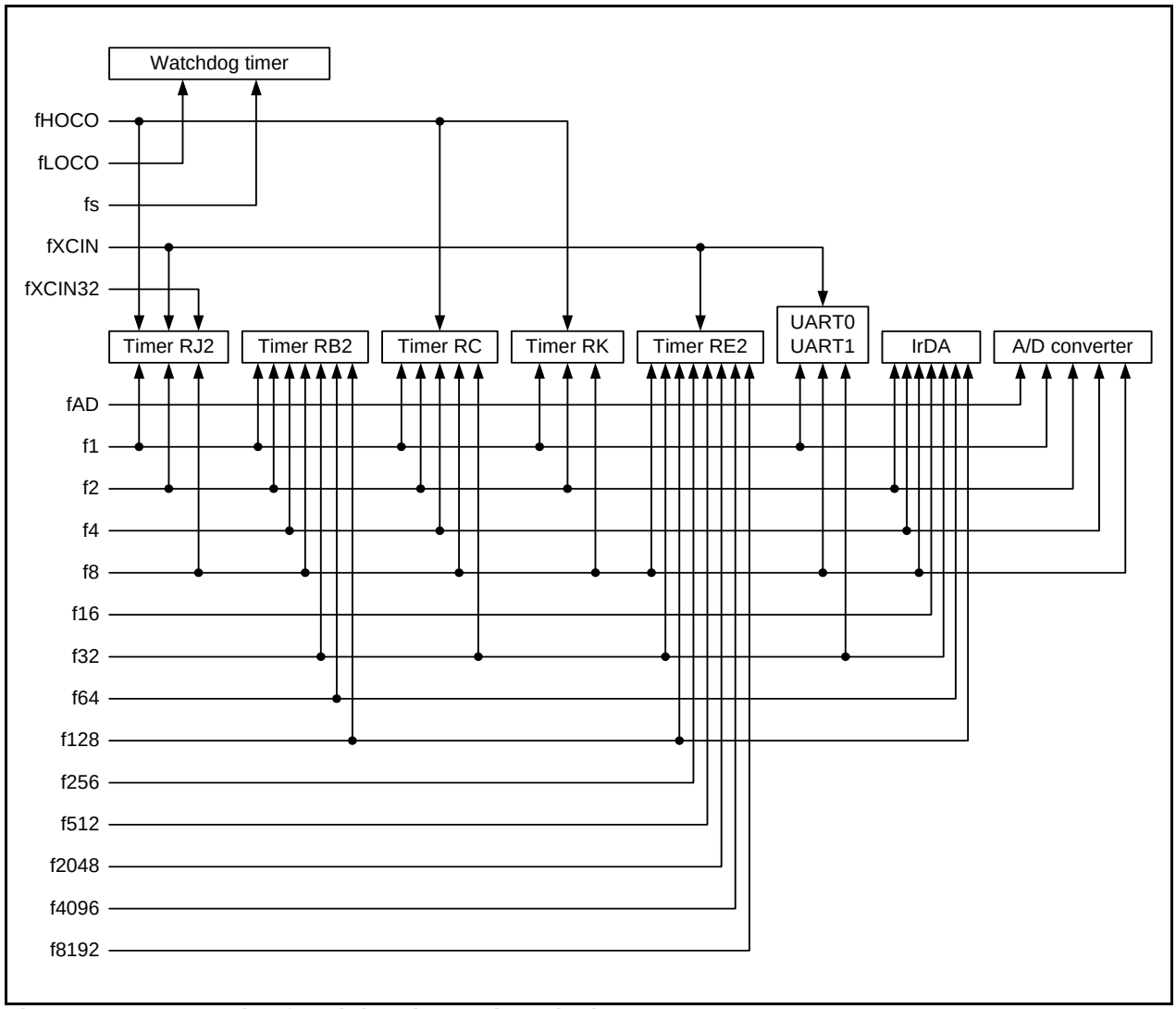


Figure 9.2 Supply of Peripheral Function Clocks

Table 9.2 Clock Generation Circuit Pin Configuration

Pin Name	I/O	Function
XIN	I	XIN clock input/external clock input
XOUT	O	XIN clock output
XCIN	I	XCIN clock input/external clock input
XCOUT	O	XCIN clock output

9.2 Registers

Table 9.3 lists the Clock Generation Circuit Register Configuration.

Table 9.3 Clock Generation Circuit Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
External Clock Control Register	EXCKCR	00h	00020h	8
High-Speed/Low-Speed On-Chip Oscillator Control Register	OCOCR	00h	00021h	8
System Clock f Control Register	SCKCR	00h	00022h	8
System Clock f Select Register	PHISEL	00h	00023h	8
Clock Stop Control Register	CKSTPR	00h	00024h	8
Clock Control Register When Returning	CKRSCR	00h	00025h	8
Oscillation Stop Detection Register	BAKCR	00h	00026h	8
High-Speed On-Chip Oscillator 18.432 MHz Control Register 0	FR18S0	Value when shipped	00064h	8
High-Speed On-Chip Oscillator 18.432 MHz Control Register 1	FR18S1	Value when shipped	00065h	8
High-Speed On-Chip Oscillator Control Register 1	FRV1	Value when shipped	00067h	8
High-Speed On-Chip Oscillator Control Register 2	FRV2	Value when shipped	00068h	8

9.2.1 External Clock Control Register (EXCKCR)

Address 00020h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	XCRCUT	XRCUT	XCINNC1	XCINNC0	CKPT3	CKPT2	CKPT1	CKPT0
After Reset	0	0	0	0	0	0	0	0

<table>
<tr><th>Bit</th><th>Symbol</th><th>Bit Name</th><th>Function</th><th>R/W</th></tr>
<tr><td>b0</td><td>CKPT0</td><td rowspan="2">P3_1 and P4_5 pin function select bits</td><td rowspan="2">
<table>
<tr><th colspan="2">Register Setting</th><th colspan="2">Pin Function</th></tr>
<tr><th>CKPT1</th><th>CKPT0</th><th>P3_1</th><th>P4_5</th></tr>
<tr><td>0</td><td>0</td><td>I/O port</td><td>I/O port</td></tr>
<tr><td>0</td><td>1</td><td>XIN clock input (External clock input)</td><td>I/O port</td></tr>
<tr><td>1</td><td>0</td><td>I/O port</td><td>System clock output</td></tr>
<tr><td>1</td><td>1</td><td>XIN</td><td>XOUT</td></tr>
</table>
</td><td>R/W</td></tr>
<tr><td>b1</td><td>CKPT1</td><td>R/W</td></tr>
<tr><td>b2</td><td>CKPT2</td><td rowspan="2">P4_6 and P4_7 pin function select bits</td><td rowspan="2">
<table>
<tr><th colspan="2">Register Setting</th><th colspan="2">Pin Function</th></tr>
<tr><th>CKPT3</th><th>CKPT2</th><th>P4_6</th><th>P4_7</th></tr>
<tr><td>0</td><td>0</td><td>I/O port</td><td>I/O port</td></tr>
<tr><td>0</td><td>1</td><td>XCIN clock input (External clock input)</td><td>I/O port</td></tr>
<tr><td>1</td><td>0</td><td>XCIN</td><td>XOUT</td></tr>
<tr><td>1</td><td>1</td><td colspan="2">Do not set</td></tr>
</table>
</td><td>R/W</td></tr>
<tr><td>b3</td><td>CKPT3</td><td>R/W</td></tr>
<tr><td>b4</td><td>XCINNC0</td><td rowspan="2">XCIN clock noise cancel sampling function setting bits</td><td rowspan="2">b5 b4
0 0: Sampling function disabled
0 1: Sampling function disabled
1 0: fHSCK divided-by-4 clock sampling
1 1: fHSCK divided-by-16 clock sampling</td><td>R/W</td></tr>
<tr><td>b5</td><td>XCINNC1</td><td>R/W</td></tr>
<tr><td>b6</td><td>XRCUT</td><td>XIN-XOUT on-chip feedback resistor select bit</td><td rowspan="2">0: On-chip feedback resistor enabled
1: On-chip feedback resistor disabled</td><td>R/W</td></tr>
<tr><td>b7</td><td>XCRCUT</td><td>XCIN-XCOUT on-chip feedback resistor select bit</td><td>R/W</td></tr>
</table>

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the EXCKCR register.

Bits CKPT0 to CKPT1 (P3_1 and P4_5 pin function select bits)

When stopping oscillation with an oscillator attached, set bits CKPT0 to CKPT0 to 00b and set P3_1 and P4_5 to input ports according to Tables 12.23 and 12.29.

While the high-speed on-chip oscillator clock or the low-speed on-chip oscillator clock is selected as the system base clock, the system clock can be output from P4_5 by setting bits CKPT0 to CKPT0 to 10b and bits P45SEL1 to P45SEL0 in the PMH4 register to 00b.

Bits CKPT2 to CKPT3 (P4_6 and P4_7 pin function select bits)

When stopping oscillation with an oscillator attached, set bits CKPT3 to CKPT2 to 00b and set P4_6 and P4_7 to input ports according to Tables 12.30 and 12.31.

When setting bits CKPT3 to CKPT2 to 10b (P4_6: XCIN, P4_7: XCOUT), set the SUBMODE bit in the SUBCR register to 1 first.

While the XCIN clock oscillates, the XCIN clock divided by 32 (fXCIN32) can be used.

Bits XCINNC0 to XCINNC1 (XCIN clock noise cancel sampling function setting bits)

When fHSCK stops in stop mode, the sampling function is disabled. fHSCK is selected from the XIN clock or high-speed on-chip oscillator clock by the HSCKSEL bit in the SCKCR register. When enabling the sampling function, oscillate the selected clock.

XRCUT Bit (XIN-XOUT on-chip feedback resistor select bit) XCRCUT Bit (XCIN-XCOUT on-chip feedback resistor select bit)

The XRCUT bit is enabled only when bits CKPT3 to CKPT0 are 1011b.
When the STPM bit in the CKSTPR register is set to 1 (stop mode), the on-chip feedback resistor is disabled.

9.2.2 High-Speed/Low-Speed On-Chip Oscillator Control Register (OCOCR)

Address 00021h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	LOCODIS	HOCOE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	HOCOE	High-speed on-chip oscillator oscillation enable bit	0: High-speed on-chip oscillator off 1: High-speed on-chip oscillator on	R/W
b1	LOCODIS	Low-speed on-chip oscillator oscillation stop bit	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCOCR register.

HOCOE Bit (High-speed on-chip oscillator oscillation enable bit)

The high-speed on-chip oscillator clock generated by the high-speed on-chip oscillator is stopped after a reset. Table 9.4 lists the Register Settings and High-Speed On-Chip Oscillator States. When selecting the high-speed on-chip oscillator clock as the system base clock, switch the clock according to **9.4.6 Procedure for Switching System Base Clock**.

Table 9.4 Register Settings and High-Speed On-Chip Oscillator States

Register	CKSTPR	SCKCR	CKSTPR	OCOCR	High-Speed On-Chip Oscillator State
Bit	STPM	HSCKSEL	SCKSEL	HOCOE	
Setting value	0	Other than 11b		0	Oscillation off
	0	Other than 11b		1	Oscillation on
	0	11b		X	Oscillation on
	1	X		X	Oscillation off

X: 0 or 1

LOCODIS Bit (Low-speed on-chip oscillator oscillation stop bit)

Table 9.5 lists the Register Settings and Low-Speed On-Chip Oscillator States. If the XINBAKE bit in the BAKCR register is 1 (oscillation stop detection function enabled), when the XIN clock is stopped, the low-speed on-chip oscillator starts operation and supplies the system base clock.

Table 9.5 Register Settings and Low-Speed On-Chip Oscillator States

Register	CSPR	WDTC		CKSTPR	SCKSEL	CKSTPR	OCOCR	Low-Speed On-Chip Oscillator State
Bit	CSPRO	WDTC7	WDTC6	STPM	LSCKSEL	SCKSEL	LOCODIS	
Setting value	0	Other than 11b		0	Other than 00b		0	Oscillation on
	0	Other than 11b		0	Other than 00b		1	Oscillation off
	0	Other than 11b		0	0		X	Oscillation on
	0	Other than 11b		1	X		X	Oscillation off
	0	11b		X	X		X	Oscillation on
	1	X		X	X		X	Oscillation on

X: 0 or 1

9.2.3 System Clock f Control Register (SCKCR)

Address 00022h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LSCKSEL	HSCKSEL	WAITM	—	—	PHISSEL2	PHISSEL1	PHISSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PHISSEL0	CPU clock division ratio select bits	These bits are used to select the division ratio of the system clock (f) to generate the CPU clock (fs). b2 b1 b0 0 0 0: fs = System clock with no division 0 0 1: fs = System clock divided by 2 0 1 0: fs = System clock divided by 4 0 1 1: fs = System clock divided by 8 1 0 0: fs = System clock divided by 16 1 0 1: fs = System clock divided by 32 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b1	PHISSEL1			R/W
b2	PHISSEL2			R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	WAITM	Wait control bit	0: Not in wait mode 1: Wait mode is entered	R/W
b6	HSCKSEL	High-speed on-chip oscillator/XIN clock select bit	0: XIN clock 1: High-speed on-chip oscillator clock	R/W
b7	LSCKSEL	Low-speed on-chip oscillator/XCIN clock select bit	0: Low-speed on-chip oscillator clock 1: XCIN clock	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the SCKCR register.

Bits PHISSEL0 to PHISSEL2 (CPU clock division ratio select bits)

Bits PHISSEL2 to PHISSEL0 are set to 000b (fs = f1) if the PHISRS bit in the CKRSCR register is 1 (no division) when the MCU returns from wait mode or stop mode.

WAITM Bit (Wait control bit)

[Condition for setting to 0]
• When a peripheral function interrupt is used to return from wait mode.
[Condition for setting to 1]
• When 1 is written to the WAITM bit after the PRC0 bit in the PRCR register is set to 1 (write enabled).

9.2.4 System Clock f Select Register (PHISEL)

Address 00023h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PHISEL7	PHISEL6	PHISEL5	PHISEL4	PHISEL3	PHISEL2	PHISEL1	PHISEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0 to b7	PHISEL0 to PHISEL7	System clock division ratio select bits	These bits are used to set the division ratio of the system base clock (fBASE) to generate the system clock (f) and the A/D converter clock fAD). • System clock (f) f = fBASE/(n + 1) • Clock for A/D converter (fAD) fAD = fBASE/(n + 1) .....when (n + 1) is not a multiple of 4 fAD = 4 × fBASE/(n + 1) ....when (n + 1) is a multiple of 4 n: Binary value set by the PHISEL register	00h to FFh	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the PHISEL register.
Table 9.6 lists the PHISEL Register Setting Example.

Table 9.6 PHISEL Register Setting Example

Value Set in PHISEL Register (n)	System Clock (f)	A/D Converter Clock (fAD)
00h	fBASE	fBASE
01h	Division of fBASE by 2	Division of fBASE by 2
02h	Division of fBASE by 3	Division of fBASE by 3
03h	Division of fBASE by 4	fBASE
04h	Division of fBASE by 5	Division of fBASE by 5
05h	Division of fBASE by 6	Division of fBASE by 6
06h	Division of fBASE by 7	Division of fBASE by 7
07h	Division of fBASE by 8	Division of fBASE by 2

9.2.5 Clock Stop Control Register (CKSTPR)

Address 00024h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SCKSEL	—	—	—	—	PSCSTP	WCKSTP	STPM
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	STPM	All clock stop control bit	0: Clocks oscillate 1: All clocks are stopped (stop mode)	R/W
b1	WCKSTP	fBASE stop bit in wait mode	0: System clock supplied in wait mode 1: System clock stopped in wait mode	R/W
b2	PSCSTP	Prescaler stop bit	0: Prescaler operates 1: Prescaler is stopped	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	SCKSEL	System base clock select bit	0: fLSCK 1: fHSCK	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CKSTPR register.

STPM Bit (All clock stop control bit)

When count source protection mode is enabled or the low-speed on-chip oscillator divided by 16 is selected as the count source for the watchdog timer, the low-speed on-chip oscillator clock oscillates even if a transition is made to stop mode.

WCKSTP Bit (fBASE stop bit in wait mode)

This bit is used to control supply and stop of the system clock in wait mode.

PSCSTP Bit (Prescaler stop bit)

Setting the PSCSTP bit to 1 stops the prescaler. The peripheral functions that use f2 to f8192 are stopped operating. However, the values of corresponding registers are retained.

SCKSEL Bit (System base clock select bit)

[Conditions for setting to 0]
- When 0 is written to this bit.
- When the XIN clock oscillation stopped state is detected and the system clock is switched to fLOCO when the XIN clock is selected as the system clock and the XINBAKE bit in the BAKCR register is set to 1 (oscillation stop detection function enabled).

[Conditions for setting to 1]
- When 1 is written to this bit.
- When the MCU returns from wait mode when the WAITRS bit in the CKRSCR register is 1 (fHSCK).
- When the MCU returns from stop mode when the STOPRS bit in the CKRSCR register is 1 (fHSCK).

9.2.6 Clock Control Register When Returning (CKRSCR)

Address 00025h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	STOPRS	WAITRS	PHISRS	—	CKST3	CKST2	CKST1	CKST0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKST0	Clock oscillator circuit oscillation stabilization state select bits	Number of wait states b3 b2 b1 b0 0 0 0 0: 4 0 0 0 1: 16 0 0 1 0: 32 0 0 1 1: 64 0 1 0 0: 128 0 1 0 1: 256 0 1 1 0: 512 0 1 1 1: 1024 1 0 0 0: 2048 1 0 0 1: 4096 1 0 1 0: 8192 1 0 1 1: 16384 1 1 0 0: 32768 1 1 0 1: 65536 1 1 1 0: 131072 1 1 1 1: 262144	R/W
b1	CKST1			R/W
b2	CKST2			R/W
b3	CKST3			R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	PHISRS	CPU clock division select bit when returning from wait mode or stop mode	0: The value set in bits PHISSEL0 to PHISSEL2 in the SCKCR register is valid 1: No division	R/W
b6	WAITRS	System base clock select bit when returning from wait mode	0: Return using the system base clock used immediately before entering wait mode 1: fHSCK (1, 2)	R/W
b7	STOPRS	System base clock select bit when returning from stop mode	0: Return using the system base clock used immediately before entering stop mode 1: fHSCK (1, 2)	R/W

Notes:
1. When the HSCKSEL bit in the SCKCR register is 0 (XIN clock), set pins P4_6 and P4_7 to XIN oscillation by a program before entering wait mode or stop mode.
2. Set this bit to 0 before entering wait mode or stop mode if the FMR27 bit in the FMR2 register is set to 1 (low current-consumption read mode enabled).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CKRSCR register.

Bits CKST0 to CKST3 (Clock oscillator circuit oscillation stabilization state select bits)

These bits are used to set the oscillation stabilization time of the oscillator circuit for the system base clock when returning wait mode or stop mode. Set appropriate values according to Table 9.7.

Table 9.7 Oscillation Stabilization Time When Returning Wait Mode or Stop Mode

System Base Clock after Returning	Stabilization Time (Automatic Generation)	Setting Value for Number of Wait States (Bits CKST0 to CKST3)
XIN clock	XIN clock period × system clock division ratio × number of wait states	Contact the oscillator manufacturer.
XCIN clock	XCIN clock period × system clock division ratio × number of wait states	Contact the oscillator manufacturer.
High-speed on-chip oscillator clock	High-speed on-chip oscillator clock period × system clock division ratio × number of wait states	See **Table 24.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
Low-speed on-chip oscillator clock	Low-speed on-chip oscillator clock period × system clock division ratio × 2 wait states	— (Value set in CKST0 to CKST3 is invalid)

When the oscillation stop detection function is disabled, the system base clock used after returning from stop mode is the XIN clock. The stabilization time generated by the hardware is expressed as follows:
Stabilization time = XIN clock period × System clock division ratio × Number of steps for stabilization

When the oscillation stop detection function is enabled, the system base clock used after returning from stop mode is the low-speed on-chip oscillator clock. The stabilization time generated by the hardware is expressed as follows:
Stabilization time = Low-speed on-chip oscillator clock cycle × System clock division ratio × Number of steps for stabilization

9.2.7 Oscillation Stop Detection Register (BAKCR)

Address 00026h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	CKSWIF	XINHALT	CKSWIE	XINBAKE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	XINBAKE	Oscillation stop detection enable bit	0: Oscillation stop detection function disabled 1: Oscillation stop detection function enabled	R/W
b1	CKSWIE	Oscillation stop detection interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b2	XINHALT	Clock monitor bit (1)	0: XIN clock oscillating 1: XIN clock halted	R/W
b3	CKSWIF	Oscillation stop detection interrupt flag (1)	0: No oscillation stop detection interrupt request is generated 1: Oscillation stop detection interrupt request is generated	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Bits XINHALT and CKSWIF are enabled when the XINBAKE bit is 1 (oscillation stop detection function enabled). When the XINHALT bit is 0 (XIN clock oscillating), it indicates that the XIN clock is oscillating. It does not indicate oscillation is stable.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the BAKCR register.

CKSWIF Bit (Oscillation stop detection interrupt flag)

[Condition for setting to 0]
- When 0 is written to this bit.

[Condition for setting to 1]
- When oscillation stop is detected while the XIN clock is selected as the system base clock and the XINBAKE bit in the BAKCR register is 1 (oscillation stop detection function enabled).

9.2.8 High-Speed On-Chip Oscillator 18.432 MHz Control Register 0 (FR18S0)

Address 00064h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	Value when shipped							

Bit	Function	R/W
b7 to b0	Frequency adjustment data for 18.432 MHz is stored. The frequency of the high-speed on-chip oscillator can be adjusted to 18.432 MHz by transferring this value to the FRV1 register and the adjustment value in the FR18S1 register to the FRV2 register.	R/W

9.2.9 High-Speed On-Chip Oscillator 18.432 MHz Control Register 1 (FR18S1)

Address 00065h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	Value when shipped							

Bit	Function	R/W
b7 to b0	Frequency adjustment data for 18.432 MHz is stored. The frequency of the high-speed on-chip oscillator can be adjusted to 18.432 MHz by transferring this value to the FRV2 register and the adjustment value in the FR18S0 register to the FRV1 register.	R/W

9.2.10 High-Speed On-Chip Oscillator Control Register 1 (FRV1)

Address 00067h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	Value when shipped							

Bit	Function	R/W
b7 to b0	The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows: 20 MHz: FRV1 = Value after reset, FRV2 = Value after reset 18.432 MHz: Transfer the value in the FR18S0 register to the FRV1 register and the value in the FR18S1 register to the FRV2 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRV1 register.

9.2.11 High-Speed On-Chip Oscillator Control Register 2 (FRV2)

Address 00068h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	Value when shipped							

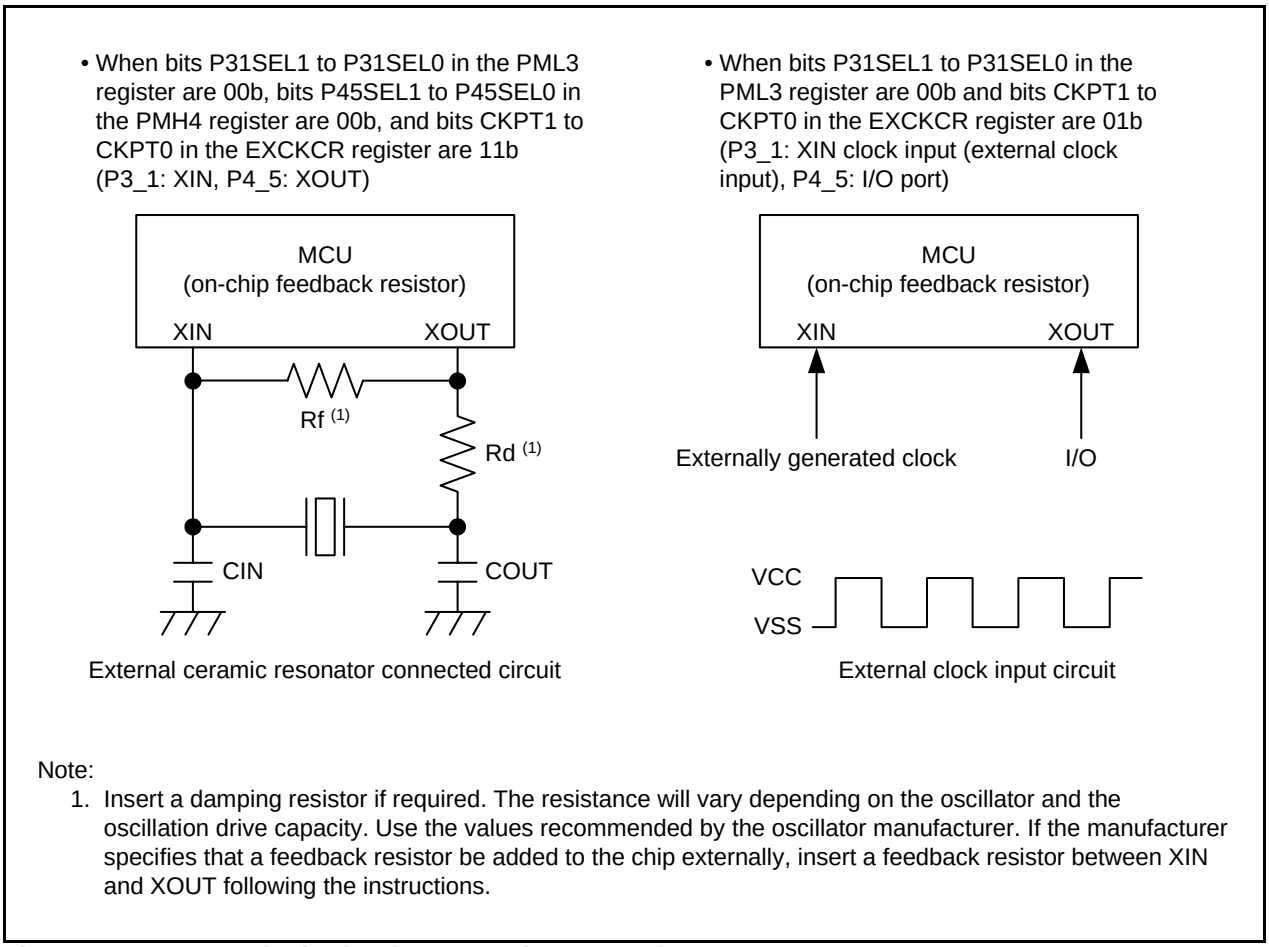
Bit	Function	R/W
b7 to b0	The frequency of the high-speed on-chip oscillator can be adjusted by setting as follows: 20 MHz: FRV1 = Value after reset, FRV2 = Value after reset 18.432 MHz: Transfer the value in the FR18S0 register to the FRV1 register and the value in the FR18S1 register to the FRV2 register.	R/W

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the FRV2 register.

9.3 Clock Oscillation Circuit

9.3.1 XIN Clock Oscillation Circuit

The XIN clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU clock and the peripheral function clock. The XIN clock oscillation circuit is configured by connecting an oscillator between pins XIN and XOUT. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode to reduce power consumption. To input an externally generated clock to the XIN pin, set bits P31SEL1 to P31SEL0 in the PML3 register to 00b (I/O port or XIN input) and bits CKPT1 to CKPT0 in the EXCKCR register to 01b (XIN clock input).
Figure 9.3 shows the XIN Clock Circuit Connection Examples.
The XIN clock is stopped during and after a reset.
The XIN clock starts oscillating when bits P31SEL1 to P31SEL0 in the PML3 register are set to 00b, bits P45SEL1 to P45SEL0 in the PMH4 register are set to 00b, and bits CKPT1 to CKPT0 in the EXCKCR register are set to 11b (P3_1:XIN, P4_5: XOUT). After the XIN clock oscillation stabilizes, when the HSCKSEL bit in the SCKCR register is set to 0 (XIN clock) and the SCKSEL bit in the CKSTPR register is set to 1 (fHSCK), the XIN clock is selected to be used as the clock source for the CPU clock and the peripheral function clock.
When the high-speed on-chip oscillator or the low-speed on-chip oscillator is used as the system base clock, the XIN clock oscillation is stopped by setting bits CKPT1 to CKPT0 in the EXCKCR register to 00b. This reduces power consumption.
The XIN clock is stopped in stop mode. When inputting an externally generated clock to the XIN clock, do not use stop mode. See **10. Power Control** for details.

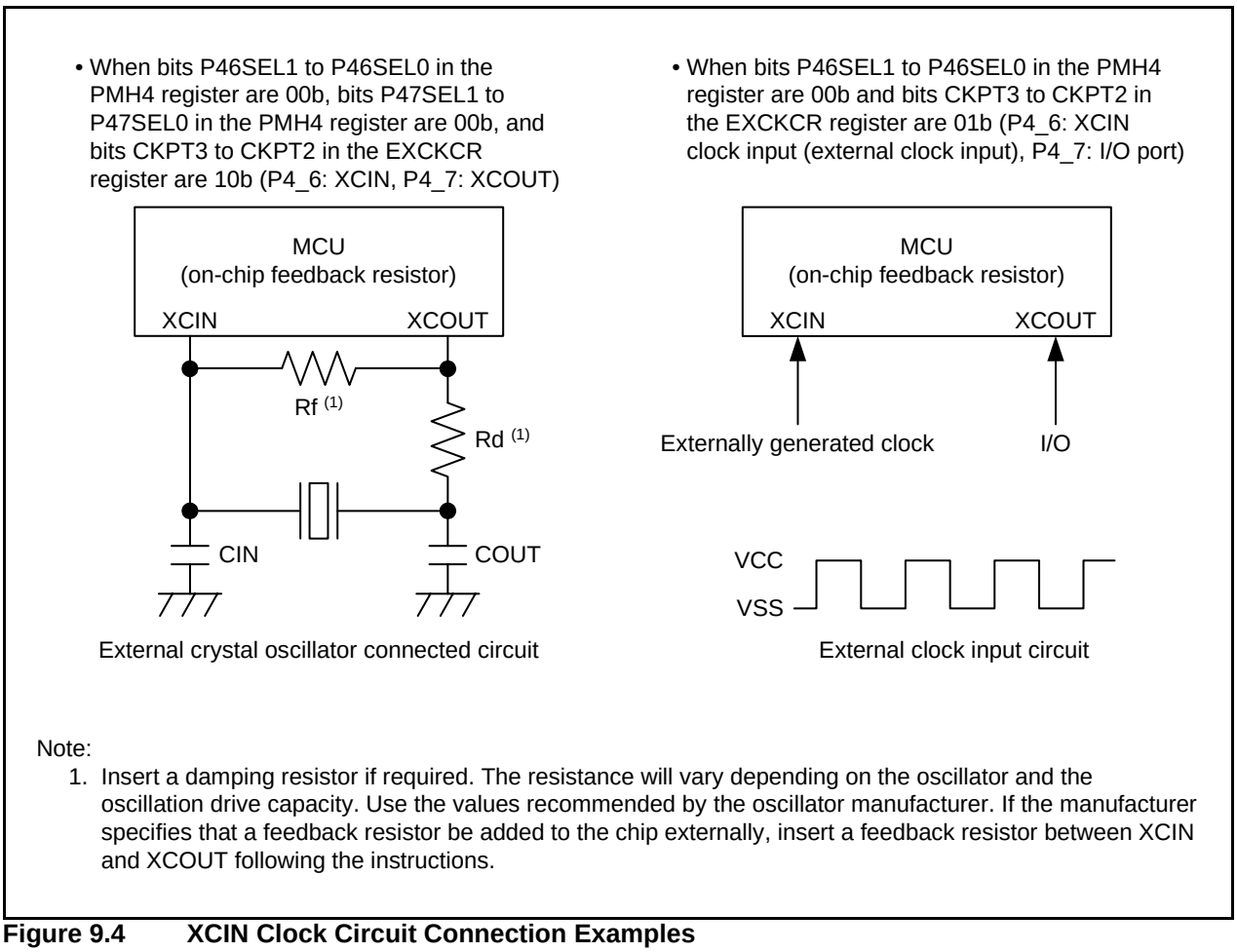


Note:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity. Use the values recommended by the oscillator manufacturer. If the manufacturer specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT following the instructions.

Figure 9.3 XIN Clock Circuit Connection Examples

9.3.2 XCIN Clock Oscillation Circuit

The XCIN clock is supplied by the XCIN clock oscillation circuit. This clock is used as the clock source for the CPU clock and the peripheral function clock. The XCIN clock oscillation circuit is configured by connecting an oscillator between pins XCIN and XCOUT. The XCIN clock oscillation circuit includes an on-chip feedback resistor, which is not disconnected from the oscillation circuit in stop mode. To input an externally generated clock to the XCIN pin, set bits P46SEL1 to P46SEL0 in the PMH4 register are 00b (I/O port or XCIN input) and bits CKPT3 to CKPT2 in the EXCKCR register to 01b (XCIN clock input).
Figure 9.4 shows the XCIN Clock Circuit Connection Examples.
The XCIN clock starts oscillating when bits P46SEL1 to P46SEL0 in the PMH4 register are set to 00b, bits P47SEL1 to P47SEL0 in the PMH4 register are set to 00b, and bits CKPT3 to CKPT2 in the EXCKCR register are set to 10b (P4_6: XIN, P4_7: XOUT). After the XCIN clock oscillation stabilizes, when the LSCKSEL bit in the SCKCR register is set to 1 (XCIN clock) and the SCKSEL bit in the CKSTPR register is set to 0 (fLSCK), the XCIN clock is selected to be used as the clock source for the CPU clock and the peripheral function clock.
When the high-speed on-chip oscillator or the low-speed on-chip oscillator is used as the system base clock, the XCIN clock oscillation is stopped by setting bits CKPT3 to CKPT2 in the EXCKCR register to 00b. This reduces power consumption.
The XCIN clock is not stopped in stop mode. See **10. Power Control** for details



Note:
1. Insert a damping resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity. Use the values recommended by the oscillator manufacturer. If the manufacturer specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XCIN and XCOUT following the instructions.

Figure 9.4 XCIN Clock Circuit Connection Examples

9.3.3 High-Speed On-Chip Oscillator Clock

The clock generated by the high-speed on-chip oscillator is used as the clock source for the CPU clock and the peripheral function clock.

After the HOCOE bit in the OCOCR register is set to 1 (high-speed on-chip oscillator on) and the wait time for oscillation stabilization has elapsed, when the HSCKSEL bit in the SCKCR register is set to 1 (high-speed on-chip oscillator clock) and the SCKSEL bit in the CKSTPR register is set to 1 (fHSCK), the high-speed on-chip oscillator clock is the system base clock (fBASE).

Frequency adjustment data is stored in registers FRV1, FRV2, FR18S0, and FR18S1.

To adjust the frequency of the high-speed on-chip oscillator clock to 18.432 MHz, transfer the adjustment values in registers FR18S0 and FR18S1 to registers FRV1 and FRV2 respectively before use.

This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode. (See **Table 18.8 Setting Example for Clock Asynchronous Serial I/O Mode (Internal Clock Selected)**).

9.3.4 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock and the peripheral function clock.

After the LOCODIS bit in the OCOCR register is set to 0 (low-speed on-chip oscillator on) and the wait time for oscillation stabilization has elapsed, when the LSCKSEL bit in the SCKCR register is set to 0 (low-speed on-chip oscillator clock) and the SCKSEL bit in the CKSTPR register is set to 0 (fLOCO), the low-speed on-chip oscillator clock is the system base clock (fBASE).

After a reset, the on-chip oscillator clock (with no division) is the CPU clock.

The frequency of the on-chip oscillator clock will vary greatly depending on the power supply voltage and operating ambient temperature. Application products must be designed with sufficient margin to allow for these variations in frequency.

9.4 Clocks

9.4.1 System Base Clock (fBASE)

The system base clock is selected from the XIN clock oscillation circuit, XCIN clock oscillation circuit, high-speed on-chip oscillator, or low-speed on-chip oscillator to operate the MCU.
After a reset, the MCU operates using the on-chip oscillator clock in standard mode.

9.4.2 System Clock (f)

The system clock is obtained by dividing the system base clock by any value from 1 to 256, set by bits PHISEL0 to PHISEL7 in the PHISEL register. After a reset is cleared, the low-speed on-chip oscillator clock (no division) is used as the system clock.

9.4.3 CPU Clock (fs)

The CPU clock can be obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32 for CPU operation. After a reset is cleared, the low-speed on-chip oscillator clock (no division) is used as the system clock.

9.4.4 Various Clocks

Table 9.8 lists the Names and Descriptions of Various Clocks that can be generated in the clock generation circuit.

Table 9.8 Names and Descriptions of Various Clocks

Clock Name	Description
Peripheral function clocks f1 to f8192	Clocks for the peripheral functions. These clocks are generated by dividing the system clock. They are used in timer RJ2, timer RB2, timer RC, timer RK, timer RE2, UART0, UART1, IrDA, or the A/D converter. The peripheral function clocks are stopped when wait mode is entered after the WCKSTP bit in the CKSTPR register is set to 1 (system clock stopped in wait mode).
fHOCO	fHOCO is generated by the high-speed on-chip oscillator, and oscillates when the HOCOE bit in the OCOCR register is set to 1. fHOCO is not stopped in wait mode.
fLOCO	fLOCO is generated by the low-speed on-chip oscillator, and oscillates when the LOCODIS bit in the OCOCR register is set to 0. fLOCO is not stopped in wait mode.
fXCIN	fXCIN is generated by the XCIN clock oscillation circuit, and oscillates when bits CKPT3 to CKPT2 in the EXCKCR register are set to 01b (P4_6: XCIN clock input (external clock input), P4_7: I/O port) or 10b (P4_6: XCIN, P4_7: XCOUT). fXCIN is not stopped in wait mode and stop mode.
fHSCK	fHSCK is selected from the XIN clock or high-speed on-chip oscillator clock using the HSCKSEL bit in the SCKCR register.
fLSCK	fLSCK is selected from the XCIN clock or low-speed on-chip oscillator clock using the LSCKSEL bit in the SCKCR register.
fAD	A clock for the A/D converter. This clock is obtained by dividing the system clock. fAD is not stopped in wait mode.

9.4.5 Prescaler

The prescaler is a 13-bit counter that uses the system clock as an input clock. The divided output is used as the internal clock for the on-chip peripheral functions. The prescaler starts operating when the PSCSTP bit in the CKSTPR register is set to 0 (prescaler operates).
The prescaler is stopped when wait mode is entered after the WCKSTP bit in the CKSTPR register is set to 1 (system clock stopped in wait mode). If the clock is switched by the WAITRS bit in the CKRSCR register when a transition is made from wait mode to standard mode, the prescaler is initialized. When a transition is made from stop mode to standard mode, the prescaler is initialized. The prescaler cannot be read or written.

9.4.6 Procedure for Switching System Base Clock

Figure 9.5 shows the Flowchart for Clock Switching between XIN Clock Oscillation Circuit, XCIN Clock Oscillation Circuit, Low-Speed On-Chip Oscillator, and High-Speed On-Chip Oscillator.

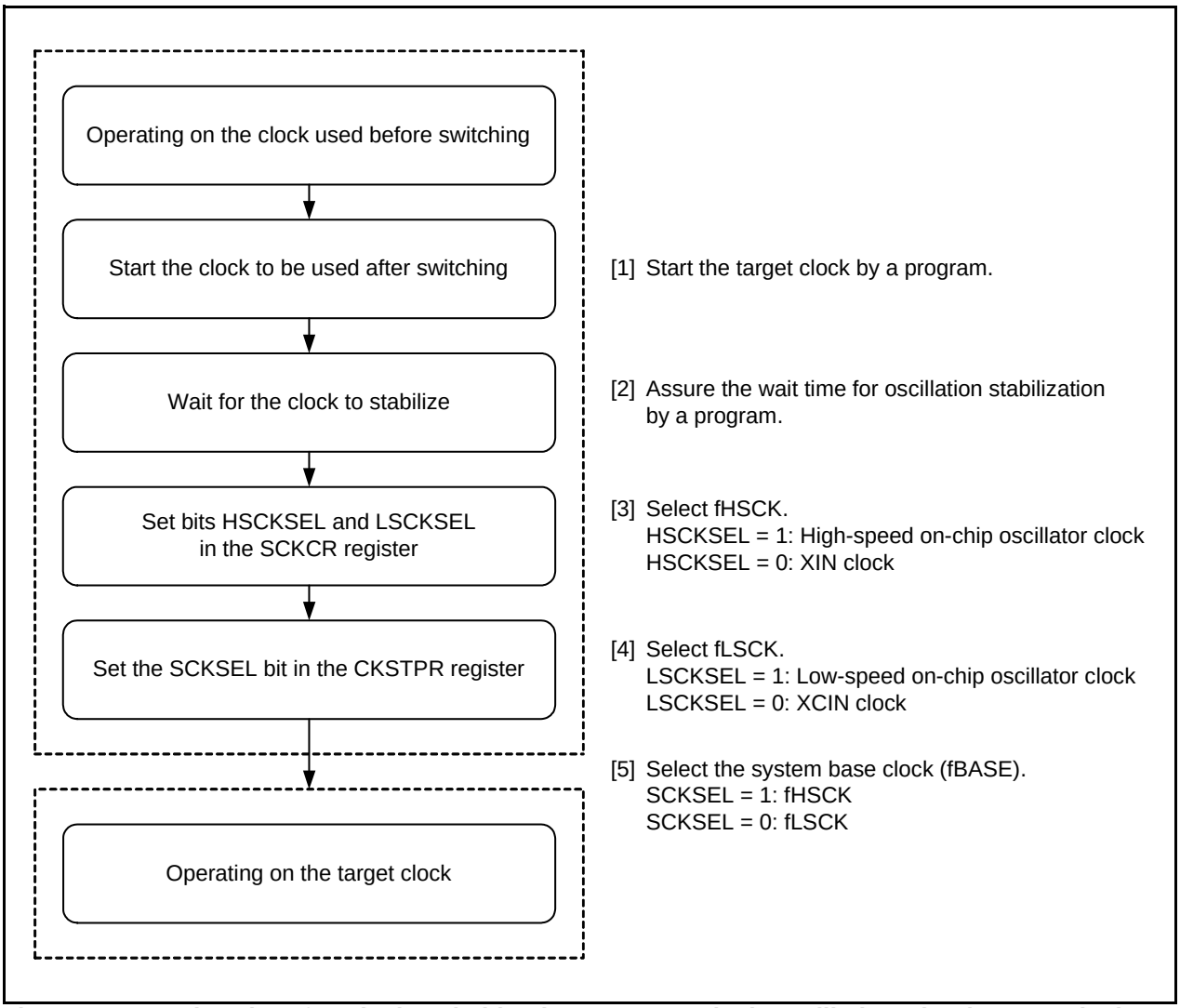


Figure 9.5 Flowchart for Clock Switching between XIN Clock Oscillation Circuit, XCIN Clock Oscillation Circuit, Low-Speed On-Chip Oscillator, and High-Speed On-Chip Oscillator

9.4.6.1 Procedure for Switching System Base Clock to High-Speed On-Chip Oscillator

Figure 9.6 shows the Flowchart for Switching from Low-Speed On-Chip Oscillator to High-Speed On-Chip Oscillator Clock.

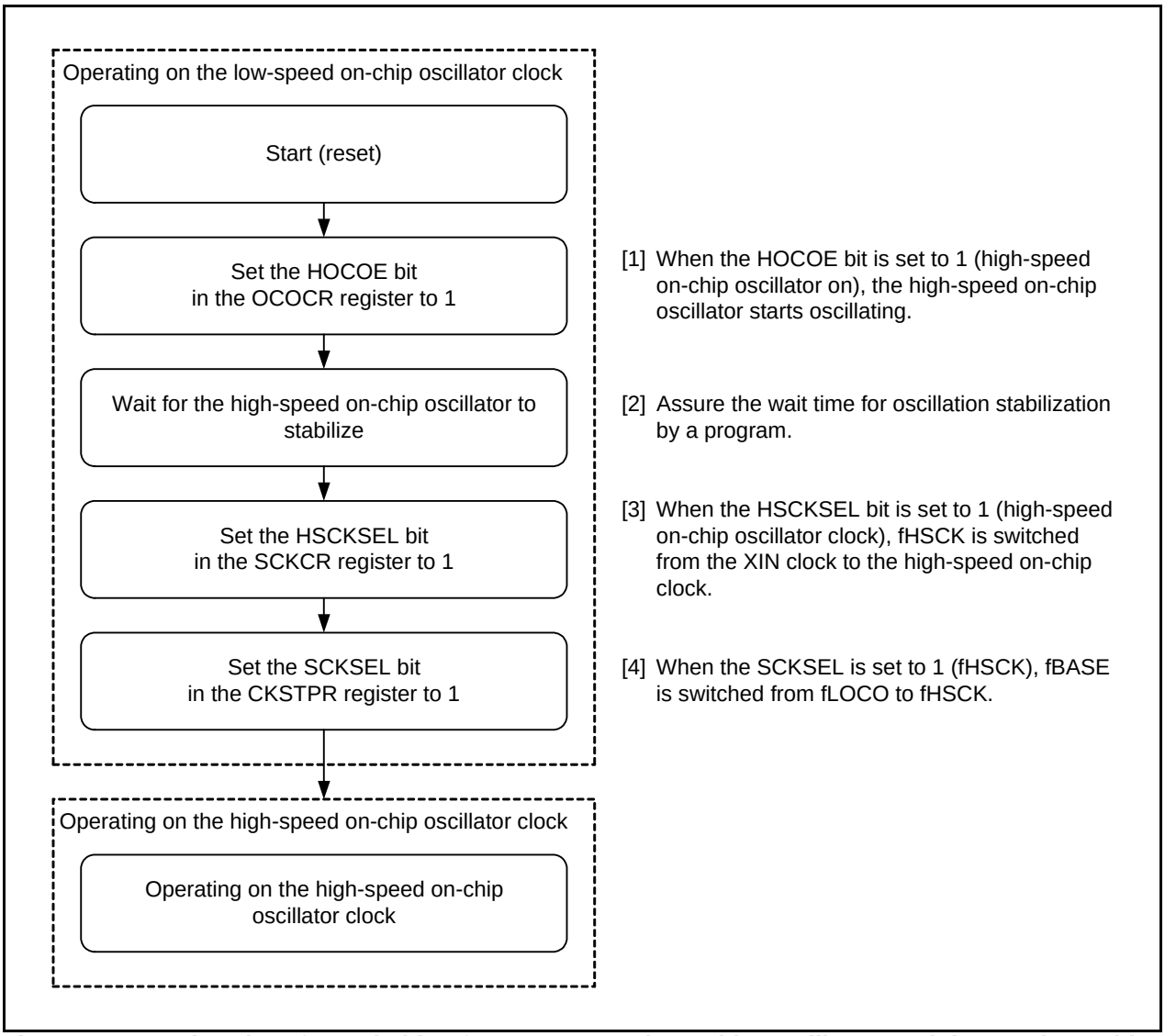


Figure 9.6 Flowchart for Switching from Low-Speed On-Chip Oscillator to High-Speed On-Chip Oscillator Clock

9.4.6.2 Procedure for Switching System Base Clock to XIN Clock

Figure 9.7 shows the Flowchart for Switching from Low-Speed On-Chip Oscillator to XIN Clock.

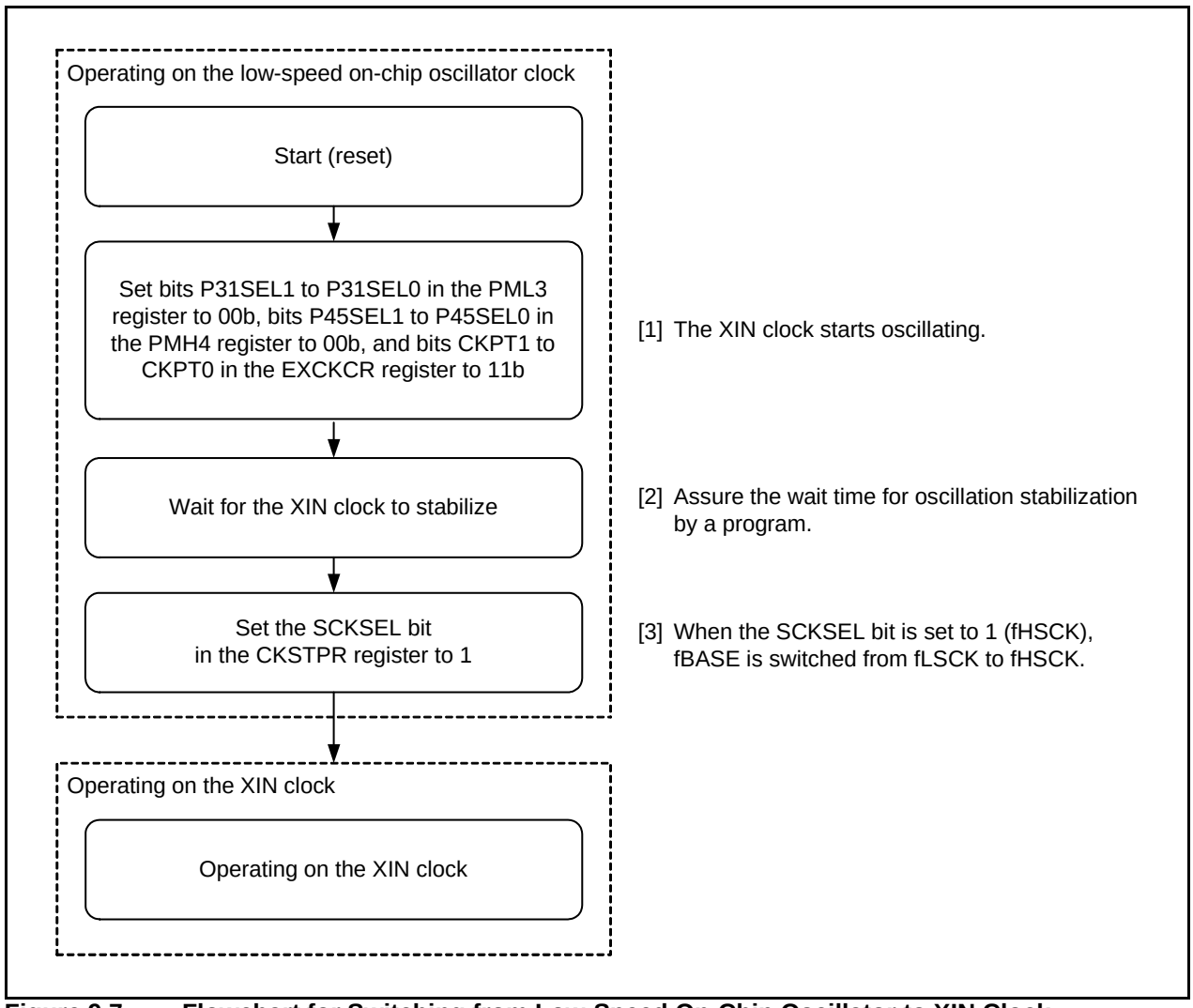


Figure 9.7 Flowchart for Switching from Low-Speed On-Chip Oscillator to XIN Clock

9.5 Oscillation Stop Detection Function

The oscillation stop detection function is used to detect whether the XIN clock oscillation is stopped.
Whether this function is enabled can be selected by the XINBAKE bit in the BAKCR register. To enable the oscillation stop detection function, set the LSCKSEL bit in the SCKCR register to 0 (low-speed on-chip oscillator).
Table 9.9 lists the Oscillation Stop Detection Function Specifications.
When the XIN clock is selected as the system base clock and bits CKSWIE to XINBAKE in the BAKCR register are set to 11b (interrupt request enabled, oscillation stop detection function enabled), if the XIN clock is stopped, the states will change as follows:

- The low-speed on-chip oscillator oscillates. However, the value in the LOCODIS bit in the OCOCR register does not change.
- The SCKSEL bit in the CKSTPR register = 0 (fLSCK)
- The XINHALT bit in the BAKCR register = 0 (external XIN clock halted)
- An oscillation stop detection interrupt is generated.

Table 9.9 Oscillation Stop Detection Function Specifications

Item	Specification
Clock frequency range for oscillation stop detection	f(XIN) ≥ 2 MHz
Condition for enabling the oscillation stop detection function	Set bits CKSWIE through XINBAKE to 11b (interrupt request enabled, oscillation stop detection function enabled).
Operation at oscillation stop detection	An oscillation stop detection interrupt is generated.

9.5.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares a vector with the watchdog timer and voltage monitor 1 interrupts. To use both the oscillation stop detection and watchdog timer interrupts, the interrupt source needs to be determined. See **11.8 How to Determine Interrupt Sources** for how to determine interrupt sources.
- When the XIN clock starts oscillating after oscillation is stopped, switch the XIN clock to the clock source for the CPU clock and the peripheral functions by a program.
  Figure 9.7 shows the Flowchart for Switching from Low-Speed On-Chip Oscillator to XIN Clock.
- The oscillation stop detection function can stop the XIN clock by an external cause. In that case, set bits CKSWIE to XINBAKE in the BAKCR register to 00b (interrupt request disabled, oscillation stop detection function disabled) to stop or oscillate the XIN clock by a program (to select stop mode or change bits CKPT0 to CKPT1 in the EXCKCR register).
- This function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits CKSWIE to XINBAKE in the BAKCR register to 00b (interrupt request disabled, oscillation stop detection function disabled).
- After the oscillation stop is detected, the low-speed on-chip oscillator is used as the clock source for the CPU clock and the peripheral functions. To reduce power consumption, the low-speed on-chip oscillator can be set to stop while the oscillation stop detection function is enabled. In that case, allow the low-speed on-chip oscillator to automatically oscillate when the stop of the XIN clock is detected, then switch the system clock after the wait time for oscillation stabilization.

9.6 Notes on Clock Generation Circuit

9.6.1 Oscillation Stop Detection Function

The oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz, so set bits CKSWIE to XINBAKE in the BAKCR register to 00b (interrupt request disabled, oscillation stop detection function disabled).

9.6.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

10. Power Control

Power control refers to controlling power consumption by selecting or stopping the CPU clock and the peripheral function clocks.

10.1 Overview

There are three power control modes. Standard operating mode is further divided into four modes depending on the system base clock (fBASE).

Table 10.1 Types of Modes

Item		Description	
Standard operating mode		The CPU and the peripheral functions operate.	
	High-speed clock mode	System base clock (fBASE)	XIN clock
	Low-speed clock mode		XCIN clock
	High-speed on-chip oscillator mode		High-speed on-chip oscillator clock
	Low-speed on-chip oscillator mode		Low-speed on-chip oscillator clock
Wait mode		The CPU is stopped and the peripheral functions operate.	
Stop mode		The CPU and the peripheral functions are stopped, and power consumption is lowest.	

Figure 10.1 shows the Power Control State Transition Diagram.

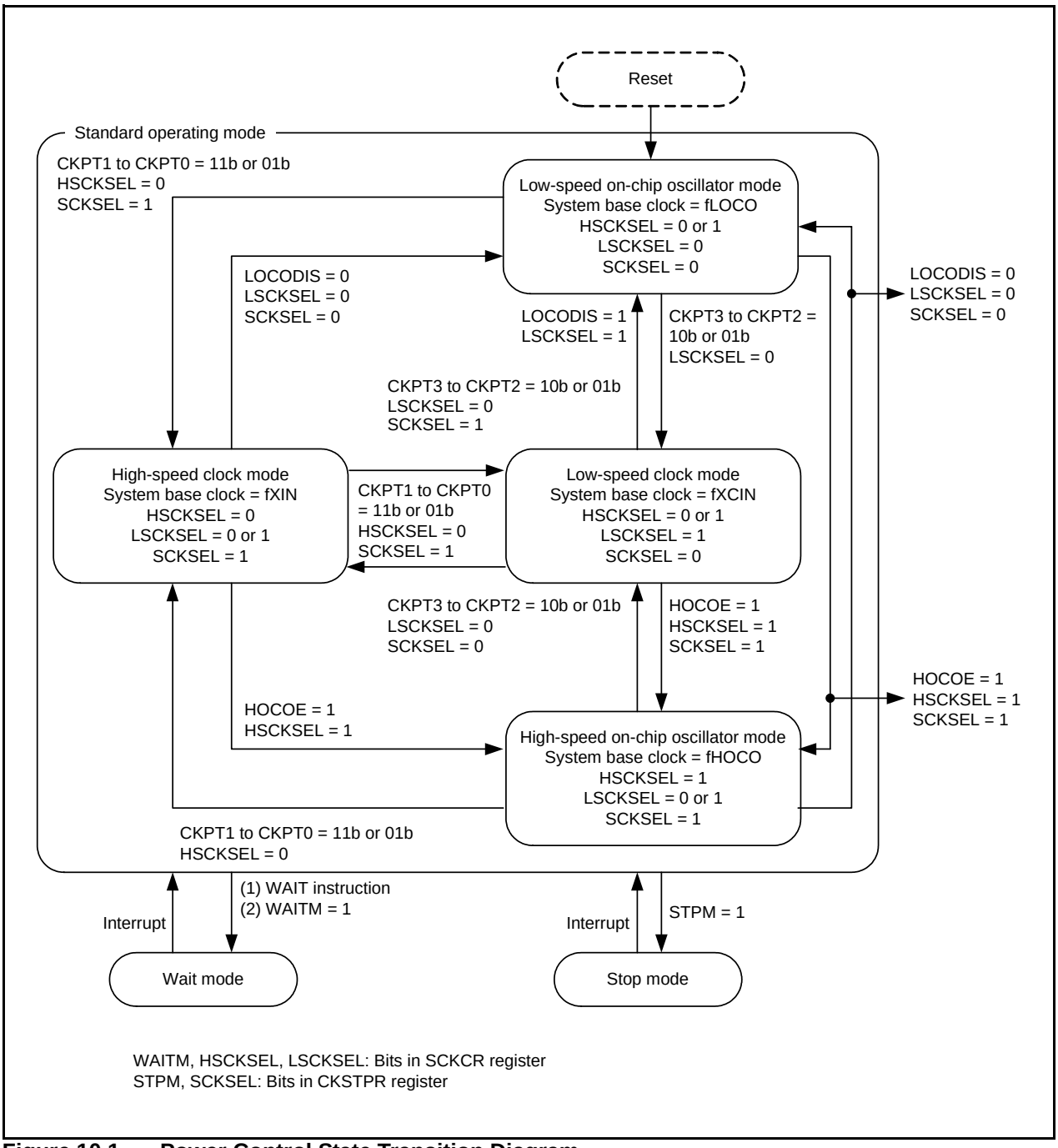


Figure 10.1 Power Control State Transition Diagram

10.2 Standard Operating Mode

In standard operating mode, the system clock is supplied to operate the CPU and the peripheral functions. Power consumption control is implemented by controlling the frequency of the system clock or CPU clock.
The higher the CPU clock frequency, the higher processing power. The lower the CPU clock frequency, the lower the power consumption. Stopping unnecessary oscillation circuits will further reduce power consumption.
When the clock sources for the CPU clock are switched, the new clock needs to be oscillating and stable. Assure the wait time for the new clock oscillation to stabilize by a program before switching the clocks.
Table 10.2 lists the Register Settings in Standard Operating Mode.

Table 10.2 Register Settings in Standard Operating Mode

Mode	Register	OCOCR		SCKCR		CKSTPR	EXCKCR			
	Bit	HOCOE	LOCODIS	HSCKSEL	LSCKSEL	SCKSEL	CKPT3	CKPT2	CKPT1	CKPT0
	Content to be Switched	fHOCO Oscillate/ Stop	fLOCO Oscillate/ Stop	XIN/ fHOCO	XCIN/ fLOCO	fLSCK/ fHSCK	P4_6 and P4_7 Pin Function		P3_1 and P4_5 Pin Function	
High-speed clock mode		—	—	0 (XIN)	—	1 (fHSCK)	—	—	1	1
Low-speed clock mode		—	—	—	1 (XCIN)	0 (fLSCK)	1	0	—	—
High-speed on-chip oscillator mode		1 (oscillate)	—	1 (fHOCO)	—	1 (fHSCK)	—	—	—	—
Low-speed on-chip oscillator mode		—	0 (oscillate)	—	0 (fLOCO)	0 (fLSCK)	—	—	—	—

—: Indicates that either 0 or 1 can be set.
The setting in ( ) is selected.

10.2.1 High-Speed Clock Mode

When the HSCKSEL bit in the SCKCR register is 0 (XIN clock) and the SCKSEL bit in the CKSTPR register is 1 (fHSCK), the XIN clock is used as the system base clock (fBASE). At this time, the system clock is obtained by dividing the XIN clock by any value from 1 (no division) to 256. The CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32. Also, the peripheral function clock is obtained by dividing the system clock with the prescaler. In addition, fLOCO when the LOCODIS bit is 0 (low-speed on-chip oscillator on).

10.2.2 Low-Speed Clock Mode

When the LSCKSEL bit in the SCKCR register is 1 (XCIN clock) and the SCKSEL bit in the CKSTPR register is 0 (fLSCK), the XCIN clock is used as the system base clock (fBASE). At this time, the system clock is obtained by dividing the XCIN clock by any value from 1 (no division) to 256. The CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32. Also, the peripheral function clock is obtained by dividing the system clock with the prescaler. In addition, fHOCO can be used as the peripheral function clock when the HOCOE bit in the OCOCR register is 1 (high-speed on-chip oscillator on).
In this mode, low-power operation can be enabled by stopping the XIN clock and the high-speed on-chip oscillator and setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled). Furthermore, if wait mode is entered from this mode, power consumption in wait mode can be reduced even further by setting the VCA2 register LPE bit to 1 (low-power-consumption wait mode enabled).
For details on how to reduce power consumption, see **10.5 Reducing Power Consumption**.

10.2.3 High-Speed On-Chip Oscillator Mode

When the HOCOE bit in the OCOCR register is 1 (high-speed on-chip oscillator on), the HSCKSEL bit in the SCKCR register is 1 (high-speed on-chip oscillator clock), and the SCKSEL bit in the CKSTPR register is 1 (fHSCK), the high-speed on-chip oscillator clock is used as the system base clock (fBASE). At this time, the system clock is obtained by dividing the high-speed on-chip oscillator clock by any value from 1 (no division) to 256. The CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32. Also, the peripheral function clock is obtained by dividing the system clock with the prescaler. In addition, fHOCO can be used as the peripheral function clock when the HOCOE bit is 1 (high-speed on-chip oscillator on), and fLOCO when the LOCODIS bit is 0 (low-speed on-chip oscillator on).

10.2.4 Low-Speed On-Chip Oscillator Mode

When the LOCODIS bit in the OCOCR register is 0 (low-speed on-chip oscillator on), the LSCKSEL bit in the SCKCR register is 0 (low-speed on-chip oscillator), and the SCKSEL bit in the CKSTPR register is 0 (fLSCK), the low-speed on-chip oscillator clock is used as the system base clock (fBASE). At this time, the system clock is obtained by dividing the low-speed on-chip oscillator clock by any value from 1 (no division) to 256. The CPU clock is obtained by dividing the system clock by 1 (no division), 2, 4, 8, 16, or 32. Also, the peripheral function clock is obtained by dividing the system clock with the prescaler. In addition, fHOCO can be used as the peripheral function clock when the HOCOE bit in the OCOCR register is 1 (high-speed on-chip oscillator on), and fLOCO when the LOCODIS bit is 0 (low-speed on-chip oscillator on).
In this mode, low-power operation can be enabled by stopping the XIN clock and the high-speed on-chip oscillator and setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled). Furthermore, if wait mode is entered from this mode, power consumption in wait mode can be reduced even further by setting the VCA2 register LPE bit to 1 (low-power-consumption wait mode enabled).
For details on how to reduce power consumption, see **10.5 Reducing Power Consumption**.

10.3 Wait Mode

The watchdog timer when count source protection mode is disabled and the CPU clock is used is stopped. The XIN clock, the XCIN clock, and the high-speed/low-speed on-chip oscillator clock are not stopped, so the peripheral functions that use these clocks continue operating. The system clock and the peripheral function clock can be stopped with WCKSTP bit in the CKSTPR register. At this time, the peripheral functions that use the system clock and a divided system clock generated by the prescaler are stopped.

10.3.1 Peripheral Function Clock Stop Function

When the WCKSTP bit in the CKSTPR register is 1 (peripheral function clock stopped in wait mode), the system clock and the prescaler are stopped in wait mode to reduce power consumption. At this time, the peripheral functions that use the system clock and a divided system clock generated by the prescaler are stopped.

10.3.2 Entering Wait Mode

Wait mode is entered when the WAIT instruction is executed or the WAITM bit in the SCKCR register is set to 1 (wait mode is entered).

10.3.3 Pin States in Wait Mode

The I/O ports retain the states immediately before wait mode is entered.

10.3.4 Returning from Wait Mode

A reset or a peripheral function interrupt is used to return from wait mode.
Peripheral function interrupts are affected by the WCKSTP bit in the CKSTPR register. When the WCKSTP bit is 0 (system clock is supplied in wait mode), the peripheral function interrupts can be used to return from wait mode. When the WCKSTP bit is 1 (system clock is stopped in wait mode), the peripheral functions that use the peripheral function clock are stopped. Only the peripheral function interrupts that operate using external signals, fAD, the high-speed on-chip oscillator clock, or the low-speed on-chip clock (oscillation of each oscillator is necessary) can be used to return from wait mode.
Table 10.3 lists the Interrupts Used to Return from Wait Mode and Usage Conditions.

Table 10.3 Interrupts Used to Return from Wait Mode and Usage Conditions

Interrupt	CKSTPR Register	
	When WCKSTP Bit = 0	When WCKSTP Bit = 1
Oscillation stop detection interrupt	Usable	Not usable.
$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ interrupts	Usable	Usable without a filter.
Key input interrupt	Usable	Usable
Periodic timer interrupt	Usable when fLOCO/16 is selected as the count source.	Not usable.
Timer RJ2 interrupt	Usable in all modes.	• Usable without a filter in event counter mode. • Usable when fHOCO, fXCIN, or fXCIN32 is selected as the count source.
Timer RB2 interrupt	Usable in all modes.	• Usable when timer RJ2 is used without a filter in event counter mode, and timer RJ2 underflow is selected as the count source for timer RB2. • Usable when fHOCO, fXCIN, or fXCIN32 is selected as the count source for timer RJ2, and timer RJ2 underflow is selected as the count source for timer RB2.
Timer RC interrupt	Usable in all modes.	Not usable.
Timer RK interrupt	Usable	Usable when fHOCO is selected as the count source.
Timer RE2 interrupt	Usable	Usable when fXCIN is selected as the count source.
Serial interface interrupt	Usable with an internal clock or external clock supplied.	Usable with an external clock supplied.
A/D conversion interrupt	Usable	Usable when the flash memory operates and fAD is selected as the A/D conversion clock.
Voltage monitor 1 interrupt	Usable	Usable
Comparator B1 interrupt	Usable	Usable without a filter.
Comparator B3 interrupt	Usable	Usable without a filter.

Figure 10.2 shows the Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed.
When a peripheral function interrupt is used to return from wait mode, the following items must be set before executing the WAIT instruction:

(1) Set the interrupt priority level in bits ILVLi0 to ILVLi1 or bits ILVLi4 to ILVLi5 in the interrupt priority level registers for the peripheral function interrupts that are used to return from wait mode. Also, set 00b (level 0 (interrupt disabled)) in bits ILVLi1 to ILVLi0 or bits ILVLi5 to ILVLi4 for the peripheral function interrupts that are not to be used to return from wait mode.
(2) Set the I flag to 1 (maskable interrupts enabled).
(3) Operate the peripheral functions to be used to return from wait mode.

The system base clock when returning from wait mode by a peripheral interrupt is the clock set by the WAITRS bit in the CKRSCR register. At this time, bits PHISSEL0 to PHISSEL2 in the SCKCR register and the SCKSEL bit in the CKSTPR register are automatically changed according to bits PHISRS and WAITRS.
If the system base clock when returning is different from the clock used immediately before entering wait mode, a period until the clock supply (oscillation stabilization time) is generated automatically. If the system base clock when returning is the high-speed on-chip oscillator clock, oscillation is started when an interrupt request is generated. If the system base clock is the XIN clock, set pins P3_1 and P4_5 to XIN oscillation by a program to start oscillation before entering wait mode.
Depending on the clock to be used, set appropriate values for oscillation stabilization time using bits CKST0 to CKST3 in the CKRSCR register. It is unnecessary to generate a wait time by a program. When returning from wait mode using the same clock as the one used immediately before entering the mode, no oscillation stabilization time is generated.

FMR0 Register FMSTP Bit	FMR1 Register WTFMSTP Bit	VCA2 Register LPE Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Clock Stabilization Time (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	1 (flash memory is stopped in wait mode)	0 (low-power-consumption wait mode disabled)	0 µs	60 µs (max.)	Set by bits CKST0 to CKST3 in the CKRSCR register if the clocks are switched when returning from wait mode 0 if the clocks are not switched when returning from wait mode	CPU clock period × 2 cycles	CPU clock period × 20 cycles	The total on the left amounts to the time from wait mode until execution of an interrupt routine.
		1 (low-power-consumption wait mode enabled)	100 µs (max.)					
1 (flash memory is stopped)	—	0 (low-power-consumption wait mode disabled)	0 µs	— (Flash memory is not activated)				
		1 (low-power-consumption wait mode enabled)	100 µs (max.)					
0 (flash memory operates)	0 (flash memory operates in wait mode)	0 (low-power-consumption wait mode disabled)	0 µs					
		1 (low-power-consumption wait mode enabled)	—					Setting prohibited

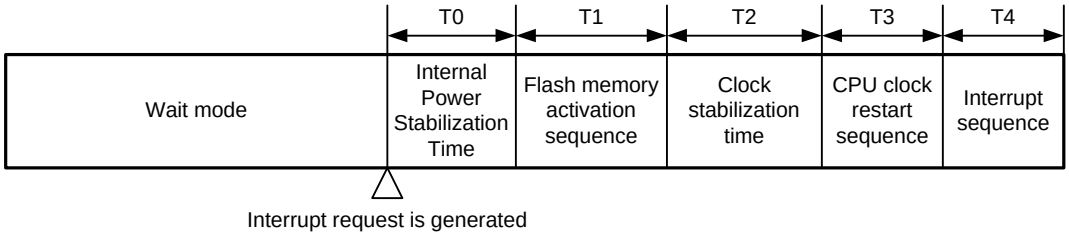


Figure 10.2 Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed

Figure 10.3 shows the Time from Wait Mode to First Instruction Execution after Exit after WAITM Bit in SCKCR Register is Set to 1 (Wait Mode is Entered).

When a peripheral function interrupt is used to return from wait mode, the following items must be set before setting the WAITM bit to 1:

(1) Set the I flag to 0 (maskable interrupt disabled).

(2) Set the interrupt priority level in bits ILVLi0 to ILVLi1 or bits ILVLi4 to ILVLi5 in the interrupt priority level registers for the peripheral function interrupts that are used to return from wait mode. Also, set 00b (level 0 (interrupt disabled)) in bits ILVLi1 to ILVLi0 or bits ILVLi5 to ILVLi4 for the peripheral function interrupts that are not to be used to return from wait mode.

(3) Operate the peripheral functions to be used to return from wait mode.

After the MCU exits from wait mode without executing any interrupt for external interrupts ($\overline{INT0}$ to $\overline{INT3}$ and $\overline{KI0}$ to $\overline{KI3}$), bits IRI0 to IRI3 and IRKI (external interrupt request flags) in the IRR3 register are not automatically, set to 0. Set these bits to 0 by a program.

The system base clock when returning from wait mode by a peripheral interrupt is the clock set by the WAITRS bit in the CKRSCR register. At this time, bits PHISSEL0 to PHISSEL2 in the SCKCR register and the SCKSEL bit in the CKSTPR register are automatically changed according to bits PHISRS and WAITRS.

If the system base clock when returning is different from the clock used immediately before entering wait mode, a period until the clock supply (oscillation stabilization time) is generated automatically. If the system base clock when returning is the high-speed on-chip oscillator clock, oscillation is started when an interrupt request is generated. If the system base clock is the XIN clock, set pins P3_1 and P4_5 to XIN oscillation by a program to start oscillation before entering wait mode.

Depending on the clock to be used, set appropriate values for oscillation stabilization time using bits CKST0 to CKST3 in the CKRSCR register. It is unnecessary to generate a wait time by a program. When returning from wait mode using the same clock as the one used immediately before entering the mode, no oscillation stabilization time is generated.

FMR0 Register FMSTP Bit	FMR1 Register WTFMSTP Bit	VCA2 Register LPE Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Clock Stabilization Time (T2)	Time until CPU Clock Supply (T3)	Remarks
0 (flash memory operates)	1 (flash memory is stopped in wait mode)	0 (low-power-consumption wait mode disabled)	0 μs	60 μs (max.)	Set by bits CKST0 to CKST3 in the CKRSCR register if the clocks are switched when returning from wait mode 0 if the clocks are not switched when returning from wait mode	CPU clock period × 2 cycles	The total on the left amounts to the time from wait mode until execution of an interrupt routine.
		1 (low-power-consumption wait mode enabled)	100 μs (max.)				
1 (flash memory is stopped)	—	0 (low-power-consumption wait mode disabled)	0 μs	— (Flash memory is not activated)			
		1 (low-power-consumption wait mode enabled)	100 μs (max.)				
0 (flash memory operates)	0 (flash memory operates in wait mode)	0 (low-power-consumption wait mode disabled)	0 μs				
		1 (low-power-consumption wait mode enabled)	—				Setting prohibited

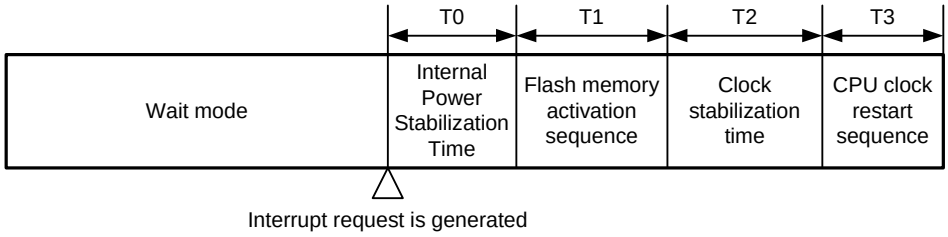


Figure 10.3 Time from Wait Mode to First Instruction Execution after Exit after WAITM Bit in SCKCR Register is Set to 1 (Wait Mode is Entered)

10.4 Stop Mode

All oscillations except the XCIN clock are stopped in stop mode. Thus, the CPU clock and the peripheral function clocks (except the XCIN clock) are stopped, and the CPU and the peripheral functions (except the functions with the XCIN clock selected) that operate using these clocks are stopped. However, when the low-speed on-chip oscillator is selected as the count source for the watchdog timer (in count source protection mode or when bits WDTC7 to WDTC6 in the WDTC register are set to 11b (division of low-speed on-chip oscillator by 16)), the low-speed on-chip oscillator oscillates. To stop the XCIN clock in stop mode, set bits CKPT3 to CKPT2 in the EXCKCR register to 00b (P4_6: I/O port, P4_7: I/O port) and then enter stop mode.
Power consumption is lowest compared to other modes. When the voltage applied to the VCC pin is VRAM or above, the content of the internal RAM is retained.

10.4.1 Entering Stop Mode

Stop mode is entered when the STPM bit in the CKSTPR register is set to 1 (all clocks are stopped (stop mode)).

10.4.2 Pin States in Stop Mode

The I/O ports retain the states immediately before the MCU enters stop mode.
When bits CKPT1 to CKPT0 in the EXCKCR register are 11b (P3_1: XIN, P4_5: XOUT), pins XIN (P3_1) and XOUT (P4_5) become high impedance in the stop mode. When bits CKPT1 to CKPT0 in the EXCKCR register are 01b (P3_1: XIN clock input (external clock input), P4_5: I/O port), do not make a transition to stop mode.

10.4.3 Returning from Stop Mode

A reset or a peripheral function interrupt is used to return from stop mode.
Table 10.4 lists the Interrupts Used to Return from Stop Mode and Usage Conditions.

Table 10.4 Interrupts Used to Return from Stop Mode and Usage Conditions

Interrupt	Usage Condition
$\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ interrupts	Usable without a filter.
Key input interrupt	Usable
Timer RJ2 interrupt	• Usable when an external pulse is counted without a filter in event counter mode. • Usable when fXCIN or fXCIN32 is selected as the count source.
Timer RB2 interrupt	• Usable when timer RJ2 is used without a filter in event counter mode and timer RJ2 underflow is selected as the count source for timer RB2. • Usable when fXCIN or fXCIN32 is selected as the count source for timer RJ2, and timer RJ2 underflow is selected as the count source for timer RB2.
Timer RE2 interrupt	Usable when fXCIN is selected as the count source.
Serial interface interrupt	Usable with an external clock or fXCIN supplied.
Voltage monitor 1 interrupt	Usable in digital filter disabled mode (when the VW1C1 bit in the VW1C register is 1).
Comparator B1 interrupt	Usable without a filter.
Comparator B3 interrupt	Usable without a filter.

Figure 10.4 shows the Sequence from Stop Mode to Interrupt Routine Execution.
When a peripheral function interrupt is used to return from stop mode, the following items must be set before setting the STPM bit in the CKSTPR register to 1 (all clocks are stopped (stop mode)):

(1) Set the interrupt priority level in bits ILVLi0 to ILVLi1 or bits ILVLi4 to ILVLi5 in the interrupt priority level registers for the peripheral function interrupts that are used to return from stop mode. Also, set 00b (level 0 (interrupt disabled)) in bits ILVLi1 to ILVLi0 or bits ILVLi5 to ILVLi4 for the peripheral function interrupts that are not to be used to return from stop mode.
(2) Set the I flag to 1 (maskable interrupt enabled).
(3) Operate the peripheral function to be used to return from stop mode.

The system base clock when returning from stop mode by a peripheral interrupt is the clock set by the STOPRS bit in the CKRSCR register. At this time, bits PHISSEL0 to PHISSEL2 in the SCKCR register and the SCKSEL bit in the CKSTPR register are automatically changed according to bits PHISRS and STOPRS.
When an interrupt is generated, oscillation is started, and a period until the clock supply (oscillation stabilization time) is generated automatically. If the system base clock when returning is the XIN clock, set pins P3_1 and P4_5 to XIN oscillation by a program before entering stop mode.
Depending on the clock to be used, set appropriate values for oscillation stabilization time using bits CKST0 to CKST3 in the CKRSCR register. It is unnecessary to generate a wait time by a program.

FMR0 Register FMSTP bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Clock Stabilization Time (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	100 μs (max.)	60 μs (max.)	Set by bits CKST0 to CKST3 in the CKRSCR register	CPU clock period × 2 cycles	CPU clock period × 20 cycles	The total on the left amounts to the time from stop mode to execution of an interrupt routine.
1 (flash memory is stopped)	100 μs (max.)	— (Flash memory is not activated)				

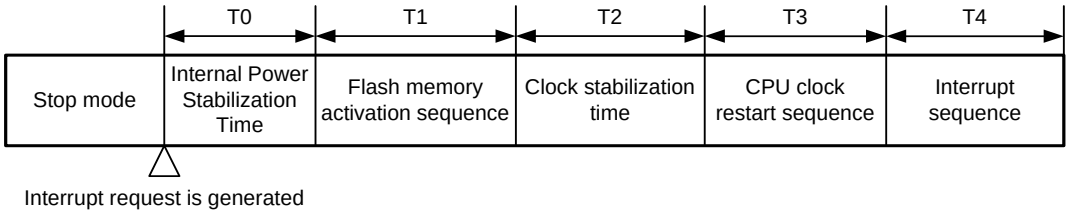


Figure 10.4 Sequence from Stop Mode to Interrupt Routine Execution

10.5 Reducing Power Consumption

The following describes key points and processing methods for reducing power consumption. They should be referred to when designing a system or creating a program.

10.5.1 Voltage Detection Circuit

When voltage monitor 1 is not used, set the VC1E bit in the VCA2 register to 0 (voltage detection 1 circuit disabled). When power-on reset or voltage monitor 0 reset is not used, set the VC0E bit in the VCA2 register to 0 (voltage detection 0 circuit disabled).

10.5.2 Ports

Even after entering wait mode or stop mode, the states of the I/O ports are retained. Current flows into the output ports in the active state. Shoot-through current flows into the input ports in the high-impedance state. Unnecessary ports should be set to input and fixed to a stable electric potential before entering wait mode or stop mode.

10.5.3 Clocks

Power consumption generally depends on the number of the operating clocks and their frequencies. The fewer the number of operating clocks or the lower their frequencies, the more power consumption decreases.
Unnecessary clocks should be stopped accordingly.
Stopping low-speed on-chip oscillator oscillation: LOCODIS bit in OCOCR register
Stopping high-speed on-chip oscillator oscillation: HOCOE bit in OCOCR register

10.5.4 Wait Mode and Stop Mode

Power consumption can be reduced in wait mode and stop mode.

10.5.5 Stopping Peripheral Function Clocks

If the peripheral function clocks f1 to f8192 are not necessary, set the PSCSTP bit in the CKSTPR register to 1 to stop these peripheral function clocks. If the peripheral function clocks f1 to f8192 are not necessary in wait mode, set the WCKSTP bit in the CKSTPR register to 1 to stop the system clock in wait mode.

10.5.6 Timers

When timer RJ2 is not used, set the TCKCUT bit in the TRJMR register to 1 (count source cutoff). Or set the MSTTRJ bit in the MSTCR register to 1 (standby).
When timer RB2 is not used, set the TCKCUT bit in the TRBMR register to 1 (count source cutoff). Or set the MSTTRB bit in the MSTCR register to 1 (standby).
When timer RC is not used, set the MSTTRC bit in the MSTCR register to 1 (standby).
When timer RK is not used, set the MSTTMRK bit in the MSTCR1 register to 1 (standby).
When timer RE2 is not used, set the MSTTRE bit in the MSTCR register to 1 (standby).

10.5.7 Serial Interface (UART0/UART1)

When the serial interface (UART0) is not used, set the MSTUART0 bit in the MSTCR register to 1 (standby).
When the serial interface (UART1) is not used, set the MSTUART1 bit in the MSTCR register to 1 (standby).

10.5.8 A/D Converter

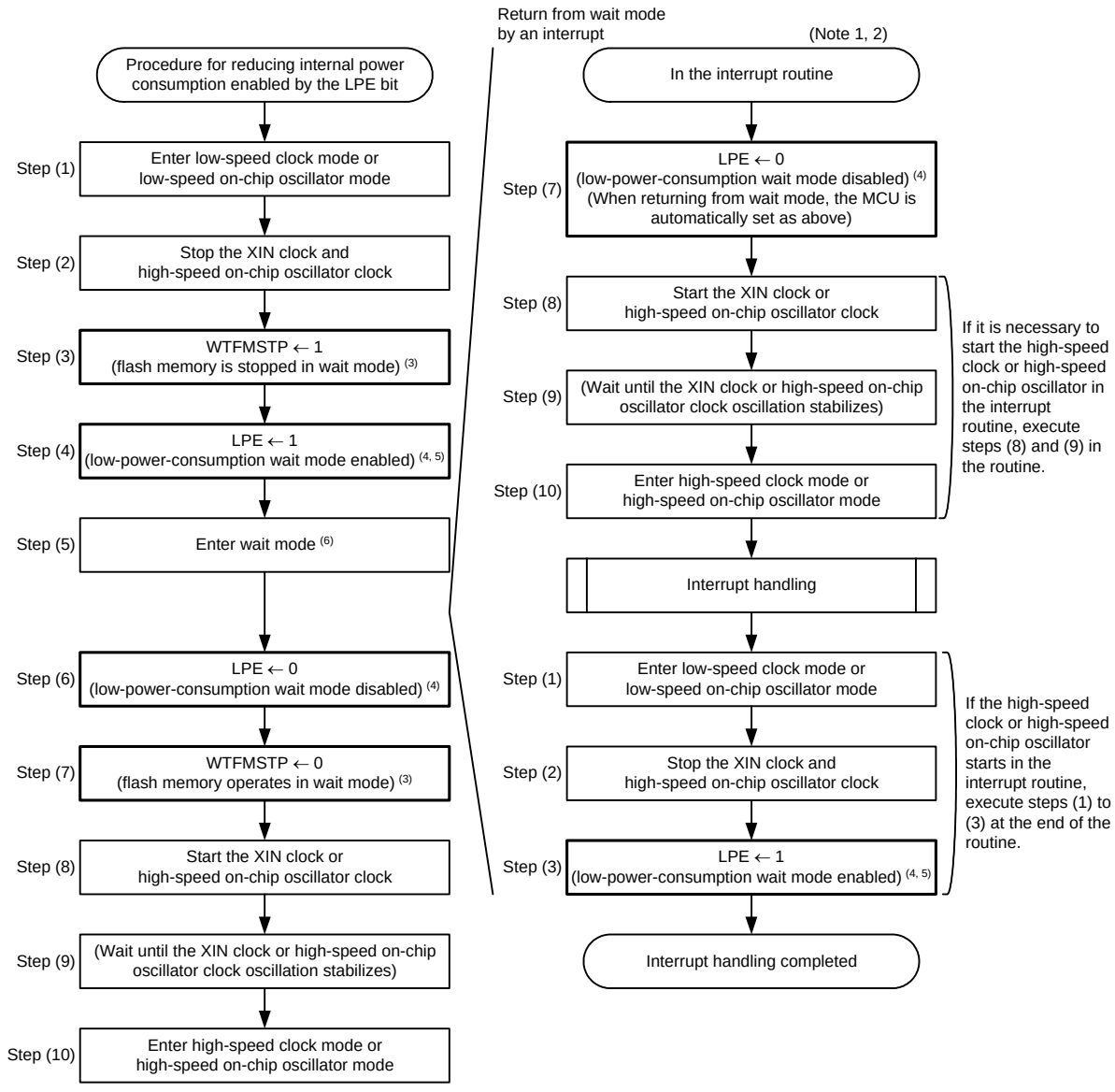
When the A/D converter is not used, set the MSTAD bit in the MSTCR register to 1 (standby).

10.5.9 Infrared Data Association (IrDA) Interface

When the infrared data association (IrDA) interface is not used, set the MSTIRDA bit in the MSTCR1 register to 1 (standby).

10.5.10 Reducing Internal Power Consumption

When entering wait mode using low-speed clock mode or low-speed on-chip oscillator mode, internal power consumption can be reduced using the LPE bit in the VCA2 register. To enable low internal power consumption using the LPE bit, follow **Figure 10.5 Procedure for Reducing Internal Power Consumption by Using LPE Bit**.



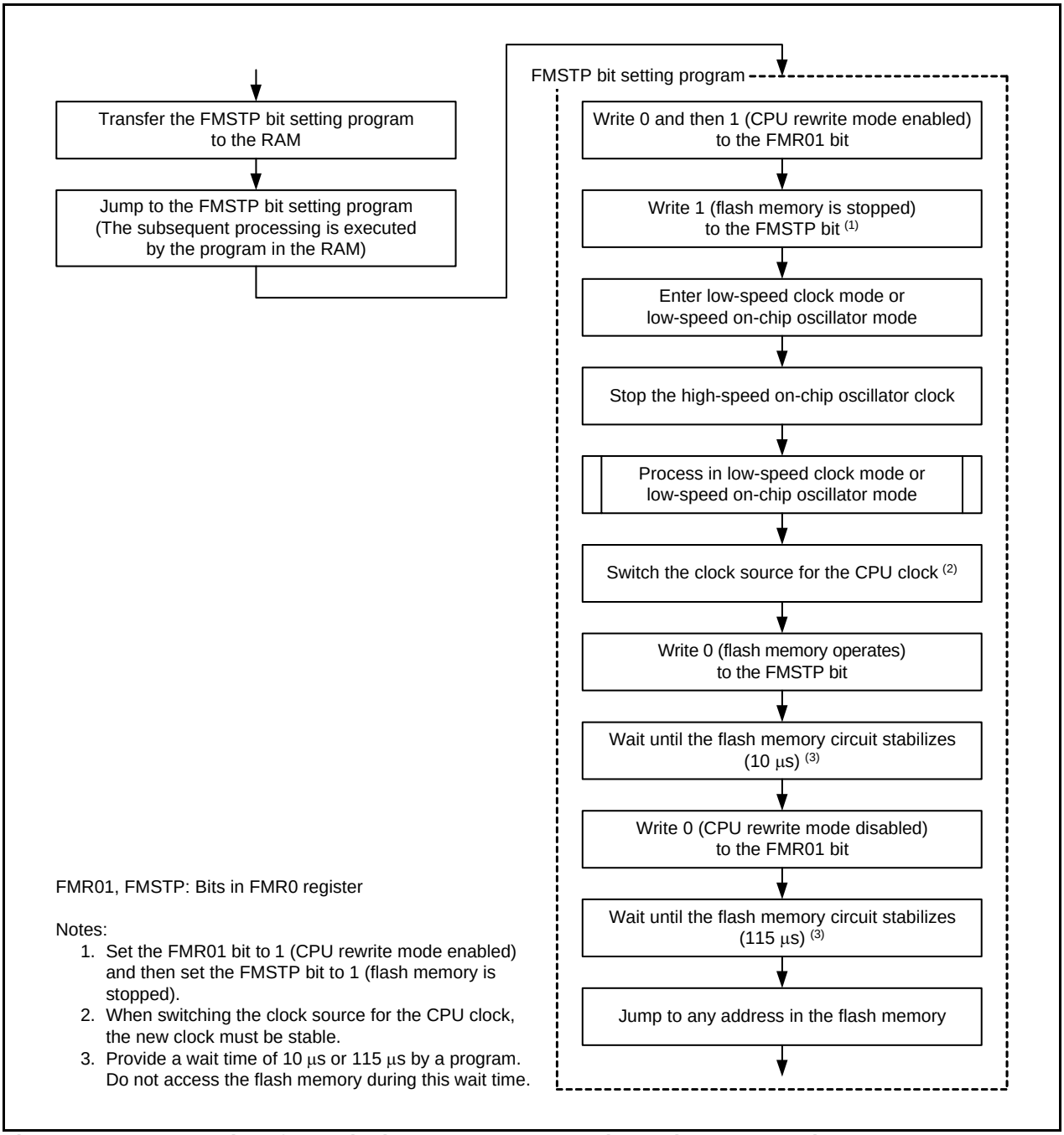
LPE: Bit in VCA2 register
WTFMSTP: Bit in FMR1 register

Notes:
1. Execute this routine for all interrupt processing that occurs in wait mode.
   However, this is not required if it is not necessary to start the high-speed clock or high-speed on-chip oscillator in the interrupt routine.
2. When a maskable interrupt request is generated in wait mode set by the WAITM bit in the SCKCR register, interrupt handling is not performed but execution is resumed immediately after the instruction used to set the WAITM bit to 1. See **10.3 Wait Mode** for returning from wait mode.
3. When the FMSTP bit in the FMR0 register is 1 (flash memory is stopped), the WTFMSTP bit is disabled. This setting is not required.
4. Do not write 0 to the LPE bit with the instruction immediately after 1 is written to the LPE bit. Sequential writes in the opposite order are also not allowed.
5. When the LPE bit is 1, do not set the STPM bit in the CKSTPR register to 1 (all clocks are stopped (stop mode)).
6. For entering wait mode, see **10.3 Wait Mode**.

Figure 10.5 Procedure for Reducing Internal Power Consumption by Using LPE Bit

10.5.11 Stopping Flash Memory

In low-speed clock mode or low-speed on-chip oscillator mode, the flash memory can be stopped using the FMSTP bit in the FMR0 register to further reduce the power consumption.
When the FMSTP bit is set to 1 (flash memory is stopped), the flash memory cannot be accessed. The FMSTP bit must be written by a program that has been transferred to the RAM.
When the MCU enters stop mode or wait mode with CPU rewrite mode disabled while the WTFMSTP bit is 1 (flash memory is stopped in wait mode), the power supply for the flash memory is automatically turned off. It is turned on again when the MCU exits stop mode or wait mode. This eliminates the need to set the FMR0 register.
Figure 10.6 shows the Procedure for Reducing Power Consumption Using FMSTP Bit.



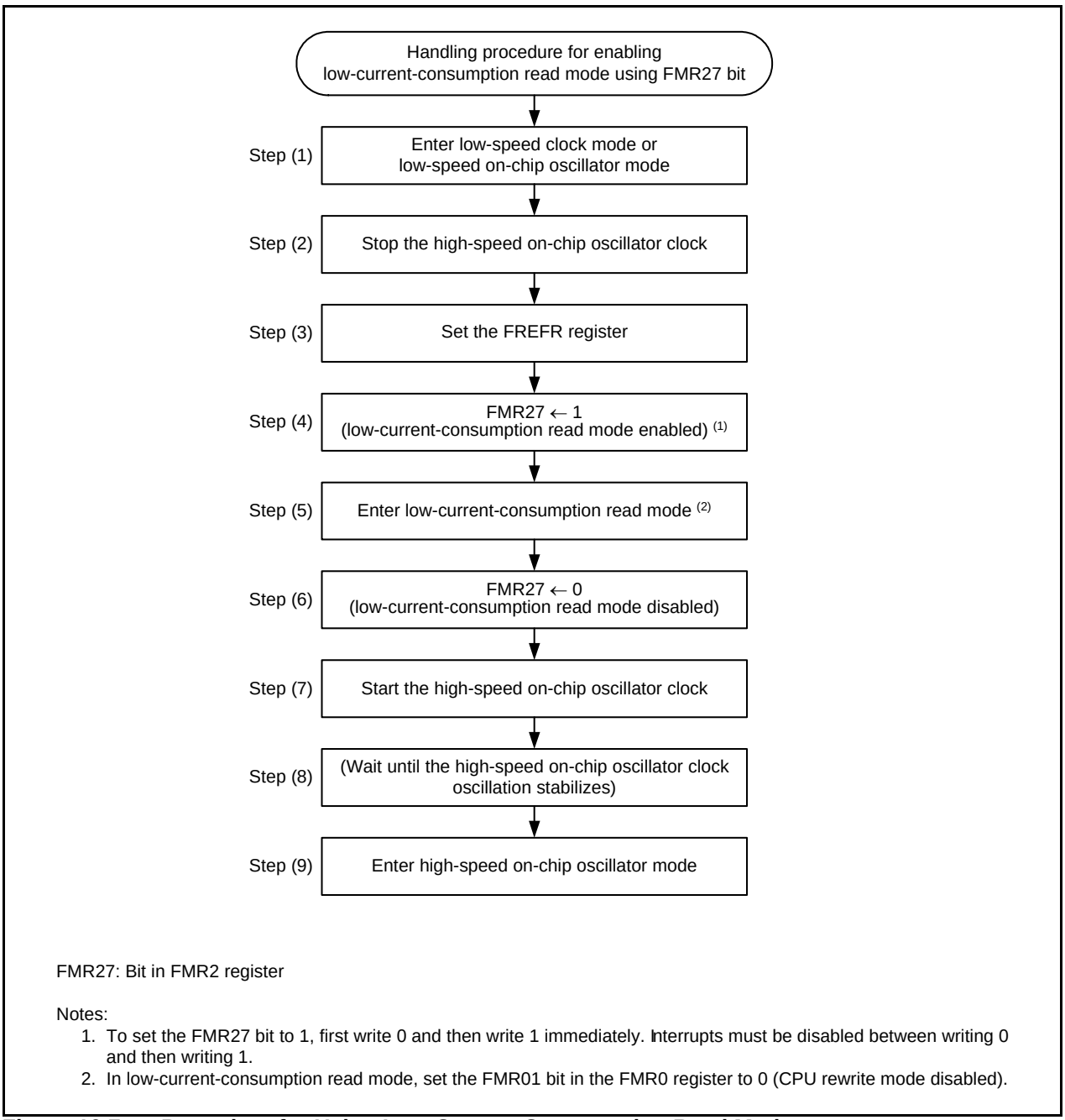
FMR01, FMSTP: Bits in FMR0 register

Notes:
1. Set the FMR01 bit to 1 (CPU rewrite mode enabled) and then set the FMSTP bit to 1 (flash memory is stopped).
2. When switching the clock source for the CPU clock, the new clock must be stable.
3. Provide a wait time of 10 µs or 115 µs by a program. Do not access the flash memory during this wait time.

Figure 10.6 Procedure for Reducing Power Consumption Using FMSTP Bit

10.5.12 Low-Current-Consumption Read Mode

In low-speed clock mode or low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Set the CPU clock (fs) to a frequency in the range of 3 kHz to 50 kHz.
Figure 10.7 shows the Procedure for Using Low-Current-Consumption Read Mode.



FMR27: Bit in FMR2 register

Notes:
1. To set the FMR27 bit to 1, first write 0 and then write 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
2. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).

Figure 10.7 Procedure for Using Low-Current-Consumption Read Mode

10.6 Notes on Power Control

10.6.1 Program Restrictions When Entering Wait Mode

To enter wait mode by setting the WAITM bit to 1, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the WAITM bit to 1.
To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before executing the WAIT instruction. The 4 bytes of instruction data following the instruction that sets the WAITM bit to 1 (wait mode is entered) or the WAIT instruction are prefetched from the instruction queue and then the program stops. Insert at least four NOP instructions after the instruction that sets the WAITM bit to 1 (wait mode is entered) or after the WAIT instruction.

• Program example to execute the WAIT instruction

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        FSET    I               ; Interrupt enabled
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

• Program example to set the WAITM bit to 1

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        BSET    0, PRCR         ; Writing to SCKCR register enabled
        FCLR    I               ; Interrupt disabled
        BSET    5, SCKCR        ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR         ; Writing to the SCKCR register disabled
        FSET    I               ; Interrupt enabled
```

10.6.2 Program Restrictions When Entering Stop Mode

When entering stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the STPM bit in the CKSTPR register to 1 (all clocks are stopped (stop mode)). The four bytes of instruction data following the instruction that sets the STPM bit to 1 are prefetched from the instruction queue and then the program stops.
Insert at least four NOP instructions following the JMP.B instruction immediately after the instruction that sets the STPM bit to 1.

• Program example to enter stop mode

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        BSET    0, PRCR         ; Writing to CKSTPR register enabled
        FSET    I               ; Interrupt enabled
        BSET    0, CKSTPR       ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

11. Interrupts

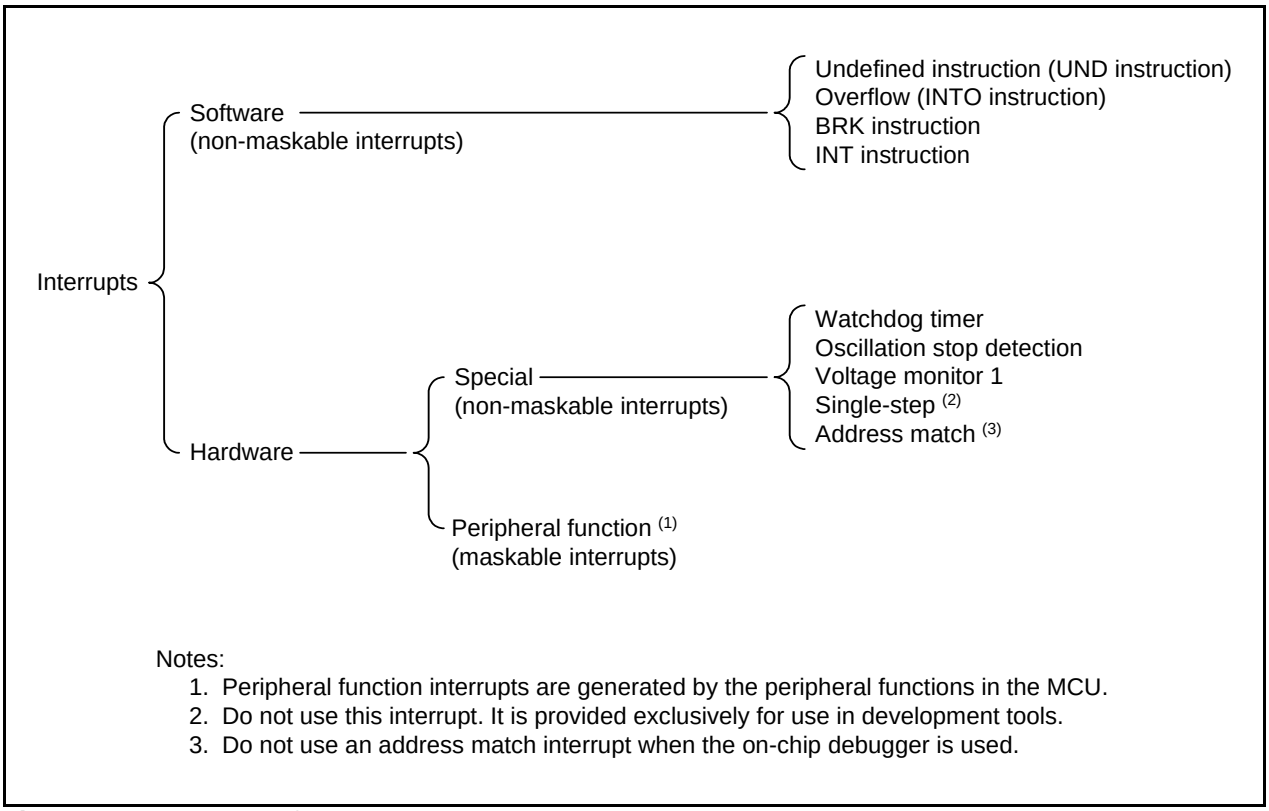
11.1 Overview

Interrupts are classified into non-maskable and maskable interrupts. These differ in whether or not the interrupt can be enabled or disabled by an interrupt enable flag (I flag) and in whether or not the interrupt priority level can be changed as listed in Table 11.1.

Table 11.1 Maskable/Non-Maskable Interrupts

	Disabling Interrupt by Interrupt Enable Flag (I Flag)	Changing Priority by Setting Interrupt Priority Level
Non-maskable interrupts	Not possible	Not possible
Maskable interrupts	Possible	Possible

Figure 11.1 shows the Types of Interrupts. Table 11.2 lists the Descriptions of Interrupts.



Notes:
1. Peripheral function interrupts are generated by the peripheral functions in the MCU.
2. Do not use this interrupt. It is provided exclusively for use in development tools.
3. Do not use an address match interrupt when the on-chip debugger is used.

Figure 11.1 Types of Interrupts

Table 11.2 Descriptions of Interrupts

Interrupt	Description
Undefined instruction interrupt	An unidentified instruction interrupt is generated when the UND instruction is executed.
Overflow interrupt	An overflow interrupt is generated when the O flag is 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that change the O flag are as follows: ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.
BRK instruction interrupt	A BRK interrupt is generated when the BRK instruction is executed.
INT instruction interrupt	An INT instruction interrupt is generated when the INT instruction is executed. Software interrupt numbers the INT instruction can specify are 0 to 63. The number is assigned to each peripheral function interrupt. When the INT instruction is executed specifying the number, the peripheral function interrupt with the same number can be executed. For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution, and the U flag is set to 0 (ISP) before the interrupt sequence is executed. The U flag is restored from the stack when the MCU returns from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.
Watchdog timer interrupt	This interrupt is generated by the watchdog timer. For details, see **8. Watchdog Timer**.
Oscillation stop detection interrupt	This interrupt is generated by the oscillation stop detection function. For details on the oscillation stop detection function, see **9. Clock Generation Circuit**.
Voltage monitor 1 interrupt	This interrupt is generated by the voltage detection circuit. For details on the voltage detection circuit, see **7. Voltage Detection Circuit**.
Single-step interrupt	Do not use this interrupt. It is provided exclusively for use in development tools.
Address match interrupt	When one of the AIENi0 bit (i = 0 or 1) in the AIENi register is 1 (enabled), an address match interrupt is generated immediately before executing the instruction that is stored at an address indicated by the corresponding AIADRi register (i = 0 or 1). For details on the address match interrupt, see **11.7 Address Match Interrupt**.
Peripheral function interrupt	A peripheral function interrupt is generated by a peripheral function in the MCU. For the interrupt sources for the corresponding peripheral function interrupt, see the interrupts and the vector table addresses as listed in **Table 11.6 Relocatable Vector Table**. For details on the peripheral functions, see the descriptions of individual peripheral functions.

11.2 Registers

Table 11.3 lists the Register Configuration for Interrupts.

Table 11.3 Register Configuration for Interrupts

Register Name	Symbol	After Reset	Address	Access Size
External Input Enable Register	INTEN	00h	00038h	8
INT Input Filter Select Register 0	INTF0	00h	0003Ah	8
INT Input Edge Select Register 0	ISCR0	00h	0003Ch	8
Key Input Enable Register	KIEN	00h	0003Eh	8
Interrupt Priority Level Register 0	ILVL0	00h	00040h	8
Interrupt Priority Level Register 1	ILVL1	00h	00041h	8
Interrupt Priority Level Register 2	ILVL2	00h	00042h	8
Interrupt Priority Level Register 3	ILVL3	00h	00043h	8
Interrupt Priority Level Register 4	ILVL4	00h	00044h	8
Interrupt Priority Level Register 5	ILVL5	00h	00045h	8
Interrupt Priority Level Register 6	ILVL6	00h	00046h	8
Interrupt Priority Level Register 7	ILVL7	00h	00047h	8
Interrupt Priority Level Register 8	ILVL8	00h	00048h	8
Interrupt Priority Level Register 9	ILVL9	00h	00049h	8
Interrupt Priority Level Register A	ILVLA	00h	0004Ah	8
Interrupt Priority Level Register B	ILVLB	00h	0004Bh	8
Interrupt Priority Level Register C	ILVLC	00h	0004Ch	8
Interrupt Priority Level Register D	ILVLD	00h	0004Dh	8
Interrupt Priority Level Register E	ILVLE	00h	0004Eh	8
Interrupt Monitor Flag Register 0	IRR0	00h	00050h	8
Interrupt Monitor Flag Register 1	IRR1	00h	00051h	8
Interrupt Monitor Flag Register 2	IRR2	00h	00052h	8
External Interrupt Flag Register	IRR3	00h	00053h	8
Address Match Interrupt Register 0	AIADR0L	00h	001C0h	8
	AIADR0M	00h	001C1h	8
	AIADR0H	00h	001C2h	8
Address Match Interrupt Enable Register 0	AIEN0	00h	001C3h	8
Address Match Interrupt Register 1	AIADR1L	00h	001C4h	8
	AIADR1M	00h	001C5h	8
	AIADR1H	00h	001C6h	8
Address Match Interrupt Enable Register 1	AIEN1	00h	001C7h	8

11.2.1 External Input Enable Register (INTEN)

Address 00038h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INT3EN	INT2EN	INT1EN	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit (1)	0: Disabled 1: Enabled	R/W
b1	INT1EN	$\overline{\text{INT1}}$ input enable bit (1)		R/W
b2	INT2EN	$\overline{\text{INT2}}$ input enable bit (1)		R/W
b3	INT3EN	$\overline{\text{INT3}}$ input enable bit (1)		R/W
b4	—	Reserved	Set to 0.	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—	Reserved	Set to 0.	R/W

Note:
1. Changing the INTiEN bit (i = 0 to 3) may set the IRIi bit (i = 0 to 3) in the IRR3 register to 1 (interrupt requested). See **11.9.4 Rewriting Registers PMLi (i = 1 to 4), PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN**.

11.2.2 INT Input Filter Select Register 0 (INTF0)

Address 0003Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	INT2F1	INT2F0	INT1F1	INT1F0	INT0F1	INT0F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{\text{INT0}}$ input filter select bits	b1 b0 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b1	INT0F1			R/W
b2	INT1F0	$\overline{\text{INT1}}$ input filter select bits	b3 b2 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b3	INT1F1			R/W
b4	INT2F0	$\overline{\text{INT2}}$ input filter select bits	b5 b4 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b5	INT2F1			R/W
b6	INT3F0	$\overline{\text{INT3}}$ input filter select bits	b7 b6 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b7	INT3F1			R/W

11.2.3 INT Input Edge Select Register 0 (ISCR0)

Address 0003Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3SB	INT3SA	INT2SB	INT2SA	INT1SB	INT1SA	INT0SB	INT0SA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0SA	$\overline{\text{INT0}}$ input edge select bits (1)	b1 b0 0 0: Interrupt request is generated on the falling edge of $\overline{\text{INT0}}$ input 0 1: Interrupt request is generated on the rising edge of $\overline{\text{INT0}}$ input 1 0: Do not set. 1 1: Interrupt request is generated on both the falling and rising edges of $\overline{\text{INT0}}$ input	R/W
b1	INT0SB			R/W
b2	INT1SA	$\overline{\text{INT1}}$ input edge select bits (1)	b3 b2 0 0: Interrupt request is generated on the falling edge of $\overline{\text{INT1}}$ input 0 1: Interrupt request is generated on the rising edge of INT1 input 1 0: Do not set. 1 1: Interrupt request is generated on both the falling and rising edges of $\overline{\text{INT1}}$ input	R/W
b3	INT1SB			R/W
b4	INT2SA	$\overline{\text{INT2}}$ input edge select bits (1)	b5 b4 0 0: Interrupt request is generated on the falling edge of $\overline{\text{INT2}}$ input 0 1: Interrupt request is generated on the rising edge of INT2 input 1 0: Do not set. 1 1: Interrupt request is generated on both the falling and rising edges of $\overline{\text{INT2}}$ input	R/W
b5	INT2SB			R/W
b6	INT3SA	$\overline{\text{INT3}}$ input edge select bits (1)	b7 b6 0 0: Interrupt request is generated on the falling edge of $\overline{\text{INT3}}$ input 0 1: Interrupt request is generated on the rising edge of $\overline{\text{INT3}}$ input 1 0: Do not set. 1 1: Interrupt request is generated on both the falling and rising edges of $\overline{\text{INT3}}$ input	R/W
b7	INT3SB			R/W

Note:

1. Changing bits INTiSA to INTiSB (i = 0 to 3) may set the IRIi bit (i = 0 to 3) in the IRR3 register to 1 (interrupt requested). See **11.9.4 Rewriting Registers PMLi (i = 1 to 4), PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN**.

11.2.4 Key Input Enable Register (KIEN)

Address 0003Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI3PL	KI3EN	KI2PL	KI2EN	KI1PL	KI1EN	KI0PL	KI0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0EN	$\overline{KI0}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	KI0PL	$\overline{KI0}$ input edge select bit (1)	0: Falling edge 1: Rising edge	R/W
b2	KI1EN	$\overline{KI1}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	KI1PL	$\overline{KI1}$ input edge select bit (1)	0: Falling edge 1: Rising edge	R/W
b4	KI2EN	$\overline{KI2}$ input enable bit	0: Disabled 1: Enabled	R/W
b5	KI2PL	$\overline{KI2}$ input edge select bit (1)	0: Falling edge 1: Rising edge	R/W
b6	KI3EN	$\overline{KI3}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	KI3PL	$\overline{KI3}$ input edge select bit (1)	0: Falling edge 1: Rising edge	R/W

Note:
1. Changing the bits KIiPL or KIiEN (i = 0 to 3) may set the IRKI bit in the IRR3 register to 1 (interrupt requested). See **11.9.4 Rewriting Registers PMLi (i = 1 to 4), PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN**.

11.2.5 Interrupt Priority Level Register i (ILVLi) (i = 0 to E)

Address 00040h to 0004Eh (ILVL0 to ILVLE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	ILVLi5	ILVLi4	—	—	ILVLi1	ILVLi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVLi0	Interrupt priority level setting bits	b1 b0 0 0: Level 0 (interrupt disabled) 0 1: Level 1 1 0: Level 2 1 1: Level 2	R/W
b1	ILVLi1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	ILVLi4	Interrupt priority level setting bits	b5 b4 0 0: Level 0 (interrupt disabled) 0 1: Level 1 1 0: Level 2 1 1: Level 2	R/W
b5	ILVLi5			R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The ILVLi register (i = 0 to E) is used to set the priority levels (levels 0 to 2) of the maskable interrupts. The settings in bits ILVLi0 to ILVLi1 or bits ILVLi4 to ILVLi5 in each register are used to decide the priority of the corresponding interrupt request.
See **Table 11.4 Correspondence between Interrupt Requests and ILVLi (i = 0 to E)** for the interrupt setting bits.
The interrupt priority level register must be rewritten only while no interrupt requests corresponding to that register are generated. See **11.9.7 Changing Interrupt Priority Levels and Flag Registers**.

Table 11.4 Correspondence between Interrupt Requests and ILVLi (i = 0 to E)

ILVLi Register	Bit							
	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	ILVLi5	ILVLi4	—	—	ILVLi1	ILVLi0
ILVL0	—	—	Flash ready		—	—	—	
ILVL1	—	—	—		—	—	Timer RK	
ILVL2	—	—	Comparator B3		—	—	Comparator B1	
ILVL3	—	—	Timer RC		—	—	—	
ILVL4	—	—	—		—	—	—	
ILVL5	—	—	—		—	—	Timer RE2	
ILVL6	—	—	Key input		—	—	—	
ILVL7	—	—	Synchronous serial communication unit (SSU)/I^{2}C bus interface		—	—	A/D conversion	
ILVL8	—	—	UART0 transmission		—	—	—	
ILVL9	—	—	UART1 transmission		—	—	UART0 reception	
ILVLA	—	—	$\overline{\text{INT2}}$		—	—	UART1 reception	
ILVLB	—	—	Periodic timer		—	—	Timer RJ2	
ILVLC	—	—	$\overline{\text{INT1}}$		—	—	Timer RB2	
ILVLD	—	—	—		—	—	$\overline{\text{INT3}}$	
ILVLE	—	—	$\overline{\text{INT0}}$		—	—	—	

—: Not used. The write value must be 0.
i = 0 to E

11.2.6 Interrupt Monitor Flag Register 0 (IRR0)

Address 00050h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IRS1R	IRS1T	IRS0R	IRS0T	IRTE	IRTC	IRTB	IRTJ
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IRTJ	Timer RJ2 interrupt request monitor flag	0: No interrupt requested 1: Interrupt requested	R
b1	IRTB	Timer RB2 interrupt request monitor flag		R
b2	IRTC	Timer RC interrupt request monitor flag		R
b3	IRTE	Timer RE2 interrupt request monitor flag		R
b4	IRS0T	UART0 transmit interrupt request monitor flag		R
b5	IRS0R	UART0 receive interrupt request monitor flag		R
b6	IRS1T	UART1 transmit interrupt request monitor flag		R
b7	IRS1R	UART1 receive interrupt request monitor flag		R

The IRR0 register is the monitor flag register for timer RJ2, timer RB2, timer RC, timer RE2, UART0 transmit, UART0 receive, UART1 transmit, and UART1 receive interrupt requests.
See **11.4.2.1 Registers IRR0 to IRR2** for the relation between interrupt monitor flag bits and peripheral function interrupts.

11.2.7 Interrupt Monitor Flag Register 1 (IRR1)

Address 00051h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IRTK	IRWD	IRFM	IRIS	IRAD	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is 0.	R
b1	—			
b2	IRAD	A/D conversion interrupt request monitor flag	0: No interrupt requested 1: Interrupt requested	R
b3	IRIS	SSU/I^{2}C bus interrupt request monitor flag		R
b4	IRFM	Flash ready interrupt request monitor flag		R
b5	IRWD	Periodic timer interrupt request monitor flag		R
b6	IRTK	Timer RK interrupt request monitor flag		R
b7	—	Nothing is assigned. The write value must be 0. The read value is 0.		—

The IRR1 register is the monitor flag register for A/D conversion, synchronous serial communication unit (SSU)/I^{2}C bus interface, flash ready, periodic timer, and timer RK interrupt requests.
See **11.4.2.1 Registers IRR0 to IRR2** for the relation between interrupt monitor flag bits and peripheral function interrupts.

11.2.8 Interrupt Monitor Flag Register 2 (IRR2)

Address 00052h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IRCMP3	IRCMP1	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The read value is 0.	R
b1	—			
b2	IRCMP1	Comparator B1 interrupt request monitor flag	0: No interrupt requested 1: Interrupt requested	R
b3	IRCMP3	Comparator B3 interrupt request monitor flag		R
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

The IRR2 register is the monitor flag register for comparator B1 and comparator B3 interrupt requests. See **11.4.2.1 Registers IRR0 to IRR2** for the relation between interrupt monitor flag bits and peripheral function interrupts.

11.2.9 External Interrupt Flag Register (IRR3)

Address 00053h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	IRKI	—	IRI3	IRI2	IRI1	IRI0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IRI0	$\overline{\text{INT0}}$ interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b1	IRI1	$\overline{\text{INT1}}$ interrupt request flag		R/W
b2	IRI2	$\overline{\text{INT2}}$ interrupt request flag		R/W
b3	IRI3	$\overline{\text{INT3}}$ interrupt request flag		R/W
b4	—	Reserved	Set to 0.	R/W
b5	IRKI	Key input interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

IRI0 Bit ($\overline{\text{INT0}}$ interrupt request flag)

Writing 0 after reading the value 1 sets the IRI0 bit to 0. This bit is also automatically set to 0 when the corresponding interrupt ($\overline{\text{INT0}}$) is acknowledged.

IRI1 Bit ($\overline{\text{INT1}}$ interrupt request flag)

Writing 0 after reading the value 1 sets the IRI1 bit to 0. This bit is also automatically set to 0 when the corresponding interrupt ($\overline{\text{INT1}}$) is acknowledged.

IRI2 Bit ($\overline{\text{INT2}}$ interrupt request flag)

Writing 0 after reading the value 1 sets the IRI2 bit to 0. This bit is also automatically set to 0 when the corresponding interrupt ($\overline{\text{INT2}}$) is acknowledged.

IRI3 Bit ($\overline{\text{INT3}}$ interrupt request flag)

Writing 0 after reading the value 1 sets the IRI3 bit to 0. This bit is also automatically set to 0 when the corresponding interrupt ($\overline{\text{INT3}}$) is acknowledged.

IRKI Bit (Key input interrupt request flag)

Writing 0 after reading the value 1 sets the IRKI bit to 0. This bit is also automatically set to 0 when the corresponding interrupt (key input) is acknowledged.

The interrupt priority level register must be rewritten only while no interrupt requests corresponding to that register are generated. See **11.9.7 Changing Interrupt Priority Levels and Flag Registers**.

11.2.10 Address Match Interrupt Register i (AIADRi) (i = 0 or 1)

Address 001C0h (AIADR0L), 001C4h (AIADR1L)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Address 001C1h (AIADR0M), 001C5h (AIADR1M)

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Address 001C2h (AIADR0H), 001C6h (AIADR1H)

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Function	Setting Range	R/W
b19 to b0	—	Setting for the addresses to be matched	00000h to FFFFFh	R/W
b20	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b21	—			
b22	—			
b23	—			

The AIADRi register (i = 0 or 1) is initialized after a voltage monitor 0 reset, power-on reset, or hardware reset. This register remains unchanged after a watchdog timer reset or software reset.

11.2.11 Address Match Interrupt Enable Register i (AIENi) (i = 0 or 1)

Address 001C3h (AIEN0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	AIEN00
After Reset	0	0	0	0	0	0	0	0

Address 001C7h (AIEN1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	AIEN10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	AIENi0	Address match interrupt enable i bit (i = 0 or 1)	0: Disabled 1: Enabled	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The AIENi register (i = 0 or 1) is initialized after a voltage monitor 0 reset, power-on reset, or hardware reset. This register remains unchanged after a watchdog timer reset or software reset.

11.3 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Set the start address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 11.2 shows an Interrupt Vector.

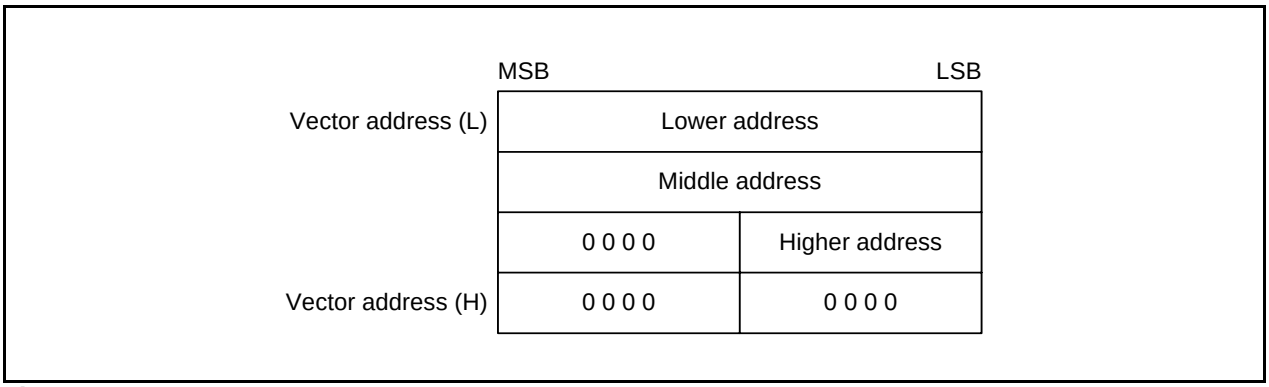


Figure 11.2 Interrupt Vector

11.3.1 Fixed Vector Table

The fixed vector table is allocated to addresses 0FFDCh to 0FFFFh.
Table 11.5 lists the Fixed Vector Table. The vector addresses (H) of the fixed vectors are used by the ID code check function. For details, see **23.3 ID Code Check Function**.

Table 11.5 Fixed Vector Table

Interrupt Source	Vector Address Address (L) to Address (H)	Remarks
Undefined instruction	0FFDCh to 0FFDFh	Interrupt by the UND instruction
Overflow	0FFE0h to 0FFE3h	Interrupt by the INTO instruction
BRK instruction	0FFE4h to 0FFE7h	If the content of address 0FFE6h is FFh, program execution starts from the address indicated by the vector in the relocatable vector table.
Address match	0FFE8h to 0FFEBh	
Single-step (1)	0FFECh to 0FFEFh	
Watchdog timer, oscillation stop detection, voltage monitor 1	0FFF0h to 0FFF3h	
Reserved	0FFF4h to 0FFF7h	
Reserved	0FFF8h to 0FFFBh	
Reset	0FFFCh to 0FFFFh	

Note:
1. Do not use this interrupt. It is provided exclusively for use in development tools.

11.3.2 Relocatable Vector Table

The relocatable vector table occupies 256 bytes beginning from the start address set in the INTB register. Table 11.6 lists the Relocatable Vector Table.

Table 11.6 Relocatable Vector Table

Interrupt Source	Vector Address (1) Address (L) to Address (H)	Software Interrupt Number	Priority Level Setting (ILVL0 to ILVLE)
BRK instruction (2)	+0 to +3 (+00000h to +00003h)	0	—
Flash ready	+4 to +7 (+00004h to +00007h)	1	ILVL05 to ILVL04
Timer RK	+8 to +11 (+00008h to +0000Bh)	2	ILVL11 to ILVL10
Reserved	+12 to +15 (+0000Ch to +0000Fh)	3	—
Comparator B1	+16 to +19 (+00010h to +00013h)	4	ILVL21 to ILVL20
Comparator B3	+20 to +23 (+00014h to +00017h)	5	ILVL25 to ILVL24
Reserved	+24 to +27 (+00018h to +0001Bh)	6	—
Timer RC	+28 to +31 (+0001Ch to +0001Fh)	7	ILVL35 to ILVL34
Reserved	+32 to +35 (+00020h to +00023h)	8	—
Reserved	+36 to +39 (+00024h to +00027h)	9	—
Timer RE2	+40 to +43 (+00028h to +0002Bh)	10	ILVL51 to ILVL50
Reserved	+44 to +47 (+0002Ch to +0002Fh)	11	—
Reserved	+48 to +51 (+00030h to +00033h)	12	—
Key input	+52 to +55 (+00034h to +00037h)	13	ILVL65 to ILVL64
A/D conversion	+56 to +59 (+00038h to +0003Bh)	14	ILVL71 to ILVL70
SSU/I^{2}C bus (3)	+60 to +63 (+0003Ch to +0003Fh)	15	ILVL75 to ILVL74
Reserved	+64 to +67 (+00040h to +00043h)	16	—
UART0 transmission	+68 to +71 (+00044h to +00047h)	17	ILVL85 to ILVL84
UART0 reception	+72 to +75 (+00048h to +0004Bh)	18	ILVL91 to ILVL90
UART1 transmission	+76 to +79 (+0004Ch to +0004Fh)	19	ILVL95 to ILVL94
UART1 reception	+80 to +83 (+00050h to +00053h)	20	ILVLA1 to ILVLA0
$\overline{\text{INT2}}$	+84 to +87 (+00054h to +00057h)	21	ILVLA5 to ILVLA4
Timer RJ2	+88 to +91 (+00058h to +0005Bh)	22	ILVLB1 to ILVLB0
Periodic timer	+92 to +95 (+0005Ch to +0005Fh)	23	ILVLB5 to ILVLB4
Timer RB2	+96 to +99 (+00060h to +00063h)	24	ILVLC1 to ILVLC0
$\overline{\text{INT1}}$	+100 to +103 (+00064h to +00067h)	25	ILVLC5 to ILVLC4
$\overline{\text{INT3}}$	+104 to +107 (+00068h to +0006Bh)	26	ILVLD1 to ILVLD0
Reserved	+108 to +111 (+0006Ch to +0006Fh)	27	—
Reserved	+112 to +115 (+00070h to +00073h)	28	—
$\overline{\text{INT0}}$	+116 to +119 (+00074h to +00077h)	29	ILVLE5 to ILVLE4
Reserved	+120 to +123 (+00078h to +0007Bh)	30	—
Reserved	+124 to +127 (+0007Ch to +0007Fh)	31	—
Software (2)	+128 to +131 (+00080h to +00083h) to +252 to +255 (+000FCh to +000FFh)	32 to 63	—

Notes:
1. These addresses are relative to those indicated by the INTB register.
2. These interrupts are not disabled by the I flag.
3. The interrupts for the synchronous serial communication unit (SSU)/I^{2}C bus interface can be selected by the IICCR register.

11.4 Interrupt Control

The following describes enabling and disabling maskable interrupts and setting the priority for acknowledgement. This description does not apply to non-maskable interrupts.

11.4.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

11.4.2 Registers IRR0 to IRR3

11.4.2.1 Registers IRR0 to IRR2

Registers IRR0 to IRR2 are the monitor flag registers for peripheral function interrupts. These registers can only be read and cannot be written. Table 11.7 lists the Relation between Registers IRR0 to IRR2 and Registers Associated with Peripheral Function Interrupts.

Peripheral functions have individual interrupt request flags and interrupt enable registers. When both of the interrupt request flag and interrupt enable bit for a peripheral function are set to 1, the monitor flag in the corresponding IRR0 to IRR2 registers is set to 1 (interrupt requested). When either or both of the interrupt request flag and interrupt enable bit for a peripheral function are set to 1, the monitor flag in the corresponding IRR0 to IRR2 registers is set to 0 (no interrupt requested).

Table 11.7 Relation between Registers IRR0 to IRR2 and Registers Associated with Peripheral Function Interrupts

	Peripheral Function Interrupt Request Flag		Peripheral Function Interrupt Enable		Corresponding Interrupt Monitor Flag	
	Register	Bit	Register	Bit	Register	Bit
Timer RJ2	TRJIR	TRJIF	TRJIR	TRJIE	IRR0	IRTJ
Timer RB2	TRBIR	TRBIF	TRBIR	TRBIE	IRR0	IRTB
Timer RC (1)	TRCSR	IMFA	TRCIER	IMIEA	IRR0	IRTC
		IMFB		IMIEB		
		IMFC		IMIEC		
		IMFD		IMIED		
		OVF		OVIE		
Timer RE	TREIFR	RTCF/AUF	TREIER	YR1E/MOIE/ DYIE/HRIE/ 1SIE/0.5SIE/ 0.25SIE	IRR0	IRTE
		CMF/OVF		OVIE/CMIE		
Serial interface (UART0)	U0IR	U0TIF	U0IR	U0TIE	IRR0	IRS0T
		U0RIF		U0RIE		IRS0R
Serial interface (UART1)	U1IR	U1TIF	U1IR	U1TIE	IRR0	IRS1T
		U1RIF		U1RIE		IRS1R
A/D converter	ADICSR	ADF	ADICSR	ADIE	IRR1	IRAD
I^2C	SISR	TDRE	SIER	TIE	IRR1	IRIS
		TEND		TEIE		
		RDRF		RIE		
		ORER_AL/ NACKF		TE_NAKIE		
		STOP		RE_STIE		
SSU		TDRE		TIE		
		TEND		TEIE		
		RDRF		RIE		
		ORER_AL		RIE		
		CE_ADZ		CEIE_ACKBT		
Flash memory (1)	FST	RDYSTI	FMR0	RDYSTIE	IRR1	IRFM
		BSYAEI		BSYAEIE		
				CMDERIE		
Periodic timer	WDTIR	WDTIF	WDTIR	WDTIE	IRR1	IRWD
Timer RK	TMKIR	TMKCMIF	TMKIR	TMKCMIE	IRR1	IRTK
		TMKOVIF		TMKOVIE		
Comparator B	WCB1INTR	WCB1F	WCB1INTR	WCB1INTEN	IRR2	IRCMP1
	WCB3INTR	WCB3F	WCB3INTR	WCB3INTEN		IRCMP3

Note:
1. Timer RC and the flash memory each have multiple interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request sources and is reflected in the monitor flag (the IRTC bit in the IRR0 register or the IRFM bit in the IRR1 register).

11.4.2.2 IRR3 Register

The IRR3 register is the flag register for external interrupts ($\overline{INT0}$ to $\overline{INT3}$ and $\overline{KI0}$ to $\overline{KI3}$). When external input is enabled and an active edge is detected, the interrupt request flag in the IRR3 register is set to 1. When an interrupt request is acknowledged, the flag for this interrupt request is automatically set to 0 after the CPU branches to the corresponding interrupt vector. Writing 0 after reading the value 1 also sets the interrupt request flag to 0.

11.4.3 Interrupt Priority Levels in ILVLi Register (i = 0 to E) and IPL

Interrupt priority levels can be set by the ILVLi register (i = 0 to E).
Table 11.8 lists the Interrupt Priority Level Settings. Table 11.9 lists the Interrupt Priority Levels Enabled by IPL.
The following are the conditions when an interrupt is acknowledged:

- I flag = 1
- The interrupt request flag and interrupt enable bit for each peripheral function = 1 or external interrupt request flag (IRR3) = 1
- Interrupt priority level > IPL

The I flag, registers IRR0 to IRR3, the ILVLi register (i = 0 to E), and IPL are independent of each other. They do not affect one another.

Table 11.8 Interrupt Priority Level Settings

Bits ILVLi1 to ILVLi0 or Bits ILVLi5 to ILVLi4 (1)	Interrupt Priority Level	Priority Level
00b	Level 0 (interrupt disabled)	—
01b	Level 1	Low ↓ High
10b	Level 2	
11b	Level 2	

Note:
1. Values to be set in interrupt priority level register i (ILVLi) (i = 0 to E).

Table 11.9 Interrupt Priority Levels Enabled by IPL

IPL	Interrupt Priority Level to be Enabled
000b	Levels 1 and 2
001b	Level 2
010b to 111b	None (all maskable interrupts are disabled)

11.4.4 Interrupt Sequence

The following describes the interrupt sequence performed from when an interrupt request is acknowledged until the interrupt routine is executed.
When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction has completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, and RMPA instructions, if an interrupt request is generated while the instruction is being executed, the MCU suspends the instruction to start the interrupt sequence.
The interrupt sequence is performed as described below.
Figure 11.3 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. Then, for an $\overline{\text{INT}}$ interrupt and a key input interrupt, the corresponding interrupt request flag is set to 0 (no interrupt requested). For any other peripheral interrupts, the corresponding interrupt request flag remains 1 (interrupt requested) and does not change.
(2) The FLG register is saved to a temporary register (1) in the CPU immediately before the interrupt sequence is entered.
(3) Flags I, D, and U in the FLG register are set as follows:
• The I flag is 0 (interrupt disabled).
• The D flag is 0 (single-step interrupt disabled).
• The U flag is set to 0 (ISP selected).
However, the U flag does not change if an INT instruction for software interrupt number 32 to 63 is executed.
(4) The CPU internal temporary register (1) is saved on the stack.
(5) The PC is saved on the stack.
(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
(7) The start address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the start address of the interrupt routine.

Note:
1. Temporary registers cannot be used by the user.

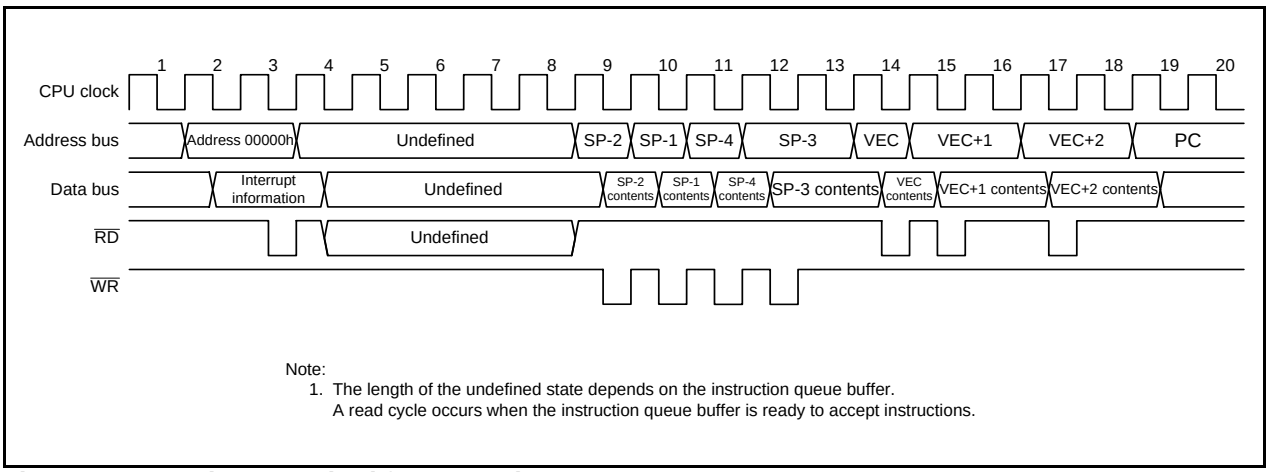
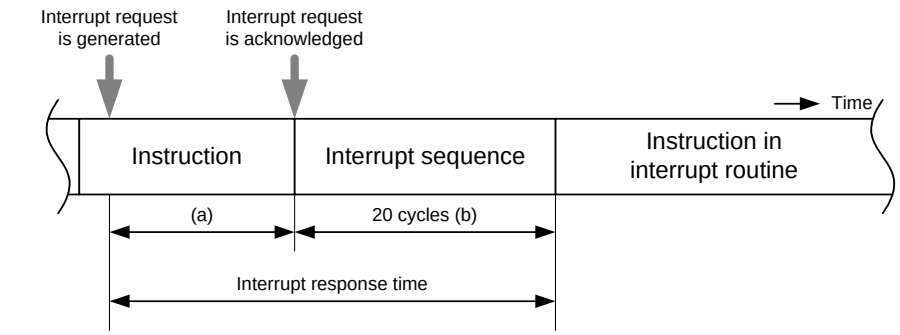


Figure 11.3 Time Required for Executing Interrupt Sequence

11.4.5 Interrupt Response Time

Figure 11.4 shows the Interrupt Response Time. The interrupt response time is the period from when an interrupt request is generated until the first instruction in the interrupt routine is executed. This time consists of two periods: the first period ranges from when an interrupt request is generated until the currently executing instruction is completed ((a) in Figure 11.4) and the second from when an interrupt request is acknowledged until the interrupt sequence is executed (20 cycles (b)).



(a) The period from when an interrupt request is generated until the currently executing instruction is completed. The length of this time varies with the instruction being executed. The DIVX instruction requires the longest time, 30 cycles (no wait states, and the divisor is a register).
(b) 21 cycles for address match and single-step interrupts.

Figure 11.4 Interrupt Response Time

11.4.6 IPL Change When Interrupt Request is Acknowledged

When a maskable interrupt request is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.

For a software interrupt or special interrupt request, the level listed in Table 11.10 is set in the IPL.

Table 11.10 IPL Value When Software Interrupt or Special Interrupt is Acknowledged

Interrupt Source without Interrupt Priority Level	Value Set in IPL
Watchdog timer, oscillation stop detection, voltage monitor 1	7
Software, address match, single-step	Not changed

11.4.7 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.
After a total of 16 bits: higher 4 bits in the PC, higher 4 (IPL) and lower 8 bits in the FLG register, are saved on the stack, the lower 16 bits in the PC are saved.
Figure 11.5 shows the Stack State Before and After Interrupt Request is Acknowledged.
Any other necessary registers should be saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being used (1) with a single instruction.

Note:
1. Selectable from among registers R0, R1, R2, R3, A0, A1, SB, and FB.

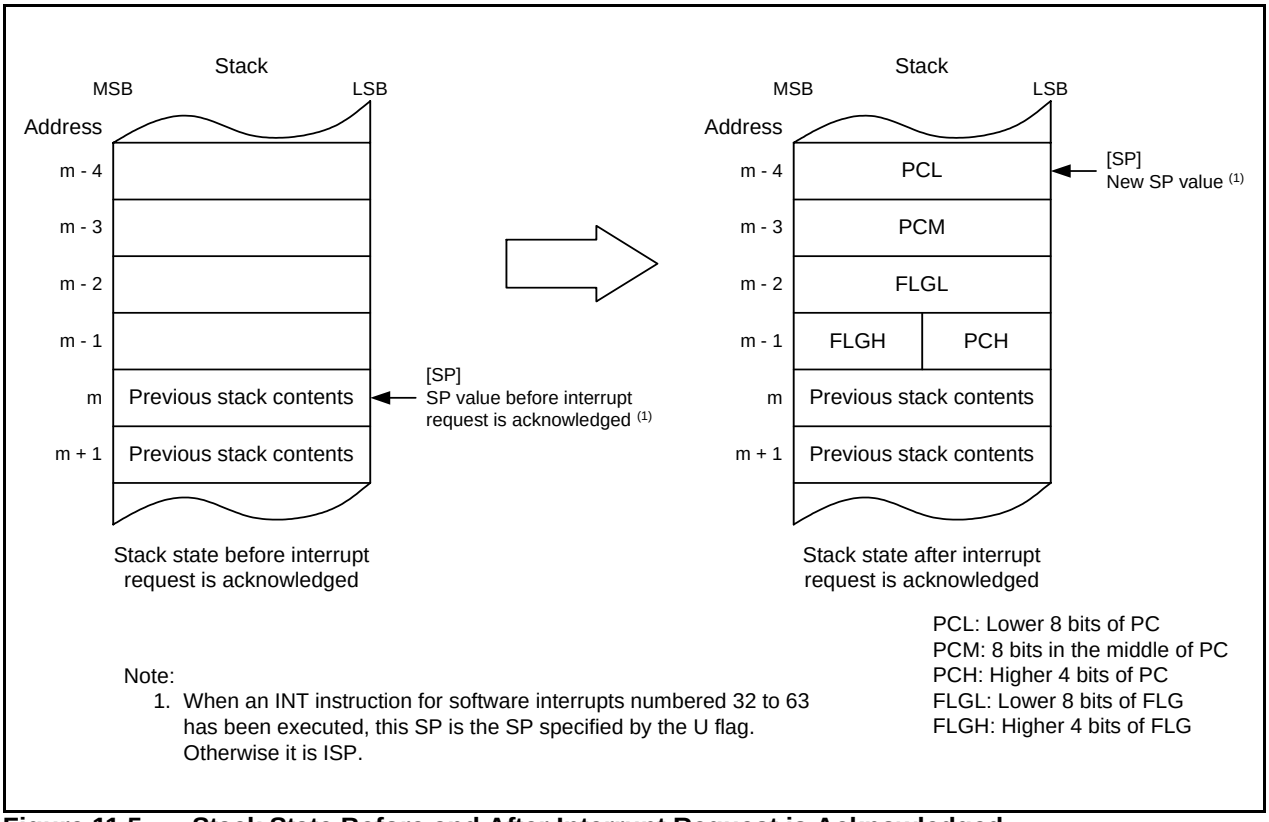
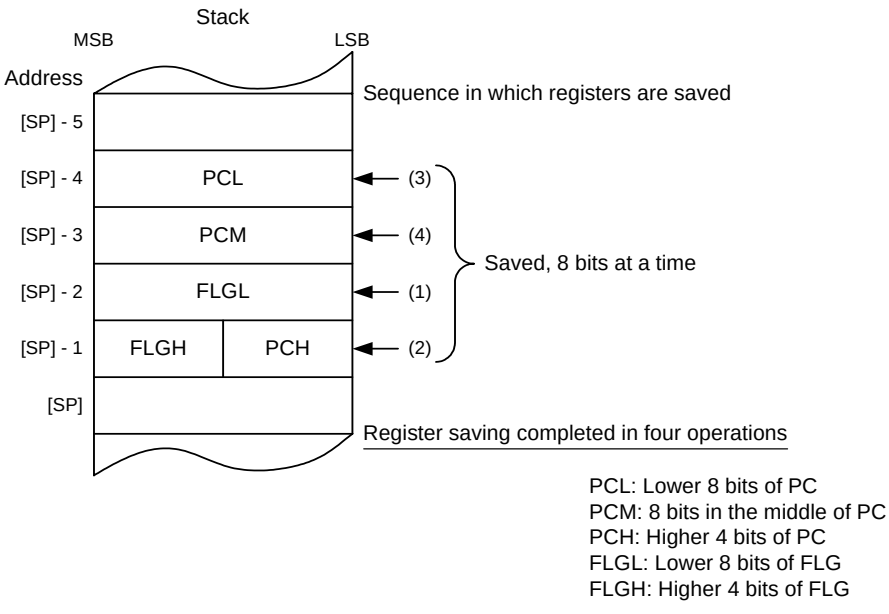


Figure 11.5 Stack State Before and After Interrupt Request is Acknowledged

The register saving operation in the interrupt sequence uses four operations, each one of which saves 8 bits. Figure 11.6 shows the Register Saving Operation.



Note:
1. [SP] indicates the SP initial value when an interrupt request is acknowledged. After registers are saved, the SP content becomes [SP] minus 4. When an INT instruction for software interrupts numbered 32 to 63 has been executed, this SP is the SP specified by the U flag. Otherwise it is ISP.

Figure 11.6 Register Saving Operation

11.4.8 Returning from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved on the stack, are restored. The program that was running before the interrupt request was acknowledged starts running again.

The registers saved by a program in the interrupt routine should be restored using the POPM or similar instruction before executing the REIT instruction.

11.4.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.

Any maskable interrupt (peripheral function) priority level can be selected by bits ILVLi0 to ILVLi1 or bits ILVLi4 to ILVLi5. However, if two or more maskable interrupts have the same priority level, the interrupt with higher priority given by hardware is acknowledged.

The priority of special interrupts such as the watchdog timer interrupt is set by hardware.

Figure 11.7 shows the Hardware Interrupt Priority.

Software interrupts are not affected by the interrupt priority. If a software interrupt instruction is executed, the MCU will execute the corresponding interrupt routine.

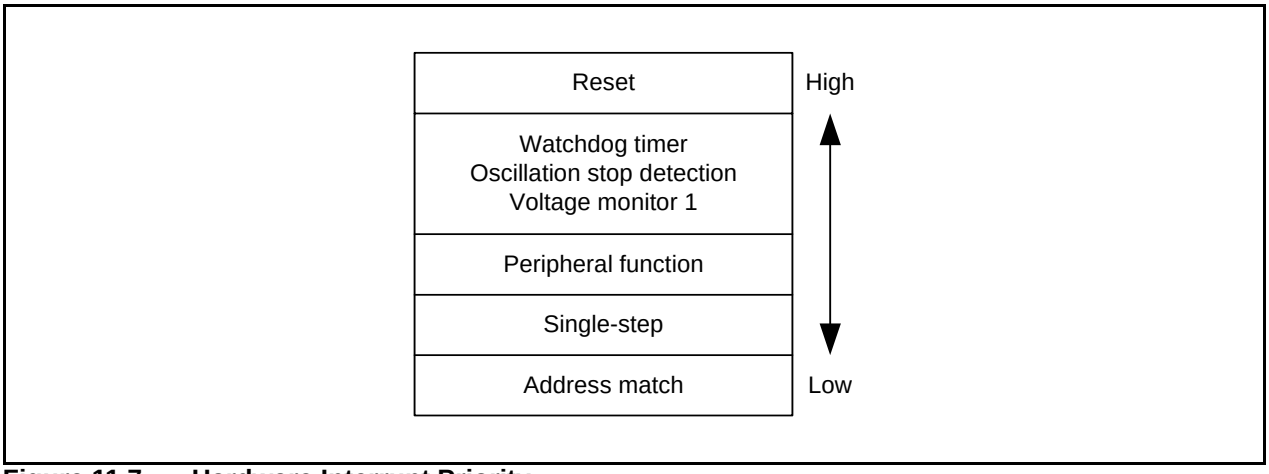


Figure 11.7 Hardware Interrupt Priority

11.4.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt.
Figure 11.8 shows the Interrupt Priority Level Selection Circuit.

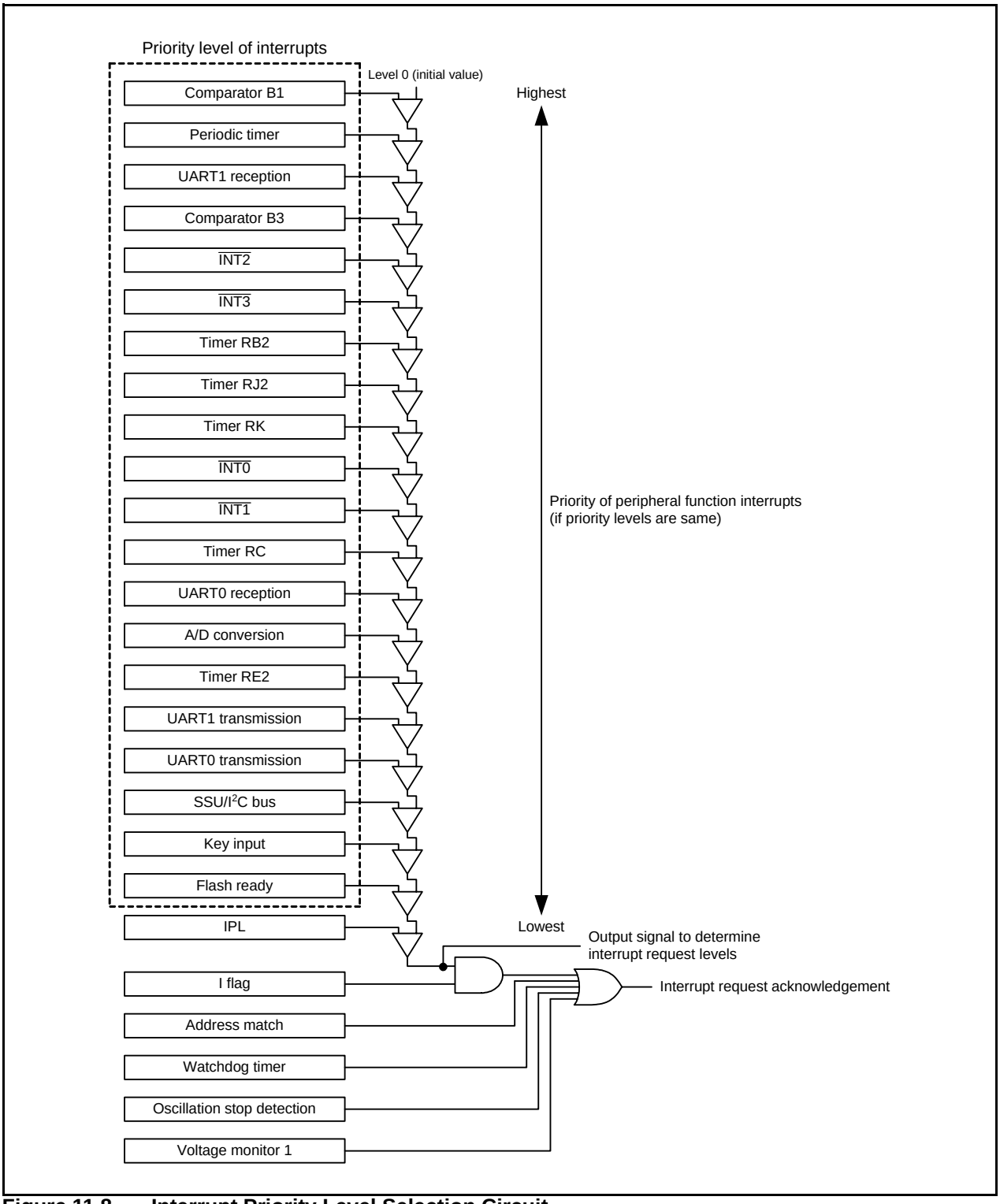


Figure 11.8 Interrupt Priority Level Selection Circuit

11.5 $\overline{\text{INT}}$ Interrupt

11.5.1 $\overline{\text{INTi}}$ Interrupt (i = 0 to 3)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN register is to 1 (enabled). The edge polarity can be selected by bits INTiSA to INTiSB in the ISCR0 register. The input pins used as the $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ input can be selected.
Inputs can be passed through a digital filter with three different sampling clocks.
The interrupt by the $\overline{\text{INTi}}$ input can be used as a wakeup function to cancel wait mode or stop mode.
Table 11.11 lists the Pin Configuration for $\overline{\text{INTi}}$ Interrupt.

Table 11.11 Pin Configuration for $\overline{\text{INTi}}$ Interrupt

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P1_4, P4_5	I	$\overline{\text{INT0}}$ interrupt input
$\overline{\text{INT1}}$	P1_5, P1_7, P2_0	I	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT2}}$	P3_4, P4_7	I	$\overline{\text{INT2}}$ interrupt input
$\overline{\text{INT3}}$	P3_3	I	$\overline{\text{INT3}}$ interrupt input

11.5.2 $\overline{\text{INTi}}$ Input Filter (i = 0 to 3)

The $\overline{\text{INTi}}$ input has a digital filter. The sampling clock can be selected by bits INTiF0 to INTiF1 in the INTF0 register. The $\overline{\text{INTi}}$ level is sampled every sampling clock cycle, and the corresponding IRIi bit in the IRR3 register is set to 1 (interrupt requested) when the sampled input level matches three successive times.
Figure 11.9 shows the $\overline{\text{INTi}}$ Input Filter Configuration. Figure 11.10 shows an Example of $\overline{\text{INTi}}$ Input Filter Operation.

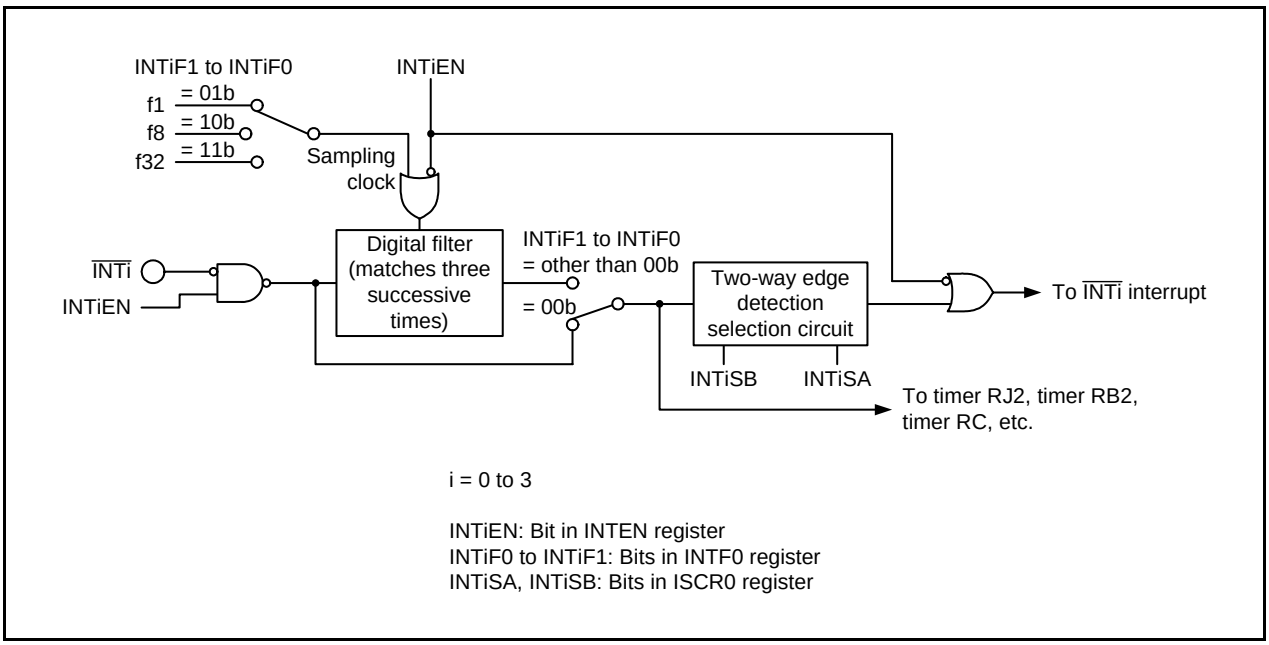


Figure 11.9 $\overline{\text{INTi}}$ Input Filter Configuration

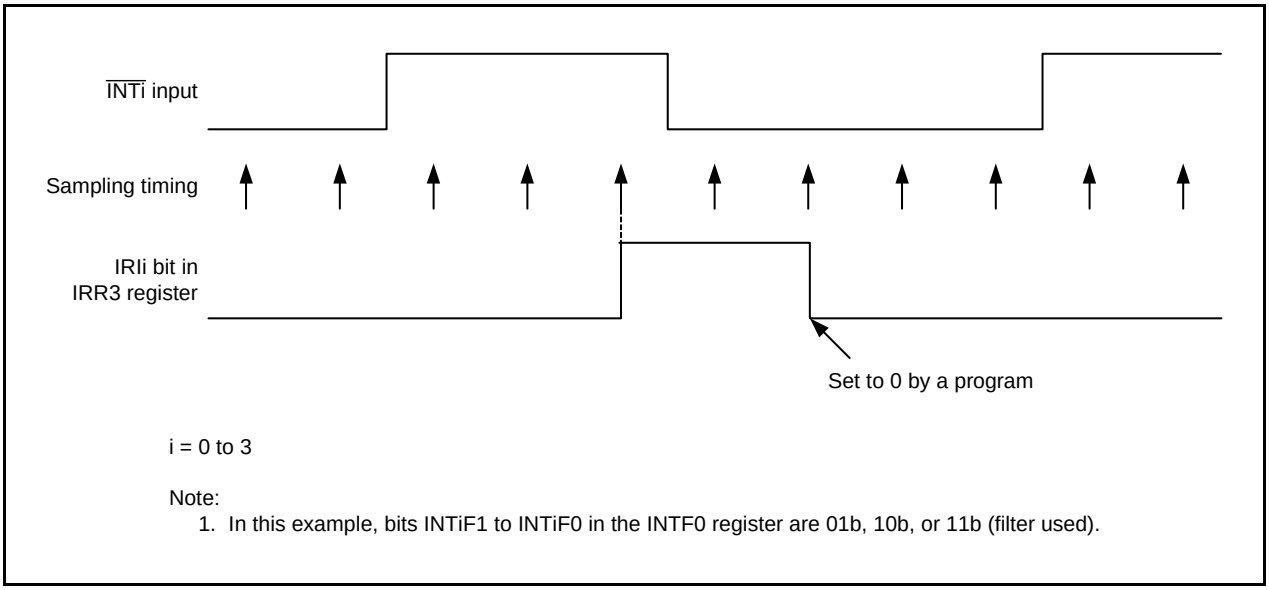


Figure 11.10 Example of $\overline{\text{INTi}}$ Input Filter Operation

11.6 Key Input Interrupt

A key input interrupt request is generated by one of the input edges on pins $\overline{KI0}$ to $\overline{KI3}$. The key input interrupt can be used as a key-on wakeup function to cancel wait mode or stop mode.

The KIiEN bit (i = 0 to 3) in the KIEN register is be used to select whether the pins are used as the $\overline{KIi}$ input. The KIiPL bit in the KIEN register is be used to select the input polarity.

When a low level is input to the $\overline{KIi}$ pin, which sets the KIiPL bit to 0 (falling edge), inputs to the other pins $\overline{KI0}$ to $\overline{KI3}$ are not detected as interrupts. Likewise, when a high level is input to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), inputs to the other pins $\overline{KI0}$ to $\overline{KI3}$ are not detected as interrupts.

Figure 11.11 shows the Block Diagram for Key Input Interrupts. Table 11.12 lists the Pin Configuration for Key Input Interrupts.

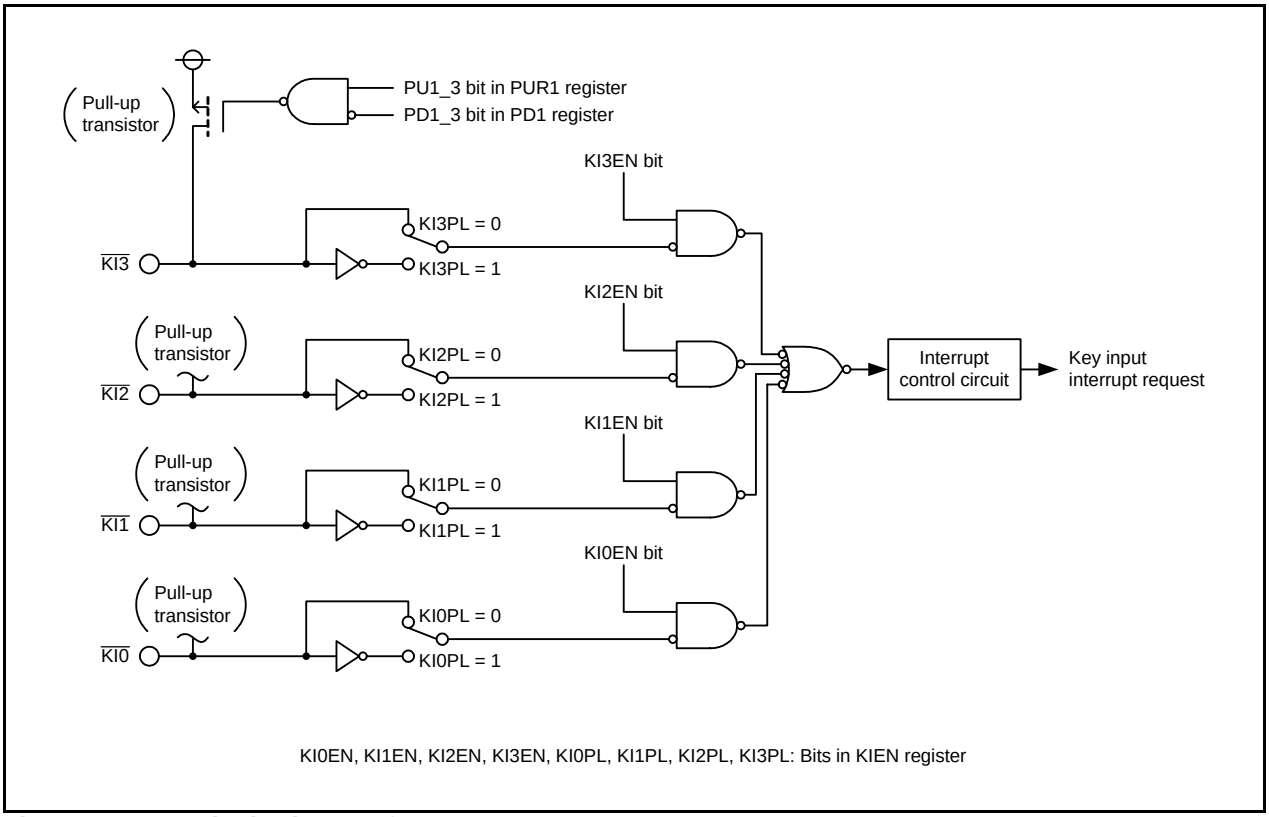


Figure 11.11 Block Diagram for Key Input Interrupts

Table 11.12 Pin Configuration for Key Input Interrupts

Pin Name	I/O	Function
$\overline{KI0}$	I	$\overline{KI0}$ interrupt input
$\overline{KI1}$	I	$\overline{KI1}$ interrupt input
$\overline{KI2}$	I	$\overline{KI2}$ interrupt input
$\overline{KI3}$	I	$\overline{KI3}$ interrupt input

11.7 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the AIADRi register (i = 0 or 1). This interrupt is used as a break function for the debugger. When the on-chip debugger is used, do not set an address match interrupt (registers AIENi and AIADRi, and fixed vector table) in the user system.

Set the start address of any instruction in these registers. The AIENi0 bit (i = 0 or 1) in the AIENi register can be used to enable or disable the interrupt. The address match interrupt is not affected by the I flag and IPL.

The PC value (see **11.4.7 Saving Registers**), which is saved on the stack when an address match interrupt request is acknowledged, will differ depending on the instruction at the address indicated by the AIADRi register. The appropriate return address is not saved on the stack. When the MCU returns from the address match interrupt, use one of the following methods:

- Rewrite the contents of the stack and use the REIT instruction to return.
- Use an instruction such as POP to restore the stack to its previous state where the interrupt request was acknowledged. Then use a jump instruction to return.

Table 11.13 lists the PC Value Saved When Address Match Interrupt Request is Acknowledged. Table 11.14 lists the Correspondence between Address Match Interrupt Sources and Associated Registers.

Table 11.13 PC Value Saved When Address Match Interrupt Request is Acknowledged

Instruction at Address Indicated by AIADRi Register (i = 0 or 1)	PC Value Saved (1)
• Instruction with 16-bit operation code • Instruction shown below among the instructions with 8-bit operation code: ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ.B:S #IMM8,dest STNZ.B:S #IMM8,dest STZX.B:S #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (however, dest = A0 or A1)	Address indicated by AIADRi register + 2
Instructions other than the above	Address indicated by AIADRi register + 1

Note:
1. PC value saved: See **11.4.7 Saving Registers**.

Table 11.14 Correspondence between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIEN00	AIADR0
Address match interrupt 1	AIEN10	AIADR1

11.8 How to Determine Interrupt Sources

Table 11.15 lists How to Determine Interrupt Source for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, or Voltage Monitor 1 Interrupt. Figure 11.12 shows How to Determine Interrupt Source for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, or Voltage Monitor 1 Interrupt.

Table 11.15 How to Determine Interrupt Source for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, or Voltage Monitor 1 Interrupt

Generated Interrupt Source	Bit Indicating Interrupt Source
Oscillation stop detection	CKSWIF bit in BAKCR register = 1
Watchdog timer	UFIF bit in RISR register = 1
Voltage monitor 1	VW1C2 bit in VW1C register = 1

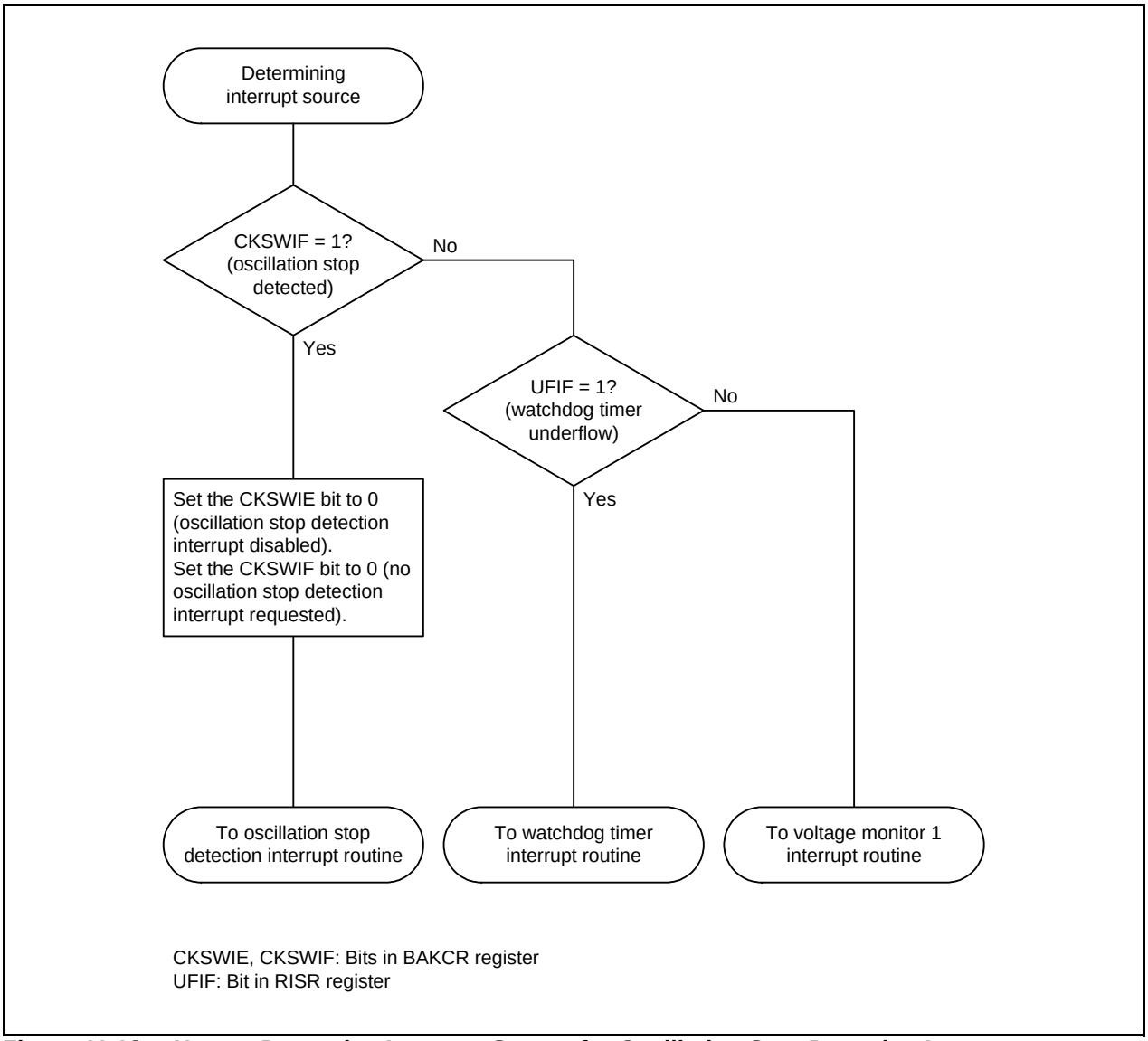


Figure 11.12 How to Determine Interrupt Source for Oscillation Stop Detection Interrupt, Watchdog Timer Interrupt, or Voltage Monitor 1 Interrupt

11.9 Notes on Interrupts

11.9.1 Reading Address 00000h

Do not read address 00000h by a program. When an external interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from address 00000h in the interrupt sequence. At this time, the corresponding bit in the IRR3 register for the acknowledged interrupt is set to 0.
If a program is used to read address 00000h, the corresponding bit in the IRR3 register for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

11.9.2 SP Setting

Set a value in the SP before any interrupt is acknowledged. The SP is 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

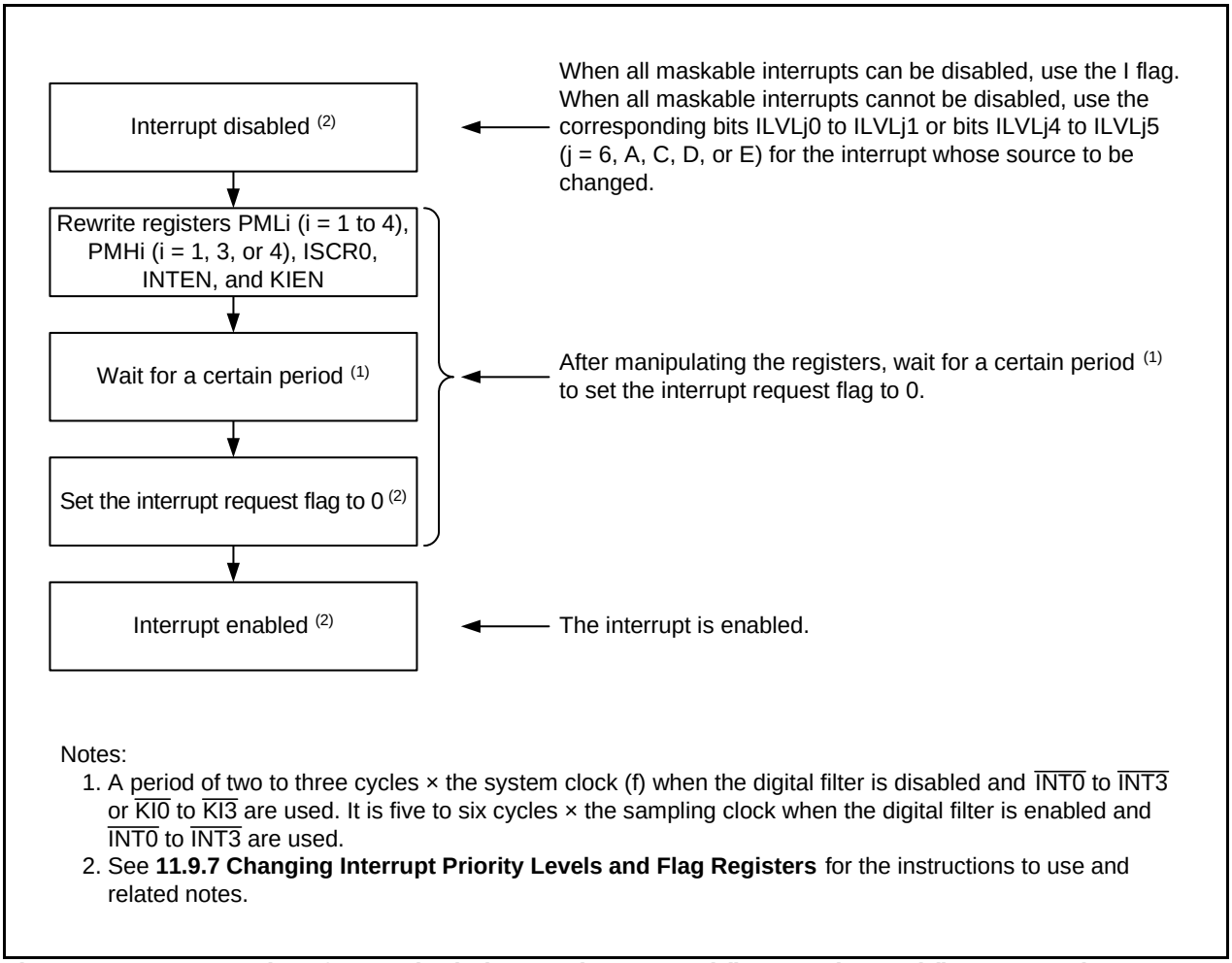
11.9.3 External Interrupt and Key Input Interrupt

Signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ must meet either the low-level width or the high-level width requirements shown in External Interrupt $\overline{\text{INTi}}$ Input (i = 0 to 3) in the Electrical Characteristics, regardless of the CPU operating clock. For details, see **Table 24.20** (Vcc = 5 V), **Table 24.26** (Vcc = 3 V), and **Table 24.32** (Vcc = 2.2 V) **External Interrupt $\overline{\text{INTi}}$ Input, Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 3)**.

11.9.4 Rewriting Registers PMLi (i = 1 to 4), PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN

When changing the functions of the $\overline{INT0}$ to $\overline{INT3}$ and $\overline{KI0}$ to $\overline{KI3}$ interrupts, an interrupt request flag may be set to 1 by rewriting registers PMLi (i = 1 to 4), PMHi (i = 1, 3, or 4), ISCR0, and KIEN. When an interrupt function is switched, rewrite these registers with interrupt requests disabled, and wait for a certain period (1) before setting the interrupt request flag to 0.
Figure 11.13 shows the Procedure for Manipulating Registers PMLi (i = 1 to 4), PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN, and Setting Interrupt Request Flag to 0.

Note:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{INT0}$ to $\overline{INT3}$ or $\overline{KI0}$ to $\overline{KI3}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{INT0}$ to $\overline{INT3}$ are used.



Notes:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{INT0}$ to $\overline{INT3}$ or $\overline{KI0}$ to $\overline{KI3}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{INT0}$ to $\overline{INT3}$ are used.
2. See **11.9.7 Changing Interrupt Priority Levels and Flag Registers** for the instructions to use and related notes.

Figure 11.13 Procedure for Manipulating Registers PMLi (i = 1 to 4), PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN, and Setting Interrupt Request Flag to 0

11.9.5 $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) When Returning from Wait Mode or Stop Mode to Standard Operating Mode

When a transition is made to wait mode or stop mode with the WCKSTP bit in the CKSTPR register set to 1 (system clock stopped in wait mode) while in use of the $\overline{\text{INTi}}$ filter, the $\overline{\text{INTi}}$ interrupt cannot be used to return to standard mode.

When the $\overline{\text{INTi}}$ interrupt is used to return, set the WCKSTP bit to 1 and bits INTiF1 to INTiF0 in the INTF0 register to 00b (no filter) before a transition is made to wait mode or stop mode. When the filter is used again, select the sampling clock with bits INTiF0 to INTiF1 to enable the INTiEN bit in the INTEN register.

Figure 11.14 shows the Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) is Used.

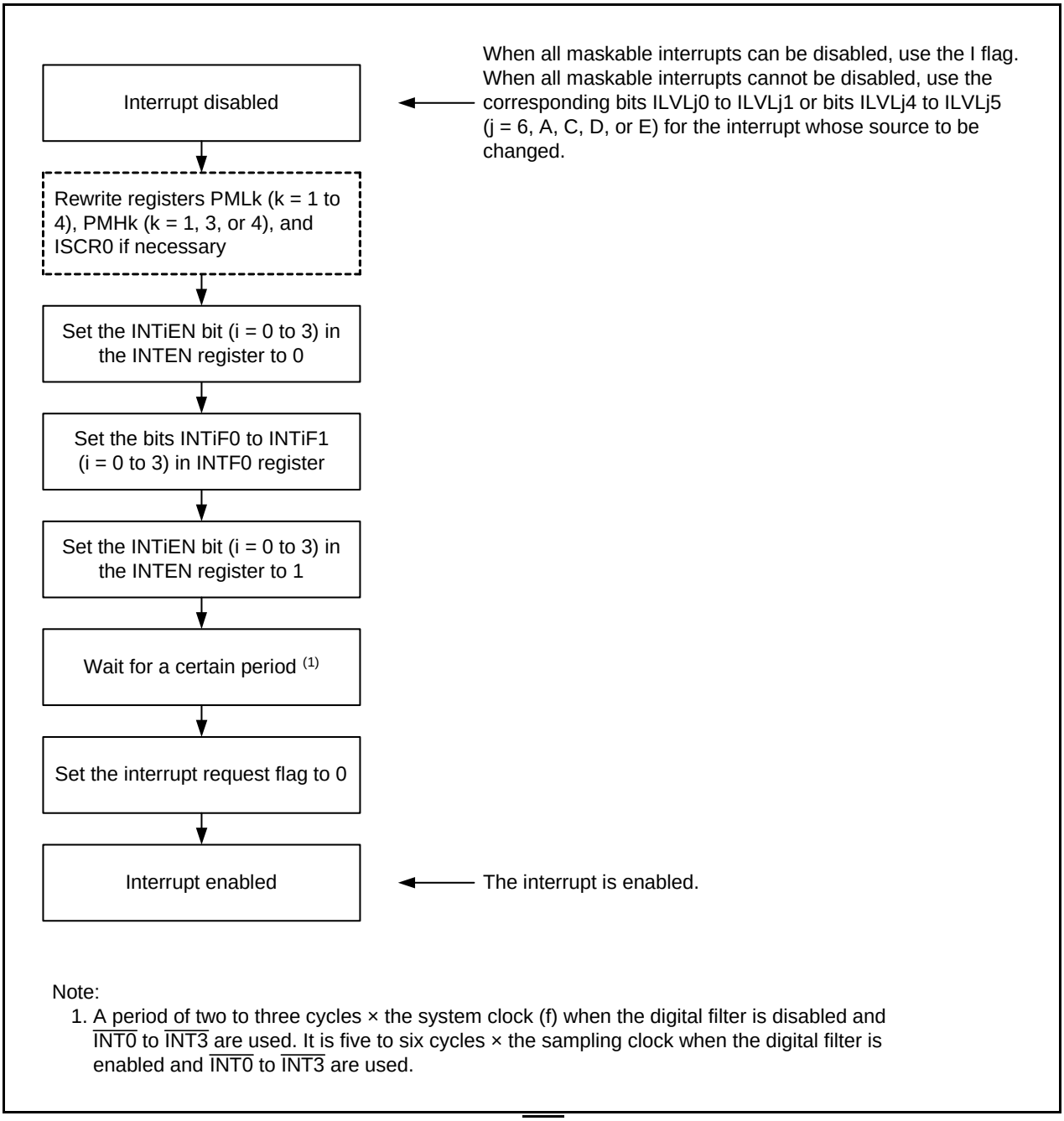
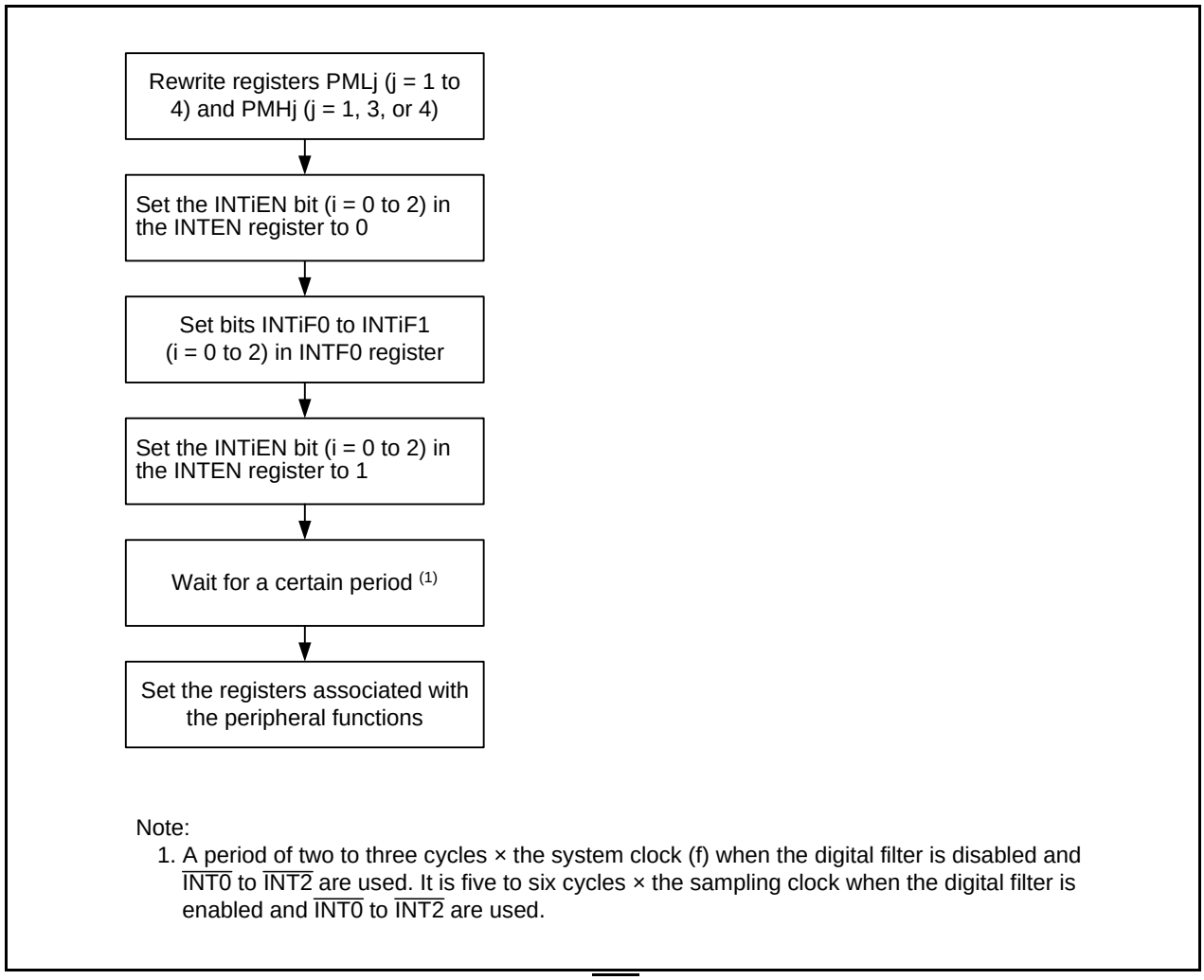


Figure 11.14 Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) is Used

11.9.6 Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions

Figure 11.15 shows the Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions (Timer RJ2, Timer RB2, and Timer RC).



Note:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ are used.

Figure 11.15 Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions (Timer RJ2, Timer RB2, and Timer RC)

11.9.7 Changing Interrupt Priority Levels and Flag Registers

(a) The interrupt priority level and the flag register must be changed only while no interrupt requests are generated. If an interrupt may be generated, using the I flag to disable the interrupt before changing the interrupt priority level and the flag register.

(b) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below.

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupts enabled) before the interrupt priority level and the flag register are changed due to effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause the program until the interrupt priority level register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #CFH, ILVLE     ; Set INT0 interrupt priority level 0
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #CFH, ILVLE     ; Set INT0 interrupt priority level 0
    MOV.W   MEM, R0         ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #CFH, ILVLE     ; Set INT0 interrupt priority level 0
    POPC     FLG            ; Enable interrupts
```

12. I/O Ports

There are 29 I/O ports. P3_1 and P4_5 can be used as I/O ports when the XIN clock oscillation circuit is not used, and P4_6 and P4_7 can be used as I/O ports when the XCIN clock oscillation circuit is not used. PA_0 can be used as an I/O port when a hardware reset is not used. In addition, all the ports are multiplexed with multiple peripheral functions.

12.1 Overview

The functions of the ports are selected by the peripheral function mapping registers (PMLi (i = 0 to 4), PMHi (i = 0, 1, 3, or 4) and the peripheral function mapping expansion register (PMH1E). The functions of the I/O ports are selected by the port direction registers (PDi (i = 0 to 4, A)). In addition, the drive capacity of some ports can be switched. Table 12.1 shows the I/O Port Overview. Table 12.2 lists the Port Functions by Pin. Table 12.3 lists the I/O Port Register Configuration.

Table 12.1 I/O Port Overview

Ports	I/O	Output Type	I/O Setting	Internal Pull-Up Resistor	Drive Capacity Switching
P0_0 to P0_7	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (4)	None
P1_0, P1_1, P1_6, P1_7	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (4)	None
P1_2 to P1_5					Set in 1-bit units. (5)
P2_0 to P2_2	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (4)	None
P3_1 (1)	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (4)	None
P3_3, P3_4, P3_5, P3_7					Set in 1-bit units. (5)
PA_0 (2)	I/O	3-state CMOS	Set in 1-bit units.	None	None
P4_2, P4_5 (1), P4_6 (3), P4_7 (3)	I/O	3-state CMOS	Set in 1-bit units.	Set in 1-bit units. (4)	None

Notes:
1. When the XIN clock oscillation circuit or direct input of the XIN clock is not used, these can be used as I/O ports.
2. When the hardware reset is not used, this port can be used as an I/O port.
3. When the XCIN clock oscillation circuit or direct input of the XCIN clock is not used, these can be used as I/O ports.
4. In input mode, whether an internal pull-up resistor is connected or not can be selected by the PURi register (i = 0 to 4).
5. The drive capacity of the output transistors (low or high) can be selected by the DRRi register (i = 1 or 3).

Table 12.2 Port Functions by Pin

Pin Number	R8C/M13B Group	Function 0	Function 1	Function 2	Function 3	Function 4	Function Select Bit		
		PM2 to PM0 = 000b	PM2 to PM0 = 001b	PM2 to PM0 = 010b	PM2 to PM0 = 011b	PM2 to PM0 = 100b	PM2	PM1	PM0
1	P4_2	P4_2	TRBO	TXD0/IrTXD	$\overline{KI3}$	—	—	P42SEL1	P42SEL0
2	P3_7	P3_7	$\overline{ADTRG}$	TRJO	TRCIOD	—	—	P37SEL1	P37SEL0
3	$\overline{RESET}$	PA_0	—	—	—	—	—	—	—
4	P4_7/XCOUT	P4_7/XCOUT	$\overline{INT2}$	—	—	—	—	P47SEL1	P47SEL0
5	VSS/AVSS	—	—	—	—	—	—	—	—
6	P4_6/XCIN	P4_6/XCIN	RXD0/IrRXD	TXD0/IrTXD	—	—	—	P46SEL1	P46SEL0
7	VCC/AVCC	—	—	—	—	—	—	—	—
8	MODE	—	—	—	—	—	—	—	—
9	P3_5	P3_5	TRCIOD	$\overline{KI2}$	VCOUT3	—	—	P35SEL1	P35SEL0
10	P3_4	P3_4/IVREF3	TRCIOC	$\overline{INT2}$	SSI	—	—	P34SEL1	P34SEL0
11	P3_3	P3_3/IVCMP3	TRCCLK	$\overline{INT3}$	$\overline{SCS}$	—	—	P33SEL1	P33SEL0
12	P2_2	P2_2	TRCIOD	TRKI	SSO/SDA	—	—	P22SEL1	P22SEL0
13	P2_1	P2_1	TRCIOC	TRKO	SSCK/SCL	—	—	P21SEL1	P21SEL0
14	P2_0	P2_0	TRCIOB	TRKO	$\overline{INT1}$	—	—	P20SEL1	P20SEL0
15	P3_1/XIN	P3_1/XIN	TRBO	—	—	—	—	P31SEL1	P31SEL0
16	P4_5/XOUT	P4_5/XOUT	$\overline{INT0}$	$\overline{ADTRG}$	—	—	—	P45SEL1	P45SEL0
17	P1_7	P1_7/AN7/IVCMP1	$\overline{INT1}$	TRJIO	TRCCLK	—	—	P17SEL1	P17SEL0
18	P1_6	P1_6/AN6/IVREF1	CLK0	TRJO	TRCIOB	—	—	P16SEL1	P16SEL0
19	P1_5	P1_5/AN5	RXD0/IrRXD	TRJIO	$\overline{INT1}$	VCOUT1	P15SEL2	P15SEL1	P15SEL0
20	P1_4	P1_4/AN4	TXD0/IrTXD	RXD0/IrRXD	$\overline{INT0}$	TRCIOB	P14SEL2	P14SEL1	P14SEL0
21	P1_3	P1_3/AN3	TRCIOC	$\overline{KI3}$	TRBO	—	—	P13SEL1	P13SEL0
22	P1_2	P1_2/AN2	TRCIOB	$\overline{KI2}$	TREO	—	—	P12SEL1	P12SEL0
23	P1_1	P1_1/AN1	TRCIOA/TRCTRG	$\overline{KI1}$	—	—	—	P11SEL1	P11SEL0
24	P1_0	P1_0/AN0	TRCIOD	$\overline{KI0}$	TRKI	—	—	P10SEL1	P10SEL0
25	P0_7	P0_7	TRCIOC	TRKO	—	—	—	P07SEL1	P07SEL0
26	P0_6	P0_6	TRCIOD	—	—	—	—	P06SEL1	P06SEL0
27	P0_5	P0_5	TRCIOB	—	—	—	—	P05SEL1	P05SEL0
28	P0_4	P0_4	TRCIOB	TREO	—	—	—	P04SEL1	P04SEL0
29	P0_3	P0_3	TRCIOB	CLK1	—	—	—	P03SEL1	P03SEL0
30	P0_2	P0_2	TRCIOA/TRCTRG	RXD1/IrRXD	—	—	—	P02SEL1	P02SEL0
31	P0_1	P0_1	TRCIOA/TRCTRG	TXD1/IrTXD	—	—	—	P01SEL1	P01SEL0
32	P0_0	P0_0	TRCIOA/TRCTRG	—	—	—	—	P00SEL1	P00SEL0

Table 12.3 I/O Port Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Port P0 Direction Register	PD0	00h	000A8h	8
Port P1 Direction Register	PD1	00h	000A9h	8
Port P2 Direction Register	PD2	00h	000AAh	8
Port P3 Direction Register	PD3	00h	000ABh	8
Port P4 Direction Register	PD4	00h	000ACh	8
Port PA Direction Register	PDA	00h	000ADh	8
Port P0 Register	P0	00h	000AEh	8
Port P1 Register	P1	00h	000AFh	8
Port P2 Register	P2	00h	000B0h	8
Port P3 Register	P3	00h	000B1h	8
Port P4 Register	P4	00h	000B2h	8
Port PA Register	PA	00h	000B3h	8
Pull-Up Control Register 0	PUR0	00h	000B4h	8
Pull-Up Control Register 1	PUR1	00h	000B5h	8
Pull-Up Control Register 2	PUR2	00h	000B6h	8
Pull-Up Control Register 3	PUR3	00h	000B7h	8
Pull-Up Control Register 4	PUR4	00h	000B8h	8
Port I/O Function Control Register	PINSR	00h	000B9h	8
Drive Capacity Control Register 1	DRR1	00h	000BBh	8
Drive Capacity Control Register 3	DRR3	00h	000BDh	8
Open-Drain Control Register 0	POD0	00h	000C0h	8
Open-Drain Control Register 1	POD1	00h	000C1h	8
Open-Drain Control Register 2	POD2	00h	000C2h	8
Open-Drain Control Register 3	POD3	00h	000C3h	8
Open-Drain Control Register 4	POD4	00h	000C4h	8
Port PA Mode Control Register	PAMCR	11h	000C5h	8
Port 0 Function Mapping Register 0	PML0	00h	000C6h	8
Port 0 Function Mapping Register 1	PMH0	00h	000C7h	8
Port 1 Function Mapping Register 0	PML1	00h	000C8h	8
Port 1 Function Mapping Register 1	PMH1	00h	000C9h	8
Port 2 Function Mapping Register 0	PML2	00h	000CAh	8
Port 3 Function Mapping Register 0	PML3	00h	000CCh	8
Port 3 Function Mapping Register 1	PMH3	00h	000CDh	8
Port 4 Function Mapping Register 0	PML4	00h	000CEh	8
Port 4 Function Mapping Register 1	PMH4	00h	000CFh	8
Port 1 Function Mapping Expansion Register	PMH1E	00h	000D1h	8

12.2 Reading of Port Input Level

Regardless of the mapping settings for port functions, whether to read the port latch or the pin level can be selected when reading the Pi register (i = 0 to 4, or A).

12.2.1 Port I/O Function Control Register (PINSR)

Address 000B9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOINSEL	TRJIOSEL	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	The write value is invalid. The read value is undefined.	—
b1	—	Reserved	Set to 0. The read value is 0.	—
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	—			
b5	—			
b6	TRJIOSEL	TRJIO input signal select bit	0: Input from external TRJIO pin 1: Internal input from VCOUT1 of comparator B	R/W
b7	IOINSEL	Pin level forced read-out bit	0: Disabled (control by PDi register) 1: Enabled (read of pin input level)	R/W

Set the PRC4 bit in the PRCR register to 1 (write enabled) before rewriting the PINSR register.

[When the IOINSEL bit in the PINSR register is 0]
When the PDi_j bit (j = 0 to 7) in the PDi register (i = 0 to 4, or A) is 0 (input mode), if the Pi_j bit in the Pi register is read, the input level of the corresponding pin is read.
If the Pi_j bit in the Pi register is read when the PDi_j bit is 1 (output mode), the port latch is read.
[When the IOINSEL bit in the PINSR register is 1]
If the Pi register is read, the input level of the corresponding pin is read regardless of the setting of the PDi register.

12.3 Port 0

Figure 12.1 shows the Port 0 Pin Configuration.

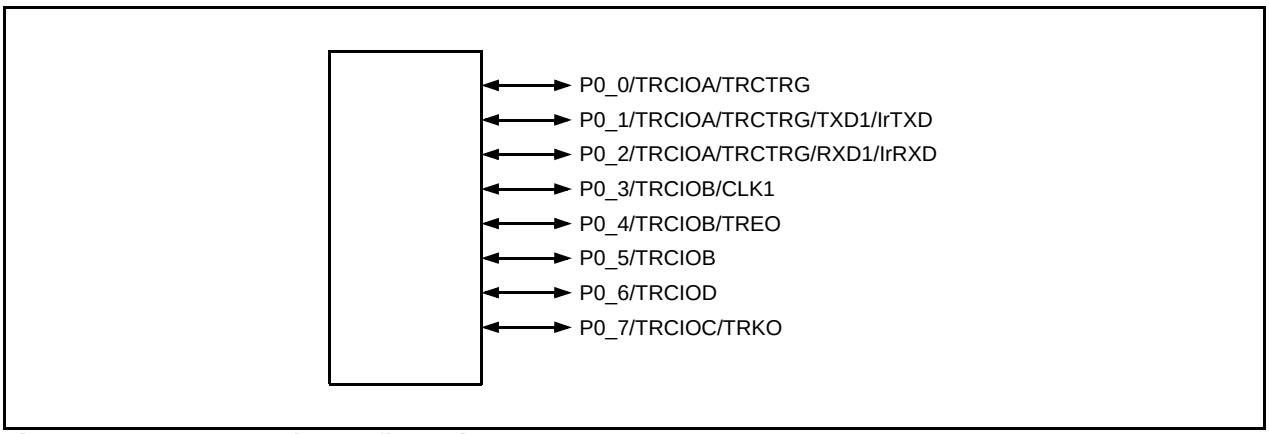


Figure 12.1 Port 0 Pin Configuration

12.3.1 Port P0 Direction Register (PD0)

Address 000A8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD0_7	PD0_6	PD0_5	PD0_4	PD0_3	PD0_2	PD0_1	PD0_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PD0_0	Port P0_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	PD0_1	Port P0_1 direction bit		R/W
b2	PD0_2	Port P0_2 direction bit		R/W
b3	PD0_3	Port P0_3 direction bit		R/W
b4	PD0_4	Port P0_4 direction bit		R/W
b5	PD0_5	Port P0_5 direction bit		R/W
b6	PD0_6	Port P0_6 direction bit		R/W
b7	PD0_7	Port P0_7 direction bit		R/W

The PD0 register is used to select whether I/O ports are used as input or output.
Each bit in the PD0 register corresponds to individual ports.

12.3.2 Port P0 Register (P0)

Address 000AEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P0_0	Port P0_0 bit	0: Low level 1: High level	R/W
b1	P0_1	Port P0_1 bit		R/W
b2	P0_2	Port P0_2 bit		R/W
b3	P0_3	Port P0_3 bit		R/W
b4	P0_4	Port P0_4 bit		R/W
b5	P0_5	Port P0_5 bit		R/W
b6	P0_6	Port P0_6 bit		R/W
b7	P0_7	Port P0_7 bit		R/W

The P0 register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the P0 register. The P0 register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pins. Each bit in the P0 register corresponds to individual ports.

12.3.3 Pull-Up Control Register 0 (PUR0)

Address 000B4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU0_7	PU0_6	PU0_5	PU0_4	PU0_3	PU0_2	PU0_1	PU0_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PU0_0	Port P0_0 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W
b1	PU0_1	Port P0_1 pull-up control bit		R/W
b2	PU0_2	Port P0_2 pull-up control bit		R/W
b3	PU0_3	Port P0_3 pull-up control bit		R/W
b4	PU0_4	Port P0_4 pull-up control bit		R/W
b5	PU0_5	Port P0_5 pull-up control bit		R/W
b6	PU0_6	Port P0_6 pull-up control bit		R/W
b7	PU0_7	Port P0_7 pull-up control bit		R/W

The PUR0 register is used to control the port P0 pull-up resistors. I/O ports are pulled up when the corresponding PD0_j bit (j = 0 to 7) in the PD0 register is set to 0 (input mode (functions as an I/O port)) and the PU0_j bit (j = 0 to 7) in the PUR0 register is set to 1. The input pins for peripheral functions are pulled up when the corresponding PD0_j bit is set to 0 and the PU0_j bit is set to 1.
Do not set the corresponding PU0_j bit to 1 for the output pins for peripheral functions.

12.3.4 Open-Drain Control Register 0 (POD0)

Address 000C0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	POD0_7	POD0_6	POD0_5	POD0_4	POD0_3	POD0_2	POD0_1	POD0_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POD0_0	Port P0_0 open-drain control bit	0: Not open-drain 1: Open-drain	R/W
b1	POD0_1	Port P0_1 open-drain control bit		R/W
b2	POD0_2	Port P0_2 open-drain control bit		R/W
b3	POD0_3	Port P0_3 open-drain control bit		R/W
b4	POD0_4	Port P0_4 open-drain control bit		R/W
b5	POD0_5	Port P0_5 open-drain control bit		R/W
b6	POD0_6	Port P0_6 open-drain control bit		R/W
b7	POD0_7	Port P0_7 open-drain control bit		R/W

The POD0 register is used to select whether the output type is CMOS output or N-channel open-drain output. These settings are enabled when the peripheral function output or output port function is selected.
The corresponding pins are set to N-channel open-drain output when the POD0_j bit (j = 0 to 7) is set to 1 (open-drain), and CMOS output when the bit is set to 0 (not open-drain).

12.3.5 Port 0 Function Mapping Register 0 (PML0)

Address 000C6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P03SEL1	P03SEL0	P02SEL1	P02SEL0	P01SEL1	P01SEL0	P00SEL1	P00SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P00SEL0	Port P0_0 function select bits	b1 b0 0 0: I/O port 0 1: TRCIOA/TRCTRG Other than the above: Do not set.	R/W
b1	P00SEL1			R/W
b2	P01SEL0	Port P0_1 function select bits	b3 b2 0 0: I/O port 0 1: TRCIOA/TRCTRG 1 0: TXD1/IrTXD 1 1: Do not set.	R/W
b3	P01SEL1			R/W
b4	P02SEL0	Port P0_2 function select bits	b5 b4 0 0: I/O port 0 1: TRCIOA/TRCTRG 1 0: RXD1/IrRXD 1 1: Do not set.	R/W
b5	P02SEL1			R/W
b6	P03SEL0	Port P0_3 function select bits	b7 b6 0 0: I/O port 0 1: TRCIOB 1 0: CLK1 1 1: Do not set.	R/W
b7	P03SEL1			R/W

The PML0 register is used to select the functions of pins P0_0 to P0_3.

12.3.6 Port 0 Function Mapping Register 1 (PMH0)

Address 000C7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P07SEL1	P07SEL0	P06SEL1	P06SEL0	P05SEL1	P05SEL0	P04SEL1	P04SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P04SEL0	Port P0_4 function select bits	b1 b0 0 0: I/O port 0 1: TRCIOB 1 0: TREO 1 1: Do not set.	R/W
b1	P04SEL1			R/W
b2	P05SEL0	Port P0_5 function select bits	b3 b2 0 0: I/O port 0 1: TRCIOB Other than the above: Do not set.	R/W
b3	P05SEL1			R/W
b4	P06SEL0	Port P0_6 function select bits	b5 b4 0 0: I/O port 0 1: TRCIOD Other than the above: Do not set.	R/W
b5	P06SEL1			R/W
b6	P07SEL0	Port P0_7 function select bits	b7 b6 0 0: I/O port 0 1: TRCIOC 1 0: TRKO 1 1: Do not set.	R/W
b7	P07SEL1			R/W

The PMH0 register is used to select the functions of pins P0_4 to P0_7.

12.3.7 Pin Settings for Port 0

Tables 12.4 to 12.11 list the pin settings for port 0.

Table 12.4 Port P0_0/TRCIOA/TRCTRG

Register	PD0	PML0		Timer RC Setting	Function
Bit	PD0_0	P00SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.33 TRCIOA Pin Settings**.	TRCIOA input
	X	0	1	See **Table 12.33 TRCIOA Pin Settings**.	TRCIOA output
	X	0	1	See **Table 12.33 TRCIOA Pin Settings**.	TRCTRG input

X: 0 or 1

Table 12.5 Port P0_1/TRCIOA/TRCTRG/TXD1/IrTXD

Register	PD0	PML0		Timer RC Setting	Function
Bit	PD0_1	P01SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.33 TRCIOA Pin Settings**.	TRCIOA input
	X	0	1	See **Table 12.33 TRCIOA Pin Settings**.	TRCIOA output
	X	0	1	See **Table 12.33 TRCIOA Pin Settings**.	TRCTRG input
	X	1	0	X	TXD1/IrTXD output

X: 0 or 1

Table 12.6 Port P0_2/TRCIOA/TRCTRG/RXD1/IrRXD

Register	PD0	PML0		Timer RC Setting	Function
Bit	PD0_2	P02SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.33 TRCIOA Pin Settings**.	TRCIOA input
	X	0	1	See **Table 12.33 TRCIOA Pin Settings**.	TRCIOA output
	X	0	1	See **Table 12.33 TRCIOA Pin Settings**.	TRCTRG input
	X	1	0	X	RXD1/IrRXD input

X: 0 or 1

Table 12.7 Port P0_3/TRCIOB/CLK1

Register	PD0	PML0		Timer RC Setting	Function
Bit	PD0_3	P03SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB input
	X	0	1	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB output
	X	1	0	X	CLK1

X: 0 or 1

Table 12.8 Port P0_4/TRCIOB/TREO

Register	PD0	PMH0		Timer RC Setting	Function
Bit	PD0_4	P04SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB input
	X	0	1	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB output
	X	1	0	X	TREO output

X: 0 or 1

Table 12.9 Port P0_5/TRCIOB

Register	PD0	PMH0		Timer RC Setting	Function
Bit	PD0_5	P05SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB input
	X	0	1	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB output

X: 0 or 1

Table 12.10 Port P0_6/TRCIOD

Register	PD0	PMH0		Timer RC Setting	Function
Bit	PD0_6	P06SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.36 TRCIOD Pin Settings**.	TRCIOD input
	X	0	1	See **Table 12.36 TRCIOD Pin Settings**.	TRCIOD output

X: 0 or 1

Table 12.11 Port P0_7/TRCIOC/TRKO

Register	PD0	PMH0		Timer RC Setting	Function
Bit	PD0_7	P07SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.35 TRCIOC Pin Settings**.	TRCIOC input
	X	0	1	See **Table 12.35 TRCIOC Pin Settings**.	TRCIOC output
	X	1	0	X	TRKO output

X: 0 or 1

12.4 Port 1

Figure 12.2 shows the Port 1 Pin Configuration.

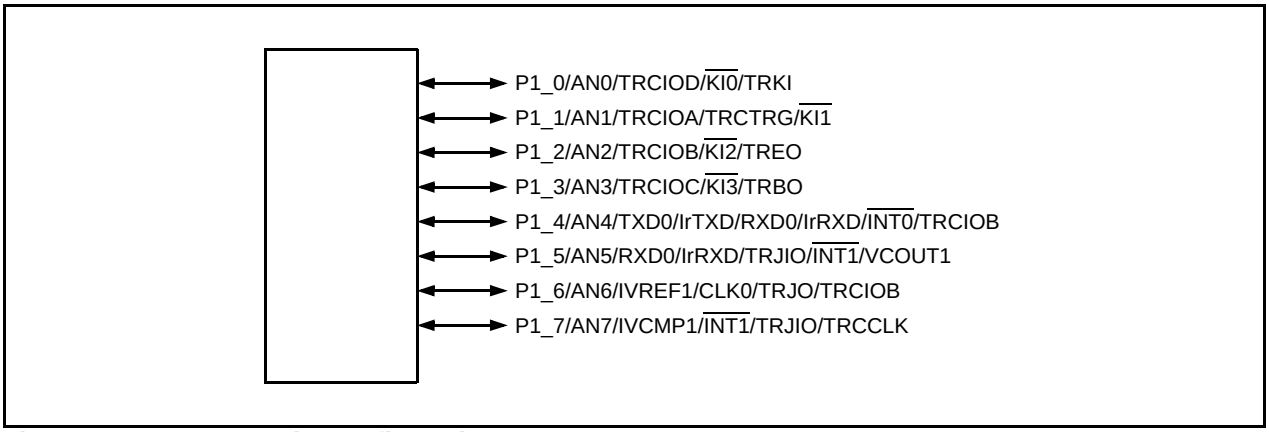


Figure 12.2 Port 1 Pin Configuration

12.4.1 Port P1 Direction Register (PD1)

Address 000A9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD1_7	PD1_6	PD1_5	PD1_4	PD1_3	PD1_2	PD1_1	PD1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PD1_0	Port P1_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	PD1_1	Port P1_1 direction bit		R/W
b2	PD1_2	Port P1_2 direction bit		R/W
b3	PD1_3	Port P1_3 direction bit		R/W
b4	PD1_4	Port P1_4 direction bit		R/W
b5	PD1_5	Port P1_5 direction bit		R/W
b6	PD1_6	Port P1_6 direction bit		R/W
b7	PD1_7	Port P1_7 direction bit		R/W

The PD1 register is used to select whether I/O ports are used as input or output.
Each bit in the PD1 register corresponds to individual ports.

12.4.2 Port P1 Register (P1)

Address 000AFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P1_0	Port P1_0 bit	0: Low level 1: High level	R/W
b1	P1_1	Port P1_1 bit		R/W
b2	P1_2	Port P1_2 bit		R/W
b3	P1_3	Port P1_3 bit		R/W
b4	P1_4	Port P1_4 bit		R/W
b5	P1_5	Port P1_5 bit		R/W
b6	P1_6	Port P1_6 bit		R/W
b7	P1_7	Port P1_7 bit		R/W

The P1 register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the P1 register. The P1 register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pins. Each bit in the P1 register corresponds to individual ports.

12.4.3 Pull-Up Control Register 1 (PUR1)

Address 000B5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU1_7	PU1_6	PU1_5	PU1_4	PU1_3	PU1_2	PU1_1	PU1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PU1_0	Port P1_0 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W
b1	PU1_1	Port P1_1 pull-up control bit		R/W
b2	PU1_2	Port P1_2 pull-up control bit		R/W
b3	PU1_3	Port P1_3 pull-up control bit		R/W
b4	PU1_4	Port P1_4 pull-up control bit		R/W
b5	PU1_5	Port P1_5 pull-up control bit		R/W
b6	PU1_6	Port P1_6 pull-up control bit		R/W
b7	PU1_7	Port P1_7 pull-up control bit		R/W

The PUR1 register is used to control the port P1 pull-up resistors. I/O ports are pulled up when the corresponding PD1_j bit (j = 0 to 7) in the PD1 register is set to 0 (input mode (functions as an I/O port)) and the PU1_j bit (j = 0 to 7) in the PUR1 register is set to 1. The input pins for peripheral functions are pulled up when the corresponding PD1_j bit is set to 0 and the PU1_j bit is set to 1.
Do not set the corresponding PU1_j bit to 1 for the output pins for peripheral functions.

12.4.4 Drive Capacity Control Register 1 (DRR1)

Address 000BBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	DRR1_5	DRR1_4	DRR1_3	DRR1_2	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	—
b1	—			
b2	DRR1_2	Port P1_2 drive capacity control bit	0: Low drive capacity 1: High drive capacity (1)	R/W
b3	DRR1_3	Port P1_3 drive capacity control bit		R/W
b4	DRR1_4	Port P1_4 drive capacity control bit		R/W
b5	DRR1_5	Port P1_5 drive capacity control bit		R/W
b6	—	Reserved	Set to 0.	—
b7	—			

Note:
1. Both H and L output are set to high drive capacity.

The DRR1 register is used to select the drive capacity of the output transistors (low or high) when P1 is set to output (an output port or a peripheral function output pin). The drive capacity of the corresponding output transistors is high when the DRR1_j bit (j = 2 to 5) in the DRR1 register is set to 1.

12.4.5 Open-Drain Control Register 1 (POD1)

Address 000C1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	POD1_7	POD1_6	POD1_5	POD1_4	POD1_3	POD1_2	POD1_1	POD1_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POD1_0	Port P1_0 open-drain control bit	0: Not open-drain 1: Open-drain	R/W
b1	POD1_1	Port P1_1 open-drain control bit		R/W
b2	POD1_2	Port P1_2 open-drain control bit		R/W
b3	POD1_3	Port P1_3 open-drain control bit		R/W
b4	POD1_4	Port P1_4 open-drain control bit		R/W
b5	POD1_5	Port P1_5 open-drain control bit		R/W
b6	POD1_6	Port P1_6 open-drain control bit		R/W
b7	POD1_7	Port P1_7 open-drain control bit		R/W

The POD1 register is used to select whether the output type is CMOS output or N-channel open-drain output. These settings are enabled when the peripheral function output or output port function is selected.
The corresponding pins are set to N-channel open-drain output when the POD1_j bit (j = 0 to 7) is set to 1 (open-drain), and CMOS output when the bit is set to 0 (not open-drain).

12.4.6 Port 1 Function Mapping Register 0 (PML1)

Address 000C8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P13SEL1	P13SEL0	P12SEL1	P12SEL0	P11SEL1	P11SEL0	P10SEL1	P10SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P10SEL0	Port P1_0 function select bits	b1 b0 0 0: I/O port or AN0 input 0 1: TRCIOD 1 0: $\overline{KI0}$ 1 1: TRKI	R/W
b1	P10SEL1			R/W
b2	P11SEL0	Port P1_1 function select bits	b3 b2 0 0: I/O port or AN1 input 0 1: TRCIOA/TRCTRG 1 0: $\overline{KI1}$ 1 1: Do not set.	R/W
b3	P11SEL1			R/W
b4	P12SEL0	Port P1_2 function select bits	b5 b4 0 0: I/O port or AN2 input 0 1: TRCIOB 1 0: $\overline{KI2}$ 1 1: TREO	R/W
b5	P12SEL1			R/W
b6	P13SEL0	Port P1_3 function select bits	b7 b6 0 0: I/O port or AN3 input 0 1: TRCIOC 1 0: $\overline{KI3}$ 1 1: TRBO	R/W
b7	P13SEL1			R/W

The PML1 register is used to select the functions of pins P1_0 to P1_3.

12.4.7 Port 1 Function Mapping Register 1 (PMH1)

Address 000C9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P17SEL1	P17SEL0	P16SEL1	P16SEL0	P15SEL1	P15SEL0	P14SEL1	P14SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P14SEL0	Port P1_4 function select bits	bx b1 b0 0 0 0: I/O port or AN4 input 0 0 1: TXD0/IrTXD 0 1 0: RXD0/IrRXD 0 1 1: INT0 1 0 0: TRCIOB Other than the above: Do not set. (bx: P14SEL2 bit in the PMH1E register)	R/W
b1	P14SEL1			R/W
b2	P15SEL0	Port P1_5 function select bits	bx b3 b2 0 0 0: I/O port or AN5 input 0 0 1: RXD0/IrRXD 0 1 0: TRJIO 0 1 1: INT1 1 0 0: VCOUT1 Other than the above: Do not set. (bx: P15SEL2 bit in the PMH1E register)	R/W
b3	P15SEL1			R/W
b4	P16SEL0	Port P1_6 function select bits	b5 b4 0 0: I/O port or AN6 input or IVREF1 input 0 1: CLK0 1 0: TRJO 1 1: TRCIOB	R/W
b5	P16SEL1			R/W
b6	P17SEL0	Port P1_7 function select bits	b7 b6 0 0: I/O port or AN7 input or IVCMP1 input 0 1: INT1 1 0: TRJIO 1 1: TRCCLK	R/W
b7	P17SEL1			R/W

The PMH1 register is used to select the functions of pins P1_4 to P1_7.

12.4.8 Port 1 Function Mapping Expansion Register (PMH1E)

Address 000D1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	P15SEL2	—	P14SEL2
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P14SEL2	The P1_4 pin function is selected in conjunction with bits P14SEL0 to P14SEL1 in the PMH1 register. For details, see **12.4.7 Port 1 Function Mapping Register 1 (PMH1)**.		R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	P15SEL2	The P1_5 pin function is selected in conjunction with bits P15SEL0 to P15SEL1 in the PMH1 register. For details, see **12.4.7 Port 1 Function Mapping Register 1 (PMH1)**.		R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

The PMH1E register is used to select the port 1 function in conjunction with registers PML1 and PMH1.

12.4.9 Pin Settings for Port 1

Tables 12.12 to 12.19 list the pin settings for port 1.

Table 12.12 Port P1_0/AN0/TRCIOD/$\overline{KI0}$/TRKI

Register	PD1	ADINSEL			PML1		Timer RC Setting	Function
Bit	PD1_0	ADGSEL		CH0	P10SEL			
		1	0		1	0		
Setting value	0	X	X	X	0	0	X	Input port
	1	X	X	X	0	0	X	Output port
	0	0	0	0	0	0	X	A/D converter input (AN0)
	X	X	X	X	0	1	See **Table 12.36 TRCIOD Pin Settings**.	TRCIOD input
	X	X	X	X	0	1	See **Table 12.36 TRCIOD Pin Settings**.	TRCIOD output
	X	X	X	X	1	0	X	$\overline{KI0}$ input
	X	X	X	X	1	1	X	TRKI input

X: 0 or 1

Table 12.13 Port P1_1/AN1/TRCIOA/TRCTRG/$\overline{KI1}$

Register	PD1	ADINSEL			PML1		Timer RC Setting	Function
Bit	PD1_1	ADGSEL		CH0	P11SEL			
		1	0		1	0		
Setting value	0	X	X	X	0	0	X	Input port
	1	X	X	X	0	0	X	Output port
	0	0	0	1	0	0	X	A/D converter input (AN1)
	X	X	X	X	0	1	See **Table 12.33 TRCIOA Pin Settings**.	TRCIOA input or TRCTRG input
	X	X	X	X	0	1	See **Table 12.33 TRCIOA Pin Settings**.	TRCIOA output
	X	X	X	X	1	0	X	$\overline{KI1}$ input

X: 0 or 1

Table 12.14 Port P1_2/AN2/TRCIOB/$\overline{KI2}$/TREO

Register	PD1	ADINSEL			PML1		Timer RC Setting	Function
Bit	PD1_2	ADGSEL		CH0	P12SEL			
		1	0		1	0		
Setting value	0	X	X	X	0	0	X	Input port
	1	X	X	X	0	0	X	Output port
	0	0	1	0	0	0	X	A/D converter input (AN2)
	X	X	X	X	0	1	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB input
	X	X	X	X	0	1	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB output
	X	X	X	X	1	0	X	$\overline{KI2}$ input
	X	X	X	X	1	1	X	TREO output

X: 0 or 1

Table 12.15 Port P1_3/AN3/TRCIOC/$\overline{KI3}$/TRBO

Register	PD1	ADINSEL			PML1		Timer RC Setting	Timer RB2 Setting	Function
Bit	PD1_3	ADGSEL		CH0	P13SEL				
		1	0		1	0			
Setting value	0	X	X	X	0	0	X	X	Input port
	1	X	X	X	0	0	X	X	Output port
	0	0	1	1	0	0	X	X	A/D converter input (AN3)
	X	X	X	X	0	1	See **Table 12.35 TRCIOC Pin Settings**.	X	TRCIOC input
	X	X	X	X	0	1	See **Table 12.35 TRCIOC Pin Settings**.	X	TRCIOC output
	X	X	X	X	1	0	X	X	$\overline{KI3}$ input
	X	X	X	X	1	1	X	X	TRBO output

X: 0 or 1

Table 12.16 Port P1_4/AN4/TXD0/IrTXD/RXD0/IrRXD/$\overline{\text{INT0}}$/TRCIOB

Register	PD1	ADINSEL			PMH1E	PMH1		Timer RC Setting	Function
Bit	PD1_4	ADGSEL		CH0	P14SEL2	P14SEL			
		1	0			1	0		
Setting value	0	X	X	X	0	0	0	X	Input port
	1	X	X	X	0	0	0	X	Output port
	0	1	0	0	0	0	0	X	A/D converter input (AN4)
	X	X	X	X	0	0	1	X	TXD0/IrTXD output
	X	X	X	X	0	1	0	X	RXD0/IrRXD input
	X	X	X	X	0	1	1	X	$\overline{\text{INT0}}$ input
	X	X	X	X	1	0	0	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB input
	X	X	X	X	1	0	0	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB output

X: 0 or 1

Table 12.17 Port P1_5/AN5/RXD0/IrRXD/TRJIO/$\overline{\text{INT1}}$/VCOUT1

Register	PD1	ADINSEL			PMH1E	PMH1		TRJIOC	TRJMR			Function
Bit	PD1_5	ADGSEL		CH0	P15SEL2	P15SEL		TOPCR	TMOD			
		1	0			1	0		2	1	0	
Setting value	0	X	X	X	0	0	0	X	X	X	X	Input port
	1	X	X	X	0	0	0	X	X	X	X	Output port
	0	1	1	0	0	0	0	X	X	X	X	A/D converter input (AN5)
	X	X	X	X	0	0	1	X	X	X	X	RXD0/IrRXD input
	X	X	X	X	0	1	0	0	Other than 000b, 001b			TRJIO input
	X	X	X	X	0	1	0	0	001b			TRJIO pulse output
	X	X	X	X	0	1	1	X	X	X	X	$\overline{\text{INT1}}$ input
	X	X	X	X	1	0	0	X	X	X	X	VCOUT1 output

X: 0 or 1

Table 12.18 Port P1_6/AN6/IVREF1/CLK0/TRJO/TRCIOB

Register	PD1	ADINSEL			PMH1		U0MR				Timer RC Setting	Function
Bit	PD1_6	ADGSEL		CH0	P16SEL		SMD			CKDIR		
		1	0		1	0	2	1	0			
Setting value	0	X	X	X	0	0	X	X	X	X	X	Input port/IVREF1
	1	X	X	X	0	0	X	X	X	X	X	Output port
	0	1	1	1	X	X	X	X	X	X	X	A/D converter input (AN6)
	X	X	X	X	0	1	X	X	X	1	X	CLK0 (external clock) input
	X	X	X	X	0	1	0	0	1	0	X	CLK0 (internal clock) output
	X	X	X	X	1	0	X	X	X	X	X	TRJO output
	X	X	X	X	1	1	X	X	X	X	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB input
	X	X	X	X	1	1	X	X	X	X	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB output

X: 0 or 1

Table 12.19 Port P1_7/AN7/IVCMP1/$\overline{\text{INT1}}$/TRJIO/TRCCLK

Register	PD1	ADINSEL			PMH1		TRJIOC	TRJMR			Function
Bit	PD1_7	ADGSEL		CH0	P17SEL		TOPCR	TMOD			
		1	0		1	0		2	1	0	
Setting value	0	X	X	X	0	0	X	X	X	X	Input port/IVCMP1
	1	X	X	X	0	0	X	X	X	X	Output port
	0	1	0	1	0	0	X	X	X	X	A/D converter input (AN7)
	X	X	X	X	0	1	X	X	X	X	$\overline{\text{INT1}}$ input
	X	X	X	X	1	0	0	Other than 000b, 001b			TRJIO input
	X	X	X	X	1	0	0	001b			TRJIO pulse output
	X	X	X	X	1	1	X	X	X	X	TRCCLK input

X: 0 or 1

12.5 Port 2

Figure 12.3 shows the Port 2 Pin Configuration.

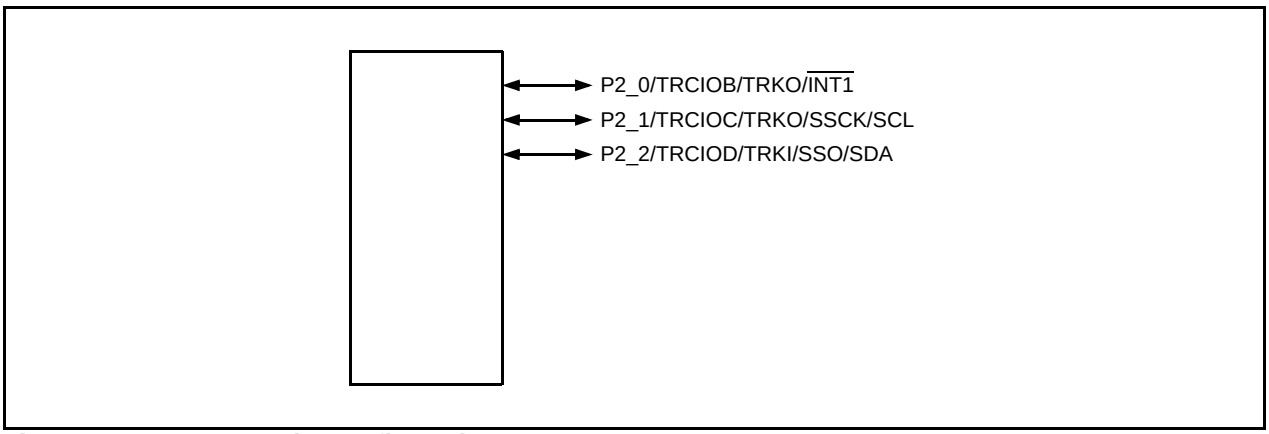


Figure 12.3 Port 2 Pin Configuration

12.5.1 Port P2 Direction Register (PD2)

Address 000AAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	PD2_2	PD2_1	PD2_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PD2_0	Port P2_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	PD2_1	Port P2_1 direction bit		R/W
b2	PD2_2	Port P2_2 direction bit		R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

The PD2 register is used to select whether I/O ports are used as input or output.
Each bit in the PD2 register corresponds to individual ports.

12.5.2 Port P2 Register (P2)

Address 000B0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	P2_2	P2_1	P2_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P2_0	Port P2_0 bit	0: Low level 1: High level	R/W
b1	P2_1	Port P2_1 bit		R/W
b2	P2_2	Port P2_2 bit		R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

The P2 register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the P2 register. The P2 register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pins. Each bit in the P2 register corresponds to individual ports.

12.5.3 Pull-Up Control Register 2 (PUR2)

Address 000B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	PU2_2	PU2_1	PU2_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PU2_0	Port P2_0 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W
b1	PU2_1	Port P2_1 pull-up control bit		R/W
b2	PU2_2	Port P2_2 pull-up control bit		R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

The PUR2 register is used to control the port P2 pull-up resistors. I/O ports are pulled up when the corresponding PD2_j bit (j = 0 to 2) in the PD2 register is set to 0 (input mode (functions as an I/O port)) and the PU2_j bit (j = 0 to 2) in the PUR2 register is set to 1. The input pins for peripheral functions are pulled up when the corresponding PD2_j bit is set to 0 and the PU2_j bit is set to 1.
Do not set the corresponding PU2_j bit to 1 for the output pins for peripheral functions.

12.5.4 Open-Drain Control Register 2 (POD2)

Address 000C2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	POD2_2	POD2_1	POD2_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POD2_0	Port P2_0 open-drain control bit	0: Not open-drain 1: Open-drain	R/W
b1	POD2_1	Port P2_1 open-drain control bit		R/W
b2	POD2_2	Port P2_2 open-drain control bit		R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

The POD2 register is used to select whether the output type is CMOS output or N-channel open-drain output. These settings are enabled when the peripheral function output or output port function is selected.
The corresponding pins are set to N-channel open-drain output when the POD2_j bit (j = 0 to 2) is set to 1 (open-drain), and CMOS output when the bit is set to 0 (not open-drain).

12.5.5 Port 2 Function Mapping Register 0 (PML2)

Address 000CAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	P22SEL1	P22SEL0	P21SEL1	P21SEL0	P20SEL1	P20SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P20SEL0	Port P2_0 function select bits	b1 b0 0 0: I/O port 0 1: TRCIOB 1 0: $\overline{\text{TRKO}}$ 1 1: INT1	R/W
b1	P20SEL1			R/W
b2	P21SEL0	Port P2_1 function select bits	b3 b2 0 0: I/O port 0 1: TRCIOC 1 0: TRKO 1 1: SSCK/SCL	R/W
b3	P21SEL1			R/W
b4	P22SEL0	Port P2_2 function select bits	b5 b4 0 0: I/O port 0 1: TRCIOD 1 0: TRKI 1 1: SSO/SDA	R/W
b5	P22SEL1			R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The PML2 register is used to select the functions of pins P2_0 to P2_2.

12.5.6 Pin Settings for Port 2

Tables 12.20 to 12.22 list the pin settings for port 2.

Table 12.20 Port P2_0/TRCIOB/TRKO/$\overline{\text{INT1}}$

Register	PD2	PML2		Timer RC Setting	Function
Bit	PD2_0	P20SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB input
	X	0	1	See **Table 12.34 TRCIOB Pin Settings**.	TRCIOB output
	X	1	0	X	TRKO output
	X	1	1	X	$\overline{\text{INT}}$ input

X: 0 or 1

Table 12.21 Port P2_1/TRCIOC/TRKO/SSCK/SCL

Register	PD2	PML2		Timer RC Setting	Function
Bit	PD2_1	P21SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.35 TRCIOC Pin Settings**.	TRCIOC input
	X	0	1	See **Table 12.35 TRCIOC Pin Settings**.	TRCIOC output
	X	1	0	X	TRKO output
	X	1	1	X	SSCK/SCL

X: 0 or 1

Table 12.22 Port P2_2/TRCIOD/TRKI/SSO/SDA

Register	PD2	PML2		Timer RC Setting	Function
Bit	PD2_2	P22SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.36 TRCIOD Pin Settings**.	TRCIOD input
	X	0	1	See **Table 12.36 TRCIOD Pin Settings**.	TRCIOD output
	X	1	0	X	TRKI input
	X	1	1	X	SSO/SDA

X: 0 or 1

12.6 Port 3

Figure 12.4 shows the Port 3 Pin Configuration.

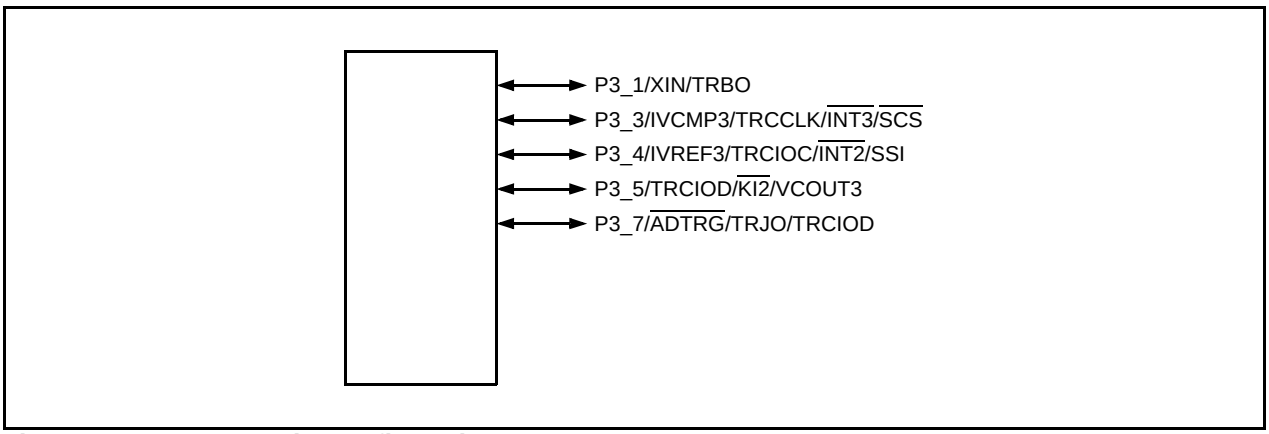


Figure 12.4 Port 3 Pin Configuration

12.6.1 Port P3 Direction Register (PD3)

Address 000ABh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD3_7	—	PD3_5	PD3_4	PD3_3	—	PD3_1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	PD3_1	Port P3_1 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	PD3_3	Port P3_3 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b4	PD3_4	Port P3_4 direction bit		R/W
b5	PD3_5	Port P3_5 direction bit		R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	PD3_7	Port P3_7 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W

The PD3 register is used to select whether I/O ports are used as input or output.
Each bit in the PD3 register corresponds to individual ports.

12.6.2 Port P3 Register (P3)

Address 000B1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P3_7	—	P3_5	P3_4	P3_3	—	P3_1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	P3_1	Port P3_1 bit	0: Low level 1: High level	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	P3_3	Port P3_3 bit	0: Low level 1: High level	R/W
b4	P3_4	Port P3_4 bit		R/W
b5	P3_5	Port P3_5 bit		R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	P3_7	Port P3_7 bit	0: Low level 1: High level	R/W

The P3 register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the P3 register. The P3 register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pins. Each bit in the P3 register corresponds to individual ports.

12.6.3 Pull-Up Control Register 3 (PUR3)

Address 000B7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU3_7	—	PU3_5	PU3_4	PU3_3	—	PU3_1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	PU3_1	Port P3_1 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	PU3_3	Port P3_3 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W
b4	PU3_4	Port P3_4 pull-up control bit		R/W
b5	PU3_5	Port P3_5 pull-up control bit		R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	PU3_7	Port P3_7 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W

The PUR3 register is used to control the port P3 pull-up resistors. I/O ports are pulled up when the corresponding PD3_j bit (j = 1, 3 to 5, or 7) in the PD3 register is set to 0 (input mode (functions as an I/O port)) and the PU3_j bit (j = 1, 3 to 5, or 7) in the PUR3 register is set to 1. The input pins for peripheral functions are pulled up when the corresponding PD3_j bit is set to 0 and the PU3_j bit is set to 1.
Do not set the corresponding PU3_j bit to 1 for the output pins for peripheral functions.

12.6.4 Drive Capacity Control Register 3 (DRR3)

Address 000BDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DRR3_7	—	DRR3_5	DRR3_4	DRR3_3	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	DRR3_3	Port P3_3 drive capacity control bit	0: Low drive capacity 1: High drive capacity (1)	R/W
b4	DRR3_4	Port P3_4 drive capacity control bit		R/W
b5	DRR3_5	Port P3_5 drive capacity control bit		R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	DRR3_7	Port P3_7 drive capacity control bit	0: Low drive capacity 1: High drive capacity	R/W

Note:
1. Both H and L output are set to high drive capacity.

The DRR3 register is used to select the drive capacity of the output transistors (low or high) when P3 is set to output (an output port or a peripheral function output pin). The drive capacity of the corresponding output transistors is high when the DRR3_j bit (j = 3 to 5, or 7) in the DRR3 register is set to 1.

12.6.5 Open-Drain Control Register 3 (POD3)

Address 000C3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	POD3_7	—	POD3_5	POD3_4	POD3_3	—	POD3_1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	POD3_1	Port P3_1 open-drain control bit	0: Not open-drain 1: Open-drain	R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	POD3_3	Port P3_3 open-drain control bit	0: Not open-drain 1: Open-drain	R/W
b4	POD3_4	Port P3_4 open-drain control bit		R/W
b5	POD3_5	Port P3_5 open-drain control bit		R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	POD3_7	Port P3_7 open-drain control bit	0: Not open-drain 1: Open-drain	R/W

The POD3 register is used to select whether the output type is CMOS output or N-channel open-drain output. These settings are enabled when the peripheral function output or output port function is selected.
The corresponding pins are set to N-channel open-drain output when the POD3_j bit (j = 1, 3 to 5, or 7) is set to 1 (open-drain), and CMOS output when the bit is set to 0 (not open-drain).

12.6.6 Port 3 Function Mapping Register 0 (PML3)

Address 000CCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P33SEL1	P33SEL0	—	—	P31SEL1	P31SEL0	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	P31SEL0	Port P3_1 function select bits	b3 b2 0 0: I/O port or XIN input 0 1: TRBO Other than the above: Do not set.	R/W
b3	P31SEL1			R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	P33SEL0	Port P3_3 function select bits	b7 b6 0 0: I/O port or IVCMP3 input 0 1: TRCCLK 1 0: $\overline{\text{INT3}}$ 1 1: $\overline{\text{SCS}}$	R/W
b7	P33SEL1			R/W

The PML3 register is used to select the functions of pins P3_1 and P3_3.

12.6.7 Port 3 Function Mapping Register 1 (PMH3)

Address 000CDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P37SEL1	P37SEL0	—	—	P35SEL1	P35SEL0	P34SEL1	P34SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P34SEL0	Port P3_4 function select bits	b1 b0 0 0: I/O port or IVREF3 input 0 1: TRCIOC 1 0: INT2 1 1: SSI	R/W
b1	P34SEL1			R/W
b2	P35SEL0	Port P3_5 function select bits	b3 b2 0 0: I/O port 0 1: TRCIOD 1 0: KI2 1 1: VCOUT3	R/W
b3	P35SEL1			R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	P37SEL0	Port P3_7 function select bits	b7 b6 0 0: I/O port 0 1: ADTRG 1 0: TRJO 1 1: TRCIOD	R/W
b7	P37SEL1			R/W

The PMH3 register is used to select the functions of pins P3_4, P3_5, and P3_7.

12.6.8 Pin Settings for Port 3

Tables 12.23 to 12.27 list the pin settings for port 3.

Table 12.23 Port P3_1/XIN/TRBO

Register	PD3	PML3		EXCKCR		Function
Bit	PD3_3	P31SEL		CKPT		
		1	0	1	0	
Setting value	0	0	0	X	0	Input port
	1	0	0	X	0	Output port
	X	0	0	0	1	XIN clock input (external clock input)
	X	0	0	1	1	XIN input
	X	0	1	X	X	TRBO output

X: 0 or 1

Table 12.24 Port P3_3/IVCMP3/TRCCLK/$\overline{\text{INT3}}$/$\overline{\text{SCS}}$

Register	PD3	PML3		Function
Bit	PD3_3	P33SEL		
		1	0	
Setting value	0	0	0	Input port/IVCMP3
	1	0	0	Output port
	X	0	1	TRCCLK input
	X	1	0	$\overline{\text{INT3}}$ input
	X	1	1	$\overline{\text{SCS}}$ input/output

X: 0 or 1

Table 12.25 Port P3_4/IVREF3/TRCIOC/$\overline{\text{INT2}}$/SSI

Register	PD3	PMH3		Timer RC Setting	Function
Bit	PD3_4	P34SEL			
		1	0		
Setting value	0	0	0	X	Input port/IVREF3
	1	0	0	X	Output port
	X	0	1	See **Table 12.35 TRCIOC Pin Settings**.	TRCIOC input
	X	0	1	See **Table 12.35 TRCIOC Pin Settings**.	TRCIOC output
	X	1	0	X	$\overline{\text{INT2}}$ input
	X	1	1	X	SSI input/output

X: 0 or 1

Table 12.26 Port P3_5/TRCIOD/$\overline{\text{KI2}}$/VCOUT3

Register	PD3	PMH3		Timer RC Setting	Function
Bit	PD3_5	P35SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	See **Table 12.36 TRCIOD Pin Settings**.	TRCIOD input
	X	0	1	See **Table 12.36 TRCIOD Pin Settings**.	TRCIOD output
	X	1	0	X	$\overline{\text{KI2}}$ input
	X	1	1	X	VCOUT3 output

X: 0 or 1

Table 12.27 Port P3_7/$\overline{\text{ADTRG}}$/TRJO/TRCIOD

Register	PD3	PMH3		Timer RC Setting	Function
Bit	PD3_7	P37SEL			
		1	0		
Setting value	0	0	0	X	Input port
	1	0	0	X	Output port
	X	0	1	X	$\overline{\text{ADTRG}}$ input
	X	1	0	X	TRJO output
	X	1	1	See **Table 12.36 TRCIOD Pin Settings**.	TRCIOD input
	X	1	1	See **Table 12.36 TRCIOD Pin Settings**.	TRCIOD output

X: 0 or 1

12.7 Port 4

Figure 12.5 shows the Port 4 Pin Configuration.

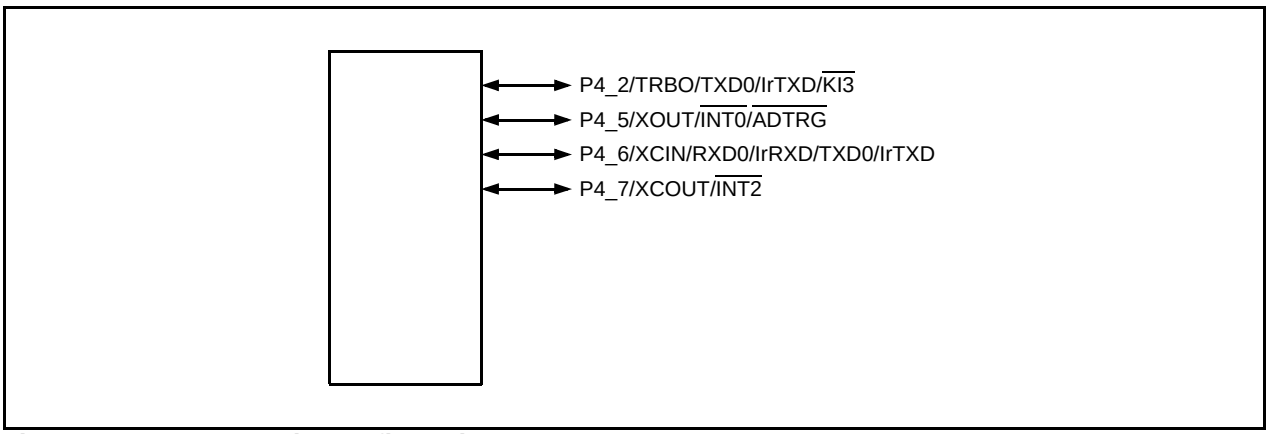


Figure 12.5 Port 4 Pin Configuration

12.7.1 Port P4 Direction Register (PD4)

Address 000ACh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PD4_7	PD4_6	PD4_5	—	—	PD4_2	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	PD4_2	Port P4_2 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	PD4_5	Port P4_5 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b6	PD4_6	Port P4_6 direction bit		R/W
b7	PD4_7	Port P4_7 direction bit		R/W

The PD4 register is used to select whether I/O ports are used as input or output.
Each bit in the PD4 register corresponds to individual ports.

12.7.2 Port P4 Register (P4)

Address 000B2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P4_7	P4_6	P4_5	—	—	P4_2	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	P4_2	Port P4_2 bit	0: Low level 1: High level	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	P4_5	Port P4_5 bit	0: Low level 1: High level	R/W
b6	P4_6	Port P4_6 bit		R/W
b7	P4_7	Port P4_7 bit		R/W

The P4 register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the P4 register. The P4 register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pin. Each bit in the P4 register corresponds to individual ports.

12.7.3 Pull-Up Control Register 4 (PUR4)

Address 000B8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU4_7	PU4_6	PU4_5	—	—	PU4_2	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	PU4_2	Port P4_2 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	PU4_5	Port P4_5 pull-up control bit	0: No pull-up resistor 1: Pull-up resistor	R/W
b6	PU4_6	Port P4_6 pull-up control bit		R/W
b7	PU4_7	Port P4_7 pull-up control bit		R/W

The PUR4 register is used to control the port P4 pull-up resistors. I/O ports are pulled up when the corresponding PD4_j bit (j = 2, or 5 to 7) in the PD4 register is set to 0 (input mode (functions as I/O port)) and the PU4_j bit (j = 2, or 5 to 7) in the PUR4 register is set to 1. The input pins for peripheral functions are pulled up when the corresponding PD4_j bit is set to 0 and the PU4_j bit is set to 1.
Do not set the corresponding PU4_j bit to 1 for the output pins for peripheral functions.

12.7.4 Open-Drain Control Register 4 (POD4)

Address 000C4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	POD4_7	POD4_6	POD4_5	—	—	POD4_2	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	POD4_2	Port P4_2 open-drain control bit	0: Not open-drain 1: Open-drain	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	POD4_5	Port P4_5 open-drain control bit	0: Not open-drain 1: Open-drain	R/W
b6	POD4_6	Port P4_6 open-drain control bit		R/W
b7	POD4_7	Port P4_7 open-drain control bit		R/W

The POD4 register is used to select whether the output type is CMOS output or N-channel open-drain output. These settings are enabled when the peripheral function output or output port function is selected.
The corresponding pins are set to N-channel open-drain output when the POD4_j bit (j = 2, or 5 to 7) is set to 1 (open-drain), and CMOS output when the bit is set to 0 (not open-drain).

12.7.5 Port 4 Function Mapping Register 0 (PML4)

Address 000CEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	P42SEL1	P42SEL0	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	P42SEL0	Port P4_2 function select bits	b5 b4 0 0: I/O port 0 1: TRBO 1 0: TXD0/IrTXD 1 1: $\overline{KI3}$	R/W
b5	P42SEL1			R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The PML4 register is used to select the P4_2 pin function.

12.7.6 Port 4 Function Mapping Register 1 (PMH4)

Address 000CFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P47SEL1	P47SEL0	P46SEL1	P46SEL0	P45SEL1	P45SEL0	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	P45SEL0	Port P4_5 function select bits	b3 b2 0 0: I/O port or XOUT output 0 1: $\overline{INT0}$ 1 0: $\overline{ADTRG}$ 1 1: Do not set.	R/W
b3	P45SEL1			R/W
b4	P46SEL0	Port P4_6 function select bits	b5 b4 0 0: I/O port or XCIN input 0 1: RXD0/IrRXD 1 0: TXD0/IrTXD 1 1: Do not set.	R/W
b5	P46SEL1			R/W
b6	P47SEL0	Port P4_7 function select bits	b7 b6 0 0: I/O port or XCOUT output 0 1: INT2 Other than the above: Do not set.	R/W
b7	P47SEL1			R/W

The PMH4 register is used to select the functions of pins P4_5 to P4_7.

12.7.7 Pin Settings for Port 4

Tables 12.28 to 12.31 list the pin settings for port 4.

Table 12.28 Port P4_2/TRBO/TXD0/IrTXD/$\overline{KI3}$

Register	PD4	PML4		Function
Bit	PD4_2	P42SEL		
		1	0	
Setting value	0	0	0	Input port
	1	0	0	Output port
	X	0	1	TRBO output
	X	1	0	TXD0/IrTXD output
	X	1	1	$\overline{INT3}$ input

X: 0 or 1

Table 12.29 Port P4_5/XOUT/$\overline{INT0}$/$\overline{ADTRG}$

Register	PD4	PMH4		EXCKCR		Function
Bit	PD4_5	P45SEL		CKPT		
		1	0	1	0	
Setting value	0	0	0	0	X	Input port
	1	0	0	0	X	Output port
	X	0	0	1	0	System clock (f) output
	X	0	0	1	1	XOUT output
	X	0	1	X	X	$\overline{INT0}$ input
	X	1	0	X	X	$\overline{ADTRG}$ input

X: 0 or 1

Table 12.30 Port P4_6/XCIN/RXD0/IrRXD/TXD0/IrTXD

Register	PD4	PMH4		EXCKCR		Function
Bit	PD4_6	P46SEL		CKPT		
		1	0	3	2	
Setting value	0	0	0	0	0	Input port
	1	0	0	0	0	Output port
	X	0	0	0	1	XCIN clock input (external clock input)
	X	0	0	1	0	XCIN input
	X	0	1	X	X	RXD0/IrRXD input
	X	1	0	X	X	TXD0/IrTXD output

X: 0 or 1

Table 12.31 Port P4_7/XCOUT/$\overline{INT2}$

Register	PD4	PMH4		EXCKCR		Function
Bit	PD4_7	P47SEL		CKPT		
		1	0	3	2	
Setting value	0	0	0	0	X	Input port
	1	0	0	0	X	Output port
	X	0	0	1	0	XCOUT output
	X	0	1	X	X	$\overline{INT2}$ input

X: 0 or 1

12.8 Port A

Figure 12.6 shows the Port A Pin Configuration.

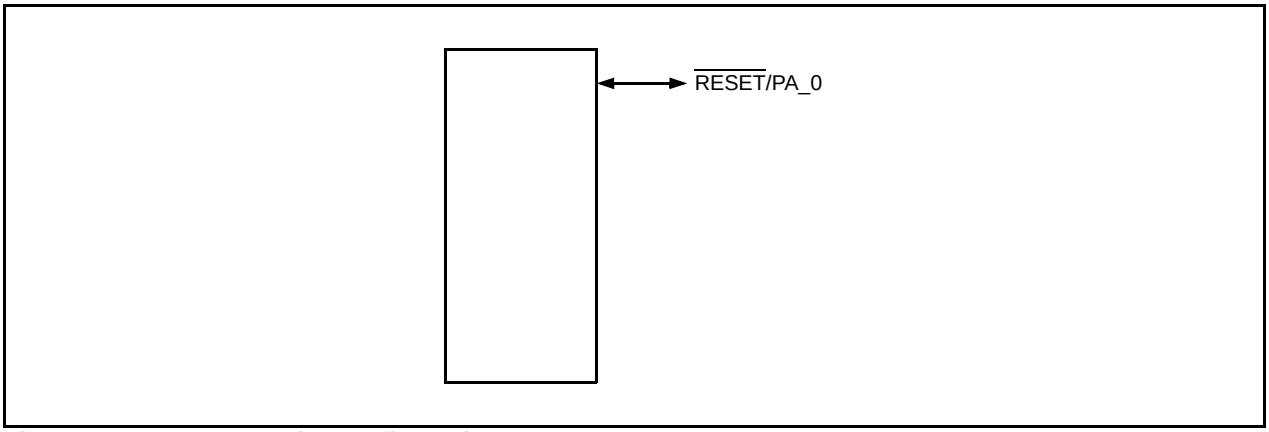


Figure 12.6 Port A Pin Configuration

12.8.1 Port PA Direction Register (PDA)

Address 000ADh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	PDA_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PDA_0	Port PA_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The PDA register is used to select whether PA_0 is used as input or output.

12.8.2 Port PA Register (PA)

Address 000B3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	PA_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PA_0	Port PA_0 bit	0: Low level 1: High level	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The PA register is an I/O port data register. Data input to and output from external devices are accomplished by reading from and writing to the PA register. The PA register consists of a port latch to retain output data and a circuit to read the pin states. The value written to the port latch is output from the pin.

12.8.3 Port PA Mode Control Register (PAMCR)

Address 000C5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	HWRSTE	—	—	—	PODA_0
After Reset	0	0	0	1	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	PODA_0	Port PA_0 open-drain control bit (1)	0: Not open-drain 1: Open-drain	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	HWRSTE	Hardware reset enabled bit	0: Port PA_0 functions as an I/O port 1: Port PA_0 functions as a hardware reset ($\overline{\text{RESET}}$)	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	—			

Note:
1. Setting this bit to 1 (open-drain) enables N-channel open-drain output and setting this bit to 0 (not open-drain) enables CMOS output.

The PAMCR register is used to control the port PA open-drain and the port A function. The open-drain is enabled when the peripheral function or output port function is selected.
Set the PAMCRE bit in the HRPR register to 1 (write enabled) before rewriting the PAMCR register.

12.8.4 Pin Setting for Port A

Table 12.32 lists the pin setting for port A.

Table 12.32 $\overline{\text{RESET}}$/Port PA_0

Register	PDA	PAMCR	Function
Bit	PDA_0	HWRSTE	
Setting value	X	1	$\overline{\text{RESET}}$
	0	0	Input port (1)
	1	0	Output port (2)

X: 0 or 1
Notes:
1. Connect a pull-up resistor. For details, see **12.13.1 Notes on $\overline{\text{RESET}}$/PA_0 Pin**.
2. Setting the PODA_0 bit to 1 enables N-channel open-drain output.

12.9 Procedure for Setting Peripheral Functions Associated with Ports 0 to 4

After a reset, use the following procedure to set the peripheral functions associated with ports 0 to 4.

(1) Set the function mapping registers for ports 0 to 4.
(2) Set the operating mode for the peripheral functions.
(3) Start operation of the peripheral functions.

12.10 Pin Settings for Peripheral Function I/O

Tables 12.33 to 12.36 list the pin settings for peripheral function I/O.

Table 12.33 TRCIOA Pin Settings

Register	TRCOER	TRCMR	TRCIOR0			TRCCR2		Function
Bit	EA	PWM2	IOA2	IOA1	IOA0	TCEG1	TCEG0	
Setting value	0	1	0	0	1	X	X	Timer mode waveform output (output compare function)
				1	X			
	0	1	1	X	X	X	X	Timer mode (input capture function)
	1							
	1	0	X	X	X	0	1	PWM2 mode (TRCTRG input)
						1	X	

X: 0 or 1

Table 12.34 TRCIOB Pin Settings

Register	TRCOER	TRCMR		TRCIOR0			Function
Bit	EB	PWM2	PWMB	IOB2	IOB1	IOB0	
Setting value	0	0	X	X	X	X	PWM2 mode waveform output
	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 12.35 TRCIOC Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	EC	PWM2	PWMC	IOC2	IOC1	IOC0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 12.36 TRCIOD Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	ED	PWM2	PWMD	IOD2	IOD1	IOD0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

12.11 Handling of Unused Pins

Table 12.37 lists the Handling of Unused Pins. Figure 12.7 shows the Handling of Unused Pins.

Table 12.37 Handling of Unused Pins

Pin Name	Connection
Ports P0, P1, P2_0 to P2_2, P3_1, P3_3 to P3_5, P3_7, P4_2, P4_5 to 4_7	• Set each of these pins to input mode and connect the pin to VSS through a resistor (pull-down) or connect it to VCC through a resistor (pull-up). (2) • Set each of these pins to output mode and leave it open. (2, 3)
$\overline{\text{RESET}}$/PA_0 (1)	Connect to VCC through a pull-up resistor. (2)

Notes:
1. When the power-on reset is used.
2. Use lines that are as short as possible (2 cm or shorter) to handle unused pins in the vicinity of the MCU.
3. When these ports are set to output mode and left open, keep the following in mind. They remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be unstable and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. The program should periodically reconfigure the content for enhanced reliability.

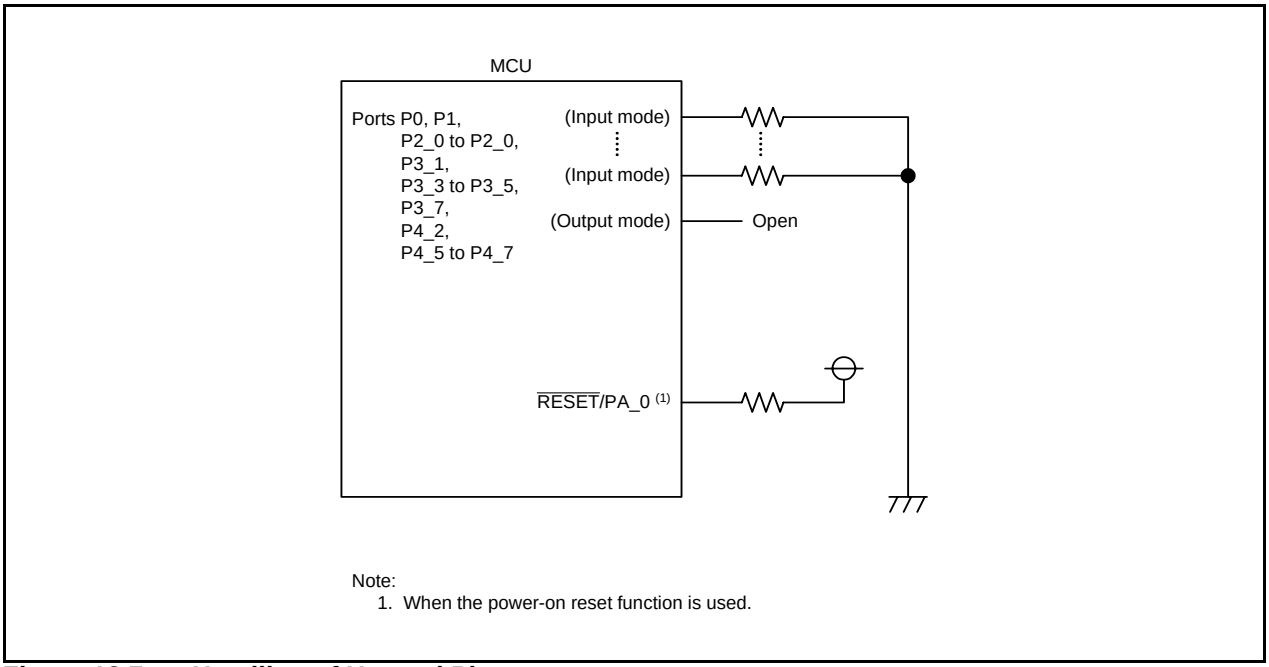


Figure 12.7 Handling of Unused Pins

12.12 I/O Port Configuration

Figures 12.8 to 12.22 show the I/O Port Configuration. Figure 12.23 shows the Pin Configuration.

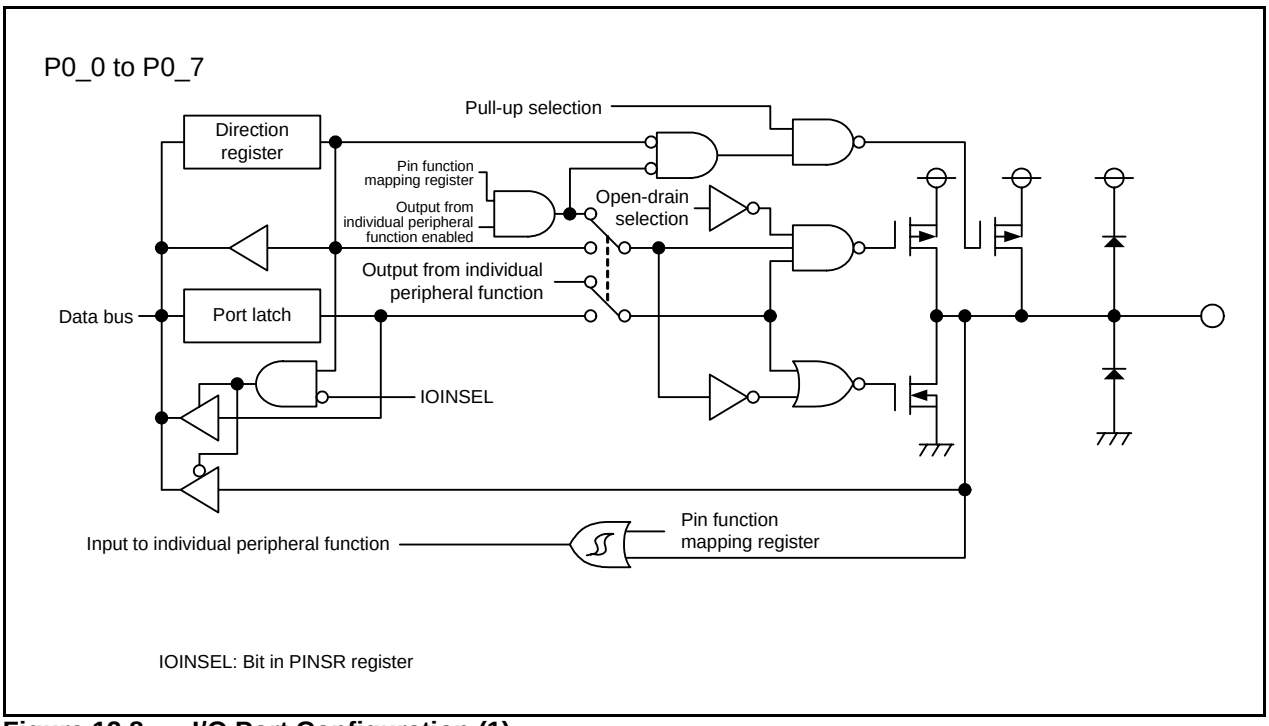


Figure 12.8 I/O Port Configuration (1)

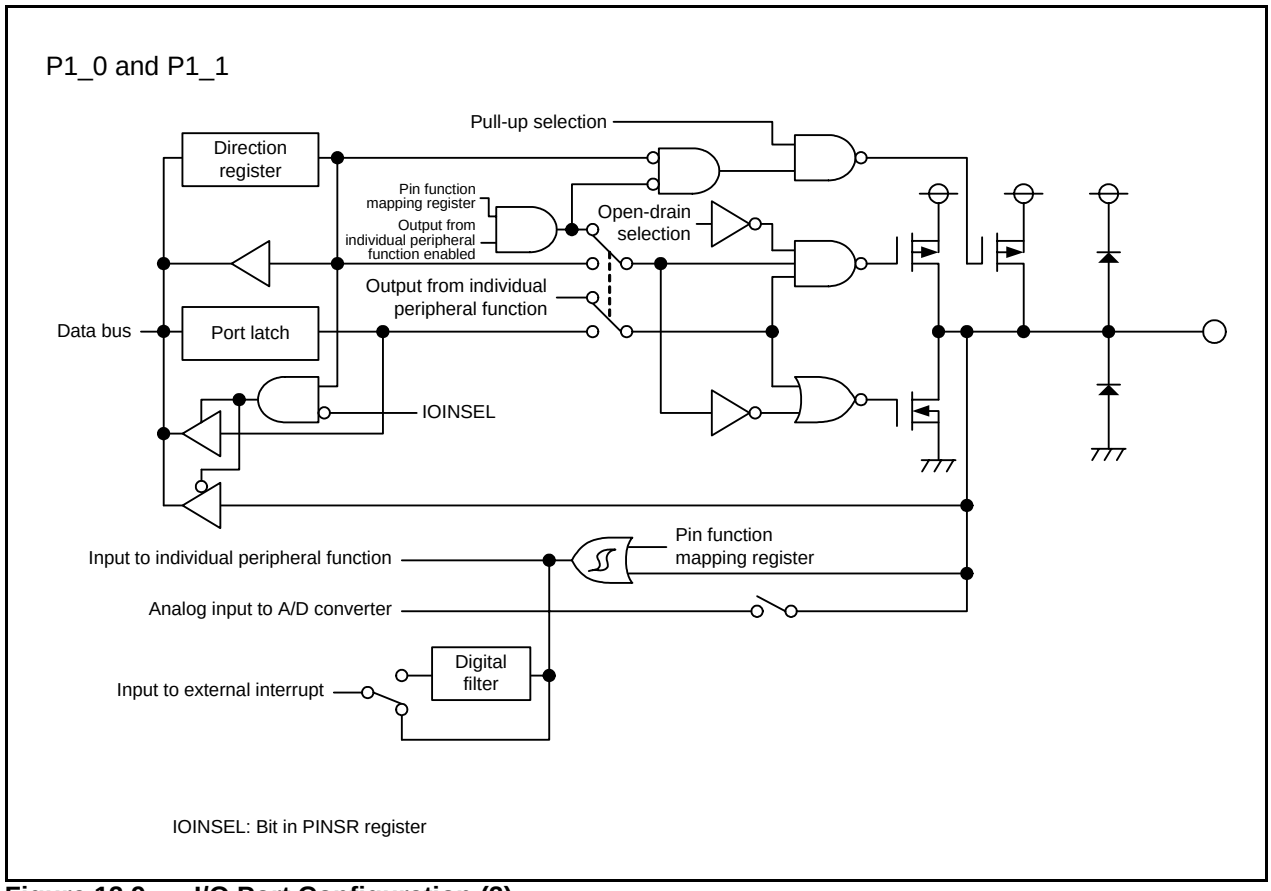


Figure 12.9 I/O Port Configuration (2)

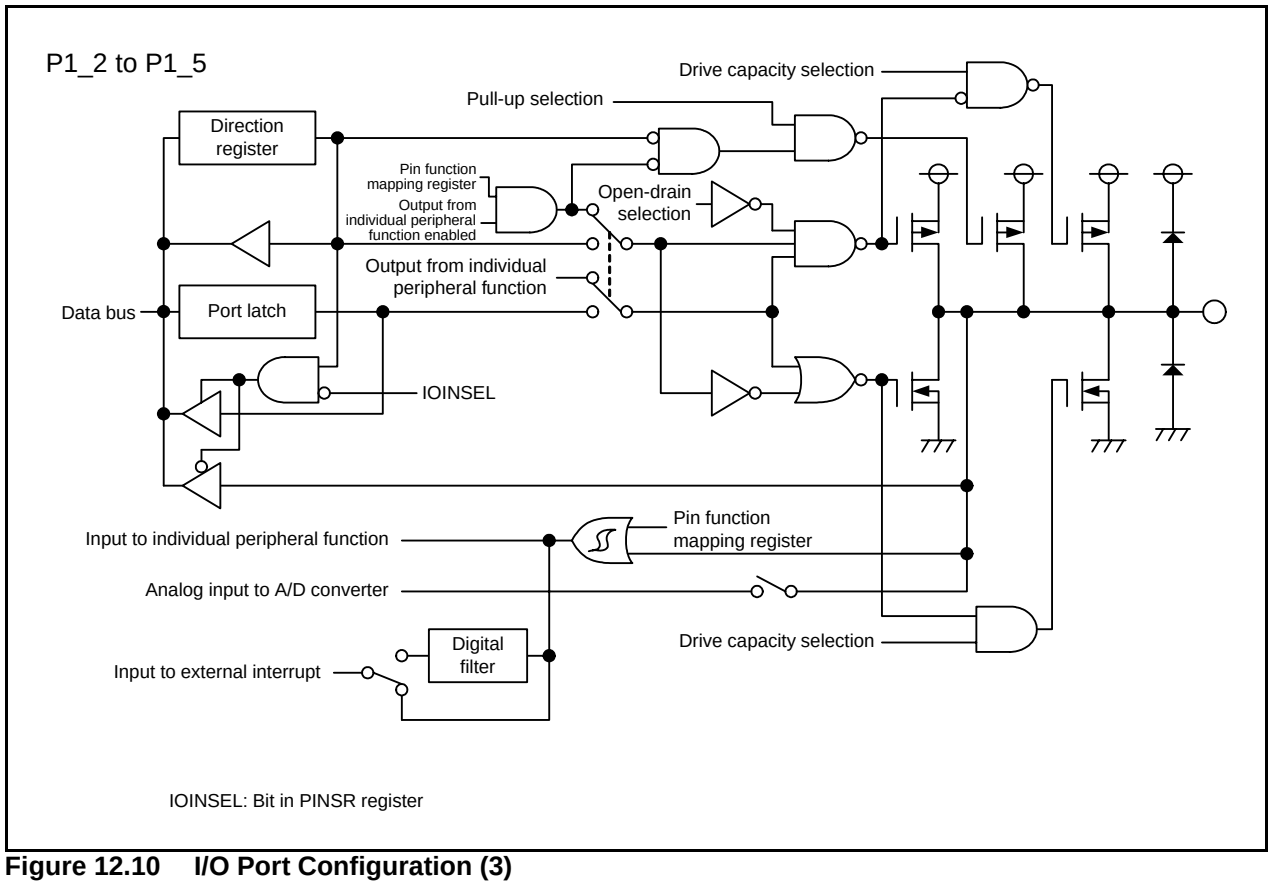


Figure 12.10 I/O Port Configuration (3)

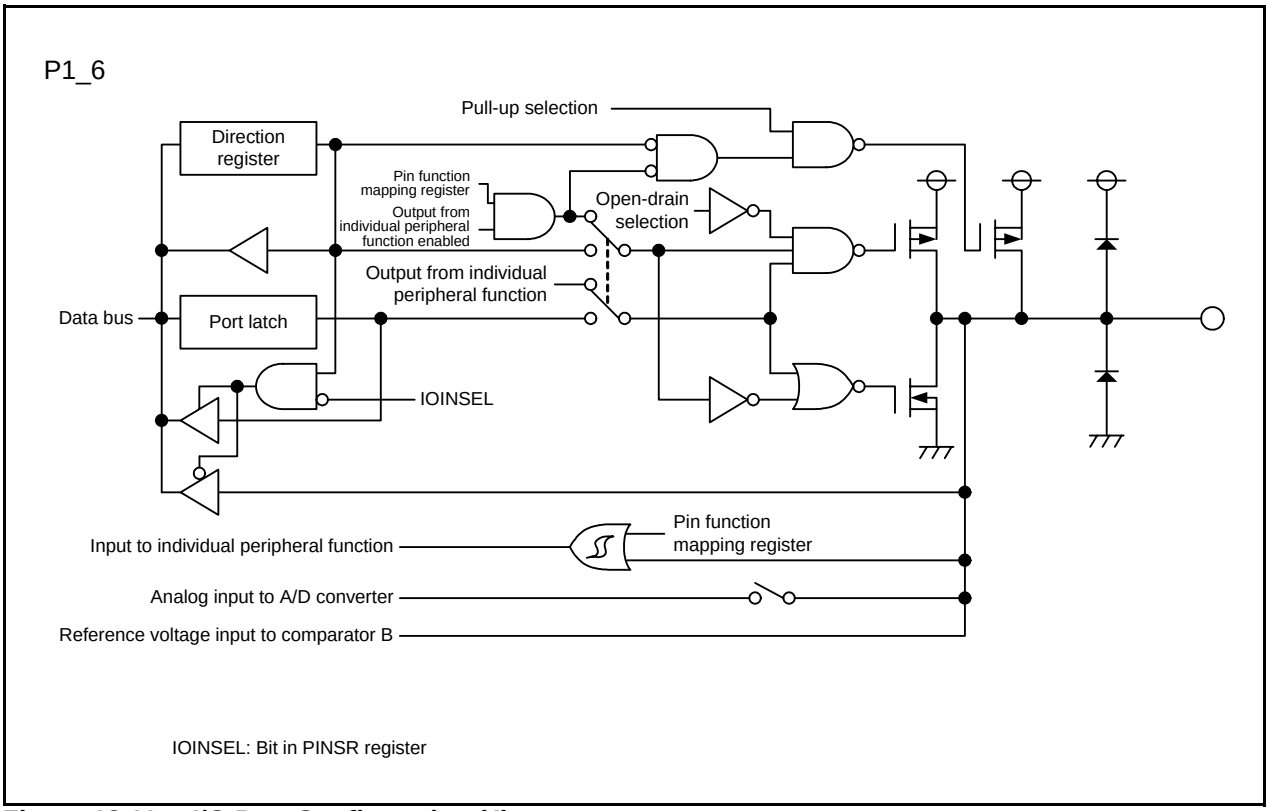


Figure 12.11 I/O Port Configuration (4)

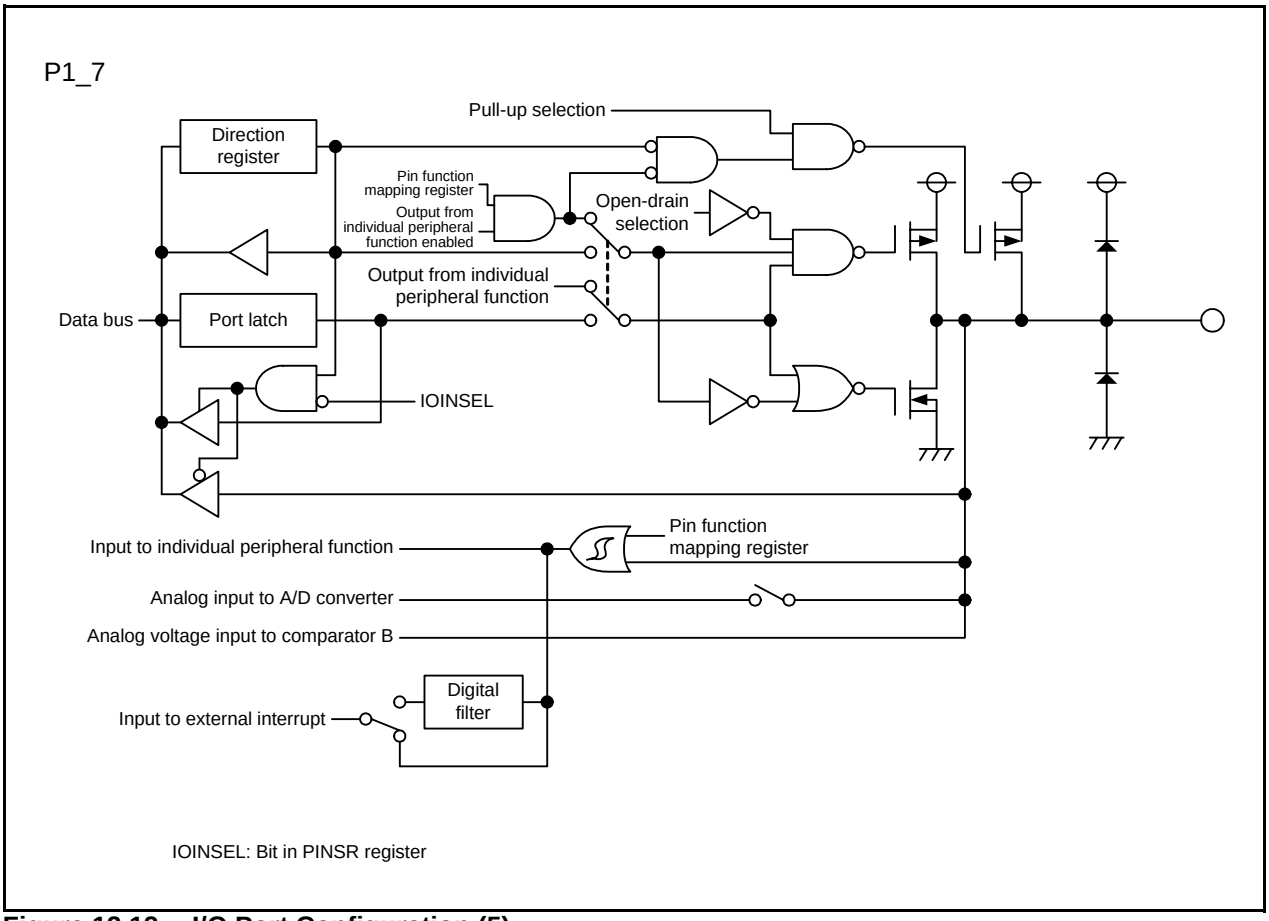


Figure 12.12 I/O Port Configuration (5)

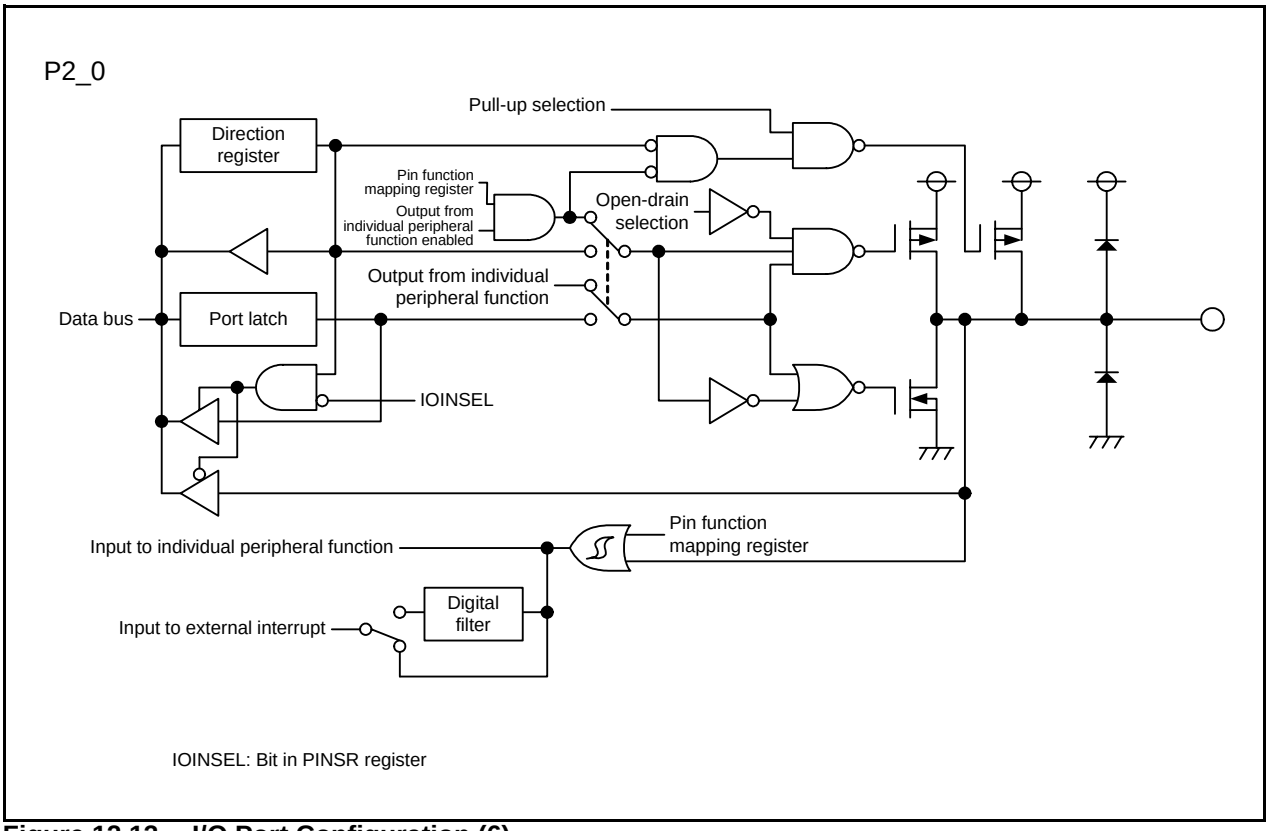


Figure 12.13 I/O Port Configuration (6)

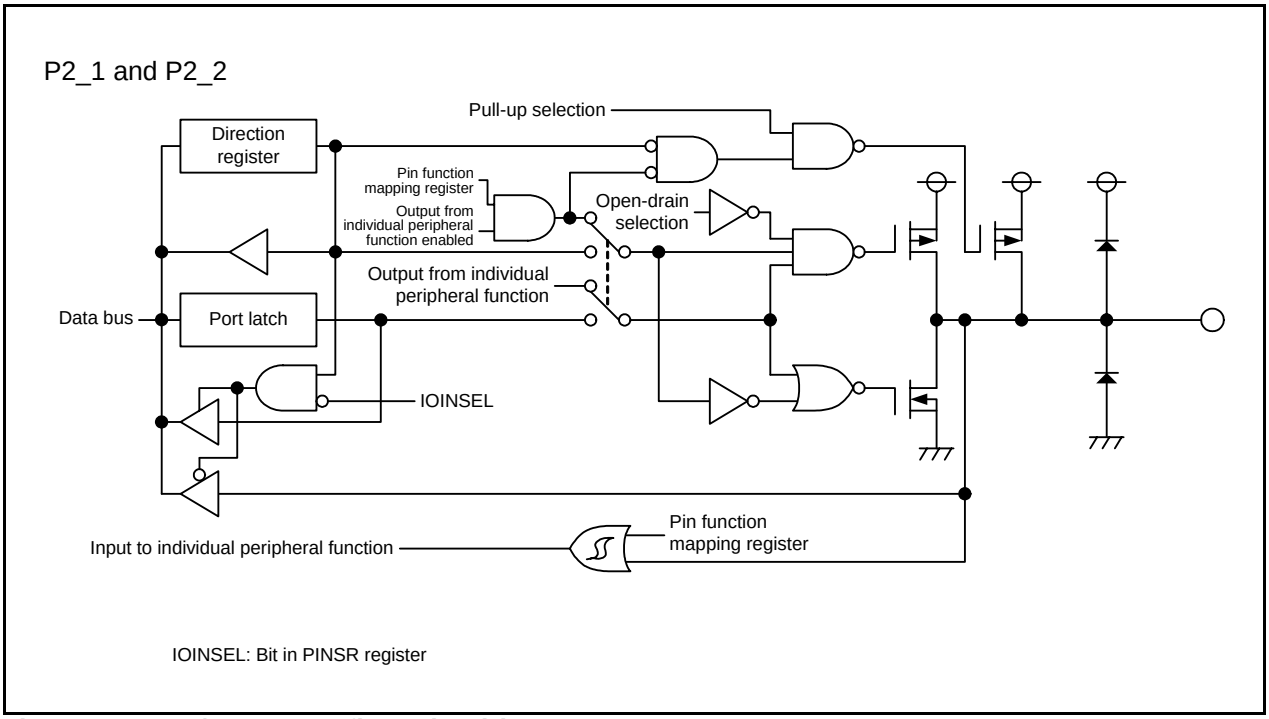


Figure 12.14 I/O Port Configuration (7)

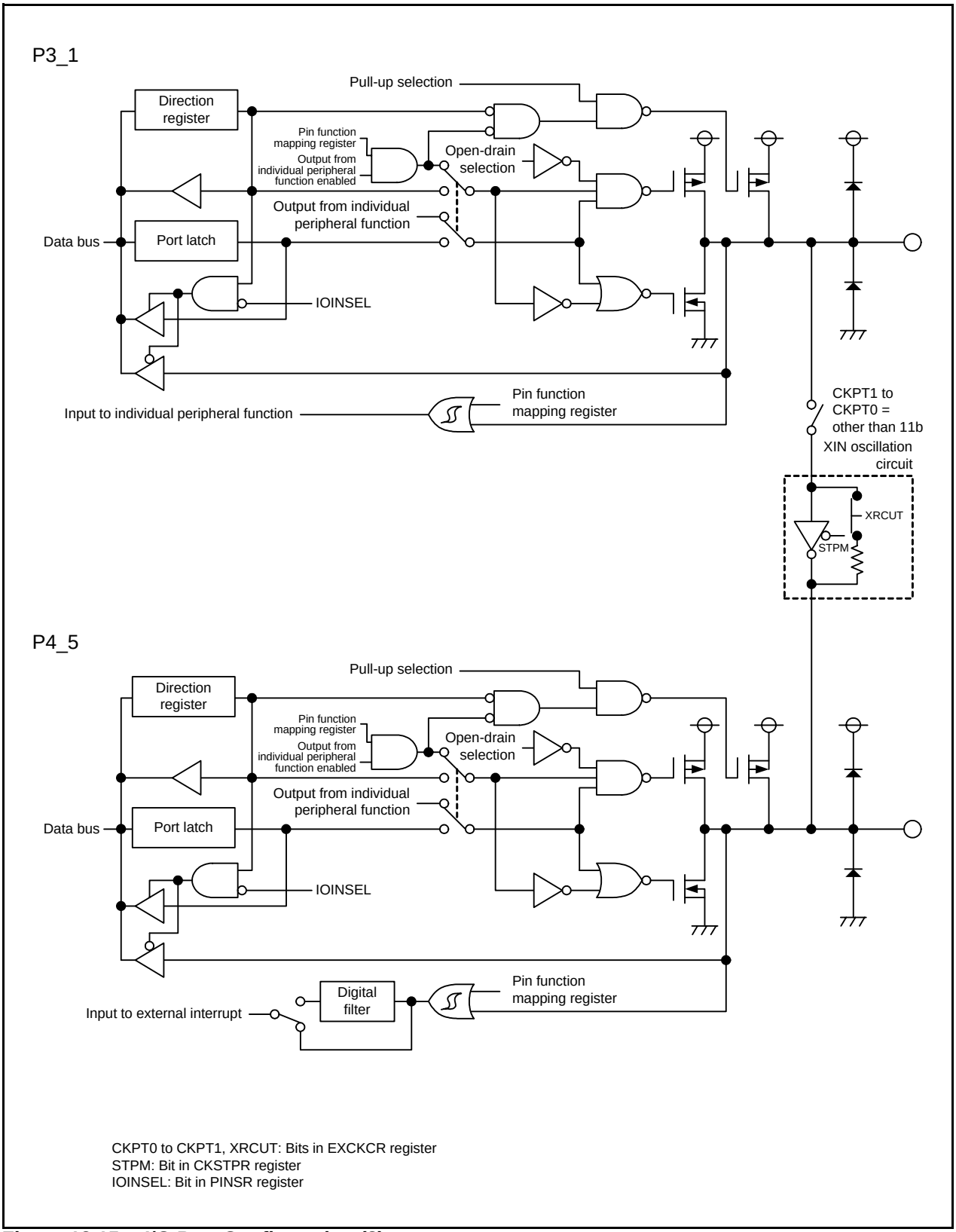


Figure 12.15 I/O Port Configuration (8)

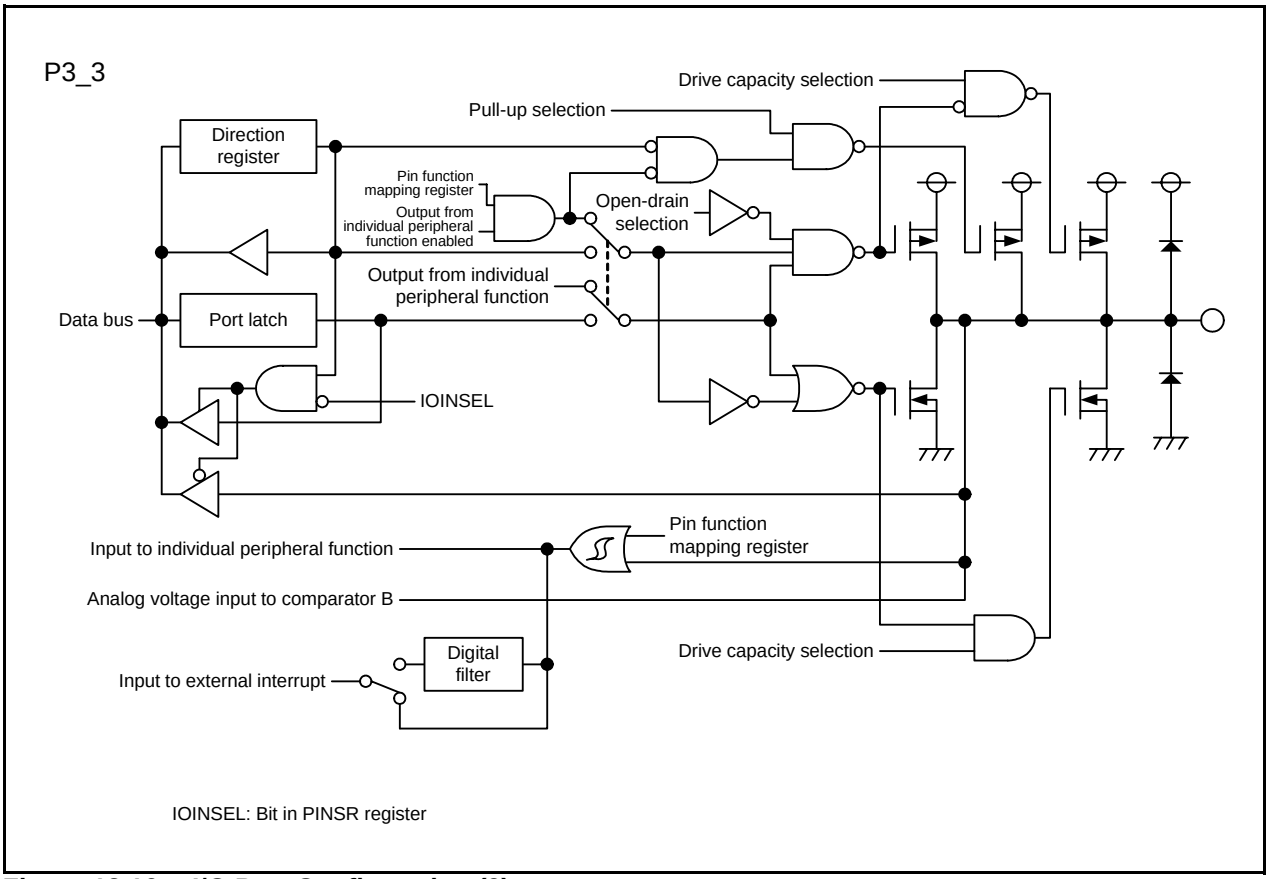


Figure 12.16 I/O Port Configuration (9)

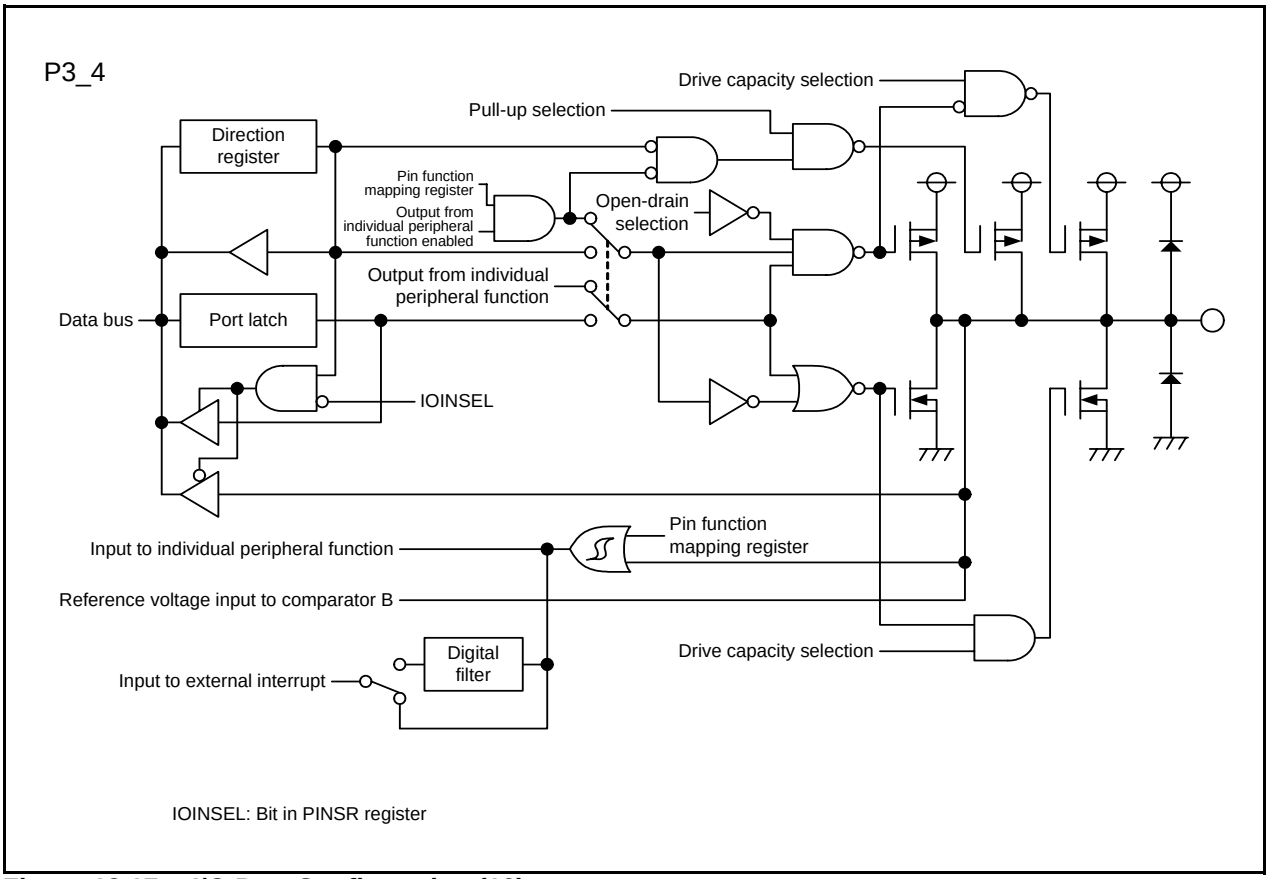


Figure 12.17 I/O Port Configuration (10)

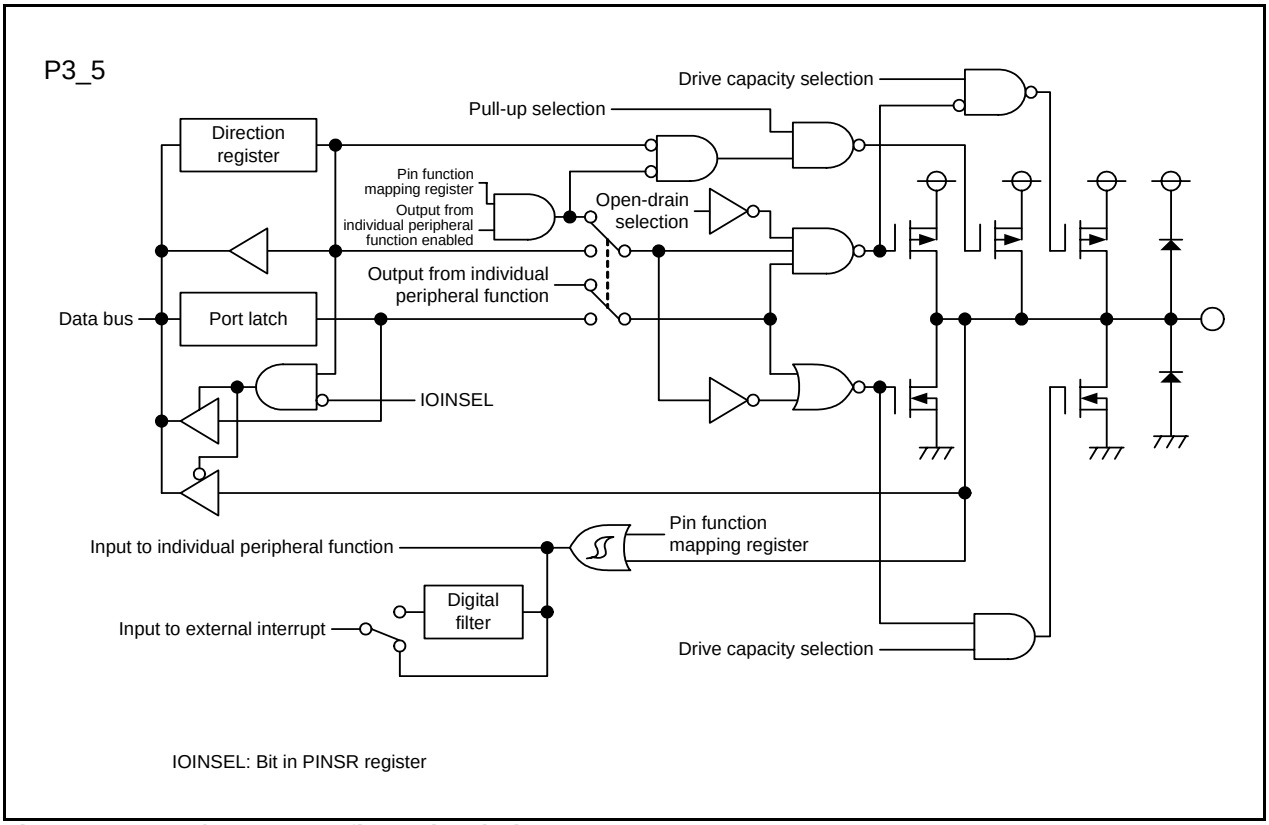


Figure 12.18 I/O Port Configuration (11)

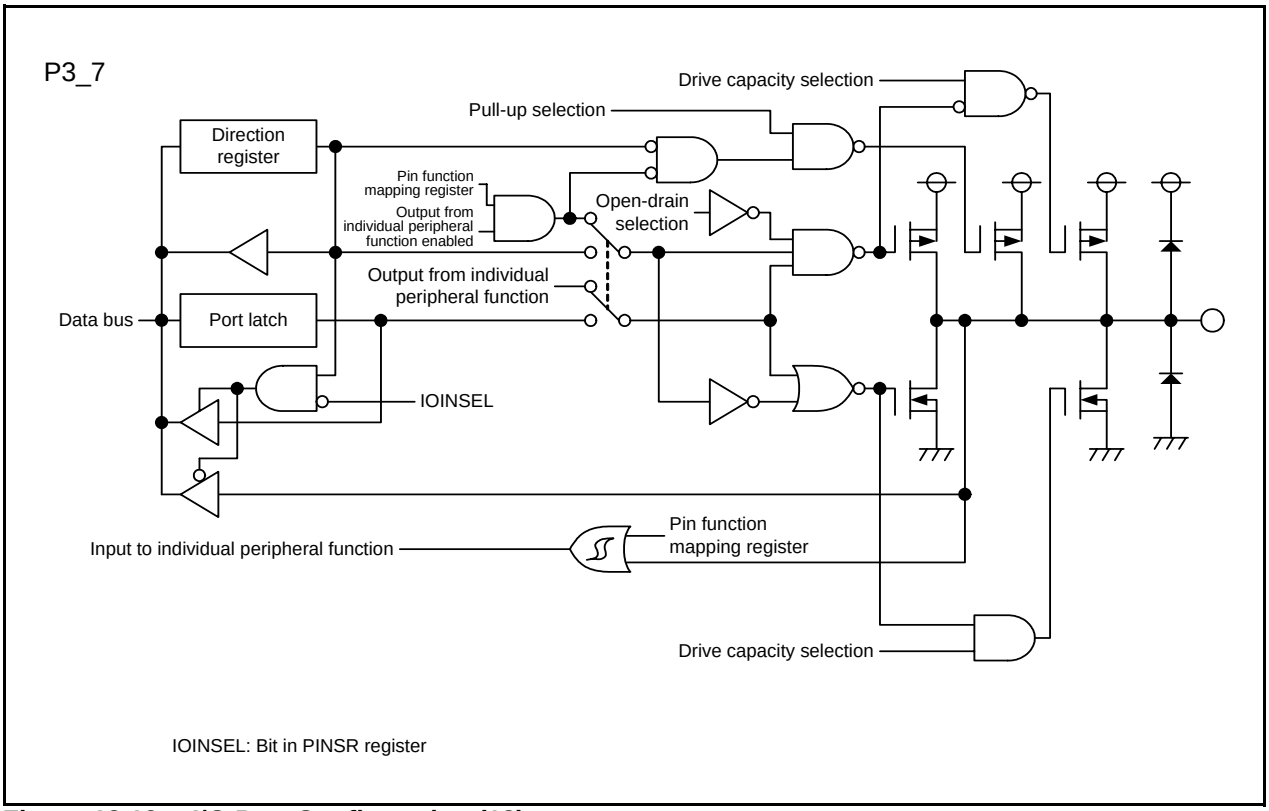


Figure 12.19 I/O Port Configuration (12)

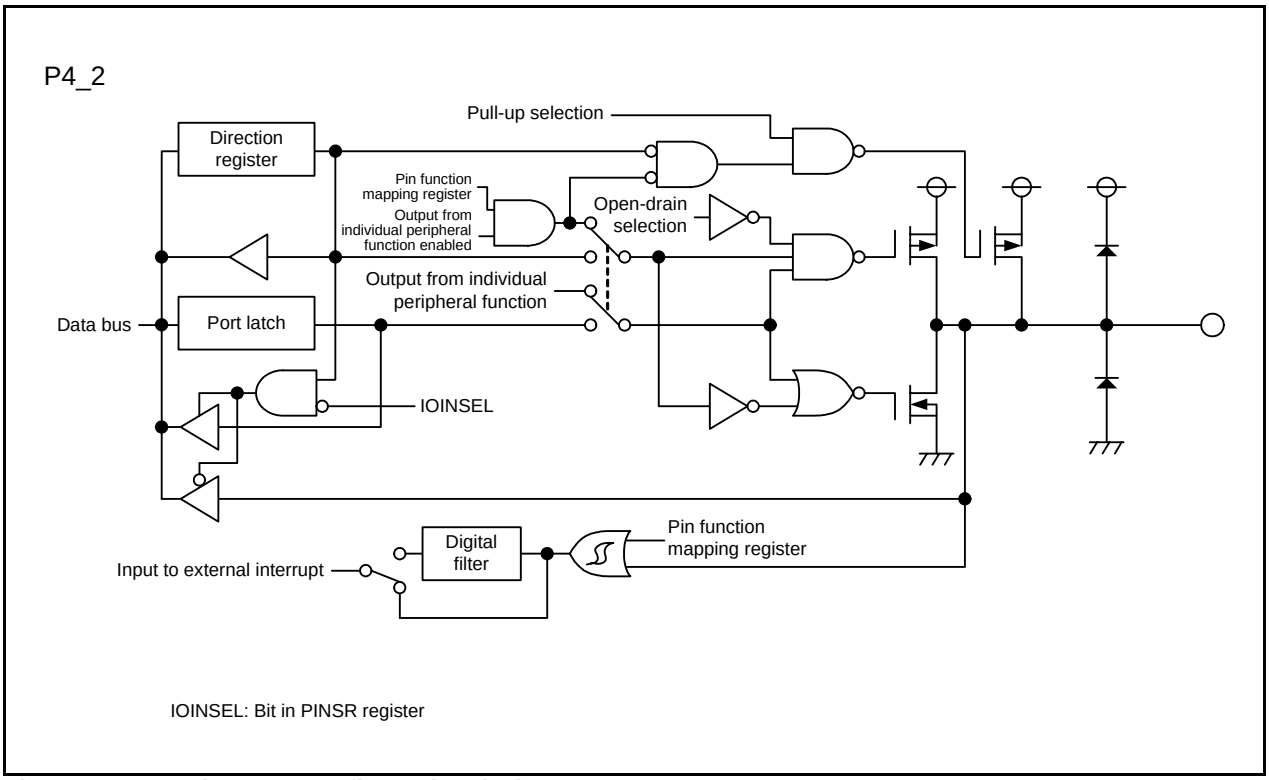
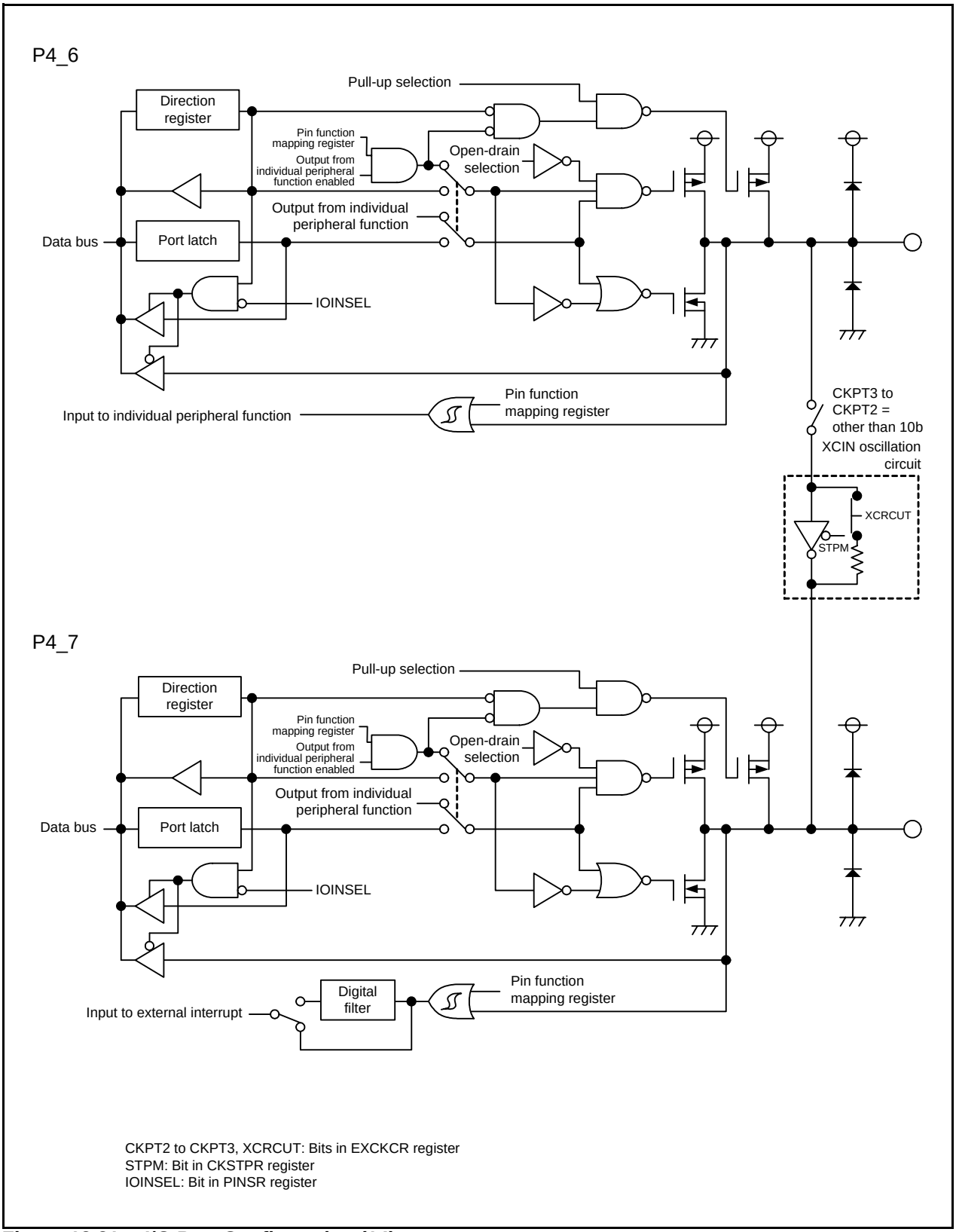


Figure 12.20 I/O Port Configuration (13)



CKPT2 to CKPT3, XCRCUT: Bits in EXCKCR register
STPM: Bit in CKSTPR register
IOINSEL: Bit in PINSR register

Figure 12.21 I/O Port Configuration (14)

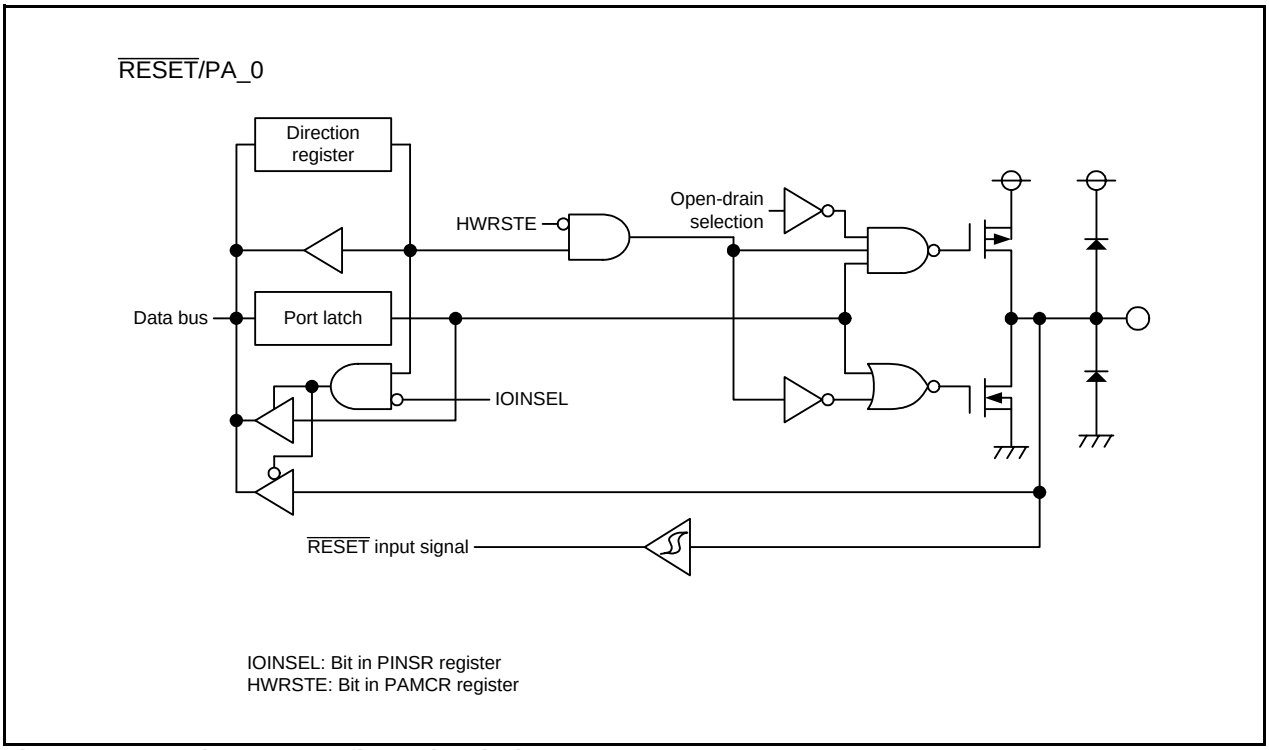


Figure 12.22 I/O Port Configuration (15)

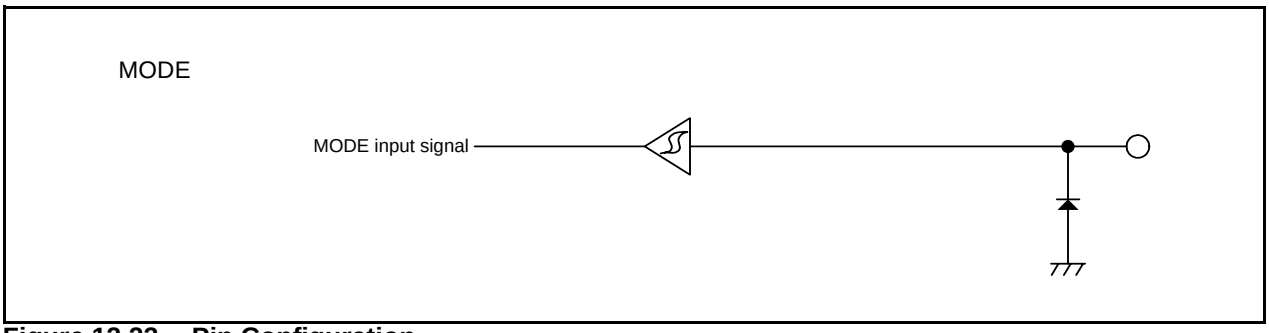


Figure 12.23 Pin Configuration

12.13 Notes on I/O Ports

12.13.1 Notes on $\overline{\text{RESET}}$/PA_0 Pin

The $\overline{\text{RESET}}$/PA_0 pin is multiplexed with the hardware reset function ($\overline{\text{RESET}}$), and this pin functions as the $\overline{\text{RESET}}$ pin when a reset is cleared. After the reset is cleared, the $\overline{\text{RESET}}$/PA_0 pin functions as the I/O port (PA_0) when the HWRSTE bit in the PAMCR register is set to 0. In this case, an external pull-up resistor must be connected.
This pin can also be used as CMOS output when it is set as an output port, but be sure not to conflict with an external reset input signal.
Refer to the following program example to use this pin as N-channel open-drain output as necessary.

• Program example to set PA_0 as an N-channel open-drain output port

```
FCLR    I
BCLR    0, HRPR
BSET    0, HRPR          ; Writing to the PAMCR register enabled
FSET    I
BSET    0, PAMCR         ; Port PA_0 function selected, N-channel open-drain output
                           selected
BSET    0, PDA           ; Output mode setting
```

12.13.2 I/O Pins for Peripheral Functions

In this MCU, the pin assignment of the peripheral functions can be changed using the port function mapping register. However, multiple pins must not be assigned to the same peripheral function input at the same time. Otherwise, no signal can be input correctly.

13. Timer RJ2

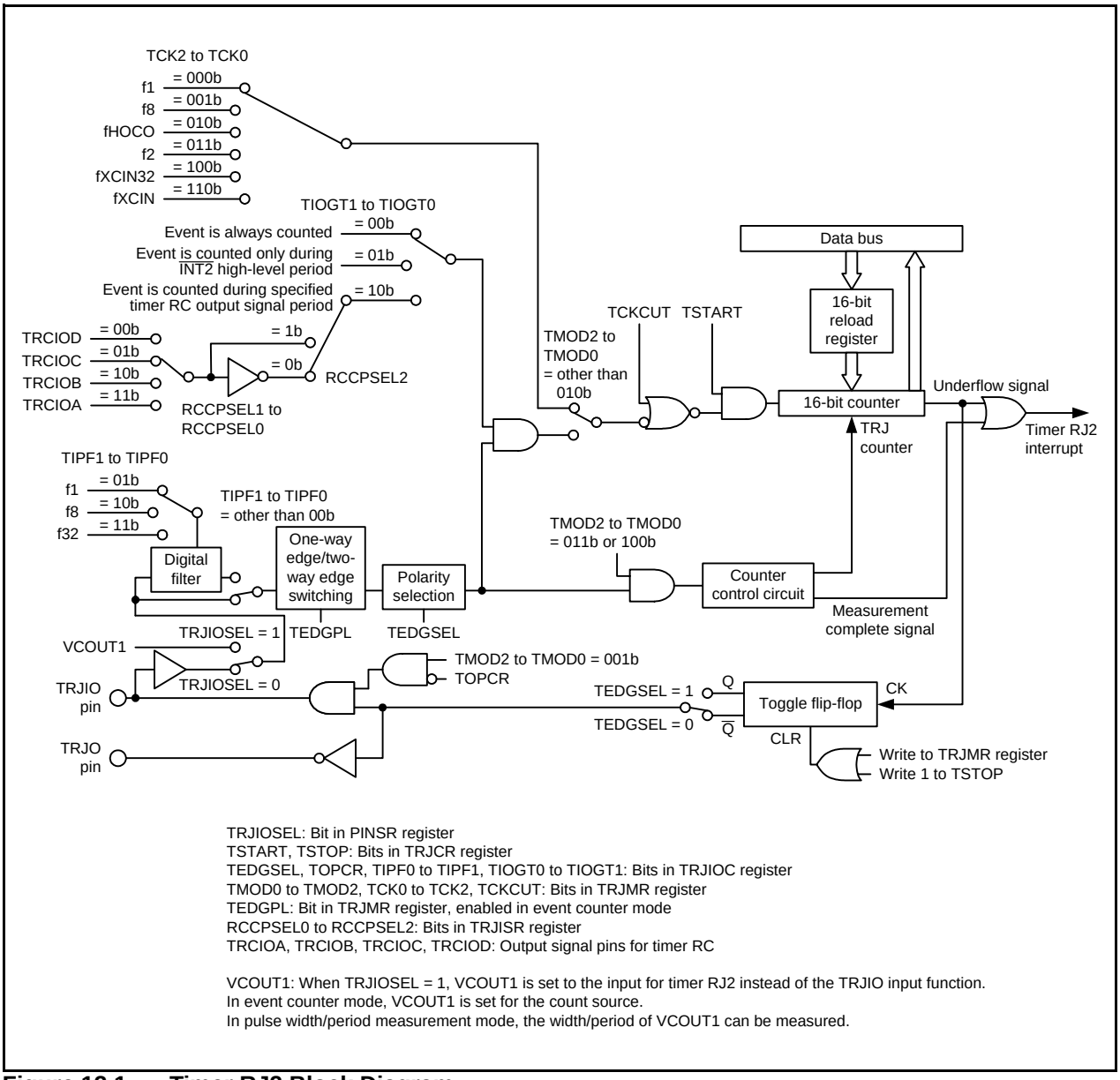
Timer RJ2 is a 16-bit timer that can be used for pulse output, external input pulse width or period measurement, and counting an internal source or external pulse. This timer consists of a reload register and down counter which are allocated to the same address.

13.1 Overview

Table 13.1 lists the Timer RJ2 Specifications. Figure 13.1 shows the Timer RJ2 Block Diagram.

Table 13.1 Timer RJ2 Specifications

Item		Description
Operating modes	Timer mode	The internal count source is counted.
	Pulse output mode	The internal count source is counted and the output is inverted at each underflow of the timer.
	Event counter mode	An external pulse is counted.
	Pulse width measurement mode	An external pulse width is measured.
	Pulse period measurement mode	An external pulse period is measured.
Count source		f1, f2, f8, fHOCO, fXCIN, fXCIN32, or external pulse selectable.
Interrupt		• When the counter underflows. • When the measurement of the active width of the external input (TRJIO) is completed in pulse width measurement mode. • When the set edge of the external input (TRJIO) is input in pulse period measurement mode.



TRJIOSEL: Bit in PINSR register
TSTART, TSTOP: Bits in TRJCR register
TEDGSEL, TOPCR, TIPF0 to TIPF1, TIOGT0 to TIOGT1: Bits in TRJIOC register
TMOD0 to TMOD2, TCK0 to TCK2, TCKCUT: Bits in TRJMR register
TEDGPL: Bit in TRJMR register, enabled in event counter mode
RCCPSEL0 to RCCPSEL2: Bits in TRJISR register
TRCIOA, TRCIOB, TRCIOC, TRCIOD: Output signal pins for timer RC

VCOUT1: When TRJIOSEL = 1, VCOUT1 is set to the input for timer RJ2 instead of the TRJIO input function.
In event counter mode, VCOUT1 is set for the count source.
In pulse width/period measurement mode, the width/period of VCOUT1 can be measured.

Figure 13.1 Timer RJ2 Block Diagram

13.2 I/O Pins

Table 13.2 lists the Timer RJ2 Pin Configuration.

Table 13.2 Timer RJ2 Pin Configuration

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT2}}$	P3_4, P4_7	I	Event counter mode count control
TRJIO (1)	P1_5, P1_7	I/O	External pulse input and pulse output for timer RJ2
TRJO (1)	P1_6, P3_7	O	Pulse output for timer RJ2

Note:
1. When a pulse is output from TRJIO and TRJO simultaneously, TRJIO is set to the inverted output of TRJO.

13.3 Registers

Table 13.3 lists the Timer RJ2 Register Configuration.

Table 13.3 Timer RJ2 Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RJ Counter Register	TRJ	FFh	000D8h	16
		FFh	000D9h	
Timer RJ Control Register	TRJCR	00h	000DAh	8
Timer RJ I/O Control Register	TRJIOC	00h	000DBh	8
Timer RJ Mode Register	TRJMR	00h	000DCh	8
Timer RJ Event Select Register	TRJISR	00h	000DDh	8
Timer RJ Interrupt Control Register	TRJIR	00h	000DEh	8

13.3.1 Timer RJ Counter Register (TRJ), Timer RJ Reload Register

Address 000D8h to 000D9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	Setting Range	R/W
b15 to b0	—	16-bit counter and reload register (1, 2, 3)	0000h to FFFFh	R/W

Notes:
1. When 1 is written to the TSTOP bit in the TRJCR register, the 16-bit counter is forcibly stopped and set to FFFFh.
2. The TRJ register must be accessed in 16-bit units. Do not access this register in 8-bit units. When this register is accessed as 16-bit units, it is accessed twice in 8-bit units.
3. Do not set the TRJ register to 0000h in pulse width measurement mode and pulse period measurement mode.

TRJ is a 16-bit register. The write value is written to the reload register and the read value is read from the counter.
The states of the reload register and the counter are changed depending on the TSTART bit in the TRJCR register. For details, see **13.4.1 Reload Register and Counter Rewrite Operation**.

13.3.2 Timer RJ Control Register (TRJCR)

Address 000DAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RJ count start bit (1)	0: Count is stopped 1: Count is started	R/W
b1	TCSTF	Timer RJ count status flag (1)	0: Count is stopped 1: Count is in progress	R
b2	TSTOP	Timer RJ count forced stop bit (2)	When 1 is written to this bit, the count is forcibly stopped. The read value is 0.	W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	TEDGF	Active edge judgement flag	0: No active edge received 1: Active edge received	R/W
b5	TUNDF	Timer RJ underflow flag	0: No underflow 1: Underflow	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

Notes:
1. For notes on using bits TSTART and TCSTF, see **13.5 Notes on Timer RJ2 (2)**.
2. When 1 (count is forcibly stopped) is written to the TSTOP bit, the counter, the TRJ register, and bits TSTART and TCSTF are initialized at the same time. The pulse output level is also initialized.

Use the MOV instruction to set the TRJCR register in pulse width measurement mode and pulse period measurement mode. To avoid changing TEDGF and TUNDF at this time, write 1 to these bits.

TSTART Bit (Timer RJ count start bit)

Count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When the TSTART bit is set to 1 (count is started), the TCSTF bit is set to 1 (count is in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF bit is set to 0 (count is stopped) in synchronization with the count source. For details, see **13.5 Notes on Timer RJ2 (2)**.

TCSTF Bit (Timer RJ count status flag)

[Conditions for setting to 0]
- When 0 is written to the TSTART bit (the TCSTF bit is set to 0 in synchronization with the count source).
- When 1 is written to the TSTOP bit.

[Condition for setting to 1]
- When 1 is written to the TSTART bit (the TCSTF bit is set to 1 in synchronization with the count source).

TEDGF Bit (Active edge judgement flag)

[Condition for setting to 0]
- When 0 is written to this bit by a program.

[Conditions for setting to 1]
- When the measurement of the active width of the external input (TRJIO) is completed in pulse width measurement mode.
- The set edge of the external input (TRJIO) is input in pulse period measurement mode.

TUNDF Bit (Timer RJ underflow flag)

[Condition for setting to 0]
- When 0 is written to this bit by a program.

[Condition for setting to 1]
- When the counter underflows.

13.3.3 Timer RJ I/O Control Register (TRJIOC)

Address 000DBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	—	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	I/O polarity switch bit	Function varies depending on the operating mode.	R/W
b1	TOPCR	TRJIO output control bit	0: TRJIO output enabled (toggle output is started) 1: TRJIO output disabled (toggle output is stopped)	R/W
b2	—	Reserved	Set to 0.	R/W
b3	—			
b4	TIPF0	TRJIO input filter select bits	b5 b4 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRJIO count control bits	b7 b6 0 0: Event is always counted 0 1: Event is counted only during $\overline{\text{INT2}}$ high-level period 1 0: Event is counted during timer RC output signal period specified by RCCPSEL bit in TRJISR register 1 1: Do not set.	R/W
b7	TIOGT1			R/W

TEDGSEL Bit (I/O polarity switch bit)

The TEDGSEL bit is used to switch the TRJO output polarity and the TRJIO I/O edge and polarity. In pulse output mode, only the inversion/non-inversion of toggle flip-flop is controlled. The toggle flip-flop is initialized when the TRJMR register is written or 1 is written to the TSTOP bit in the TRJCR register.

Table 13.4 TRJIO I/O Edge and Polarity Switching

Operating Mode	Function
Pulse output mode	0: Output is started at high 1: Output is started at low
Event counter mode	0: Count on rising edge 1: Count on falling edge
Pulse width measurement mode	0: Low-level width is measured 1: High-level width is measured
Pulse period measurement mode	0: Measure from one rising edge to the next rising edge 1: Measure from one falling edge to the next falling edge

Table 13.5 TRJO Output Polarity Switching

Operating Mode	Function
All modes	0: Output is started at low 1: Output is started at high

TOPCR Bit (TRJIO output control bit)

The TOPCR bit is enabled only in pulse output mode. When this bit is set to 0, output is toggled. When it is set to 1, output is disabled and the port selected as the TRJIO function becomes high impedance.
In other operating modes, the functions listed in Table 13.6 are supported regardless of the setting of the TOPCR bit.

Table 13.6 TRJIO Pin Function

Operating Mode	Function
Timer mode	Not used
Event counter mode	Event input (count source input)
Pulse width measurement mode	Input for pulse width measurement
Pulse period measurement mode	Input for pulse period measurement

Bits TIPF0 to TIPF1 (TRJIO input filter select bits)

These bits are used to specify the sampling frequency of the filter for the TRJIO input. If the input to the TRJIO pin is sampled and the value matches three successive times, that value is taken as the input value.

Bits TIOGT0 to TIOGT1 (TRJIO count control bits)

These bits are enabled only in event counter mode.
They are used to select the period to count an event input from the TRJIO pin.
When bits TIOGT1 to TIOGT0 are set to 00b, an event is always counted.
When bits TIOGT1 to TIOGT0 are set to 01b, an event is counted while the $\overline{\text{INT2}}$ pin is held high.
When bits TIOGT1 to TIOGT0 are set to 10b, an event is counted for the period corresponding to the timer RC output set by the TRJISR register. Bits RCCPSEL0 to RCCPSEL1 in the TRJISR register are used to select the timer RC output signal and the RCCPSEL2 bit is used to select the level of the timer RC output signal.

13.3.4 Timer RJ Mode Register (TRJMR)

Address 000DCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	TEDGPL	TMOD2	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RJ operating mode select bits	b2 b1 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode Other than the above: Do not set.	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b3	TEDGPL	TRJIO edge polarity select bit	0: One-way edge 1: Two-way edge	R/W
b4	TCK0	Timer RJ count source select bits (1, 2)	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: fHOCO 0 1 1: f2 1 0 0: fXCIN32 1 1 0: fXCIN Other than the above: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RJ count source cutoff bit (2)	0: Count source is supplied 1: Count source is cut off	R/W

Notes:
1. When event counter mode is selected, the external input (TRJIO) is selected as the count source regardless of the setting of bits TCK0 to TCK2.
2. Do not switch or cut off the count source during count operation. When switching or cutting off the count source, set the TSTART bit in the TRJCR register to 0 (count is stopped) and the TCSTF bit to 0 (count is stopped) to stop the timer count.

Select the operating mode when the count is stopped (the TSTART bit is 0 and the TCSTF bit is 0).
When a value is written to the TRJMR register, the toggle flip-flop is initialized.

13.3.5 Timer RJ Event Select Register (TRJISR)

Address 000DDh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	RCCPSEL2	RCCPSEL1	RCCPSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RCCPSEL0	Timer RC output signal select bits	b1 b0 0 0: TRCIOD 0 1: TRCIOC 1 0: TRCIOB 1 1: TRCIOA	R/W
b1	RCCPSEL1			R/W
b2	RCCPSEL2	Timer RC output signal inversion bit	0: Low-level period of timer RC output signal is counted 1: High-level period of timer RC output signal is counted	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

13.3.6 Timer RJ Interrupt Control Register (TRJIR)

Address 000DEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRJIE	TRJIF	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	TRJIF	Timer RJ interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b7	TRJIE	Timer RJ interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W

TRJIF Bit (Timer RJ interrupt request flag)

[Condition for setting to 0]
- When 0 is written to this bit after reading it as 1.

[Conditions for setting to 1]
- When timer RJ2 underflows.
- When the measurement of the active width of the external input (TRJIO) is completed in pulse width measurement mode.
- When the set edge of the external input (TRJIO) is input in pulse period measurement mode.

13.4 Operation

13.4.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value in the TSTART bit in the TRJCR register. When the TSTART bit is 0 (count is stopped), the count value is directly written to the reload register, and then to the counter in synchronization with the system clock (f). When the TSTART bit is 1 (count is started), the value is written to the reload register in synchronization with the count source after two or three cycles, and then to the counter in synchronization with the next count source.

Figure 13.2 shows the Timing of Rewrite Operation with TSTART Bit Value.

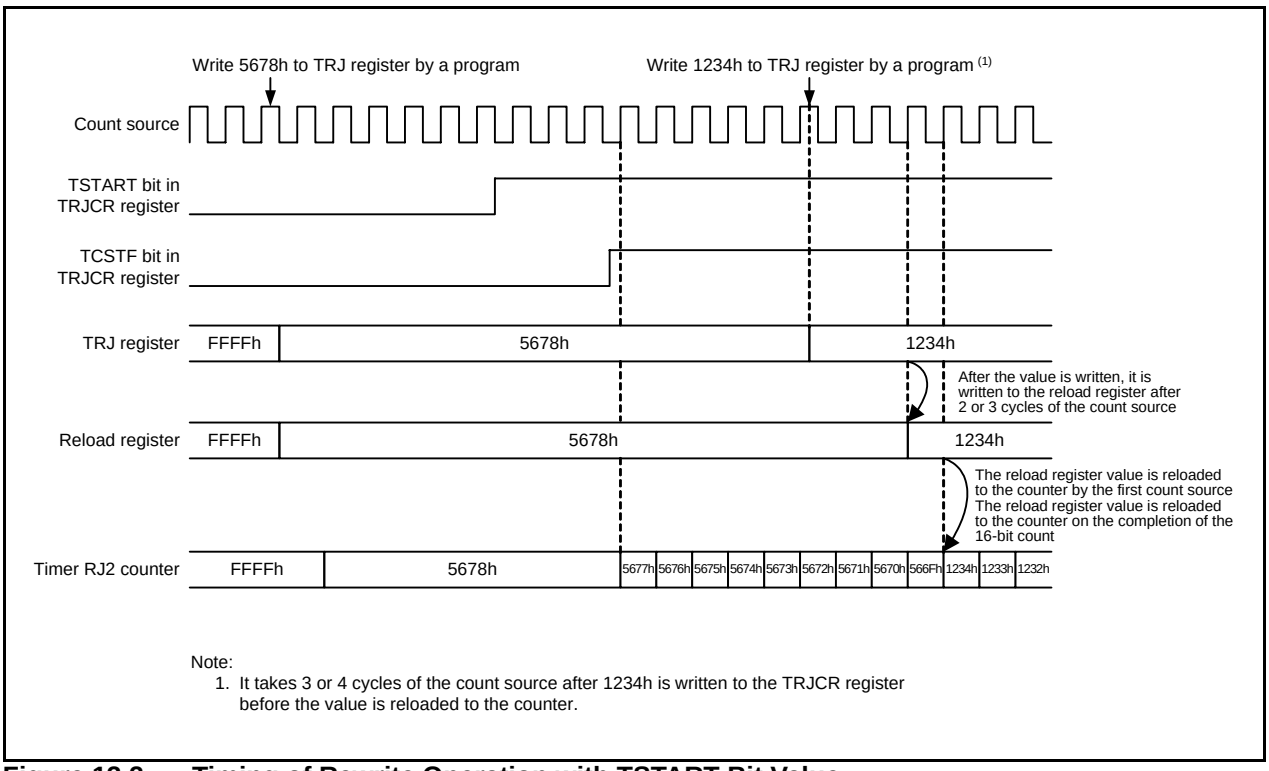


Figure 13.2 Timing of Rewrite Operation with TSTART Bit Value

13.4.2 Timer Mode

In this mode, the counter is decremented by the count source selected by bits TCK0 to TCK2 in the TRJMR register.

The count value is decremented by 1 each time the count source is input, and an underflow occurs if the next count source is input after the count value reaches 0000h. The TRJIF bit in the TRJIR register is set to 1 (interrupt requested) at that time and the value set in the reload register is loaded simultaneously. When the TRJIE bit in the TRJIR register is 1 (interrupt enabled), an interrupt request signal is generated to the CPU.

Figure 13.3 shows an Operation Example in Timer Mode.

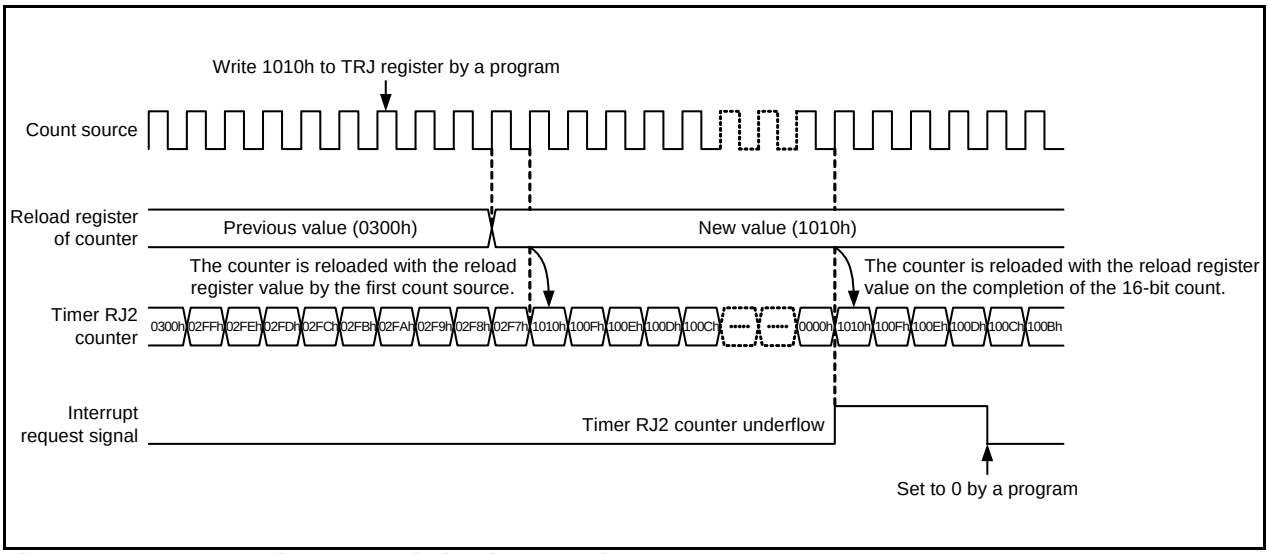
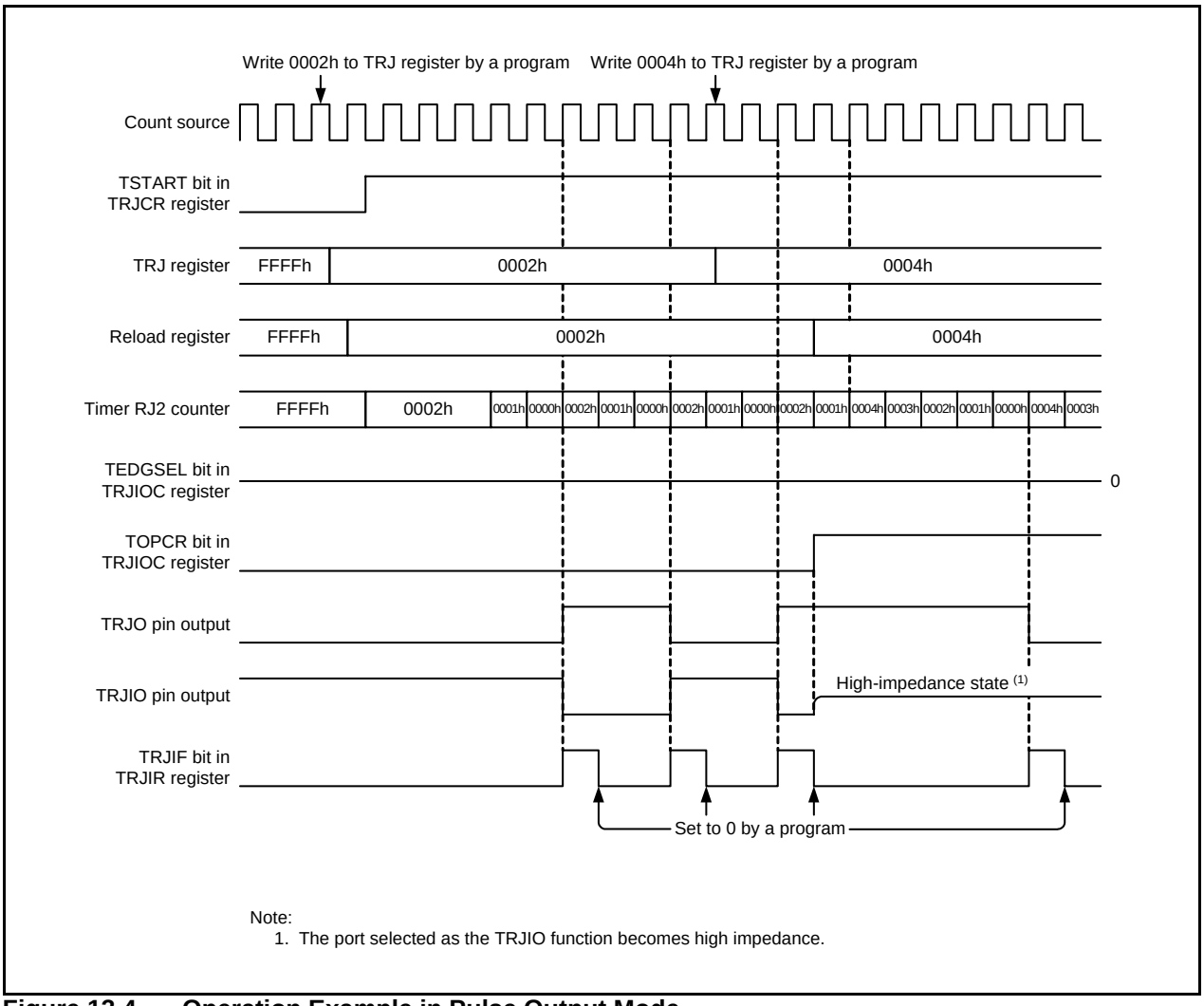


Figure 13.3 Operation Example in Timer Mode

13.4.3 Pulse Output Mode

In this mode, the counter is decremented by the count source selected by bits TCK0 to TCK2 in the TRJMR register and a pulse is output from the TRJIO pin. The output level is inverted when an underflow occurs.
The count value is decremented by 1 each time the count source is input, and an underflow occurs if the next count source is input after the count value reaches 0000h. The TRJIF bit in the TRJIR register is set to 1 (interrupt requested) at that time and the value set in the reload register is loaded simultaneously. When the TRJIE bit in the TRJIR register is 1 (interrupt enabled), an interrupt request signal is generated to the CPU.
In addition, a pulse can be output from pins TRJIO and TRJO. The output level is inverted each time an underflow occurs. The pulse output from the TRJIO pin can be stopped by the TOPCR bit in the TRJIOC register.
Also, the output level can be selected by the TEDGSEL bit in the TRJIOC register.
Figure 13.4 shows an Operation Example in Pulse Output Mode.



Note:
1. The port selected as the TRJIO function becomes high impedance.

Figure 13.4 Operation Example in Pulse Output Mode

13.4.4 Event Counter Mode

In this mode, the counter is decremented by an external pulse signal input to the TRJIO pin.
Various periods for counting events can be set by bits TIOGT0 to TIOGT1 in the TRJIOC register and the TRJISR register. In addition, the filter function for the TRJIO input can be specified by bits TIPF0 to TIPF1 in the TRJIOC register.
Also, the output from the TRJO pin can be toggled even in event counter mode.
When event counter mode is used, see **13.5 Notes on Timer RJ2 (3)**.
Figure 13.5 shows an Operation Example in Event Counter Mode.

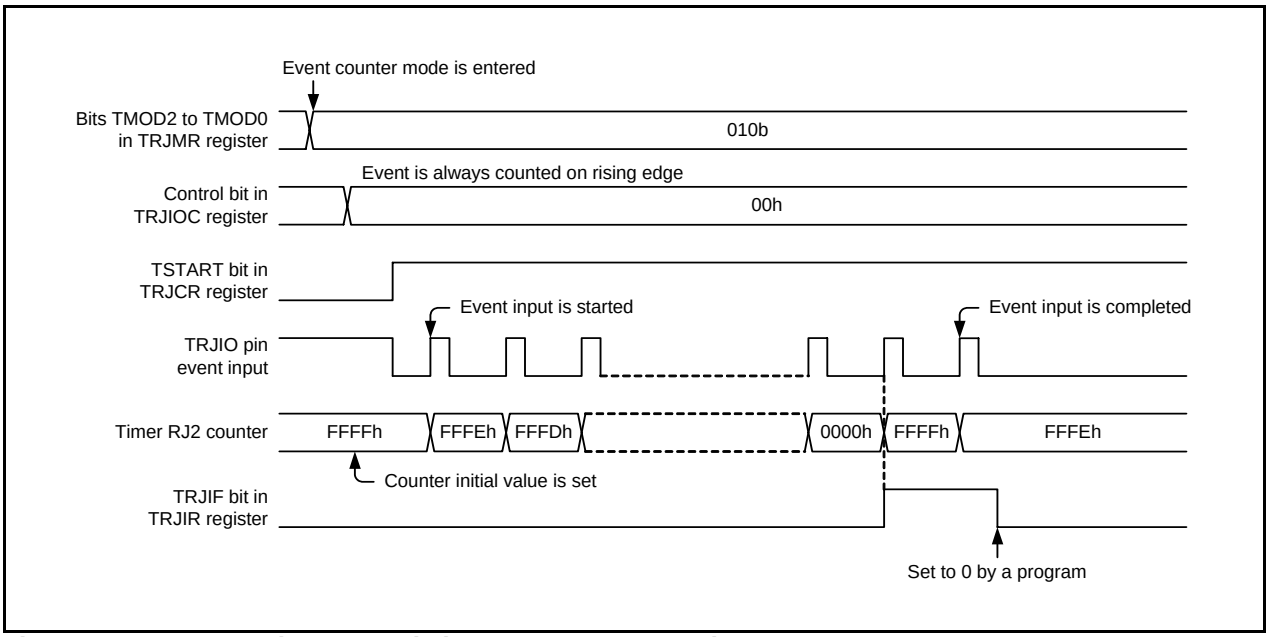


Figure 13.5 Operation Example in Event Counter Mode

13.4.5 Pulse Width Measurement Mode

In this mode, the pulse width of an external signal input to the TRJIO pin is measured.
When the level specified by the TEDGSEL bit in the TRJIOC register is input to the TRJIO pin, the decrement is started with the selected count source. When the specified level on the TRJIO pin ends, the counter is stopped, the TEDGF bit in the TRJCR register is set to 1 (active edge received), and the TRJIF bit in the TRJIR register is set to 1 (interrupt requested). The measurement of pulse width data is performed by reading the count value while the counter is stopped. Also, when the counter underflows during measurement, the TUNDF bit in the TRJCR register is set to 1 (underflow) and the TRJIF bit in the TRJIR register is set to 1 (interrupt requested). When the TRJIE bit in the TRJIR register is 1 (interrupt enabled), an interrupt request signal is generated to the CPU.
Figure 13.6 shows an Operation Example in Pulse Width Measurement Mode.
When accessing bits TEDGF and TUNDF in the TRJCR register, see **13.5 Notes on Timer RJ2 (4)**.

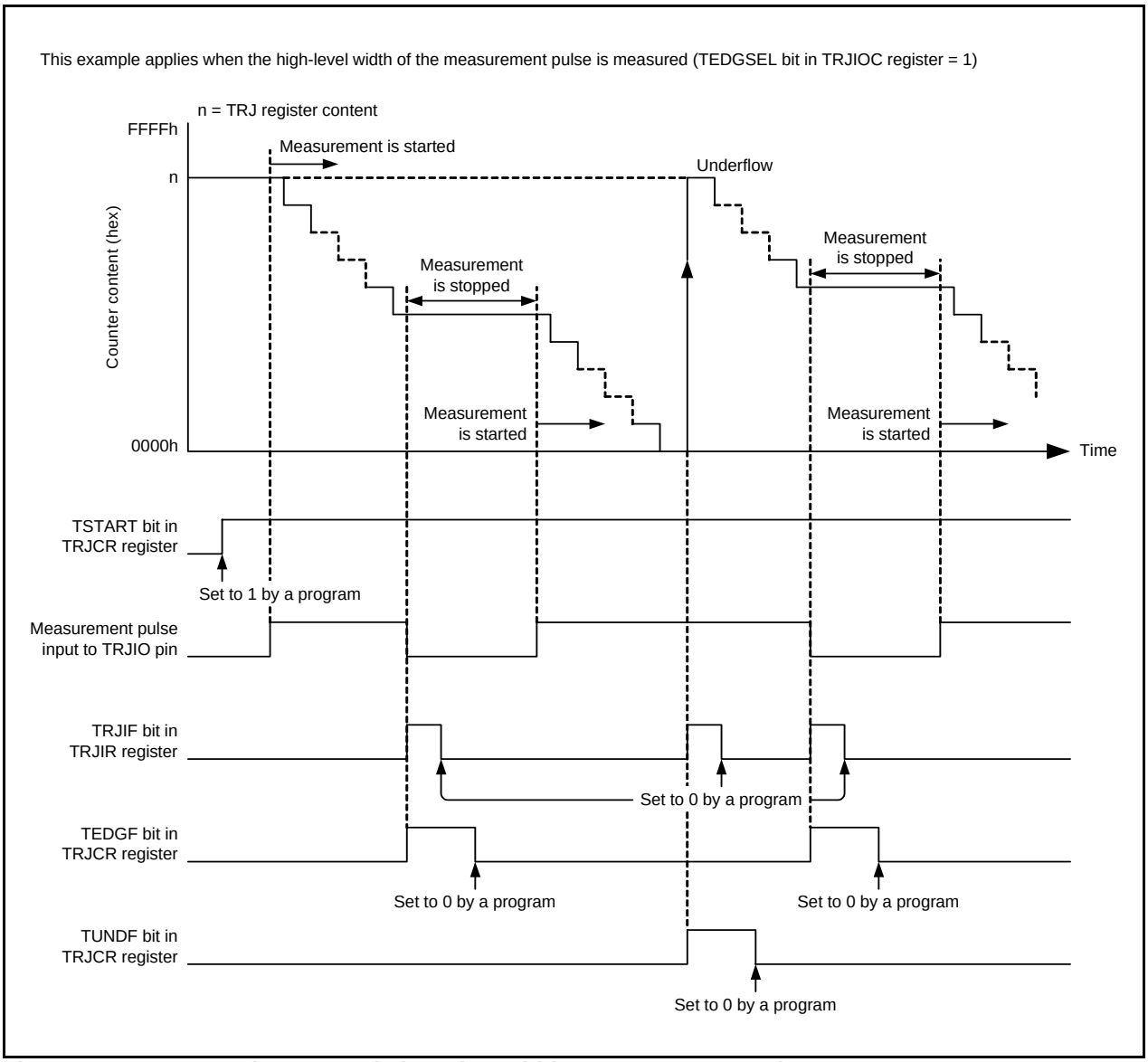


Figure 13.6 Operation Example in Pulse Width Measurement Mode

13.4.6 Pulse Period Measurement Mode

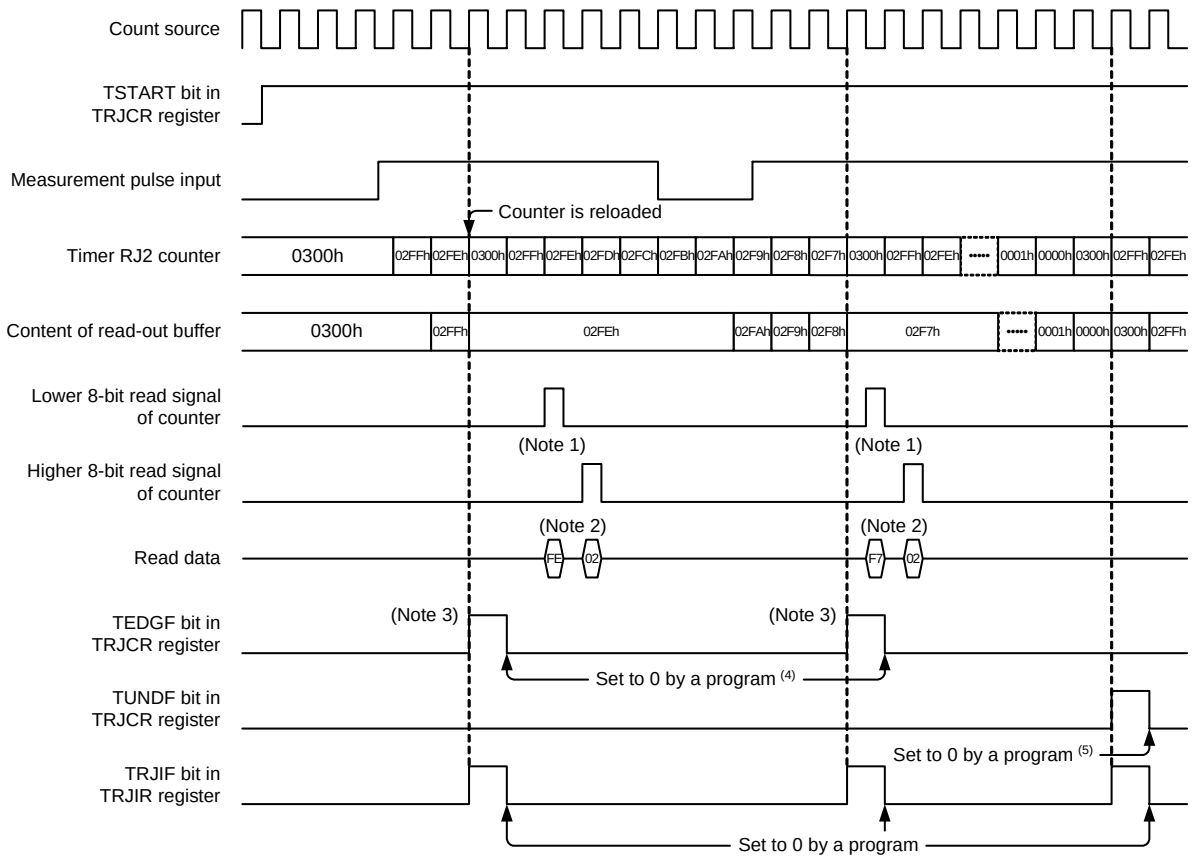
In this mode, the pulse period of an external signal input to the TRJIO pin is measured.

The counter is decremented by the count source selected by bits TCK0 to TCK2 in the TRJMR register. When a pulse with the period specified by the TEDGSEL bit in the TRJIOC register is input to the TRJIO pin, the count value is transferred to the read-out buffer on the rising edge of the count source. The value in the reload register is loaded to the counter on the next rising edge. The TEDGF bit in the TRJCR register is set to 1 (active edge received) and the TRJIF bit in the TRJIR register is set to 1 (interrupt requested) at the same time. The read-out buffer (TRJ register) is read at this time and the difference from the reload value is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDF bit in the TRJCR register is set to 1 (underflow) and the TRJIF bit in the TRJIR register is set to 1 (interrupt requested). When the TRJIE bit in the TRJIR register is 1 (interrupt enabled), an interrupt request signal is generated to the CPU.

Figure 13.7 shows an Operation Example in Pulse Period Measurement Mode.

Only input pulses with a period longer than twice the period of the count source. Also, the low-level and high-level widths must be both longer than the period of the count source. If a pulse period shorter than these conditions is input, the input may be ignored.

This example applies when the initial value in the TRJ register is set to 0300h, the TEDGSEL bit in the TRJIOC register is set to 0, and the period from one rising edge to the next edge of the measurement pulse is measured.



Notes:
1. Reading from the TRJ register must be performed during the period from when the TEDGF bit is set to 1 (active edge received) until the next active edge is input. The content of the read-out buffer is retained until the TRJ register is read. If it is not read before the active edge is input, the measurement result of the previous period is retained.
2. When the TRJ register is read in pulse period measurement mode, the content of the read-out buffer is be read.
3. After the active edge of the measurement pulse is input, the TRJ register is reloaded at the third rising edge of the count source. Then, the TEDGF bit in the TRJCR register is set to 1 (active edge received) at the fourth rising edge of the system clock (f).
4. To set to 0 by a program, use the MOV instruction to write 0 to the TEDGF bit in TRJCR register, and write 1 to the TUNDF bit at that time.
5. To set to 0 by a program, use the MOV instruction to write 0 to the TUNDF bit in TRJCR register, and write 1 to the TEDGF bit at that time.

Figure 13.7 Operation Example in Pulse Period Measurement Mode

13.4.7 Output Settings for Each Mode

Table 13.7 TRJIO Pin Setting

Operating Mode	TRJIOC Register		TRJIO Pin I/O
	TOPCR Bit	TEDGSEL Bit	
Timer mode	0 or 1	0 or 1	Input
Pulse output mode	1	0 or 1	Output disabled (1)
	0	1	Output is started at low
		0	Output is started at high
Event counter mode	0 or 1	0 or 1	Input
Pulse width measurement mode			
Pulse period measurement mode			

Note:
1. The port selected as the TRJIO function becomes high impedance.

Table 13.8 TRJO Pin Setting

Operating Mode	TRJIOC Register	TRJO Pin Output
	TEDGSEL Bit	
All modes	1	Output is started at high
	0	Output is started at low

13.5 Notes on Timer RJ2

(1) Timer RJ2 stops counting after a reset. Start the count only after setting the value in the timer.

(2) After 1 (count is started) is written to the TSTART bit in the TRJCR register while the count is stopped, the TCSTF bit in the TRJCR register remains 0 (count is stopped) for two to three cycles of the count source. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 1 (count is in progress). The count is started from the first active edge of the count source after the TCSTF bit is set to 1. After 0 (count is stopped) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for two to three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 0.
Note:
1. Registers associated with timer RJ2: TRJ, TRJCR, TRJIOC, and TRJMR

(3) In event counter mode, set the TSTART bit in the TRJCR register to 1 (count is started) and then input an external pulse.

(4) In pulse width/pulse period measurement modes, bits TEDGF and TUNDF in the TRJCR register used are set to 0 by writing 0 by a program but remain unchanged even if 1 is written to these bits. If a read-modify-write instruction is used to set the TRJCR register, bits TEDGF and TUNDF may be erroneously set to 0 depending on the timing, even when the TEDGF bit is set to 1 (active edge received) and the TUNDF bit is set to 1 (underflow) during execution of the instruction.
In this case, write 1 using the MOV instruction to the TEDGF or TUNDF bit which is not supposed to be set to 0.

(5) Insert NOP instructions between writing to and reading from registers associated with the TRJ counter while the counter is stopped.

(6) When the TSTART bit in the TRJCR register is 1 (count is started) or the TCSTF bit is 1 (count is in progress), allow at least three cycles of the count source clock for each write interval when writing to the TRJ register successively.

(7) When the mode is changed to pulse width measurement mode or pulse period measurement mode from another mode, the values of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before starting the timer RJ2 count.

(8) The TEDGF bit may be set to 1 by the first count source signal after the count is started.

(9) When using pulse period measurement mode, allow at least two periods of the count source for timer RJ2 immediately after the count is started and set the TEDGF bit to 0 before use.

(10) If the count is forcibly stopped by writing 1 to the TSTOP bit in the TRJCR register during count operation, the TRJIF bit in the TRJIR register may be set to 1 (interrupt requested). Set the TRJIF bit to 0 (no interrupt requested) before restarting the count.

(11) In pulse width measurement mode or pulse period measurement mode, set associated registers and set the TSTART bit in the TRJCR register to 1 (count is started) before inputting an external event.

(12) Do not set the TRJ register to 0000h in pulse width measurement mode and pulse period measurement mode.

(13) Note the following when writing 0 to the TEDGF bit in the TRJCR register in pulse width measurement mode or pulse period measurement mode.
Set the TRJIF bit in the TRJIR register to 0 before setting the TEDGF bit to 0.
When reading the TEDGF bit immediately after setting it to 0, it is read as 0. However the internal signal of the TEDGF bit remains 1 for one to two cycles of the count source. If an active edge is input during this period, the internal signal of the TEDGF bit does not become 0 and the TEDGF bit is read as 1.
Since the TRJIF bit becomes 1 when the internal signal of the TEDGF bit changes from 0 to 1, the TRJIF bit does not become 1 and no interrupt is generated.
After setting the TEDGF bit to 0, confirm that 0 can be read after waiting for three or more count source cycles in order to accept the next interrupt request.

14. Timer RB2

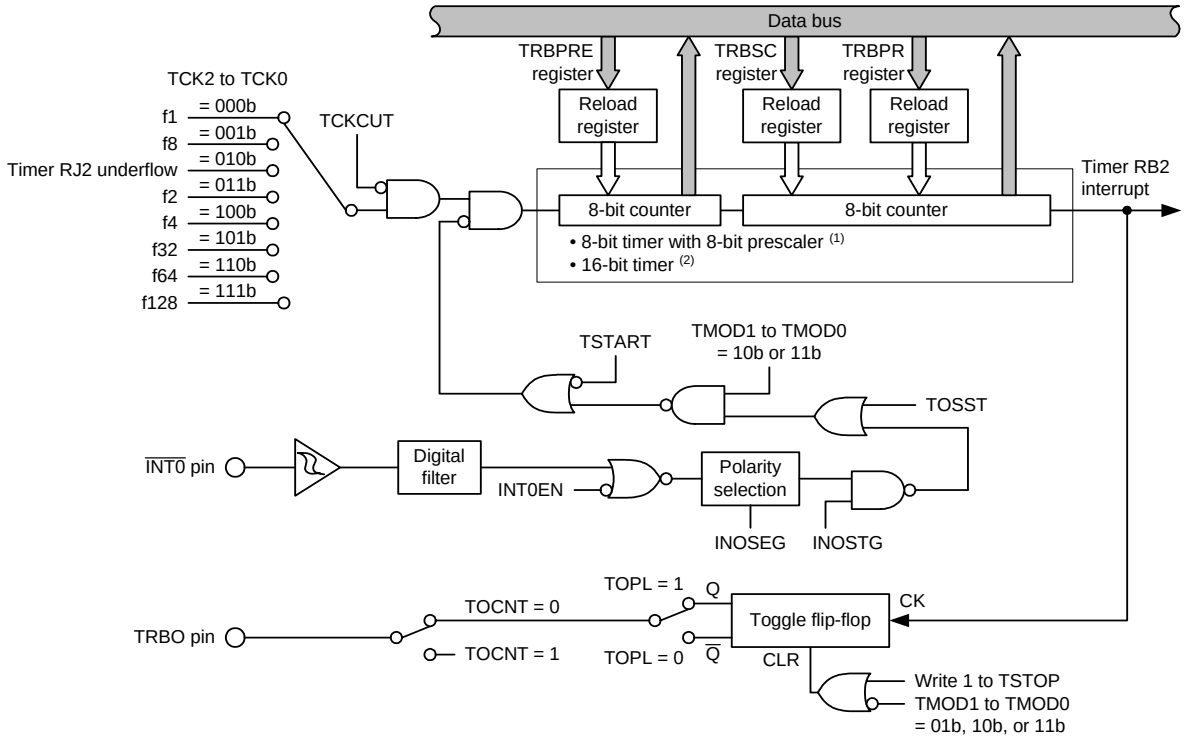
Timer RB2 can be used as an 8-bit timer with an 8-bit prescaler or as a 16-bit timer. The prescaler and timer each consist of a reload register and counter which are allocated to the same address. Timer RB2 has timer RB primary and timer RB secondary reload registers.

14.1 Overview

Table 14.1 lists the Timer RB2 Specifications. Figure 14.1 shows the Timer RB2 Block Diagram.

Table 14.1 Timer RB2 Specifications

Item		Description
Operating modes	Timer mode	An internal count source or timer RJ2 underflow is counted.
	Programmable waveform generation mode	An arbitrary pulse width is output successively.
	Programmable one-shot generation mode	A one-shot pulse is output.
	Programmable wait one-shot generation mode	A delayed one-shot pulse is output.
Count source		Selectable from f1, f2, f4, f8, f32, f64, f128, and timer RJ2 underflow.
Interrupt		Timer RB2 underflow



INT0EN: Bit in INTEN register
TSTART, TSTOP: Bits in TRBCR register
TOSST: Bit in TRBOCR register
TOPL, TOCNT, INOSTG, INOSEG: Bits in TRBIOC register
TMOD0 to TMOD1, TCK0 to TCK2, TCKCUT: Bits in TRBMR register

Notes:
1. When the TCNT16 bit in the TRBMR register is 0, the 8-bit timer with 8-bit prescaler is selected.
2. When the TCNT16 bit in the TRBMR register is 1, the 16-bit timer is selected.

Figure 14.1 Timer RB2 Block Diagram

14.2 I/O Pins

Table 14.2 lists the Timer RB2 Pin Configuration.

Table 14.2 Timer RB2 Pin Configuration

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P1_4, P4_5	I	External trigger
TRBO	P1_3, P3_1, P4_2	O	Continuous pulse or one-shot pulse output

For details on $\overline{\text{INT0}}$, see **11. Interrupts**.

14.3 Registers

Table 14.3 lists the Timer RB2 Register Configuration.

Table 14.3 Timer RB2 Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RB Control Register	TRBCR	00h	000E0h	8
Timer RB One-Shot Control Register	TRBOCR	00h	000E1h	8
Timer RB I/O Control Register	TRBIOC	00h	000E2h	8
Timer RB Mode Register	TRBMR	00h	000E3h	8
8-bit timer with 8-bit prescaler: Timer RB Prescaler Register 16-bit timer: Timer RB Primary/Secondary Register (Lower 8 Bits)	TRBPRE	FFh	000E4h	8
8-bit timer with 8-bit prescaler: Timer RB Primary Register 16-bit timer: Timer RB Primary Register (Higher 8 Bits)	TRBPR	FFh	000E5h	8
8-bit timer with 8-bit prescaler: Timer RB Secondary Register 16-bit timer: Timer RB Secondary Register (Higher 8 Bits)	TRBSC	FFh	000E6h	8
Timer RB Interrupt Control Register	TRBIR	00h	000E7h	8

14.3.1 Timer RB Control Register (TRBCR)

Address 000E0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RB count start bit (1)	[When the TMOD1 bit in the TRBMR register is 0] 0: Count is stopped 1: Count is started [When the TMOD1 bit in the TRBMR register is 1] 0: Count is stopped 1: Count is enabled	R/W
b1	TCSTF	Timer RB count status flag (1)	[When the TMOD1 bit in the TRBMR register is 0] 0: Count is stopped 1: Count is in progress [When the TMOD1 bit in the TRBMR register is 1] 0: Count is stopped 1: Count is enabled	R
b2	TSTOP	Timer RB count forced stop bit (1, 2)	When 1 is written to this bit, the count is forcibly stopped. The read value is 0.	R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. For notes on using bits TSTART, TCSTF, and TSTOP, see **14.8 Notes on Timer RB2**.
2. When 1 (count is forcibly stopped) is written to the TSTOP bit, the counter, registers TRBPRE, TRBPR, and TRBSC, bits TSTART and TCSTF, and bits TOSST, TOSSP, and TOSSTF in the TRBOCR register are initialized. The TRBO output is also initialized.

TSTART Bit (Timer RB count start bit)

[Condition for setting to 0]
• When 0 is written to this bit.
[Condition for setting to 1]
• When 1 is written to this bit.

TCSTF Bit (Timer RB count status flag)

[Conditions for setting to 0]
• When 0 is written to the TSTART bit.
• When 1 is written to the TSTOP bit.
[Condition for setting to 1]
• When 1 is written to the TSTART bit.

14.3.2 Timer RB One-Shot Control Register (TRBOCR)

Address 000E1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TOSSTF	TOSSP	TOSST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOSST	Timer RB one-shot start bit (1, 2)	When 1 is written to this bit, a one-shot trigger is generated. The read value is 0.	R/W
b1	TOSSP	Timer RB one-shot stop bit (2, 3)	When 1 is written to this bit, the one-shot pulse count (including wait time) is stopped. The read value is 0	R/W
b2	TOSSTF	Timer RB one-shot status flag	0: One-shot is stopped 1: One-shot is operating (including wait period)	R
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. Make sure the TOSSTF bit is 0 (one-shot is stopped) before writing 1 (one-shot count is started) to the TOSST bit.
2. When 0 is written to this bit, the value is invalid.
3. Make sure the TOSSTF bit is 1 (one-shot is operating (including wait period)) before writing 1 (one-shot count is stopped) to the TOSSP bit.

TOSSTF Bit (Timer RB one-shot status flag)

[Conditions for setting to 0]
- When the TSTOP bit in the TRBCR register is set to 1 (count is forcibly stopped).
- When the count value reaches 00h and is reloaded in programmable one-shot generation mode.
- When the secondary count value reaches 00h and is reloaded in programmable wait one-shot generation mode.
- When the TOSSP bit is set to 1 (one-shot count is stopped).
- When the TSTART bit in the TRBCR register is set to 0 (count is stopped) and then 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register.

[Conditions for setting to 1]
- When the TOSST bit is set to 1 (one-shot count is started).
- When a trigger is input.

The TRBOCR register is enabled when bits TMOD1 to TMOD0 in the TRBMR register are 10b (programmable one-shot generation mode) or 11b (programmable wait one-shot generation mode).

14.3.3 Timer RB I/O Control Register (TRBIOC)

Address 000E2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	See **Table 14.4 Functions of Timer RB Output Level Select Bit**.	R/W
b1	TOCNT	Timer RB output switch bit	0: Waveform output 1: Fixed-value output	R/W
b2	INOSTG	One-shot trigger control bit	0: One-shot trigger to $\overline{\text{INT0}}$ pin disabled 1: One-shot trigger to $\overline{\text{INT0}}$ pin enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	—			
b7	—			

TOCNT Bit (Timer RB output switch bit)

The setting of the TOCNT bit is valid only in programmable waveform, programmable one-shot, and programmable wait one-shot generation modes.

For details on the change in the states of the TRBO output in each mode, see **14.5.3 TOCNT Bit Setting and Pin States**.

Table 14.4 Functions of Timer RB Output Level Select Bit

Operating Mode	Function	
Timer mode	Set to 0 in timer mode.	
Programmable waveform generation mode	0	High-level output during primary period Low-level output during secondary period Low-level output at timer stop
	1	Low-level output during primary period High-level output during secondary period High-level output at timer stop
Programmable one-shot generation mode	0	High-level one-shot pulse output Low-level output at timer stop
	1	Low-level one-shot pulse output High-level output at timer stop
Programmable wait one-shot generation mode	0	High-level one-shot pulse output Low-level output at timer stop and during wait period
	1	Low-level one-shot pulse output High-level output at timer stop and during wait period

14.3.4 Timer RB Mode Register (TRBMR)

Address 000E3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	TWRC	TCNT16	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RB operating mode select bits (1)	b1 b0 0 0: Timer mode 0 1: Programmable waveform generation mode 1 0: Programmable one-shot generation mode 1 1: Programmable wait one-shot generation mode	R/W
b1	TMOD1			R/W
b2	TCNT16	Timer RB counter select bit (1)	0: 8-bit timer with 8-bit prescaler 1: 16-bit timer	R/W
b3	TWRC	Timer RB write control bit (2)	0: Write to reload register and counter 1: Write to reload register only	R/W
b4	TCK0	Timer RB count source select bits (1)	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: Timer RJ2 underflow 0 1 1: f2 1 0 0: f4 1 0 1: f32 1 1 0: f64 1 1 1: f128	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RB count source cutoff bit (1)	0: Count source is supplied 1: Count source is cut off	R/W

Notes:
1. Only change these bits when bits TSTART and TCSTF in the TRBCR register are 0 (count is stopped).
2. For details on writing to the register and counter using the TWRC bit, see **14.5.2 Prescaler and Counter Using TWRC Bit**.

14.3.5 Timer RB Prescaler Register (TRBPRE)

Address 000E4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Initial Value	Setting Range	R/W
b7 to b0	Timer mode	An internal count source or the timer RJ2 underflow is counted.	FFh	00h to FFh	R/W
	Programmable waveform generation mode		FFh	00h to FFh	R/W
	Programmable one-shot generation mode		FFh	00h to FFh	R/W
	Programmable wait one-shot generation mode		FFh	00h to FFh	R/W

In the 8-bit timer with 8-bit prescaler, the TRBPRE register is used to set the period of the prescaler. Each time the prescaler decrements and underflows, the value in the TRBPRE register is reloaded. When read, the value is read from the prescaler.

In the 16-bit timer, the TRBPRE register is used as the lower 8-bit counter. Each time the counter decrements and underflows, the value in the TRBPRE register is reloaded. When read, the value is read from the lower 8 bits of the counter. Access the TRBPRE register first and then the TRBPR register.

The TRBPRE register is configured with a master – reload register structure, so the reload register is written simultaneously while the count is stopped. During the counter operation, the timing for updating the reload register differs in each mode. For details, see **Table 14.6 Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler**, and **Table 14.7 Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer**. The value is updated in synchronization with the count source.

14.3.6 Timer RB Primary Register (TRBPR)

Address 000E5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function		Initial Value	Setting Range	R/W
		8-Bit Timer with 8-Bit Prescaler	16-Bit Timer			
b7 to b0	Timer mode	Timer RB prescaler underflow is counted.	An internal count source or the timer RJ2 underflow is counted.	FFh	00h to FFh	R/W
	Programmable waveform generation mode	Timer RB prescaler underflow is counted. (1)		FFh	00h to FFh	R/W
	Programmable one-shot generation mode	Timer RB prescaler underflow is counted (the one-shot width is counted).		FFh	00h to FFh	R/W
	Programmable wait one-shot generation mode	Timer RB prescaler underflow is counted (the wait period is counted).		FFh	00h to FFh	R/W

Note:
1. The values in registers TRBPR and TRBSC are reloaded and counted alternately.

In the 8-bit timer with 8-bit prescaler, the TRBPR register is used to set the period of the counter and the primary period. When read, the value is from the 8-bit counter.
In the 16-bit timer, the TRBPR register is used to set the period of the higher 8-bit counter and the primary period. When read, the value is read from the higher 8 bits of the 16-bit timer. Access the TRBPRE register and then the TRBPR register.
The TRBPR register is configured with a master – reload register structure, so the reload register is written simultaneously while the count is stopped. During the counter operation, the timing for updating the reload register differs in each mode. For details, see **Table 14.6 Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler**, and **Table 14.7 Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer**.

14.3.7 Timer RB Secondary Register (TRBSC)

Address 000E6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function		Initial Value	Setting Range	R/W
		8-Bit Timer with 8-Bit Prescaler	16-Bit Timer			
b7 to b0	Timer mode	Disabled		FFh	Invalid	—
	Programmable waveform generation mode	Timer RB prescaler underflow	Internal count source or timer RJ2 underflow (1)	FFh	00h to FFh	R/W
	Programmable one-shot generation mode	Disabled		FFh	Invalid	—
	Programmable wait one-shot generation mode	Timer RB prescaler underflow	Internal count source or timer RJ2 underflow (1)	FFh	00h to FFh	R/W

Note:
1. The values in registers TRBPR and TRBSC are reloaded and counted alternately. The count value can be read from the TRBPR register while the secondary period is counted.

In the 8-bit timer with 8-bit prescaler, use the following procedure when writing to the TRBSC register.
(1) Write a value to the TRBSC register.
(2) Write a value to TRBPR register (write the same value as the previous one again even if the value is not changed).
In the 16-bit timer, use the following procedure when writing to the TRBSC register.
(1) Write values to registers TRBPRE and TRBSC.
(2) Write a value to TRBPR register (write the same value as the previous one again even if the value is not changed).

In the 8-bit timer with 8-bit prescaler, the TRBSC register is used to set the secondary period used in programmable waveform and programmable wait one-shot generation modes. When read, the value is read from the reload register.
In the 16-bit timer, the TRBSC register is used to set the higher 8-bit secondary period used in programmable waveform and programmable wait one-shot generation modes. This setting can be made in timer mode and programmable one-shot generation mode, but it is not used for counter operation. When read, the value is read from the reload register.
The TRBSC register is configured with a master – reload register structure, so the reload register is written simultaneously while the count is stopped. During the counter operation, the timing for updating the reload register differs in each mode. For details, see **Table 14.6 Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler**, and **Table 14.7 Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer**.

14.3.8 Timer RB Interrupt Control Register (TRBIR)

Address 000E7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TRBIE	TRBIF	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	TRBIF	Timer RB interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W
b7	TRBIE	Timer RB interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W

TRBIF Bit (Timer RB interrupt request flag)

[Condition for setting to 0]

• When 0 is written to this bit after reading it as 1.

[Condition for setting to 1]

• See **Table 14.5 Conditions for Setting TRBIF Bit to 1**.

Table 14.5 Conditions for Setting TRBIF Bit to 1

Operating Mode	Condition
Timer mode	When timer RB2 underflows.
Programmable waveform generation mode	When timer RB2 underflows during the secondary period.
Programmable one-shot generation mode	When timer RB2 underflows.
Programmable wait one-shot generation mode	When timer RB2 underflows during the secondary period.

14.4 Operation

14.4.1 Timer Mode

In this mode, an internally generated count source or the timer RJ2 underflow is counted. Registers TRBOCR and TRBSC are not used.

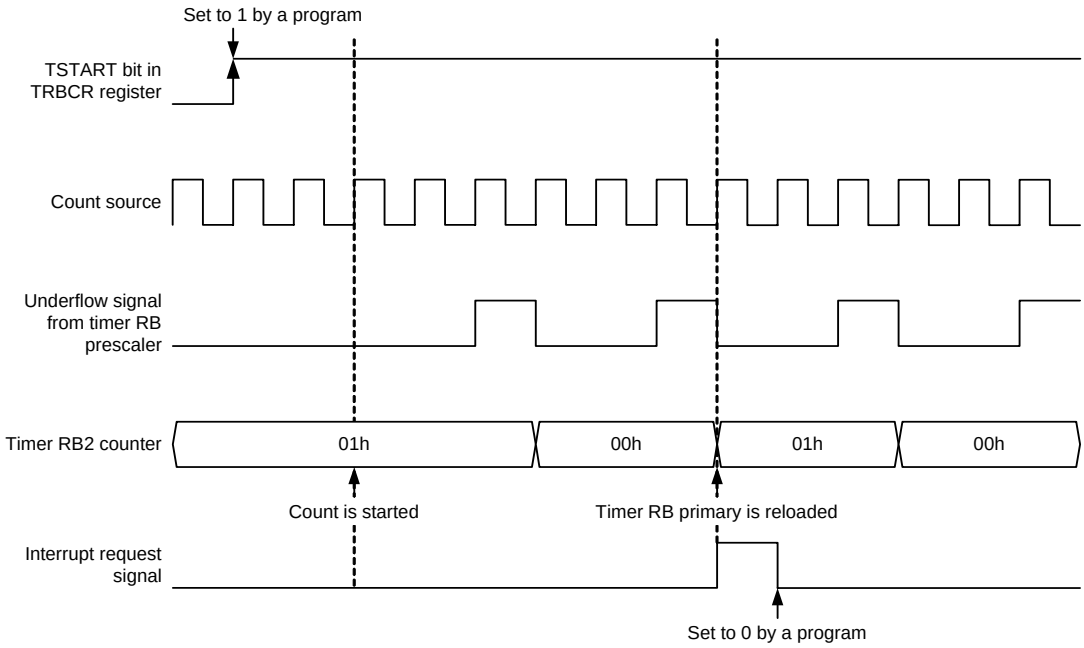
When 1 (count is started) is written to the TSTART bit in the TRBCR register, the count is started after the count source is sampled three times. When 0 (count is stopped) is written to the TSTART bit, the count is stopped after the count source is sampled three times. When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped. The actual count state should be monitored with the TCSTF bit in the TRBCR register.

An interrupt request is generated when timer RB2 underflows.

When registers TRBPRE and TRBPR are read, each count value can be read. When registers TRBPRE and TRBPR are written to while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during the count operation, values are written to both the reload register and counter. When the TWRC bit is 1, values are written to the reload register only.

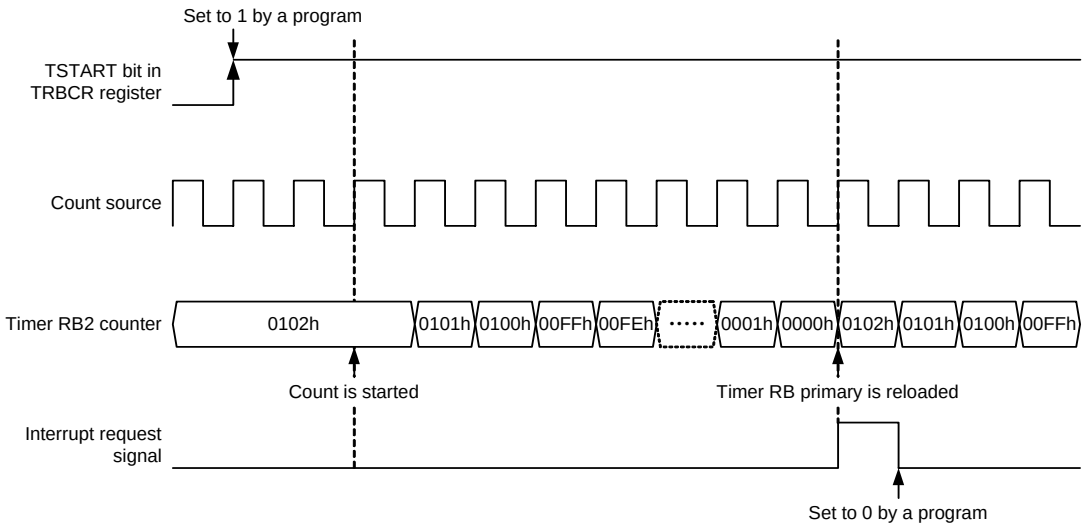
Figure 14.2 shows an Operation Example in Timer Mode.

• 8-bit timer with 8-bit prescaler in timer mode



The above diagram applies under the following conditions:
- TRBPRE register = 02h, TRBPR register = 01h
- TOCNT bit in TRBIOC register = 0 (waveform output)
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)

• 16-bit timer in timer mode

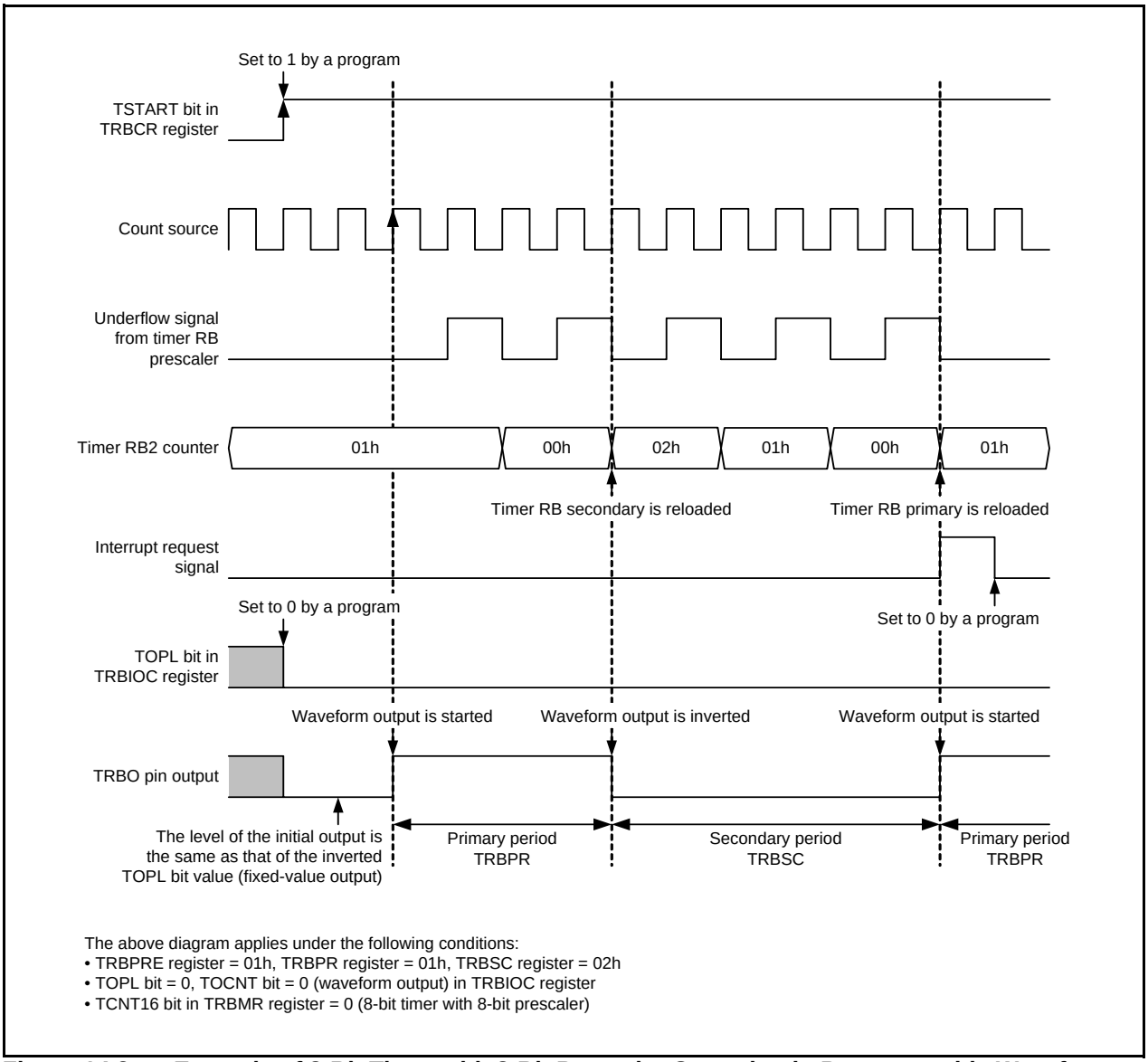


The above diagram applies under the following conditions:
- TRBPRE register = 02h, TRBPR register = 01h
- TOCNT bit in TRBIOC register = 0 (waveform output)
- TCNT16 bit in TRBMR register = 1 (16-bit timer)

Figure 14.2 Operation Example in Timer Mode

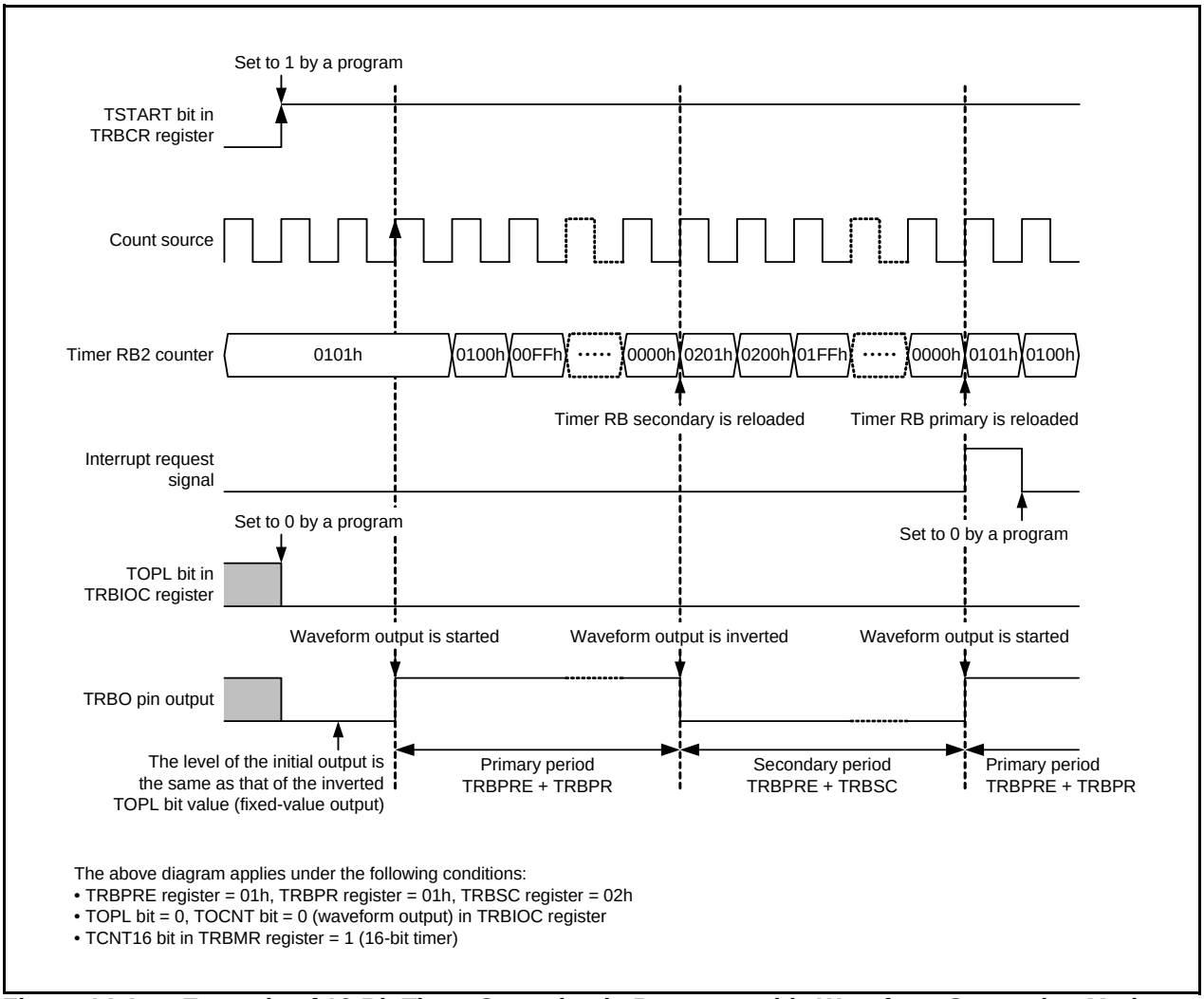
14.4.2 Programmable Waveform Generation Mode

In the 8-bit timer with 8-bit prescaler, the values in registers TRBPR and TRBSC are counted alternately.
In the 16-bit timer, the lower 8 bits are counted by the TRBPRE register and the higher 8 bits are counted by registers TRBPR and TRBSC alternately.
The TRBO pin outputs a signal which is inverted each time the counter underflows. The count is started from the value set in the TRBPR register. In programmable waveform generation mode, the TRBOCR register is not used.
When 1 (count is started) is written to the TSTART bit in the TRBCR register, the count is started after the count source is sampled three times. When 0 (count is stopped) is written to the TSTART bit, the count is stopped after the count source is sampled three times. When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped. The actual count state should be monitored with the TCSTF bit in the TRBCR register.
An interrupt request is generated when timer RB2 underflows during the secondary period.
When registers TRBPRE and TRBPR are read, each count value can be read. Read the TRBPR register even while the secondary period is counted. When registers TRBPRE, TRBPR, and TRBSC are written while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during the count operation, values are written to the reload register and then transferred to the counter at the next reload operation.
Figure 14.3 shows an Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Waveform Generation Mode. Figure 14.4 shows an Example of 16-Bit Timer Operation in Programmable Waveform Generation Mode.



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h, TRBSC register = 02h
- TOPL bit = 0, TOCNT bit = 0 (waveform output) in TRBIOC register
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)

Figure 14.3 Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Waveform Generation Mode



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h, TRBSC register = 02h
- TOPL bit = 0, TOCNT bit = 0 (waveform output) in TRBIOC register
- TCNT16 bit in TRBMR register = 1 (16-bit timer)

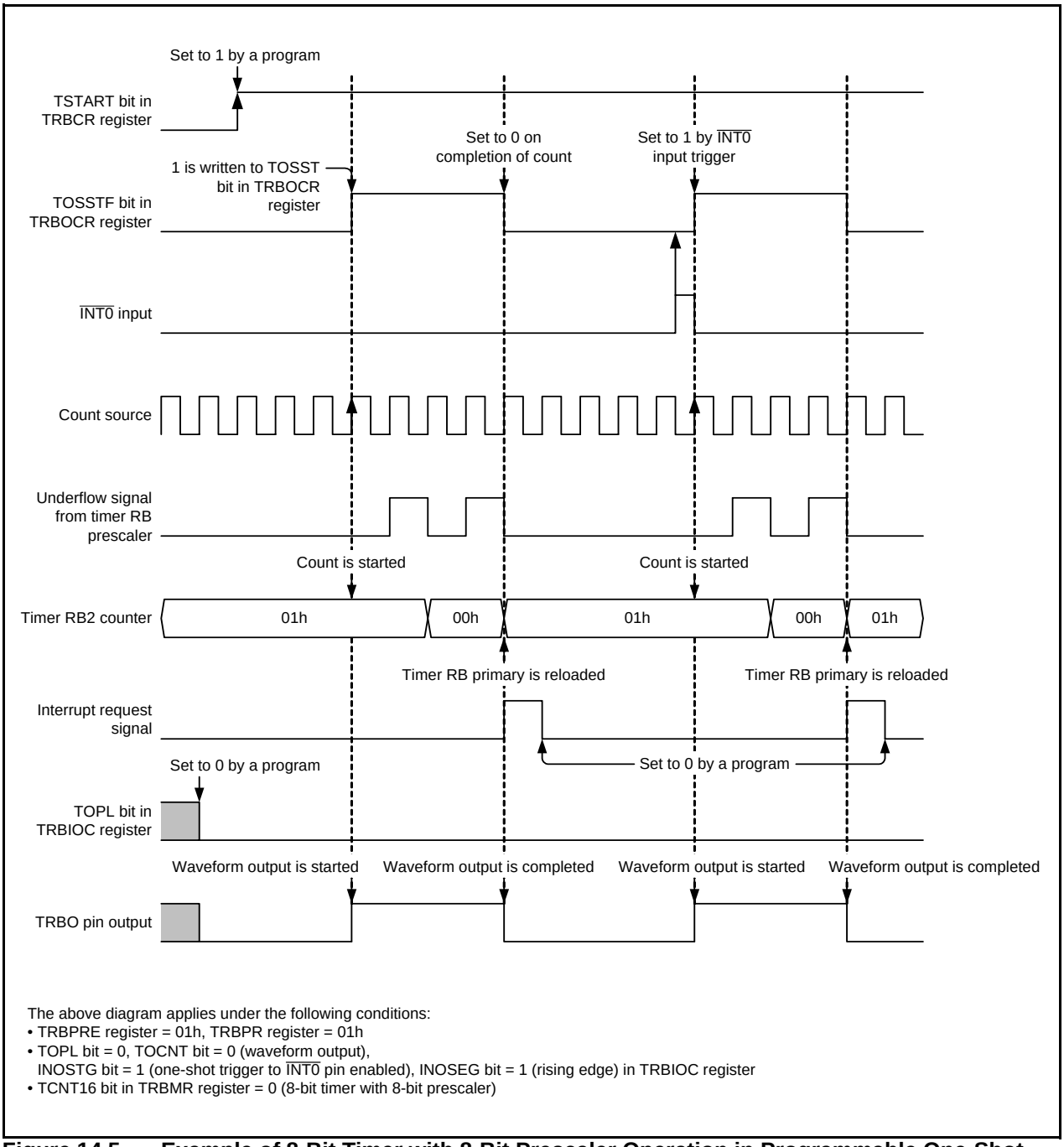
Figure 14.4 Example of 16-Bit Timer Operation in Programmable Waveform Generation Mode

14.4.3 Programmable One-Shot Generation Mode

In this mode, a one-shot pulse is output from the TRBO pin by a program or the $\overline{\text{INT0}}$ pin input. When a trigger is generated from that point, the timer operates only once to count a given length of the time equal to the setting value of the TRBPR register.
In the 8-bit timer with 8-bit prescaler, the count value is set in the TRBPR register.
In the 16-bit timer, the count value of the higher 8 bits is set in the TRBPR register and that of the lower 8 bits is set in the TRBPRE register.
In programmable one-shot generation mode, the TRBSC register is not used.
When 1 (one-shot count is started) is written to the TOSST bit in the TRBOCR register while the TCSTF bit in the TRBCR register is 1 (count is enabled), the count is started after the count source is sampled three times. If an enabled trigger is input to the $\overline{\text{INT0}}$ pin while the TCSTF bit is 1, the count is started after the count source is sampled three times. When the count value in the timer RB secondary overflows and then it is reloaded, the count is stopped. The count is also stopped with any of the following settings:

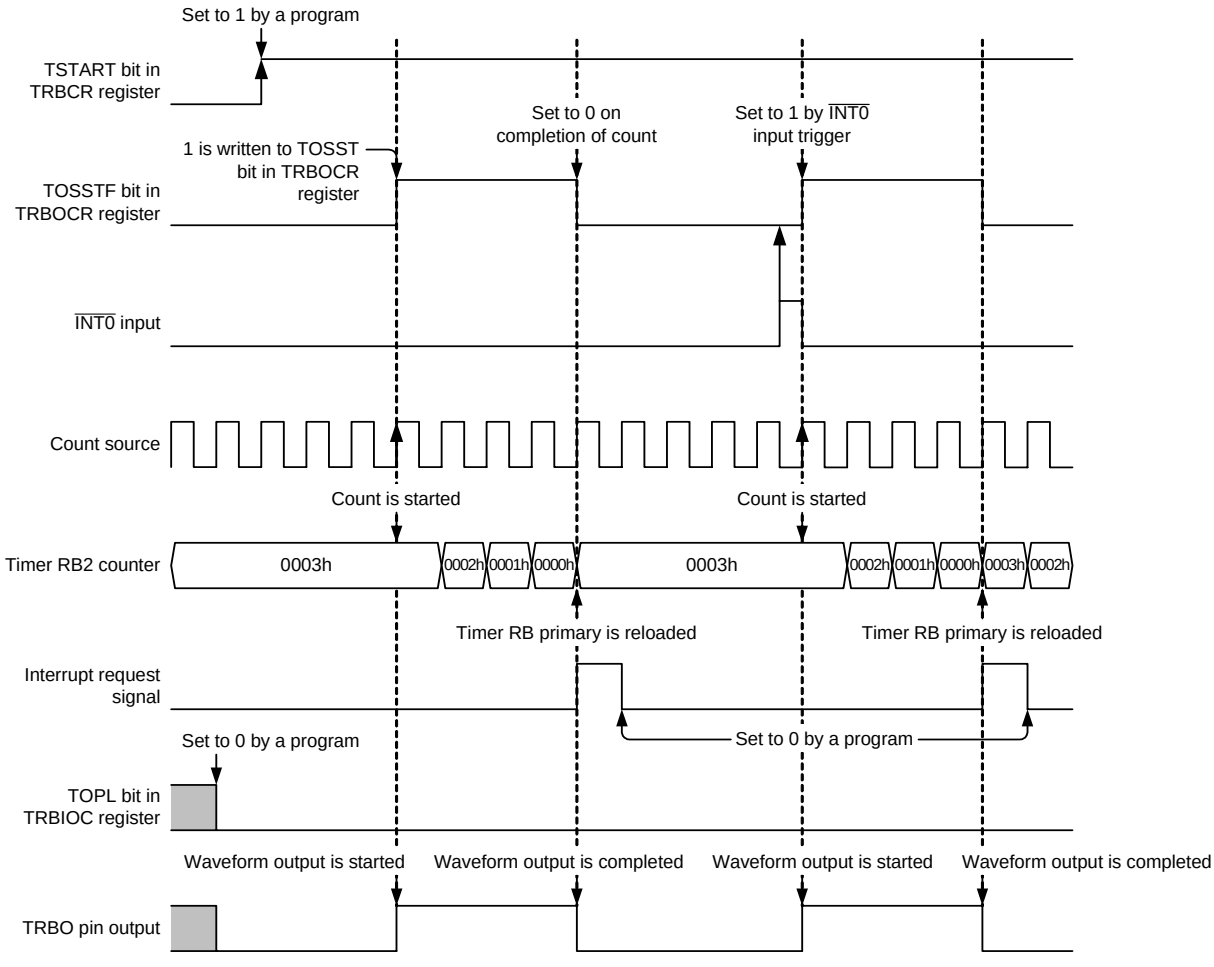
- When 1 (one-shot count is stopped) is written to the TOSSP bit in the TRBOCR register, the count is stopped after the count source is sampled three times.
- When 0 (count is stopped) is written to the TSTART bit in the TRBCR register, the count is stopped after the count source is sampled three times.
- When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped.

The actual count state must be monitored with the TCSTF bit in the TRBCR register.
An interrupt request is generated when timer RB2 underflows.
When registers TRBPRE and TRBPR are read, each count value can be read. When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during the count operation, values are written to the reload register and then transferred to the counter at the next reload operation.
For the setting of trigger by the $\overline{\text{INT0}}$ input, see **14.7 INT0 Input Trigger Selection**.
Figure 14.5 shows an Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable One-Shot Generation Mode. Figure 14.6 shows an Example of 16-Bit Timer Operation in Programmable One-Shot Generation Mode.



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h
- TOPL bit = 0, TOCNT bit = 0 (waveform output), INOSTG bit = 1 (one-shot trigger to INT0 pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)

Figure 14.5 Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable One-Shot Generation Mode



The above diagram applies under the following conditions:
- TRBPRE register = 03h, TRBPR register = 00h
- TOPL bit = 0, TOCNT bit = 0 (waveform output), INOSTG bit = 1 (one-shot trigger to INT0 pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TCNT16 bit in TRBMR register = 1 (16-bit timer)

Figure 14.6 Example of 16-Bit Timer Operation in Programmable One-Shot Generation Mode

14.4.4 Programmable Wait One-Shot Generation Mode

In this mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger ($\overline{\text{INT0}}$ pin input) after a specified period. When a trigger is generated from that point, the timer outputs a pulse only once for a given length of the time equal to the setting value of the TRBSC register after waiting for a given length of time equal to the setting value of the TRBPR register.

In the 8-bit timer with 8-bit prescaler, set the count value of the wait time in the TRBPR register and set the count value of the pulse width in the TRBSC register.

In the 16-bit timer, set the count value of the wait time of the higher 8 bits in the TRBPR register and that of the lower 8 bits in the TRBPRE register. Set the count value of the pulse width of the higher 8 bits in the TRBSC register and that of the lower 8 bits in the TRBPRE register.

When 1 (one-shot count is started) is written to the TOSST bit in the TRBOCR register while the TCSTF bit in the TRBCR register is 1 (count is enabled), the count is started after the count source is sampled three times. If an enabled trigger is input to the $\overline{\text{INT0}}$ pin while the TCSTF bit is 1, the count is started after the count source is sampled three times. When the count value in the timer RB secondary underflows and then it is reloaded, the count is stopped. The count is also stopped with any of the following settings:

- When 1 (one-shot count is stopped) is written to the TOSSP bit in the TRBOCR register, the count is stopped after the count source is sampled three times.
- When 0 (count is stopped) is written to the TSTART bit in the TRBCR register, the count is stopped after the count source is sampled three times.
- When 1 (count is forcibly stopped) is written to the TSTOP bit in the TRBCR register, the count is stopped.

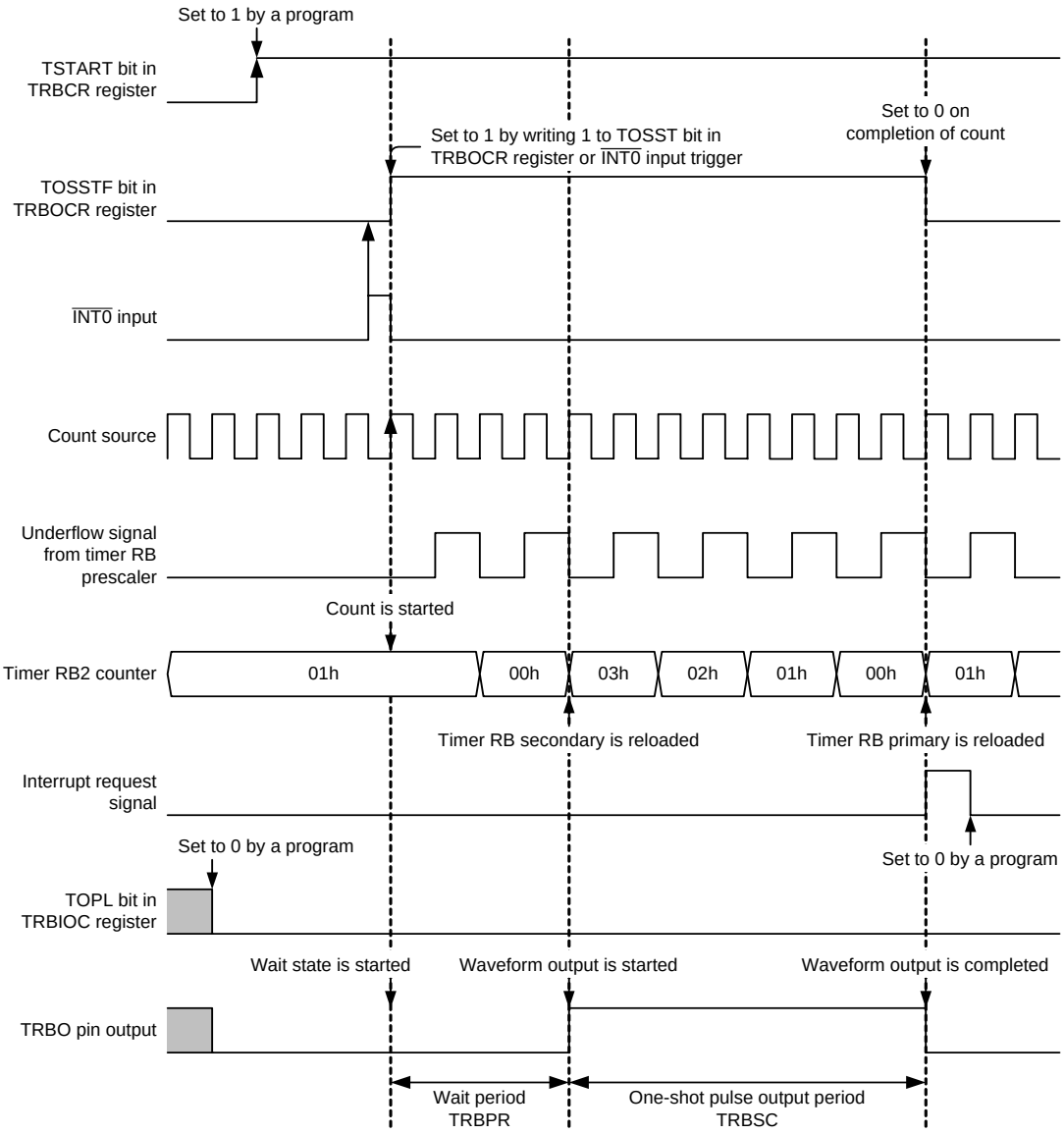
The actual count state must be monitored with the TCSTF bit in the TRBCR register.

An interrupt request is generated when timer RB2 underflows during the secondary period.

When registers TRBPRE and TRBPR are read, each count value is read. When registers TRBPRE, TRBPR, and TRBSC are written while the count is stopped, values are written to both the reload register and counter, respectively. When these registers are written during the count operation, values are written to the reload register and then transferred to the counter at the next reload operation.

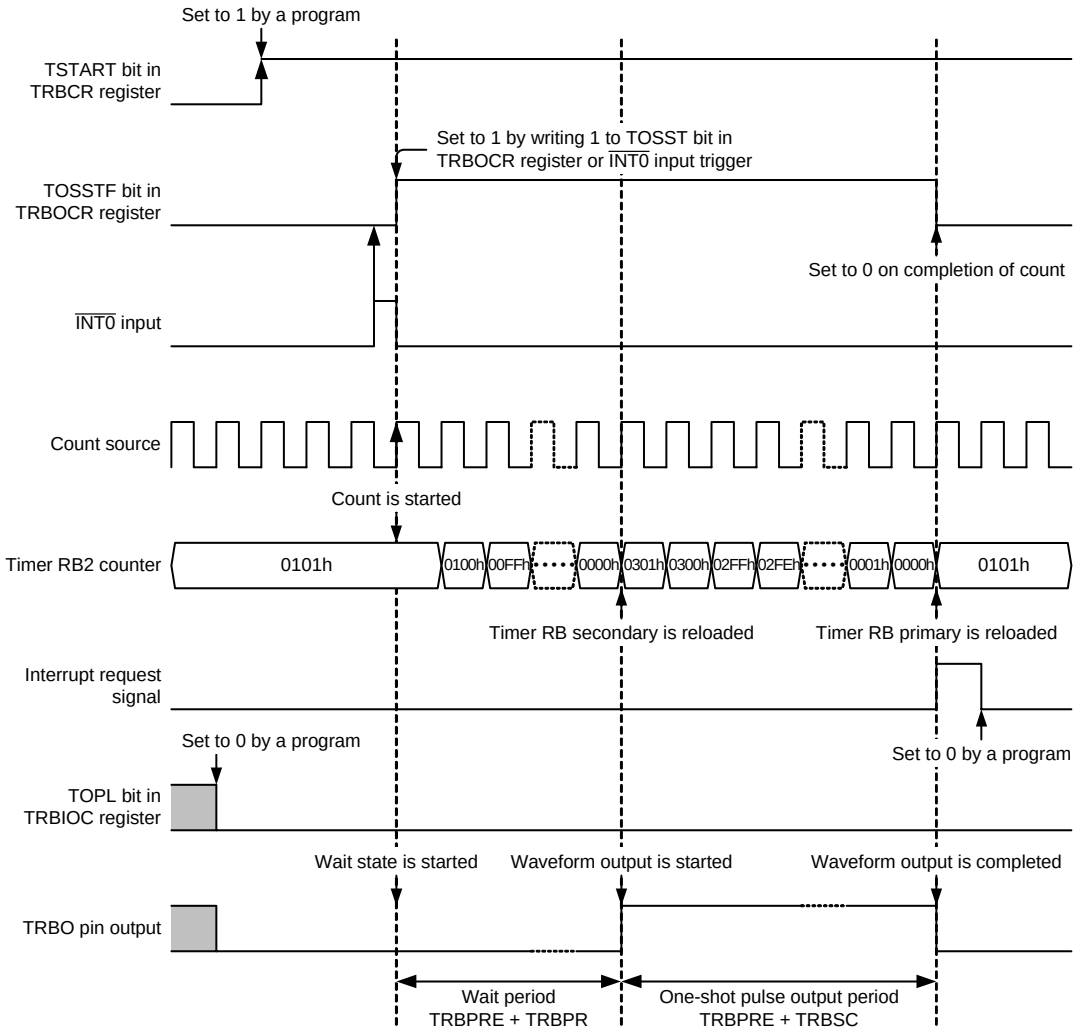
For the setting of trigger by the $\overline{\text{INT0}}$ input, see **14.7 $\overline{\text{INT0}}$ Input Trigger Selection**.

Figure 14.7 shows an Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Wait One-Shot Generation Mode. Figure 14.8 shows an Example of 16-Bit Timer Operation in Programmable Wait One-Shot Generation Mode.



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h, TRBSC register = 03h
- TOPL bit = 0, TOCNT bit = 0 (waveform output), INOSTG bit = 1 (one-shot trigger to INT0 pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TCNT16 bit in TRBMR register = 0 (8-bit timer with 8-bit prescaler)

Figure 14.7 Example of 8-Bit Timer with 8-Bit Prescaler Operation in Programmable Wait One-Shot Generation Mode



The above diagram applies under the following conditions:
- TRBPRE register = 01h, TRBPR register = 01h, TRBSC register = 03h
- TOPL bit = 0, TOCNT bit = 0 (waveform output),
  INOSTG bit = 1 (one-shot trigger to INT0 pin enabled), INOSEG bit = 1 (rising edge) in TRBIOC register
- TCNT16 bit in TRBMR register = 1 (16-bit timer)

Figure 14.8 Example of 16-Bit Timer Operation in Programmable Wait One-Shot Generation Mode

14.5 Selectable Functions

14.5.1 Configuration and Update Timing for Registers TRBPRE, TRBPR, and TRBSC

Registers TRBPRE, TRBPR, and TRBSC are configured with a master – reload register structure. Figure 14.9 shows the Configuration of Registers TRBPRE, TRBPR, and TRBSC. When the TSTART bit in the TRBCR register is set to 0 (count is stopped), values are updated to the reload registers immediately after the registers are written. However, when the TSTART bit is 1 (count is started), the timing for updating the reload registers differs in each mode. In the 8-bit timer with 8-bit prescaler, after the TRBPRE register is written, the TRBPRE register reload register is updated in synchronization with the count source.
Table 14.6 lists the Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler. Table 14.7 lists the Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer.

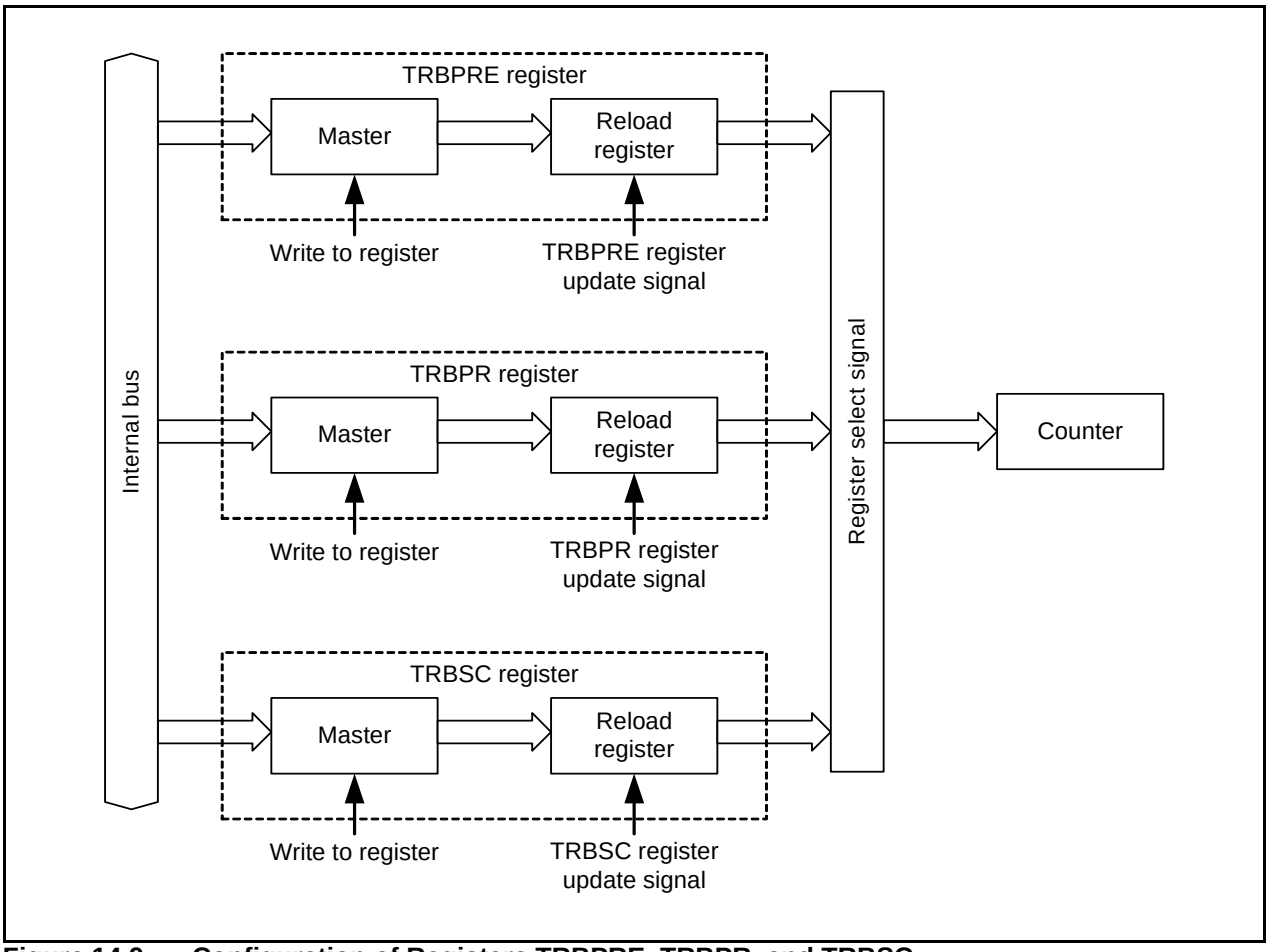


Figure 14.9 Configuration of Registers TRBPRE, TRBPR, and TRBSC

Table 14.6 Reload Register Update Timing for Registers TRBPR and TRBSC in 8-Bit Timer with 8-Bit Prescaler

Operating Mode		Update Timing (1)	
		TRBPR Register	TRBSC Register
Timer mode		Updated in synchronization with the prescaler underflow.	
Programmable waveform generation mode	TWRC = 1	Updated immediately before the end of the secondary output period after the TRBPR register is written.	
	TWRC = 0	Updated in synchronization with the prescaler underflow after the TRBPR register is written. (2)	
Programmable one-shot generation mode		Updated in synchronization with the prescaler underflow. (3)	
Programmable wait one-shot generation mode	TWRC = 1	Updated immediately before the end of the secondary output period after the TRBPR register is written.	
	TWRC = 0	Updated in synchronization with the prescaler underflow after the TRBPR register is written. (2)	

TWRC: Bit in the TRBMR register

Notes:
1. For details, see **14.5.2 Prescaler and Counter Using TWRC Bit**.
2. When the TWRC bit is 0 (write to reload register and counter) in programmable waveform and programmable wait one-shot generation modes, if the data in registers TRBSC and TRBPR is updated during count operation, the waveform is output for the updated period from that time.
3. When the TWRC bit is 0 (write to reload register and counter) in programmable one-shot generation mode, if the data in the TRBPR register is updated during count operation, the waveform is output for the updated period from that time.

Table 14.7 Reload Register Update Timing for Registers TRBPRE, TRBPR, and TRBSC in 16-Bit Timer

Operating Mode		Update Timing (1)	
		Registers TRBPRE and TRBPR	TRBSC Register
Timer mode		Updated in synchronization with the count source after the TRBPR register is written.	Updated in synchronization with the count source after the TRBSC register is written.
Programmable waveform generation mode	TWRC = 1	Updated immediately before the end of the secondary output period after the TRBPR register is written.	
	TWRC = 0	Updated in synchronization with the count source after the TRBPR register is written. (2)	
Programmable one-shot generation mode		Updated in synchronization with the count source after the TRBPR register is written.	Updated in synchronization with the count source after the TRBSC register is written. (3)
Programmable wait one-shot generation mode	TWRC = 1	Updated immediately before the end of the secondary output period after the TRBPR register is written.	
	TWRC = 0	Updated in synchronization with the count source after the TRBPR register is written. (2)	

TWRC: Bit in the TRBMR register

Notes:
1. For details, see **14.5.2 Prescaler and Counter Using TWRC Bit**.
2. When the TWRC bit is 0 (write to reload register and counter) in programmable waveform and programmable wait one-shot generation modes, if the data in registers TRBSC and TRBPR is updated during count operation, the waveform is output for the updated period from that time.
3. When the TWRC bit is 0 (write to reload register and counter) in programmable one-shot generation mode, if the data in the TRBPR register is updated during count operation, the waveform is output for the updated period from that time.

14.5.2 Prescaler and Counter Using TWRC Bit

In timer RB2, the TWRC bit in the TRBMR register can be used to select whether to write to the reload register only (TRBPR, TRBSC, TRBPRE) or both the reload register and counter. However, when the TCSTF bit in the TRBCR register is 0 (count is stopped), both the reload register and counter are written regardless of the setting of the TWRC bit.

In the 8-bit timer with 8-bit prescaler, when the TWRC bit is 0 (write to reload register and counter), transfer from the reload register to the prescaler is performed in synchronization with the count source, and transfer to the counter is performed in synchronization with prescaler underflows. Therefore, the count value is not updated immediately after the write instruction is executed. When the TWRC bit is 1 (write to reload register only), transfer from the reload register to the prescaler is performed in synchronization with prescaler underflows, and transfer to the counter is performed in synchronization with counter underflows. Only the value of the prescaler is updated before the counter underflows. Figures 14.10 and 14.11 show Examples of Prescaler and Counter Operation in 8-Bit Timer with 8-Bit Prescaler.

In the 16-bit timer, when the TWRC bit is 0 (write to reload register and counter), transfer to the 16-bit counter is performed in synchronization with the count source. When the TWRC bit is 1 (write to reload register only), transfer to the 16-bit counter is performed in synchronization with 16-bit counter underflows. Figures 14.12 and 14.13 show Examples of Counter Operation in 16-Bit Timer.

During programmable wait one-shot generation mode, when the TCSTF bit in the TRBCR register is 1 (count is in progress) and the TOSSTF bit in the TRBOCR register is 0 (one-shot is stopped), the reload register and counter can be written because the setting of the TWRC bit in the TRBMR register is invalid.

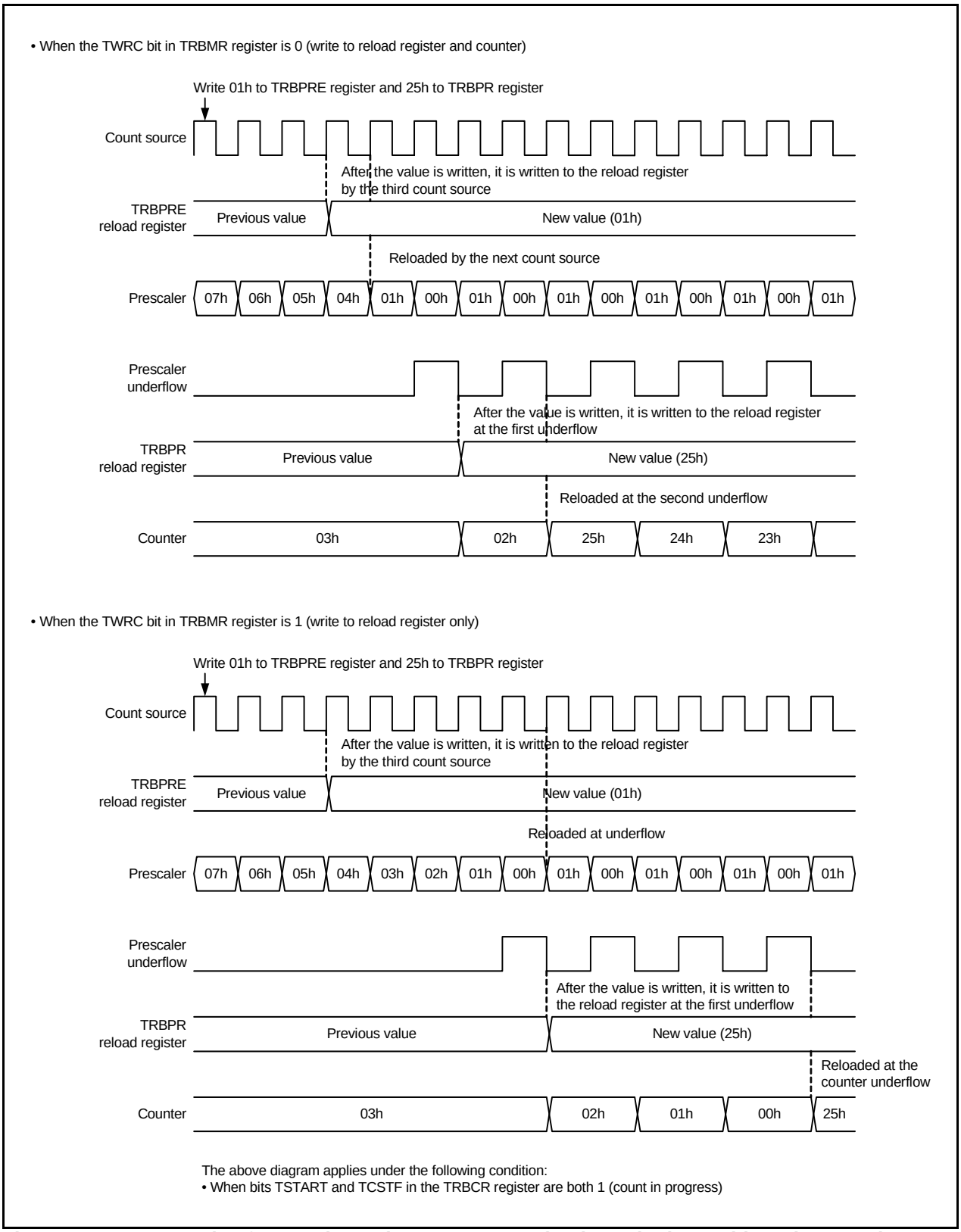


Figure 14.10 Example of Prescaler and Counter Operation in 8-Bit Timer with 8-Bit Prescaler (Timer Mode or Programmable One-Shot Generation Mode)

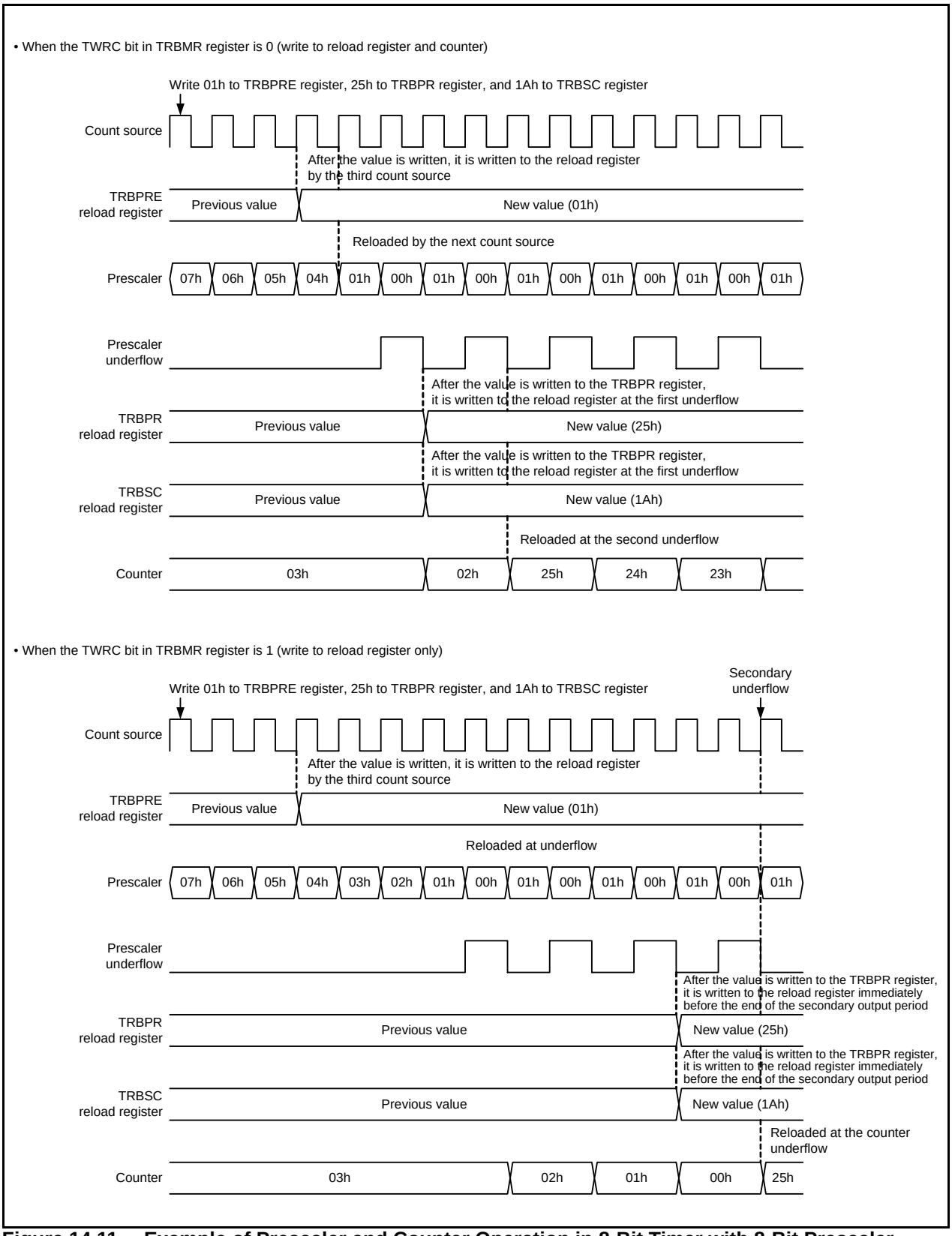


Figure 14.11 Example of Prescaler and Counter Operation in 8-Bit Timer with 8-Bit Prescaler (Programmable Waveform Generation Mode or Programmable Wait One-Shot Generation Mode)

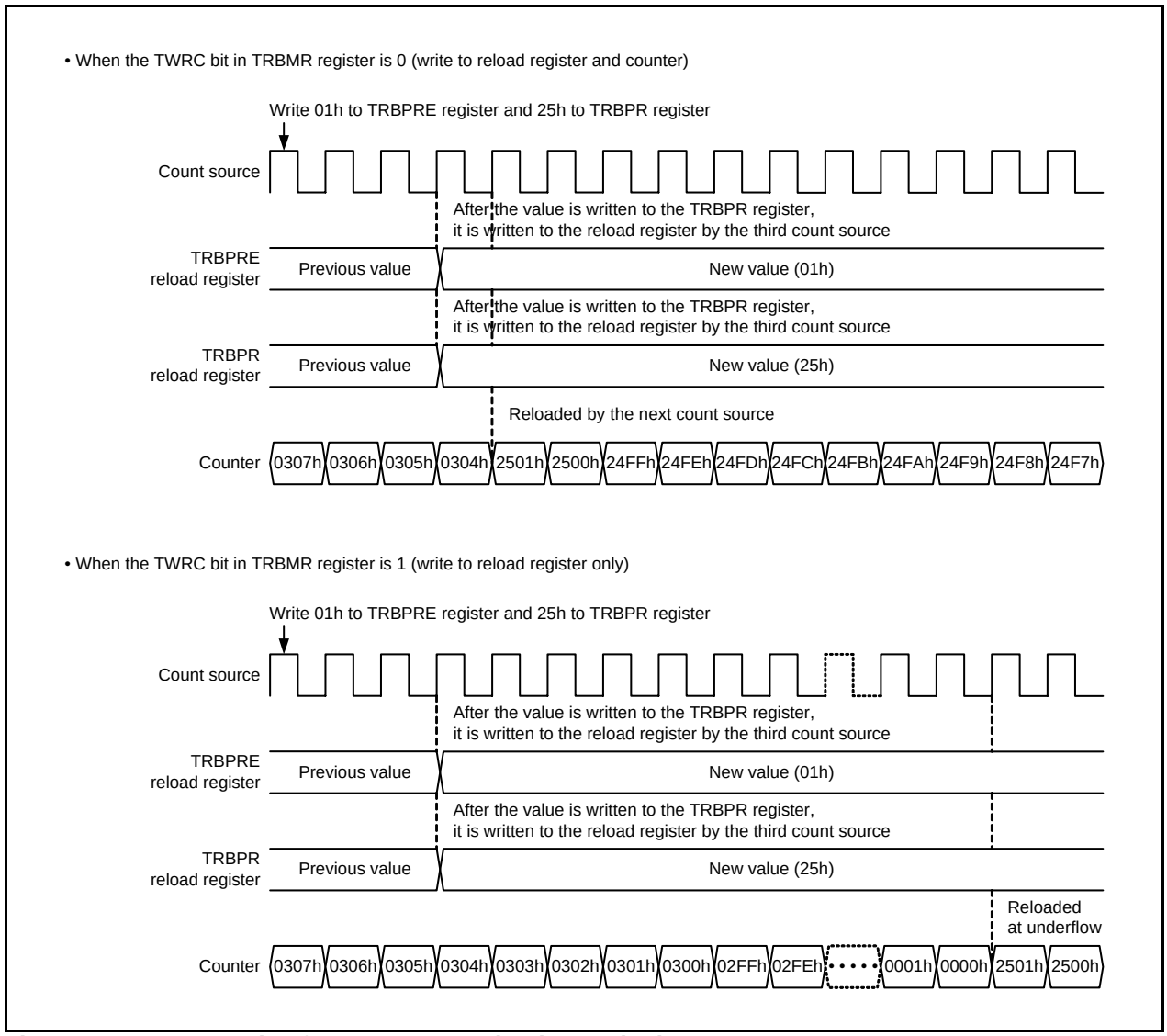


Figure 14.12 Example of Counter Operation in 16-Bit Timer (Timer Mode or Programmable One-Shot Generation Mode)

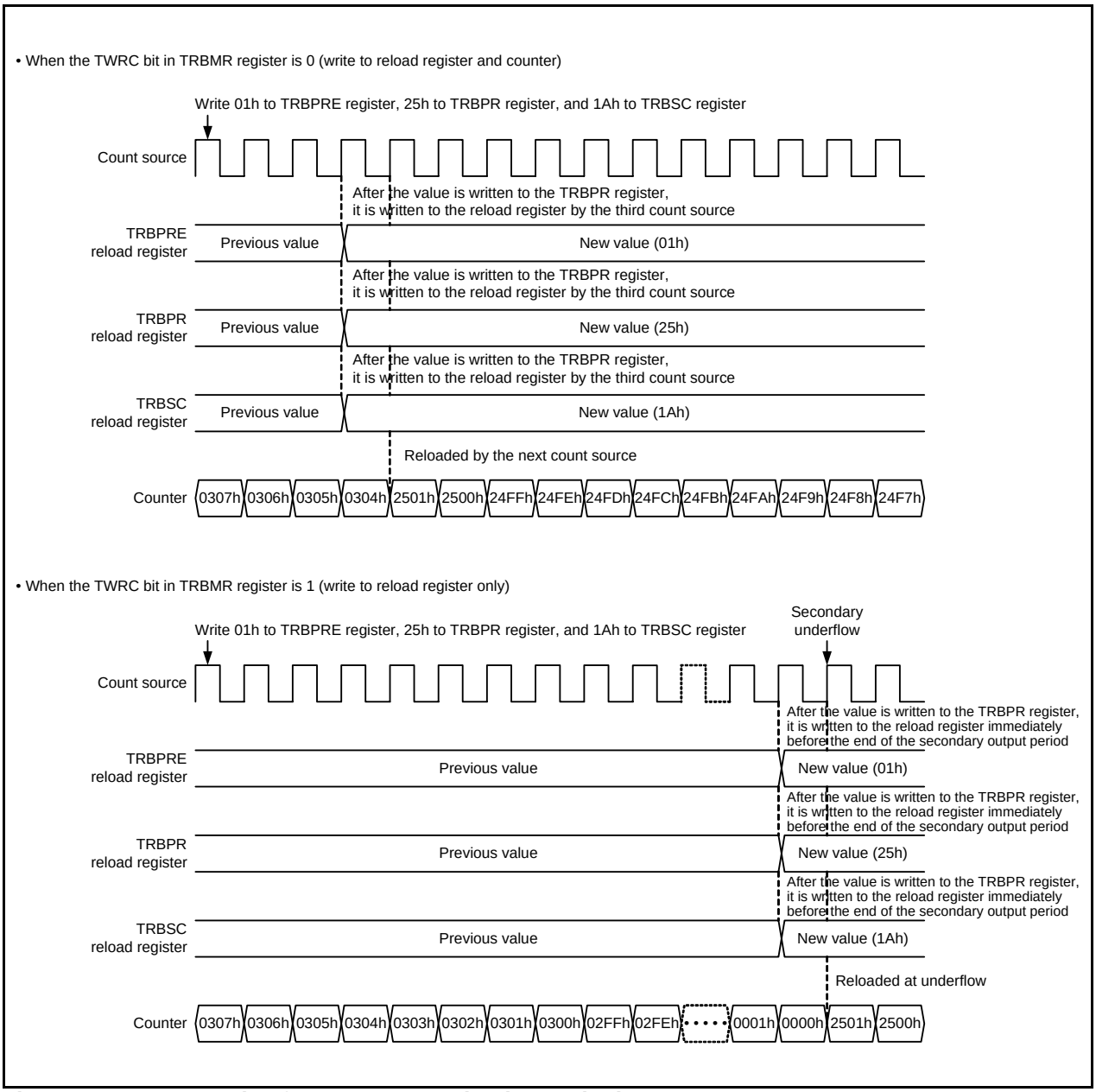


Figure 14.13 Example of Counter Operation in 16-Bit Timer (Programmable Waveform Generation Mode or Programmable Wait One-Shot Generation Mode)

14.5.3 TOCNT Bit Setting and Pin States

The TOCNT bit in the TRBIOC register can be used to select whether a timer waveform or fixed value is output. However, regardless of the setting of the TOCNT bit, an undefined value is output in timer mode and a waveform is output in programmable one-shot and programmable wait one-shot generation modes.
Table 14.8 lists the Output Data in Each Mode.

Table 14.8 Output Data in Each Mode

Operating Mode	Output Enabled/Disabled		Output Data
Timer mode	Output disabled		Undefined-value output
Programmable waveform generation mode	TCONT	0	Waveform output
		1	Fixed value (inverted value of TOPL)
Programmable one-shot generation mode	Output enabled		Waveform output
Programmable wait one-shot generation mode			

TOPL, TOCNT: Bits in TRBIOC register

If the TOCNT bit is rewritten in programmable waveform generation mode, the pin state is not changed immediately. The data is reflected in the pin state when one of the following conditions is met. Note that when the TOCNT bit is 1 (fixed-value output), the value, which is set for the primary period in the TOPL bit in the TRBIOC register, is output.

[Update conditions for pin states]
- When the TSTART bit in the TRBCR register is changed from 0 (count is stopped) to 1 (count is started).
- When the TRBPR register is reloaded to the counter.

14.6 Interrupt Request

When the TRBIF bit in the TRBIR register is 1 (interrupt requested) and the TRBIE bit is 1 (interrupt enabled), an interrupt request is generated to the CPU. The conditions for setting the TRBIF bit to 1 differ depending on the mode. See the descriptions of the TRBIF bit and individual modes.

14.7 $\overline{\text{INT0}}$ Input Trigger Selection

In programmable one-shot and programmable wait one-shot generation modes, when 1 (one-shot count is started) is written to the TOSST bit in the TRBCR register or a trigger is input to the $\overline{\text{INT0}}$ pin with the TCSTF bit in the TRBCR register set to 1 (count is in progress), one-shot operation is started.

When using the trigger input from the $\overline{\text{INT0}}$ pin, make the following settings beforehand.

(1) Set the port mapping register to set port P1_4 or P4_5 as the $\overline{\text{INT0}}$ pin.
(2) Set bits INT0F0 to INT0F1 in the INTF0 register to select the digital filter sampling clock for the $\overline{\text{INT0}}$ pin.
(3) Set the INT0EN bit in the INTEN register to 1 (enabled) to enable an interrupt.
(4) Set the INOSEG bit in the TRBIOC register to select the falling or rising edge.
(5) Set the INOSTG bit in the TRBIOC register to 1 (one-shot trigger to $\overline{\text{INT0}}$ pin enabled).

When an interrupt request is generated by the trigger input from the $\overline{\text{INT0}}$ pin, note the following:

- Set bits INT0SA to INT0SB in the ISCR0 register to select the falling edge, rising edge, or two-way edge for the interrupt.

Even if a one-shot trigger is generated while the TOSSTF bit in the TRBOCR is 1 (one-shot is operating (including wait period)), timer RB2 operation is not influenced, but the IRI0 bit in the IRR3 register is changed.
For details on interrupts, see **11. Interrupts**.

14.8 Notes on Timer RB2

- Timer RB2 stops counting after a reset. Start the count after setting the value in the timer and prescaler.
- In the 8-bit timer with 8-bit prescaler, even if the prescaler and timer are read in 16-bit units, they are actually read sequentially byte by byte in the MCU. This may cause the value in the timer to be updated during reading of these two registers.
  In the 16-bit timer, access the TRBPRE register first and then the TRBPR register. Read the TRBPRE register first to read the count value in the lower byte. The count value in the higher byte will be retained. Next, read the TRBPR register to read the retained value in the higher byte. The timer value is not updated during reading of these two registers.
- In programmable one-shot and programmable wait one-shot generation modes, when the TOSSP bit in the TRBOCR register is set to 1 and the one-shot is stopped, the timer reloads the reload register value and is stopped. The timer count value must be read before the timer is stopped.
- After 1 (count is started) is written to the TSTART bit in the TRBCR register while the count is stopped, the TCSTF bit in the TRBCR register remains 0 (count is stopped) for two to three cycles of the count source. Do not access the registers associated with timer RB2 (1) other than the TCSTF bit until this bit is set to 1 (count is in progress). The count is started on the first active edge of the counter source after the TCSTF bit is set to 1.
  After 0 (count is stopped) is written to the TSTART bit during count operation, the TCSTF bit remains 1 for two to three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RB2 (1) other than the TCSTF bit until this bit is set to 0.
  Note:
  1. Registers associated with timer RB2:
     TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBPR, and TRBSC
- In timer mode, do not set both the TRBPRE and TRBPR registers to 00h at the same time.
- When the TSTART bit in the TRBCR register is 0 (count is stopped), change the values of registers TRBPRE, TRBPR, and TRBSC, then wait for at least two cycles of the system clock (f) before setting the TSTART bit in the TRBCR register to 1 (count is started).
- When the TSTART bit in the TRBCR register is 1 (count is started) or the TCSTF bit is 1 (count is in progress), do not change the values in registers TRBIOC and TRBMR, and the TRBIE bit in the TRBIR register.
- Make sure the TCSTF bit in the TRBCR register is 1 (count is in progress) before writing 1 (one-shot count is started) to the TOSST bit in the TRBOCR register. When the TCSTF bit is 0 (count is stopped), writing 1 (one-shot count is started) to the TOSST bit is invalid.
- When writing to registers TRBPRE, TRBPR, and TRBSC during count operation (the TSTART bit is 1 or the TCSTF bit is 1), note the following points:
  - When writing to the TRBPRE register successively, allow at least three cycles of the count source for each write interval.
  - When writing to the TRBPR register successively, allow at least three cycles of the count source for each write interval.
  - When writing to the TRBSC register successively, allow at least three cycles of the count source for each write interval.
- When the TRBPR register is rewritten in programmable waveform generation mode, do not write to the TRBPRE, TRBPR, or TRBSC register during the secondary output period as described below after rewriting.
  - 8-bit timer with 8-bit prescaler:
    Two cycles of the prescaler underflow before the secondary output period ends.
  - 16-bit timer:
    Two cycles of the count source clock before the secondary output period ends.
- When the underflow signal from timer RJ2 is used as the count source for timer RB2, set timer RJ2 to timer mode, pulse output mode, or event counter mode.
- When 1 is written to the TOSST bit or the TOSSP bit in the TRBOCR register, the TOSSTF bit is changed after two to three cycles of the count source. If 1 is written to the TOSSP bit from when 1 is written to the TOSST bit until the TOSSTF bit is set to 1, the TOSSTF bit may be set to 0 or 1 depending on the internal state. Likewise, if 1 is written to the TOSST bit from when 1 is written to the TOSSP bit until the TOSSTF bit is set to 0, the TOSSTF may be set to 0 or 1 depending on the internal state.

- In programmable waveform generation mode and programmable wait one-shot mode, write to the TRBSC register before writing to the TRBPR register. At the underflow during the secondary period after the TRBPR register is written, the value written to the TRBPR register is transferred to the counter. If registers TRBPR and TRBSC are written two or more times after the TRBPR register is written until the underflow during the secondary period, the last written value is transferred to the counter at the underflow.
- When 1 is written to the TSTOP bit in the TRBCR register during count operation, timer RB2 is immediately stopped.
- If the count is forcibly stopped by writing 1 to the TSTOP bit during count operation, the TRBIF bit in the TRBIR register may be set to 1 (interrupt requested). Set the TRBIF bit to 0 (no interrupt requested) before restarting the count.
- When the TSTART bit in the TRBCR register is 0 (count is stopped), wait for at least two cycles of the system clock (f) after writing the values of registers TRBPRE and TRBPR before reading them.

15. Timer RC

Timer RC is a 16-bit timer that provides output compare and input capture functions and can count external events. It can be used as a multifunction timer with various applications such as generation of pulse output with an arbitrary duty cycle using the compare match between the timer RC counter and four general registers.

15.1 Overview

Table 15.1 lists the Timer RC Specifications. Table 15.2 lists the Timer RC Functions. Figure 15.1 shows the Timer RC Block Diagram. Table 15.3 lists Timer RC Pin Configuration.

Table 15.1 Timer RC Specifications

Item			Description
Count sources (counter input clocks)	Operating clock	Internal clock	• f1, f2, f4, f8, or f32: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 000b to 100b. • fHOCO: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 110b.
		External clock (external event count)	TRCCLK input: Selected when bits CKS2 to CKS0 in the TRCCR1 register are 101b.
Pulse I/O pins			4
General registers			4 • Can be set as output compare or input capture registers individually. • Can be used as buffer registers for output compare or input capture.
Operating modes		Timer mode	• Output compare function: Low-level, high-level, or toggle output can be performed. • Input capture function: A rising edge, falling edge, or two-way edge can be detected. • Counter clear function: A count period can be set.
		PWM mode	PWM output with up to three phases.
		PWM2 mode	Pulse output with an arbitrary period and duty.
Interrupt sources			• Compare match/input capture multiplexed interrupt × 4 sources • Overflow interrupt
Others			• The initial value of the timer RC output can be set arbitrarily. • A/D conversions triggered by compare matches in registers TRCGRA, TRCGRB, TRCGRC, and TRCGRD can be set.

Table 15.2 Timer RC Functions

Item		Counter	I/O Pin			
			TRCIOA	TRCIOB	TRCIOC	TRCIOD
General registers (output compare/input capture multiplexed registers)		Period setting with the TRCGRA register	TRCGRA register	TRCGRB register	TRCGRC register In buffer operation Buffer register for the TRCGRA register	TRCGRD register In buffer operation Buffer register for the TRCGRB register
Counter clear function		Input capture/ compare match for the TRCGRA register	Input capture/ compare match for the TRCGRA register	—	—	—
		TRCTRG input	—	—	—	—
Setting function for initial output level		—	Available	Available	Available	Available
Buffer operation		—	Available	Available	—	—
Compare match	Low-level output	—	Available	Available	Available	Available
	High-level output	—	Available	Available	Available	Available
	Toggle output	—	Available	Available	Available	Available
Input capture function		—	Available	Available	Available	Available
PWM mode		—	—	Available	Available	Available
PWM2 mode		—	—	Available	—	—
Interrupt sources		Overflow	Compare match/ input capture	Compare match/ input capture	Compare match/ input capture	Compare match/ input capture

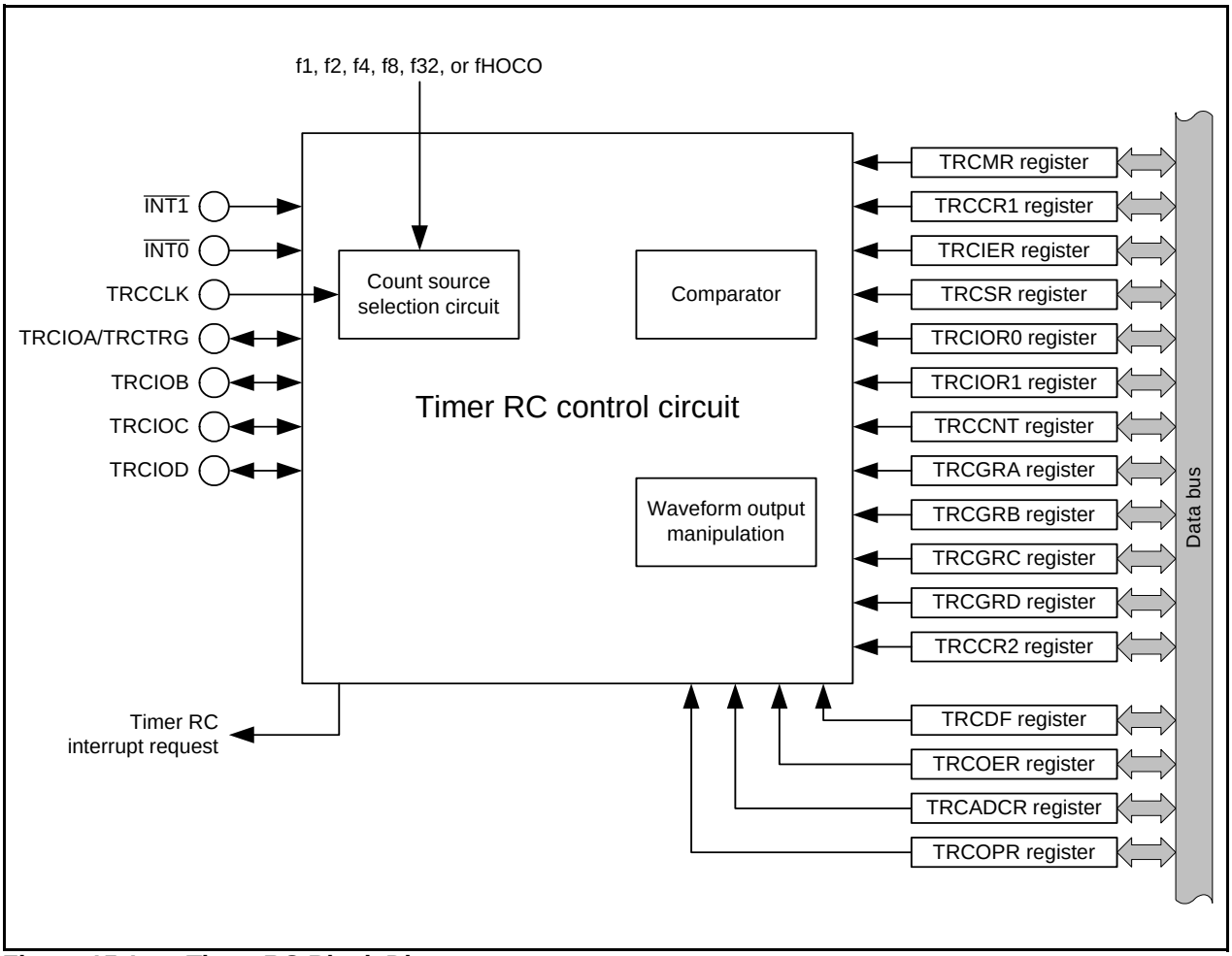


Figure 15.1 Timer RC Block Diagram

Table 15.3 Timer RC Pin Configuration

Pin Name	I/O	Function
TRCCLK	I	External clock input
TRCIOA/TRCTRG	I/O	TRCGRA output compare output/TRCGRA input capture input/external trigger input (TRCTRG)
TRCIOB	I/O	TRCGRB output compare output/TRCGRB input capture input/PWM output (in PWM mode)
TRCIOC	I/O	TRCGRC output compare output/TRCGRC input capture input/PWM output (in PWM mode)
TRCIOD	I/O	TRCGRD output compare output/TRCGRD input capture input/PWM output (in PWM mode)
$\overline{\text{INT0}}$	I	Timer output disabling control input
$\overline{\text{INT1}}$	I	Waveform output manipulation event input

15.2 Registers

Table 15.4 lists the Timer RC Register Configuration.

Table 15.4 Timer RC Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RC Counter	TRCCNT	00h	000E8h	16
		00h	000E9h	
Timer RC General Register A	TRCGRA	FFh	000EAh	16
		FFh	000EBh	
Timer RC General Register B	TRCGRB	FFh	000ECh	16
		FFh	000EDh	
Timer RC General Register C	TRCGRC	FFh	000EEh	16
		FFh	000EFh	
Timer RC General Register D	TRCGRD	FFh	000F0h	16
		FFh	000F1h	
Timer RC Mode Register	TRCMR	01001000b	000F2h	8
Timer RC Control Register 1	TRCCR1	00h	000F3h	8
Timer RC Interrupt Enable Register	TRCIER	01110000b	000F4h	8
Timer RC Status Register	TRCSR	01110000b	000F5h	8
Timer RC I/O Control Register 0	TRCIOR0	10001000b	000F6h	8
Timer RC I/O Control Register 1	TRCIOR1	10001000b	000F7h	8
Timer RC Control Register 2	TRCCR2	00011000b	000F8h	8
Timer RC Digital Filter Function Select Register	TRCDF	00h	000F9h	8
Timer RC Output Enable Register	TRCOER	01111111b	000FAh	8
Timer RC A/D Conversion Trigger Control Register	TRCADCR	11110000b	000FBh	8
Timer RC Waveform Output Manipulation Register	TRCOPR	00h	000FCh	8

15.2.1 Timer RC Counter (TRCCNT)

Address 000E8h to 000E9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	16-bit readable/writable up counter. When this counter overflows, the OVF bit in the TRCSR register is set to 1. If the OVIE bit in the TRCIER register is set to 1 (interrupt request (FOVI) by OVF bit is enabled) at this time, an interrupt request is generated.	0000h to FFFFh	R/W

The count source for the TRCCNT register is selected by bits CKS0 to CKS2 in the TRCCR1 register. When the CCLR bit in the TRCCR1 register is 1, the TRCCNT register is cleared to 0000h when a compare match with the TRCGRA register occurs.

TRCCNT register must be accessed in 16-bit units. Do not access this register in 8-bit units. When this register is accessed as 16-bit units, it is accessed twice in 8-bit units.

15.2.2 Timer RC General Register A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, and TRCGRD)

Address 000EAh to 000EBh (TRCGRA), 000ECh to 000EDh (TRCGRB), 000EEh to 000EFh (TRCGRC), 000F0h to 000F1h (TRCGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Table 15.5 Functions of TRCGRj Register when Using Input Capture Function

Register	Setting	Register Function	Input Capture Input Pin
TRCGRA	—	General register. Can be used to read the TRC register value at input capture.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BUFEA = 0	General register. Can be used to read the TRC register value at input capture.	TRCIOC
TRCGRD	BUFEB = 0		TRCIOD
TRCGRC	BUFEA = 1	Buffer registers. Can be used to hold transferred value from the general register. (Refer to **15.5.5 Buffer Operation Timing**.)	TRCIOA
TRCGRD	BUFEB = 1		TRCIOB

j = A, B, C, or D
BUFEA, BUFEB: Bits in TRCMR register

Table 15.6 Functions of TRCGRj Register when Using Output Compare Function

Register	Setting	Register Function	Output Compare Output Pin
TRCGRA	—	General register. Write a compare value to one of these registers.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BUFEA = 0	General register. Write a compare value to one of these registers.	TRCIOC
TRCGRD	BUFEB = 0		TRCIOD
TRCGRC	BUFEA = 1	Buffer register. Write the next compare value to one of these registers. (Refer to **15.5.5 Buffer Operation Timing**.)	TRCIOA
TRCGRD	BUFEB = 1		TRCIOB

j = A, B, C, or D
BUFEA, BUFEB: Bits in TRCMR register

Table 15.7 Functions of TRCGRh Register in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRCGRA	—	General register. Set the PWM period.	—
TRCGRB	—	General register. Set the PWM output change point.	TRCIOB
TRCGRC	BUFEA = 0	General register. Set the PWM output change point.	TRCIOC
TRCGRD	BUFEB = 0		TRCIOD
TRCGRC	BUFEA = 1	Buffer register. Set the next PWM period. (Refer to **15.5.5 Buffer Operation Timing**.)	—
TRCGRD	BUFEB = 1	Buffer register. Set the next PWM output change point. (Refer to **15.5.5 Buffer Operation Timing**.)	TRCIOB

h = A, B, C, or D
BUFEA, BUFEB: Bits in TRCMR register
Note:
1. The output level does not change even when a compare match occurs if the TRCGRA register value (PWM period) is the same as the TRCGRB, TRCGRC, or TRCGRD register value.

Table 15.8 Functions of TRCGRj Register in PWM2 Mode

Register	Setting	Register Function	PWM2 Output Pin
TRCGRA	—	General register. Set the PWM period.	TRCIOB pin
TRCGRB (1)	—	General register. Set the PWM output change point.	
TRCGRC (1)	BUFEA = 0	General register. Set the PWM output change point (wait time after trigger).	
TRCGRD	BUFEB = 0	(Not used in PWM2 mode)	—
TRCGRD	BUFEB = 1	Buffer register. Set the next PWM output change point. (Refer to **15.5.5 Buffer Operation Timing**.)	TRCIOB pin

j = A, B, C, or D
BUFEA, BUFEB: Bits in TRCMR register
Note:
1. Do not set the TRCGRB and TRCGRC registers to the same value.

15.2.3 Timer RC Mode Register (TRCMR)

Address 000F2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CTS	—	BUFEB	BUFEA	PWM2	PWMD	PWMC	PWMB
After Reset	0	1	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB	TRCIOB PWM mode select bit (1)	0: Timer mode 1: PWM mode	R/W
b1	PWMC	TRCIOC PWM mode select bit (1)		R/W
b2	PWMD	TRCIOD PWM mode select bit (1)		R/W
b3	PWM2	PWM2 mode select bit	0: PWM2 mode 1: Timer mode or PWM mode	R/W
b4	BUFEA	TRCGRC register function select bit (2)	0: Output compare or input capture register 1: TRCGRC register is used as a buffer register for TRCGRA register	R/W
b5	BUFEB	TRCGRD register function select bit	0: Output compare or input capture register 1: TRCGRD register is used as a buffer register for TRCGRB register	R/W
b6	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b7	CTS	TRCCNT count start bit	0: Count is stopped 1: Count is started	R/W

Notes:
1. These bits are enabled when the PWM2 bit is 1 (timer mode or PWM mode).
2. Set the BUFEA bit to 0 (general register) in PWM2 mode.

CTS Bit (TRCCNT count start bit)

[Conditions for setting to 0]
- When 0 is written to this bit.
- When a compare match occurs while the CSTP bit in the TRCCR2 register is 1 (count is stopped) in PWM2 mode.

[Condition for setting to 1]
- When 1 is written to this bit.

15.2.4 Timer RC Control Register 1 (TRCCR1)

Address 000F3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	CKS2	CKS1	CKS0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	Timer output level select A bit	0: Output value 0 (1) 1: Output value 1 (1)	R/W
b1	TOB	Timer output level select B bit		R/W
b2	TOC	Timer output level select C bit		R/W
b3	TOD	Timer output level select D bit		R/W
b4	CKS0	Count source select bits	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: Falling edge of TRCCLK input (3) 1 1 0: fHOCO (2) 1 1 1: Do not set.	R/W
b5	CKS1			R/W
b6	CKS2			R/W
b7	CCLR	TRCCNT counter clear select bit	0: Clear disabled (free-running operation) 1: TRCCNT counter is cleared by input capture/compare match A	R/W

Notes:
1. The values set by bits TOA to TOD are reflected immediately after they are changed. Set the value when the CTS bit in the TRCMR register is 0 (count is stopped).
2. When selecting fHOCO, set these bits with the on-chip oscillator operating. When switching the count sources, set these bits with the counter stopped.
3. The pulse width of an external clock input to TRCCLK must be three or more cycles of the operating clock.

TOA Bit (Timer output level select A bit)

This bit is used to set the output value from the TRCIOA pin until the first compare match A occurs. In PWM mode, this bit is used to control the output level of the TRCIOA pin.

TOB Bit (Timer output level select B bit)

This bit is used to set the output value from the TRCIOB pin until the first compare match B occurs. In PWM mode, this bit is used to control the output level of the TRCIOB pin.

TOC Bit (Timer output level select C bit)

This bit is used to set the output value from the TRCIOC pin until the first compare match C occurs. In PWM mode, this bit is used to control the output level of the TRCIOC pin.

TOD Bit (Timer output level select D bit)

This bit is used to set the output value from the TRCIOD pin until the first compare match D occurs. In PWM mode, this bit is used to control the output level of the TRCIOD pin.

15.2.5 Timer RC Interrupt Enable Register (TRCIER)

Address 000F4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVIE	—	—	—	IMIED	IMIEC	IMIEB	IMIEA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match A interrupt enable bit	0: Interrupt request (IMIA) by IMFA bit in TRCSR register is disabled 1: Interrupt request (IMIA) by IMFA bit in TRCSR register is enabled	R/W
b1	IMIEB	Input capture/compare match B interrupt enable bit	0: Interrupt request (IMIB) by IMFB bit in TRCSR register is disabled 1: Interrupt request (IMIB) by IMFB bit in TRCSR register is enabled	R/W
b2	IMIEC	Input capture/compare match C interrupt enable bit	0: Interrupt request (IMIC) by IMFC bit in TRCSR register is disabled 1: Interrupt request (IMIC) by IMFC bit in TRCSR register is enabled	R/W
b3	IMIED	Input capture/compare match D interrupt enable bit	0: Interrupt request (IMID) by IMFD bit in TRCSR register is disabled 1: Interrupt request (IMID) by IMFD bit in TRCSR register is enabled	R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	OVIE	Timer overflow interrupt enable bit	0: Interrupt request (FOVI) by OVF bit in TRCSR register is disabled 1: Interrupt request (FOVI) by OVF bit in TRCSR register is enabled	R/W

15.2.6 Timer RC Status Register (TRCSR)

Address 000F5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match A flag	[Condition for setting to 0] • When 0 is written to this bit after reading it as 1. (1) [Condition for setting to 1] • See **Table 15.9 Conditions for Setting Each Flag to 1**.	R/W
b1	IMFB	Input capture/compare match B flag		R/W
b2	IMFC	Input capture/compare match C flag		R/W
b3	IMFD	Input capture/compare match D flag		R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	OVF	Timer overflow flag	[Condition for setting to 0] • When 0 is written to this bit after reading it as 1. [Condition for setting to 1] • See **Table 15.9 Conditions for Setting Each Flag to 1**.	R/W

Note:
1. The results of writing this bit are as follows.
   - If the result of reading this bit is 1, writing 0 to this bit will set it to 0.
   - If the result of reading this bit is 0, writing 0 to this bit will not change its value. (If this bit changes from 0 to 1 after the read, the bit will remain 1 even if 0 is written.)
   - Writing 1 has no effect.

Table 15.9 Conditions for Setting Each Flag to 1

Symbol	Timer Mode		PWM Mode	PWM2 Mode
	Input Capture Function	Output Compare Function		
IMFA	When the value in the TRCCNT register is transferred to the TRCGRA register on the input edge (1) of the TRCIOA pin.	When the values in registers TRCCNT and TRCGRA match.		
IMFB	When the value in the TRCCNT register is transferred to the TRCGRB register on the input edge (1) of the TRCIOB pin.	When the values in registers TRCCNT and TRCGRB match.		
IMFC	When the value in the TRCCNT register is transferred to the TRCGRC register on the input edge (1) of the TRCIOC pin.	When the values in registers TRCCNT and TRCGRC match. (2)		
IMFD	When the value in the TRCCNT register is transferred to the TRCGRD register on the input edge (1) of the TRCIOD pin.	When the values in registers TRCCNT and TRCGRD match. (2)		
OVF	When the TRCCNT register overflows from FFFFh to 0000h.			

Notes:
1. The edge is selected by bits IOj0 to IOj1 (j = A, B, C, or D) in registers TRCIO0 and TRCIOR1. However, all of bits IOA2 and IOB2 in the TRCIOR0 register and bits IOC2 and IOD2 in the TRCIOR1 register must be set to 1 (input capture function).
2. Includes when bits BUFEA and BUFEB in the TRCMR register are 1 (buffer registers for TRCGRA and TRCGRB).

15.2.7 Timer RC I/O Control Register 0 (TRCIOR0)

Address 000F6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control A0 bit	[IOA2 = 0 (output compare function)]	R/W
b1	IOA1	TRCGRA control A1 bit	b1 b0 0 0: Pin output by compare match A is disabled 0 1: Low-level output from TRCIOA pin at compare match A 1 0: High-level output from TRCIOA pin at compare match A 1 1: Toggle output from TRCIOA pin at compare match A [IOA2 = 1 (input capture function)] b1 b0 0 0: Rising edge on TRCIOA pin 0 1: Falling edge on TRCIOA pin 1 0: Two-way edge on TRCIOA pin 1 1: Do not set.	R/W
b2	IOA2	TRCGRA control A2 bit (1)	0: Output compare function 1: Input capture function	R/W
b3	—	Reserved	Set to 1.	R/W
b4	IOB0	TRCGRB control B0 bit	[IOB2 = 0 (output compare function)]	R/W
b5	IOB1	TRCGRB control B1 bit	b5 b4 0 0: Pin output by compare match B is disabled 0 1: Low-level output from TRCIOB pin at compare match B 1 0: High-level output from TRCIOB pin at compare match B 1 1: Toggle output from TRCIOB pin at compare match B [IOB2 = 1 (input capture function)] b5 b4 0 0: Rising edge on TRCIOB pin 0 1: Falling edge on TRCIOB pin 1 0: Two-way edge on TRCIOA pin 1 1: Do not set.	R/W
b6	IOB2	TRCGRB control B2 bit (1)	0: Output compare function 1: Input capture function	R/W
b7	—	Nothing is assigned. The write value must be 1. The read value is 1.		—

Note:
1. When bits BUFEA and BUFEB in the TRCMR register are set to 1, registers TRCGRA and TRCGRC, and registers TRCGRB and TRCGRD are paired. The same values must be set in the IOA2 bit and the IOC2 bit in the TRCIOR1 register, and in the IOB2 bit and the IOD2 bit in the TRCIOR1 register, respectively.

The setting of the TRCIOR0 register is invalid in PWM and PWM2 modes.

15.2.8 Timer RC I/O Control Register 1 (TRCIOR1)

Address 000F7h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control C0 bit	[IOC2 = 0, IOC3 = 0 (output from TRCIOA pin at compare match C)] (1, 2) b1 b0 0 0: Pin output by compare match C is disabled 0 1: Low-level output from TRCIOA pin at compare match C 1 0: High-level output from TRCIOA pin at compare match C 1 1: Toggle output from TRCIOA pin at compare match C [IOC2 = 0, IOC3 = 1 (output from TRCIOC pin at compare match C)] (1) b1 b0 0 0: Pin output by compare match C is disabled 0 1: Low-level output from TRCIOC pin at compare match C 1 0: High-level output from TRCIOC pin at compare match C 1 1: Toggle output from TRCIOC pin at compare match C [IOC2 = 1, IOC3 = 1 (TRCIOC input edge selected at input capture C)] (3) b1 b0 0 0: Input capture C occurs on the rising edge of TRCIOC input 0 1: Input capture C occurs on the falling edge of TRCIOC input 1 0: Input capture C occurs on the two-way edge of TRCIOC input 1 1: Do not set.	R/W
b1	IOC1	TRCGRC control C1 bit		R/W
b2	IOC2	TRCGRC control C2 bit (4)	0: Output compare function 1: Input capture function	R/W
b3	IOC3	TRCGRC control C3 bit	0: Output from TRCIOA pin at compare match C (8) 1: Output from TRCIOC pin at compare match C	R/W
b4	IOD0	TRCGRD control D0 bit	[IOD2 = 0, IOD3 = 0 (output from TRCIOB pin at compare match D)] (5, 6) b5 b4 0 0: Pin output by compare match D is disabled 0 1: Low-level output from TRCIOB pin at compare match D 1 0: High-level output from TRCIOB pin at compare match D 1 1: Toggle output from TRCIOB pin at compare match D [IOD2 = 0, IOD3 = 1 (output from TRCIOD pin at compare match D)] (5) b5 b4 0 0: Pin output by compare match D is disabled 0 1: Low-level output from TRCIOD pin at compare match D 1 0: High-level output from TRCIOD pin at compare match D 1 1: Toggle output from TRCIOD pin at compare match D [IOD2 = 1, IOD3 = 1 (TRCIOD input edge selected at input capture D)] (7) b5 b4 0 0: Input capture D occurs on the rising edge of TRCIOD input 0 1: Input capture D occurs on the falling edge of TRCIOD input 1 0: Input capture D occurs on the two-way edge of TRCIOD input 1 1: Do not set.	R/W
b5	IOD1	TRCGRD control D1 bit		R/W
b6	IOD2	TRCGRD control D2 bit (4)	0: Output compare function 1: Input capture function	R/W
b7	IOD3	TRCGRD control D3 bit	0: Output from TRCIOB pin at compare match D 1: Output from TRCIOD pin at compare match D	R/W

Notes:
1. When the BUFEA bit in the TRCMR register is 1 (TRCGRC register is used as a buffer register for TRCGRA register), the value of the TRCGRC register is transferred to the TRCGRA register at compare match A.
2. When the IOA2 bit in the TRCIOR0 register is 0 (output compare function), if compare matches A and C occur simultaneously, the output from the TRCIOA pin at compare match C takes precedence.
3. When the BUFEA bit is 1 (TRCGRC register is used as a buffer register for TRCGRA register), the value of the TRCGRA register is transferred to the TRCGRC register at input capture A. When the input capture edge of the TRCIOC pin selected by bits IOC0 to IOC1 is input, the IMFC bit in the TRCSR register is set to 1. However, the count value is not transferred to the TRCGRC register.

4. In buffer operation, registers TRCGRA and TRCGRC, and registers TRCGRB and TRCGRD are paired. The same values must be set in the IOC2 bit and the IOA2 bit in the TRCIOR0 register, and in the IOD2 bit and the IOB2 bit in the TRCIOR0 register, respectively.
5. When the BUFEB bit in the TRCMR register is 1 (TRCGRD register is used as a buffer register for TRCGRB register), the value of the TRCGRD register is transferred to the TRCGRB register at compare match B.
6. When the IOB2 bit in the TRCIOR0 register is 0 (output compare function), if compare matches B and D occur simultaneously, the output from the TRCIOB pin at compare match D takes precedence.
7. When the BUFEB bit is 1 (TRCGRD register is used as a buffer register for TRCGRB register), the value of the TRCGRB register is transferred to the TRCGRD register at input capture B. When the input capture edge of the TRCIOD pin selected by bits IOD0 to IOD1 is input, the IMFD bit in the TRCSR register is set to 1. However, the count value is not transferred to the TRCGRD register.
8. When IOC2 = 1, do not set the IOC3 bit to 0.
   When IOD2 = 1, do not set the IOD3 bit to 0.

The setting of the TRCIOR1 register is invalid in PWM and PWM2 modes.

15.2.9 Timer RC Control Register 2 (TRCCR2)

Address 000F8h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSTP	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	TRCIOB PWM mode output level control bit (1)	0: Output level is active low 1: Output level is active high	R/W
b1	POLC	TRCIOC PWM mode output level control bit (1)		R/W
b2	POLD	TRCIOD PWM mode output level control bit (1)		R/W
b3	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b4	—			
b5	CSTP	Count stop bit (2)	0: Count is continued even after compare match with TRCGRA register 1: Count is stopped at compare match with TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bits (3)	b7 b6 0 0: TRCTRG input disabled 0 1: Rising edge 1 0: Falling edge 1 1: Both rising and falling edges	R/W
b7	TCEG1			R/W

Notes:
1. Enabled in PWM mode.
2. Enabled in the output compare function, PWM mode, and PWM2 mode. For notes on PWM2 mode, see **15.7.6 TRCMR Register in PWM2 Mode**.
3. Enabled in PWM2 mode.

15.2.10 Timer RC Digital Filter Function Select Register (TRCDF)

Address 000F9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA digital filter function bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB digital filter function bit (1)		R/W
b2	DFC	TRCIOC digital filter function bit (1)		R/W
b3	DFD	TRCIOD digital filter function bit (1)		R/W
b4	DFTRG	TRCTRG digital filter function bit (2)		R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	DFCK0	Digital filter clock select bits (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits CKS2 to CKS0 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

Notes:
1. Enabled in the input capture function.
2. Enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

15.2.11 Timer RC Output Enable Register (TRCOER)

Address 000FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	ED	EC	EB	EA
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA	TRCIOA output disable bit (3)	[When the OPE bit in the TRCOPR register is 0 (waveform output manipulation disabled)] (1) 0: Output enabled (dependent on settings of registers TRCMR and TRCIOR0) 1: Output disabled (independent of settings of registers TRCMR and TRCIOR0) [When the OPE bit in the TRCOPR register is 1 (waveform output manipulation enabled)] (2) 0: Output enabled (dependent on settings of registers TRCMR and TRCIOR0) 1: Output level is fixed or high impedance depending on TRCOPR register setting	R/W
b1	EB	TRCIOB output disable bit (3)		R/W
b2	EC	TRCIOC output disable bit (3)	[When the OPE bit in the TRCOPR register is 0 (waveform output manipulation disabled)] (1) 0: Output enabled (dependent on settings of registers TRCMR and TRCIOR1) 1: Output disabled (independent of settings of registers TRCMR and TRCIOR1) [When the OPE bit in the TRCOPR register is 1 (waveform output manipulation enabled)] (2) 0: Output enabled (dependent on settings of registers TRCMR and TRCIOR1) 1: Output level is fixed or high impedance depending on TRCOPR register setting	R/W
b3	ED	TRCIOD output disable bit (3)		R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	PTO	Timer output disable bit	[When the OPE bit in the TRCOPR register is 0 (waveform output manipulation disabled)] 0: Bits EA to ED do not change even if a low level is input to the $\overline{\text{INT0}}$ pin 1: When a low level is input to the $\overline{\text{INT0}}$ pin, bits EA to ED are set to 1 (output disabled) (For $\overline{\text{INT0}}$, see **11. Interrupts**.) [When the OPE bit in the TRCOPR register is 1 (waveform output manipulation enabled)] The function of the PTO bit is disabled (bits EA to ED do not change even if a low level is input to the $\overline{\text{INT0}}$ pin). This bit can be read or written.	R/W

Notes:
1. Bits EA to ED can be set by software. When the PTO bit is 1 and a low level is input to the $\overline{\text{INT0}}$ pin, bits EA to ED are set to 1 (output disabled)).
2. Regardless of the set value of the PTO bit, bits EA to ED do not change even if a low level is input to the $\overline{\text{INT0}}$ pin.
   When the RESTATS bit in the TRCOPR register is 1, bits EA to ED cannot be set by software. When the waveform output manipulation event selected by bits OPSEL0 to OPSEL1 in the TRCOPR register is input, bits EA to ED are set to 1. If the waveform output manipulation event is cancelled, bits EA to ED are set to 0.
   When the RESTATS bit is 0, bits EA to ED can be set by software. When the waveform output manipulation event selected by bits OPSEL0 to OPSEL1 is input, bits EA to ED are set to 1. However, bits EA to ED are not automatically set to 0 even if the waveform output manipulation event is cancelled. Set these bits to 0 by software.
3. Disabled when the corresponding pin is used as input capture input.

15.2.12 Timer RC A/D Conversion Trigger Control Register (TRCADCR)

Address 000FBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	ADTRGDE	ADTRGCE	ADTRGBE	ADTRGAE
After Reset	1	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADTRGAE	TRCGRA A/D conversion start trigger enable bit	0: No A/D conversion start trigger occurs at compare match A 1: An A/D conversion start trigger occurs at compare match A	R/W
b1	ADTRGBE	TRCGRB A/D conversion start trigger enable bit	0: No A/D conversion start trigger occurs at compare match B 1: An A/D conversion start trigger occurs at compare match B	R/W
b2	ADTRGCE	TRCGRC A/D conversion start trigger enable bit	0: No A/D conversion start trigger occurs at compare match C 1: An A/D conversion start trigger occurs at compare match C	R/W
b3	ADTRGDE	TRCGRD A/D conversion start trigger enable bit	0: No A/D conversion start trigger occurs at compare match D 1: An A/D conversion start trigger occurs at compare match D	R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	—			

15.2.13 Timer RC Waveform Output Manipulation Register (TRCOPR)

Address 000FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	OPE	RESTATS	OPOL1	OPOL0	OPSEL1	OPSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OPSEL0	Waveform output manipulation event select bits (1)	b1 b0 0 0: Waveform output is manipulated during low-level period of comparator B1 (VCOUT1) output level 0 1: Waveform output is manipulated during low-level period of INT1 input level Other than the above: Waveform output is manipulated during low-level period of comparator B1 (VCOUT1) output level or INT1 input level	R/W
b1	OPSEL1			R/W
b2	OPOL0	Waveform output manipulation period output level select bits	b3 b2 0 0: When timer RC pin is pulled down, timer RC output level is fixed to high impedance during waveform output manipulation period 0 1: When timer RC pin is pulled up, timer RC output level is fixed to high impedance during waveform output manipulation period 1 0: Timer RC output level is fixed at low during waveform output manipulation period 1 1: Timer RC output level is fixed at high during waveform output manipulation period	R/W
b3	OPOL1			R/W
b4	RESTATS	Restart method select bit (2)	0: Output is restarted by software (3) 1: Output is automatically restarted (4)	R/W
b5	OPE	Waveform output manipulation enable bit (5)	0: Waveform output manipulation disabled 1: Waveform output manipulation enabled	R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

Notes:
1. When the OPE bit is 1 (waveform output manipulation enabled), bits EA to ED in the TRCOER register are set to 1 (output level is fixed or high impedance depending on TRCOPR register setting) if the waveform output manipulation event is input.
2. When the OPE bit is 0 (waveform output manipulation disabled), bits EA to ED in the TRCOER register are not affected by the setting of this bit.
3. When the OPE bit is 1 or the RESTATS bit is 0 (output is restarted by software), bits EA to ED in the TRCOER register are set to 0 by software. Bits EA to ED are not automatically set to 0 even if the waveform output manipulation event is cancelled.
4. When the OPE bit is 1 or the RESTATS bit is 1 (output is automatically restarted), bits EA to ED are automatically set to 0 if the waveform output manipulation event is cancelled.
5. When the OPE bit is 0, only the setting of the TRCOER register is used to manipulate the output for timer RC. When the OPE bit is 1, regardless of the setting of the PTO bit in the TRCOER register, the waveform output for timer RC is manipulated with the settings of the TRCOPR register. Bits EA to ED in the TRCOER register are used as the flags for manipulating the waveform output. When a waveform output manipulation event is input, bits EA to ED are set to 1.

15.3 Operation

Table 15.10 lists the Timer RC Operating Modes.

Table 15.10 Timer RC Operating Modes

Item	Description
Timer mode	Timer mode is used by setting the PWM2 bit to 0 and bits PWMB to PWMD to 0 in the TRCMR register. In this case, the output compare function or input capture function is used by setting bits IOA0 to IOA2 and IOB0 to IOB2 in the TRCIOR0 register and bits IOC0 to IOC2 and IOD0 to IOD2 in the TRCIOR1 register.
PWM mode	PWM mode is used by setting the PWM2 bit to 0 and bits PWMB to PWMD to 1 in the TRCMR register.
PWM2 mode	PWM2 mode is used by setting the PWM2 bit in the TRCMR register to 1.

Tables 15.11 to 15.14 list the settings of pins TRCIOA to TRCIOD. For the assignments of pins TRCIOA to TRCIOD, see **12. I/O Ports**.

Table 15.11 TRCIOA Pin Settings

Register	TRCOER	TRCMR	TRCIOR0			Function
Bit	EA	PWM2	IOA2	IOA1	IOA0	
Setting value	0	1	0	0	1	Timer mode waveform output (output compare function)
				1	X	
	X	1	1	X	X	Timer mode (input capture function)
	Other than the above					I/O port

X: 0 or 1

Table 15.12 TRCIOB Pin Settings

Register	TRCOER	TRCMR		TRCIOR0			Function
Bit	EB	PWM2	PWMB	IOB2	IOB1	IOB0	
Setting value	0	0	X	X	X	X	PWM2 mode waveform output
	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	X	1	0	1	X	X	Timer mode (input capture function)
	Other than the above						I/O port

X: 0 or 1

Table 15.13 TRCIOC Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	EC	PWM2	PWMC	IOC2	IOC1	IOC0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	X	1	0	1	X	X	Timer mode (input capture function)
	PWM2 = 1 and other than the above						I/O port

X: 0 or 1

Table 15.14 TRCIOD Pin Settings

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	ED	PWM2	PWMD	IOD2	IOD1	IOD0	
Setting value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer mode waveform output (output compare function)
					1	X	
	X	1	0	1	X	X	Timer mode (input capture function)
	PWM2 = 1 and other than the above						I/O port

X: 0 or 1

15.3.1 Timer Mode

The TRCCNT register performs free-running or period count operations. Immediately after a reset, the TRCCNT register functions as a free-running counter. When the CTS bit in the TRCMR register to set to 1 (count is started), count operation is started. When the TRCCNT register overflows from FFFFh to 0000h, the OVF bit in the TRCSR register is set to 1, and an interrupt request is generated if the OVIE bit in the TRCIER register is 1 (interrupt request (FOVI) by OVF flag is enabled).
Figure 15.2 shows an Example of Free-Running Counter Operation.

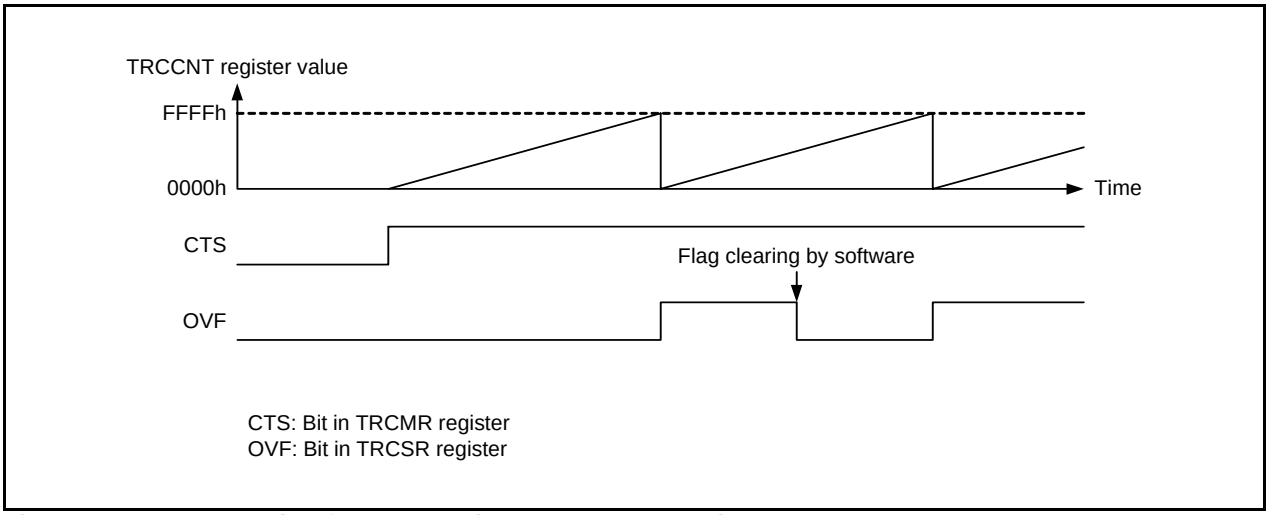


Figure 15.2 Example of Free-Running Counter Operation

When the TRCGRA register for period setting is set to an arbitrary value and the CCLR bit in the TRCCR1 register is set to 1, the TRCCNT register operates for counting periods. When the count value matches the TRCGRA register, the TRCCNT register changes to 0000h and the IMFA bit in the TRCSR register is set to 1. If the corresponding IMIEA bit in the TRCIER register is 1 (interrupt request (IMIA) by IMFA bit is enabled) at this time, an interrupt request is generated. The TRCCNT register continues increment operation from 0000h.
Figure 15.3 shows an Example of Period Counter Operation.

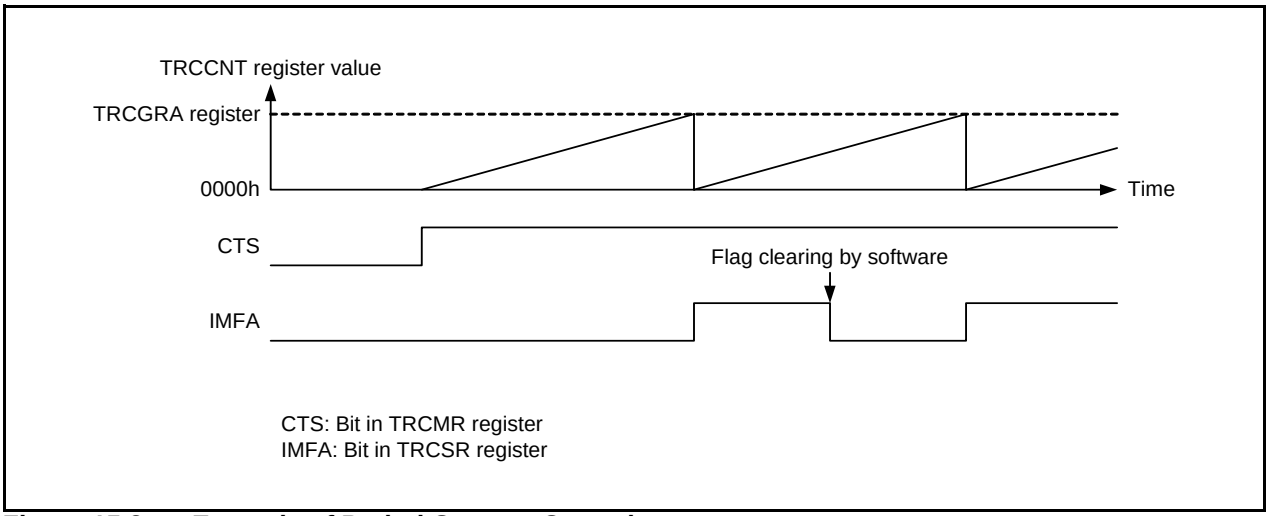


Figure 15.3 Example of Period Counter Operation

By setting the general register as an output compare register, low-level, high-level, or toggle output is performed by compare matches A to D from pins TRCIOA, TRCIOB, TRCIOC, TRCIOD.
Figure 15.4 shows an Example of Low-Level and High-Level Output Operation. The TRCCNT register is used for the free-running count operation, a low level is output at compare match B, and a high level is output at compare match A. When the set level and the pin level are the same, the pin level remains unchanged.

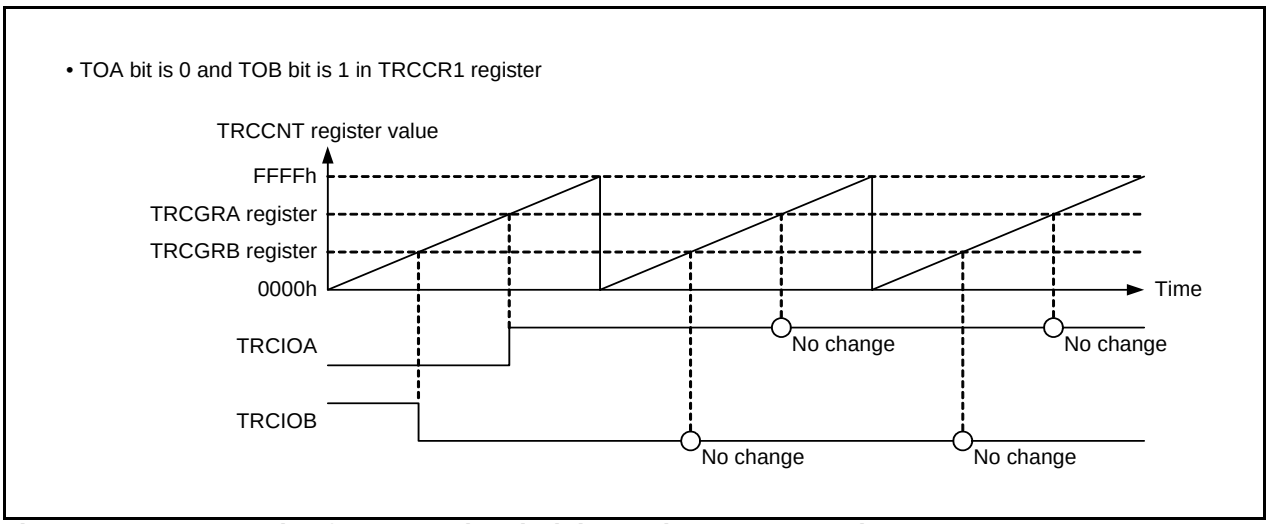


Figure 15.4 Example of Low-Level and High-Level Output Operation

Figure 15.5 shows an Example of Toggle Output Operation during Free-Running Count. The TRCCNT register is used for the free-running count operation, and toggle output is performed at compare matches A and B.

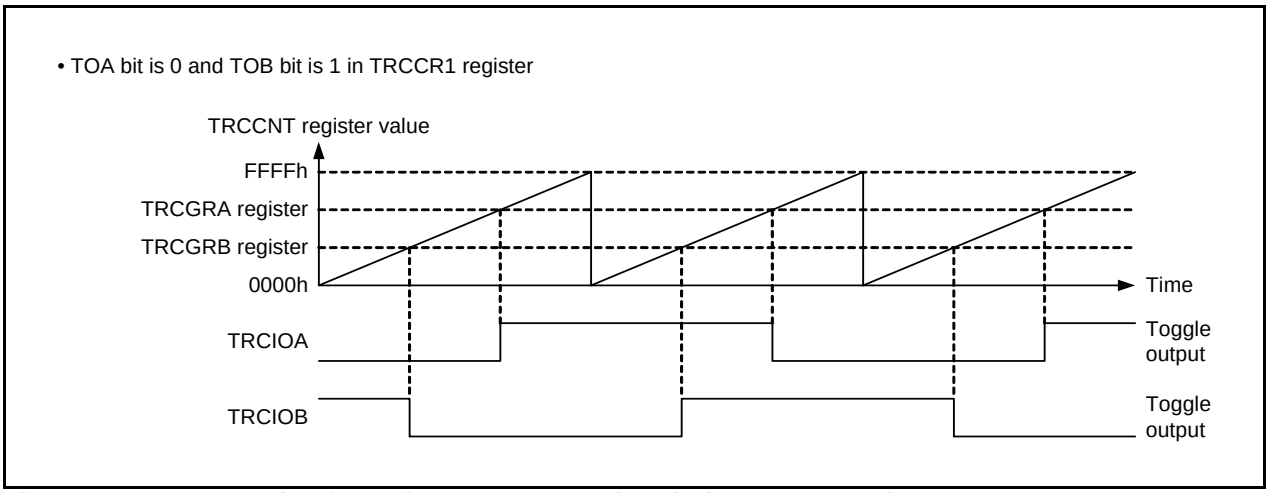


Figure 15.5 Example of Toggle Output Operation during Free-Running Count

Figure 15.6 shows an Example of Toggle Output Operation during Period Count. The TRCCNT register is used for the period count operation, and toggle output is performed at compare matches A and B.

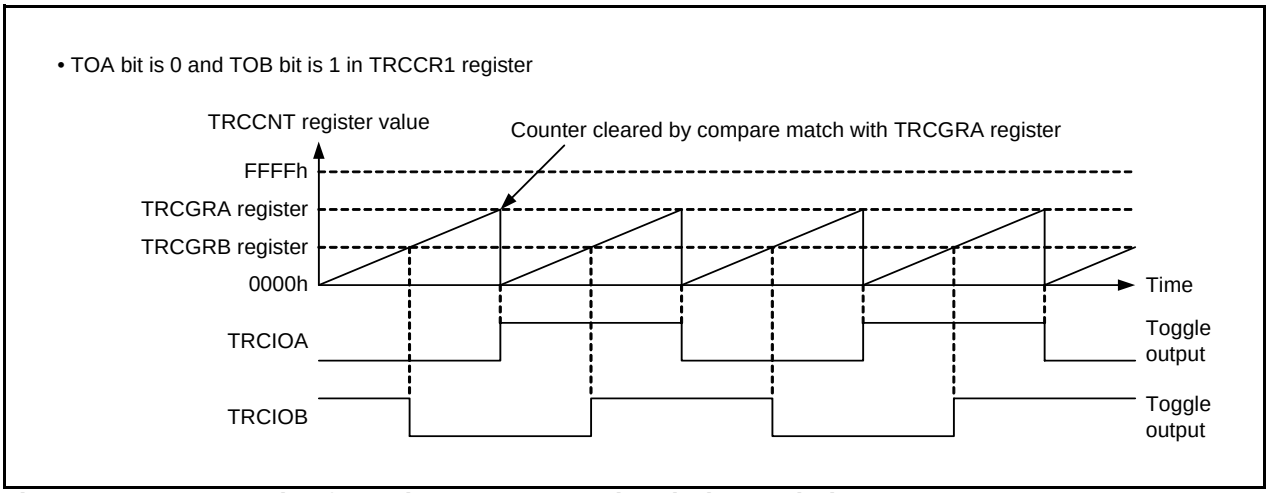


Figure 15.6 Example of Toggle Output Operation during Period Count

The input capture function can be used to measure the pulse width or period.
By setting the general register to be an input capture register, the value in the TRCCNT register on input edge detection of pins TRCIOA to TRCIOD is transferred to registers TRCGRA to TRCGRD. This value is used to measure the period. The detection edge can be selected to be a rising edge, falling edge, or two-way edge.
Figure 15.7 shows an Example of Input Capture Operation. The TRCCNT register is used for the free-running operation, and a two-way edge is selected for the input capture input to the TRCIOA pin and a falling edge is selected for the input capture input to the TRCIOB pin.

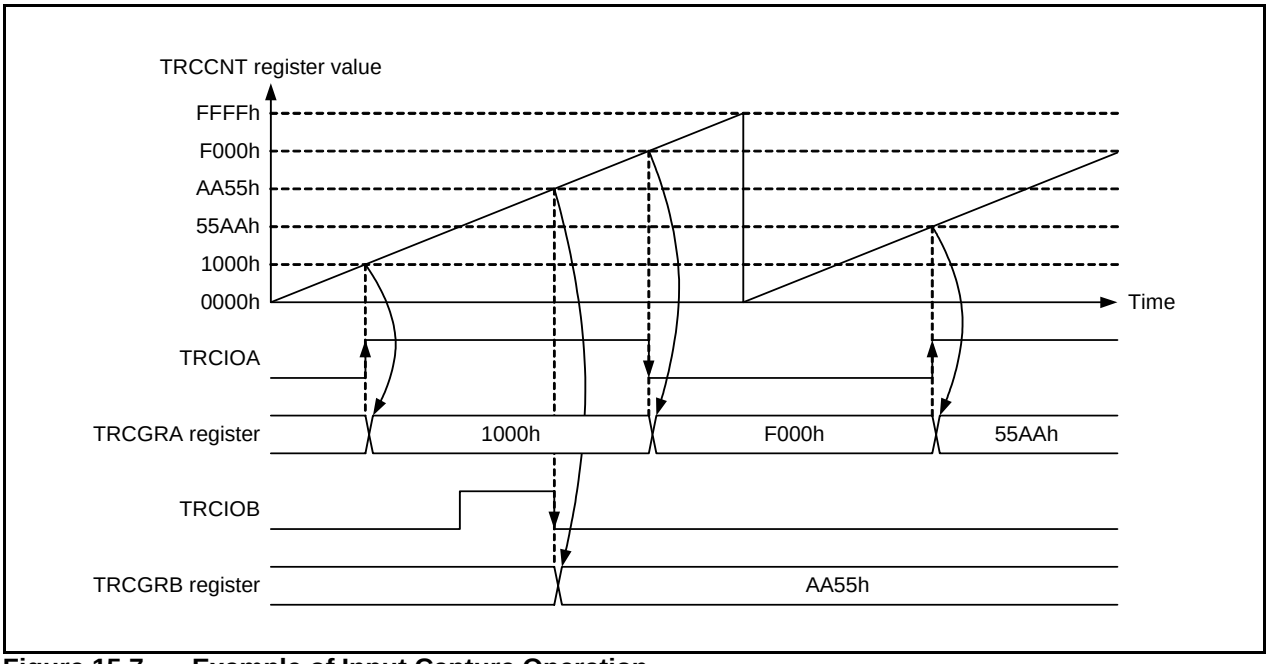


Figure 15.7 Example of Input Capture Operation

Figure 15.8 shows an Example of Buffer Operation during Input Capture. This example applies when the TRCGRA register is set as an input capture register and the TRCGRC register is set as a buffer register for the TRCGRA register. In this example, the TRCCNT register is used for the free-running count operation and both rising and falling edges are selected for the input capture input to the TRCIOA pin. Since buffer operation is set, the value in the TRCCNT register is stored in the TRCGRA register by input capture A and the value that has been stored in the TRCGRA register is transferred to the TRCGRC register at the same time.

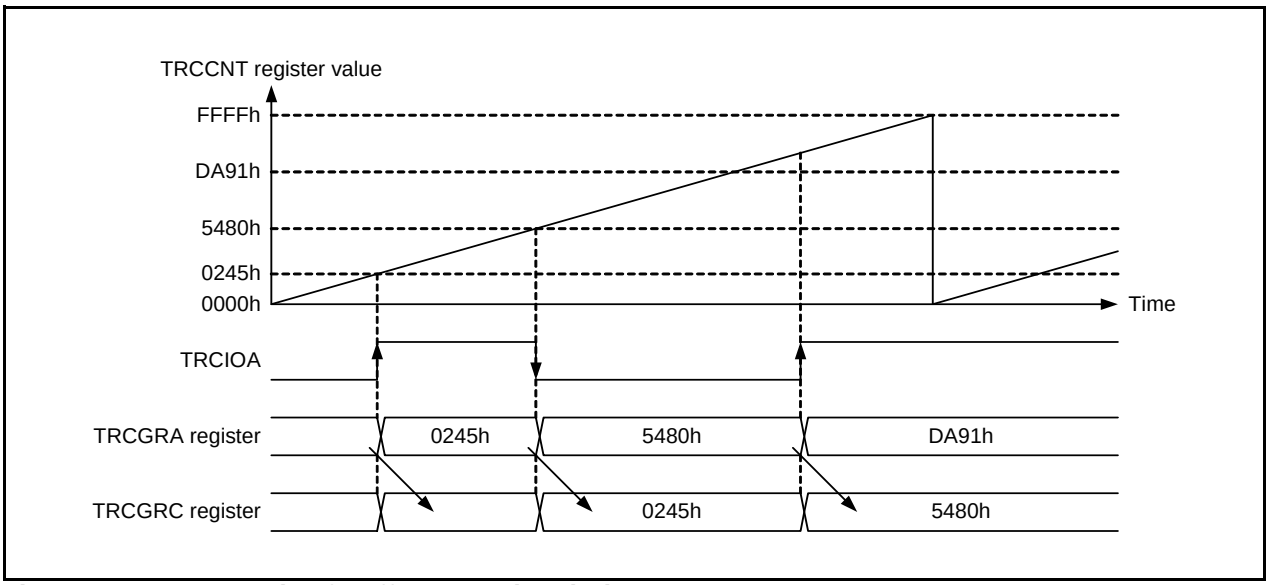


Figure 15.8 Example of Buffer Operation during Input Capture

15.3.2 PWM Mode

In PWM mode, when the TRCGRA register is set as the period register and registers TRCGRB, TRCGRC, and TRCGRD are set as duty registers, a PWM waveform is output from pins TRCIOB, TRCIOC, and TRCIOD individually. A PWM waveform with up to three phases can be output. In this mode, the general register automatically functions as an output compare register. The settings of bits IOB2, IOC2, and IOD2 are invalid. The initial output level of the corresponding pin is set according to the values in bits TOA to TOD in the TRCCR1 register and bits POLB to POLD in the TRCCR2 register.
Table 15.15 lists the Initial Output Levels of TRCIOB Pin.

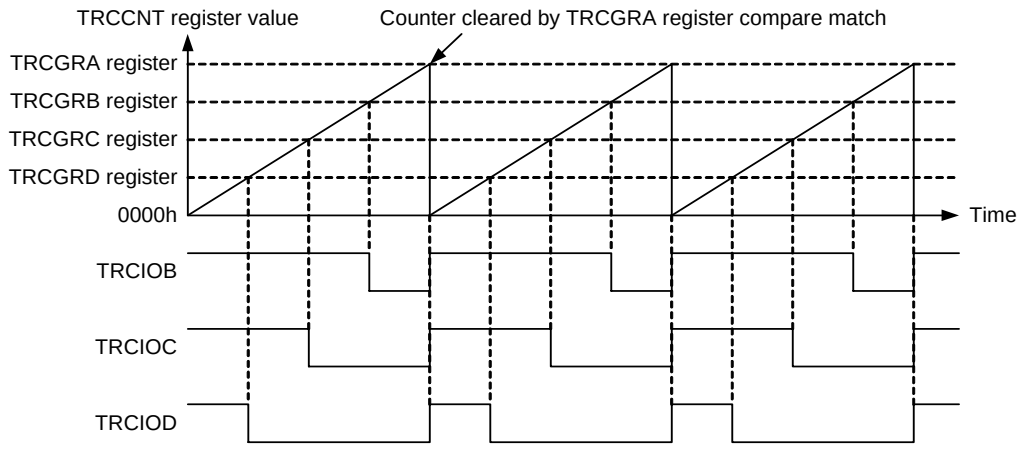
Table 15.15 Initial Output Levels of TRCIOB Pin

TOB Bit in TRCCR1 Register	POLB Bit in TRCCR2 Register	Initial Output Level
0	0	1
	1	0
1	0	0
	1	1

The output level is determined by bits POLB to POLD in the TRCCR2 register. When the POLB bit is 0 (output level is active low), the TRCIOB output pin is set to low at compare match B and high at compare match A. When the POLB bit is 1 (output level is active high), the TRCIOB output pin is set to high at compare match B and low at compare match A.
The setting values of bits PWMD to PWMB in TRCMR take precedence over those in registers TRCIOR0 and TRCIOR1. When the values set in the period and duty registers are the same, the output value remains unchanged even if a compare match occurs.

Figure 15.9 shows an Operation Example in PWM Mode.

• High-level output when TRCCNT register is cleared at compare match A. Low-level output at compare matches B, C, and D. (POLB bit = 0, POLC bit = 0, and POLD bit = 0 in TRCCR2 register)



• Low-level output when TRCCNT register is cleared at compare match A. High-level output at compare matches B, C, and D. (POLB bit = 1, POLC bit = 1, and POLD bit = 1 in TRCCR2 register)

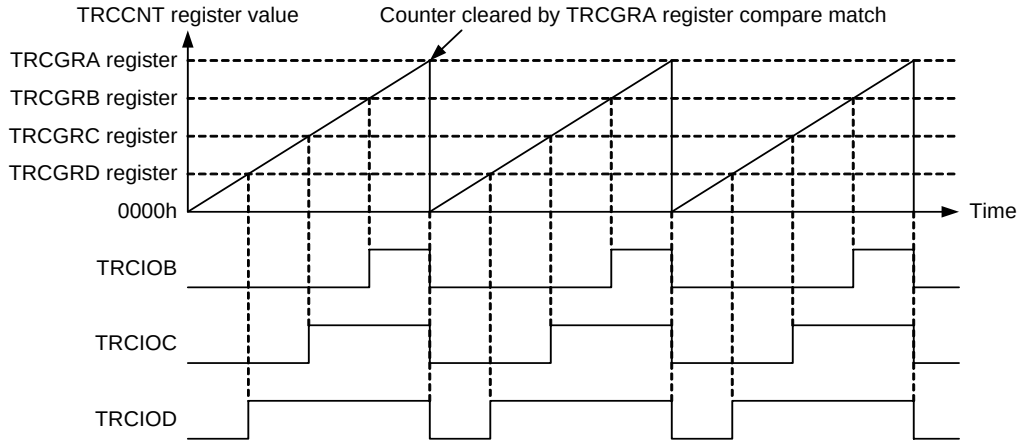


Figure 15.9 Operation Example in PWM Mode

Figure 15.10 shows an Example of Buffer Operation in PWM Mode. In this example, the TRCIOB pin is set to PWM mode and the TRCGRD register is set as the buffer register for the TRCGRB register. The TRCCNT register is cleared by compare match A, and output is set to low at compare match A and high at compare match B.
Since buffer operation is set, the output is changed when compare match B occurs, and the value in the buffer register TRCGRD is transferred to the TRCGRB register at the same time. This operation is repeated each time compare match B occurs.

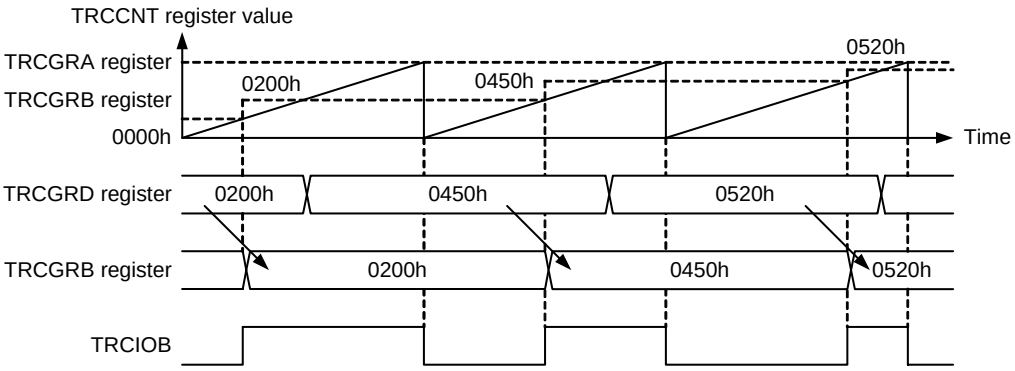
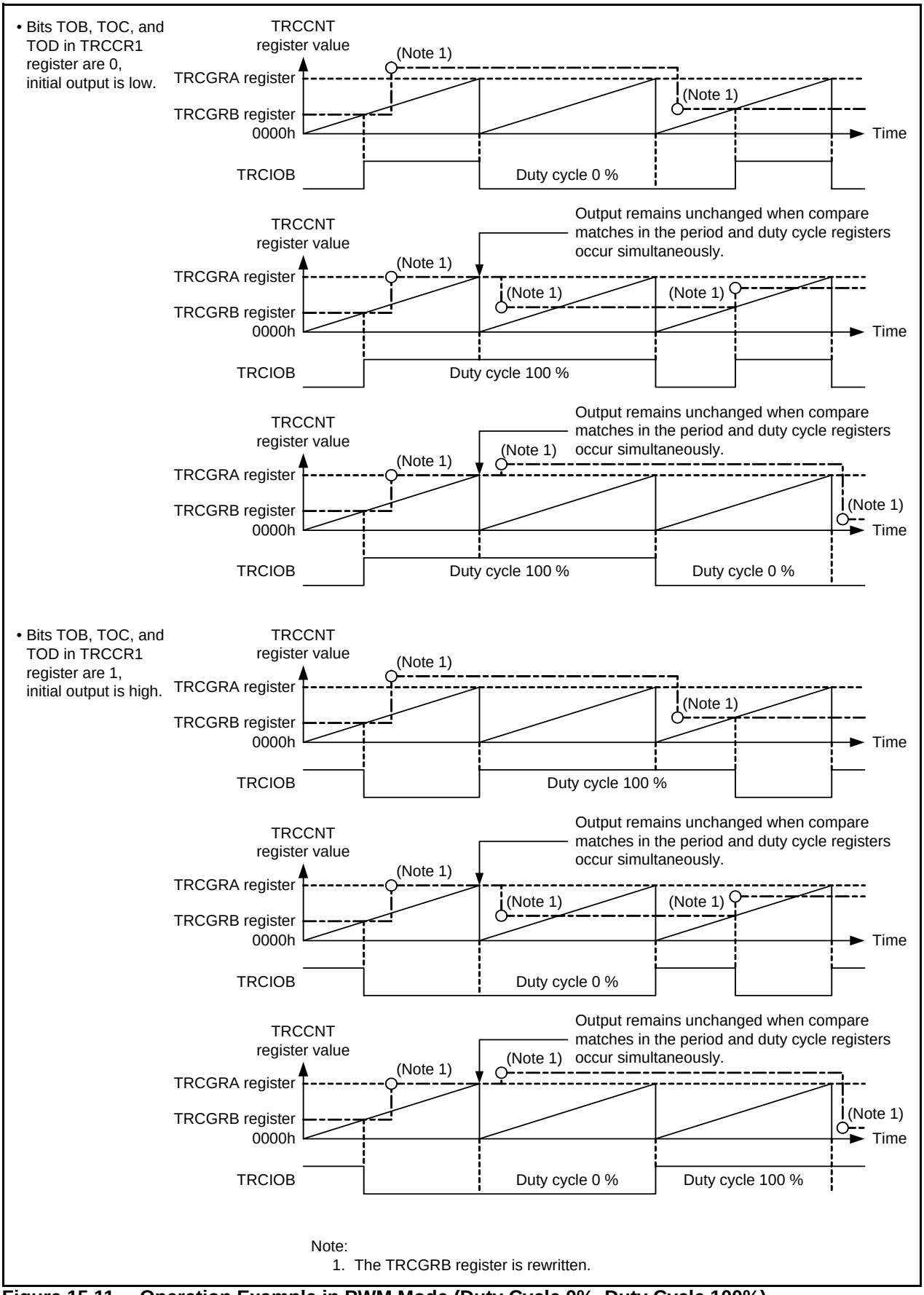


Figure 15.10 Example of Buffer Operation in PWM Mode

Figure 15.11 shows an Operation Example in PWM Mode (Duty Cycle 0%, Duty Cycle 100%).



Note:
1. The TRCGRB register is rewritten.

Figure 15.11 Operation Example in PWM Mode (Duty Cycle 0%, Duty Cycle 100%)

15.3.3 PWM2 Mode

Unlike PWM mode in PWM2 mode, a waveform is output from the TRCIOB pin at a compare match with registers TRCGRB and TRCGRC. When the BUFEB bit in the TRCMR register is set to 1 (TRCGRD register is used as a buffer register for TRCGRB register), the TRCGRD register functions as a buffer register for the TRCGRB register. The output level is determined by the TOB bit in the TRCCR1 register.

When the TOB bit is 0 (output value 0), a low level is output at a compare match with the TRCGRB register and a high level is output at a compare match with the TRCGRC register. When the TOB bit is 1 (output value 1), a high level is output at a compare match with the TRCGRB register and a low level is output at a compare match with the TRCGRC register.

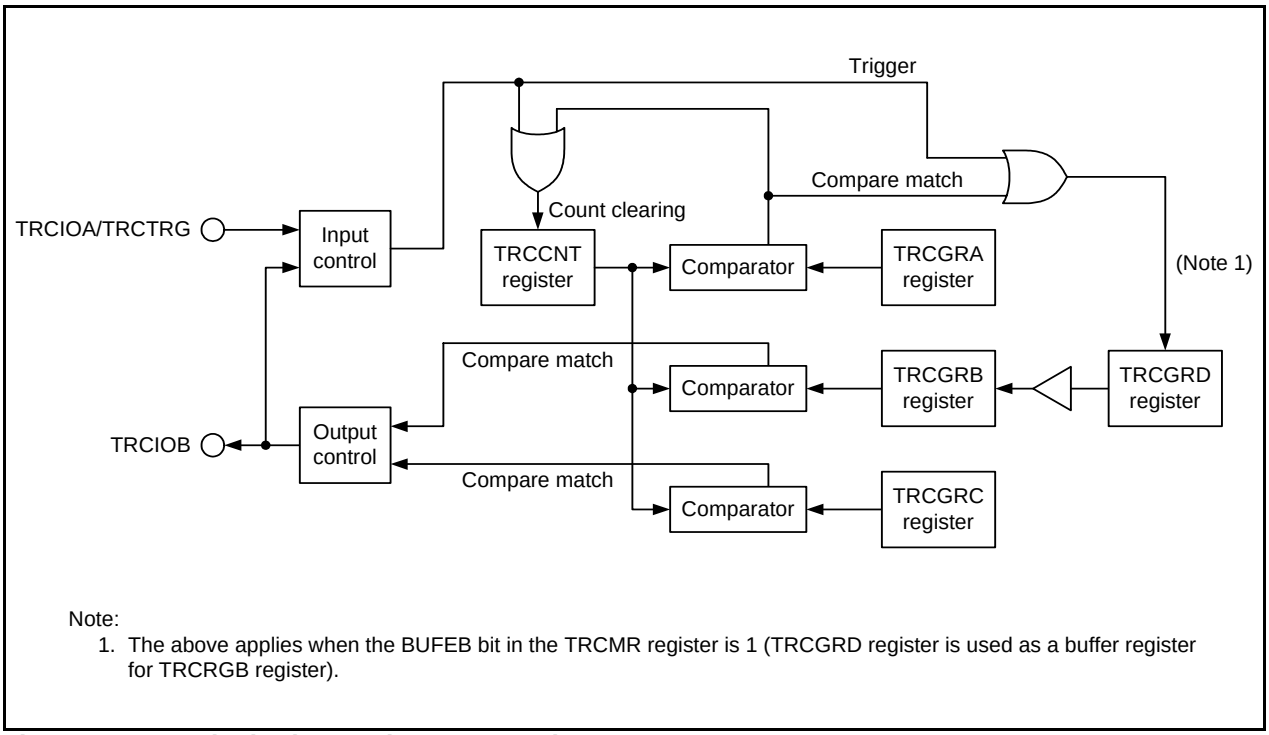
Table 15.16 lists the Combinations of Pin Functions and General Registers for PWM2 Mode and General Registers for PWM2 Mode. Figure 15.12 shows the Block Diagram in PWM2 Mode. Figure 15.13 shows the Timing of Buffer Operations for Registers TRCGRD and TRCGRB in PWM2 Mode.

The value in the TRCGRD register is transferred to the TRCGRB register and the counter is cleared by a compare match with the TRCGRA register. However, the counter is cleared only when the CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A). Also, when trigger input is enabled by bits TCEG0 to TCEG1 in the TRCCR2 register in PWM2 mode, the value in the TRCGRD register is transferred to the TRCGRB register and the counter is cleared by a trigger. The timer I/O pins that are not used in PWM2 mode can be used as I/O ports.

Table 15.16 Combinations of Pin Functions and General Registers for PWM2 Mode

Pin Name	I/O	Compare Match Register	Buffer Register
TRCIOA	I/O	Port function (1)/TRCTRG input	
TRCIOB	O	TRCGRB register	TRCGRD register
		TRCGRC register	—
TRCIOC	I/O	Port function (1)	
TRCIOD			

Note:
1. To use the port function, set the corresponding bit in registers PMLi (i = 0 to 4) and PMHi (i = 0, 1, 3, or 4) to 0.



Note:
1. The above applies when the BUFEB bit in the TRCMR register is 1 (TRCGRD register is used as a buffer register for TRCRGB register).

Figure 15.12 Block Diagram in PWM2 Mode

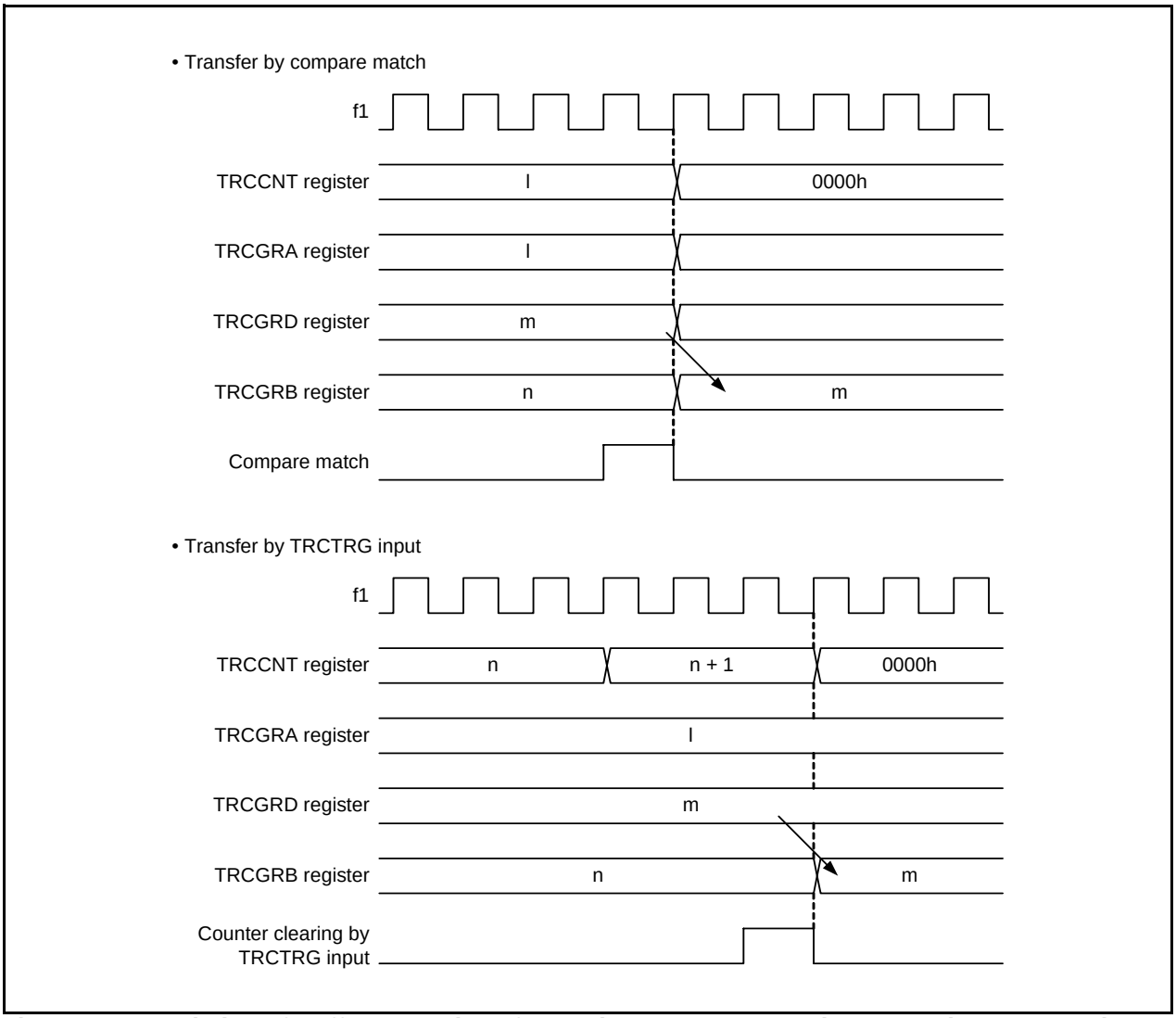


Figure 15.13 Timing of Buffer Operations for Registers TRCGRD and TRCGRB in PWM2 Mode

In PWM2 mode, the TRCTRG input is used to output a pulse with an arbitrary delay time and width from the TRCIOB pin.
Set bits TCEG1 to TCEG0 in the TRCCR2 register to 10b (falling edge) to set the falling edge for the TRCTRG input. Set the CSTP bit in the TRCCR2 register to 0 (increment is continued) to continue incrementing when compare match A with the TRCGRA register occurs. Set the BUFEB bit in the TRCMR register to 1 (TRCGRD register is used as a buffer register for TRCGRB register) to set the TRCGRD register as the buffer register. Set the TOB bit in the TRCCR1 register to 0 (output value 0) or 1 (output value 1) to set the initial level of the output level to 0 or 1. Next, set the CCLR bit in the TRCCR1 register to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the TRCCNT register by compare match A.
Figure 15.14 shows an Operation Example in PWM2 Mode When TRCTRG Input is Enabled. Figure 15.15 shows an Operation Example in PWM2 Mode When TRCTRG Input is Disabled. These examples apply when the PWM2 bit in the TRCMR register is set to 0 (PWM2 mode) and a waveform is output from the TRCIOB pin.
In PWM2 mode, when the TOB bit in the TRCCR1 register is 0 (output value 0), the TRCTRG input edge is disabled while a high level is output from the TRCIOB pin. Likewise, when the TOB bit is 1 (output value 1), the TRCTRG input edge is disabled while a low level is output from the TRCIOB pin. In addition, transfer from registers TRCGRD to TRCGRB is performed when a compare match with the TRCGRA register or TRCTRG input occurs. However, if the TRCTRG input is disabled depending on the level of the TRCIOB pin, transfer from registers TRCGRD to TRCGRB is not performed.

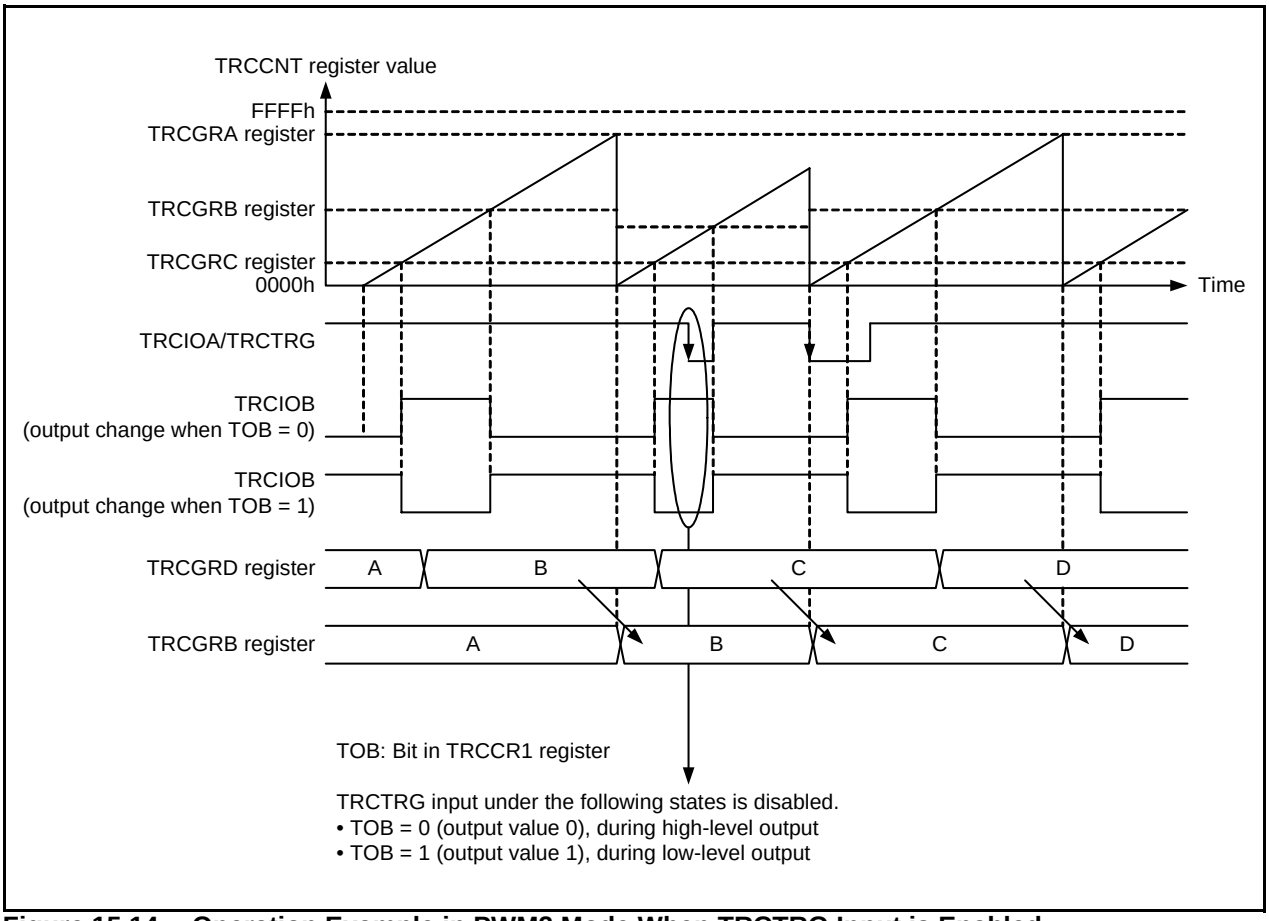


Figure 15.14 Operation Example in PWM2 Mode When TRCTRG Input is Enabled

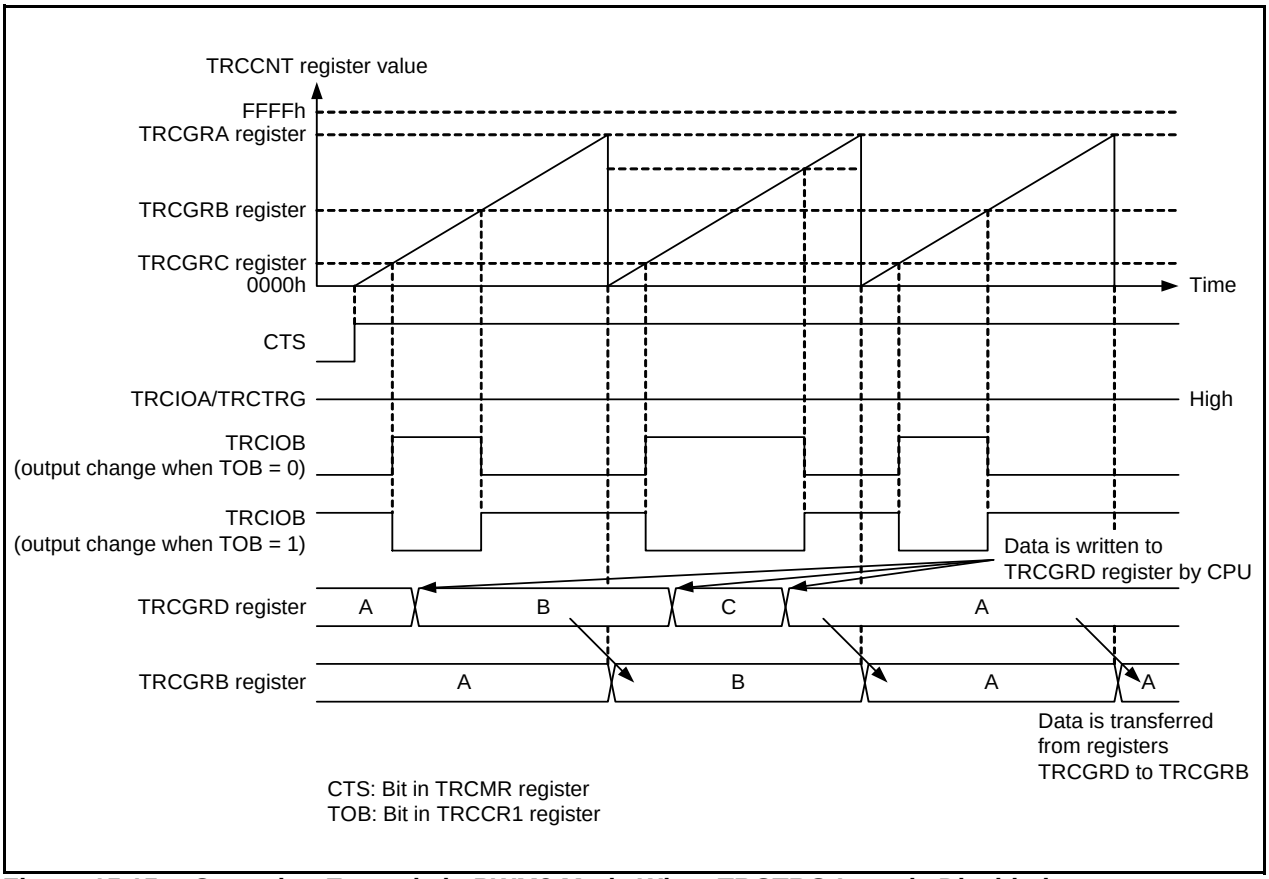


Figure 15.15 Operation Example in PWM2 Mode When TRCTRG Input is Disabled

Figure 15.16 shows an Example of Count Stop Operation in PWM2 Mode. In this example, the TOB bit in the TRCCR1 register is set to 0 (output value 0) and the TOB bit is set to 1 (output value 1).
By setting the CSTP bit in the TRCCR2 register to 1 (increment is stopped) and the CCLR bit in the TRCCR1 register to 1 (TRCCNT counter is cleared by input capture/compare match A), the counter is changed to 0000h and stopped by the compare match between registers TRCCNT and TRCGRA. By setting the CTS bit in the TRCMR register to 0 (count is stopped), the counter is forcibly stopped and the output is set to the initial level.

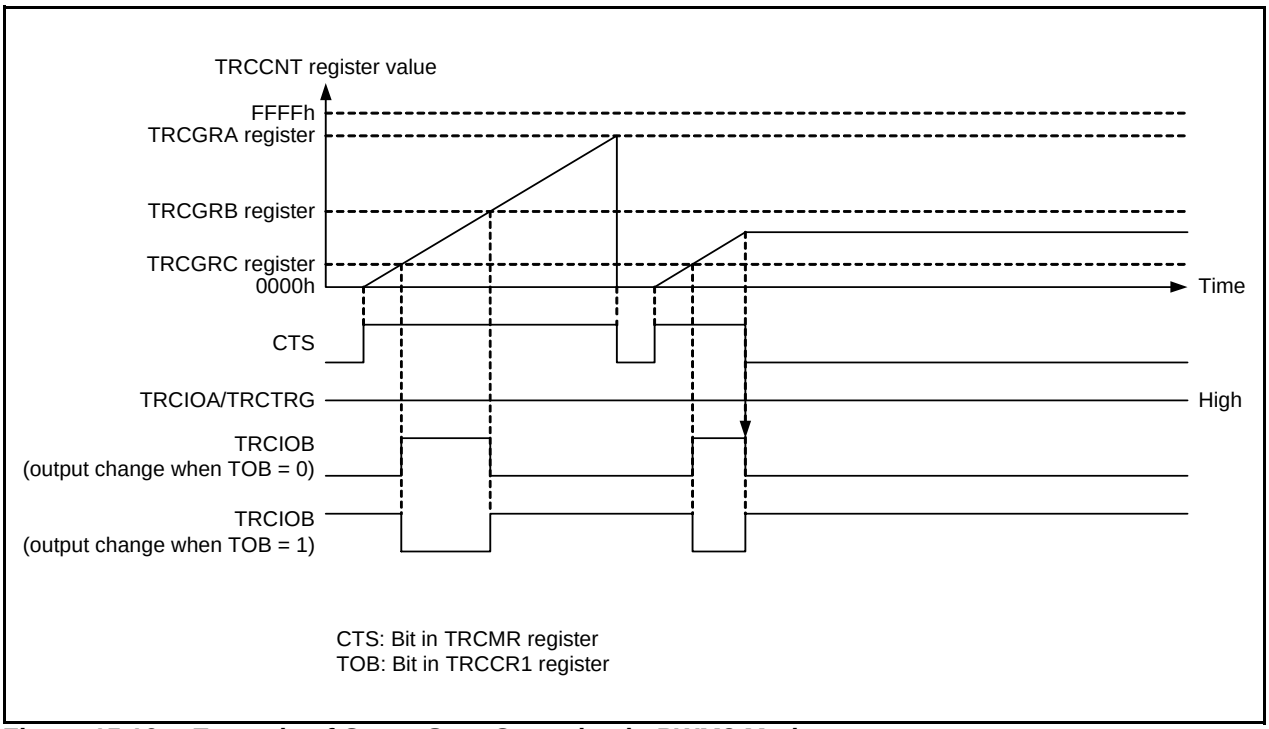


Figure 15.16 Example of Count Stop Operation in PWM2 Mode

Figure 15.17 shows an Example of One-Shot Pulse Waveform Output Operation in PWM2 Mode.
The count is started when the CTS bit in the TRCMR register is set to 1 (count is started) under the following conditions. Then, the counter is changed to 0000h by a compare match with the TRCGRA register, the count operation is stopped, and a one-shot waveform is output.

- Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 00b (TRCTRG input disabled) to disable the TRCTRG input.
- The CSTP bit in the TRCCR2 register is set to 1 (increment is stopped) to stop the increment when compare match A with the TRCGRA register occurs.
- The CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the TRCCNT register by compare match A.
- The TOB bit in the TRCCR1 register is set to 0 (output value 0) to set the initial value of the output level to 0.

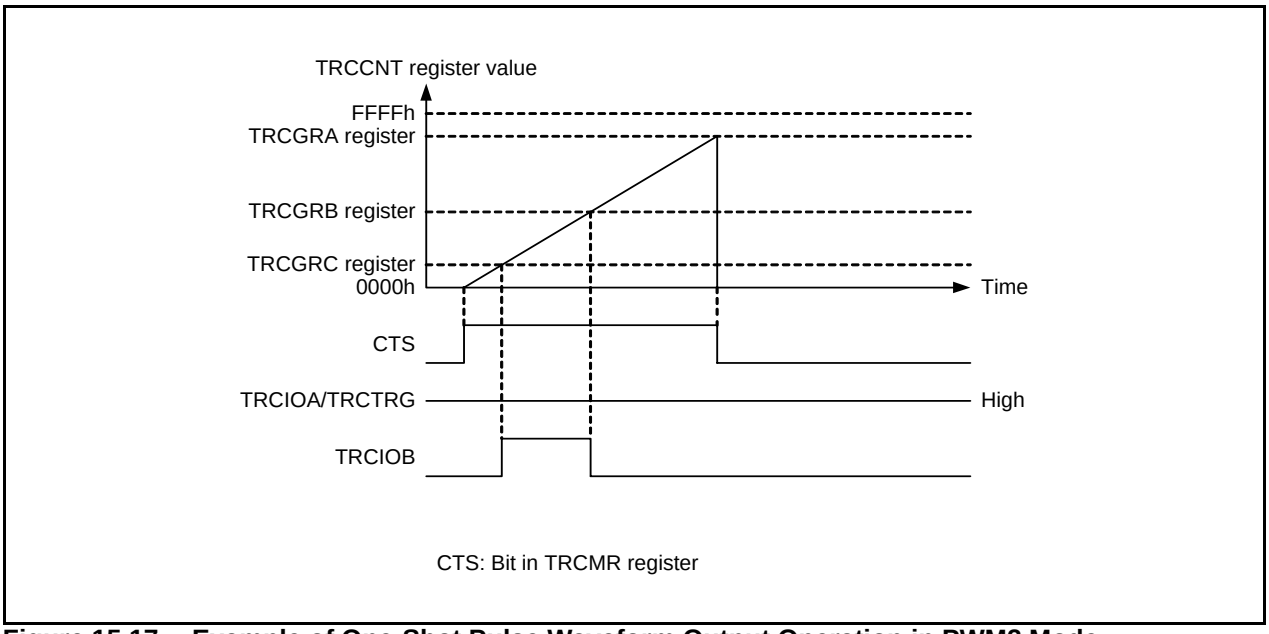


Figure 15.17 Example of One-Shot Pulse Waveform Output Operation in PWM2 Mode

Figure 15.18 shows an Example of One-Shot Waveform Output Operation in PWM2 Mode (Count is Started by TRCTRG Input).
After the CTS bit in the TRCMR register is set to 1 (count is started), the increment is started on the rising edge of TRCIOA/TRCTRG, and the counter is changed to 0000h by a compare match with the TRCGRA register, the count operation is stopped, and a one-shot waveform is output under the following conditions.

- Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 10b (falling edge) to set the falling edge of the TRCTRG input.
- The CSTP bit in the TRCCR2 register is set to 1 (increment is stopped) to stop the increment when a compare match with the TRCGRA register occurs.
- The CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the TRCCNT register by a compare match.
- The TOB bit in the TRCCR1 register is set to 0 (output value 0) to set the initial value of the output level to 0.

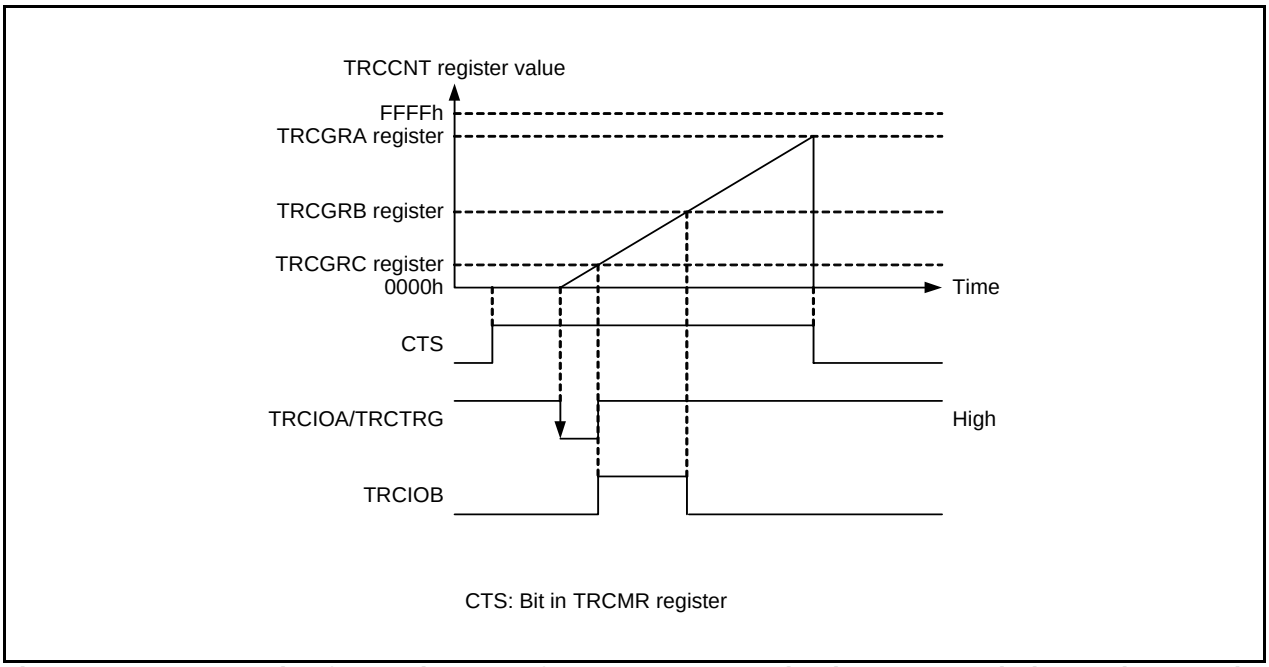


Figure 15.18 Example of One-Shot Waveform Output Operation in PWM2 Mode (Count is Started by TRCTRG Input)

15.4 Selectable Functions

15.4.1 Input Digital Filter for Input Capture

Figure 15.19 shows the Digital Filter Circuit Block Diagram. The TRCIOA to TRCIOD and TRCTRG input can be latched internally through the digital filter circuit. This circuit consists of three cascaded latch circuits and a match detection circuit. When the TRCIOA to TRCIOD and TRCTRG input are sampled on the clock selected by bits DFCK0 to DFCK1 in the TRCDF register and three outputs from the latch circuits match, the level is passed forward to the next circuit. If they do not match, the previous level is retained. That is, the pulse input with a width of three sampling clocks or more is recognized as a signal. If not, the change in the signal is recognized as noise and cancelled.

Do not use the digital filter immediately after a reset. Wait for four cycles of the sampling clock and make the setting for input capture before using the input capture function.

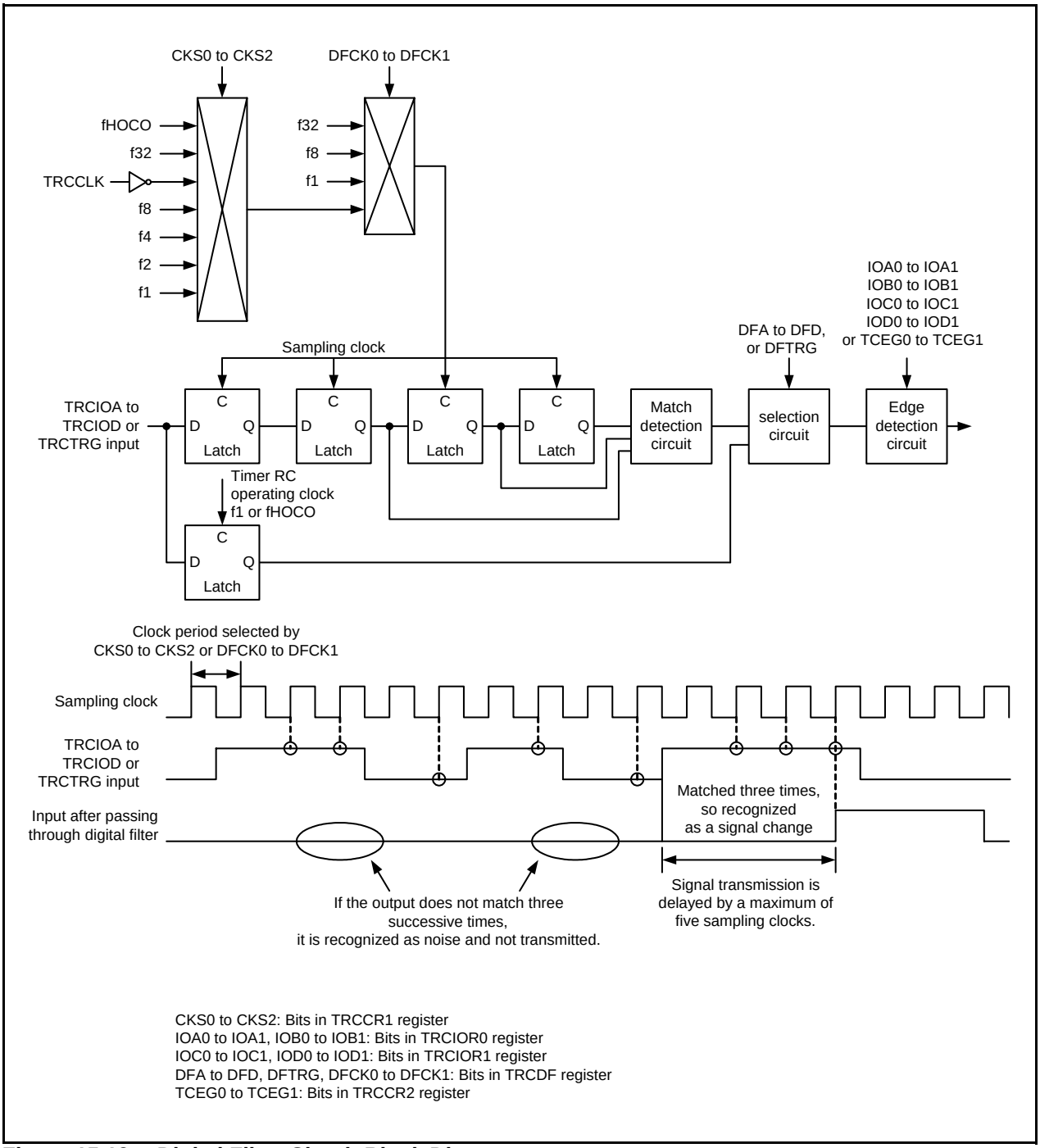


Figure 15.19 Digital Filter Circuit Block Diagram

15.4.2 A/D Conversion Start Trigger

By setting the TRCADCR register, an A/D conversion start trigger can be generated at compare matches A to D.
Figure 15.20 shows a Setting Example of A/D Conversion Start Trigger by Compare Matches B and C.

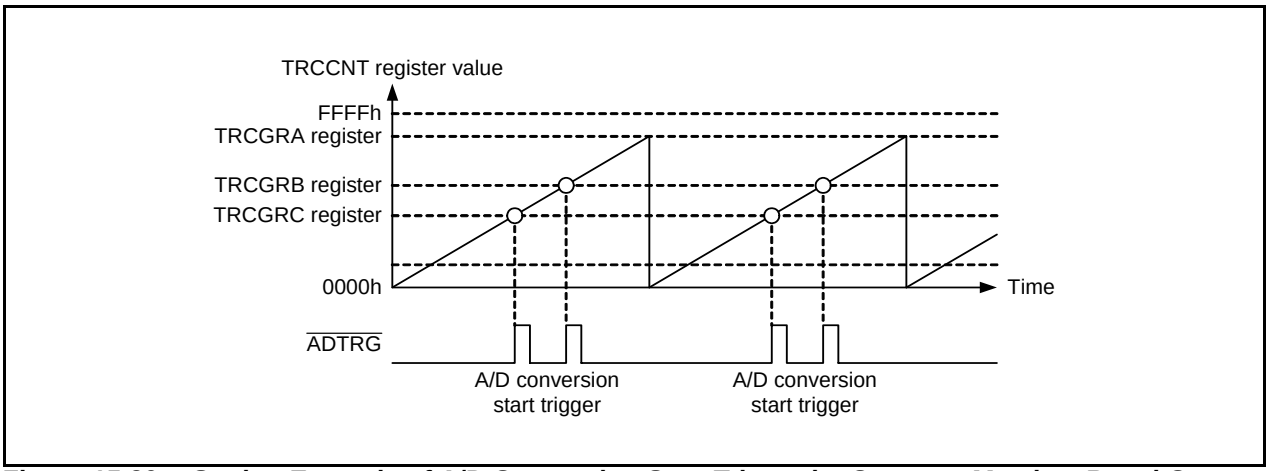


Figure 15.20 Setting Example of A/D Conversion Start Trigger by Compare Matches B and C

An A/D conversion start trigger is not generated from the buffer register during buffer operation. The TRCGRC register cannot operate as a buffer register for the TRCGRA register in PWM2 mode.
Table 15.17 lists the States Where A/D Conversion Start Trigger Sources are Generated.

Table 15.17 States Where A/D Conversion Start Trigger Sources are Generated

Operating Mode	Buffer Operation	A/D Conversion Start Trigger Source			
		TRCGRA	TRCGRB	TRCGRC	TRCGRD
Input capture	Used	No	No	No	No
	Not used	No	No	No	No
Compare match	Used	Yes	Yes	No	No
	Not used	Yes	Yes	Yes	Yes
PWM mode	Used	Yes	Yes	No	No
	Not used	Yes	Yes	Yes	Yes
PWM2 mode	Used	Yes	Yes	Yes	No
	Not used	Yes	Yes	Yes	Yes

Yes: An A/D conversion start trigger is generated.
No: No A/D conversion start trigger is generated.

15.4.3 Changing Output Pins and General Registers

The settings for bits IOC3 and IOD3 in the TRCIOR1 register can redirect the compare match output with registers TRCGRC and TRCGRD from pins TRCIOC and TRCIOD to pins TRCIOA and TRCIOB, respectively. The TRCIOA pin can output a combination of compare matches A and C and the TRCIOB pin can output a combination of compare matches B and D.
Figure 15.21 shows the Block Diagram for Changing Output Pins and General Registers.

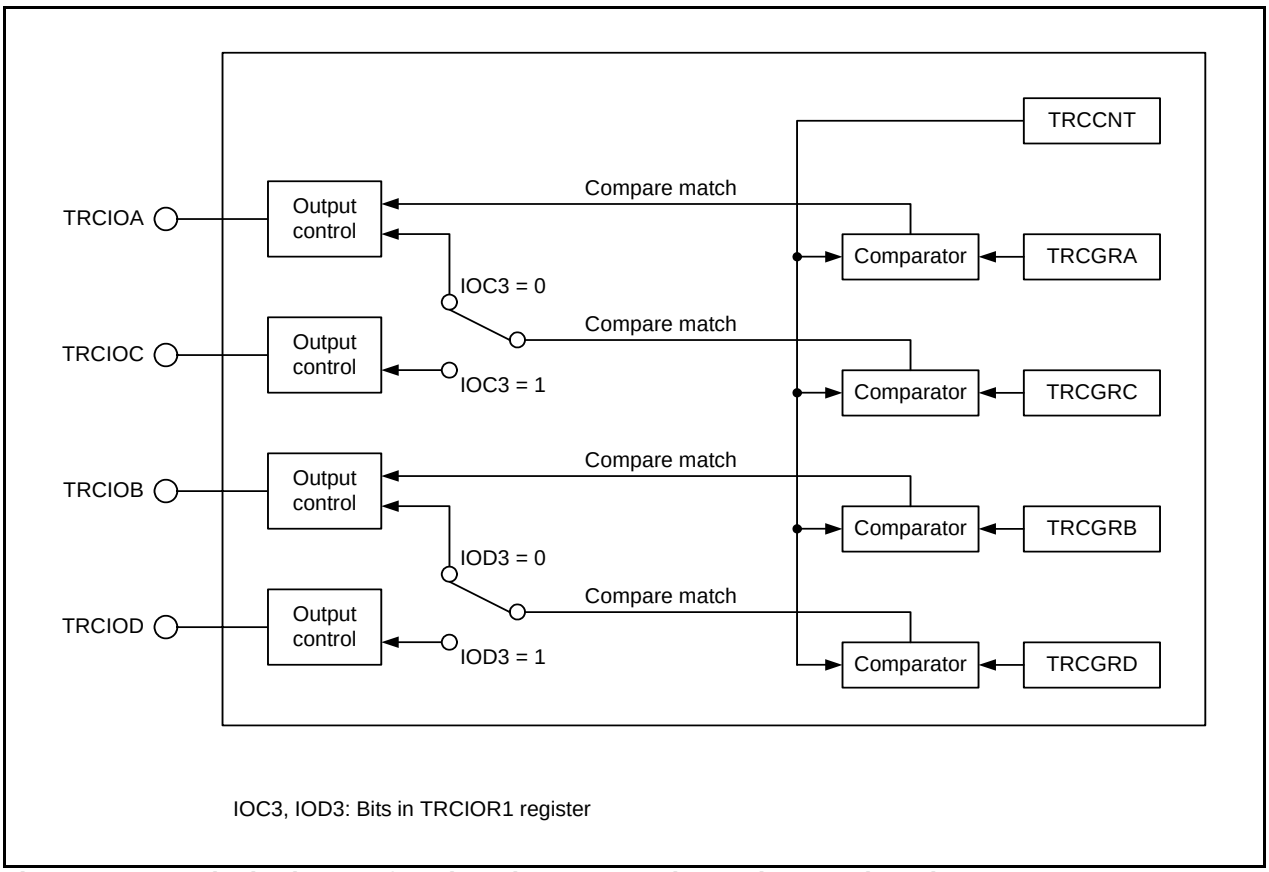


Figure 15.21 Block Diagram for Changing Output Pins and General Registers

Change output pins in registers TRDGRC and TRDGRD as follows:

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and the IOD3 bit to 0 (TRCIOB output register).
- Set bits BUFEA and BUFEB in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRA and TRCGRC. Also, set different values in registers TRCGRB and TRCGRD.

Figure 15.22 shows an Operation Example When TRCIOA and TRCIOB Output is not Overlapped. The following items must be set:

- Set the CCLR bit in the TRCCR1 register to 1 (TRCCNT counter is cleared by input capture/compare match A) to clear the counter by a compare match and set the TRCCNT register for period count operation.
- Set bits IOA2 to IOA0 in the TRCIOR0 register to 011b (toggle output from TRCIOA pin at compare match A) for toggle output.
- Set bits IOB2 to IOB0 in the TRCIOR0 register to 011b (toggle output from TRCIOB pin at compare match B) for toggle output.
- Set bits IOC3 to IOC0 in the TRCIOR1 register to 0011b (toggle output from TRCIOA pin at compare match C) for toggle output.
- Set bits IOD3 to IOD0 in the TRCIOR1 register to 0011b (toggle output from TRCIOB pin at compare match D) for toggle output.

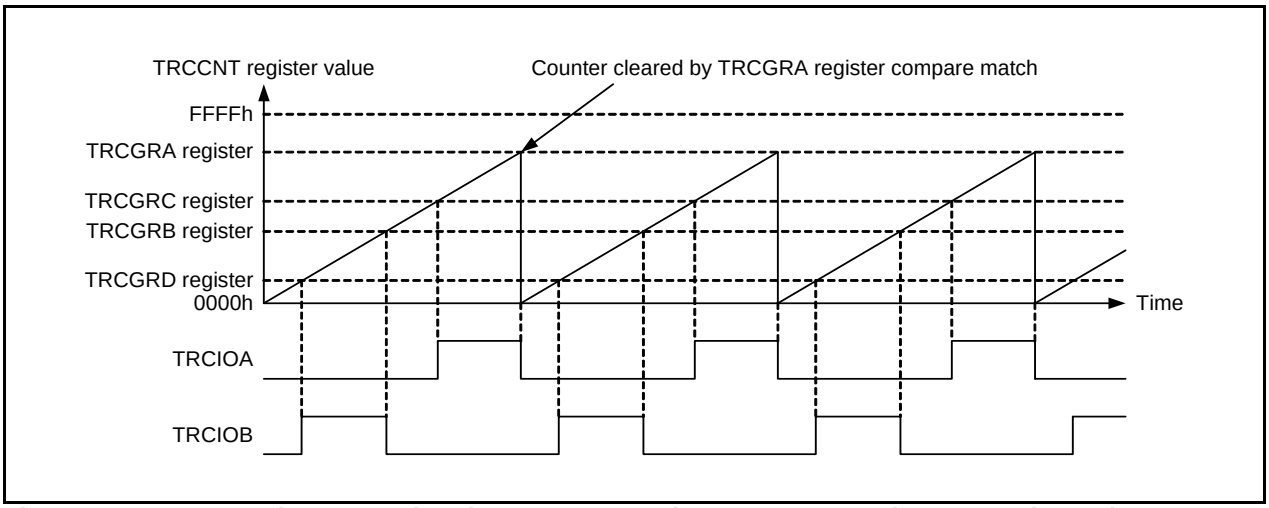


Figure 15.22 Operation Example When TRCIOA and TRCIOB Output is not Overlapped

15.4.4 Waveform Output Manipulation Function

By setting the TRCOPR register, the waveform output for timer RC can be controlled by the $\overline{\text{INT1}}$ input or comparator B1 output.

When the OPE bit in the TRCOPR register is 0, the waveform output manipulation function is disabled. The TRCIOA, TRCIOB, TRCIOC, and TRCIOD output from timer RC is output by setting registers TRCIOR0, TRCIOR1, and TRCOER. When the PTO bit in the TRCOER register is 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled), if a low level is input to the $\overline{\text{INT0}}$ pin, bits EA, EB, EC, and ED in the TRCOER register are set to all 1 (timer RC output disabled) and output pins TRCIOA to TRCIOD become high impedance.

When the OPE bit in the TRCOPR register is 1, the waveform output manipulation function is enabled. If a waveform output manipulation event is input, bits EA to ED in the TRCOER register are set to 1. Bits OPOL0 to OPOL1 in the TRCOPR register enable the output level of the timer RC pin to be fixed at low, high, or to high impedance during the waveform output manipulation period. After the waveform output manipulation event is cancelled, the waveform output manipulation for the timer RC pin is stopped and the output is restarted. The timing is automatically synchronized so that less than one cycle of waveform is not output after the output is restarted.

Figures 15.23 to 15.26 show Examples of Waveform Output Manipulation Operation.

- When the timer RC pin is pulled down, the OPE bit in the TRCOPR register is 1 (waveform output manipulation enabled), bits OPOL1 to OPOL0 are 00b (when timer RC pin is pulled down, timer RC output level is fixed to high impedance during waveform output manipulation period), and the RESTATS bit is 0 (output is restarted by software).

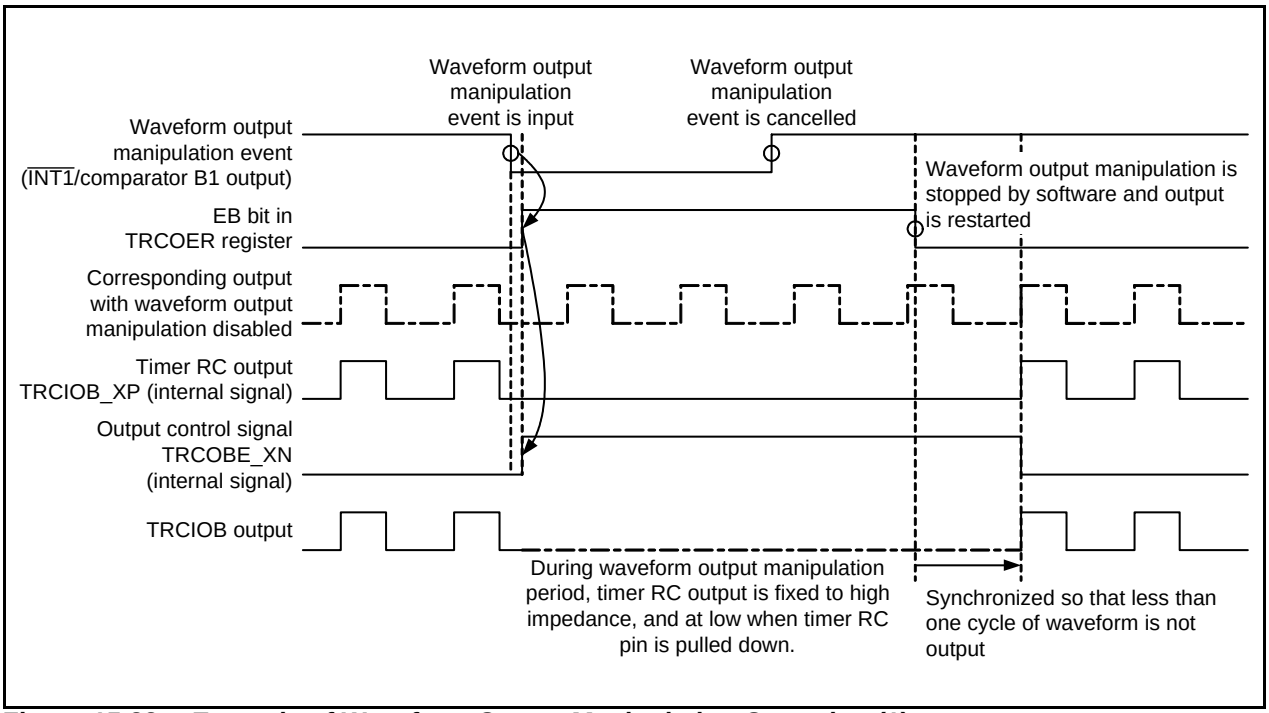


Figure 15.23 Example of Waveform Output Manipulation Operation (1)

• When the timer RC pin is pulled up, the OPE bit in the TRCOPR register is 1 (waveform output manipulation enabled), bits OPOL1 to OPOL0 are 01b (when timer RC pin is pulled up, timer RC output level is fixed to high impedance during waveform output manipulation period), and the RESTATS bit is 0 (output is restarted by software).

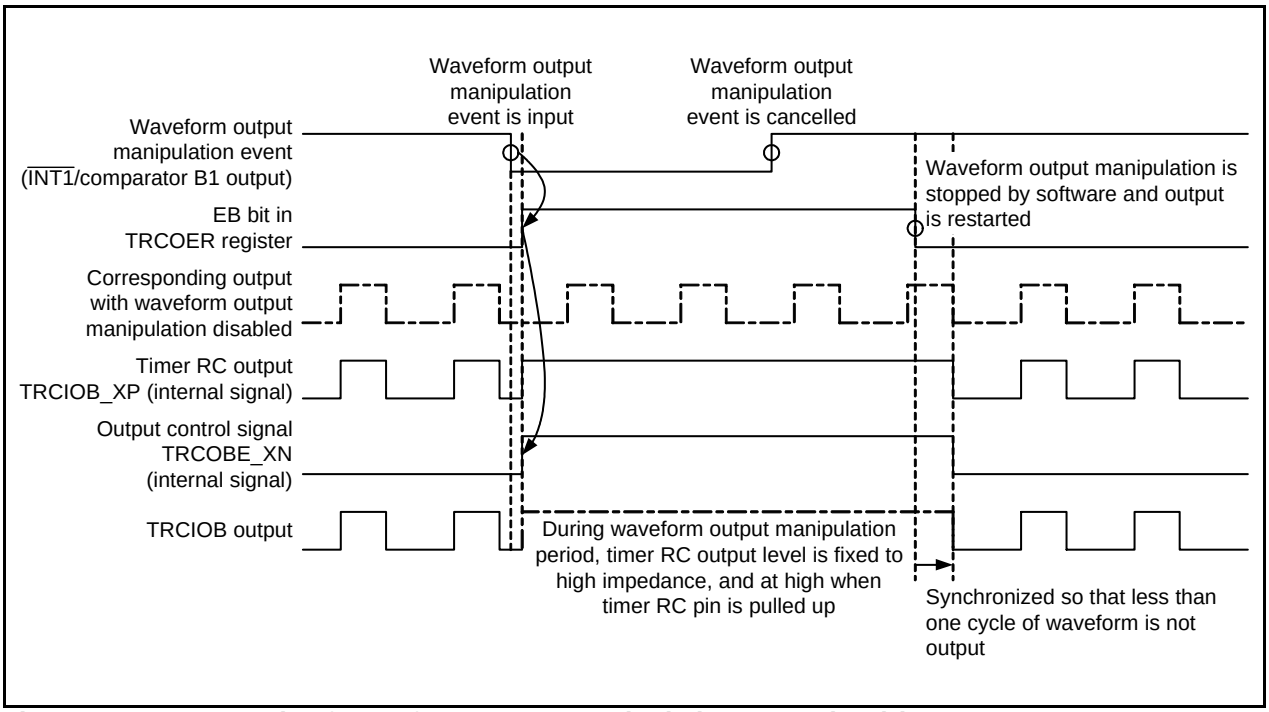


Figure 15.24 Example of Waveform Output Manipulation Operation (2)

• When the OPE bit in the TRCOPR register is 1 (waveform output manipulation enabled), bits OPOL1 to OPOL0 are 10b (timer RC output level is fixed at low during waveform output manipulation period), and the RESTATS bit is 1 (output is automatically restarted).

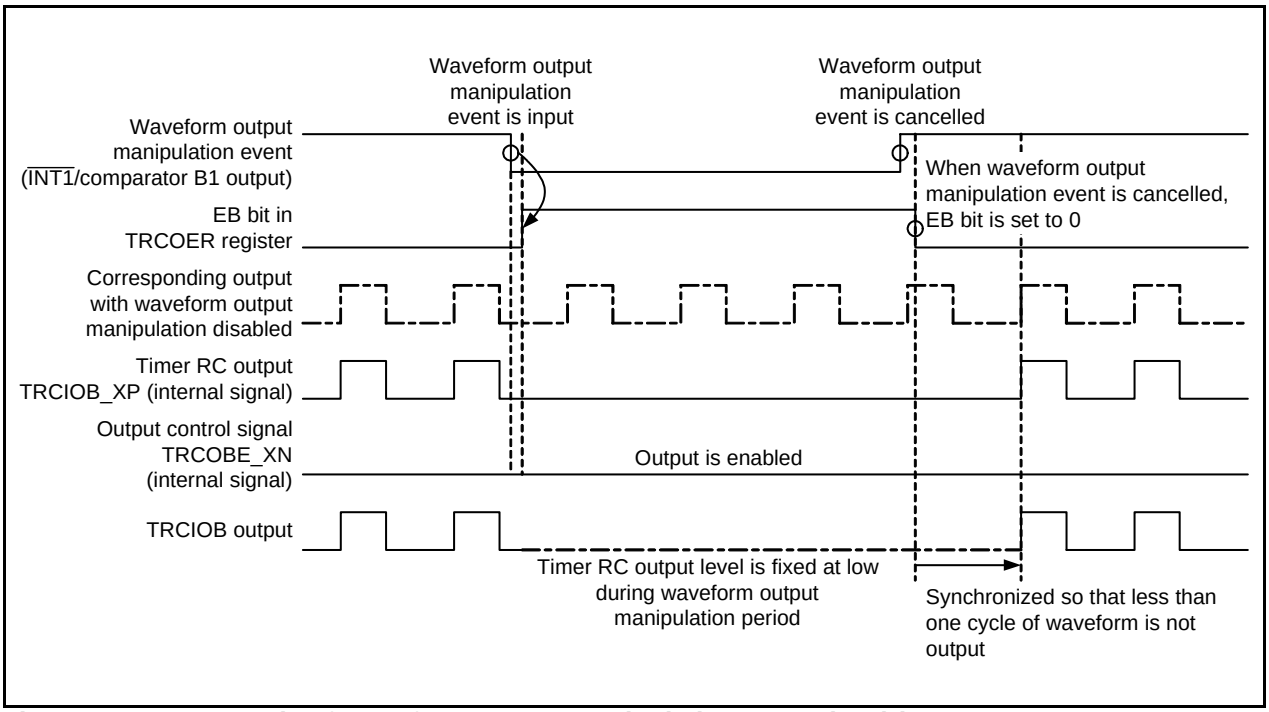


Figure 15.25 Example of Waveform Output Manipulation Operation (3)

• When the OPE bit in the TRCOPR register is 1 (waveform output manipulation control enabled), bits OPOL1 to OPOL0 are 11b (timer RC output level is fixed at high during waveform output manipulation period), and the RESTATS bit is 1 (output is automatically restarted).

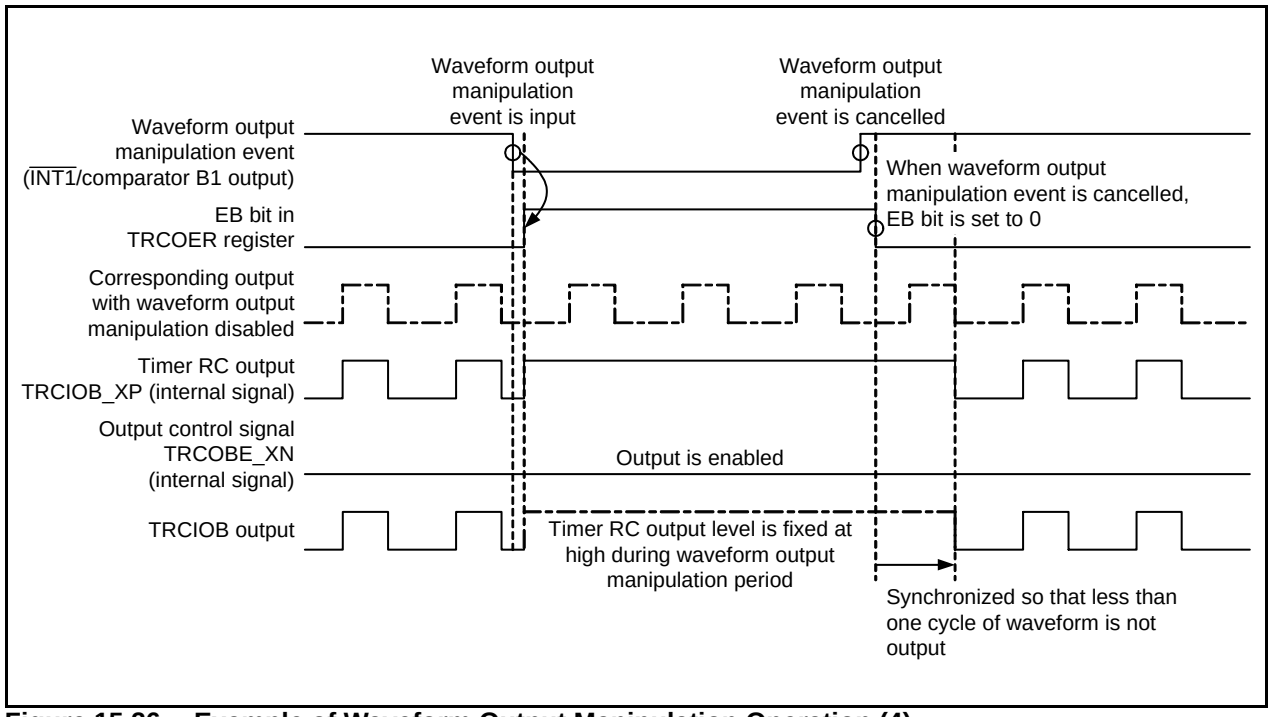


Figure 15.26 Example of Waveform Output Manipulation Operation (4)

15.5 Operation Timing

15.5.1 TRCCNT Register Count Timing

Figure 15.27 shows the Count Operation Timing.

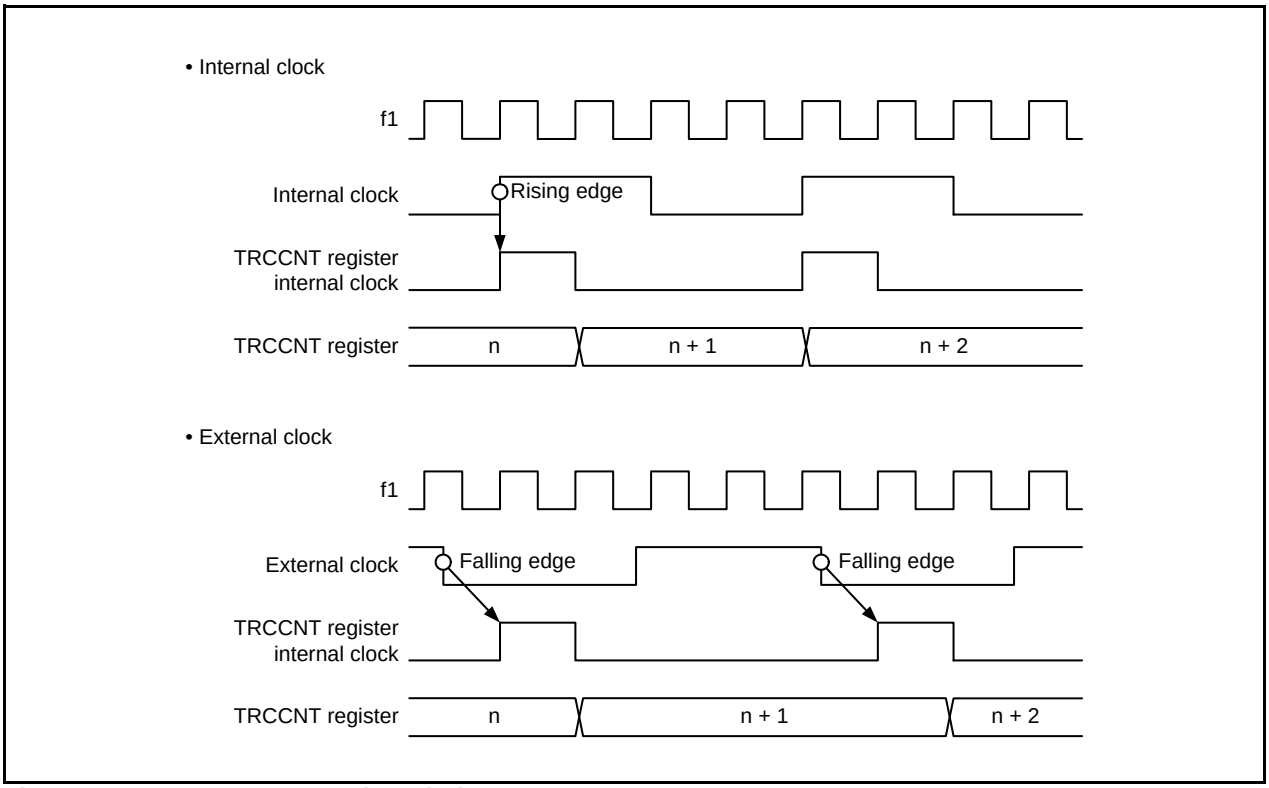


Figure 15.27 Count Operation Timing

15.5.2 Output Compare Output Timing

A compare match signal occurs at the last state (timing when the TRCCNT register updates a matched value) when the TRCCNT register and the general register match. When the compare match occurs, the output value set by the TRCIOR register is output to the output compare output pins (TRCIOA, TRCIOB, TRCIOC, and TRCIOD). After the TRCCNT register and the general register match, a compare match signal does not occur until an input clock to the TRCCNT register is generated.
Figure 15.28 shows the Output Compare Output Timing.

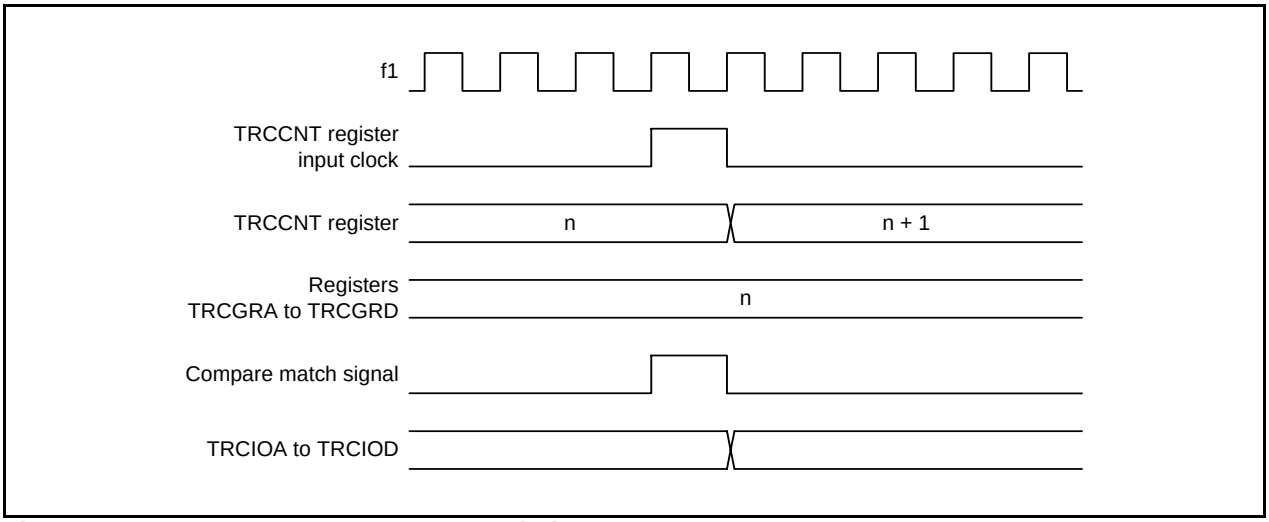


Figure 15.28 Output Compare Output Timing

15.5.3 Input Capture Input Timing

A falling edge, rising edge, or two-way edge can be selected for input capture input by setting registers TRCIOR0 and TRCIOR1.
Figure 15.29 shows the Input Capture Input Timing. This applies when a falling edge is selected.

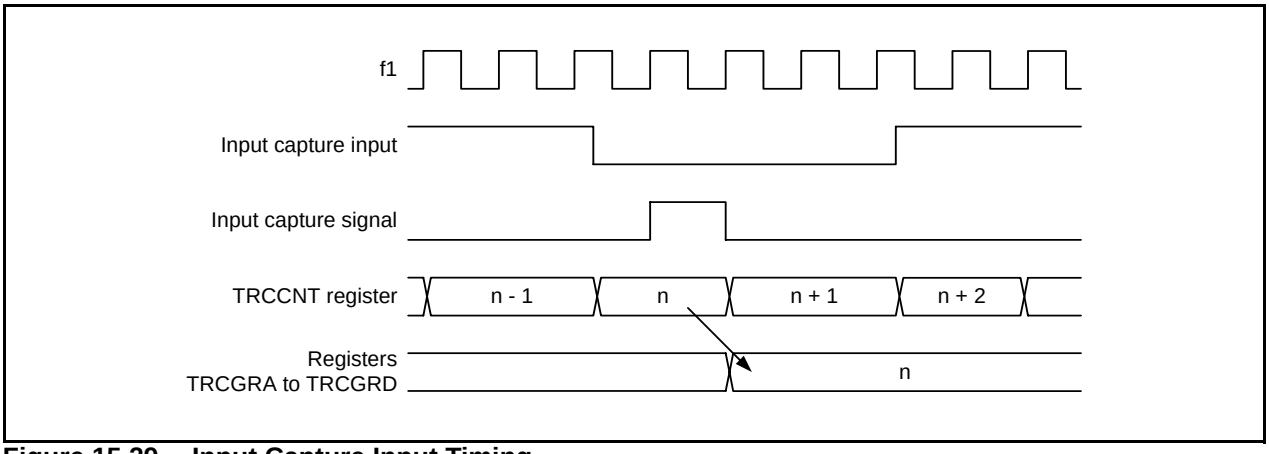


Figure 15.29 Input Capture Input Timing

15.5.4 Timing for Counter Clearing by Compare Match

Figure 15.30 shows the Timing for Counter Clearing by Compare Match. If the value in the TRCGRA register is n, the counter counts from 0 to n and the period is thus set to n + 1.

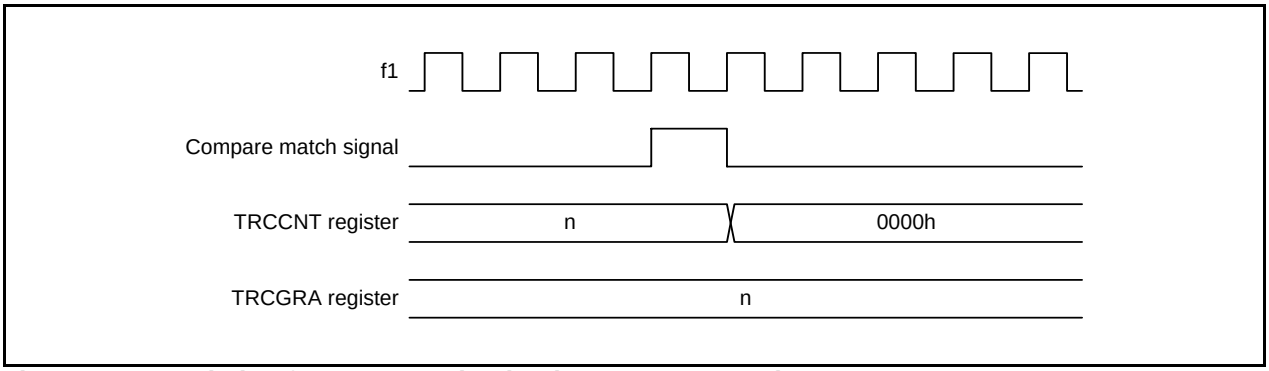


Figure 15.30 Timing for Counter Clearing by Compare Match

15.5.5 Buffer Operation Timing

Figure 15.31 shows the Buffer Operation Timing.

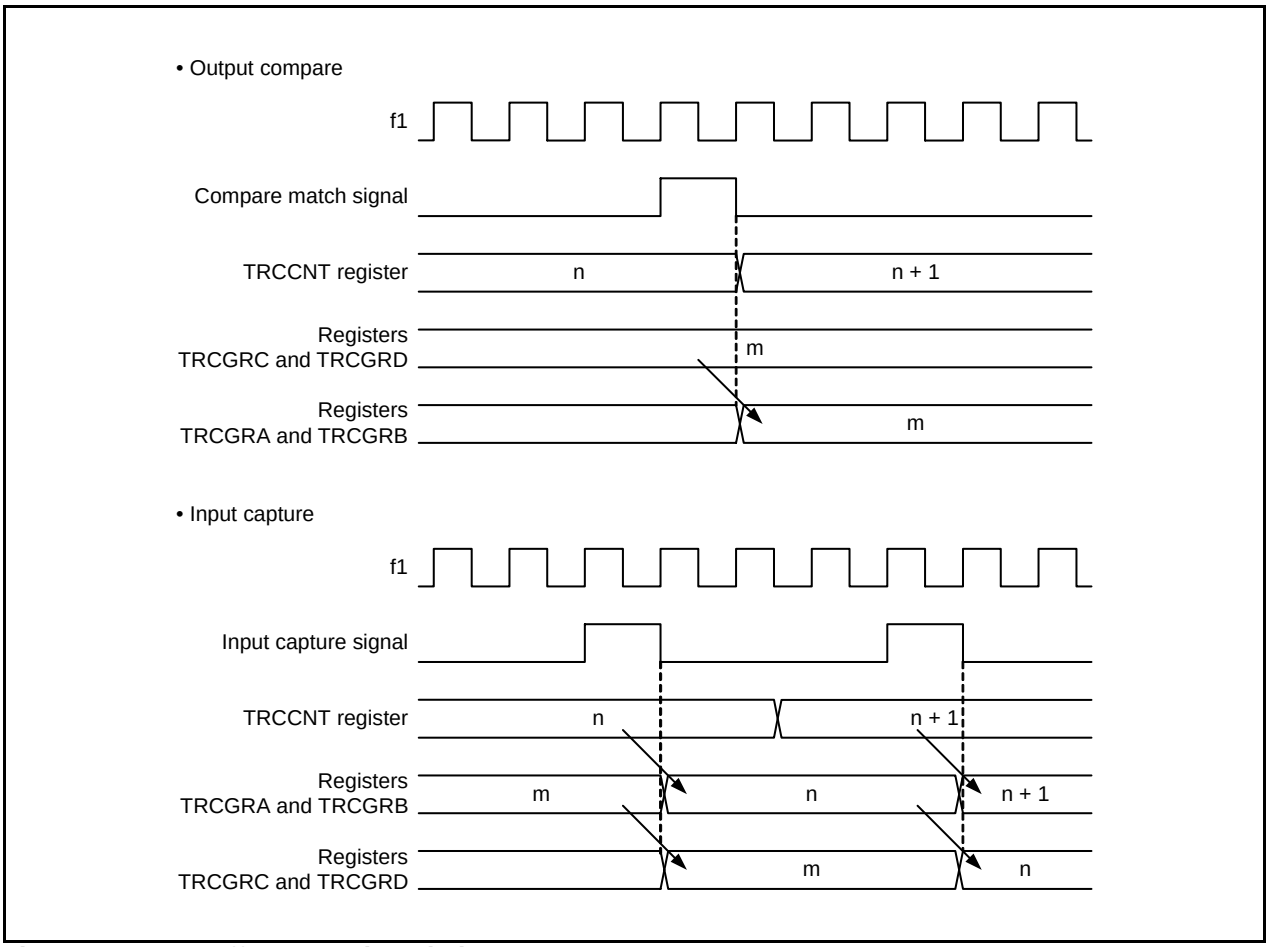


Figure 15.31 Buffer Operation Timing

15.5.6 Setting Timing at Compare Match

While the TRCSR register functions as an output compare register, bits IMFA to IMFD are set to 1 when TRCCNT register and the general registers (TRCGRA, TRCGRB, TRCGRC, TRCGRD) match.
A compare match signal occurs at the last state (timing when the TRCCNT register updates a matched value). Thus, after the TRCCNT register and the general register match, a compare match signal does not occur until an input clock to the TRCCNT register is generated.
Figure 15.32 shows the Timing at Compare Match.

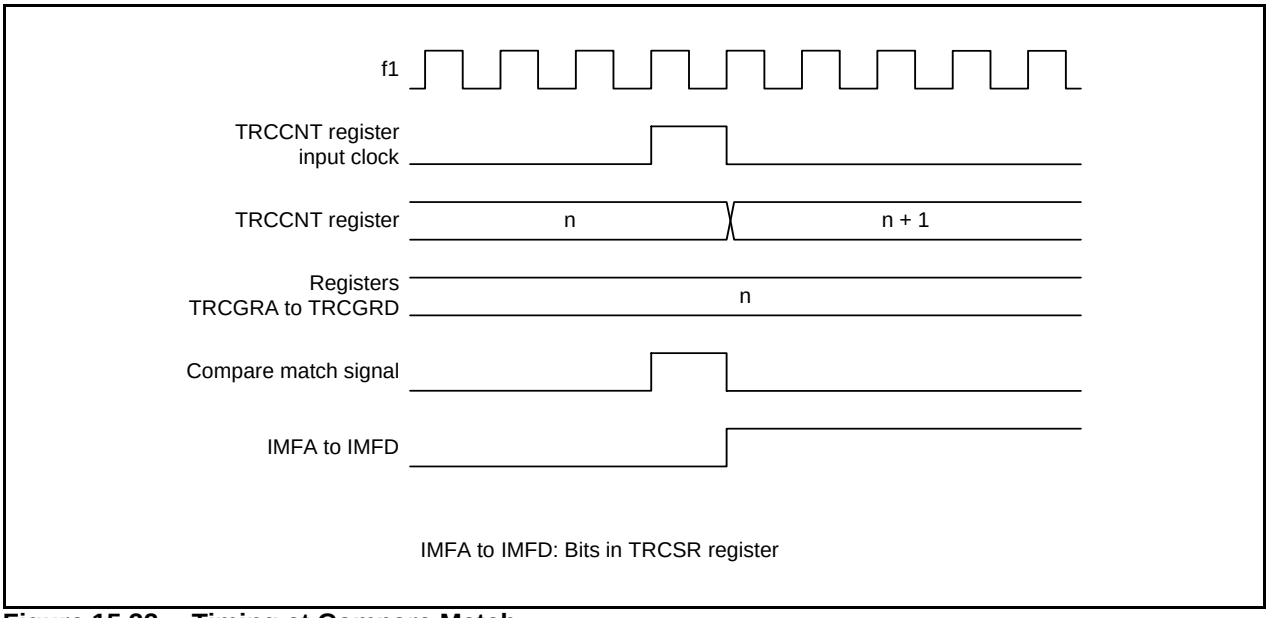


Figure 15.32 Timing at Compare Match

15.5.7 Setting Timing at Input Capture

While the TRCSR register functions as an input capture register, bits IMFA to IMFD are set to 1 when an input capture occurs.
Figure 15.33 shows the Timing at Input Capture.

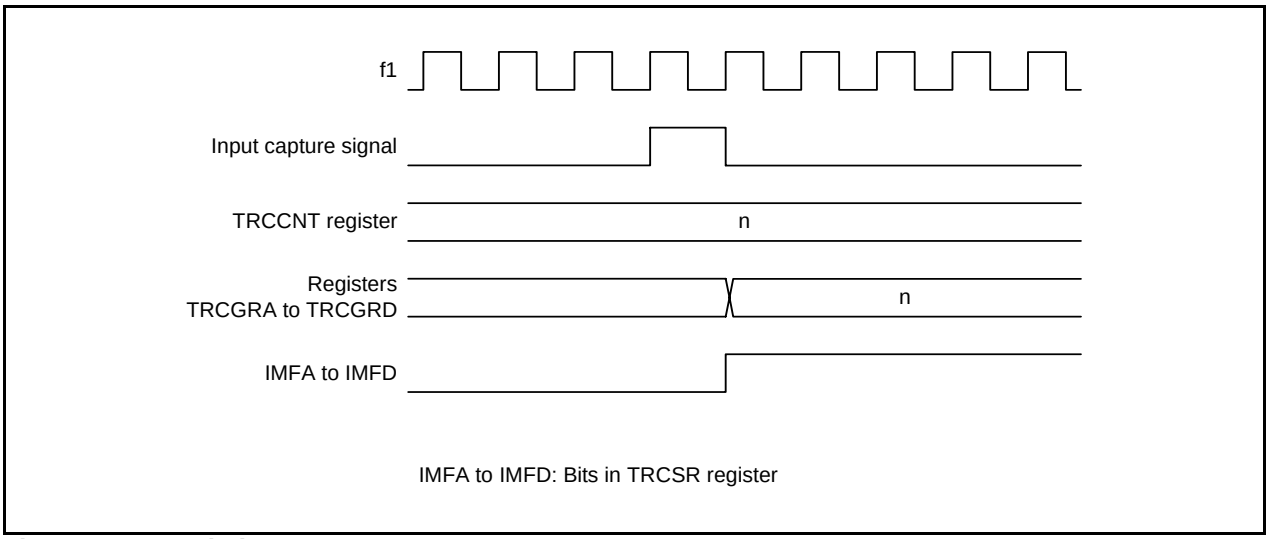


Figure 15.33 Timing at Input Capture

15.5.8 Timing for Setting Bits IMFA to IMFD and OVF to 0

Bits IMFA to IMFD and OVF are set to 0 when 0 is written after the CPU reads 1.
Figure 15.34 shows the Timing for Setting Bits IMFA to IMFD and OVF by CPU.

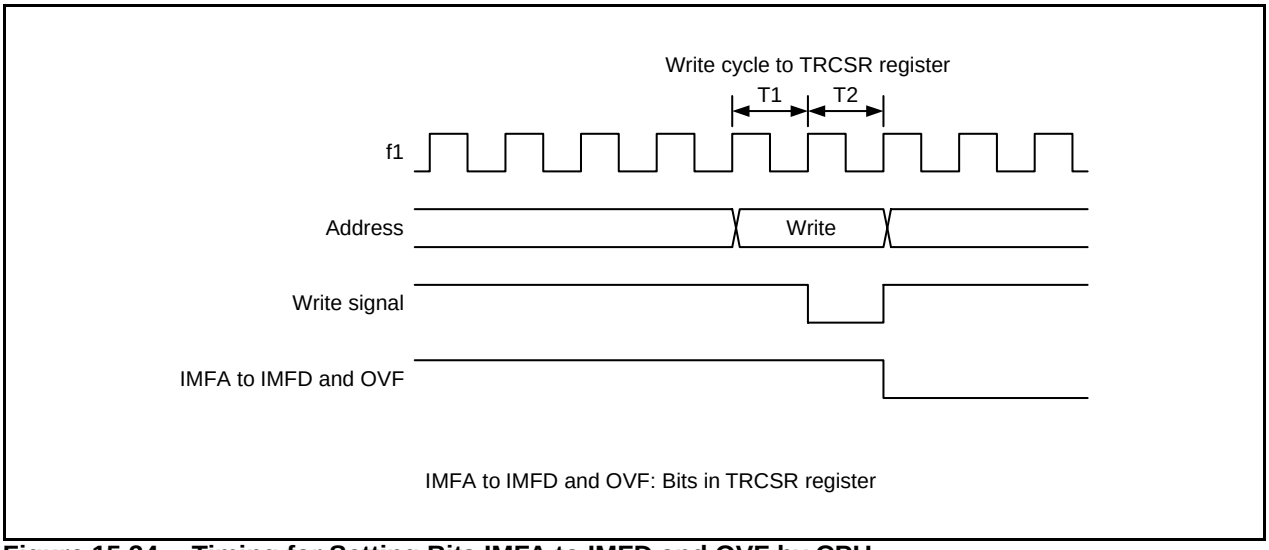


Figure 15.34 Timing for Setting Bits IMFA to IMFD and OVF by CPU

15.5.9 Timing of A/D Conversion Start Trigger due to Compare Match

Figure 15.35 shows the Timing of A/D Conversion Start Trigger due to Compare Match.

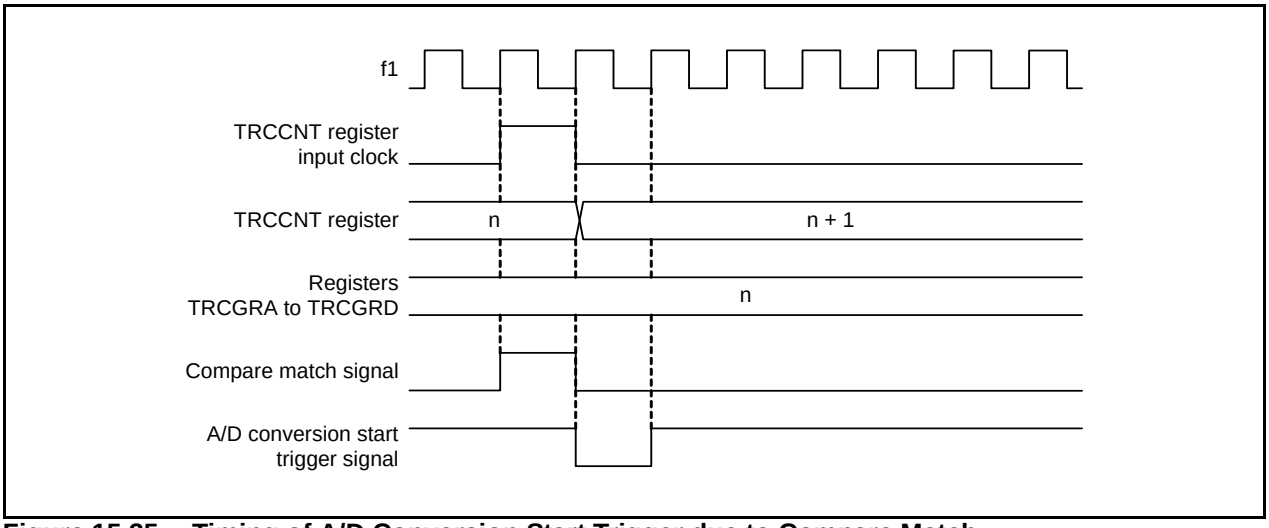


Figure 15.35 Timing of A/D Conversion Start Trigger due to Compare Match

15.6 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses bits ILVL35 and ILVL34 in the ILVL3 register, the IRTC bit in the IRR0 register, and a single vector.
Table 15.18 lists the Registers Associated with Timer RC Interrupt, and Figure 15.36 shows a Timer RC Interrupt Block Diagram.

Table 15.18 Registers Associated with Timer RC Interrupt

Timer RC Status Register	Timer RC Interrupt Enable Register	Timer RC Interrupt Control Register	Timer RC Interrupt Request Monitor Flag Register
TRCSR	TRCIER	ILVL3	IRR0

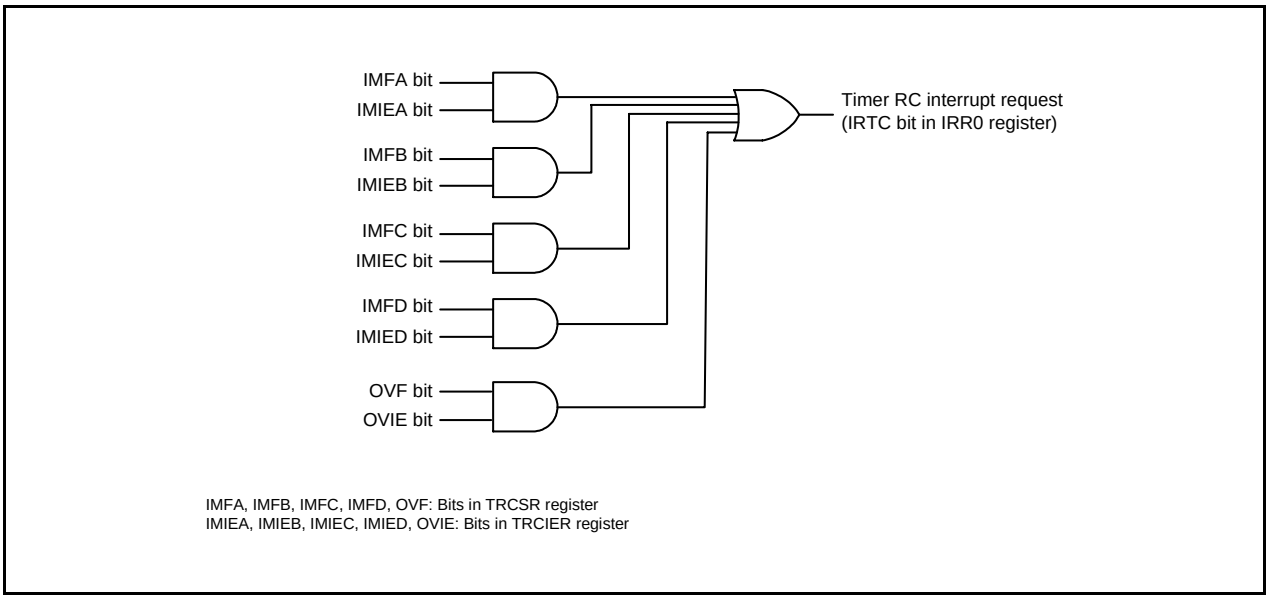


Figure 15.36 Timer RC Interrupt Block Diagram

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IRTC bit, bits ILVL35 to ILVL34, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IRTC bit in the IRR0 register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IRTC bit is set to 0 (no interrupt requested) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IRTC bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IRTC bit is set to 1, the IRTC bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **15.2.6 Timer RC Status Register (TRCSR)**, for the procedure for setting these bits to 0.

Refer to **15.2.5 Timer RC Interrupt Enable Register (TRCIER)**, for details of the TRCIER register.
Refer to **11.4 Interrupt Control**, for details of the ILVL3 register and **11.3.2 Relocatable Vector Table**, for information on interrupt vectors.

15.7 Notes on Timer RC

15.7.1 TRCCNT Register

The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A).

- When writing a value to the TRCCNT register by a program while the CTS bit in the TRCMR register is set to 1 (count is started), ensure that the write timing does not coincide with when the TRCCNT register is set to 0000h.
- If the timing when the TRCCNT register is set to 0000h and is written coincide with each other, the value is not be written and the TRCCNT register is set to 0000h.

If the TRCCNT register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.W   #XXXXh, TRCCNT      ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.W   TRCCNT, DATA        ; Read
```

15.7.2 TRCCR1 Register

To set bits CKS2 to CKS0 in the TRCCR1 register to 110b (fHOCO), set fHOCO to the clock frequency higher than the system clock frequency.

15.7.3 TRCSR Register

If the TRCSR register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.B   #XXh, TRCSR         ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.B   TRCSR, DATA         ; Read
```

15.7.4 Count Source Switching

When switching the count sources, stop the count before switching. After switching the count sources, wait for at least two cycles of the system clock before writing to the registers (at addresses 000E8h to 000FCh) associated with timer RC.

- Switching procedure

(1) Set the CTS bit in the TRCMR register to 0 (count is stopped).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of the system clock.
(4) Write to the registers (at addresses 000E8h to 000FCh) associated with timer RC.

When changing the count source from fHOCO to another source and stopping fHOCO, wait for at least two cycles of the system clock after changing the clock setting before stopping fHOCO.

- Switching procedure

(1) Set the CTS bit in the TRCMR register to 0 (count is stopped).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of the system clock.
(4) Set the HOCOE bit in the OCOCR register to 0 (high-speed on-chip oscillator off).

15.7.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 15.1 Timer RC Specifications**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 15.19 Digital Filter Circuit Block Diagram**)

- The value of the TRCCNT register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

15.7.6 TRCMR Register in PWM2 Mode

When the CSTP bit in the TRCCR2 register is 1 (increment is stopped), do not set the TRCMR register when a compare match occurs between registers TRCCNT and TRCGRA.

15.7.7 MSTCR Register

After stopping the timer RC count, set the MSTTRC bit in the MSTCR register to 1 (standby).

15.7.8 Mode Switching

- When switching the modes during operation, set the CTS bit in the TRCMR register to 0 (count is stopped) before switching.
- After switching the modes, set each flag in the TRCSR register to 0 before operation is started.

15.7.9 Procedure for Setting Registers Associated with Timer RC

Set the registers associated with timer RC following the procedure below:

(1) Set timer RC operating mode (bits PWMB, PWMC, PWMD, and PWM2 in the TRCMR register).
(2) Set the registers other than that set in (1).
(3) Set the port output to be enabled (bits EA to ED in the TRCOER register).

16. Timer RK

Timer RK is an 8-bit timer that increments by the input of the count source.

16.1 Overview

Table 16.1 lists the Timer RK Specifications. Figure 16.1 shows the Timer RK Block Diagram. Table 16.2 lists the Timer RK Pin Configuration.

Table 16.1 Timer RK Specifications

Item		Description
Count sources		f1, f2, f8, fHOCO, or an external clock (counting of an external event) can be selected.
Operating modes	Interval mode	The timer operates as an 8-bit interval timer.
	Pulse output mode	A pulse with inverted polarity is output at each timer overflow.
	Output compare mode	The count source is counted and compare matches are detected.
Interrupt		An interrupt is generated by an overflow of the counter or a compare match.
Other		Auto-reload enabled or disabled can be selected for each operating mode.

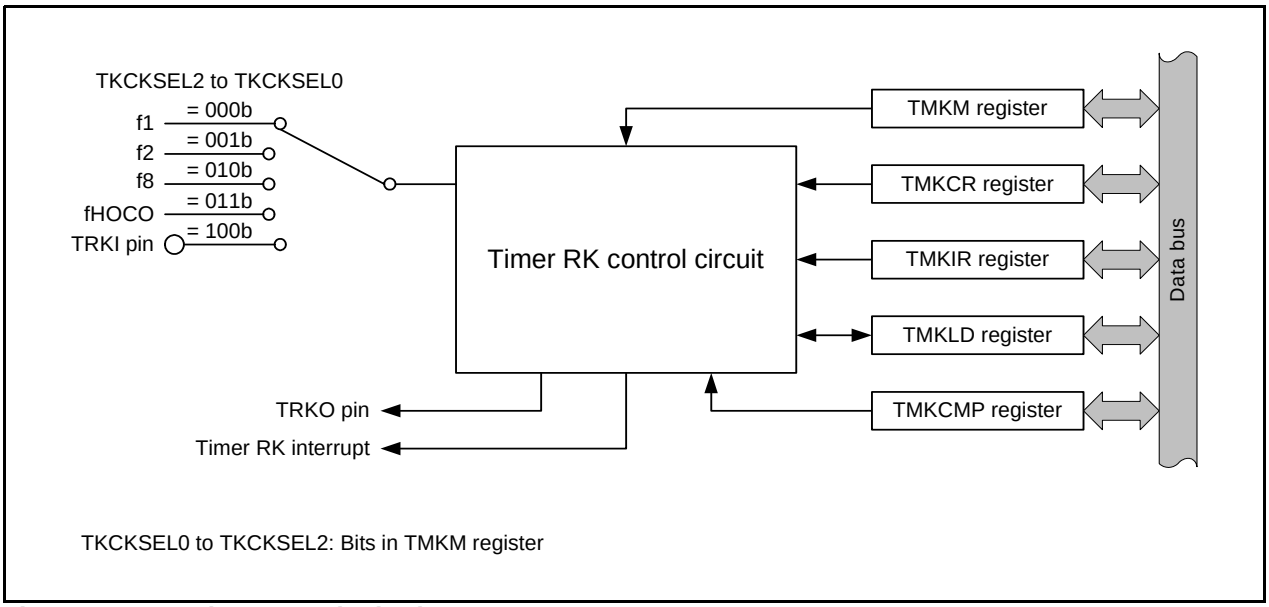


Figure 16.1 Timer RK Block Diagram

Table 16.2 Timer RK Pin Configuration

Pin Name	I/O	Function
TRKI	I	External input for timer RK
TRKO	O	Output for timer RK

16.2 Registers

Table 16.3 lists the Timer RK Register Configuration.

Table 16.3 Timer RK Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RK Mode Register	TMKM	00h	00188h	8
Timer RK Control Register	TMKCR	00h	00189h	8
Timer RK Load Register	TMKLD (TMKCNT)	00h	0018Ah	8
Timer RK Compare Match Data Register	TMKCMP	00h	0018Bh	8
Timer RK Interrupt Request and Status Register	TMKIR	00h	0018Ch	8

16.2.1 Timer RK Mode Register (TMKM)

Address 00188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TKMD1	TKMD0	TKLDM	—	—	TKCKSEL2	TKCKSEL1	TKCKSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TKCKSEL0	Timer RK count source select bits (1)	b2 b1 b0 0 0 0: f1 0 0 1: f2 0 1 0: f8 0 1 1: fHOCO 1 0 0: External clock Other than the above: Do not set.	R/W
b1	TKCKSEL1			R/W
b2	TKCKSEL2			R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	TKLDM	Auto-reload bit	0: Auto-reload disabled 1: Auto-reload enabled	R/W
b6	TKMD0	Timer RK operating mode select bits (2)	b7 b6 0 0: Interval mode 0 1: Pulse output mode 1 0: Output compare mode 1 1: Do not set.	R/W
b7	TKMD1			R/W

Notes:
1. Set the TSTART bit in the TMKCR register to 0 (count is stopped) before changing bits TKCKSEL0 to TKCKSEL2.
2. Set the TSTART bit to 0 before changing bits TKMD0 to TKMD1.

When the TMKM register is written, the output level from the TRKO pin is set to the initial output level specified by the TOLEV bit in the TMKCR register.

16.2.2 Timer RK Control Register (TMKCR)

Address 00189h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	TOLEV	IEDGE	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	IEDGE	External clock input edge select bit (1)	0: Rising edge 1: Falling edge	R/W
b6	TOLEV	Timer RK output level select bit (2)	0: Initial output is low 1: Initial output is high	R/W
b7	TSTART	Timer RK count start bit (1, 2)	0: Count is stopped 1: Count is started	R/W

Notes:
1. Set the TSTART bit to 0 (count is stopped) before changing the IEDGE bit.
2. Set the TSTART bit to 0 (count is stopped) before changing the TOLEV bit.

16.2.3 Timer RK Load Register (TMKLD (TMKCNT))

Address 0018Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TMKLD7	TMKLD6	TMKLD5	TMKLD4	TMKLD3	TMKLD2	TMKLD1	TMKLD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMKLD0	Count data bit 0	Write 8-bit count data.	R/W
b1	TMKLD1	Count data bit 1		R/W
b2	TMKLD2	Count data bit 2		R/W
b3	TMKLD3	Count data bit 3		R/W
b4	TMKLD4	Count data bit 4		R/W
b5	TMKLD5	Count data bit 5		R/W
b6	TMKLD6	Count data bit 6		R/W
b7	TMKLD7	Count data bit 7		R/W

Registers TMKCNT and TMKLD are allocated at the same address.

16.2.3.1 Timer RK Counter (TMKCNT)

The TMKCNT register is an 8-bit readable register that is incremented by the input of the count source. The TMKCNT register can be read at an arbitrary timing. When the TMKCNT register overflows (FFh to 00h or FFh to the set value of the TMKLD register), the TMKOVIF bit in the TMKIR register is set to 1 (overflow interrupt requested).

The value of the TMKCNT register after a reset is 00h.

16.2.3.2 Timer RK load Register (TMKLD)

The TMKLD register is an 8-bit write-only register that sets the reload value of the TMKCNT register. When the reload value is set in TMKLD register, the value is reloaded to the TMKCNT register at the same time and the TMKCNT register starts incrementing from the value. If the TMKCNT register overflows with auto reload enabled, the value of the TMKLD register is reloaded to the TMKCNT register. Thus, the overflow period can be set to between 1 to 256 clocks of the count source.

The value of the TMKLD register after a reset is 00h.

16.2.4 Timer RK Compare Match Data Register (TMKCMP)

Address 0018Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TMKCMP7	TMKCMP6	TMKCMP5	TMKCMP4	TMKCMP3	TMKCMP2	TMKCMP1	TMKCMP0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMKCMP0	Compare match data bit 0	Write 8-bit compare match data.	R/W
b1	TMKCMP1	Compare match data bit 1		R/W
b2	TMKCMP2	Compare match data bit 2		R/W
b3	TMKCMP3	Compare match data bit 3		R/W
b4	TMKCMP4	Compare match data bit 4		R/W
b5	TMKCMP5	Compare match data bit 5		R/W
b6	TMKCMP6	Compare match data bit 6		R/W
b7	TMKCMP7	Compare match data bit 7		R/W

16.2.5 Timer RK Interrupt Request and Status Register (TMKIR)

Address 0018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TMKOVIE	TMKOVIF	TMKCMIE	TMKCMIF	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	TMKCMIF	Timer RK compare match interrupt request flag	0: No compare match interrupt requested 1: Compare match interrupt requested	R/W
b5	TMKCMIE	Timer RK compare match interrupt enable bit	0: Compare match interrupt disabled 1: Compare match interrupt enabled	R/W
b6	TMKOVIF	Timer RK overflow interrupt request flag	0: No overflow interrupt requested 1: Overflow interrupt requested	R/W
b7	TMKOVIE	Timer RK overflow interrupt enable bit	0: Overflow interrupt disabled 1: Overflow interrupt enabled	R/W

TMKCMIF Bit (Timer RK compare match interrupt request flag)

[Condition for setting to 0]
• When 0 is written to this bit after reading it as 1.
[Condition for setting to 1]
• When timer RK is compared and matches.

TMKOVIF bit (Timer RK overflow interrupt request flag)

[Condition for setting to 0]
• When 0 is written to this bit after reading it as 1.
[Condition for setting to 1]
• When timer RK overflows.

16.3 Operation

16.3.1 Interval Mode

When bits TKMD1 to TKMD0 in the TMKM register are set to 00b (interval mode) and the TSTART bit in the TMKCR register is set to 1 (count is started), timer RK operates as an 8-bit interval timer. After a reset, timer RK stops because the TSTART bit is set to 0.
Bits TKCKSEL0 to TKCKSEL2 bit in the TMKM register can be used to select the timer RK count source among four internal clocks and an external clock from the TRKI input pin (an active edge selected by the IEDGE bit in the TMKCR register).
If the count source is input after the count value of the timer changes to FFh, timer RK overflows and the TMKOVIF bit in the TMKIR register is set to 1 (overflow interrupt requested). When the TMKOVIE bit in the TMKIR register is 1 (overflow interrupt enabled), an interrupt request signal is generated to the CPU.
At overflow, the count value of the TMKCNT register changes as follows:
• Auto-reload disabled (TKLDM bit in TMKM register = 0): 00h
• Auto-reload enabled (TKLDM bit in TMKM register = 1): TMKLD register reload value

Increment operation starts from either of the above values. When the TMKLD register is set in interval mode, the value of the TMKLD register is reloaded to the TMKCNT register at the same time.
The count value is retained while the count is stopped.
Figure 16.2 shows an Operation Example in Interval Mode.

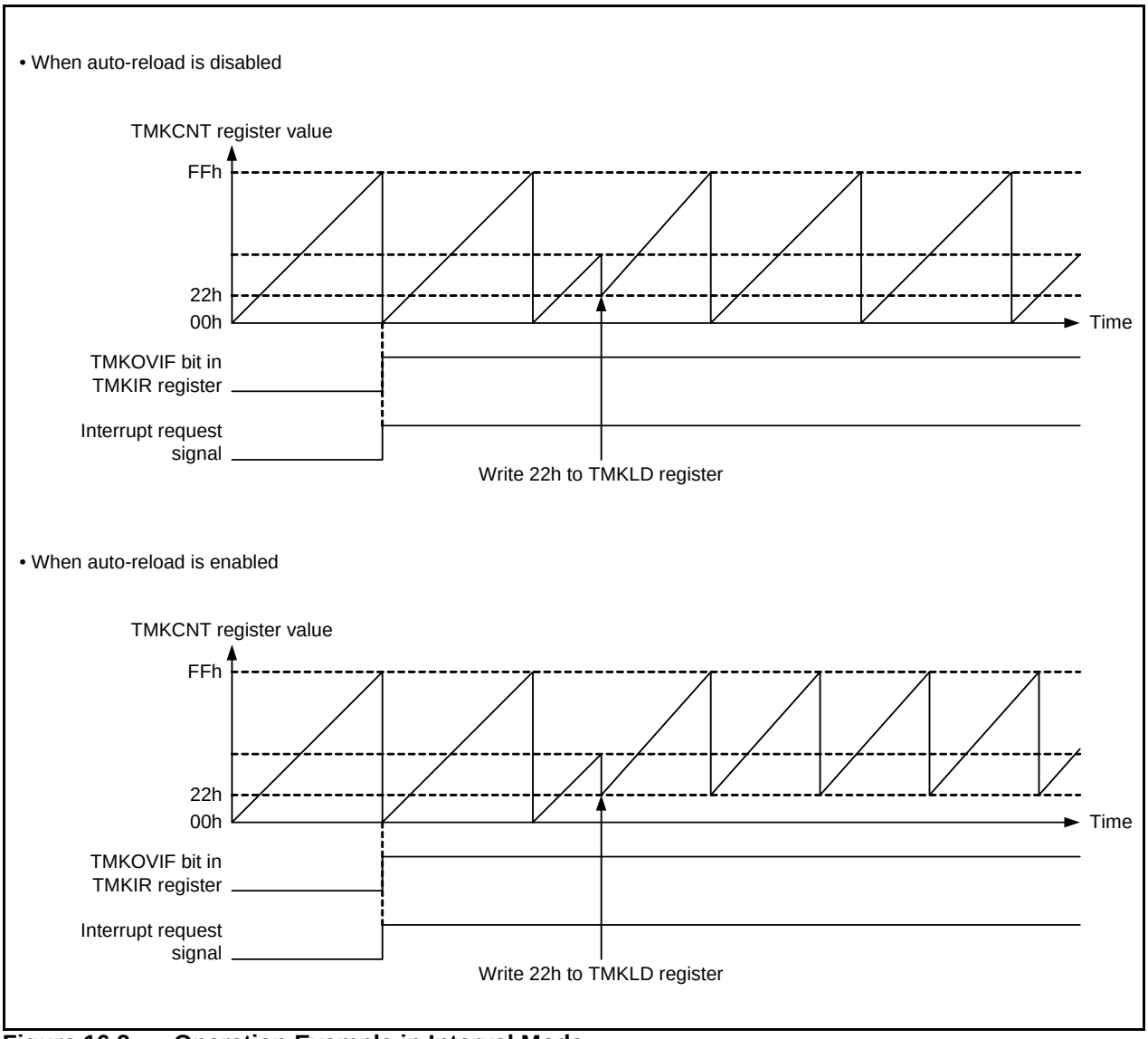


Figure 16.2 Operation Example in Interval Mode

16.3.2 Pulse Output Mode

When bits TKMD1 to TKMD0 in the TMKM register are set to 01b (pulse output mode) and the TSTART bit in the TMKCR register is set to 1 (count is started), timer RK operates as an 8-bit timer. When timer RK overflows, the output from the TRKO pin is inverted. The initial value of the output level (low or high) can be selected by the TOLEV bit in the TMKCR register.
Bits TKCKSEL0 to TKCKSEL2 bit in the TMKM register can be used to select the timer RK count source among four internal clocks and an external clock from the TRKI input pin (an active edge selected by the IEDGE bit in the TMKCR register).
If the count source is input after the count value of the timer changes to FFh, timer RK overflows and the TMKOVIF bit in the TMKIR register is set to 1 (overflow interrupt requested). When the TMKOVIE bit in the TMKIR register is 1 (overflow interrupt enabled), an interrupt request signal is generated to the CPU.
At overflow, the count value of the TMKCNT register changes as follows:
• Auto-reload disabled (TKLDM bit in TMKM register = 0): 00h
• Auto-reload enabled (TKLDM bit in TMKM register = 1): TMKLD register reload value

Increment operation starts from either of the above values. When the TMKLD register is set in pulse output mode, the value of the TMKLD register is reloaded to the TMKCNT register at the same time.
The count value is retained while the count is stopped.
Figure 16.3 shows an Operation Example in Pulse Output Mode.

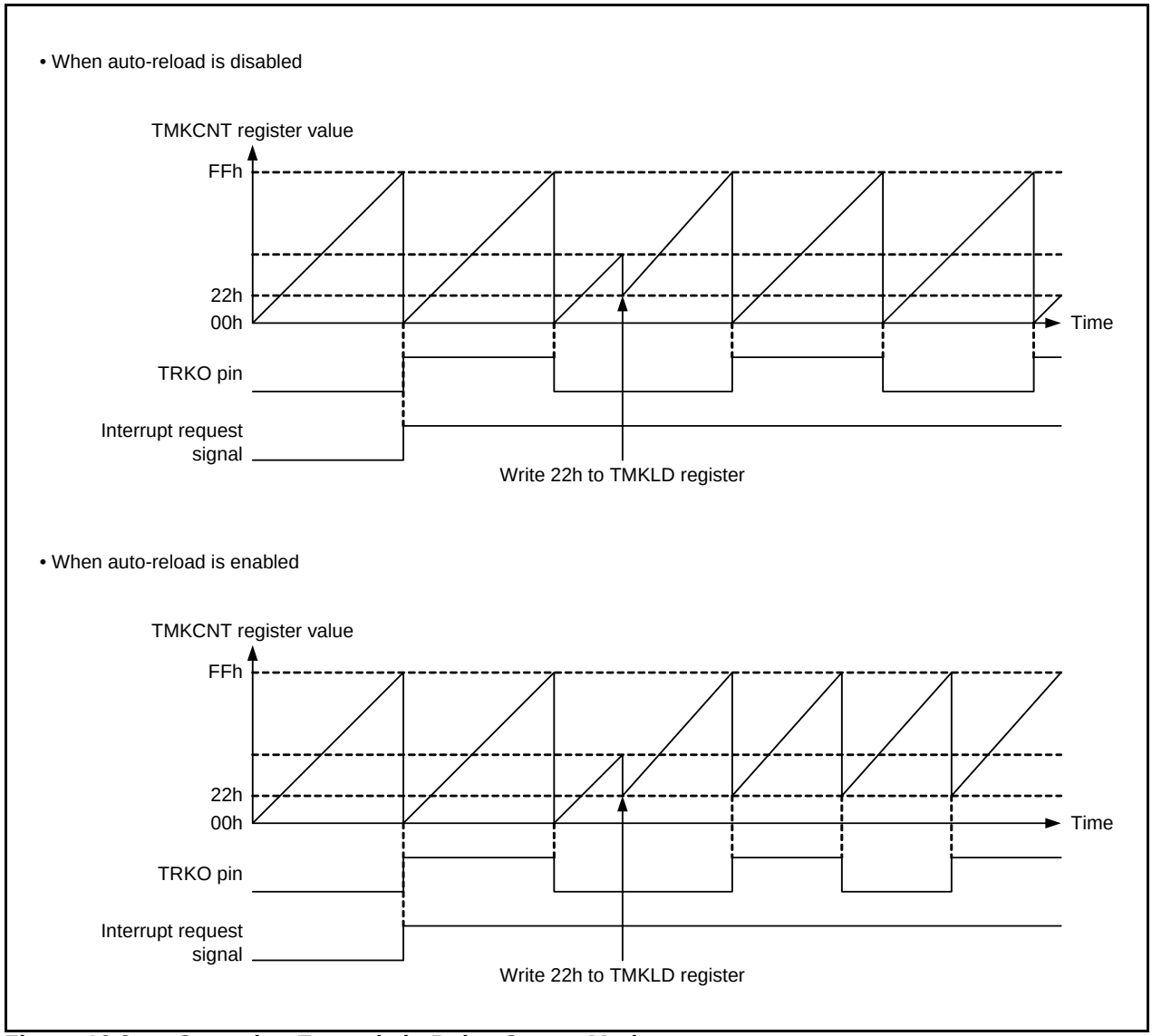


Figure 16.3 Operation Example in Pulse Output Mode

16.3.3 Output Compare Mode

When bits TKMD1 to TKMD0 in the TMKM register are set to 10b (output compare mode) and the TSTART bit in the TMKCR register is set to 1 (count is started), timer RK operates in output compare mode. When the compare value set in the TMKCMP register and the count value of timer RK match, the output from the TRKO pin is inverted. When timer RK overflows, the output from the TRKO pin is further inverted. The duty cycle and period for pulse output can be changed by rewriting the values of registers TMKLD and TMKCMP.
Bits TKCKSEL0 to TKCKSEL2 in the TMKM register are used to select the timer RK count source among four internal clocks and an external clock from the TRKI input pin (an active edge selected by the IEDGE bit in the TMKCR register).
When the contents of the 8-bit counter and the TMKCMP register match or an overflow occurs, an interrupt request signal is generated in CPU.
At overflow, the count value of the TMKCNT register changes as follows:
• Auto-reload disabled (TKLDM bit in TMKM register = 0): 00h
• Auto-reload enabled (TKLDM bit in TMKM register = 1): TMKLD register reload value

Increment operation starts from either of the above values. When the TMKLD register is set in output compare mode, the value of the TMKLD register is reloaded to the TMKCNT register at the same time.
The count value is retained while the count is stopped.
Figure 16.4 shows an Operation Example in Output Compare Mode. Table 16.4 lists the Formula for Calculating Low-Level or High-Level Width of TRKO Pin (Initial Output is Low in Output Compare Mode).

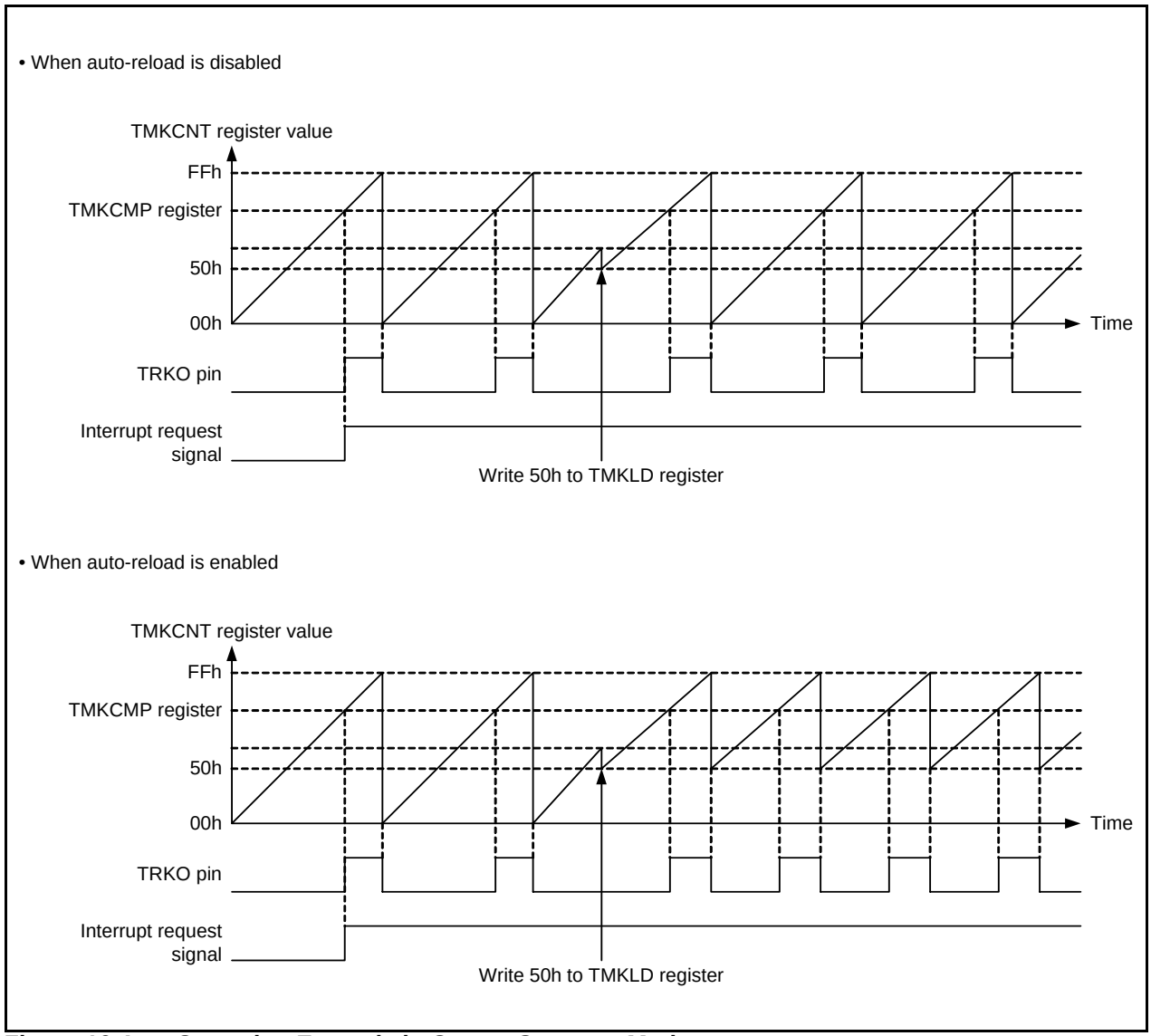


Figure 16.4 Operation Example in Output Compare Mode

Table 16.4 Formula for Calculating Low-Level or High-Level Width of TRKO Pin (Initial Output is Low in Output Compare Mode)

Auto-Reload	Values in Registers TMKLD and TMKCMP	Low-Level Width	High-Level Width
When auto-reload is disabled	TMKLD register = 00h, TMKCMP register = m (other than FFh)	m + 1	FFh – m
	TMKLD register = 00h, TMKCMP register = FFh	FFh + 1	
When auto-reload is enabled (TMKLD register ≤ TMKCMP register)	TMKLD register = n, TMKCMP register = m (other than FFh)	m – n + 1	FFh – m
	TMKLD register = n, TMKCMP register = FFh	FFh – n + 1	

16.4 Notes on Timer RK

- After writing 0 (count is stopped) to the TSTART bit in the TMKCR register during count operation, do not access the registers associated with timer RK (1) for two to three cycles of the count source.
  Note:
  1. Registers associated with timer RK: TMKM, TMKCR, TMKLD, and TMKIR
- When writing to and reading from the TMKLD register continuously while the count is stopped, insert one NOP instruction between the instructions used for writing and reading.

17. Timer RE2

17.1 Overview

Timer RE2 includes a 3-bit counter, a 4-bit counter, and an 8-bit counter.
Timer RE2 supports the following two modes:

- Real-time clock mode
  A one-second signal is generated from fXCIN and used to count seconds, minutes, hours, days of the week, days, months, and years (supporting leap years from 2000 to 2099).
- Compare match timer mode
  A count source is counted and compare matches are detected.

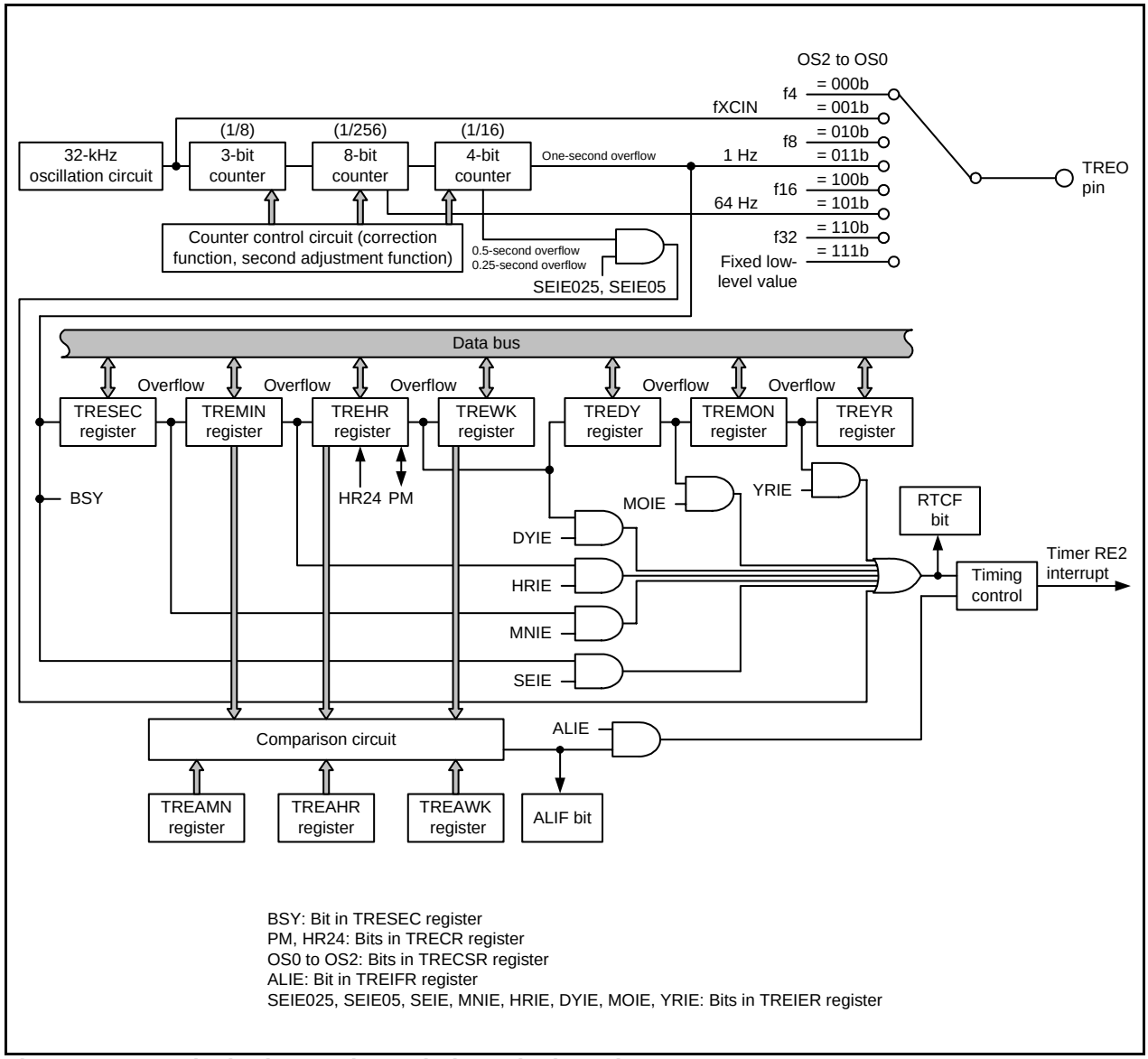
Table 17.1 lists the Real-Time Clock Mode Specifications. Table 17.2 lists the Compare Match Timer Mode Specifications. Figure 17.1 shows the Block Diagram in Real-Time Clock Mode. Figure 17.2 shows the Block Diagram in Compare Match Timer Mode. Table 17.3 lists the Timer RE2 Pin Configuration.

Table 17.1 Real-Time Clock Mode Specifications

Item	Description
Count source	fXCIN (32 kHz)
Count	Starting or stopping the count can be selected.
Reset	Reset by the RTCRST bit in the TRECR register
Interrupts	• Periodic interrupt Select one of the following: - 0.25-second period - 0.5-second period - Update of second data - Update of minute data - Update of hour data - Update of day data - Update of month data - Update of year data • Alarm interrupt When time data and alarm data match
TREO pin functions	Either of the following is selected: • Programmable I/O port • Output of f4, f8, f16, f32, 1 Hz, 64 Hz, or fXCIN
Read from and write to timer	The values of the timer RE data registers (TRESEC, TREMIN, TREHR, TREDY, TREMON, and TREYR) other than the TREWK register are represented by the BCD code.
Selectable functions	• 12-hour mode/24-hour mode switch function • Alarm function Either of following is detected: - Minutes, hours, or the day of the week - Any combination of these • Second adjustment function Reset adjustment function and 30-second adjustment function • Clock error correction function Automatic correction function or correction by software • Clock output

Table 17.2 Compare Match Timer Mode Specifications

Item	Description
Count sources	f8, f32, f128, f256, f512, f2048, f4096, or f8192
Count	Starting or stopping the count can be selected.
Reset	Reset by the RTCRST bit in the TRECR register
Interrupts	• Compare match interrupt • Overflow interrupt
TREO pin functions	Either of the following is selected: • Programmable I/O port • Output of f4, f8, f16, f32, or fXCIN • Output toggled at every compare match



BSY: Bit in TRESEC register
PM, HR24: Bits in TRECR register
OS0 to OS2: Bits in TRECSR register
ALIE: Bit in TREIFR register
SEIE025, SEIE05, SEIE, MNIE, HRIE, DYIE, MOIE, YRIE: Bits in TREIER register

Figure 17.1 Block Diagram in Real-Time Clock Mode

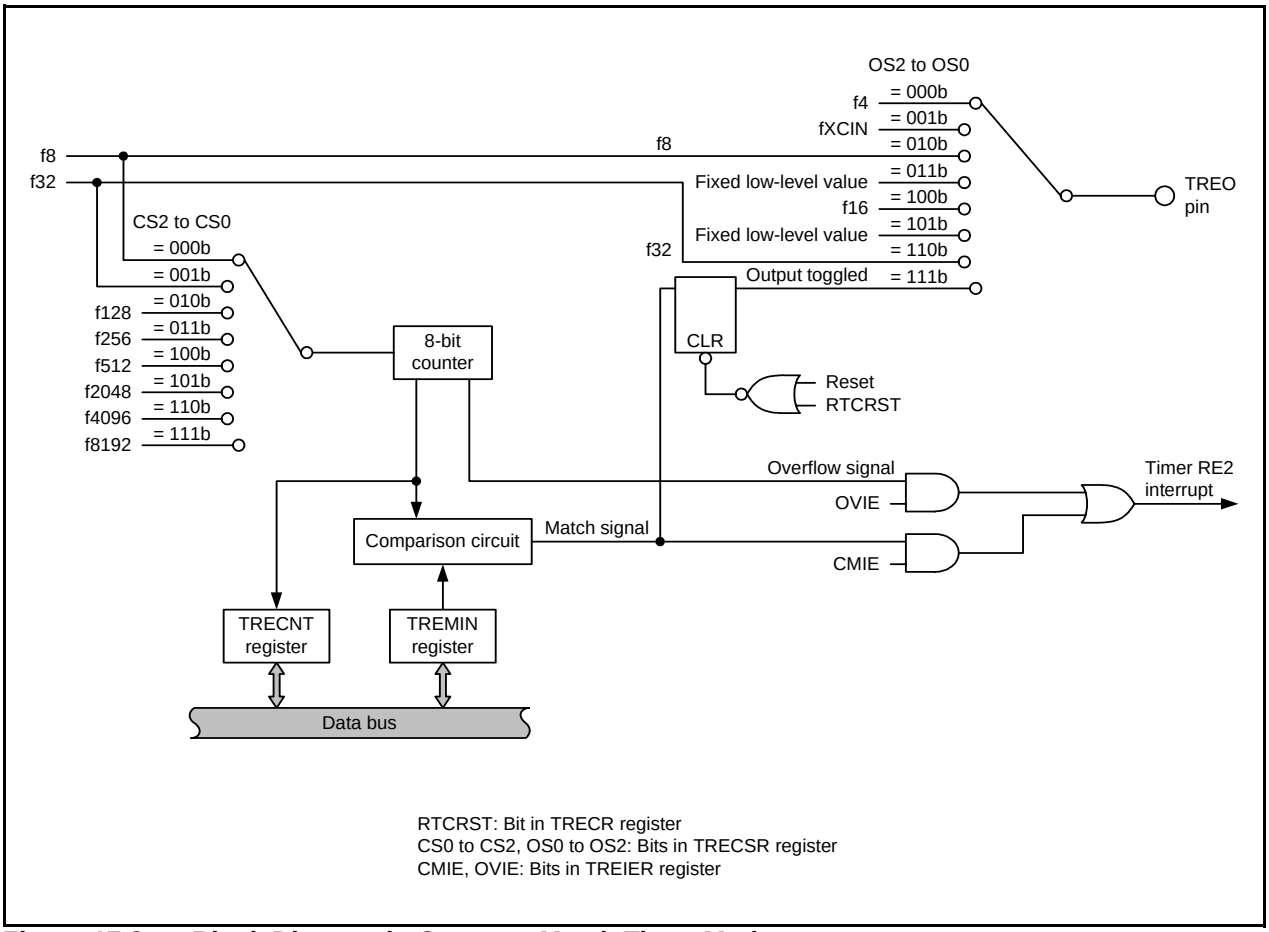


Figure 17.2 Block Diagram in Compare Match Timer Mode

Table 17.3 Timer RE2 Pin Configuration

Pin Name	I/O	Function
TREO	O	Output for timer RE2

17.2 Registers

Table 17.4 lists the Timer RE2 Register Configuration.

Table 17.4 Timer RE2 Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Timer RE Second Data Register	TRESEC	XXXXXXXXb	00130h	8
Timer RE Counter Data Register	TRECNT			
Timer RE Minute Data Register	TREMIN	XXXXXXXXb	00131h	8
Timer RE Compare Data Register				
Timer RE Hour Data Register	TREHR	00XXXXXXb	00132h	8
Timer RE Day-of-the-Week Data Register	TREWK	00000XXXb	00133h	8
Timer RE Day Data Register	TREDY	00XXXXXXb	00134h	8
Timer RE Month Data Register	TREMON	000XXXXXb	00135h	8
Timer RE Year Data Register	TREYR	XXXXXXXXb	00136h	8
Timer RE Control Register	TRECR	XXX00X0Xb	00137h	8
Timer RE Count Source Select Register	TRECSR	X0001000b	00138h	8
Timer RE Clock Error Correction Register	TREADJ	XXXXXXXXb	00139h	8
Timer RE Interrupt Flag Register	TREIFR	00000XXXb	0013Ah	8
Timer RE Interrupt Enable Register	TREIER	XXXXXXXXb	0013Bh	8
Timer RE Alarm Minute Register	TREAMN	XXXXXXXXb	0013Ch	8
Timer RE Alarm Hour Register	TREAHR	XXXXXXXXb	0013Dh	8
Timer RE Alarm Day-of-the-Week Register	TREAWK	X0000XXXb	0013Eh	8
Timer RE Protect Register	TREPRC	00000000b	0013Fh	8

17.2.1 Timer RE Second Data Register (TRESEC) in Real-Time Clock Mode

Address 00130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BSY	SC12	SC11	SC10	SC03	SC02	SC01	SC00
After Reset	X	X	X	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	SC00	First digit of second count bits	Count from 0 to 9 every second. When the digit increments, 1 is added to the second digit of seconds.	0 to 9 (BCD code)	R/W
b1	SC01				R/W
b2	SC02				R/W
b3	SC03				R/W
b4	SC10	Second digit of second count bits	When counting from 0 to 5, 60 seconds are counted.	0 to 5 (BCD code)	R/W
b5	SC11				R/W
b6	SC12				R/W
b7	BSY	Timer RE busy flag	This bit is set to 1 while timer RE data registers (1) or the PM bit in the TRECR register is updated.		R

Note:
1. Timer RE data registers: TRESEC, TREMIN, TREHR, TREWK, TREDY, TREMON, and TREYR

Set the PROTECT bit in the TREPRC register to 1 (write enabled) before rewriting the TRESEC register.

Bits SC00 to SC03 (First digit of second count bits)
Bits SC10 to SC12 (Second digit of second count bits)

Set values from 00 to 59 by the BCD code.
Read or write to these bits when the BSY bit is to 0 (data not being updated).

BSY Bit (Timer RE busy flag)

This bit is set to 1 while data is updated. Read the following registers or bit when this bit is 0 (data not being updated):
- Timer RE data registers
  (TRESEC, TREMIN, TREHR, TREWK, TREDY, TREMON, and TREYR)
- Bits PM and HR24 in the TRECR register

Write to the following registers or bits when the BSY bit is 0 (data not being updated):
- Timer RE data registers
  (TRESEC, TREMIN, TREHR, TREWK, TREDY, TREMON, and TREYR)
- Timer RE alarm registers (TREAMN, TREAHR, and TREAWK)
- Bits PM and HR24 in the TRECR register
- Registers and bits associated with correction
  (The AADJE bit in the TRECR register, the AADJM bit in the TRECSR register, and the TREADJ register)

17.2.2 Timer RE Counter Data Register (TRECNT) in Compare Match Timer Mode

Address 00130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Function	R/W
b7 to b0	The data of the 8-bit counter can be read. The count value is retained even if timer RE stops counting. When the CCLR bit in the TRECR register is 0, the count continues even if a compare match occurs, and the TRECNT register is set to 00h when the CCLR bit is 1.	R

17.2.3 Timer RE Minute Data Register (TREMIN) in Real-Time Clock Mode

Address 00131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MN7	MN12	MN11	MN10	MN03	MN02	MN01	MN00
After Reset	X	X	X	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	MN00	First digit of minute count bits	Count from 0 to 9 every minute. When the digit increments, 1 is added to the second digit of minutes.	0 to 9 (BCD code)	R/W
b1	MN01				R/W
b2	MN02				R/W
b3	MN03				R/W
b4	MN10	Second digit of minute count bits	When counting from 0 to 5, 60 minutes are counted.	0 to 5 (BCD code)	R/W
b5	MN11				R/W
b6	MN12				R/W
b7	MN7	Set to 0.			R/W

Set the PROTECT bit in the TREPRC register to 1 (write enabled) before rewriting the TREMIN register.

Bits MN00 to MN03 (First digit of minute count bits)
Bits MN10 to MN12 (Second digit of minute count bits)

Set values from 00 to 59 by the BCD code.
When the digit increments from the TRESEC register, 1 is added.
Read or write to these bits when the BSY bit in the TRESEC register is 0 (data not being updated).

17.2.4 Timer RE Compare Data Register (TREMIN) in Compare Match Timer Mode

Address 00131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MN7	MN6	MN5	MN4	MN3	MN2	MN1	MN0
After Reset	X	X	X	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MN0	Compare data bit 0	The 8-bit compare data is stored. Write the compare value.	R/W
b1	MN1	Compare data bit 1		R/W
b2	MN2	Compare data bit 2		R/W
b3	MN3	Compare data bit 3		R/W
b4	MN4	Compare data bit 4		R/W
b5	MN5	Compare data bit 5		R/W
b6	MN6	Compare data bit 6		R/W
b7	MN7	Compare data bit 7		R/W

The TREMIN register is always compared with the TRECNT register, and the CMIF bit in the TREIFR register is set to 1 (interrupt requested) when the values of both the registers match. When the CMIE bit in the TREIER register is 1 (compare match interrupt enabled), an interrupt request is generated.
Write to the TREMIN register when the RUN bit in the TRECR register is 0 (count is stopped).

17.2.5 Timer RE Hour Data Register (TREHR)

Address 00132h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	HR11	HR10	HR03	HR02	HR01	HR00
After Reset	0	0	X	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	HR00	First digit of hour count bits	Count from 0 to 9 every hour. When the digit increments, 1 is added to the second digit of hours.	0 to 9 (BCD code)	R/W
b1	HR01				R/W
b2	HR02				R/W
b3	HR03				R/W
b4	HR10	Second digit of hour count bits	Count from 0 to 1 when the HR24 bit in the TRECR register is 0 (12-hour mode). Count from 0 to 2 when the HR24 bit is 1 (24-hour mode).	0 to 2 (BCD code)	R/W
b5	HR11				R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.			—
b7	—				

The TREHR register is used in real-time clock mode.
Set the PROTECT bit in the TREPRC register to 1 (write enabled) before rewriting the TREHR register.

Bits HR00 to HR03 (First digit of hour count bits)
Bits HR10 to HR11 (Second digit of hour count bits)

Set values from 00 to 11 by the BCD code when the HR24 bit in the TRECR register is 0 (12-hour mode). Set values from 00 to 23 by the BCD code when the HR24 bit is 1 (24-hour mode).
When the digit increments from the TREMIN register, 1 is added.
Read or write to these bits when the BSY bit in the TRESEC register is 0 (data not being updated).

17.2.6 Timer RE Day-of-the-Week Data Register (TREWK)

Address 00133h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	WK2	WK1	WK0
After Reset	0	0	0	0	0	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	WK0	Day-of-the-week count bits	b2 b1 b0 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Do not set.	R/W
b1	WK1			R/W
b2	WK2			R/W
b3	—	Reserved	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	—			

The TREWK register is used in real-time clock mode.
Set the PROTECT bit in the TREPRC register to 1 (write enabled) before rewriting the TREWK register.

Bits WK0 to WK2 (Day-of-the-week count bits)

A week is counted by counting from 000b (Sunday) to 110b (Saturday) repeatedly. These bits do not change to 111b. Do not set these bits to 111b.
When the digit increments from the TREHR register, 1 is added.
Read or write to these bits when the BSY bit in the TRESEC register is 0 (data not being updated).

17.2.7 Timer RE Day Data Register (TREDY)

Address 00134h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	DY11	DY10	DY03	DY02	DY01	DY00
After Reset	0	0	X	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	DY00	First digit of day count bits	Count from 0 to 9 every day. When the digit increments, 1 is added to the second digit of day.	0 to 9 (BCD code)	R/W
b1	DY01				R/W
b2	DY02				R/W
b3	DY03				R/W
b4	DY10	Second digit of day count bits	Count from 0 to 3.	0 to 3 (BCD code)	R/W
b5	DY11				R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.			—
b7	—				

The TREDY register is used in real-time clock mode.
Set the PROTECT bit in the TREPRC register to 1 (write enabled) before rewriting the TREDY register.

Bits DY00 to DY03 (First digit of day count bits)
Bits DY10 to DY11 (Second digit of day count bits)

Set values from 01 to 31 by the BCD code.
When the digit increments from the TREHR register, 1 is added. These bits are used to count the number of the days (28 to 31) in each month, including February in a leap year, for years from 2000 to 2099.
Read or write to these bits when the BSY bit in the TRESEC register is 0 (data not being updated).

17.2.8 Timer RE Month Data Register (TREMON)

Address 00135h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	MO10	MO03	MO02	MO01	MO00
After Reset	0	0	0	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	MO00	First digit of month count bits	Count from 0 to 9 every month. When the digit increments, 1 is added to the second digit of month.	0 to 9 (BCD code)	R/W
b1	MO01				R/W
b2	MO02				R/W
b3	MO03				R/W
b4	MO10	Second digit of month count bit	Count from 0 to 1.	0 to 1 (BCD code)	R/W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.			—
b6	—				
b7	—				

The TREMON register is used in real-time clock mode.
Set the PROTECT in the TREPRC register to 1 (write enabled) before rewriting the TREMON register.

Bits MO00 to MO03 (First digit of month count bits)
MO10 Bit (Second digit of month count bit)

Set values from 01 to 12 by the BCD code.
When the digit increments from the TREDY register, 1 is added.
Read or write to these bits when the BSY bit in the TRESEC register is 0 (data not being updated).

17.2.9 Timer RE Year Data Register (TREYR)

Address 00136h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	YR13	YR12	YR11	YR10	YR03	YR02	YR01	YR00
After Reset	X	X	X	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	YR00	First digit of year count bits	Count from 0 to 9 every hour. When the digit increments, 1 is added to the second digit of year.	0 to 9 (BCD code)	R/W
b1	YR01				R/W
b2	YR02				R/W
b3	YR03				R/W
b4	YR10	Second digit of year count bits	Count from 0 to 9.	0 to 9 (BCD code)	R/W
b5	YR11				R/W
b6	YR12				R/W
b7	YR13				R/W

The TREYR register is used in real-time clock mode.
Set the PROTECT bit in the TREPRC register to 1 (write enabled) before rewriting the TREYR register.

Bits YR00 to YR03 (First digit of year count bits)
Bits YR10 to YR13 (Second digit of year count bits)

Set values from 00 to 99 by the BCD code. Fourth digit and third digit of the year are fixed to 20. Years from 2000 to 2099 can be indicated.
When the digit increments from the TREMON register, 1 is added.
Read or write to these bits when the BSY bit in the TRESEC register is 0 (data not being updated).

17.2.10 Timer RE Control Register (TRECR) in Real-Time Clock Mode

Address 00137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RUN	HR24	PM	RTCRST	CCLR	LFLAG	—	AADJE
After Reset	X	X	X	0	0	X	0	X
After reset by RTCRST bit in TRECR register	0	0	0	X	X	1	X	0

Bit	Symbol	Bit Name	Function	R/W
b0	AADJE	Timer RE automatic correction function enable bit	0: Automatic correction function disabled (correction by software enabled) 1: Automatic correction function enabled (correction by software disabled)	R/W
b1	—	Reserved	Set to 0.	R/W
b2	LFLAG	Leap year flag (1)	0: Ordinary year 1: Leap year	R
b3	CCLR	Set to 0.		R/W
b4	RTCRST	Timer RE reset bit (2)	When this bit is set to 1, the registers and bits listed in Table 17.5 are initialized and the counter control circuit is initialized.	R/W
b5	PM	a.m./p.m. bit	0: a.m. 1: p.m.	R/W
b6	HR24	Operating mode select bit	0: 12-hour mode 1: 24-hour mode	R/W
b7	RUN	Timer RE operation start bit	0: Count is stopped 1: Count is started	R/W

Notes:
1. When the RTCRST bit is set to 1, the TREYR register is set to 00h. As year 2000 is a leap year, the initial value of the LFLAG bit is set to 1.
2. Set the RTCRST bit to 0 after setting it to 1.

AADJE Bit (Timer RE automatic correction function enable bit)

Change this bit when the BSY bit in the TRESEC register is 0 (data not being updated).

LFLAG Bit (Leap year flag)

The LFLAG bit is set to 1 (leap year) when the value of the TREYR register is 00h or a multiple of four. When the LFLAG bit is set to 1, the number of days in February becomes 29.
Read this bit when the BSY bit in the TRESEC register is 0 (data not being updated).

RTCRST Bit (Timer RE reset bit)

When the RTCRST bit is set to 1, the registers and bits listed in Table 17.5 are initialized and the counter control circuit is initialized. Set the RTCRST bit to 0 after setting it to 1.

Table 17.5 Registers and Bits (1) Initialized by RTCRST Bit

Register	Bit to be Initialized	Bit to Retain Setting Value
Timer RE data registers (2)	Bits 0 to 7	—
Timer RE alarm registers (3)	Bits 0 to 7	—
TRECR	AADJE, LFLAG, PM, HR24, RUN	Bit 1, CCLR, RTCRST
TRECSR	Bit 7	Bits 0 to 6
TREADJ	Bits 0 to 7	—
TREIFR	Bits 0 to 2, 7	Bits 3 to 6
TREIER	Bits 0 to 7	—
TREPRC	Bits 0 to 7	—

Notes:
1. For the corresponding values, see each register value after a reset by the RTCRST bit.
2. Timer RE data registers: TRESEC, TREMIN, TREHR, TREWK, TREDY, TREMON, and TREYR
3. Timer RE alarm registers: TREAMN, TREAHR, and TREAWK

PM Bit (a.m./p.m. bit)

Set the PROTECT bit in the TREPRC register to 1 (write enabled) before rewriting the PM bit.
Read or write to the PM bit when the BSY bit in the TRESEC register is 0 (data not being updated).
The PM bit is enabled when the HR24 bit is 0 (12-hour mode).
The PM bit changes as follows during count operation.
• Changes to 0 when the PM bit is 1 (p.m.) and the clock increments from 11:59:59 to 00:00:00.
• Changes to 1 when the PM bit is 0 (a.m.) and the clock increments from 11:59:59 to 00:00:00.
Figure 17.3 shows the Definition of Time Representation.

<When the count starts from 0 a.m. of Saturday on January 1, 2000>

Noon

HR24 bit = 1 (24-hour mode)	TREHR register	0	1	···	10	11	12	13	···	22	23	0	1	2	···	21	22	23	0	1	2
	PM bit	0																			
HR24 bit = 0 (12-hour mode)	TREHR register	0	1	···	10	11	0	1	···	10	11	0	1	2	···	9	10	11	0	1	2
	PM bit	0 (a.m.)					1 (p.m.)					0 (a.m.)			···	1 (p.m.)			0 (a.m.)		
TREWK register		110 (Sat.)										000 (Sun.)			···	001 (Mon.)			010 (Tue.)		
TREDY register		Day 1										Day 2			···	Day 31			Day 1		
TREMON register		January																	February		
TREYR register		Year 2000																			
LFLAG bit		1																			

HR24 bit = 1 (24-hour mode)	TREHR register	3	4	5	···	21	22	23	0	1	2	···	21	22	23	0	1	2	···
	PM bit	0																	
HR24 bit = 0 (12-hour mode)	TREHR register	3	4	5	···	21	10	11	0	1	2	···	9	10	11	0	1	2	···
	PM bit	0 (a.m.)			···	1 (p.m.)			0 (a.m.)			···	1 (p.m.)			0 (a.m.)			···
TREWK register		010 (Tue.)			···	010 (Tue.)			011 (Wed.)			···	000 (Sun.)			001 (Mon.)			···
TREDY register		Day 1			···	Day 29			Day 1			···	Day 31			Day 1			···
TREMON register		February							March			···	December			January			···
TREYR register		Year 2000														Year 2001			···
LFLAG bit		1														0			···

LFLAG, PM, HR24: Bits in TRECR register

Figure 17.3 Definition of Time Representation

HR24 Bit (Operating mode select bit)

When the HR24 bit is set to 0 (12-hour mode), the TREHR register counts from 0 to 11. When this bit is set to 1 (24-hour mode), the register counts from 0 to 23. Read or write to the HR24 bit when the BSY bit in the TRESEC register is 0 (data not being updated).

17.2.11 Timer RE Control Register (TRECR) in Compare Match Timer Mode

Address 00137h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RUN	HR24	PM	RTCRST	CCLR	LFLAG	—	AADJE
After Reset	X	X	X	0	0	X	0	X
After reset by RTCRST bit in TRECR register	0	0	0	X	X	1	X	0

Bit	Symbol	Bit Name	Function	R/W
b0	AADJE	Set to 0.		R/W
b1	—	Reserved	Set to 0.	R/W
b2	LFLAG	Set to 0.		R
b3	CCLR	Counter clear enable bit	0: TRECNT register initialization by compare match is disabled 1: TRECNT register initialization by compare match is enabled	R/W
b4	RTCRST	Timer RE reset bit (1)	0: Normal operation 1. The registers (2) are initialized and the counter control circuit is initialized.	R/W
b5	PM	Set to 0.		R/W
b6	HR24			R/W
b7	RUN	Timer RE operation start bit	0: Count is stopped 1: Count is started	R/W

Notes:
1. Set the RTCRST bit to 0 after setting it to 1. For the initialized values, see each register value after a reset by the RTCRST bit.
2. Registers listed in Table 17.5.

CCLR Bit (Counter clear enable bit)

Change this bit when the RUN bit is set to 0 (count is stopped).
When registers TRECNT and TREMIN are compared and match, the CCLR bit is used to select whether to initialize the TRESEC register. This bit is enabled only when the CS3 bit in the TRECSR register is 0.

17.2.12 Timer RE Count Source Select Register (TRECSR) in Real-Time Clock Mode

Address 00138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	AADJM	OS2	OS1	OS0	CS3	CS2	CS1	CS0
After Reset	X	0	0	0	1	0	0	0
After reset by RTCRST bit in TRECR register	0	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	CS0	Count source select bits	Set to 1000b (fXCIN) in real-time clock mode (CS3 bit = 1).	R/W
b1	CS1			R/W
b2	CS2			R/W
b3	CS3			R/W
b4	OS0	Timer RE output select bits	b6 b5 b4 0 0 0: f4 0 0 1: fXCIN 0 1 0: f8 0 1 1: 1 Hz (1, 3) 1 0 0: f16 1 0 1: 64 Hz (2, 3) 1 1 0: f32 1 1 1: Do not set.	R/W
b5	OS1			R/W
b6	OS2			R/W
b7	AADJM	Automatic correction mode select bit	0: Corrected every minute 1: Corrected every 10 seconds	R/W

Notes:
1. When fC-TRH = 32.768 kHz
   When fC-TRH ≠ 32.768 kHz, the output frequency may vary from 1 Hz.
2. When fC-TRH = 32.768 kHz
   When fC-TRH ≠ 32.768 kHz, the output frequency may vary from 64 Hz.
3. When the second adjustment or clock error correction is used, the output frequency may vary depending on the timing.

Bits CS0 to CS3 (Count source select bits)

Change these bits when the RUN bit in the TRECR register is 0 (count is stopped).

Bits OS0 to OS2 (Timer RE output select bits)

Change these bit when the RUN bit is 0 (count is stopped).

AADJM Bit (Automatic correction mode select bit)

This bit is enabled when the AADJE bit in the TRECR register is 1 (automatic correction function enabled (correction by software disabled)).
When the AADJM bit is set to 0, correction is performed every minute and the resolution is ±0.5 ppm. When this bit is set to 1, correction is performed every 10 seconds and the resolution is ±3 ppm.
Change this bit when the BSY bit in the TRESEC register is 0 (data not being updated).

17.2.13 Timer RE Count Source Select Register (TRECSR) in Compare Match Timer Mode

Address 00138h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	AADJM	OS2	OS1	OS0	CS3	CS2	CS1	CS0
After Reset	X	0	0	0	1	0	0	0
After reset by RTCRST bit in TRECR register	0	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	CS0	Count source select bits	Set the following values in compare match timer mode (CS3 bit = 0): b3 b2 b1 b0 0 0 0 0: f8 0 0 0 1: f32 0 0 1 0: f128 0 0 1 1: f256 0 1 0 0: f512 0 1 0 1: f2048 0 1 1 0: f4096 0 1 1 1: f8192 Other than the above: Do not set.	R/W
b1	CS1			R/W
b2	CS2			R/W
b3	CS3			R/W
b4	OS0	Timer RE output select bits	b6 b5 b4 0 0 0: f4 0 0 1: fXCIN 0 1 0: f8 0 1 1: Do not set. 1 0 0: f16 1 0 1: Do not set. 1 1 0: f32 1 1 1: Output toggled at every compare match	R/W
b5	OS1			R/W
b6	OS2			R/W
b7	AADJM	Set to 0.		R/W

Bits CS0 to CS3 (Count source select bits)

Change these bits when the RUN bit in the TRECR register is 0 (count is stopped).

Bits OS0 to OS2 (Timer RE output select bits)

Change these bit when the RUN bit is 0 (count is stopped).
When 111b is written to bits OS2 to OS0, the internal output level is set to low.

17.2.14 Timer RE Clock Error Correction Register (TREADJ)

Address 00139h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PLUS	MINUS	ADJ5	ADJ4	ADJ3	ADJ2	ADJ1	ADJ0
After Reset	X	X	X	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADJ0	Correction value setting bits	Setting range: 00h to 3Fh (00 to 63)	R/W
b1	ADJ1			R/W
b2	ADJ2			R/W
b3	ADJ3			R/W
b4	ADJ4			R/W
b5	ADJ5			R/W
b6	MINUS	Correction counter bits	b7 b6 0 0: Not corrected 0 1: Subtraction correction 1 0: Addition correction 1 1: Do not set.	R/W
b7	PLUS			R/W

The TREADJ register is used in real-time clock mode.
Change the TREADJ register when the BSY bit in the TRESEC register is 0 (data not being updated).

Bits MINUS to PLUS (Correction counter bits)

The one-second counter is changed depending on the values of bits ADJ0 to ADJ5.
When the PLUS bit is set to 0 and the MINUS bit is set to 1, the internal counter is corrected to the minus side. The clock can be set backward when it gains time.
When the PLUS bit is set to 1 and the MINUS bit is set to 0, the internal counter is corrected to the plus side. The clock can be set forward when it loses time.
The interval for correction differs depending on the AADJE bit in the TRECR register.
When the AADJE bit is 0 (automatic correction function disabled (correction by software enabled)), correction is performed when writing to the TREADJ register. When the AADJE bit is 1 (automatic correction function enabled (correction by software disabled)), correction is performed for the interval set by the AADJM bit in the TRECSR register.
For details on the setting method of the TREADJ register, see **17.3.4 Clock Error Correction Function**.

17.2.15 Timer RE Interrupt Flag Register (TREIFR) in Real-Time Clock Mode

Address 0013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TADJSF	—	—	RSTADJ	ADJ30S	ALIE	RTCF	ALIF
After Reset	0	0	0	0	0	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ALIF	Alarm interrupt flag	0: No interrupt requested 1: Interrupt requested	R/W
b1	RTCF	Real-time clock periodic interrupt flag	0: No interrupt requested 1: Interrupt requested	R/W
b2	ALIE	Alarm interrupt enable bit	0: Alarm interrupt disabled 1: Alarm interrupt enabled	R/W
b3	ADJ30S	30-second adjustment bit	When 1 is written to this bit, the value of the TRESEC register changes as follows. When TRESEC register value ≤ 29: TRESEC ← 00h When TRESEC register value ≥ 30: TRESEC ← 00h, TREMIN ← TREMIN + 1 The read value is 0.	W
b4	RSTADJ	Second counter reset adjustment bit	When 1 is written to this bit, the value of the TRESEC register is set to 00h and the internal counter is initialized. The read value is 0.	W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	TADJSF	Correction status flag	0: No correction 1: Being corrected	R

ALIF Bit (Alarm interrupt flag)

[Condition for setting to 0]

- When 0 is written to this bit after reading it. If the result of reading this bit is 1, writing 0 to this bit will set it to 0.

[Condition for setting to 1]

- The contents of the timer RE alarm register (1) and the timer RE data register (2) match (see **17.3.5 Alarm Function**).
  If the result of reading this bit is 0, writing 0 to this bit will not change its value. If this bit changes from 0 to 1 after the read, the bit will remain 1 even if 0 is written. Writing 1 has no effect.
  To confirm the match, set an enable bit in the timer RE alarm registers (1) to 1.

Notes:

1. Timer RE alarm registers: TREAMN, TREAHR, and TREAWK
2. Timer RE data registers: TRESEC, TREMIN, TREHR, TREWK, TREDY, TREMON, and TREYR

RTCF Bit (Real-time clock periodic interrupt flag)

[Condition for setting to 0]

- When 0 is written to this bit after reading it. If the result of reading this bit is 1, writing 0 to this bit will set it to 0.

[Condition for setting to 1]

- The interrupt source enabled by the TREIER register is generated.
  If the result of reading this bit is 0, writing 0 to this bit will not change its value. If this bit changes from 0 to 1 after the read, the bit will remain 1 even if 0 is written. Writing 1 has no effect.

TADJSF Bit (Correction status flag)

While the TADJSF bit is 1 (being corrected), do not change the following bits or register:
- The AADJE bit in the TRECR register
- The AADJM bit in the TRECSR register
- The TREADJ register

[Conditions for setting to 0]
- Correction ends.
  (1) For addition correction, when the correction value set by bits ADJ0 to ADJ5 in the TREADJ register is transferred to the internal counter.
  (2) For subtraction correction, when the correction value set by bits ADJ0 to ADJ5 in the TREADJ register and the internal counter value are compared and match.
- When 00b (not corrected) is written to bits PLUS to MINUS in the TREADJ register.

[Conditions for setting to 1]
- Correction by software
  (1) When 01b (subtraction correction) is written to bits PLUS to MINUS (the TADJSF bit is set to 1 in synchronization with the count source).
  (2) When 10b (addition correction) is written to bits PLUS to MINUS (the TADJSF bit is set to 1 in synchronization with the count source).
- Automatic correction
  When the BSY bit in the TRESEC register is set to 0 (data not being updated) during the seconds which meet the conditions for subtraction correction.

17.2.16 Timer RE Interrupt Flag Register (TREIFR) in Compare Match Timer Mode

Address 0013Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TADJSF	—	—	RSTADJ	ADJ30S	ALIE	OVIF	CMIF
After Reset	0	0	0	0	0	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMIF	Compare match interrupt flag	0: No interrupt requested 1: Interrupt requested	R/W
b1	OVIF	Overflow interrupt flag	0: No interrupt requested 1: Interrupt requested	R/W
b2	ALIE	Set to 0.		R/W
b3	ADJ30S			W
b4	RSTADJ			W
b5	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b6	—			
b7	TADJSF	Disabled in compare match timer mode.		R

CMIF Bit (Compare match interrupt flag)

[Condition for setting to 0]

• When 0 is written to this bit after reading it. If the result of reading this bit is 1, writing 0 to this bit will set it to 0.

[Condition for setting to 1]

• The contents of registers TRECNT and TREMIN match.

If the result of reading this bit is 0, writing 0 to this bit will not change its value. If this bit changes from 0 to 1 after the read, the bit will remain 1 even if 0 is written. Writing 1 has no effect.

OVIF Bit (Overflow interrupt flag)

[Condition for setting to 0]

• When 0 is written to this bit after reading it. If the result of reading this bit is 1, writing 0 to this bit will set it to 0.

[Condition for setting to 1]

• The 8-bit counter overflows.

If the result of reading this bit is 0, writing 0 to this bit will not change its value. If this bit changes from 0 to 1 after the read, the bit will remain 1 even if 0 is written. Writing 1 has no effect.

17.2.17 Timer RE Interrupt Enable Register (TREIER) in Real-Time Clock Mode

Address 0013Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	YRIE	MOIE	DYIE	HRIE	MNIE	SEIE	SEIE05	SEIE025
After Reset	X	X	X	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SEIE025	Periodic interrupt triggered every 0.25 seconds enable bit	0: Periodic interrupt triggered every 0.25 seconds disabled 1: Periodic interrupt triggered every 0.25 seconds enabled	R/W
b1	SEIE05	Periodic interrupt triggered every 0.5 seconds enable bit	0: Periodic interrupt triggered every 0.5 seconds disabled 1: Periodic interrupt triggered every 0.5 seconds enabled	R/W
b2	SEIE	Periodic interrupt triggered every second enable bit	0: Periodic interrupt triggered every second disabled 1: Periodic interrupt triggered every second enabled	R/W
b3	MNIE	Periodic interrupt triggered every minute enable bit	0: Periodic interrupt triggered every minute disabled 1: Periodic interrupt triggered every minute enabled	R/W
b4	HRIE	Periodic interrupt triggered every hour enable bit	0: Periodic interrupt triggered every hour disabled 1: Periodic interrupt triggered every hour enabled	R/W
b5	DYIE	Periodic interrupt triggered every day enable bit	0: Periodic interrupt triggered every day disabled 1: Periodic interrupt triggered every day enabled	R/W
b6	MOIE	Periodic interrupt triggered every month enable bit	0: Periodic interrupt triggered every month disabled 1: Periodic interrupt triggered every month enabled	R/W
b7	YRIE	Periodic interrupt triggered every year enable bit	0: Periodic interrupt triggered every year disabled 1: Periodic interrupt triggered every year enabled	R/W

Write to the TREIER register when the RUN bit in the TRECR register is 0 (count is stopped).
An interrupt request can be generated every 0.25 seconds, 0.5 seconds, one second, minute, hour, day, month, or year. To generate an interrupt request, set one of the following bits to 1 (interrupt enabled): SEIE025, SEIE05, SEIE, MNIE, HRIE, DYIE, MOIE, and YRIE (be sure to set only one bit to 1).

17.2.18 Timer RE Interrupt Enable Register (TREIER) in Compare Match Timer Mode

Address 0013Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	YRIE	MOIE	DYIE	HRIE	MNIE	SEIE	OVIE	CMIE
After Reset	X	X	X	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CMIE	Compare match interrupt enable bit	0: Compare match interrupt disabled 1: Compare match interrupt enabled	R/W
b1	OVIE	Overflow interrupt enable bit	0: Overflow interrupt disabled 1: Overflow interrupt enabled	R/W
b2	SEIE	Set to 0.		R/W
b3	MNIE			R/W
b4	HRIE			R/W
b5	DYIE			R/W
b6	MOIE			R/W
b7	YRIE			R/W

Write to the TREIER register when the RUN bit in the TRECR register is 0 (count is stopped).

17.2.19 Timer RE Alarm Minute Register (TREAMN)

Address 0013Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ENBMN	AMN6	AMN5	AMN4	AMN3	AMN2	AMN1	AMN0
After Reset	X	X	X	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	AMN0	First digit of minute alarm data bits	Store the alarm data.	0 to 9 (BCD code)	R/W
b1	AMN1				R/W
b2	AMN2				R/W
b3	AMN3				R/W
b4	AMN4	Second digit of minute alarm data bits	Store the alarm data.	0 to 5 (BCD code)	R/W
b5	AMN5				R/W
b6	AMN6				R/W
b7	ENBMN	Minute alarm enable bit	0: Minute alarm disabled (not compared with the TREMIN register) 1: Minute alarm enabled (compared with the TREMIN register)		R/W

The TREAMN register is used in real-time clock mode.
Write to this register when the BSY bit in the TRESEC register is 0 (data not being updated).
The TREAMN register is compared with the TREMIN register when the ENBMN bit is 1 (minute alarm enabled). If the values of both the registers match, the ALIF bit in the TREIFR register is set to 1 (interrupt requested). When the ALIE bit in the TREIFR register is 1 (alarm interrupt enabled), an interrupt request is generated.

Bits AMN0 to AMN3 (First digit of minute alarm data bits)
Bits AMN4 to AMN6 (Second digit of minute alarm data bits)

Set values from 00 to 59 by the BCD code.

17.2.20 Timer RE Alarm Hour Register (TREAHR)

Address 0013Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ENBHR	APM	AHR5	AHR4	AHR3	AHR2	AHR1	AHR0
After Reset	X	X	X	X	X	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	AHR0	First digit of hour alarm data bits	Store the alarm data.	0 to 9 (BCD code)	R/W
b1	AHR1				R/W
b2	AHR2				R/W
b3	AHR3				R/W
b4	AHR4	Second digit of hour alarm data bits	Store the alarm data.	0 to 2 (BCD code)	R/W
b5	AHR5				R/W
b6	APM	a.m./p.m. alarm data bit	0: a.m. 1: p.m.		R/W
b7	ENBHR	Hour alarm enable bit	0: Hour alarm disabled (not compared with the TREHR register) 1: Hour alarm enabled (compared with the TREHR register)		R/W

The TREAHR register is used in real-time clock mode.
Write to this register when the BSY bit in the TRESEC register is 0 (data not being updated).
The TREAHR register is compared with the TREHR register when the ENBHR bit is 1 (hour alarm enabled). If the values of both the registers match, the ALIF bit in the TREIFR register is set to 1 (interrupt requested). When the ALIE bit in the TREIFR register is 1 (alarm interrupt enabled), an interrupt request is generated.

Bits AHR0 to AHR3 (First digit of hour alarm data bits)
Bits AHR4 to AHR5 (Second digit of hour alarm data bits)

Set values from 00 to 11 by the BCD code when the HR24 bit in the TRECR register is 0 (12-hour mode). Set values from 00 to 23 by the BCD code when the HR24 bit is 1 (24-hour mode).

APM Bit (a.m./p.m. alarm data bit)

Set the APM bit to 0 (a.m.) when the HR24 bit is 1 (24-hour mode).

17.2.21 Timer RE Alarm Day-of-the-Week Register (TREAWK)

Address 0013Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ENBWK	—	—	—	—	AWK2	AWK1	AWK0
After Reset	X	0	0	0	0	X	X	X
After reset by RTCRST bit in TRECR register	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	AWK0	Day-of-the-week alarm data bits	b2 b1 b0 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Do not set.	R/W
b1	AWK1			R/W
b2	AWK2			R/W
b3	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b4	—			
b5	—			
b6	—			
b7	ENBWK	Day-of-the-week alarm enable bit	0: Day-of-the-week alarm disabled (not compared with the TREWK register) 1: Day-of-the-week alarm enabled (compared with the TREWK register)	R/W

The TREAWK register is used in real-time clock mode.
Write to this register when the BSY bit in the TRESEC register is 0 (data not being updated).
The TREAWK register is compared with the TREWK register when the ENBWK bit is 1 (day-of-the-week alarm enabled). If the values of both the registers match, the ALIF bit in the TREIFR register is set to 1 (interrupt requested). When the ALIE bit in the TREIFR register is 1 (alarm interrupt enabled), an interrupt request is generated.

Bits AWK0 to AWK2 (Day-of-the-week alarm data bits)

Set 000b (Sunday) to 110b (Saturday).

17.2.22 Timer RE Protect Register (TREPRC) in Real-Time Clock Mode

Address 0013Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PROTECT	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0
After reset by RTCRST bit in TRECR register	X	X	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—	Reserved	Set to 0.	R/W
b7	PROTECT	Protect bit	Writing to the time data registers 0: Write disabled 1: Write enabled	R/W

PROTECT Bit (Protect bit)

The following registers and bit can be changed when this bit is set to 1 (write enabled):

- Timer RE data registers (TRESEC, TREMIN, TREHR, TREWK, TREDY, TREMON, and TREYR)
- The PM bit in the TRECR register

When 1 is written to the PROTECT bit by a program, this bit remains 1. Use the following procedure to change the registers protected by this bit:

(1) Write 1 to the PROTECT bit.
(2) Write a value to the register protected by this bit.
(3) Write 0 (write disabled) to this bit.

17.2.23 Timer RE Protect Register (TREPRC) in Compare Match Timer Mode

Address 0013Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PROTECT	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0
After reset by RTCRST bit in TRECR register	X	X	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—	Reserved	Set to 0.	R/W
b7	PROTECT	Protect bit	Writing to the TRECNT register 0: Write disabled 1: Write enabled	R/W

PROTECT Bit (Protect bit)

The TRECNT register can be changed when the PROTECT bit is 1 (write enabled).
When 1 is written to the PROTECT bit by a program, this bit remains 1. Use the following procedure to change the TRECNT register:

(1) Write 1 to the PROTECT bit.
(2) Write a value to the TRECNT register.
(3) Write 0 (write disabled) to this bit.

17.3 Operation in Real-Time Clock Mode

17.3.1 Operation Example

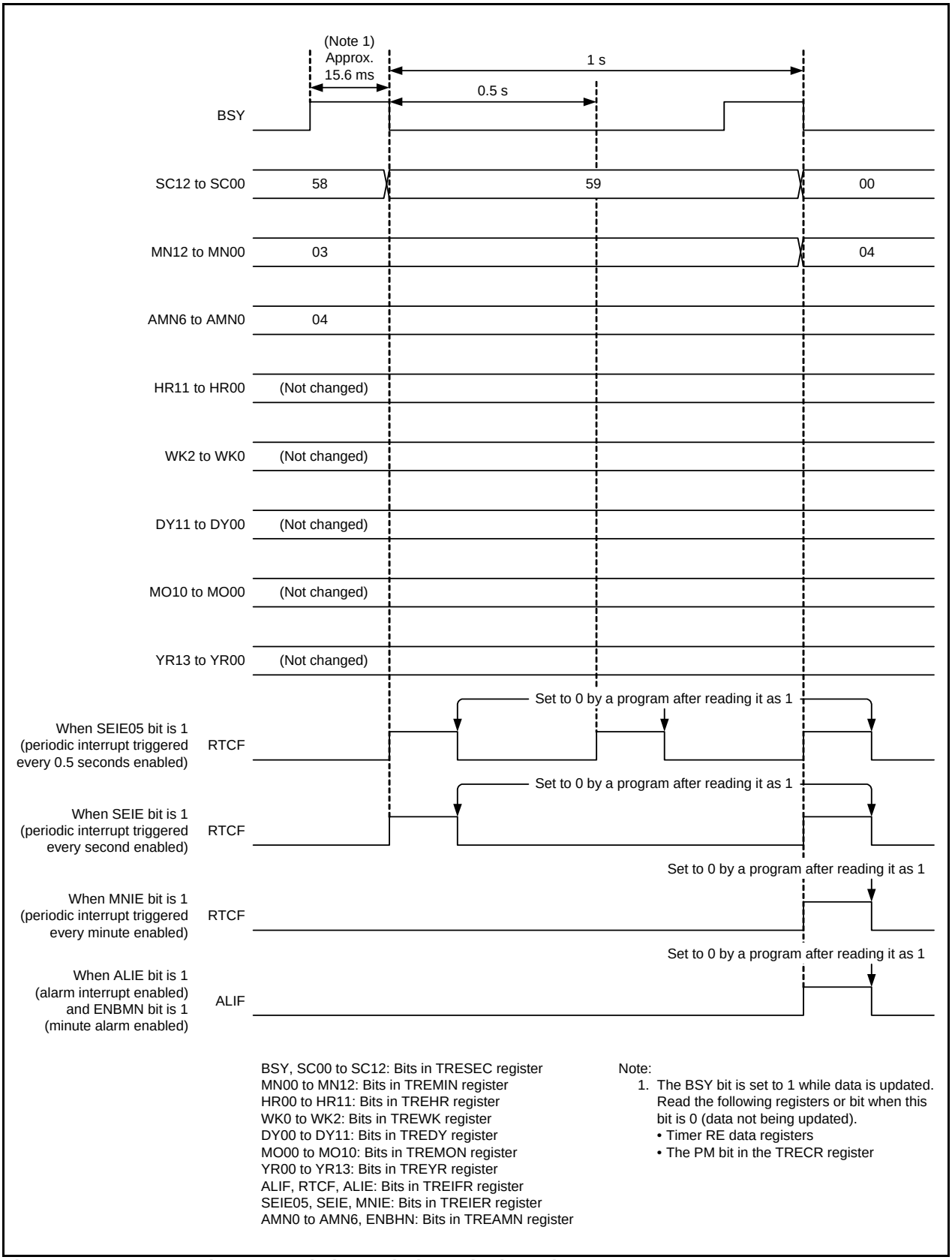


Figure 17.4 Operation Example in Real-Time Clock Mode

17.3.2 Example of Setting Associated Registers

In real-time clock mode, a reset input does not initialize the registers that store data of seconds, minutes, hours, days of the week, days, months, and years. The initial setting for all these registers is required after power on. Figure 17.5 shows the Initial Setting Procedure When Timer RE2 is Used in Real-Time Clock Mode. Also, follow Figure 17.5 when setting these registers again.

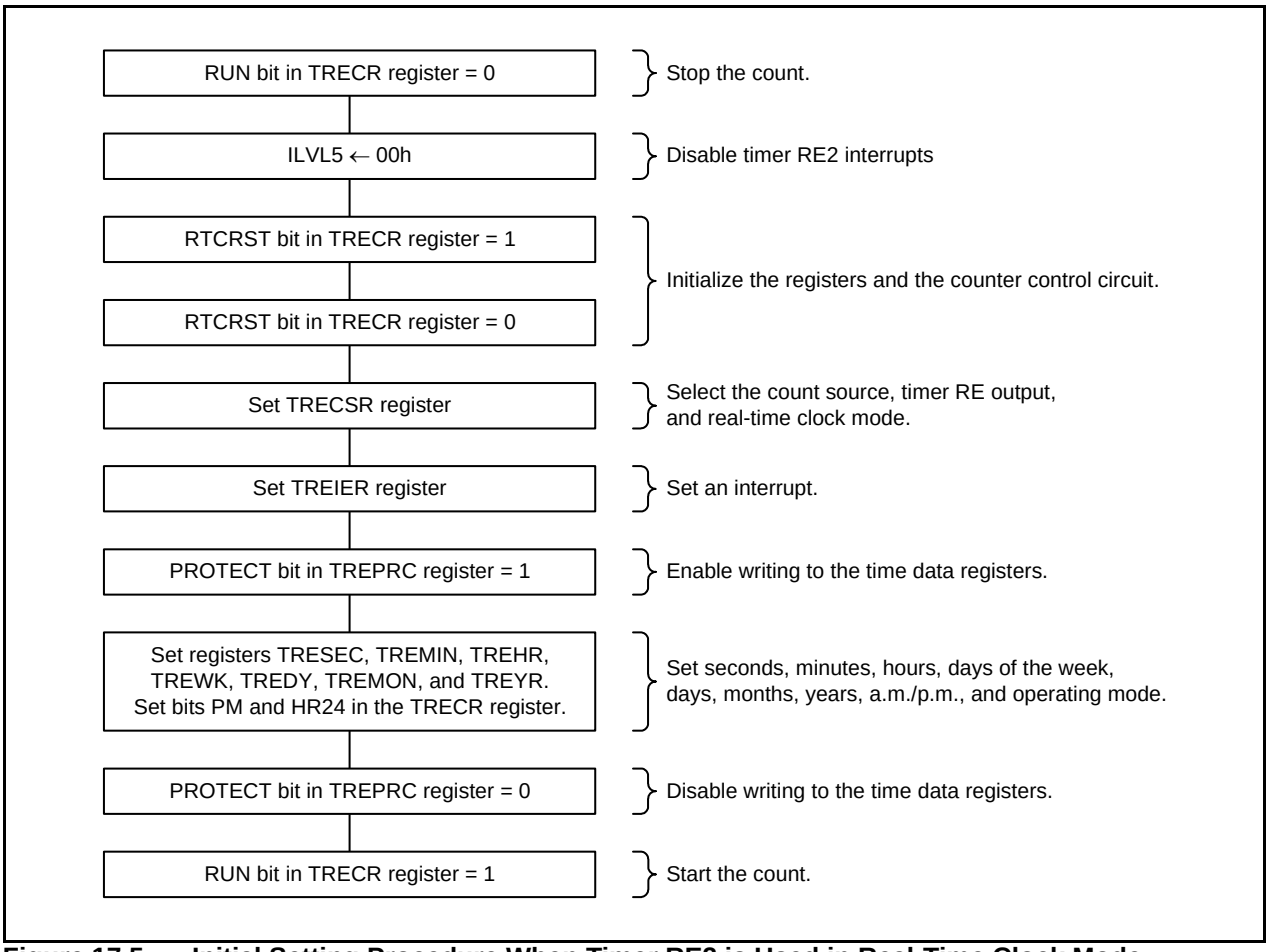


Figure 17.5 Initial Setting Procedure When Timer RE2 is Used in Real-Time Clock Mode

17.3.3 Time Changing and Reading Procedures

17.3.3.1 Time Changing Procedure

Check that the BSY bit in the TRESEC register and change the data registers of seconds, minutes, hours, days of the week, days, months, and years when the BSY bit is 0.

17.3.3.2 Time Reading Procedure

If the data of seconds, minutes, hours, days of the week, days, months, and years is updated while reading the time, a correct time will not be obtained, so the time must be read again. Figure 17.6 shows an Example When Correct Time is not Obtained. In this example, only the TRESEC register is read after the data is updated, resulting an error of approximately 1 minute.

There are the following four methods for reading a correct time:

- Monitoring method by a program 1
  Check the BSY bit in the TRESEC register, and read the data registers of seconds, minutes, hours, days of the week, days, months, and years after the BSY bit changes from 1 to 0. After the BSY bit is set to 1, the registers are updated after approximately 15.625 ms, and this bit is set to 0.
- Monitoring method by a program 2
  Read the data registers of seconds, minutes, hours, days of the week, days, months, and years in the following order:
  (1) Enable a periodic interrupt.
  (2) Monitor the RTCF bit in the TREIFR register.
  (3) Confirm that the RTCF bit is set to 1 (interrupt requested).
  (4) Check that the BSY bit in the TRESEC register is 0 (data not being updated).
  (5) Read the above data registers.
- Using an interrupt
  Read the required contents of the data registers of seconds, minutes, hours, days of the week, days, months, and years, and bits HR24 and PM in the TRECR register when the BSY bit is 0 in the timer RE2 interrupt routine.
- Using the values read only if they are the same value twice
  Read the data registers of seconds, minutes, hours, days of the week, days, months, and years consecutively twice, and use the data if the read data is the same.

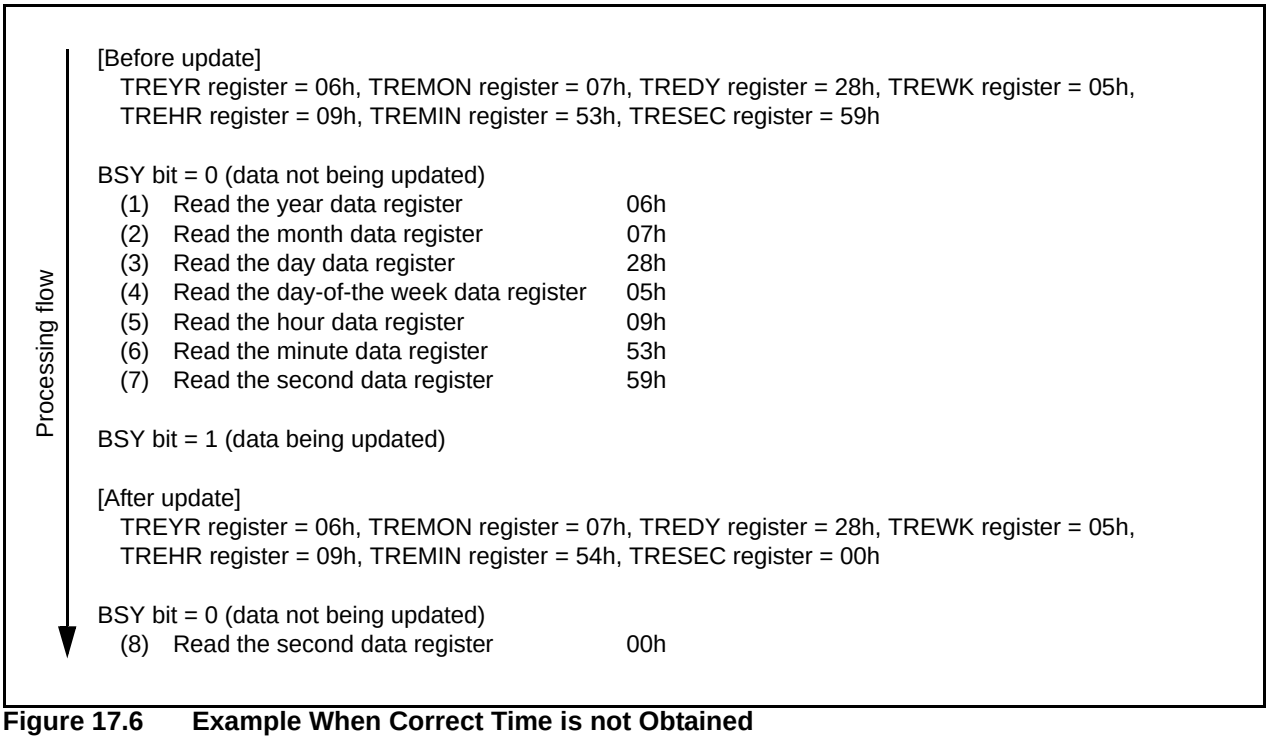


Figure 17.6 Example When Correct Time is not Obtained

17.3.4 Clock Error Correction Function

This function corrects input frequency errors in the XCIN clock. The correction amount is set by bits ADJ0 to ADJ5 in the TREADJ register. The correction direction is set by bits MINUS to PLUS in the TREADJ register. Time errors can be corrected by setting bits PLUS to MINUS to 10b (addition correction) when fXCIN is slower than 32,768 Hz, and by setting these bits to 01b (subtraction correction) when fXCIN is faster than 32,768 Hz.

17.3.4.1 Correction by Software

For correction by software, when 1 is written to the MINUS or PLUS bit in the TREADJ register once, correction is performed only for that one time. Figure 17.7 shows an Operation Example of Addition Correction by Software. For subtraction correction by software, if the TADJSF bit in the TREIFR register is set to 1 (being corrected) immediately before the counter value and the setting value of bits ADJ0 to ADJ5 are compared and match, subtraction correction is performed during the first 1/16 second (see Figure 17.8). If the TADJSF bit is set to 1 immediately after the counter value and the setting value of bits ADJ0 to ADJ5 are compared and match, subtraction correction is performed during the second 1/16 second (see Figure 17.9).

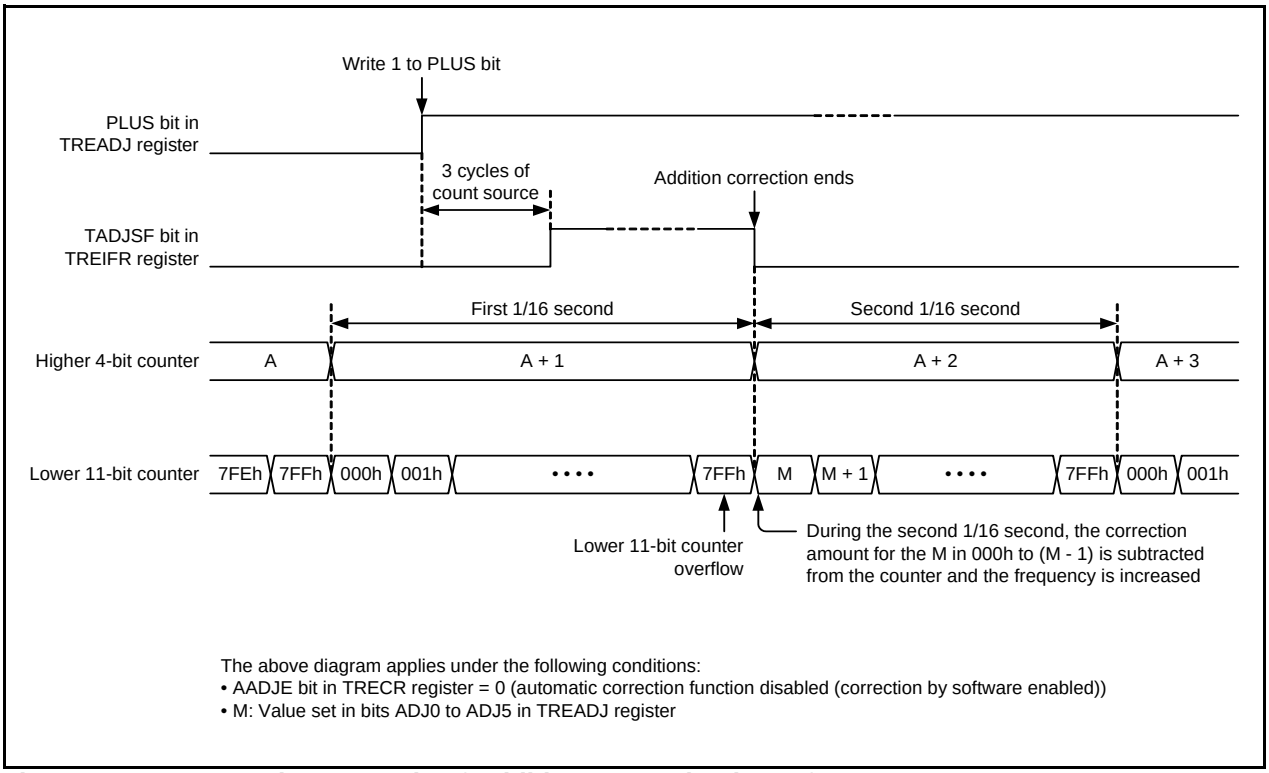


Figure 17.7 Operation Example of Addition Correction by Software

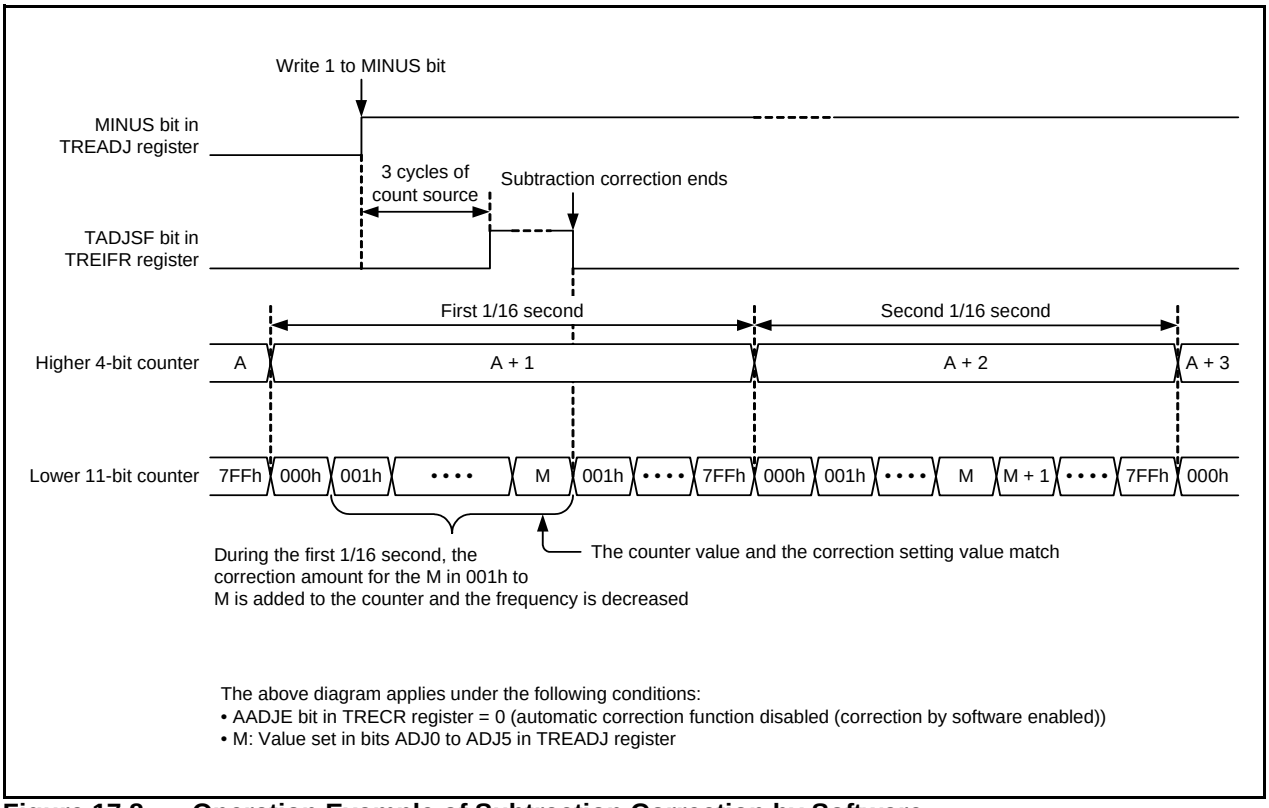


Figure 17.8 Operation Example of Subtraction Correction by Software (Correction during First 1/16 Second)

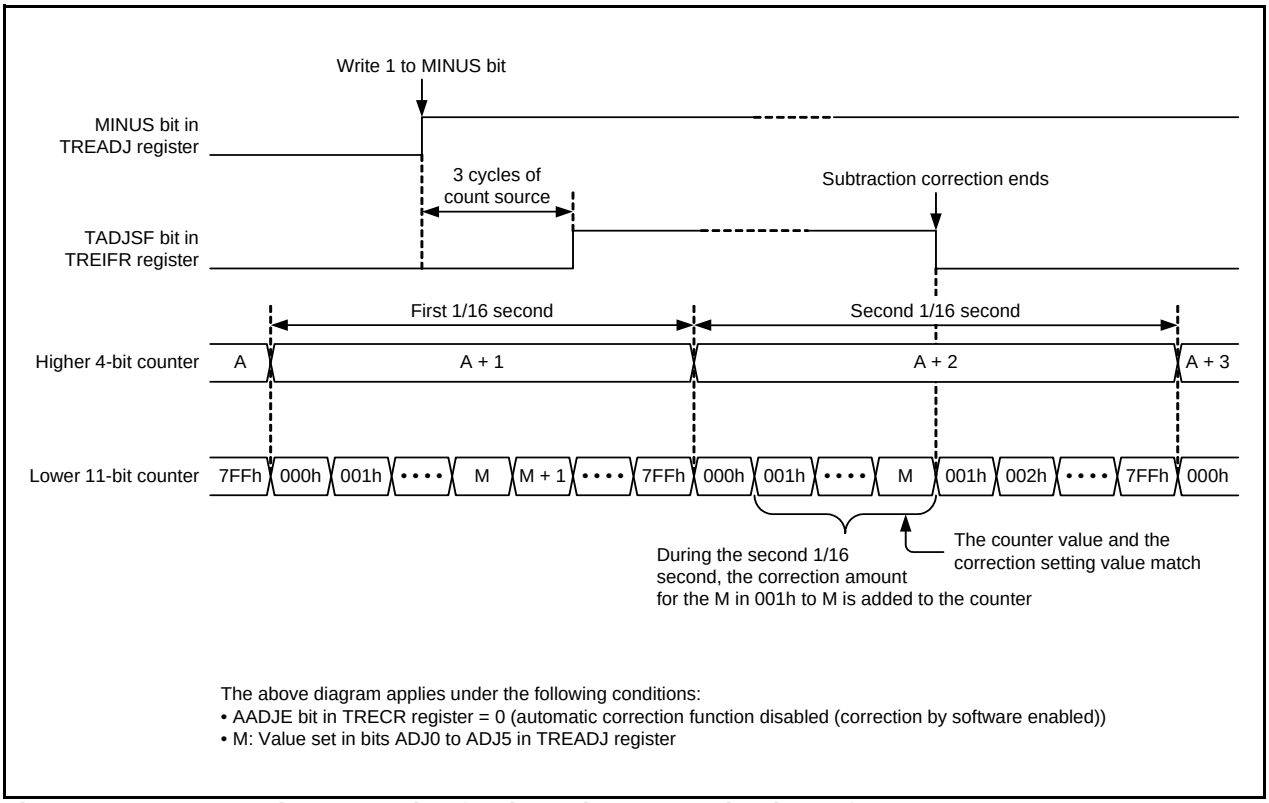


Figure 17.9 Operation Example of Subtraction Correction by Software (Correction during Second 1/16 Second)

17.3.4.2 Automatic Correction Function

For the automatic correction function, when 1 is written to the MINUS or PLUS bit in the TREADJ register, correction is performed periodically. The TREADJ register is added/subtracted to/from the internal counter value every minute or 10 seconds with the AADJM bit in the TRECSR register

Figure 17.10 shows an Operation Example of Addition Correction with Automatic Correction Function. Figure 17.11 shows an Operation Example of Subtraction Correction with Automatic Correction Function.

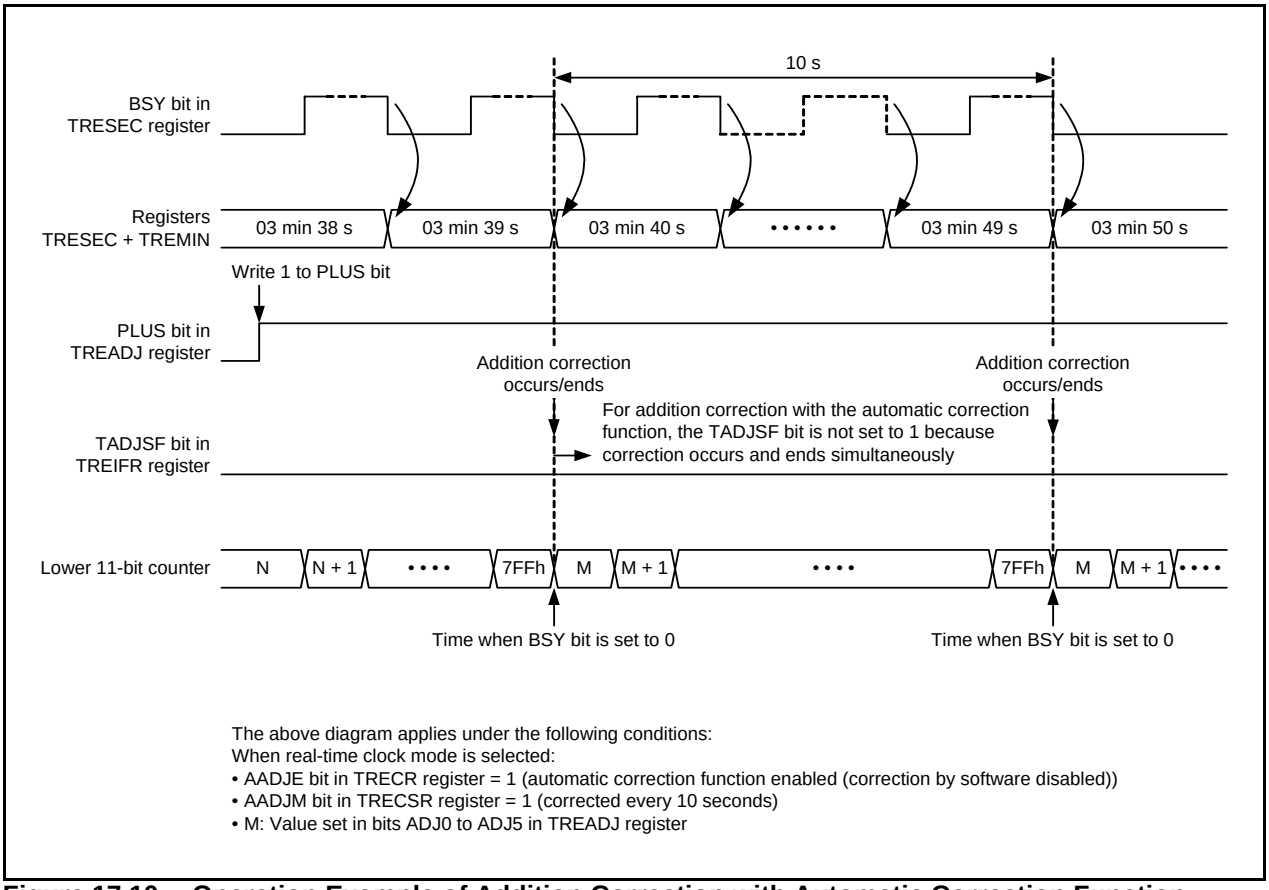


Figure 17.10 Operation Example of Addition Correction with Automatic Correction Function

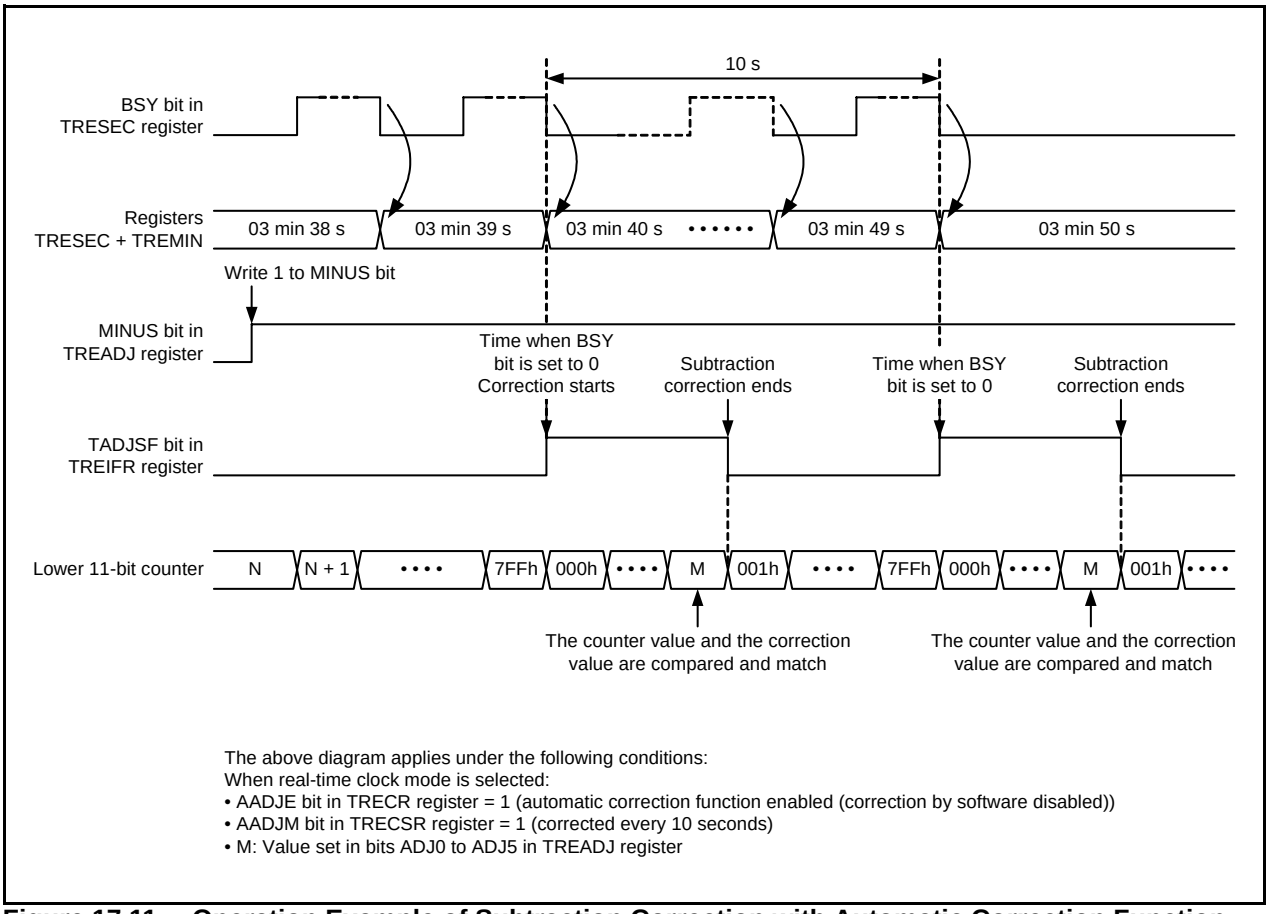
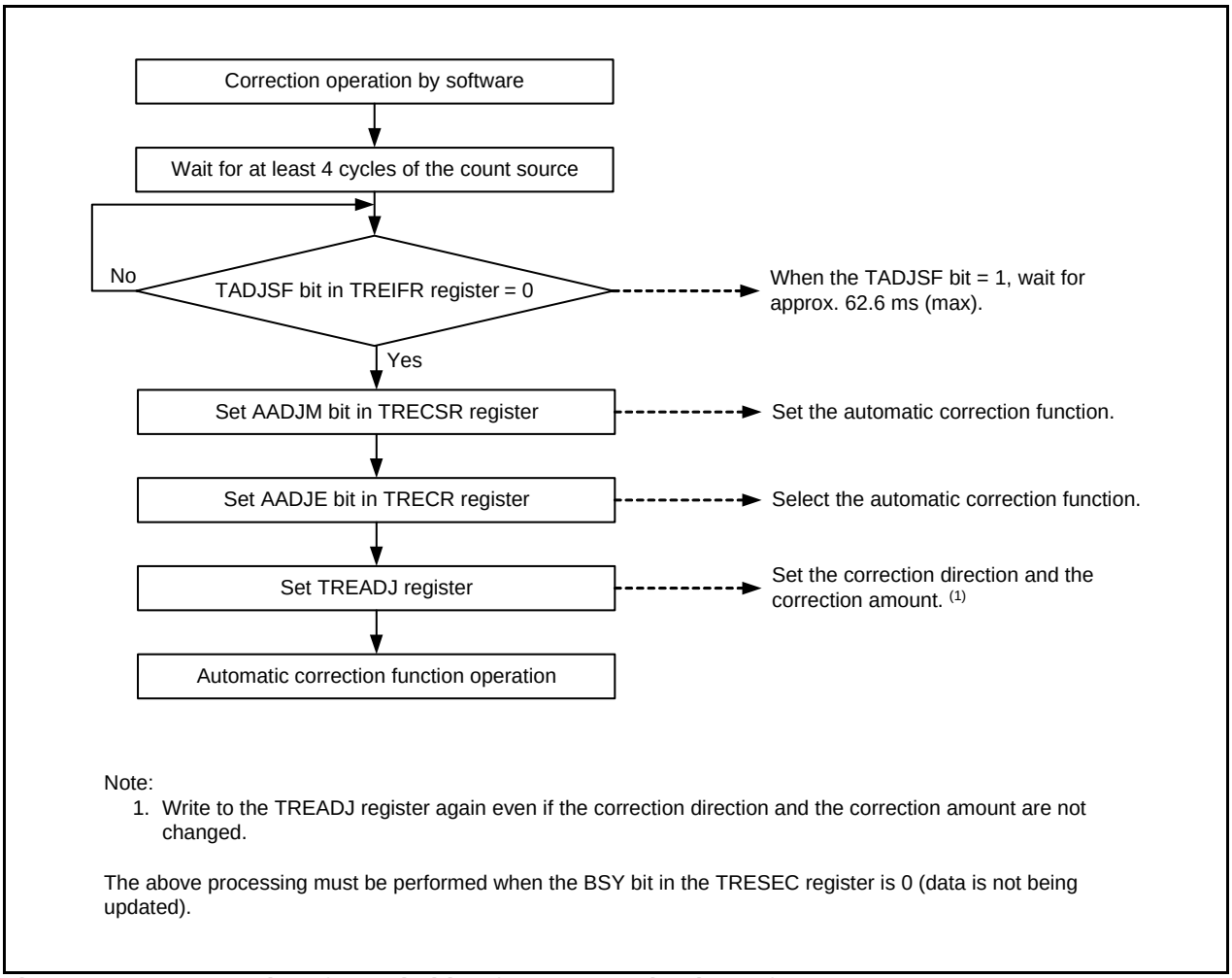


Figure 17.11 Operation Example of Subtraction Correction with Automatic Correction Function

17.3.4.3 Procedure for Switching Automatic Correction Function

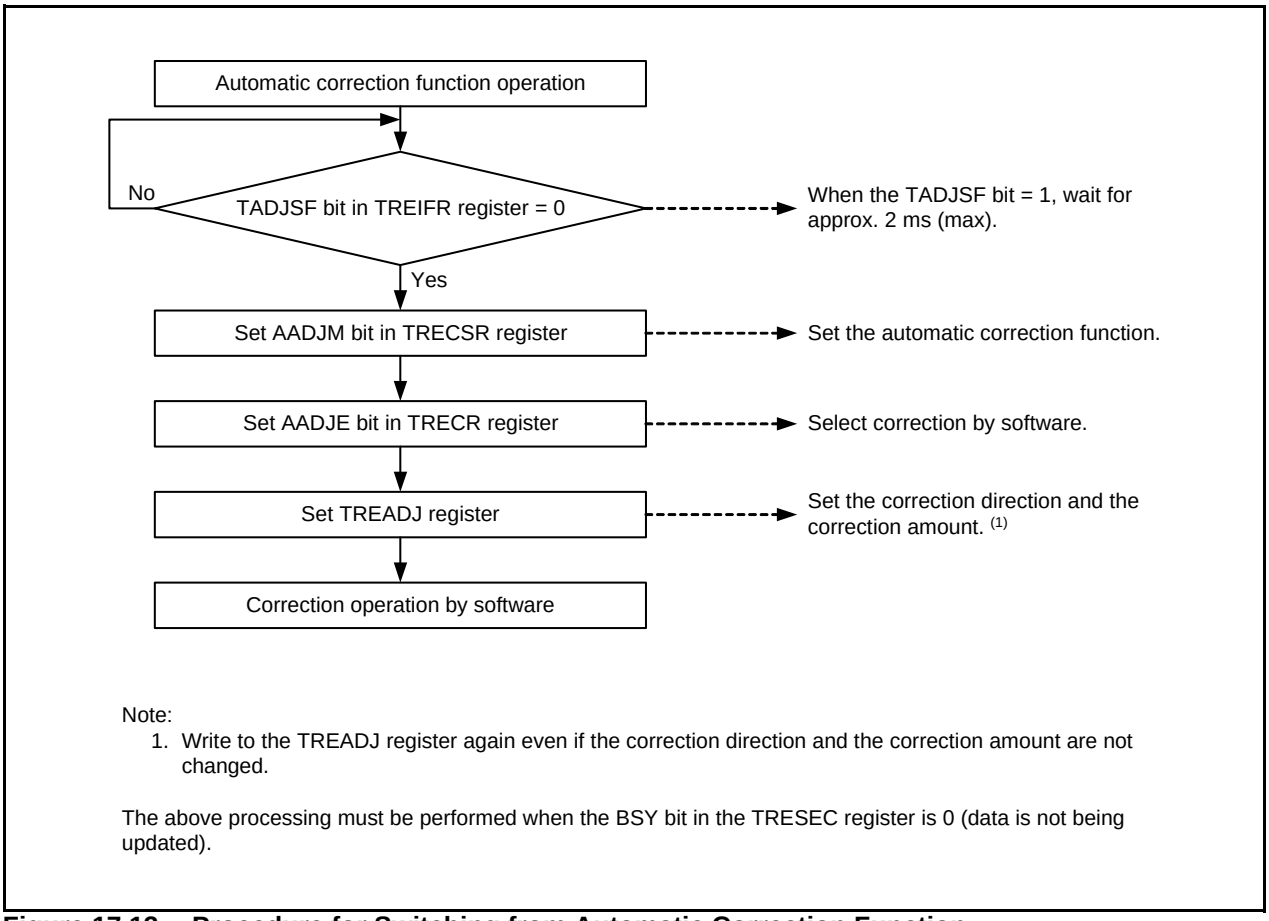
Figure 17.12 shows the Procedure for Switching from Correction by Software. Figure 17.13 shows the Procedure for Switching from Automatic Correction Function. Figure 17.14 shows the Procedure for Stopping Automatic Correction Function.



Note:
1. Write to the TREADJ register again even if the correction direction and the correction amount are not changed.

The above processing must be performed when the BSY bit in the TRESEC register is 0 (data is not being updated).

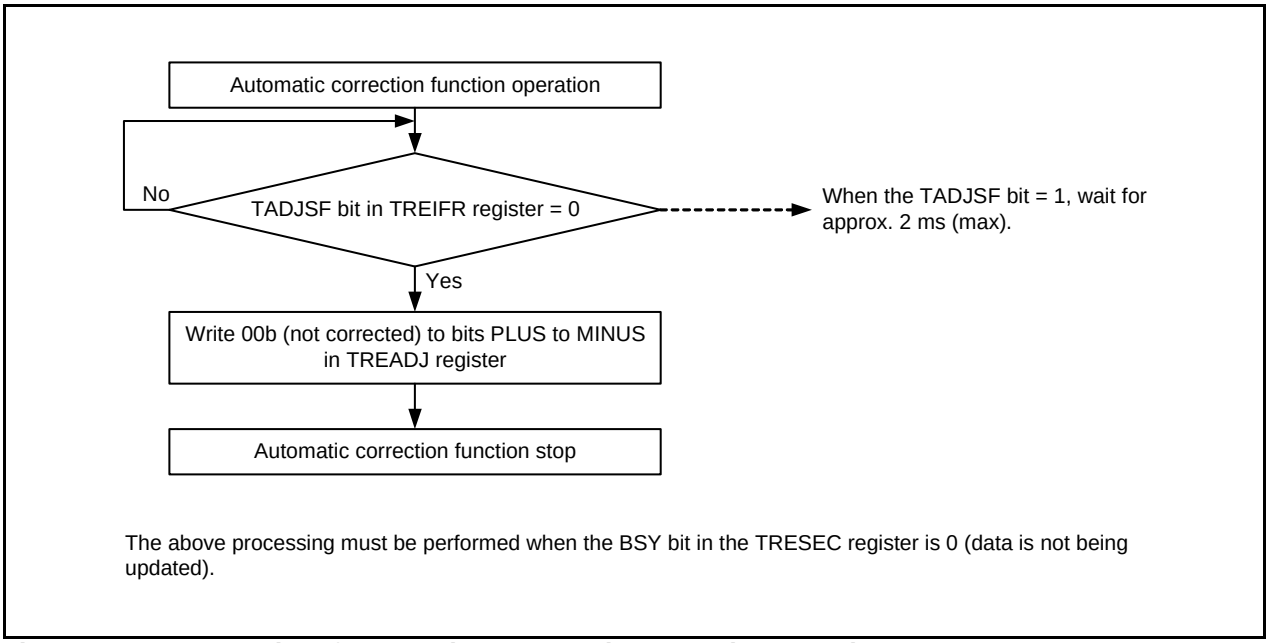
Figure 17.12 Procedure for Switching from Correction by Software



Note:
1. Write to the TREADJ register again even if the correction direction and the correction amount are not changed.

The above processing must be performed when the BSY bit in the TRESEC register is 0 (data is not being updated).

Figure 17.13 Procedure for Switching from Automatic Correction Function



The above processing must be performed when the BSY bit in the TRESEC register is 0 (data is not being updated).

Figure 17.14 Procedure for Stopping Automatic Correction Function

17.3.4.4 Examples of Setting Clock Error Correction Function

The following shows examples of setting correction by the automatic correction function and correction by software.
These examples apply under the assumptions:
• External sub oscillator frequency fsub = 32,769.55 Hz
• External sub oscillator frequency error foffsub = (32,769.55 – 32,768)/32,768 × 10^6 = 47.3 ppm

(1) Example of setting correction by the automatic correction function
The AADJE bit in the TRECR register = 1 (automatic correction function enabled (correction by software disabled)).
• When the AADJM bit in the TRECSR register = 0 (corrected every minute), the correction amount is expressed as follows:
Correction amount = (fsub – 32,768) × 60 = 93 > 63 (maximum setting value of bits ADJ0 to ADJ5)
Thus, automatic correction cannot be performed every minute.
• When the AADJM bit in the TRECSR register = 1 (corrected every 10 seconds), the correction amount is expressed as follows:
Correction amount = (fsub – 32,768) × 10 = 15.5 ≈ 16
Thus, set the TREADJ register to 01010000b (MINUS correction, the correction amount = 16).
Clock errors after correction (unit: ppm)
= ((fsub × 10 – 16)/(32,768 × 10) – 1) × 10^6
= -1.5 ppm (slower than the standard clock by 1.5 ppm)

(2) Example of setting correction by software
The AADJE bit in the TRECR register = 0 (automatic correction function disabled (correction by software enabled)).
• The minimum correction amount when writing to the TREADJ register every second is ±1/32,768 = ±30.5 ppm, and the minimum correction amount when writing to the TREADJ register every minute is ±1/32,768/60 = ±0.5 ppm, so corrections every second and every minute are combined to be used.
• If the correction amount when writing to the TREADJ register every second (writing every second) is A, and the correction amount when writing to the TREADJ register every minute (writing every minute) is B,
A = [fsub – 32,768] = [1.55] = 1 ([ ] indicates a calculation that results in an integer.)
B = A + (((fsub – 32,768) × 60) % 60) = A + (93% 60) = 34
(% indicates a calculation that results in a remainder of the division.)
Thus, correction is performed by writing 01000001b (41h) every second and 01100010b (62h) every minute to the TREADJ register.
Clock errors after correction (unit: ppm)
= (((fsub – A) × 59 + (fsub – B))/(32,768 × 60) – 1) × 10^6
= 0 ppm

17.3.5 Alarm Function

Generation of an alarm can be set by minutes, hours, or days of the week, or any combination of these. Write 1 to an enable bit in the target alarm register and set the lower bits to the alarm time. Write 0 to an enable bit in the other alarm registers.

When the counter (1) and the alarm (2) time match, the ALIF bit in the TREIFR register is set to 1 (interrupt requested). Detection of the alarm can be confirmed by reading the ALIF bit, but usually confirmed by using an interrupt. When 1 (alarm interrupt enabled) has been written to the ALIE bit in the TREIFR register, an alarm interrupt request is generated and the alarm can be detected.

The ALIF bit that has changed to 1 is set to 0 by writing 0 by a program.

Notes:

1. The counter data bits are as follows:
   - Bits MN12 to MN10 and MN03 to MN00 in the TREMIN register
   - Bits HR11 to HR10 and HR03 to HR00 in the TREHR register
   - The PM bit in the TRECR register
   - Bits WK2 to WK0 in the TREWK register
2. The alarm time data bits are as follows:
   - Bits AMN6 to AMN4 and AMN3 to AMN0 in the TREAMN register
   - Bits AHR5 to AHR4 and AHR3 to AHR0 in the TREAHR register
   - The APM bit in the TREAHR register
   - Bits AWK2 to AWK0 in the TREAWK register

The following shows an alarm setting example:

- Set bits AMN6 through AMN4 to 5 and bits AMN3 through AMN0 to 8 in the TREAMN register (58 minutes).
- Set the APM bit to 0 (a.m.) and bits AHR5 through AHR0 to 3 (3 o'clock) in the TREAHR register.
- Set bits AWK2 to AWK0 in the TREAWK register to 001b (Monday).

Table 17.6 lists the Alarm Interrupt Request Generation Conditions. Figure 17.15 shows the Alarm Time Setting Procedure.

Table 17.6 Alarm Interrupt Request Generation Conditions

ENBWK Bit in TREAWK Register	ENBHR Bit in TREAHR Register	ENBMN Bit in TREAMN Register	Alarm Interrupt Request Generation Condition
0	0	0	An alarm interrupt request is not generated.
0	0	1	An alarm interrupt request is generated at 58 minutes and 00 seconds.
0	1	0	An alarm interrupt request is generated at 3:00:00 a.m.
0	1	1	An alarm interrupt request is generated at 3:58:00 a.m.
1	0	0	An alarm interrupt request is generated at 0:00:00 a.m. on Monday.
1	0	1	An alarm interrupt request is generated at 58 minutes and 00 seconds on Monday.
1	1	0	An alarm interrupt request is generated at 3:00:00 a.m. on Monday.
1	1	1	An alarm interrupt request is generated at 3:58:00 a.m. on Monday.

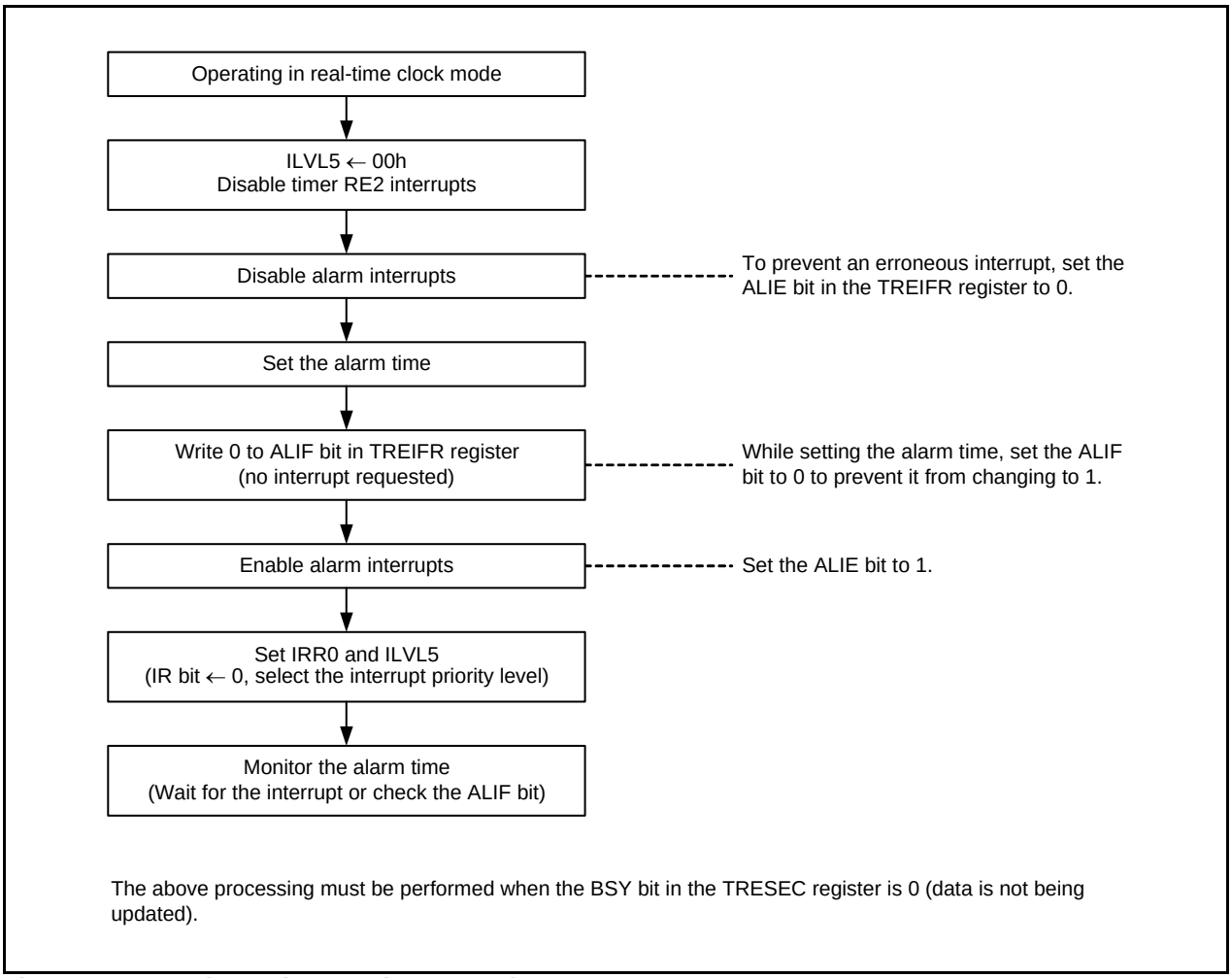


Figure 17.15 Alarm Time Setting Procedure

17.3.6 Second Adjustment Function

Two functions are provided as the second adjustment functions: reset adjustment and 30-second adjustment.

17.3.6.1 Reset Adjustment Function

The reset adjustment function initializes the TRESEC register and the internal counter. When 1 is written to the RSTADJ bit in the TREIFR register while the BSY bit in the TRESEC register is 0 (data not being updated), the TRESEC register is set to 00h in approximately 0.1 ms, and the internal counter is initialized and the count restarts. When 1 is written to the RSTADJ bit while the BSY bit is 1 (data being updated), the TRESEC register is set to 00h when the data is updated, and the internal counter is initialized and the count restarts.
The other timer RE data registers are not affected during reset adjustment. After writing 1 to the RSTADJ bit, allow at least approx. 0.2 ms to elapse before writing to the TRESEC register.

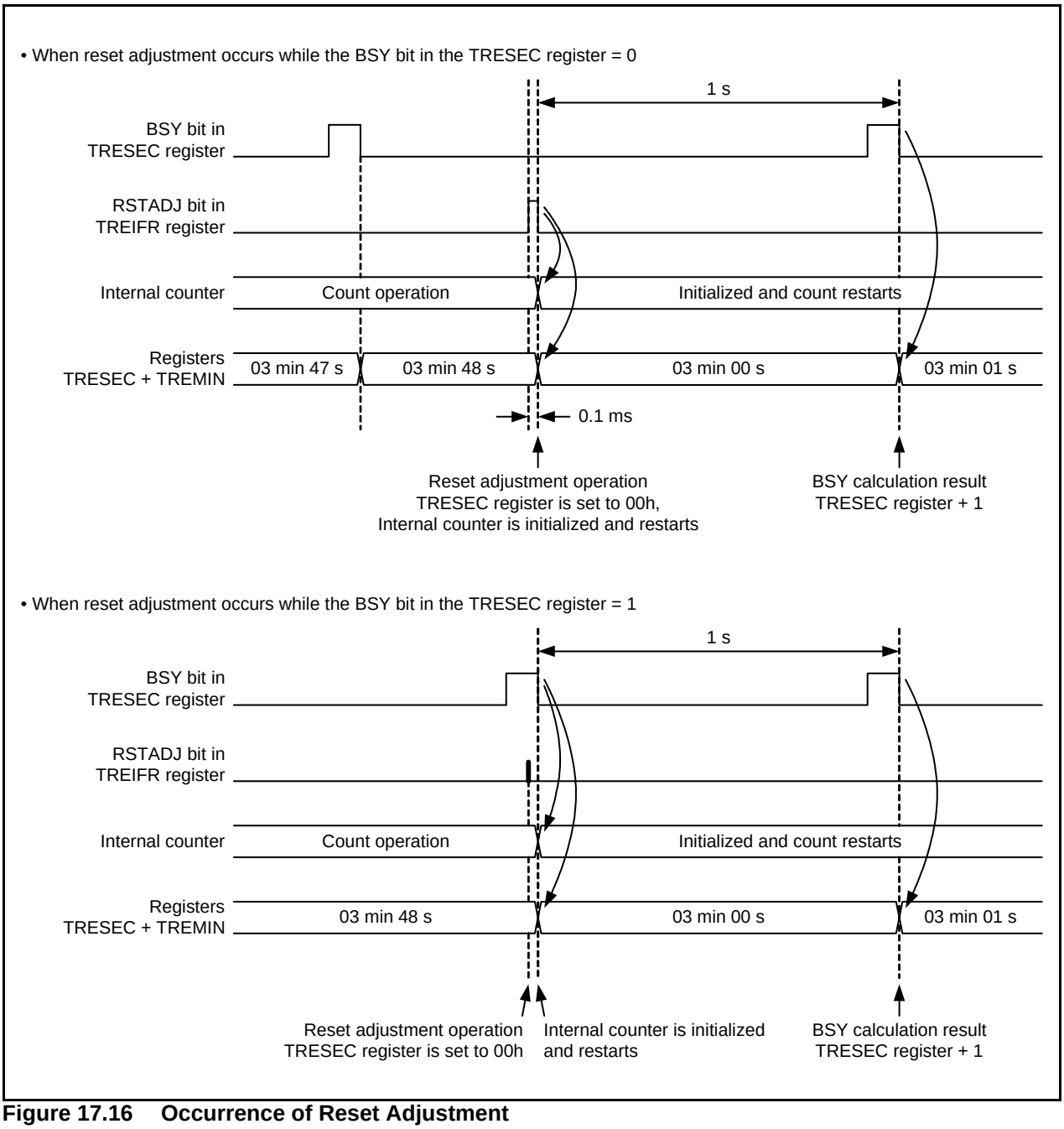


Figure 17.16 Occurrence of Reset Adjustment

17.3.6.2 30-Second Adjustment Function

The 30-second adjustment function rounds 29 seconds or less to 00 and 30 seconds or more to 00. When 1 is written to the ADJ30S bit in the TREIFR register while the BSY bit in the TRESEC register is 0 (data not being updated), the TRESEC register is adjusted by 30 seconds when the data is updated. When 1 is written to the ADJ30S bit while the BSY bit is 1 (data being updated), the TRESEC register is adjusted by 30 seconds when the data is updated the next time. The other timer RE data registers are not affected during 30-second adjustment.

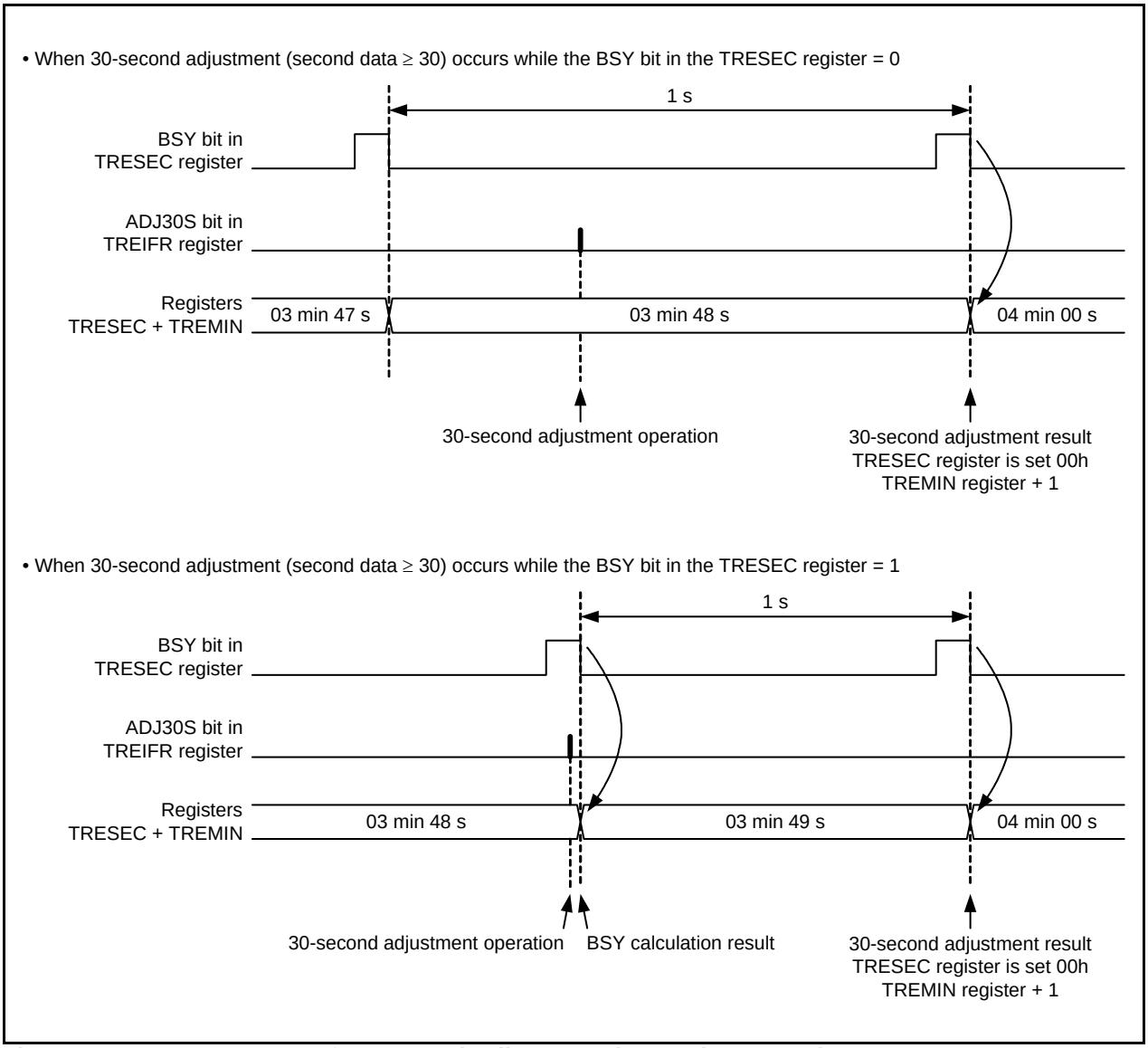


Figure 17.17 Occurrence of 30-Second Adjustment (Second Data ≥ 30)

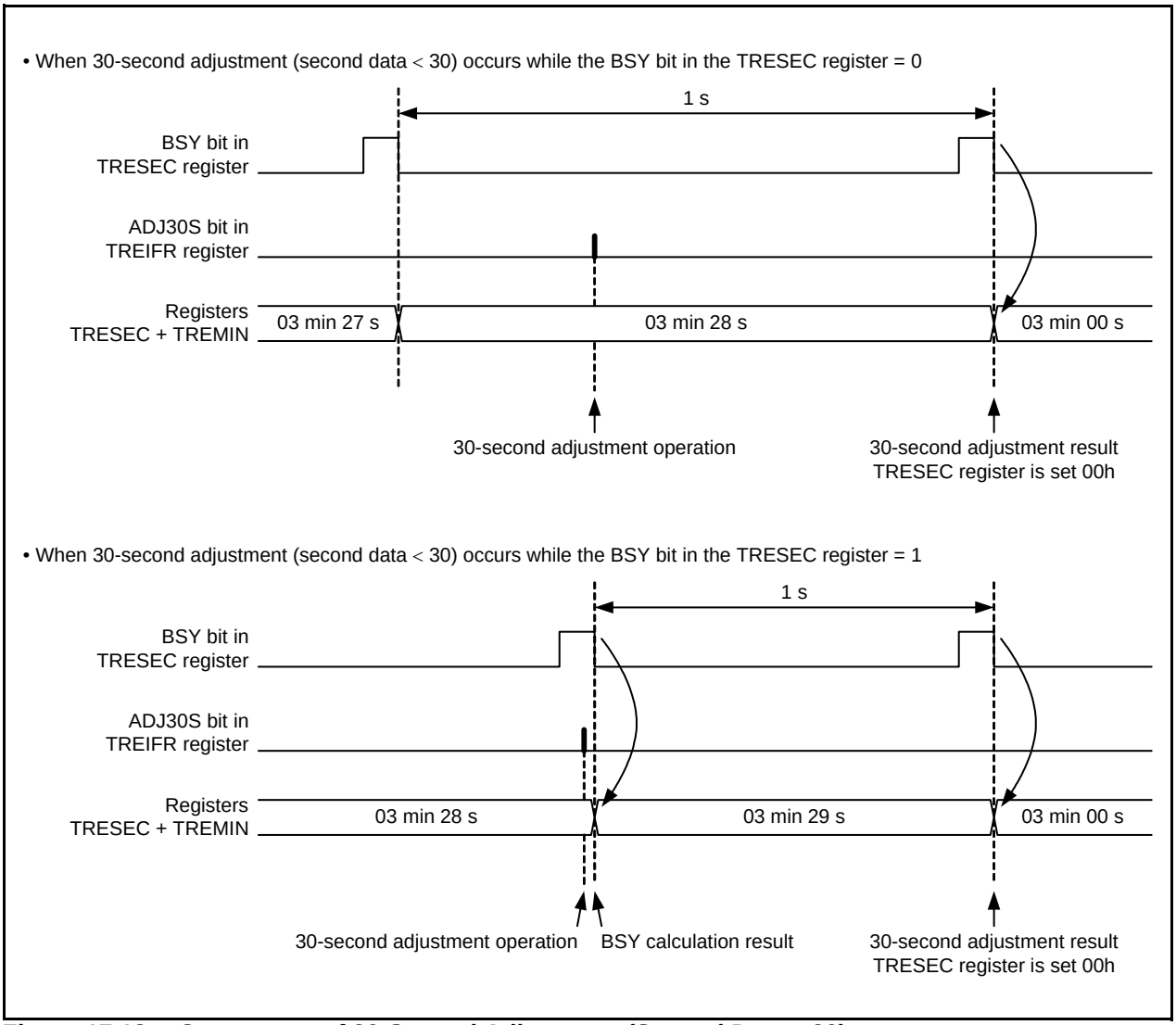


Figure 17.18 Occurrence of 30-Second Adjustment (Second Data < 30)

17.4 Operation in Compare Match Timer Mode

17.4.1 Operation Example

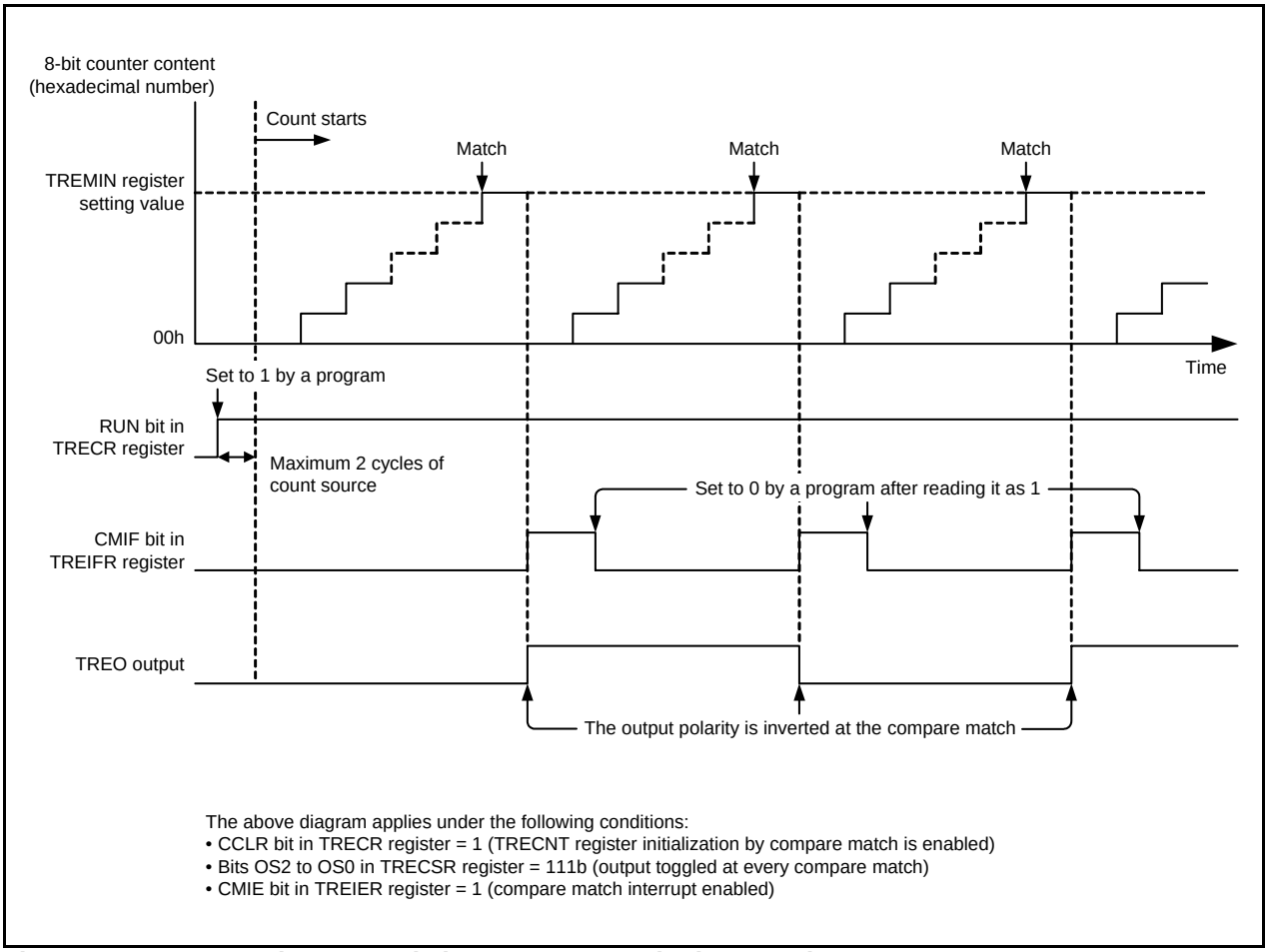


Figure 17.19 Operation Example in Compare Match Timer Mode

17.4.2 Example of Setting Associated Registers

Figure 17.20 shows the Initial Setting Procedure When Timer RE2 is Used in Compare Match Timer Mode. Also, follow Figure 17.20 when setting these registers again.

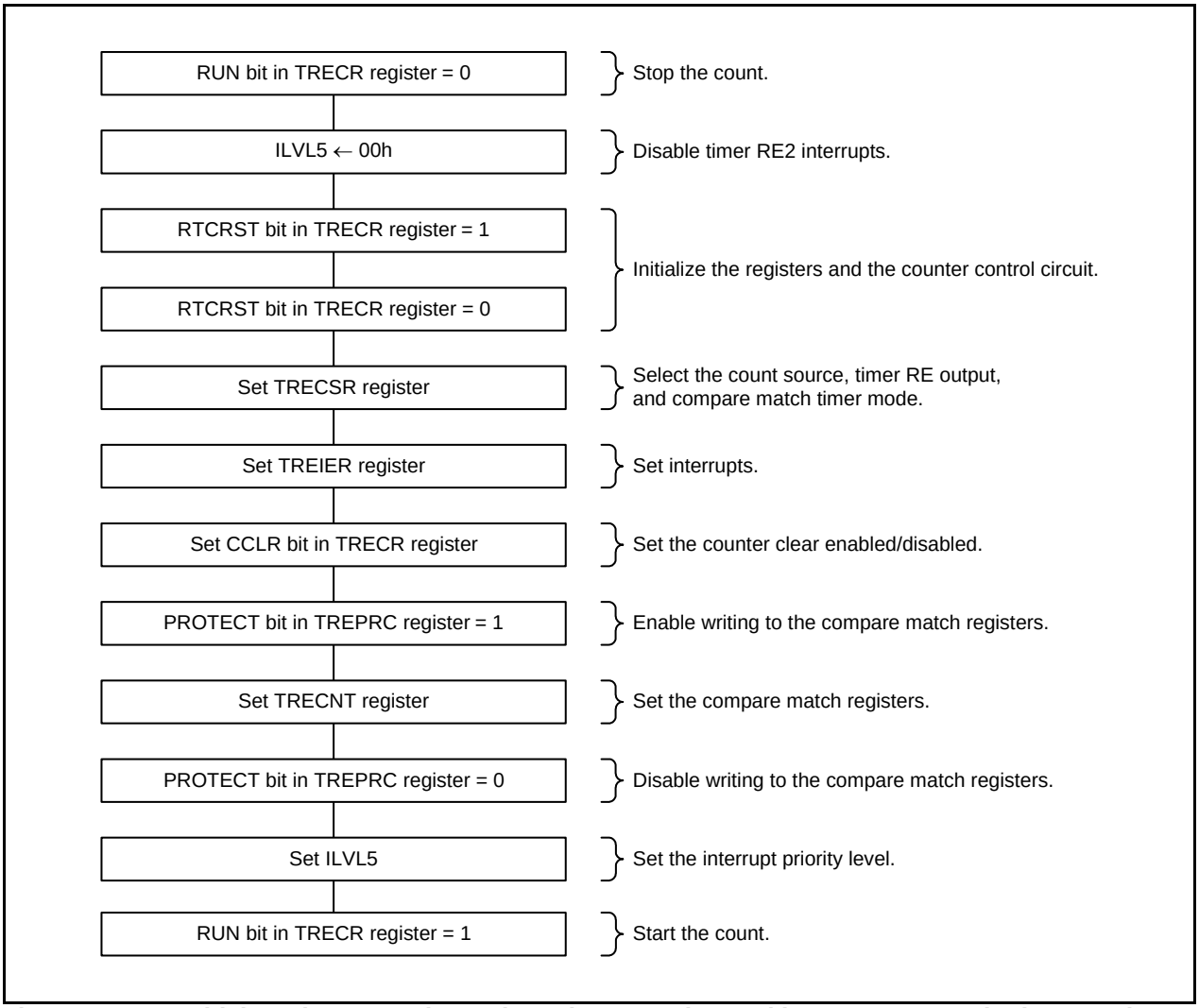


Figure 17.20 Initial Setting Procedure When Timer RE2 is Used in Compare Match Timer Mode

17.5 Interrupt Sources

The interrupt sources for timer RE2 are listed below:
• Periodic interrupts (0.25 seconds, 0.5 seconds, 1 second, minutes, hours, a day, a month, a year)
• Alarm interrupt
• Compare match interrupt
• Overflow interrupt
Table 17.7 lists Timer RE2 Interrupt Sources.
When an interrupt is used, set the registers other than the TRECR register while the RUN bit in the TRECR register is 0 (count is stopped), and set the RUN bit to 1 (count is started).

[Real-time clock mode]
When an enabled periodic interrupt source is generated, the RTCF bit in the TREIFR register is set to 1 (interrupt requested), and an interrupt request is generated.
When the alarm time and the counter match, the ALIF bit in the TREIFR register is set to 1 (interrupt requested). When an alarm interrupt is enabled, an interrupt request is generated.

[Compare match timer mode]
When the compare match timer overflows, the OVIF bit in the TREIFR register is set to 1 (interrupt requested). When the OVIE bit in the TRIER register is 1 (overflow interrupt enabled), an interrupt request is generated.
When the compare match timer is compared and matches, the CMIF bit in the TREIFR register is set to 1 (interrupt requested). When the CMIE bit in the TREIER register is 1 (compare match interrupt enabled), an interrupt request is generated.

Table 17.7 Timer RE2 Interrupt Sources

Source	Operating mode	Source Name	Interrupt Source	Interrupt Enable Bit
Real-time clock period/overflow	Real-time clock mode	Periodic interrupt triggered every 0.25 seconds	0.25-second period	SEIE025
		Periodic interrupt triggered every 0.5 seconds	0.5-second period	SEIE05
		Periodic interrupt triggered every second	The TRESEC register is updated (one-second period).	SEIE
		Periodic interrupt triggered every minute	The TREMIN register is updated (one-minute period).	MNIE
		Periodic interrupt triggered every hour	The TREHR register is updated (one-hour period).	HRIE
		Periodic interrupt triggered every day	The TREDY register is updated (one-day period).	DYIE
		Periodic interrupt triggered every month	The TREMON register is updated (one-month period).	MOIE
		Periodic interrupt triggered every year	The TREYR register is updated (one-year period).	YRIE
	Compare match timer mode	Overflow interrupt	When the compare match timer overflows.	OVIE
Alarm/compare match	Real-time clock mode	Alarm interrupt	When the alarm time set by the alarm register (TREAMN, TREAHR, or TREAWK register only with enable bit set as 1) and the counter match.	ALIE
	Compare match timer mode	Compare match interrupt	When the compare match timer is compared and matches.	CMIE

17.6 Notes on Timer RE2

- When 0 (count is stopped) is written to the RUN bit in the TRECR register, the count is stopped after three cycles of the count source.
- When switching to module standby, set the RUN bit to 0 (count is stopped) and allow three or more cycles of the count source to elapse before setting the MSTTRE bit in the MSTCR register to 1 (standby).
- Switching registers TREIFR and TREIER must be performed as follows:
  [Real-time clock mode]
  - Switch the TREIER register while the RTCF bit in the TREIFR register is 0 (no interrupt requested).
  - Switch the ALIE bit in the TREIFR register while the ALIF bit in the TREIFR register is 0 (no interrupt requested).

  [Compare match timer mode]
  - Switch the CMIE bit in the TREIER register while the CMIF bit in the TREIFR register is 0 (interrupt requested).
  - Switch the OVIE bit in the TREIER register while the OVIF bit in the TREIFR register is 0 (no interrupt requested).
- When changing the CS3 bit in the TRECSR register, all of the following conditions must be met:
  - The RUN bit is 0 (count is stopped).
  - When changing the CS3 bit from 0 to 1, the CMIF bit is 0 (no interrupt requested) and the OVIF bit is 0 (no interrupt requested).
  - When changing the CS3 bit from 1 to 0, the ALIF bit is 0 (no interrupt requested) and the RTCF bit is 0 (no interrupt requested).

18. Serial Interface (UARTi (i = 0 or 1))

The serial interface consists of two channels: UART0 and UART1.

18.1 Overview

UART0 and UART1 have a dedicated timer to generate the transfer clock and operate independently. It supports two modes: Clock synchronous serial I/O mode and clock asynchronous serial I/O (UART) mode.
Table 18.1 lists the UARTi (i = 0 or 1) Specifications. Figure 18.1 shows the UARTi (i = 0 or 1) Block Diagram. Figure 18.2 shows the Transmit/Receive Unit Block Diagram. Table 18.2 lists the UARTi (i = 0 or 1) Pin Configuration. For details, see **Table 18.4 Clock Synchronous Serial I/O Mode Specifications** and **Table 18.6 Clock Asynchronous Serial I/O Mode Specifications**.

Table 18.1 UARTi (i = 0 or 1) Specifications

Item		Description
I/O pins		3 pins (CLKi, RXDi, and TXDi)
Clock synchronous serial I/O mode	Transfer data format	Transfer data length: 8 bits
	Transfer clock	• The CKDIR bit in the UiMR register is 0 (internal clock): fj/2 (n + 1) fj = f1, f8, f32, or fXCIN n: Value set in the UiBRG register (00h to FFh) • The CKDIR bit in the UiMR register is 1 (external clock): fEXT (input from the CLKi pin)
	Error detection	Overrun error
Clock asynchronous serial I/O mode	Transfer data format	• Character bits (transfer data): Selectable from 7, 8, or 9 bits • Start bit: 1 bit • Parity bit: Selectable from odd, even, or none • Stop bit: Selectable from 1 or 2 bits
	Transfer clock	• The CKDIR bit in the UiMR register is 0 (internal clock): fk/16 (n + 1) fk = f1, f8, f32, or fXCIN n: Value set in the UiBRG register (00h to FFh) • The CKDIR bit in the UiMR register is 1 (external clock): fEXT/16 (n + 1) fEXT (input from the CLKi pin) n: Value set in the UiBRG register (00h to FFh)
	Error detection	Overrun error, framing error, parity error, error sum flag
Interrupt sources		Transmit buffer empty or transmit complete interrupt (multiplexed), and receive complete interrupt

i = 0 or 1

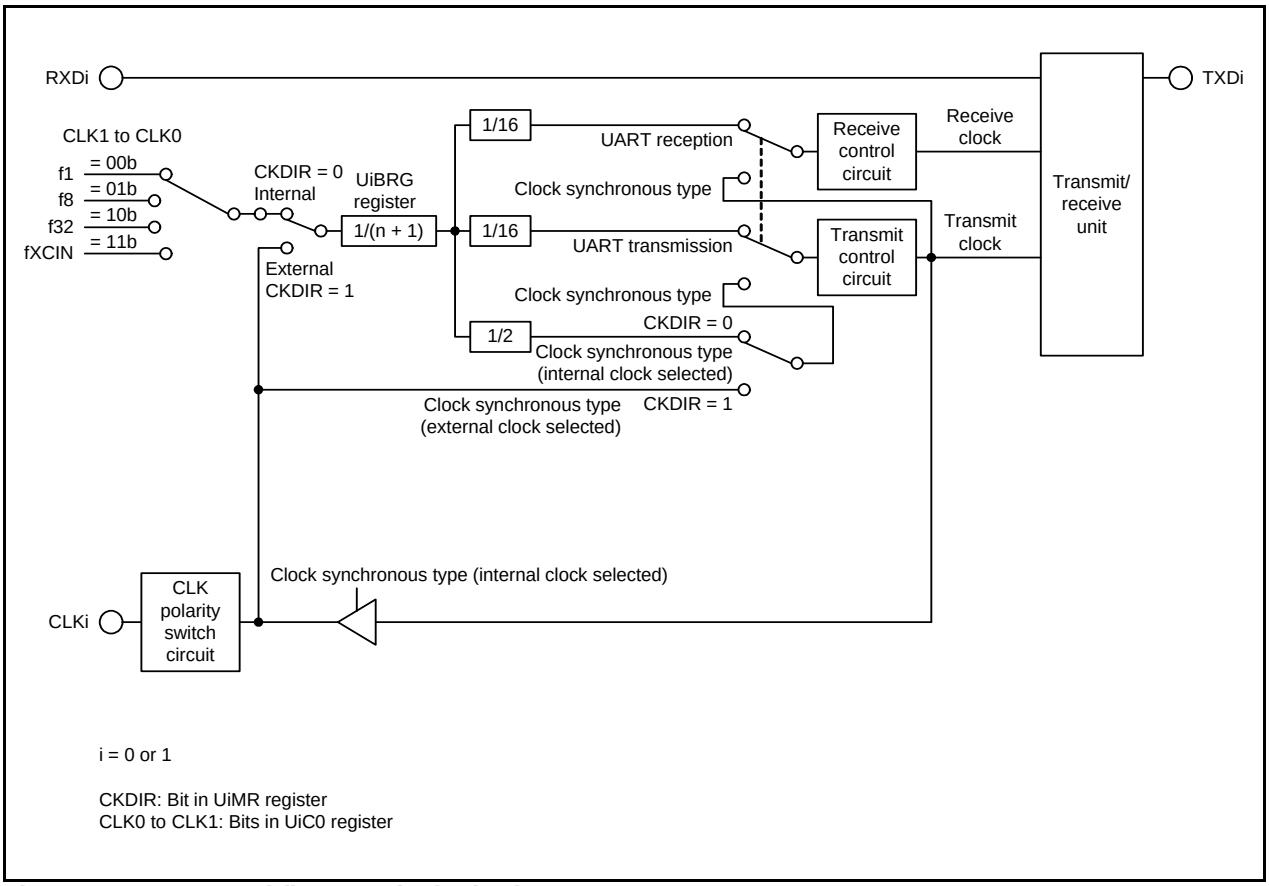
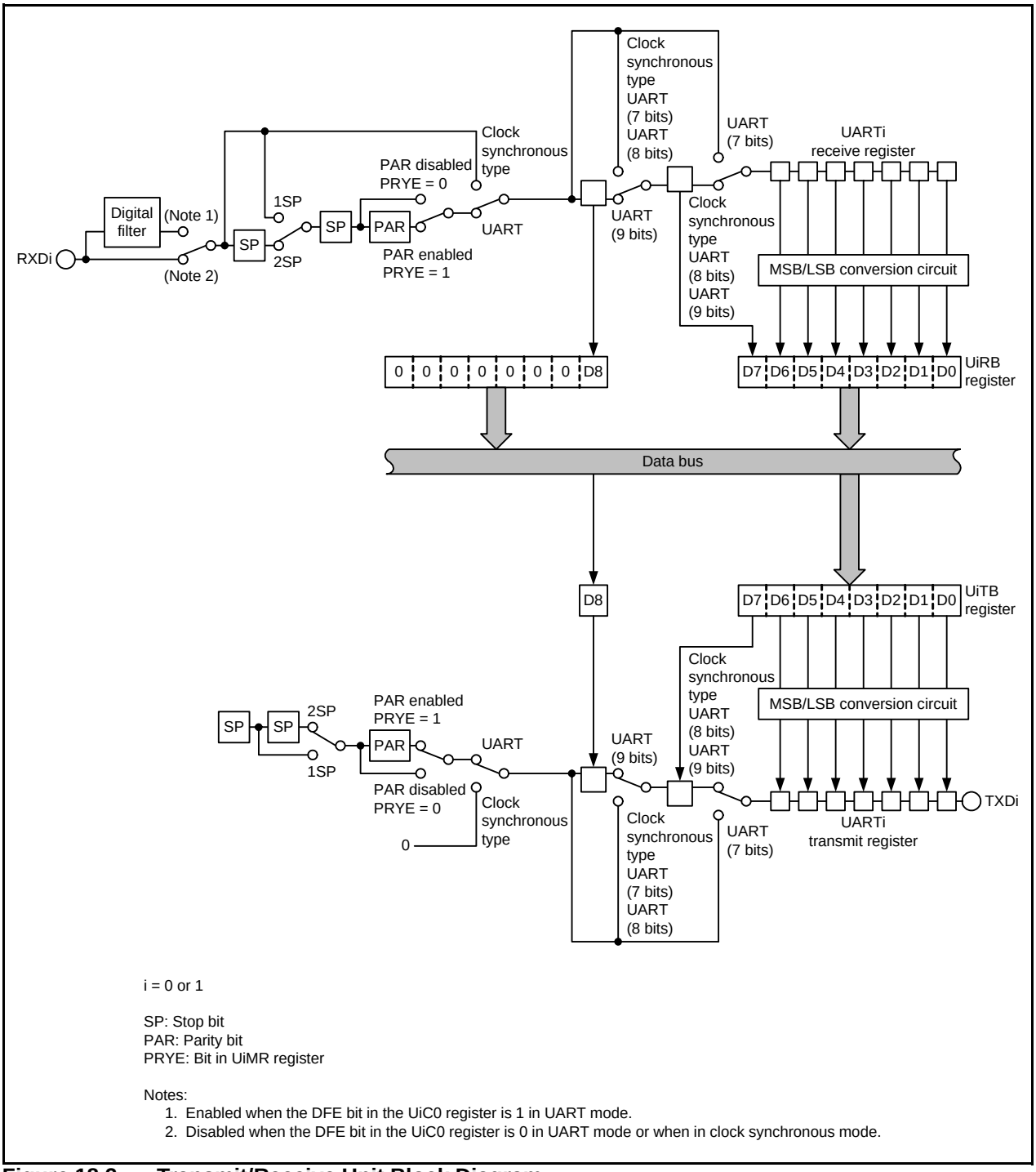


Figure 18.1 UARTi (i = 0 or 1) Block Diagram



i = 0 or 1

SP: Stop bit
PAR: Parity bit
PRYE: Bit in UiMR register

Notes:
1. Enabled when the DFE bit in the UiC0 register is 1 in UART mode.
2. Disabled when the DFE bit in the UiC0 register is 0 in UART mode or when in clock synchronous mode.

Figure 18.2 Transmit/Receive Unit Block Diagram

Table 18.2 UARTi (i = 0 or 1) Pin Configuration

Pin Name	Assigned Pin	I/O	Function
CLK0	P1_6	I/O	Transfer clock input and output
RXD0	P1_4, P1_5, P4_6	I	Serial data input
TXD0	P1_4, P4_2, P4_6	O	Serial data output
CLK1	P0_3	I/O	Transfer clock input and output
RXD1	P0_2	I	Serial data input
TXD1	P0_1	O	Serial data output

18.2 Registers

Table 18.3 lists the UARTi (i = 0 or 1) Register Configuration.

Table 18.3 UARTi (i = 0 or 1) Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
UART0 Transmit/Receive Mode Register	U0MR	00h	00080h	8
UART0 Bit Rate Register	U0BRG	XXh	00081h	8
UART0 Transmit Buffer Register	U0TBL	XXh	00082h	8 (1)
	U0TBH	XXh	00083h	8 (1)
UART0 Transmit/Receive Control Register 0	U0C0	00001000b	00084h	8
UART0 Transmit/Receive Control Register 1	U0C1	00000010b	00085h	8
UART0 Receive Buffer Register	U0RBL	XXh	00086h	8 (1)
	U0RBH	XXh	00087h	8 (1)
UART0 Interrupt Flag and Enable Register	U0IR	00h	00088h	8
UART1 Transmit/Receive Mode Register	U1MR	00h	00190h	8
UART1 Bit Rate Register	U1BRG	XXh	00191h	8
UART1 Transmit Buffer Register	U1TBL	XXh	00192h	8 (1)
	U1TBH	XXh	00193h	8 (1)
UART1 Transmit/Receive Control Register 0	U1C0	00001000b	00194h	8
UART1 Transmit/Receive Control Register 1	U1C1	00000010b	00195h	8
UART1 Receive Buffer Register	U1RBL	XXh	00196h	8 (1)
	U1RBH	XXh	00197h	8 (1)
UART1 Interrupt Flag and Enable Register	U1IR	00h	00198h	8

X: Undefined

Note:

1. For details on access, see the description of the individual registers.

18.2.1 UARTi Transmit/Receive Mode Register (UiMR) (i = 0 or 1)

Address 00080h (U0MR), 00190h (U1MR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bits (1, 2)	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than the above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit (3)	0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	—	Reserved	Set to 0.	R/W

Notes:

1. When setting bits SMD2 to SMD0 to 000b (serial interface disabled), set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. When bits SMD2 to SMD0 are set to 001b (clock synchronous serial I/O mode), the error flags (bits FER, PER, and SUM) in the UiRB register are disabled. When these bits are read, the values are undefined.
3. The PRY bit is enabled when the PRTYE bit is 1 (parity enabled).

18.2.2 UARTi Bit Rate Register (UiBRG) (i = 0 or 1)

Address 00081h (U0BRG), 00191h (U1BRG)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the set value is n, UiBRG divides the count source by n + 1.	00h to FFh	W

Write to the UiBRG register using the MOV instruction while transmission and reception are stopped.
Set bits CLK0 to CLK1 in the UiC0 register before writing to this register.

18.2.3 UARTi Transmit Buffer Register (UiTB) (i = 0 or 1)

Address 00082h (U0TBL), 00192h (U1TBL)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Address 00083h (U0TBH), 00193h (U1TBH)

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data (D8 to D0)	W
b1	—		W
b2	—		W
b3	—		W
b4	—		W
b5	—		W
b6	—		W
b7	—		W
b8	—		W
b9	—	Nothing is assigned. The write value must be 0. The read value is undefined.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

If the transfer data is 9 bits long, write to the UiTBH register first and then the UiTBL register in 8-bit units.
Write to the UiTB register using the MOV instruction. Word access is prohibited.

18.2.4 UARTi Transmit/Receive Control Register 0 (UiC0) (i = 0 or 1)

Address 00084h (U0C0), 00194h (U1C0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	DFE	TXEPT	—	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	UiBRG count source select bits (1)	b1 b0 0 0: f1 0 1: f8 1 0: f32 1 1: fXCIN	R/W
b1	CLK1			R/W
b2	—	Reserved	Set to 0.	R/W
b3	TXEPT	Transmit register empty flag	0: Data present in the transmit register (transmission is in progress) 1: The transmit register empty (transmission is completed)	R
b4	DFE	RXDi digital filter enable bit (2)	0: Digital filter disabled 1: Digital filter enabled	R/W
b5	NCH	Data output select bit	0: TXDi pin is set to CMOS output 1: TXDi pin is set to N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit (3)	0: Transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock 1: Transmit data is output on the rising edge and receive data is input on the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit	0: LSB first 1: MSB first	R/W

Notes:
1. If the UiBRG count source is changed, set the UiBRG register again.
2. The DFE bit is enabled in clock asynchronous serial I/O mode. In clock synchronous serial I/O mode, set this bit to 0 (digital filter disabled).
3. The CKPOL bit is enabled in clock synchronous serial I/O mode.

18.2.5 UARTi Transmit/Receive Control Register 1 (UiC1) (i = 0 or 1)

Address 00085h (U0C1), 00195h (U1C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	UiRRM	UiIRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data present in the UiTB register 1: The UiTB register empty	R
b2	RE	Receive enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Receive complete flag (1)	0: The UiRB register empty 1: Data present in the UiRB register	R
b4	UiIRS	UARTi transmit interrupt source select bit	0: Transmit buffer is empty (TI = 1) 1: Transmission is completed (TXEPT = 1)	R/W
b5	UiRRM	UARTi continuous receive mode enable bit (1)	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	—	Reserved	Set to 0.	R/W
b7	—			

Notes:
1. The RI bit is set to 0 when the UiRBH register is read.
2. In clock asynchronous I/O mode, set the UiRRM bit to 0 (continuous receive mode disabled).

18.2.6 UARTi Receive Buffer Register (UiRB) (i = 0 or 1)

Address 00086h (U0RBL), 00196h (U1RBL)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Address 00087h (U0RBH), 00197h (U1RBH)

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	Receive data (D8 to D0)		R
b1	—			R
b2	—			R
b3	—			R
b4	—			R
b5	—			R
b6	—			R
b7	—			R
b8	—			R
b9	—	Nothing is assigned. The write value must be 0. The read value is undefined.		—
b10	—			
b11	—			
b12	OER	Overrun error flag (1)	0: No overrun error has occurred 1: An overrun error has occurred	R
b13	FER	Framing error flag (1, 2)	0: No framing error has occurred 1: A framing error has occurred	R
b14	PER	Parity error flag (1, 2)	0: No parity error has occurred 1: A parity error has occurred	R
b15	SUM	Error sum flag (1, 2)	0: No error has occurred 1: An error has occurred	R

Note:

1. Bits OER, FER, PER, and SUM are set to 0 (no error has occurred) when bits SMD2 to SMD0 in the UiMR register are set to 000b (serial interface disabled) or the RE bit in the UiC1 register is set to 0 (reception disabled).
   The SUM bit is set to 0 (no error has occurred) when all of bits OER, FER, and PER are set to 0 (no error has occurred). In addition, bits FER and PER are set to 0 when the UiRBH register is read.
   When setting bits SMD2 to SMD0 in the UiMR register to 000b, set the TE bit in the UiC1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. These error flags are invalid when bits SMD2 to SMD0 in the UiMR register are set to 001b (clock synchronous serial I/O mode). When these bits are read, the values are undefined.

The UiRB register must be accessed in 16-bit units. Do not access this register in 8-bit units. When this register is accessed as 16-bit units, it is accessed twice in 8-bit units.

18.2.7 UARTi Interrupt Flag and Enable Register (UiIR) (i = 0 or 1)

Address 00088h (U0IR), 00198h (U1IR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UiTIF	UiRIF	—	—	UiTIE	UiRIE	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	—			
b2	UiRIE	UARTi receive interrupt enable bit	0: Receive interrupt disabled 1: Receive interrupt enabled	R/W
b3	UiTIE	UARTi transmit interrupt enable bit	0: Transmit interrupt disabled 1: Transmit interrupt enabled	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	UiRIF	UARTi receive interrupt flag	0: No receive interrupt requested 1: Receive interrupt requested	R/W
b7	UiTIF	UARTi transmit interrupt flag	0: No transmit interrupt requested 1: Transmit interrupt requested	R/W

UiRIF Bit (UARTi receive interrupt flag)

[Condition for setting to 0]
- When 0 is written to this bit after reading it as 1.

[Condition for setting to 1]
- When the RI bit in the UiC1 register is changed from 0 (the UiRB register empty) to 1 (data present in the UiRB register).

UiTIF Bit (UARTi transmit interrupt flag)

[Condition for setting to 0]
- When 0 is written to this bit after reading it as 1.

[Condition for setting to 1]
- When the transmit buffer becomes empty or transmission completes.

18.3 Operation

UARTi (i = 0 or 1) supports two modes: Clock synchronous serial I/O mode and clock asynchronous serial I/O (UART) mode.

18.3.1 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, transmission or reception is performed using a transfer clock.
Table 18.4 lists the Clock Synchronous Serial I/O Mode Specifications. Table 18.5 lists the Registers and Settings Used in Clock Synchronous Serial I/O Mode.

Table 18.4 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clock	• The CKDIR bit in the UiMR register is 0 (internal clock): fj/(2 (n + 1)) fj = f1, f8, f32, or fXCIN n = Value set in the UiBRG register (00h to FFh) • The CKDIR bit in the UiMR register is 1 (external clock): fEXT (input from the CLKi pin)
Transmit start conditions	To start transmission, the following requirements must be met: (1) • The TE bit in the UiC1 register must be 1 (transmission enabled). • The TI bit in the UiC1 register must be 0 (data present in the UiTB register).
Receive start conditions	To start reception, the following requirements must be met: (1) • The RE bit in the UiC1 register must be 1 (reception enabled). • The TE bit in the UiC1 register must be 1 (transmission enabled). • The TI bit in the UiC1 register must be 0 (data present in the UiTB register).
Interrupt request generation timing	• For transmission: One of the following can be selected. - The UiIRS bit in the UiC1 register is 0 (transmit buffer is empty): When data is transferred from the UiTB register to the UARTi transmit register (at start of transmission). - The UiIRS bit in the UiC1 register is 1 (transmission is completed): When data transmission from the UARTi transmit register is completed. • For reception: When data is transferred from the UARTi receive register to the UiRB register (at completion of reception).
Error detection	• Overrun error (2) This error occurs if the next data reception is started and the 7th bit is received before the UiRB register is read.
Selectable functions	• CLK polarity selection The output and input timing of transfer data can be selected to be either the rising or the falling edge of the transfer clock. • LSB first or MSB first selection The start bit can be selected to be bit 0 or bit 7 when transmission and reception are started. • Continuous receive mode selection Reading the UiRB register enables reception at the same time.

i = 0 or 1

Notes:

1. When an external clock is selected, the requirements must be met in either of the following states:
   • The external clock is set to high when the CKPOL bit in the UiC0 register is 0 (transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock).
   • The external clock is set to low when the CKPOL bit is 1 (transmit data is output on the rising edge and receive data is input on the falling edge of the transfer clock).
2. If an overrun error occurs, the receive data (b0 to b7) in the UiRB register is undefined. The UiRIF bit in the UiIR register remains unchanged.

Table 18.5 Registers and Settings Used in Clock Synchronous Serial I/O Mode

Register	Bit	Function
UiTB	b0 to b7	Set the transmit data.
UiRB	b0 to b7	The receive data can be read.
	OER	Overrun error flag
UiBRG	b0 to b7	Set the bit rate.
UiMR	SMD2 to SMD0	Set to 001b (clock synchronous serial I/O mode).
	CKDIR	Select an internal or external clock.
UiC0	CLK0 to CLK1	Select the UiBRG count source (f1, f8, f32, or fXCIN).
	TXEPT	Transmit register empty flag
	NCH	Select the output type (CMOS or N-channel open-drain output) of the TXDi pin.
	CKPOL	Select the polarity of the transfer clock.
	UFORM	Select LSB first or MSB first.
UiC1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	UiIRS	Select the UARTi transmit interrupt source to be transmit buffer empty or transmit complete.
	UiRRM	Select continuous receive mode from disabled or enabled.

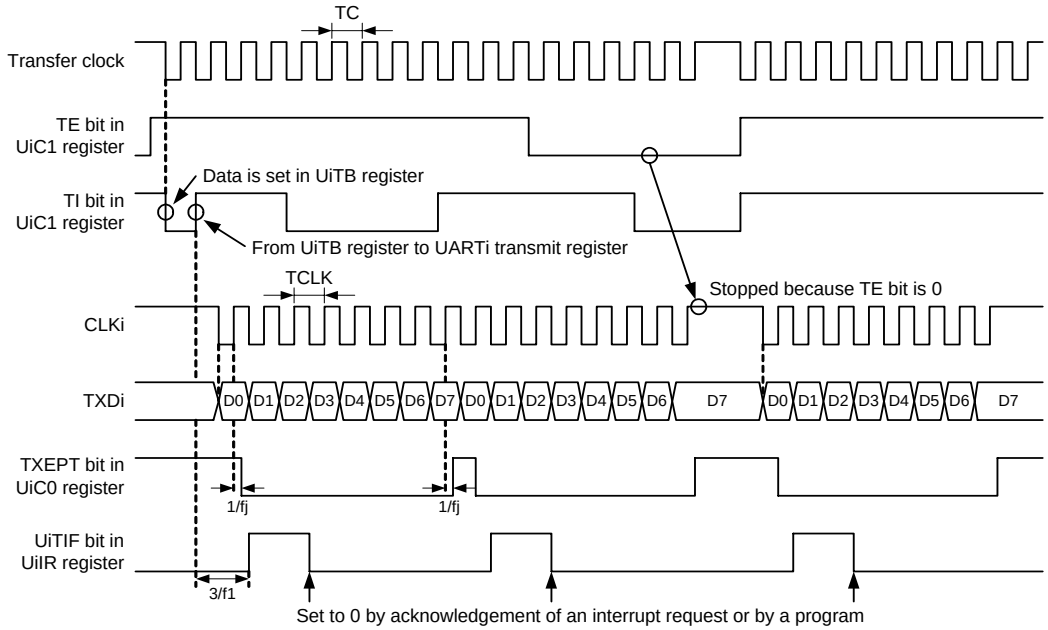
i = 0 or 1

Note:

1. The write value must be 0 for all bits not listed in this table.

18.3.1.1 Operation Examples

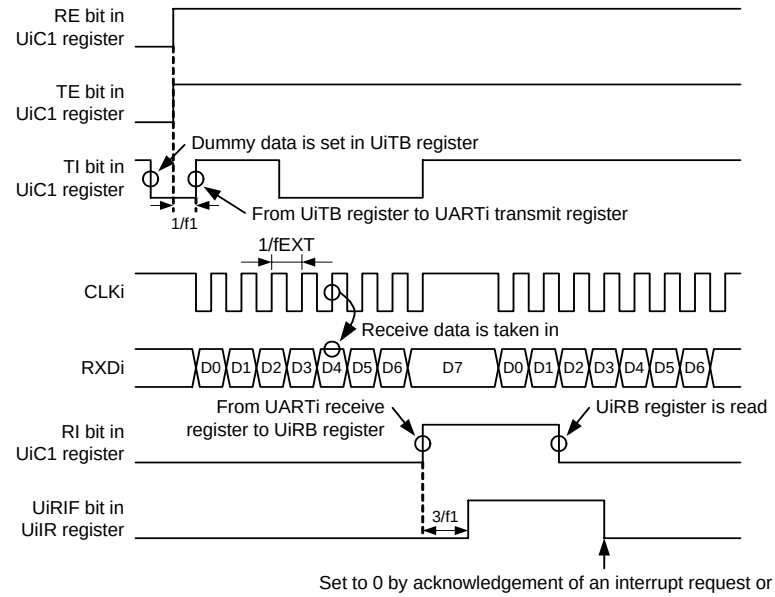
• Transmit timing example (internal clock selected)



The above diagram applies for the following settings:
- CKDIR bit in UiMR register = 0 (internal clock)
- CKPOL bit in UiC0 register = 0 (transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock)
- UiIRS bit in UiC1 register = 0 (transmit buffer is empty)

TC = TCLK = 2 (n + 1)/fj
fj: Frequency of UiBRG count source (f1, f8, f32, or fXCIN)
n: Value set in UiBRG register

• Receive timing example (external clock selected)



fEXT: Frequency of external clock

The above diagram applies for the following settings:
- CKDIR bit in UiMR register = 1 (external clock)
- CKPOL bit in UiC0 register = 0 (transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock)

The following requirements must be met when an input to the CLKi pin is high before data reception:
- TE bit in UiC1 register → 1 (transmission enabled)
- RE bit in UiC1 register → 1 (reception enabled)
- Dummy data is written to UiTB register

i = 0 or 1

Figure 18.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

18.3.1.2 Polarity Select Function

Figure 18.4 shows the Transfer Clock Polarity.
The CKPOL bit in the UiC0 register (i = 0 or 1) can be used to select the polarity of the transfer clock.

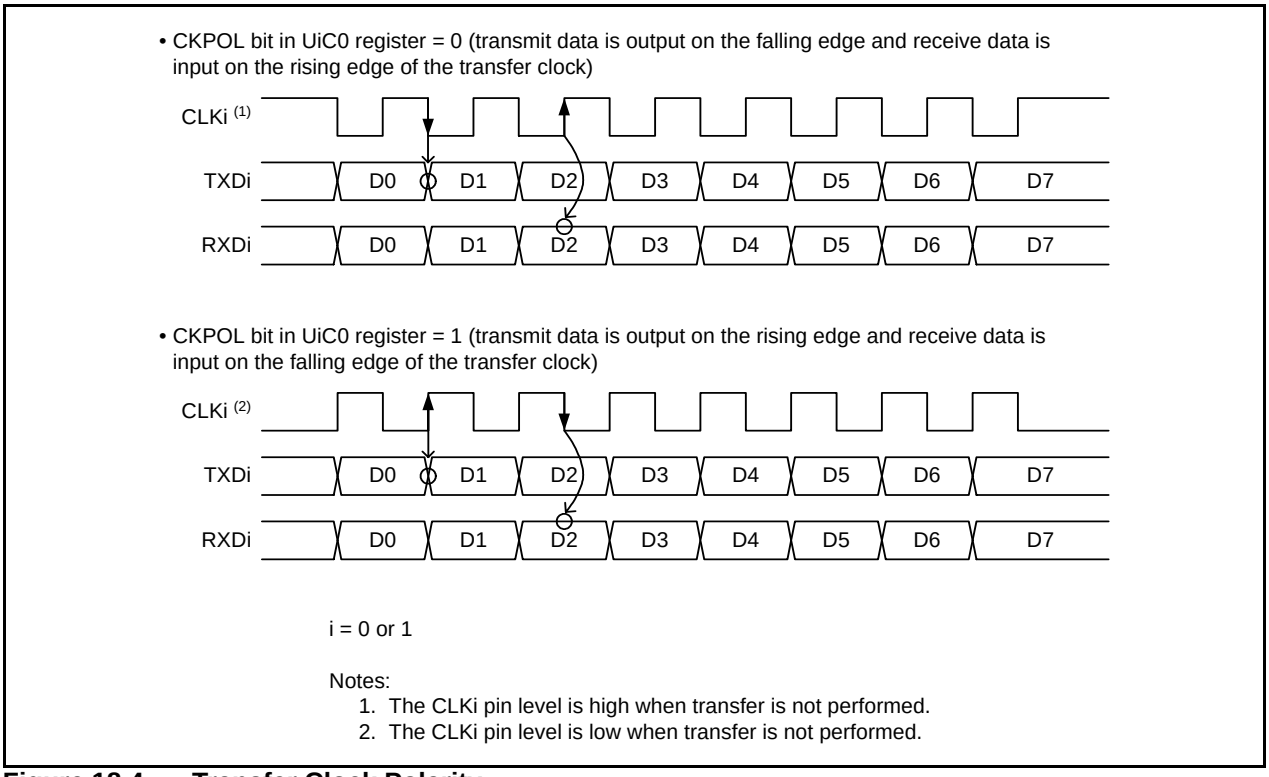


Figure 18.4 Transfer Clock Polarity

18.3.1.3 LSB First or MSB First Selection

Figure 18.5 shows the Transfer Format.
The UFORM bit in the UiC0 register (i = 0 or 1) can be used to select the transfer format.

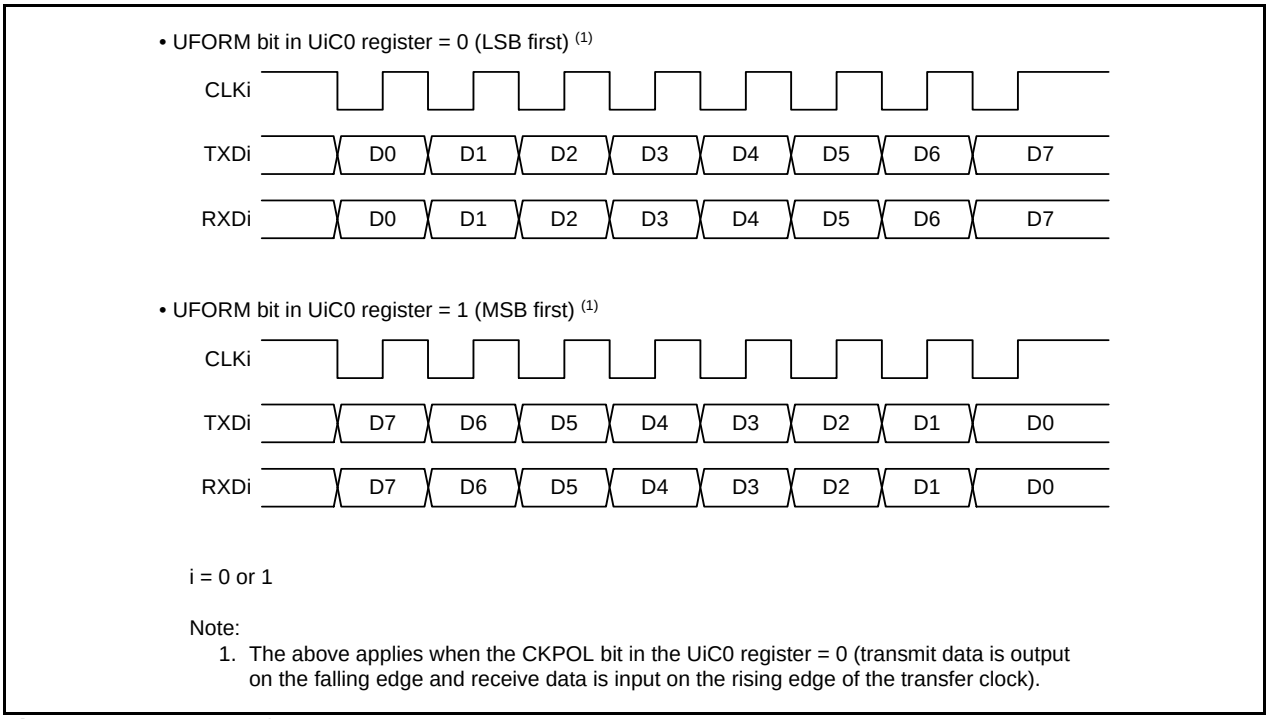


Figure 18.5 Transfer Format

18.3.1.4 Continuous Receive Mode

Continuous receive mode is selected by setting the UiRRM bit in the UiC1 register (i = 0 or 1) to 1 (continuous receive mode enabled). In this mode, reading the UiRB register sets the TI bit in the UiC1 register to 0 (data present in the UiTB register). When the UiRRM bit is 1, do not write dummy data to the UiTB register by a program.

18.3.1.5 Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedure below:

(1) Set the TE bit in the UiC1 register (i = 0 or 1) to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the UiMR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

18.3.2 Clock Asynchronous Serial I/O (UART) Mode

In clock asynchronous serial I/O mode, transmission and reception are performed at an arbitrary bit rate and in an arbitrary format.
Table 18.6 lists the Clock Asynchronous Serial I/O Mode Specifications. Table 18.7 lists the Registers and Settings Used in Clock Asynchronous Serial I/O Mode.

Table 18.6 Clock Asynchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	• Character bits (transfer data): Selectable from 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: Selectable from odd, even, or none • Stop bits: Selectable from 1 or 2 bits
Transfer clock	• The CKDIR bit in the UiMR register is 0 (internal clock): fk/16 (n + 1) fk = f1, f8, f32, or fXCIN n = Value set in the UiBRG register (00h to FFh) • The CKDIR bit in the UiMR register is 1 (external clock): fEXT/16 (n + 1) fEXT (input from the CLKi pin) n = Value set in the UiBRG register (00h to FFh)
Transmit start conditions	To start transmission, the following requirements must be met: • The TE bit in the UiC1 register must be 1 (transmission enabled). • The TI bit in the UiC1 register must be 0 (data present in the UiTB register).
Receive start conditions	To start reception, the following requirements must be met: • The RE bit in the UiC1 register must be 1 (reception enabled). • Start bit detection
Interrupt request generation timing	• For transmission: One of the following can be selected. - The UiIRS bit in the UiC1 register is 0 (transmit buffer is empty): When data is transferred from the UiTB register to the UARTi transmit register (at start of transmission). - The UiIRS bit in the UiC1 register is 1 (transmission is completed): When data transmission from the UARTi transmit register is completed. • For reception: When data is transferred from the UARTi receive register to the UiRB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the next data reception is started and the next to last bit is received before the UiRB register is read. • Framing error This error occurs when the set number of stop bits is not detected. (2) • Parity error This error occurs when parity is enabled, and the number of 1's in the parity and character bits do not match the set number of 1's. (2) • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.

i = 0 or 1
Notes:
1. If an overrun error occurs, the receive data (b0 to b8) in the UiRB register is undefined. The UiRIF bit in the UiIR register remains unchanged.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UARTi receive register to the UiRB register.

Table 18.7 Registers and Settings Used in Clock Asynchronous Serial I/O Mode

Register	Bit	Function
UiTB	b0 to b8	Set the transmit data. (1)
UiRB	b0 to b8	The receive data can be read. (2)
	OER	Overrun error flag
	FER	Framing error flag
	PER	Parity error flag
	SUM	Error sum flag
UiBRG	b0 to b7	Set the bit rate.
UiMR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select an internal or external clock.
	STPS	Select one or two stop bits.
	PRY, PRYE	Select whether parity is enabled and whether odd or even.
UiC0	CLK0 to CLK1	Select the UiBRG count source (f1, f8, f32, or fXCIN).
	TXEPT	Transmit register empty flag
	NCH	Select the output type (CMOS or N-channel open-drain output) of the TXDi pin.
	CKPOL	Set to 0 (transmit data is output on the falling edge and receive data is input on the rising edge of the transfer clock).
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 (LSB first) when transfer data is 7 bits or 9 bits long.
UiC1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	UiIRS	Select the UARTi transmit interrupt source to be transmit buffer empty or transmit complete.
	UiRRM	Set to 0 (continuous receive mode disabled).

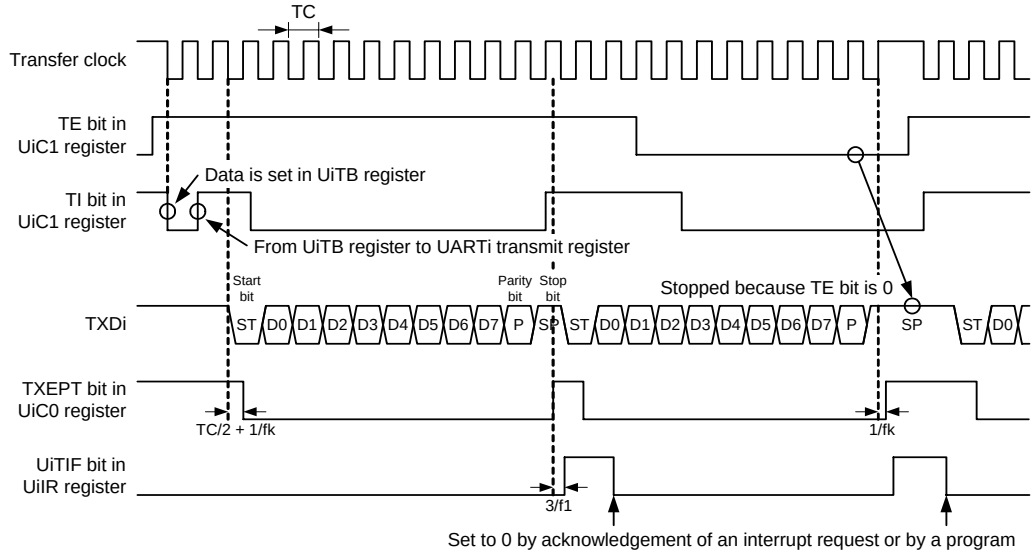
i = 0 or 1

Notes:

1. The bits used are as follows:
   - Bits 0 to 6 when transfer data is 7 bits long
   - Bits 0 to 7 when transfer data is 8 bits long
   - Bits 0 to 8 when transfer data is 9 bits long
2. The contents of the following are undefined: Bits 7 and 8 when transfer data is 7 bits long, and bit 8 when transfer data is 8 bits long.

18.3.2.1 Operation Examples

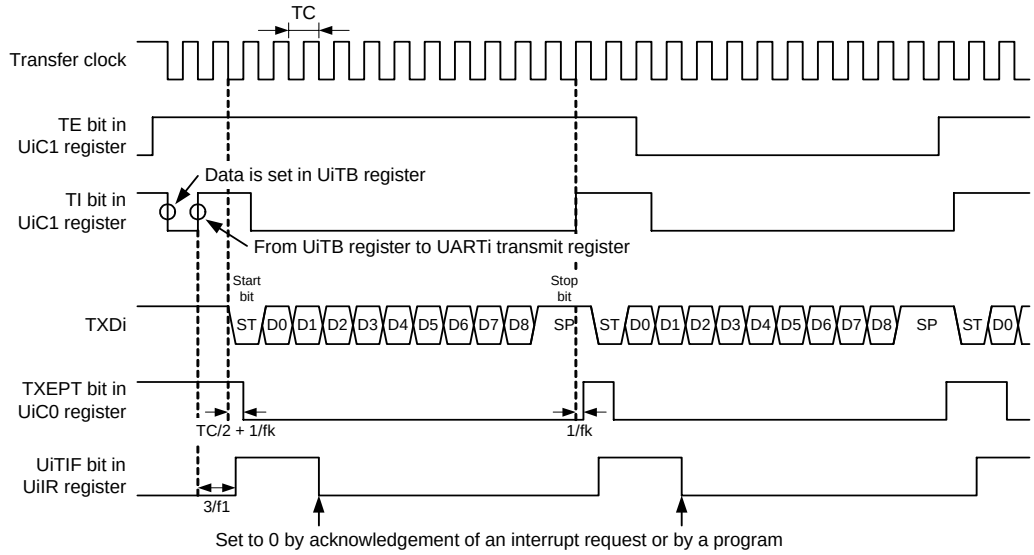
• When transfer data is 8 bits long (parity enabled, one stop bit)



The above diagram applies for the following settings:
- STPS bit in UiMR register = 0 (one stop bit)
- PRYE bit in UiMR register = 1 (parity enabled)
- UiIRS bit in UiC1 register = 1 (transmission is completed)

TC = 16 (n + 1)/fk or 16 (n + 1)/fEXT
fk: Frequency of UiBRG count source (f1, f8, f32, or fXCIN)
fEXT: Frequency of UiBRG count source (external clock)
n: Value set in UiBRG register

• When transfer data is 9 bits long (parity disabled, two stop bits)



The above diagram applies for the following settings:
- STPS bit in UiMR register = 1 (two stop bits)
- PRYE bit in UiMR register = 0 (parity disabled)
- UiIRS bit in UiC1 register = 0 (transmit buffer is empty)

TC = 16 (n + 1)/fk or 16 (n + 1)/fEXT
fk: Frequency of UiBRG count source (f1, f8, f32, or fXCIN)
fEXT: Frequency of UiBRG count source (external clock)
n: Value set in UiBRG register

i = 0 or 1

Figure 18.6 Transmit Timing in Clock Asynchronous Serial I/O Mode

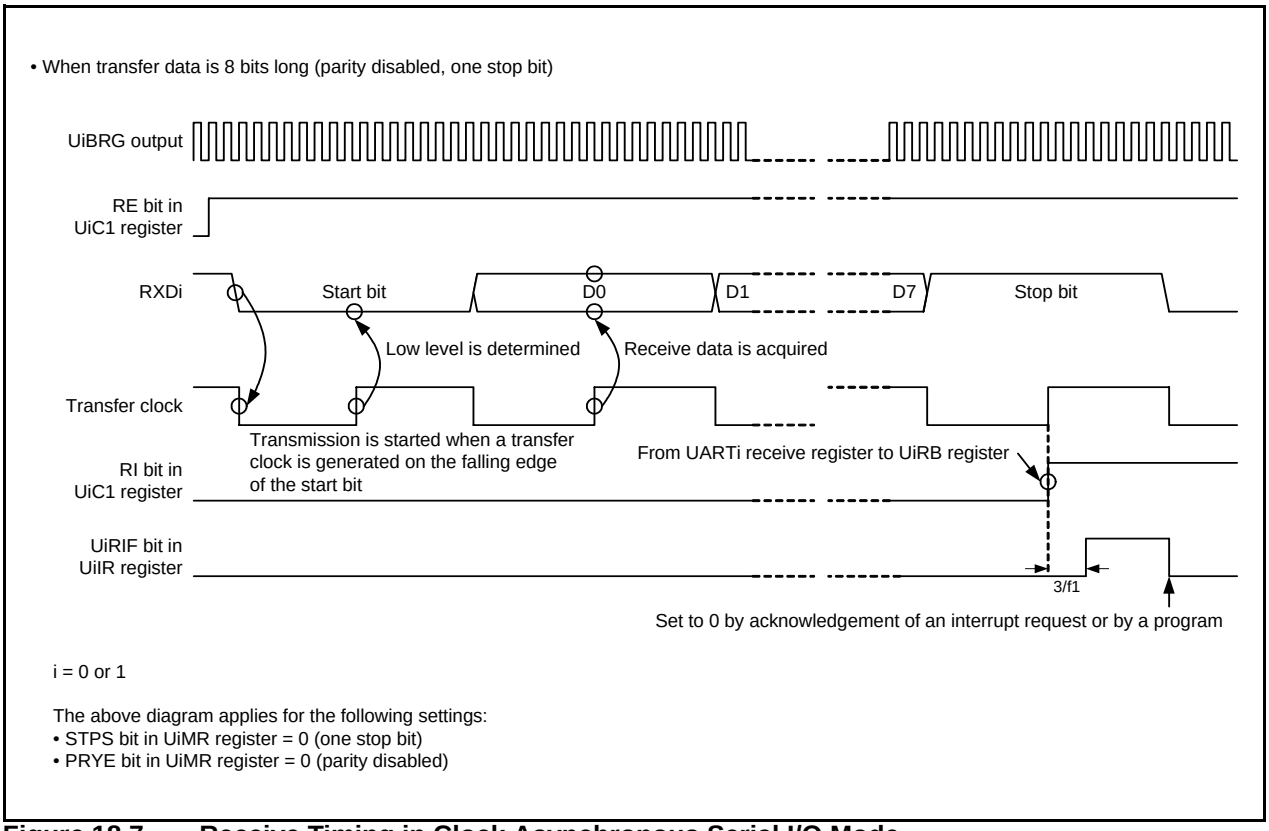


Figure 18.7 Receive Timing in Clock Asynchronous Serial I/O Mode

18.3.2.2 Bit Rate

In clock asynchronous serial I/O mode, the bit rate is obtained by dividing the frequency with the UiBRG register (i = 0 or 1) and further dividing it by 16.
The value to be set in the UiBRG register is calculated as follows:

• When an internal clock is selected

$$\text{Value set in UiBRG register} = \frac{\text{fk}}{\text{Bit rate} \times 16} - 1$$

fk: Frequency of UiBRG count source (f1, f8, f32, or fXCIN)

• When an external clock is selected

$$\text{Value set in UiBRG register} = \frac{\text{fEXT}}{\text{Bit rate} \times 16} - 1$$

fEXT: Frequency of UiBRG count source (external clock)

Table 18.8 Setting Example for Clock Asynchronous Serial I/O Mode (Internal Clock Selected)

Bit Rate (bps)	UiBRG Count Source	System Clock = 20 MHz			System Clock = 18.432 MHz (1)			System Clock = 8 MHz		
		Value Set in UiBRG Register	Actual Rate (bps)	Setting Error (%)	Value Set in UiBRG Register	Actual Rate (bps)	Setting Error (%)	Value Set in UiBRG Register	Actual Rate (bps)	Setting Error (%)
1200	f8	129 (81h)	1201.92	0.16	119 (77h)	1200.00	0.00	51 (33h)	1201.92	0.16
2400	f8	64 (40h)	2403.85	0.16	59 (3Bh)	2400.00	0.00	25 (19h)	2403.85	0.16
4800	f8	32 (20h)	4734.85	-1.36	29 (1Dh)	4800.00	0.00	12 (0Ch)	4807.69	0.16
9600	f1	129 (81h)	9615.38	0.16	119 (77h)	9600.00	0.00	51 (33h)	9615.38	0.16
14400	f1	86 (56h)	14367.82	-0.22	79 (4Fh)	14400.00	0.00	34 (22h)	14285.71	-0.79
19200	f1	64 (40h)	19230.77	0.16	59 (3Bh)	19200.00	0.00	25 (19h)	19230.77	0.16
28800	f1	42 (2Ah)	29069.77	0.94	39 (27h)	28800.00	0.00	16 (10h)	29411.76	2.12
38400	f1	32 (20h)	37878.79	-1.36	29 (1Dh)	38400.00	0.00	12 (0Ch)	38461.54	0.16
57600	f1	21 (15h)	56818.18	-1.36	19 (13h)	57600.00	0.00	8 (08h)	55555.56	-3.55
115200	f1	10 (0Ah)	113636.36	-1.36	9 (09h)	115200.00	0.00	—	—	—

i = 0 or 1
Note:
1. For the high-speed on-chip oscillator, write the adjustment values in registers FR18S0 and FR18S1 to registers FRV1 and FRV2, respectively.
This applies when the high-speed on-chip oscillator is selected as the system clock and the PHISEL register is set to 00h (no division). For details on the accuracy of the high-speed on-chip oscillator, see **24. Electrical Characteristics**.

18.3.2.3 RXDi (i = 0 or 1) Digital Filter

When the DFE bit in the UiC0 register (i = 0 or 1) is 1 (digital filter enabled), the RXDi input is latched internally through the digital filter circuit for noise cancellation. The noise canceller consists of three cascaded latch circuits and a match detection circuit. When the RXDi input is sampled on the base clock with frequency of 16 times the transfer rate and three latch outputs match, the level is passed forward to the next circuit. When they do not match, the previous level is retained.
That is, if the RXDi input retains the same level for three clocks or more, it is recognized as a signal. If not, it is recognized as noise.
Figure 18.8 shows the RXDi Digital Filter Block Diagram.

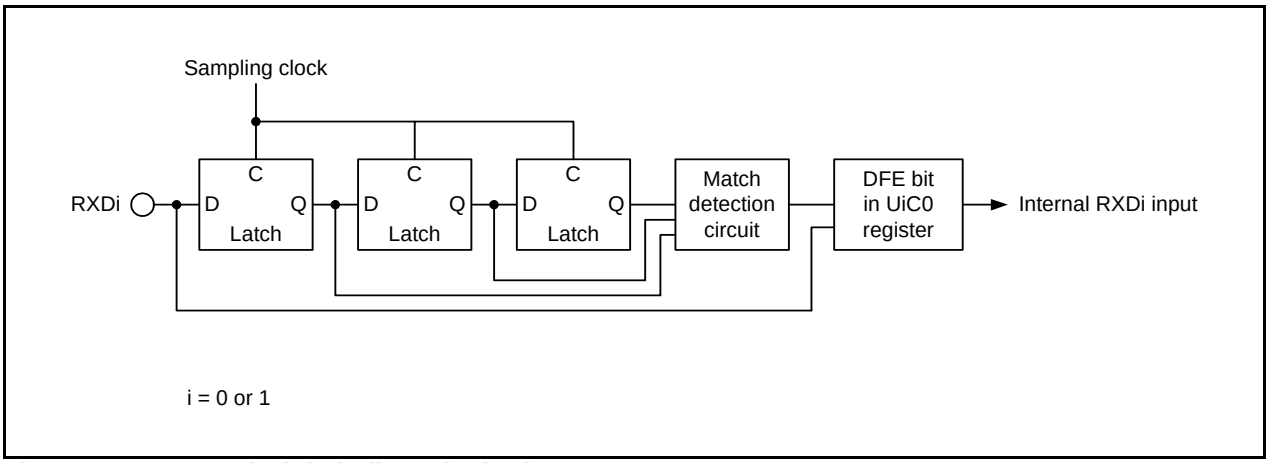


Figure 18.8 RXDi Digital Filter Block Diagram

18.3.2.4 Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedure below:

(1) Set the TE bit in the UiC1 register (i = 0 or 1) to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the UiMR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the UiC1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

18.4 UARTi (i = 0 or 1) Interrupt

The UARTi (i = 0 or 1) interrupt requests are the transmit buffer empty or transmit complete interrupt, and the receive complete interrupt.
Table 18.9 lists the Interrupt Requests.

Table 18.9 Interrupt Requests

Interrupt Request	Interrupt Generation Condition
Transmit buffer empty	UiTIF = 1 (transmit interrupt requested) and UiTIE = 1 (transmit interrupt enabled)
Transmit complete	
Receive complete	UiRIF = 1 (receive interrupt requested) and UiRIE = 1 (receive interrupt enabled)

i = 0 or 1
UiTIF, UiTIE, UiRIF, UiRIE: Bits in UiIR register
Note:
1. The CPU executes interrupt exception handling when the interrupt generation conditions are met and the I flag in the FLG register is 1.

18.5 Notes on Serial Interface (UARTi (i = 0 or 1))

Regardless of clock synchronous I/O mode or clock asynchronous I/O mode, read the UiRB register (i = 0 or 1) in 16-bit units.
When the UiRBH register is read, bits FER and PER in the UiRB register are set to 0 (no framing error, no parity error). Also, the RI bit in the UiC1 register is set to 0 (the UiRB register empty).
To check receive errors, use the data read from the UiRB register.

• Program example to read the receive buffer register

```
MOV.W    0086H, R0        ; Read the U0RB register
```

When the transfer data is 9 bits long in clock asynchronous I/O mode, write to the UiTB register in the order UiTBH first and then UiTBL in 8-bit units.

• Program example to write to the transmit buffer register

```
MOV.B    #XXH, 0083H      ; Write to the U0TBH register
MOV.B    #XXH, 0082H      ; Write to the U0TBL register
```

Do not set the MSTUART0 bit in the MSTCR register or the MSTUART1 bit in the MSTCR1 register to 1 (standby) during communication. When setting the module to the standby state, confirm whether communication has completed. After communication has completed, set bits TE and RE in the UiC1 register to 0 (communication disabled) before setting the module to the standby state. After the module standby state is cleared, the initial settings for communication must be set again.

19. IrDA (Infrared Data Association) Interface

The IrDA interface performs waveform encoding/decoding conforming to IrDA specification version 1.0, and performs communication through pins IrTxD and IrRxD. By connecting these pins to an infrared transceiver/receiver, it is possible to implement infrared transmission and reception conforming to the IrDA specification version 1.0 system.

19.1 Overview

In the IrDA specification version 1.0 system, communication is started at a transfer rate of 9600 bps, and subsequently the transfer rate can be varied as necessary. The IrDA interface does not include a function to change the transfer rate automatically. The transfer rate must be changed by a program.

Figure 19.1 shows the IrDA Interface Block Diagram. Table 19.1 lists the IrDA Interface Pin Configuration.

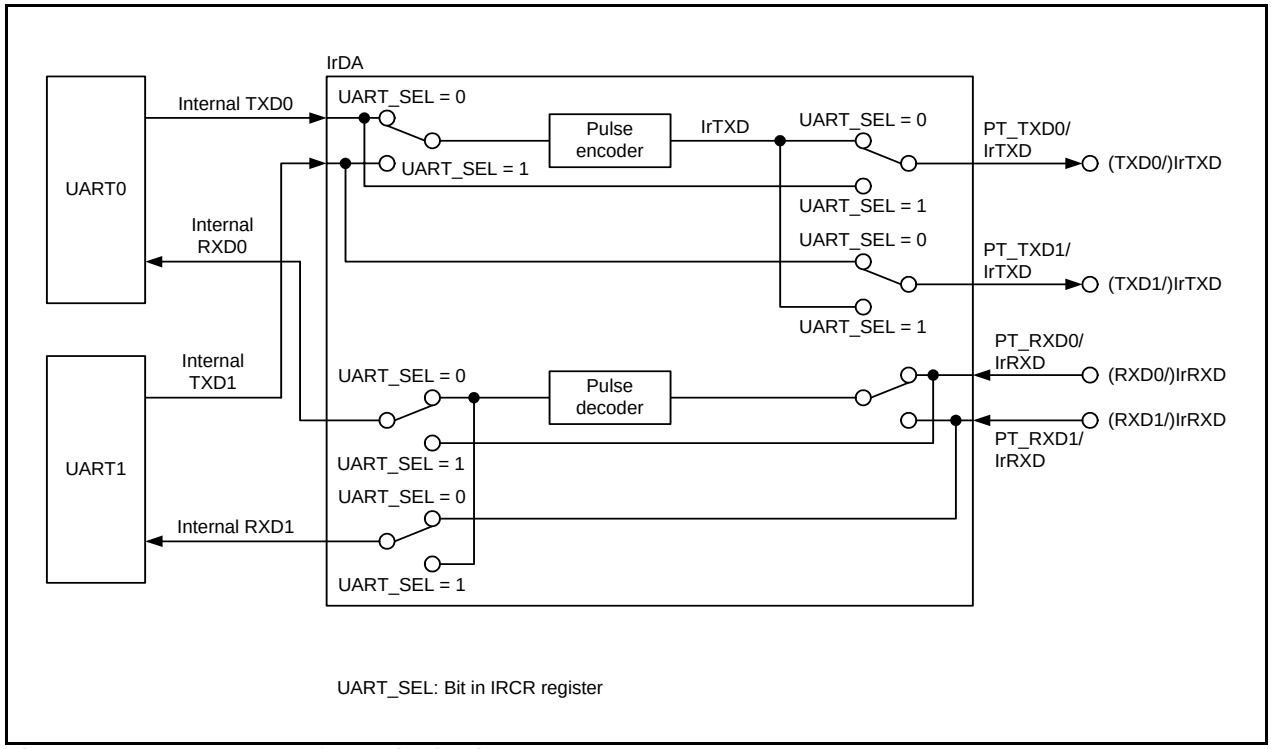


Figure 19.1 IrDA Interface Block Diagram

Table 19.1 IrDA Interface Pin Configuration

Pin Name	I/O	Function
(RXD0/)IrRXD	I	IrDA receive data input for channel 0
(TXD0/)IrTXD	O	IrDA transmit data output for channel 0
(RXD1/)IrRXD	I	IrDA receive data input for channel 1
(TXD1/)IrTXD	O	IrDA transmit data output for channel 1

19.2 Registers

19.2.1 IrDA Control Register (IRCR)

Address 0019Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IRE	IRCKS2	IRCKS1	IRCKS0	IRTXINV	IRRXINV	UART_SEL	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b1	UART_SEL	UART0 or UART1 select bit (1)	0: UART0 1: UART1	R/W
b2	IRRXINV	IrRXD data inversion bit	0: IrRXD input is used as receive data without modification 1: IrRXD input is used as receive data in inverted form	R/W
b3	IRTXINV	IrTXD data inversion bit	0: Transmit data is output from IrTXD without modification 1: Transmit data is output from IrTXD in inverted form	R/W
b4	IRCKS0	IrDA clock select bits (2)	b6 b5 b4 0 0 0: Pulse width = B × 3/16 (3/16 of the bit rate) 0 0 1: Pulse width = f2 0 1 0: Pulse width = f4 0 1 1: Pulse width = f8 1 0 0: Pulse width = f16 1 0 1: Pulse width = f32 1 1 0: Pulse width = f64 1 1 1: Pulse width = f128	R/W
b5	IRCKS1			R/W
b6	IRCKS2			R/W
b7	IRE	IrDA enable bit (3)	0: IrDA disabled (TXD/IrTXD pin functions as TXD pin, and RXD/IrRXD pin functions as RXD pin) 1: IrDA enabled (TXD/IrTXD pin functions as IrTXD pin, and RXD/IrRXD pin functions as IrRXD pin)	R/W

Notes:
1. Set the UART_SEL bit while UART operation is stopped (the TE bit is 0 and the RE bit is 0 in the U0C1 or U1C1 register), and the IRE bit is 0 (IrDA disabled).
2. When an external clock or fXCIN is selected as the UART transfer clock and the IrDA interface is used, set bits IRCKS2 to IRCKS0 to 000b (pulse width = B × 3/16).
3. Change the UART transfer clock when the IRE bit is 0 (IrDA disabled). In addition, change each bit in the IRCR register when the IRE bit is 0 (IrDA disabled).

The IRCR register is used to select the functions of UART0 and UART1.

IRRXINV Bit (IrRXD data inversion bit)

This bit is used to specify inversion of the logic level for the IrRXD input. At inversion, the high-level pulse width specified by bits IRCKS0 to IRCKS2 is set to the low-level pulse width.

IRTXINV Bit (IrTXD data inversion bit)

This bit is used to specify inversion of the logic level for the IrTXD output. At inversion, the high-level pulse width specified by bits IRCKS0 to IRCKS2 is set to the low-level pulse width.

Bits IRCKS0 to IRCKS2 (IrDA clock select bits)

These bits are used to set the high-level pulse width in encoding the IrTXD output pulse.

19.3 Operation

19.3.1 Transmission

In transmission, the output signal from the UART (UART frame) is converted to an IR frame by the IrDA interface (see Figure 19.2). When the serial data is 0, a high-level pulse of 3/16 the bit rate (period equivalent to the width of one bit) is output (initial value). The high-level pulse width can be changed by bits IRCKS0 to IRCKS2 in the IRCR register. In the IrDA specification, the high-level pulse width is fixed at a minimum of 1.41 μs and a maximum of (3/16 + 2.5%) × bit rate or (3/16 × bit rate) + 1.08 μs. When the system clock (f) is 20 MHz, 1.6 μs can be set as the minimum high-level pulse width at 1.41 μs or above. When the serial data is 1, no pulse is output.

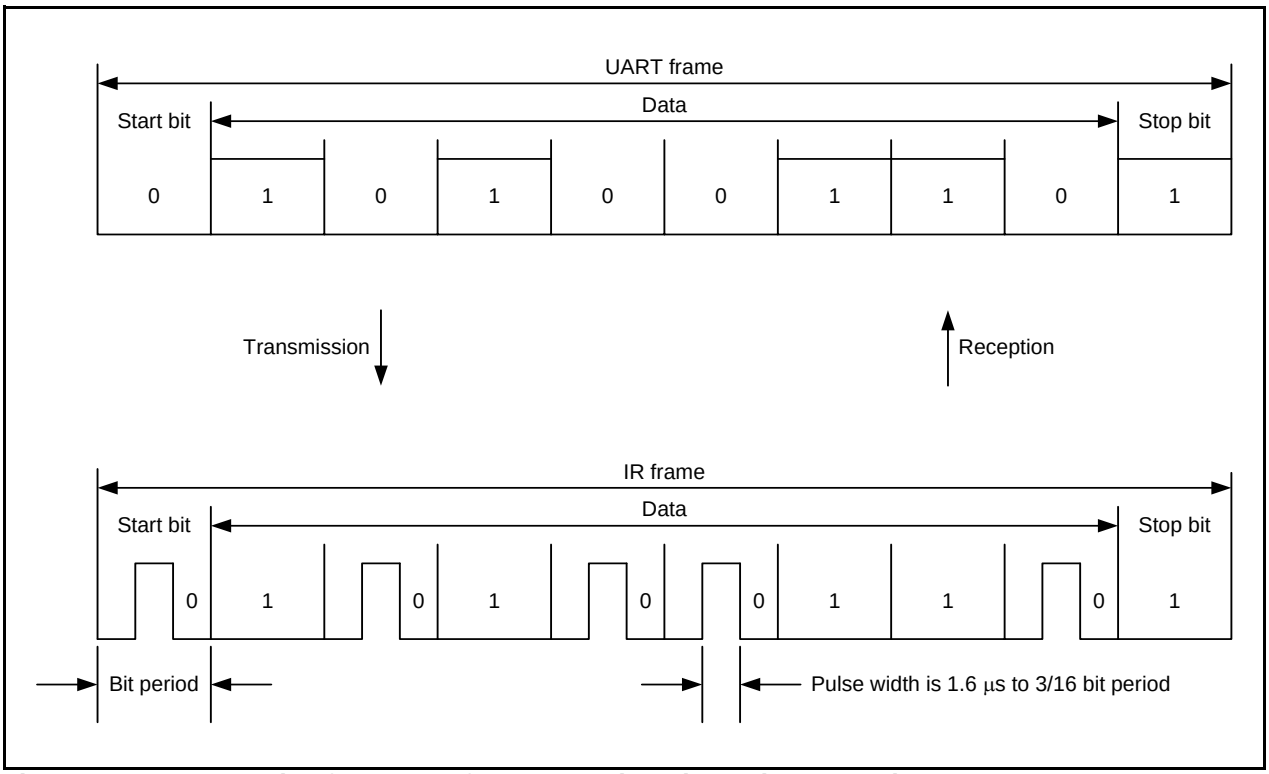


Figure 19.2 Example of IrDA Interface Transmit and Receive Operation

19.3.2 Reception

In reception, IR frame data is converted to a UART frame by the IrDA interface and input to the UART. When a high-level pulse is detected, 0 data is output. If there is no pulse during a one-bit period, 1 data is output. Note that a pulse shorter than the minimum pulse width of 1.41 μs will also be identified as a 0 signal.

19.3.3 High-Level Pulse Width Selection

When making the pulse width shorter than 3/16 times the bit rate in transmission, see **Table 19.2 IRCKS0 to IRCKS2 Bit Settings** for applicable IRCKS0 to IRCKS2 bit settings (minimum pulse width) and system clock (f) and bit rate selections.

Table 19.2 IRCKS0 to IRCKS2 Bit Settings

System Clock (f) (MHz)	Upper Row: Bit Rate (bps)/Lower Row: Bit Period × 3/16 (μs)					
	2400	9600	19200	38400	57600	115200
	78.13	19.53	9.77	4.88	3.26	1.63
2	010	010	010	010	010	—
2.097152	010	010	010	010	010	—
2.4576	010	010	010	010	010	—
3	011	011	011	011	011	—
3.6864	011	011	011	011	011	—
4.9152	011	011	011	011	011	—
5	011	011	011	011	011	011
6	100	100	100	100	100	—
6.144	100	100	100	100	100	—
7.3728	100	100	100	100	100	—
8	100	100	100	100	100	—
9.8304	100	100	100	100	100	—
10	100	100	100	100	100	100
12	101	101	101	101	101	—
12.288	101	101	101	101	101	—
14	101	101	101	101	101	—
14.7456	101	101	101	101	101	—
16	101	101	101	101	101	—
16.9344	101	101	101	101	101	—
17.2032	101	101	101	101	101	—
18	101	101	101	101	101	—
19.6608	101	101	101	101	101	—
20	101	101	101	101	101	101

—: A UART bit rate setting cannot be made.

19.4 UART and IrDA Setting Procedure

To use the IrDA interface, follow the procedure below:

(1) Set the TE bit to 0 (transmission disabled) and the RE bit to 0 (reception disabled) in the UiC1 register (i = 0 or 1), and then set bits SMD2 to SMD0 in the UiMR register to 000b (serial interface disabled).
(2) Set the IRE bit in the IRCR register to 0 (IrDA disabled).
(3) Set the UART_SEL bit in the IRCR register to 0 (UART0) or 1 (UART1).
(4) Set the function mapping registers (PML0, PMH1, and PMH4) for ports 0, 1, and 4 to assign the IrRXD pin to P0_2, P1_5, P1_4, or P4_6.
(5) Set the function mapping registers (PML4, PMH4, PMH1, and PML0) for ports 0, 1, and 4 to assign the IrTXD pin to P42, P46, P14, or P01.
(6) Set the UART communication control bits (bits in registers UiMR, UiBRG, and UiC0; i = 0 or 1) selected in step (3).
(7) Set the other bits (bit 2 to bit 6) while the IRE bit in the IRCR register is 0 (IrDA disabled).
(8) Set the IRE bit in the IRCR register to 1 (IrDA enabled).
(9) Set the TE bit to 1 (transmission enabled) or the RE bit to 1 (reception enabled) in the UART UiC1 register selected in step (3).
(10) Write transmit data to the UART transmit buffer register selected in step (3) (at transmission).

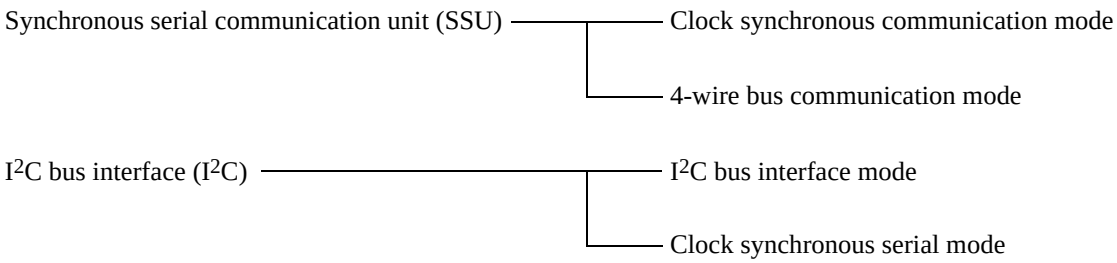
Note: For IrDA reception, complete the setting of the initial level of the pin while UART operation is stopped (the TE bit is 0 and the RE bit is 0 in the UiC1 register) and the IRE bit is 0 (IrDA disabled).

20. Clock Synchronous Serial Interface

20.1 Overview

The clock synchronous serial interface is configured as follows:

Clock synchronous serial interface



20.1.1 Mode Selection

The clock synchronous serial interface supports four modes.
Table 20.1 lists the bits associated with mode selection.

Table 20.1 Mode Selections

IICSEL Bit in IICCR Register (1)	ICE Bit in SICR1 Register (1)	MS Bit in SIMR2 Register (1)	Function Name	Mode
0	0	0	Synchronous serial communication unit	Clock synchronous communication mode
		1		4-wire bus communication mode
1	1	0	I2C bus interface	I2C bus interface mode
		1		Clock synchronous serial mode

Note:
1. Do not make the settings other than the combinations listed in the above table. Otherwise, operation cannot be guaranteed.

20.1.2 Synchronous Serial Communication Unit (SSU)

The synchronous serial communication unit (SSU) supports clock synchronous serial data communication. Table 20.2 lists the Synchronous Serial Communication Unit Specifications. Figure 20.1 shows the Synchronous Serial Communication Unit Block Diagram.

Table 20.2 Synchronous Serial Communication Unit Specifications

Item	Description
Transfer data format	Transfer data length: 8 to 16 bits
Communication modes	• Clock synchronous communication mode • 4-wire bus communication mode (including bidirectional communication) - Master or slave device can be selected. - Continuous transmission and reception of serial data are supported because the shift, transmit, and receive registers are independent.
I/O pins	SSCK (I/O): Clock I/O pin SSI (I/O): Data I/O pin $\overline{\text{SSO}}$ (I/O): Data I/O pin $\overline{\text{SCS}}$ (I/O): Chip select I/O pin
Transfer clocks	• When the MST bit in the SICR1 register is 0 (slave mode) External clock (input from the SSCK pin) • When the MST bit in the SICR1 register is 1 (master mode) Internal clock (selectable among f1/256, f1/128, f1/64, f1/32, f1/16, f1/8 and f1/4, output from the SSCK pin) • The clock polarity and phase can be selected.
Receive error detection	Overrun error detection Indicates an overrun error has occurred during reception and reception is terminated in error. When the next serial data reception is completed while the RDRF bit in the SISR register is 1 (data present in the SIRDR register), the ORER_AL bit is set to 1 (overrun error).
Multimaster error detection	Conflict error detection When starting a serial communication while the MS bit in the SIMR2 register is 1 (4-wire bus communication mode) and the MST bit in the SICR1 register is 1 (master mode), the CE_ADZ bit in the SISR register is set to 1 (conflict error) if the $\overline{\text{SCS}}$ pin input is low. When the $\overline{\text{SCS}}$ pin input changes from low to high during transfer while the MS bit in the SIMR2 register is 1 (4-wire bus communication mode) and the MST bit in the SICR1 register is 0 (slave mode), the CE_ADZ bit in the SISR register is set to 1.
Interrupt requests	5 requests (transmit end, transmit data empty, receive data full, overrun error, and conflict error (1))
Selectable functions	• Data transfer direction MSB first or LSB first can be selected. • SCL clock polarity The level (low or high) when the clock is stopped can be selected. • SCL clock phase The edge for data change and data download can be selected.

Note:
1. A conflict error occurs only in 4-wire bus communication mode.

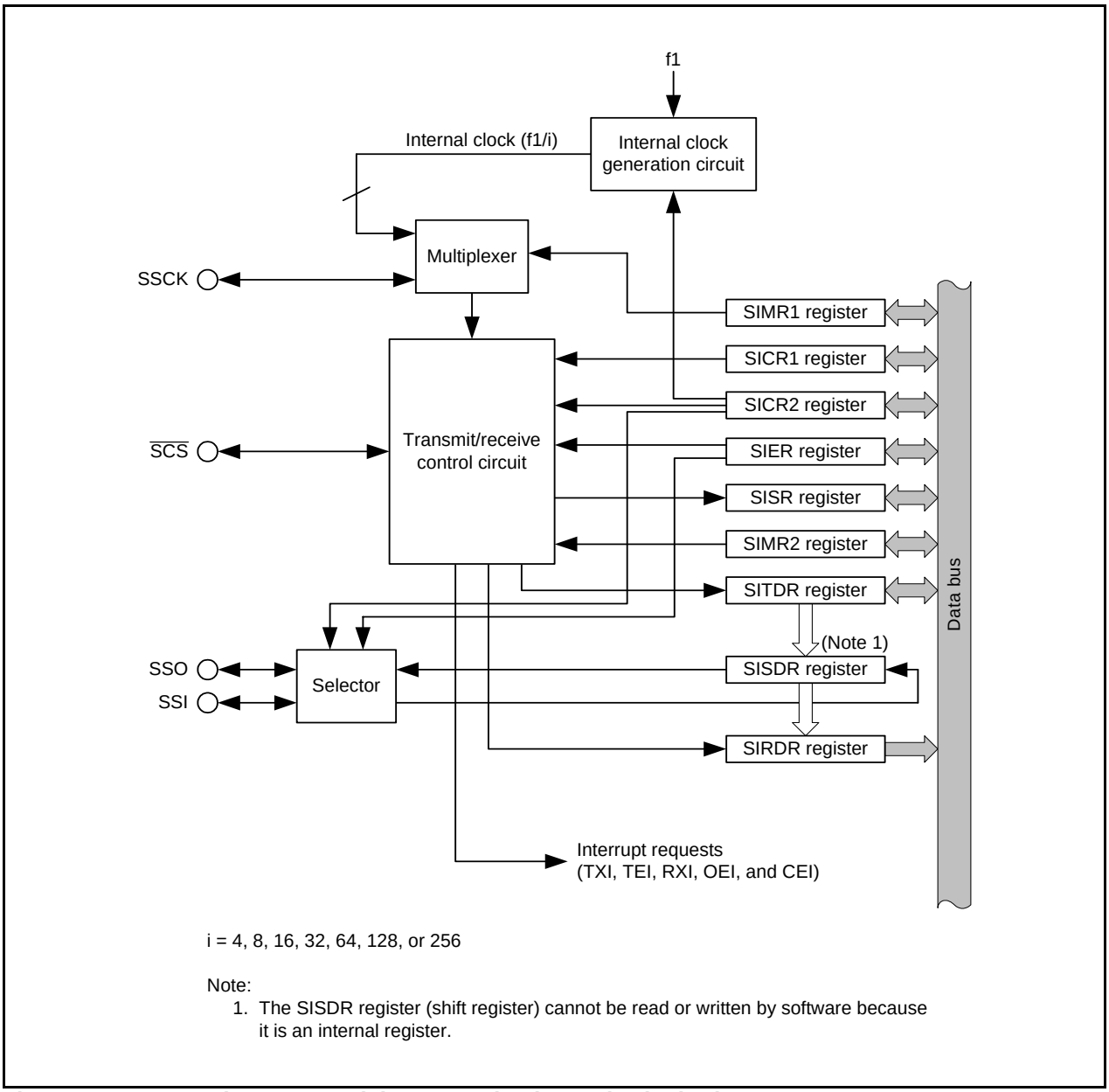


Figure 20.1 Synchronous Serial Communication Unit Block Diagram

Table 20.3 Synchronous Serial Communication Unit Pin Configuration

Pin Name	I/O	Function
SSI	I/O	Data I/O
$\overline{SCS}$	I/O	Chip select I/O
SSCK	I/O	Clock I/O
SSO	I/O	Data I/O

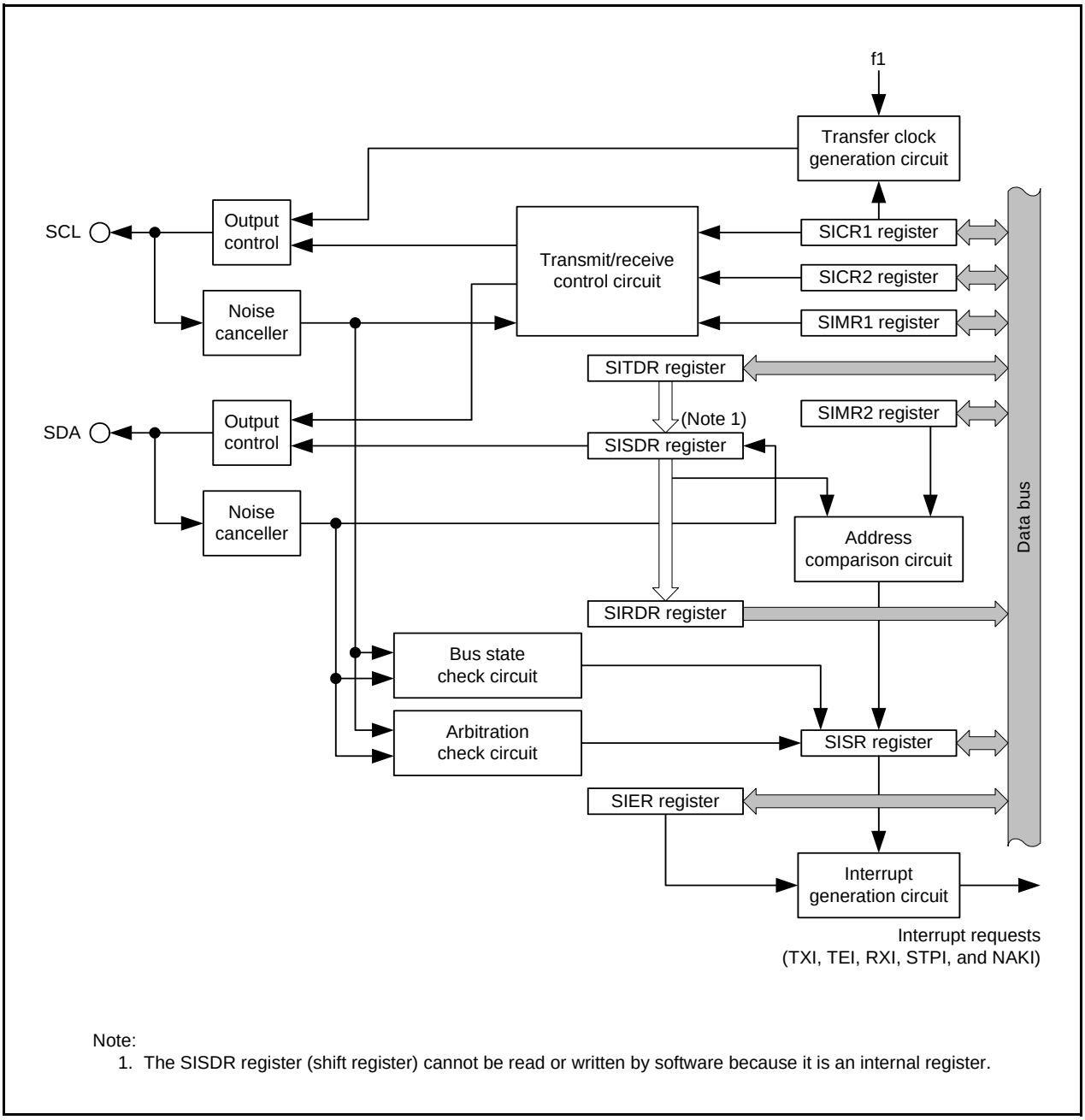
20.1.3 I²C bus Interface

The I²C bus interface is the circuit that performs serial communication based on the data transfer format of the Philips I²C bus.

Table 20.4 lists the I²C bus Interface Specifications. Figure 20.2 shows the I²C bus Interface Block Diagram. Table 20.5 lists the I²C bus Interface Pin Configuration. Figure 20.3 shows an External Circuit Connection Example for Pins SCL and SDA.

Table 20.4 I²C bus Interface Specifications

Item	Description
Communication modes	• I²C bus interface mode - Master or slave device can be selected. - Continuous transmission and reception are supported (because the shift, transmit, and receive registers are independent). - Start/stop conditions are automatically generated in master mode. - Automatic loading of the acknowledge bit during transmission. - Bit synchronization and wait function are included. (In master mode, the state of the SCL signal is monitored per bit and the timing is synchronized automatically. If the transfer is not ready yet, the SCL signal is held low and the interface stands by.) - Direct drive of pins SCL and SDA (N-channel open-drain output) is supported. • Clock synchronous serial mode Continuous transmission and reception are supported (because the shift, transmit, and receive registers are independent).
I/O pins	SCL (I/O): Serial clock I/O pin SDA (I/O): Serial data I/O pin
Transfer clocks	• When the MST bit in the SICR1 register is 0 (slave mode) External clock (input from the SCL pin) • When the MST bit in the SICR1 register is 1 (master mode) Internal clock selected by bits CKS0 to CKS3 in the SICR1 register and bits IICTCTWI and IICTCHALF in the IICCR register (output from the SCL pin)
Receive error detection	Overrun error detection (clock synchronous serial mode) Indicates an overrun error has occurred during reception. When the last bit of the next data is received while the RDRF bit in the SISR register is 1 (data present in the SIRDR register), the ORER_AL bit is set to 1 (overrun error).
Interrupt sources	• I²C bus interface mode: 6 sources Transmit data empty (including when slave address matches), transmit end, receive data full (including when slave address matches), arbitration lost, NACK detection, and stop condition detection • Clock synchronous serial mode: 4 sources Transmit data empty, transmit end, receive data full, and overrun error
Selectable functions	• I²C bus interface mode The output level of the acknowledge signal during reception can be selected. • Clock synchronous serial mode MSB first or LSB first can be selected as the data transfer direction. • SDA digital delay The digital delay value of the SDA pin can be selected by bits SDADLY0 to SDADLY1 in the IICCR register.



Note:
1. The SISDR register (shift register) cannot be read or written by software because it is an internal register.

Figure 20.2 I²C bus Interface Block Diagram

Table 20.5 I²C bus Interface Pin Configuration

Pin Name	Function
SCL	Clock I/O
SDA	Data I/O

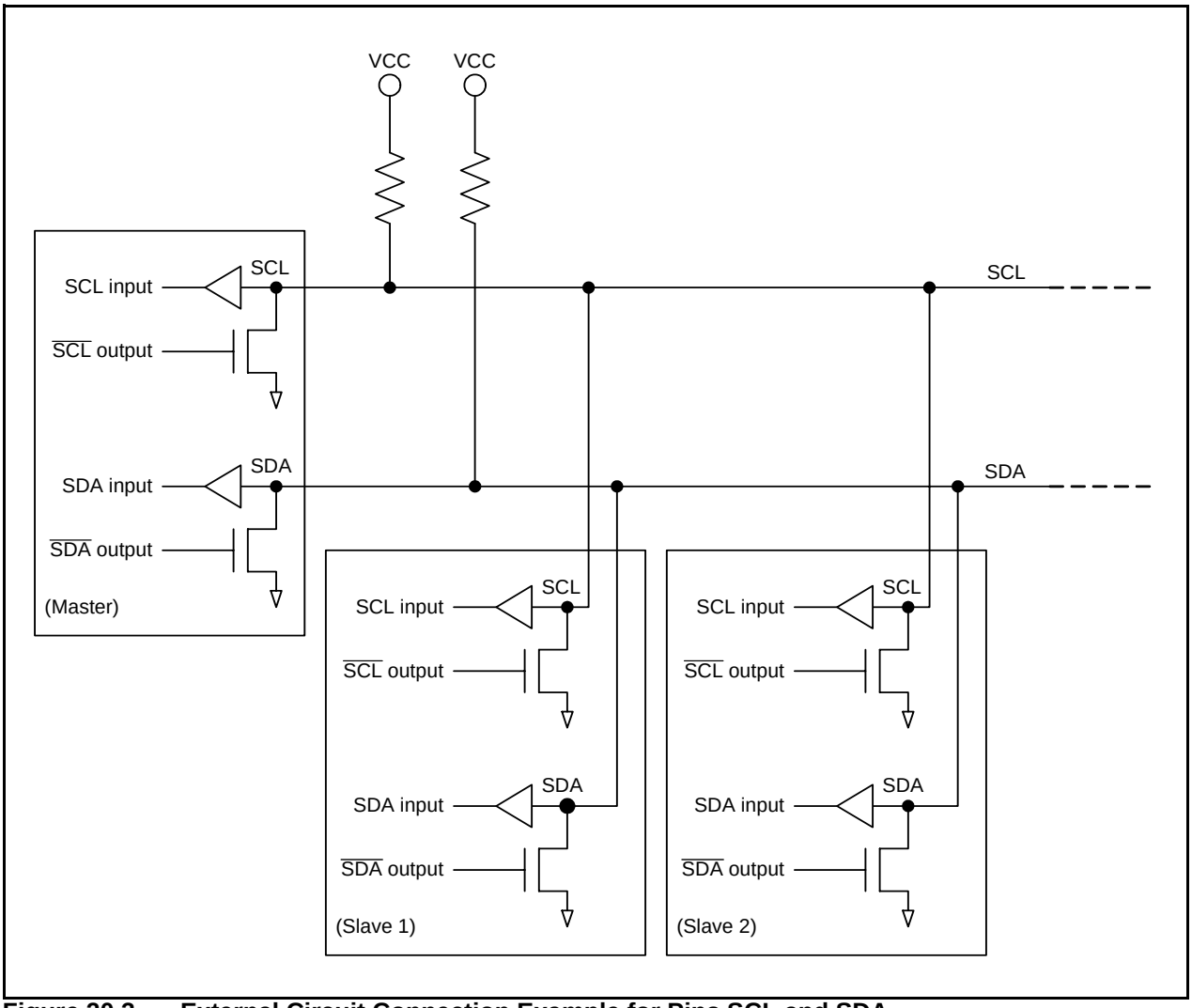


Figure 20.3 External Circuit Connection Example for Pins SCL and SDA

20.2 Registers

The registers of the clock synchronous serial interface are multiplexed with the SSU and I2C bus functions. Table 20.6 lists the Clock Synchronous Serial Interface Register Configuration.

Table 20.6 Clock Synchronous Serial Interface Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
IIC Control Register	IICCR	00001110b	00160h	8
SS Bit Counter Register	SSBR	11111000b	00161h	8
SI Transmit Data Register	SITDR	FFh	00162h	8 or 16 (1)
		FFh	00163h	
SI Receive Data Register	SIRDR	FFh	00164h	8 or 16 (1)
		FFh	00165h	
SI Control Register 1	SICR1	00h	00166h	8
SI Control Register 2	SICR2	01111101b	00167h	8
SI Mode Register 1	SIMR1	(Note 6)	00168h	8
SI Interrupt Enable Register	SIER	00h	00169h	8
SI Status Register	SISR	00h	0016Ah	8
SI Mode Register 2	SIMR2	00h	0016Bh	8

Notes:

1. Perform an 8-bit access when the I2C bus function is used and a 16-bit access when the SSU function is used.
2. In standby mode, the values of bits SCLO and SDAO in the SICR2 register, bits BC0 to BC3 in the SIMR1 register, and the internal registers are initialized. The other bits in registers SIMR1 and SICR2 and the other registers are not initialized.
3. When performing a write access after standby mode, insert at least one NOP instruction.
4. Do not set to the standby state during operation of the I2C bus or SSU function.
5. In standby state, all registers cannot be written but can be read.
6. The value after a reset is 00010000b when the SSU function is used, and 00011000b when the I2C bus function is used.

20.2.1 IIC Control Register (IICCR)

Address 00160h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SDADLY1	SDADLY0	IICTCHALF	IICTCTWI	—	—	—	IICSEL
After Reset	0	0	0	0	1	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I2C bus switch bit (1)	0: SSU function 1: I2C bus function	R/W
b1	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b2	—			
b3	—			
b4	IICTCTWI	I2C double transfer rate select bit (2, 3)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the SICR1 register 1: Transfer rate is twice the value set with bits CKS0 to CKS3 in the SICR1 register	R/W
b5	IICTCHALF	I2C half transfer rate select bit (2, 3)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the SICR1 register 1: Transfer rate is half the value set with bits CKS0 to CKS3 in the SICR1 register	R/W
b6	SDADLY0	SDA pin digital delay select bits (3, 4)	b7 b6 0 0: Digital delay of 3 × f1 cycles 0 1: Digital delay of 11 × f1 cycles 1 0: Digital delay of 19 × f1 cycles 1 1: Do not set.	R/W
b7	SDADLY1			R/W

Notes:
1. Initialize all the registers before switching between the I2C bus function and the SSU function.
2. Do not set both bits IICTCTWI and IICTCHALF to 1 when the I2C bus function is used. Set both these bits to 0 when the SSU function is used.
3. Set this bit at the initial setting and do not rewrite it during operation.
4. Do not set a digital delay which is half or more than the transfer rate.

20.2.2 SS Bit Counter Register (SSBR)

Address 00161h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	BS3	BS2	BS1	BS0
After Reset	1	1	1	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BS0	SSU data transfer length setting bits (1, 2)	b3 b2 b1 b0 0 0 0 0: 16 bits 1 0 0 0: 8 bits 1 0 0 1: 9 bits 1 0 1 0: 10 bits 1 0 1 1: 11 bits 1 1 0 0: 12 bits 1 1 0 1: 13 bits 1 1 1 0: 14 bits 1 1 1 1: 15 bits Other than the above: Do not set.	R/W
b1	BS1			R/W
b2	BS2			R/W
b3	BS3			R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	—			
b6	—			
b7	—			

Notes:
1. Do not write to bits BS0 to BS3 during operation of the SSU function. When the RE_STIE bit in the SIER register is 0 (data reception disabled) and the TE_NAKIE bit is 0 (data transmission disabled), write to bits BS0 to BS3.
2. The settings other than the determined values are invalid.

The setting of the SSBR register is valid when the SSU function is used. The setting of the SSBR register is invalid when the I^2C bus function is used.

Bits BS0 to BS3 (SSU data transfer length setting bits)

As the SSU data transfer length, 8 to 16 bits can be used.

20.2.3 SI Transmit Data Register (SITDR)

Address 00162h, 00163h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Store the transmit data. (1) When it is detected that the SISDR register is empty, the stored transmit data is transferred to the SISDR register and transmission is started. If the next transmit data has been written to the SITDR register during the data transmission from the SISDR register, the data can be transmitted consecutively. When the MLS bit in the SIMR1 register is 1 (data transfer with LSB first), the data with inverted MSB and LSB is read after writing to the SITDR register.	R/W

Note:

1. Use 8-bit access when the I^2C bus function is used. Use 16-bit access when the SSU function is used. Do not access this register in 8-bit units. When this register is accessed as 16-bit units, it is accessed twice in 8-bit units. When the SITDR register is accessed, TDRE is disabled and transmit operation is started.

20.2.4 SI Receive Data Register (SIRDR)

Address 00164h, 00165h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Store the receive data. (1, 2, 3) When 1 byte of data has been received by the SISDR register, the receive data is transferred to the SIRDR register and the receive operation is completed. At this time, the next receive operation is enabled. Continuous reception is enabled using registers SISDR and SIRDR.	R

Notes:

1. When the ORER bit in the SISR register is set to 1 (overrun error), the SIRDR register retains the data received before an overrun error occurs. The receive data (data in the SISDR register) when an overrun error occurs is discarded.
2. Use 8-bit access when the I^2C bus function is used. Use 16-bit access when the SSU function is used. Do not access this register in 8-bit units. When this register is accessed as 16-bit units, it is accessed twice in 8-bit units. When SIRDR is accessed, the RDRF bit is set to 0 (no data in the SIRDR register).
3. Read the SIRDR register when the RDRF bit is 1 (data present in the SIRDR register).

20.2.5 SI Control Register 1 (SICR1)

In the SICR1 register, the bit functions differ depending on the SSU function and the I^2C bus function.

20.2.5.1 When SSU Function is Used

Address 00166h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transfer clock select bits (1)	b3 b2 b1 b0 0 0 0 0: f1/256 0 0 0 1: f1/128 0 0 1 0: f1/64 0 0 1 1: f1/32 0 1 0 0: f1/16 0 1 0 1: f1/8 0 1 1 0: f1/4 Other than the above: Do not set.	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	CKS3			R/W
b4	TRS	Reserved	Set to 0 when the SSU function is used.	R/W
b5	MST	Master/slave select bit (2, 3, 4)	0: Slave mode 1: Master mode	R/W
b6	RCVD	Receive disable bit (5)	0: Next receive operation continues 1: Next receive operation disabled	R/W
b7	ICE	Reserved	Set to 0 when the SSU function is used.	R/W

Notes:

1. In master mode, make the setting according to the required transfer rate. For details on the transfer rate, see **20.3.1.1 Transfer Clock**.
2. If an overrun error occurs in master receive mode of clock synchronous serial mode, the MST bit is set to 0 and slave receive mode is entered.
3. When the MST bit is 1 (master mode), the SSCK pin functions as the transfer clock output pin. When the CE_ADZ bit in the SISR register is set to 1 (conflict error), the MST bit is set to 0 (slave mode).
4. In multimaster operation, use the MOV instruction to set the MST bit.
5. The RCVD bit is disabled when the MST bit is 0 (slave mode).

20.2.5.2 When I²C bus Function is Used

Address 00166h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transfer clock select bits (1)	b3 b2 b1 b0 0 0 0 0: f1/28 0 0 0 1: f1/40 0 0 1 0: f1/48 0 0 1 1: f1/64 0 1 0 0: f1/80 0 1 0 1: f1/100 0 1 1 0: f1/112 0 1 1 1: f1/128 1 0 0 0: f1/56 1 0 0 1: f1/80 1 0 1 0: f1/96 1 0 1 1: f1/128 1 1 0 0: f1/160 1 1 0 1: f1/200 1 1 1 0: f1/224 1 1 1 1: f1/256	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	CKS3			R/W
b4	TRS	Transmit/receive select bit (2, 3, 4, 6)	0: Receive mode 1: Transmit mode	R/W
b5	MST	Master/slave select bit (4, 5, 6)	0: Slave mode 1: Master mode	R/W
b6	RCVD	Receive disable bit (7)	After the SIRDR register is read while TRS = 0, 0: Next receive operation continues 1: Next receive operation disabled	R/W
b7	ICE	I²C bus interface enable bit (8)	0: Output from SCL and SDA is disabled (Input to SCL and SDA is enabled) 1: Transfer with I²C bus interface function is enabled	R/W

Notes:

1. In master mode, make the setting according to the required transfer rate. For details on the transfer rate, see **Tables 20.9** and **20.10 Transfer Rate Examples**. In slave mode, a transfer clock is used for maintaining the data setup time in transmit mode. For details on this function, see • **Maintaining Data Setup Time during Slave Transmit Operation** in **20.4.2.5 Slave Transmit Operation**.
2. Rewrite the TRS bit between transfer frames.
3. In slave receive mode, when the first 7 bits after the start condition matches the slave address set in the SIMR2 register and the 8th bit is 1, the TRS bit is set to 1.
4. If arbitration is lost in master mode of I²C bus interface mode, bits MST and TRS are set to 0 and slave receive mode is entered.
5. When an overrun error occurs in master receive mode of clock synchronous serial mode, the MST bit is set to 0 and slave receive mode is entered.
6. In multimaster operation, use the MOV instruction to set bits TRS and MST.
7. When the MST bit is 0 (slave mode), set the RCVD bit to 0.
8. When 0 is written to the ICE bit in the SICR1 register or 1 is written to the SIRST bit in the SICR2 register while the I²C bus interface is operating, the values of the BBSY bit in the SICR2 register and the STOP bit in the SISR register may be undefined.

20.2.6 SI Control Register 2 (SICR2)

In the SICR2 register, the bit functions differ depending on the SSU function and the I^2C bus function.

20.2.6.1 When SSU Function is Used

Address 00167h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BBSY	SCP	SDAO	SDAOP	SCLO	—	SIRST	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b1	SIRST	Control block reset bit (4)	When a hang-up occurs due to communication failure during operation, writing 1 to this bit initializes the control block and the shift register. The values in the internal registers (1) are retained.	R/W
b2	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b3	SCLO	Reserved	The read value is 1.	R
b4	SDAOP	SDAO write protect bit (2)	If 0 is written, the output level can be changed by the SDAO bit. Writing 1 to the SDAO bit has no effect. The read value is 1.	R/W
b5	SDAO	Serial data output value control bit	When this bit read, serial data output is monitored: 0: Serial data output is set to low 1: Serial data output is set to high When written: (2, 3) 0: Data output is set to low 1: Data output is set to high	R/W
b6	SCP	Reserved	The write value is invalid.	R/W
b7	BBSY			

Notes:
1. Registers SSBR, SITDR, SIRDR, SIMR1, SIMR2, SICR1, SICR2, SIER, and SISR
2. For the data output after serial data transmission, the last bit value of the transmitted serial data is retained. If the content of the SDAO bit is rewritten before or after serial data transmission, the change is immediately reflected in the data output until transfer starts. Do not write to the SDAO bit during data transfer.
   Do not rewrite the SDAO bit in 4-wire bus communication mode.
3. When writing to the SDAO bit, write 0 to the SDAOP bit and write 0 or 1 to the SDAO bit simultaneously using the MOV instruction.
4. After writing 1 to the SIRST bit, write 0 to bits RE_STIE and TE_NAKIE in the SIER register. When 1 is then written to bits RE_STIE and TE_NAKIE, transmission and reception can be performed again.

20.2.6.2 When I²C bus Function is Used

Address 00167h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BBSY	SCP	SDAO	SDAOP	SCLO	—	SIRST	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b1	SIRST	I²C bus control block reset bit (6, 7, 8)	When hang-up occurs due to communication failure during operation, writing 1 initializes the control block without setting ports or resetting registers (1).	R/W
b2	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b3	SCLO	SCL monitor flag	0: Internal SCL signal is set to low 1: Internal SCL signal is set to high	R
b4	SDAOP	SDAO write protect bit	When rewriting the SDAO bit, write 0 to this bit simultaneously. (2) The read value is 1.	R/W
b5	SDAO	Serial data output value control bit	When read 0: SDA pin output is held low 1: SDA pin output is held high When written: (2, 3) 0: SDA pin output is changed to low 1: SDA pin output is changed to high-impedance (High-level output via an external pull-up resistor)	R/W
b6	SCP	Start/stop condition generation disable bit	When writing to the BBSY bit, write 0 to this bit simultaneously. (4) The read value is 1. Writing 1 is invalid.	R/W
b7	BBSY	Bus busy bit (5, 8)	When read: 0: Bus is released (SDA signal changes from low to high while SCL signal is held high) 1: Bus is occupied (SDA signal changes from high to low while SCL signal is held high) When written: 0: Stop condition generated 1: Start condition generated	R/W

Notes:
1. All SFRs except the shift register, bits SCLO and SDAO, and bits BC0 to BC3 in the SIMR1 register.
2. When rewriting the SDAO bit, write 0 to the SDAOP bit simultaneously using the MOV instruction.
3. For the data output after serial data transmission, the last bit value of the transmitted serial data is retained. If the content of the SDAO bit is rewritten before or after serial data transmission, the change is immediately reflected in the data output until transmission starts. Do not write to the SDAO bit during transfer operation.
4. Enabled in master mode with the I²C bus function. When writing to the BBSY bit, write 0 to the SCP bit simultaneously using the MOV instruction. Execute the same way when a start condition is regenerated.
5. Disabled in clock synchronous serial mode.
6. To reset the control block in I²C bus interface mode, follow **20.4.7 Procedure for Resetting Control Block in I²C bus Interface Mode**. In clock synchronous serial mode, set bits RE_STIE and TE_NAKIE in the SIER register again after writing 1 to the SIRST bit.
7. When the SIRST bit is set to 1 in I²C bus interface mode, the STOP bit in the SISR register may be set to 1 (a stop condition is detected after the frame is transferred).
8. When 0 is written to the ICE bit in the SICR1 register or 1 is written to the SIRST bit in the SICR2 register while the I²C bus interface is operating, the values of the BBSY bit in the SICR2 register and the STOP bit in the SISR register may be undefined.

   Even if a start condition is generated by writing 0 to the SDAO bit, the state does not change the transfer enabled state. Only generation of a start condition by writing 1 to the BBSY bit is valid.
   Since the SCL signal is fixed at low, no stop condition can be generated by writing 1 to the SDAO bit. Generate a stop condition by writing 0 to the BBSY bit.

20.2.7 SI Mode Register 1 (SIMR1)

In the SIMR1 register, the bit functions differ depending on the SSU function and the I^2C bus function.

20.2.7.1 When SSU Function is Used

Address 00168h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	CPOS_WAIT	CPHS	—	BC3	BC2	BC1	BC0
After Reset	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bit counters 0 to 3	b3 b2 b1 b0 0 0 0 0: Remaining 16 bits 0 0 0 1: Remaining 1 bit 0 0 1 0: Remaining 2 bits 0 0 1 1: Remaining 3 bits 0 1 0 0: Remaining 4 bits 0 1 0 1: Remaining 5 bits 0 1 1 0: Remaining 6 bits 0 1 1 1: Remaining 7 bits 1 0 0 0: Remaining 8 bits 1 0 0 1: Remaining 9 bits 1 0 1 0: Remaining 10 bits 1 0 1 1: Remaining 11 bits 1 1 0 0: Remaining 12 bits 1 1 0 1: Remaining 13 bits 1 1 1 0: Remaining 14 bits 1 1 1 1: Remaining 15 bits	R
b1	BC1			R
b2	BC2			R
b3	BC3			R
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	CPHS	Transfer clock phase select bit (1)	0: Data change at odd edge (data download at even edge) 1: Data change at even edge (data download at odd edge)	R/W
b6	CPOS_WAIT	Clock select/wait insertion bit (1)	0: High when clock is stopped 1: Low when clock is stopped	R/W
b7	MLS	MSB first/LSB first select bit	0: Data transfer with MSB first 1: Data transfer with LSB first	R/W

Note:

1. For the settings of bits CPHS and CPOS_WAIT, see **20.3.1.2 Association between Transfer Clock Polarity, Phase, and Data**.
   When the MS bit in the SIMR2 register is 0 (clock synchronous communication mode), set the CPHS bit to 0 and the CPOS_WAIT bit to 0.

Bits BC0 to BC3 (Bit counters 0 to 3)

The state of the shift register during transmission can be read.

20.2.7.2 When I²C bus Function is Used

Address 00168h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	CPOS_WAIT	CPHS	—	BC3	BC2	BC1	BC0
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bit counters 0 to 2	I²C bus interface mode (Read: Number of remaining transfer bits; Write: Number of next transfer data bits) (1, 2) b2 b1 b0 0 0 0: 9 bits (3) 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits Clock synchronous serial mode (Read: Number of remaining transfer bits; Write: Always 000b) b2 b1 b0 0 0 0: 8 bits 0 0 1: 1 bit 0 1 0: 2 bits 0 1 1: 3 bits 1 0 0: 4 bits 1 0 1: 5 bits 1 1 0: 6 bits 1 1 1: 7 bits	R/W
b1	BC1			R/W
b2	BC2			R/W
b3	BC3	Bit counter 3	When rewriting bits BC0 to BC2, write 0 to this bit simultaneously. (2, 4) The read value is 1.	R/W
b4	—	Nothing is assigned. The write value must be 1. The read value is 1.		—
b5	CPHS	Reserved	Set to 0.	R/W
b6	CPOS_WAIT	Wait insertion bit (5)	0: No wait states (Data and the acknowledge bit are transferred consecutively) 1: Wait states (After the clock of the last data bit falls, a low-level period is extended for two transfer clocks)	R/W
b7	MLS	MSB first/LSB first select bit	0: Data transfer with MSB first (6) 1: Data transfer with LSB first	R/W

Notes:
1. Rewrite between transfer frames. When writing values other than 000b, write when the SCL signal is held low.
2. When writing to bits BC0 to BC2, write 0 to the BC3 bit simultaneously using the MOV instruction. The write value of bits BC0 to BC2 when 1 is written is invalid.
3. After data including the acknowledge bit is transferred, bits BC2 to BC0 are automatically set to 000b. When a start condition is detected, these bits are automatically set to 000b.
4. Do not rewrite this bit in clock synchronous serial mode.
5. The setting value is valid in master mode of I²C bus interface mode. The value is invalid in slave mode of I²C bus interface mode and in clock synchronous serial mode.
6. Set to 0 in I²C bus interface mode.

20.2.8 SI Interrupt Enable Register (SIER)

In the SIER register, the bit functions differ depending on the SSU function and the I^2C bus function.

20.2.8.1 When SSU Function is Used

Address 00169h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	TE_NAKIE	RE_STIE	ACKE	ACKBR	CEIE_ACKBT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CEIE_ACKBT	Conflict error interrupt enable bit	0: Conflict error interrupt request disabled 1: Conflict error interrupt request enabled	R/W
b1	ACKBR	Reserved	The read value is 0.	R
b2	ACKE	Reserved	Set to 0.	R/W
b3	RE_STIE	Receive enable bit (1)	0: Reception disabled 1: Reception enabled	R/W
b4	TE_NAKIE	Transmit enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b5	RIE	Receive interrupt enable bit	0: Receive data full and overrun error interrupt requests disabled 1: Receive data full and overrun error interrupt requests enabled	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Transmit end interrupt request disabled 1: Transmit end interrupt request enabled	R/W
b7	TIE	Transmit interrupt enable bit	0: Transmit data empty interrupt request disabled 1: Transmit data empty interrupt request enabled	R/W

Note:

1. In 4-wire bus (multidirectional) communication mode, do not set both bits TE_NAKIE and RE_STIE to 1. If these bits are set to 1, the RE_STIE is set to 0.

20.2.8.2 When I²C bus Function is Used

Address 00169h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	TE_NAKIE	RE_STIE	ACKE	ACKBR	CEIE_ACKBT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CEIE_ACKBT	Transmit acknowledge select bit	0: In receive mode, 0 is transmitted as the acknowledge bit 1: In receive mode, 1 is transmitted as the acknowledge bit	R/W
b1	ACKBR	Receive acknowledge bit	0: In transmit mode, the acknowledge bit received from the receive device is 0 1: In transmit mode, the acknowledge bit received from the receive device is 1	R
b2	ACKE	Acknowledge bit detection select bit	0: Content of the receive acknowledge bit is ignored and continuous transfer is performed 1: When the receive acknowledge bit is 1, transfer is halted	R/W
b3	RE_STIE	Stop condition detection interrupt enable bit	0: Stop condition detection interrupt request disabled 1: Stop condition detection interrupt request enabled (1)	R/W
b4	TE_NAKIE	NACK receive interrupt enable bit	0: NACK receive interrupt request and arbitration lost/overrun error interrupt request disabled 1: NACK receive interrupt request and arbitration lost/overrun error interrupt request (2)	R/W
b5	RIE	Receive interrupt enable bit	0: Receive data full and overrun error interrupt request disabled 1: Receive data full and overrun error interrupt request enabled (3)	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Transmit end interrupt request disabled 1: Transmit end interrupt request enabled	R/W
b7	TIE	Transmit interrupt enable bit	0: Transmit data empty interrupt request disabled 1: Transmit data empty interrupt request enabled	R/W

Notes:
1. When the STOP bit in the SISR register is 0, set the RE_STIE bit to 1 (stop condition detection interrupt request enabled).
2. Enabling of an overrun error interrupt request by the TE_NAKIE bit is invalid in I²C bus interface mode.
3. An overrun error interrupt request is generated when the clock synchronous serial mode is used.

20.2.9 SI Status Register (SISR)

In the SISR register, the bit functions differ depending on the SSU function and the I^2C bus function.

20.2.9.1 When SSU Function is Used

Address 0016Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	NACKF	STOP	ORER_AL	AAS	CE_ADZ
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CE_ADZ	Conflict error flag (1)	0: No conflict error 1: Conflict error (2)	R/W
b1	AAS	Reserved	Set to 0.	R/W
b2	ORER_AL	Overrun error flag (1)	0: No overrun error 1: Overrun error (3)	R/W
b3	STOP	Reserved	Set to 0.	R/W
b4	NACKF			R/W
b5	RDRF	Receive data register full flag (1, 4)	0: No data in the SIRDR register 1: Data present in the SIRDR register	R/W
b6	TEND	Transmit end flag (1, 5)	0: The TDRE bit is 0 when the last bit of transmit data is transmitted 1: The TDRE bit is 1 when the last bit of transmit data is transmitted	R/W
b7	TDRE	Transmit data empty flag (1, 5, 6)	0: Data is not transferred from registers SITDR to SISDR 1: Data is transferred from registers SITDR to SISDR	R/W

Notes:

1. Writing 1 to bits CE_ADZ, ORER_AL, RDRF, TEND, and TDRE is invalid. To set any of these bits to 0, write 0 after reading it as 1.
2. When starting a serial communication while the MS bit in the SIMR2 register is 1 (4-wire bus communication mode) and the MST bit in the SICR1 register is 1 (master mode), the CE_ADZ bit is set to 1 if the $\overline{SCS}$ pin input is low. See **20.3.3.4 SCS Pin Control and Arbitration**.
   When the $\overline{SCS}$ pin input changes from low to high during transfer while the MS bit in the SIMR2 register is 1 (4-wire bus communication mode) and the MST bit in the SICR1 register is 0 (slave mode), the CE_ADZ bit is set to 1.
3. Indicates an overrun error has occurred during reception and reception is terminated in error. If the next serial data receive operation is completed while the RDRF bit is 1 (data present in the SIRDR register), the ORER_AL bit is set to 1.
   After the ORER_AL bit is set to 1 (overrun error), no reception can be performed while this bit is 1. No transmission can also be performed while the MST bit is 1 (master mode).
4. The RDRF bit is set to 0 when data is read from the SIRDR register. Do not clear this bit by writing 0 in any mode other than I^2C bus interface mode.
5. Bits TEND and TDRE are set to 0 when data is written to the SITDR register.
6. When the SSU function used, the TDRE bit is set to 1 when the TE_NAKIE bit in the SIER register is set to 1 (transmission enabled).

When accessing the SISR register consecutively, insert at least one NOP instruction between the instructions for access.

20.2.9.2 When I²C bus Function is Used

Address 0016Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	NACKF	STOP	ORER_AL	AAS	CE_ADZ
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CE_ADZ	General call address recognition flag (1, 2)	This flag is set to 1 when a general call address is detected.	R/W
b1	AAS	Slave address recognition flag (1)	This flag is set to 1 when the first frame immediately after the start condition matches bits SVA0 to SVA6 in the SIMR2 register in slave receive mode (slave address detection, general call address detection).	R/W
b2	ORER_AL	Arbitration lost flag/overrun error flag (1)	In I²C bus interface mode, this flag indicates that arbitration is lost in master mode. This flag is set to 1 when: (3) • The internal SDA signal and SDA pin level do not match at the rising edge of the SCL signal in master transmit mode • The SDA pin is held high at start condition detection in master transmit/receive mode In clock synchronous serial mode, this bit indicates that an overrun error has occurred. This flag is set to 1 when: • The last bit of the next data is received while the RDRF bit is set to 1.	R/W
b3	STOP	Stop condition detection flag (1, 7)	This flag is set to 1 when a stop condition is detected after the frame is transferred.	R/W
b4	NACKF	No acknowledge detection flag (1, 4)	This flag is set to 1 when no ACKnowledge is detected from the receive device after transmission.	R/W
b5	RDRF	Receive data register full flag (1, 5)	This flag is set to 1 when receive data is transferred from registers SISDR to SIRDR.	R/W
b6	TEND	Transmit end flag (1, 6)	In I²C bus interface mode, this flag is set to 1 at the rising edge of the 9th clock cycle of the SCL signal while the TDRE bit is 1. In clock synchronous mode, this flag is set to 1 when the last bit of the transmit frame is transmitted.	R/W
b7	TDRE	Transmit data empty flag (1, 6)	This flag is set to 1 when: • Data is transferred from registers SITDR to SISDR and the SITDR register becomes empty. • The TRS bit in the SICR1 register is set to 1 (transmit mode) • A start condition is generated (including retransmission) • Slave receive mode is changed to slave transmit mode	R/W

Notes:
1. Each bit is set to 0 by writing 0 after reading it as 1.
2. Enabled in slave receive mode of I²C bus interface mode.
3. When two or more master devices attempt to occupy the bus at nearly the same time, if the I²C bus interface monitors the SDA pin and the data which the I²C bus interface transmits is different, the ORER_AL bit is set to 1 indicating the bus is occupied by another master.
4. The NACKF bit is enabled when the ACKE bit in the SIER register is 1 (when the receive acknowledge bit is 1, transfer is halted).
5. The RDRF bit is set to 0 when data is read from the SIRDR register.
6. Bits TEND and TDRE are set to 0 when data is written to the SITDR register.
7. When 0 is written to the ICE bit in the SICR1 register or 1 is written to the SIRST bit in the SICR2 register while the I²C bus interface is operating, the values of the BBSY bit in the SICR2 register and the STOP bit in the SISR register may be undefined.

   When accessing the SISR register consecutively, insert one or more NOP instructions between the instructions for access.

20.2.10 SI Mode Register 2 (SIMR2)

In the SIMR2 register, the bit functions differ depending on the SSU function and the I^2C bus function.

20.2.10.1 When SSU Function is Used

Address 0016Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BIDE	SCKS	CSS1	CSS0	SCKOS	SOOS	CSOS	MS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MS	Mode select bit (1)	0: Clock synchronous communication mode 1: 4-wire bus communication mode	R/W
b1	CSOS	$\overline{SCS}$ pin open-drain output select bit (6)	0: CMOS output 1: N-channel open-drain output	R/W
b2	SOOS	Serial data open-drain output select bit (1)	0: CMOS output (2) 1: N-channel open-drain output	R/W
b3	SCKOS	SSCK pin open-drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b4	CSS0	$\overline{SCS}$ pin select bits (3)	b5 b4 0 0: Functions as a port 0 1: Functions as the $\overline{SCS}$ input pin 1 0: Functions as the $\overline{SCS}$ output pin (4) 1 1: Functions as the $\overline{SCS}$ output pin (4)	R/W
b5	CSS1			R/W
b6	SCKS	SSCK pin select bit	0: Functions as a port 1: Functions as the serial clock pin	R/W
b7	BIDE	Bidirectional mode enable bit (1, 5)	0: Standard mode (communication using two pins for data input and data output) 1: Bidirectional mode (communication using one pin for data input and data output)	R/W

Notes:
1. See **20.3.1.3 Association between Data I/O Pins and SS Shift Register** for information on combinations of data I/O pins.
2. When the SOOS bit is 0 (CMOS output), set the port direction register bits corresponding to pins SSI and SSO to 0 (input mode).
3. When the MS bit is 0 (clock synchronous communication mode), the $\overline{SCS}$ pin functions as a port regardless of the content of bits CSS0 and CSS1.
4. This bit functions as the $\overline{SCS}$ input pin before transfer starts.
5. The BIDE bit is disabled when the MS bit is 0 (clock synchronous communication mode).
6. When using 4-wire bus communication mode, use the $\overline{SCS}$ pin as N-channel open-drain.

20.2.10.2 When I²C bus Function is Used

Address 0016Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	MS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	MS	Mode select bit	0: I²C bus interface mode 1: Clock synchronous serial mode	R/W
b1	SVA0	Slave addresses (1)	Set an address different from that of the other slave devices connected to the I²C bus. When the higher 7 bits of the first frame transmitted after the start condition match bits SVA0 to SVA6 in slave mode of I²C bus interface mode, the MCU operates as a slave device.	R/W
b2	SVA1			R/W
b3	SVA2			R/W
b4	SVA3			R/W
b5	SVA4			R/W
b6	SVA5			R/W
b7	SVA6			R/W

Note:
1. Do not set to 1111XXXb and 0000XXXb as slave addresses.

20.3 Synchronous Serial Communication Unit (SSU) Operation

20.3.1 Items Common to Clock Synchronous Communication Mode and 4-Wire Bus Communication Mode

20.3.1.1 Transfer Clock

The transfer clock can be selected from among seven internal clocks (f1/256, f1/128, f1/64, f1/32, f1/16, f1/8, and f1/4) and an external clock.

To use the synchronous serial communication unit, set the SCKS bit in the SIMR2 register to 1 and then select the SSCK pin as the serial clock pin.

When the MST bit in the SICR1 register is 1 (master mode), an internal clock is selected and the SSCK pin functions as output. When transfer is started, the SSCK pin outputs a clock of the transfer rate selected by bits CKS0 to CKS2 in the SICR1 register.

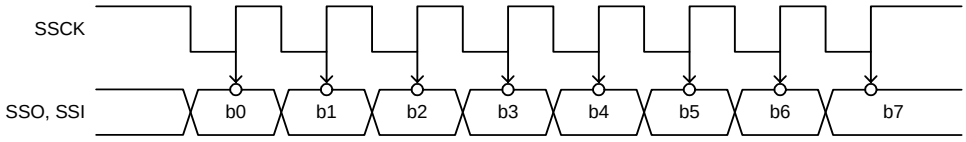
When the MST bit in the SICR1 register is 0 (slave mode), an external clock is selected and the SSCK pin functions as input.

20.3.1.2 Association between Transfer Clock Polarity, Phase, and Data

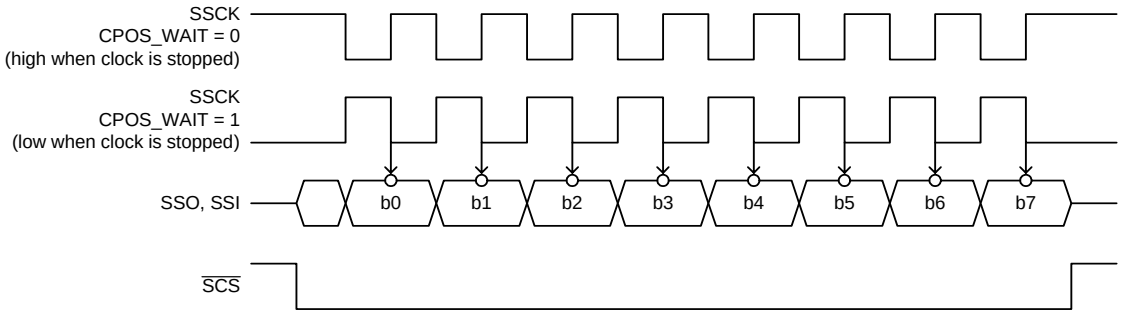
The association between the transfer clock polarity, phase and data changes according to the combinations of the MS bit in the SIMR2 register and bits CPHS and CPOS_WAIT in the SIMR1 register. Figure 20.4 shows the Association between Transfer Clock Polarity, Phase, and Transfer Data.

Also, the MSB-first transfer or LSB-first transfer can be selected by setting the MLS bit in the SIMR1 register. When the MLS bit is 1, transfer is started from the LSB and proceeds to the MSB. When the MLS bit is 0, transfer is started from the MSB and proceeds to the LSB.

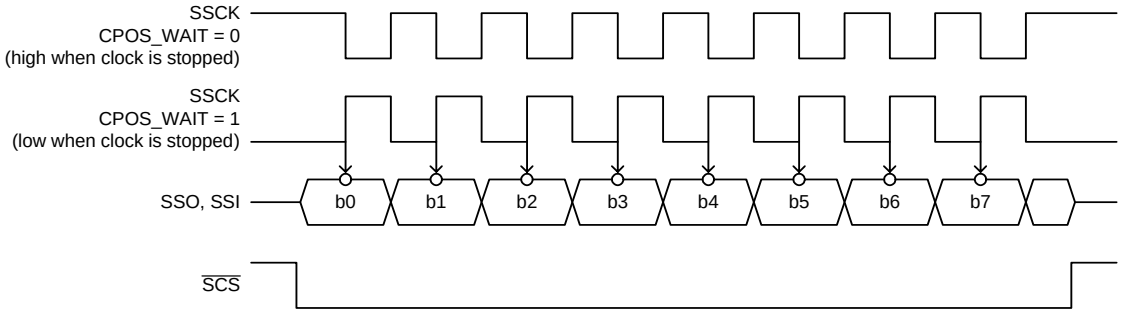
• MS = 0 (clock synchronous communication mode), CPHS = 0 (data change at odd edge), CPOS_WAIT = 0 (high when clock is stopped), and MLS = 1 (LSB-first transfer)



• MS = 1 (4-wire bus communication mode), CPHS = 0 (data change at odd edge), and MLS = 1 (LSB-first transfer)



• MS = 1 (4-wire bus communication mode), CPHS = 1 (data download at odd edge), and MLS = 1 (LSB-first transfer)



CPHS, CPOS_WAIT, MLS: Bits in SIMR1 register
MS: Bit in SIMR2 register

Figure 20.4 Association between Transfer Clock Polarity, Phase, and Transfer Data

20.3.1.3 Association between Data I/O Pins and SS Shift Register

The connection between the data I/O pins and the SISDR register changes according to the combinations of the MST bit in the SICR1 register and the MS bit in the SIMR2 register. The connection also changes according to the BIDE bit in the SIMR2 register. Figure 20.5 shows the Association between Data I/O Pins and SISDR Register.

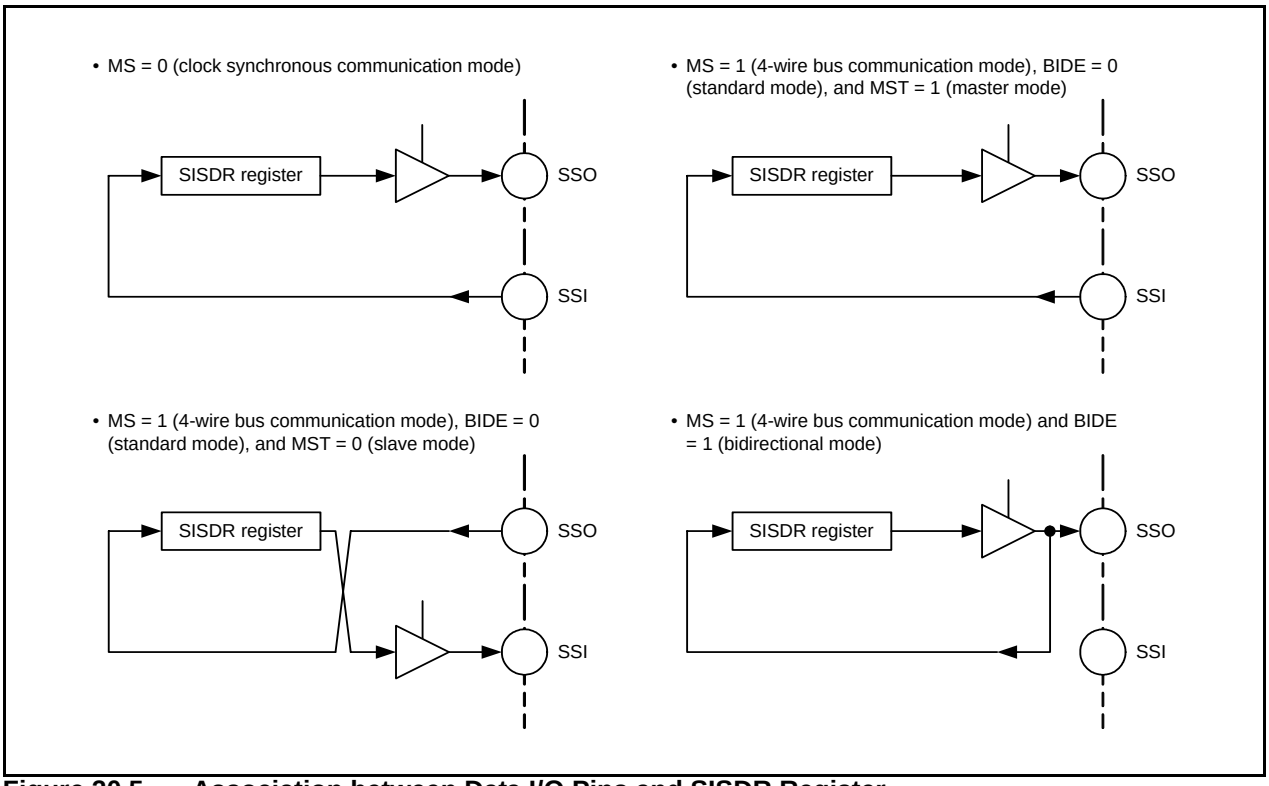


Figure 20.5 Association between Data I/O Pins and SISDR Register

20.3.1.4 Interrupt Requests

The synchronous serial communication unit has five interrupt requests: transmit data empty, transmit end, receive data full, overrun error, and conflict error. Because these interrupt requests are assigned to the synchronous serial communication unit interrupt vector table, interrupt sources must be determined using flags. Table 20.7 lists the Interrupt Requests of Synchronous Serial Communication Unit.

Table 20.7 Interrupt Requests of Synchronous Serial Communication Unit

Interrupt Request	Abbreviation	Generation Condition
Transmit data empty	TXI	TIE = 1 and TDRE = 1
Transmit end	TEI	TEIE = 1 and TEND = 1
Receive data full	RXI	RIE = 1 and RDRF = 1
Overrun error	OEI	RIE = 1 and ORER_AL = 1
Conflict error	CEI	CEIE_ACKBT = 1 and CE_ADZ = 1 (1)

CEIE_ACKBT, RIE, TEIE, TIE: Bits in SIER register
CE_ADZ, ER_AL, RDRF, TEND, TDRE: Bits in SISR register
Note:
1. Not generated in clock synchronous communication mode.

If the generation conditions in Table 20.7 are met, a synchronous serial communication unit interrupt request is generated. Set each interrupt source to 0 by the synchronous serial communication unit interrupt routine.
Note that bits TDRE and TEND in the SISR register are automatically set to 0 by writing transmit data to the SITDR register and the RDRF bit in the SISR register is automatically set to 0 by reading the SIRDR register. In particular, the TDRE bit is set back to 1 (data is transferred from registers SITDR to SISDR) at the same time transmit data is written to the SITDR register. If the TDRE bit is set to 0 (data is not transferred from registers SITDR to SISDR) by any method other than the above (register access by software), additional 1 byte of transferred data may be transmitted.

20.3.1.5 Communication Modes and Pin Functions

The synchronous serial communication unit switches the functions of the I/O pins in each communication mode according to the settings of the MST bit in the SICR1 register and bits RE_STIE and TE_NAKIE in the SIER register. Table 20.8 lists the Association between Communication Modes and I/O Pins.

Table 20.8 Association between Communication Modes and I/O Pins

Communication Mode	Bit Setting					Pin State		
	MS	BIDE	MST	TE_NAKIE	RE_STIE	SSI	SSO	SSCK
Clock synchronous communication mode	0	Disabled	0	0	1	Input	—	Input
				1	0	—	Output	Input
					1	Input	Output	Input
			1	0	1	Input	—	Output
				1	0	—	Output	Output
					1	Input	Output	Output
4-wire bus communication mode	1	0	0	0	1	—	Input	Input
				1	0	Output	—	Input
					1	Output	Input	Input
			1	0	1	Input	—	Output
				1	0	—	Output	Output
					1	Input	Output	Output
4-wire bus (bidirectional) communication mode (1)	1	1	0	0	1	—	Input	Input
				1	0	—	Output	Input
			1	0	1	—	Input	Output
				1	0	—	Output	Output

—: Used as a programmable I/O port.
MS, BIDE: Bits in SIMR2 register
MST: Bit in SICR1 register
TE_NAKIE, RE_STIE: Bits in SIER register
Note:
1. Do not set both bits TE_NAKIE and RE_STIE to 1 in 4-wire bus (bidirectional) communication mode.

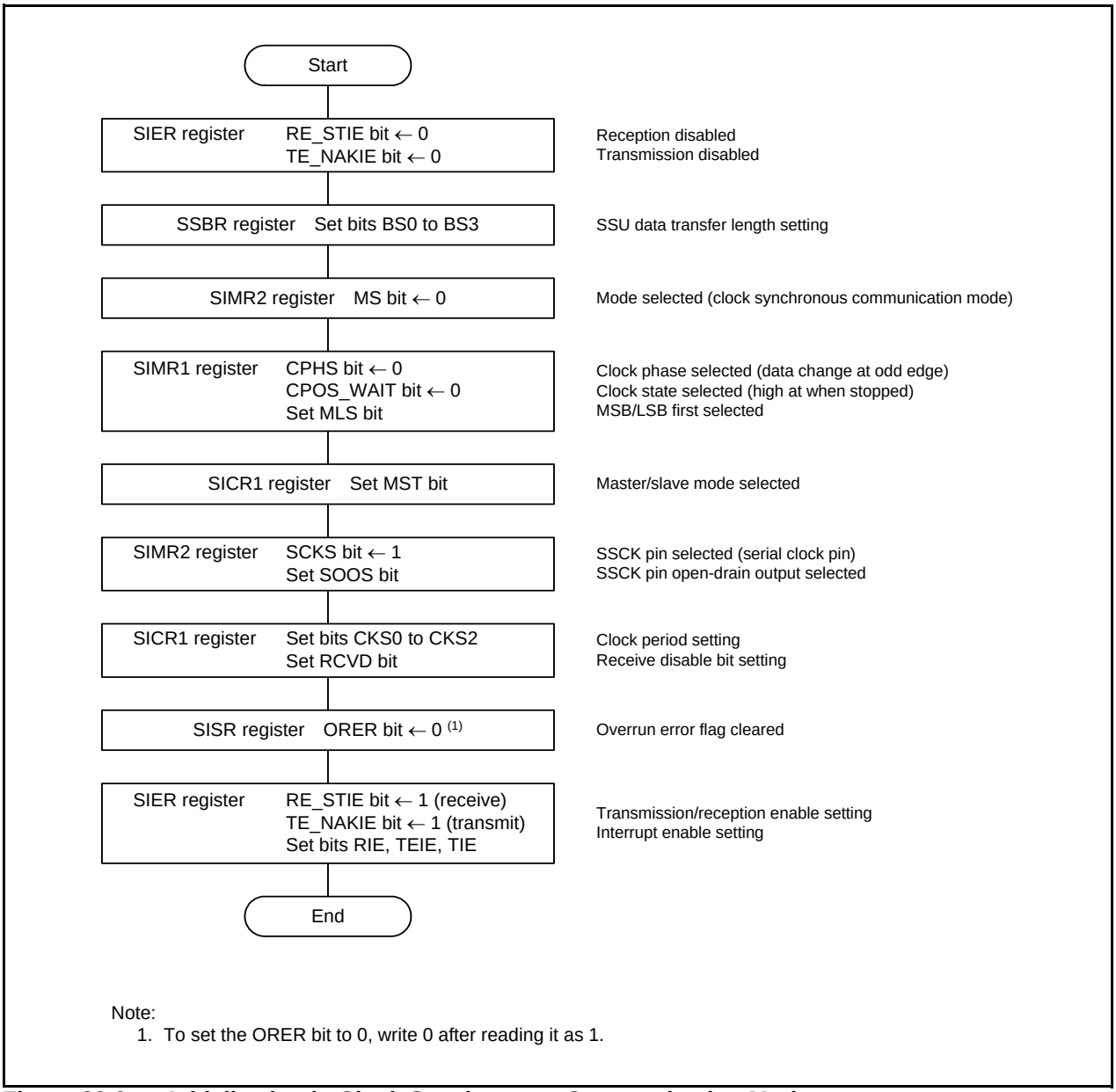
20.3.2 Clock Synchronous Communication Mode

20.3.2.1 Initialization in Clock Synchronous Communication Mode

Figure 20.6 shows the Initialization in Clock Synchronous Communication Mode. Before data transmission or reception, set the TE_NAKIE bit in the SIER register to 0 (transmission disabled) and the RE_ STIE bit to 0 (reception disabled) for initialization.

To change the communication mode (select clock synchronous communication mode by the mode select MS bit in the SIMR2 register) or the communication format, set the TE_NAKIE bit to 0 and the RE_STIE bit to 0 before making the change.

Even if the RE_STIE bit is set to 0, the contents of flags RDRF and ORER_AL and the SIRDR register are retained.



Note:
1. To set the ORER bit to 0, write 0 after reading it as 1.

Figure 20.6 Initialization in Clock Synchronous Communication Mode

20.3.2.2 Data Transmission

Figure 20.7 shows an Operation Example during Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data transmission, the synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)
When the MCU is set as the master device, it outputs a synchronous clock and data. When the MCU is set as a slave device, it outputs data synchronized with the input clock.
When the TE_NAKIE bit is set to 1 (transmission enabled) before writing the transmit data to the SITDR register, the TDRE bit is automatically set to 0 (data is not transferred from registers SITDR to SISDR) and the data is transferred from registers SITDR to SISDR. Then, the TDRE bit is set to 1 (data is transferred from registers SITDR to SISDR) and transmission is started. If the TIE bit in the SIER register is 1 at this time, the TXI interrupt request is generated.
When one frame of data is transferred while the TDRE bit is 0, data is transferred from registers SITDR to SISDR and the next frame transmission is started. If the 8th bit is transmitted while the TDRE bit is 1, the TEND bit in the SISR register is set to 1 (the TDRE bit is 1 when the last bit of transmit data is transmitted) and the state is retained. If the TEIE bit in the SIER register is 1 (transmit end interrupt request enabled) at this time, the TEI interrupt request is generated. The SSCK pin is fixed at high after transmission is completed.
Transmission cannot be performed while the ORER_AL bit in the SISR register is 1 (overrun error). Confirm that the ORER_AL bit is 0 before transmission.
Figure 20.8 shows a Sample Flowchart for Data Transmission (Clock Synchronous Communication Mode).

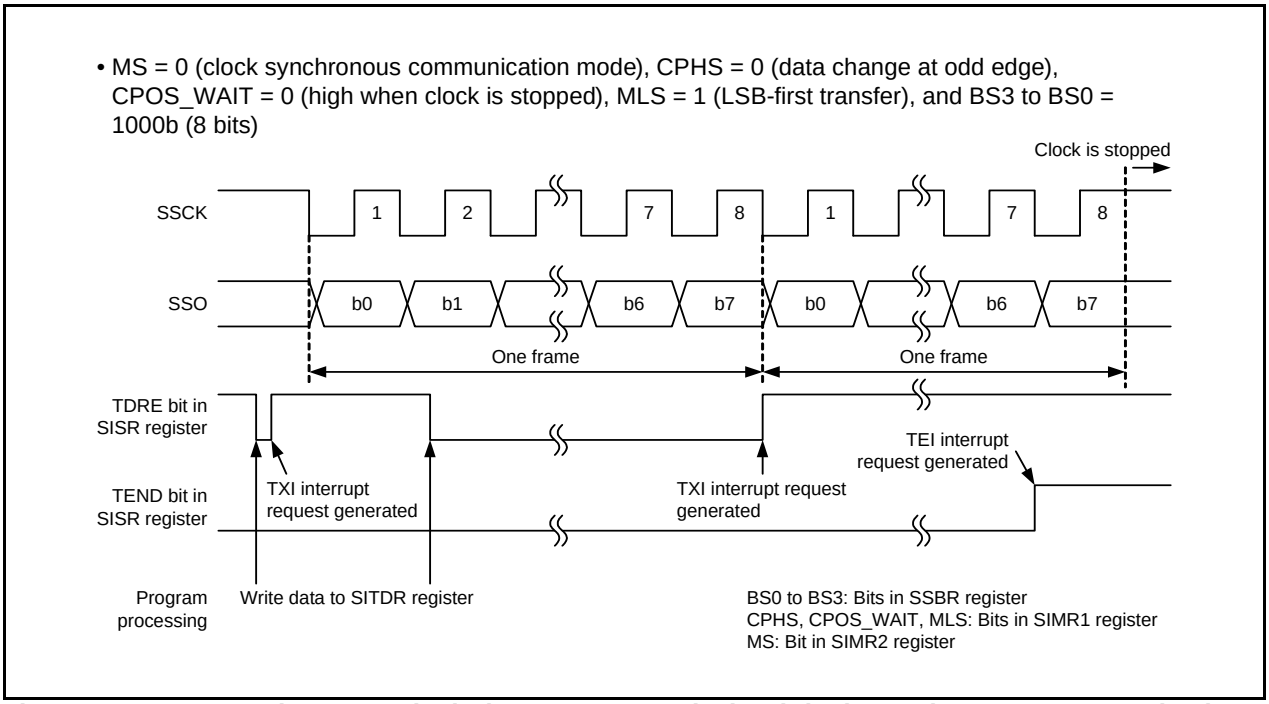


Figure 20.7 Operation Example during Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)

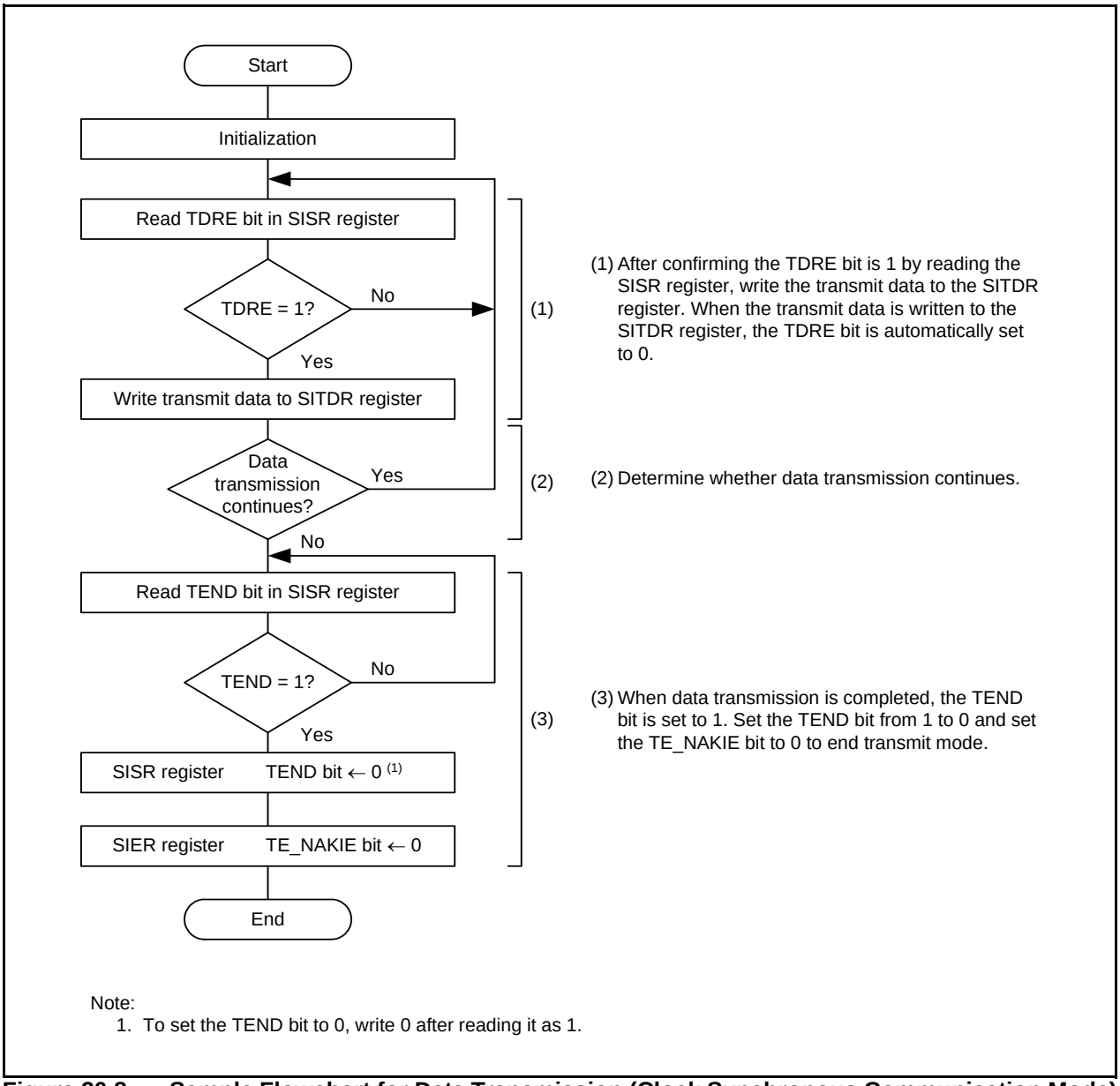


Figure 20.8 Sample Flowchart for Data Transmission (Clock Synchronous Communication Mode)

20.3.2.3 Data Reception

Figure 20.9 shows an Operation Example during Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, the synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)
When the MCU is set as the master device, it outputs a synchronous clock and inputs data. When the MCU is set as a slave device, it inputs data synchronized with the input clock.
When the MCU is set as the master device, it outputs a receive clock and reception is started by performing a dummy read of the SIRDR register.
After 8 bits of data are received, the RDRF bit in the SISR register is set to 1 (data present in the SIRDR register) and receive data is stored in the SIRDR register. If the RIE bit in the SIER register is 1 (RXI and OEI interrupt requests enabled) at this time, the RXI interrupt request is generated. When the SIRDR register is read, the RDRF bit is automatically set to 0 (no data in the SIRDR register).
When setting the MCU as the master device to complete reception, set the RCVD bit in the SICR1 register to 1 (receive operation is completed after 1 byte of data is received) and then read the received data. The synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE_STIE bit in the SIER register to 0 (reception disabled) and the RCVD bit to 0 (receive operation continues after the 1 byte of data is received), and then read the last received data from the SIRDR register. If the SIRDR register is read while the RE_STIE bit is 1 (reception enabled), a receive clock is output again.
When the 8th clock rises while the RDRF bit is 1, the ORER_AL bit in the SISR register is set to 1 (overrun error: OEI) and the operation is stopped. While the ORER_AL bit is 1, reception cannot be performed. Confirm that the ORER_AL bit is 0 before restarting reception. If an overrun error occurs, the data received in the frame where the error has occurred is discarded.
Figure 20.10 shows a Sample Flowchart for Data Reception (MST = 1) (Clock Synchronous Communication Mode).

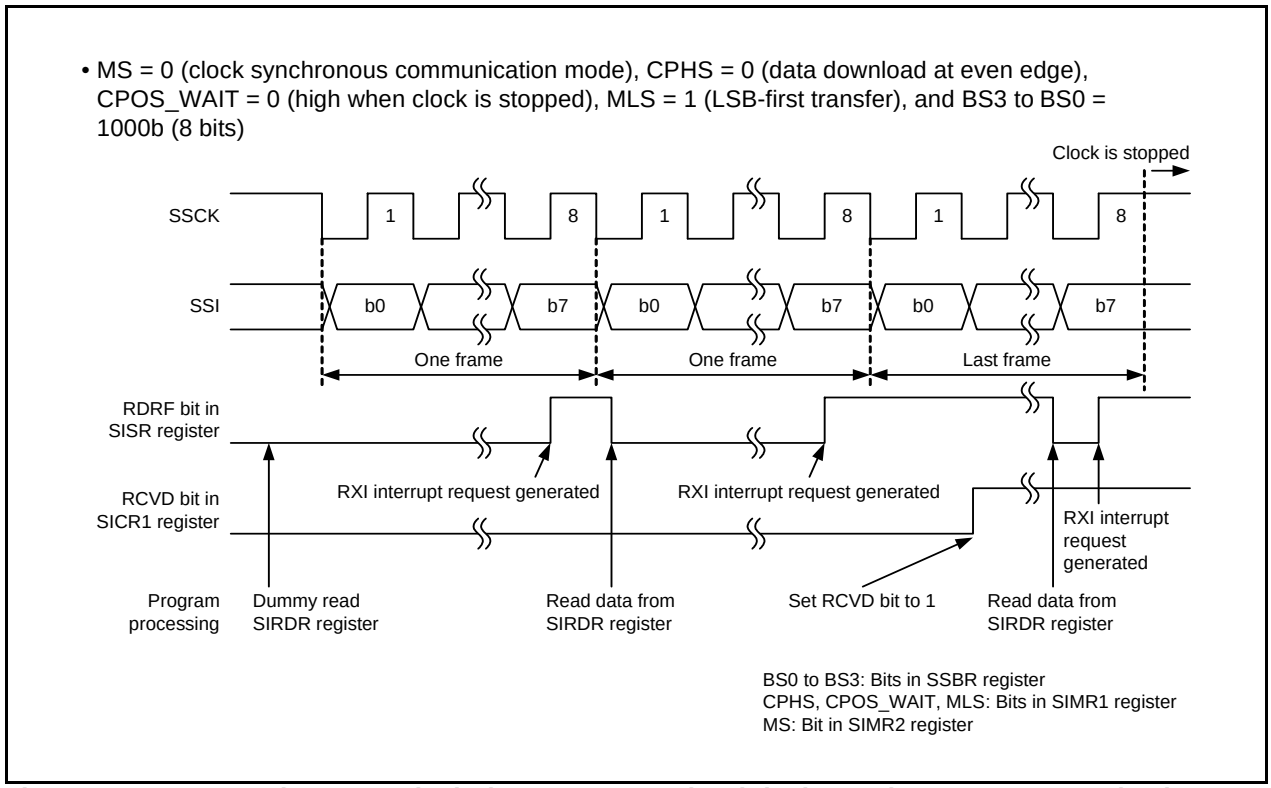


Figure 20.9 Operation Example during Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)

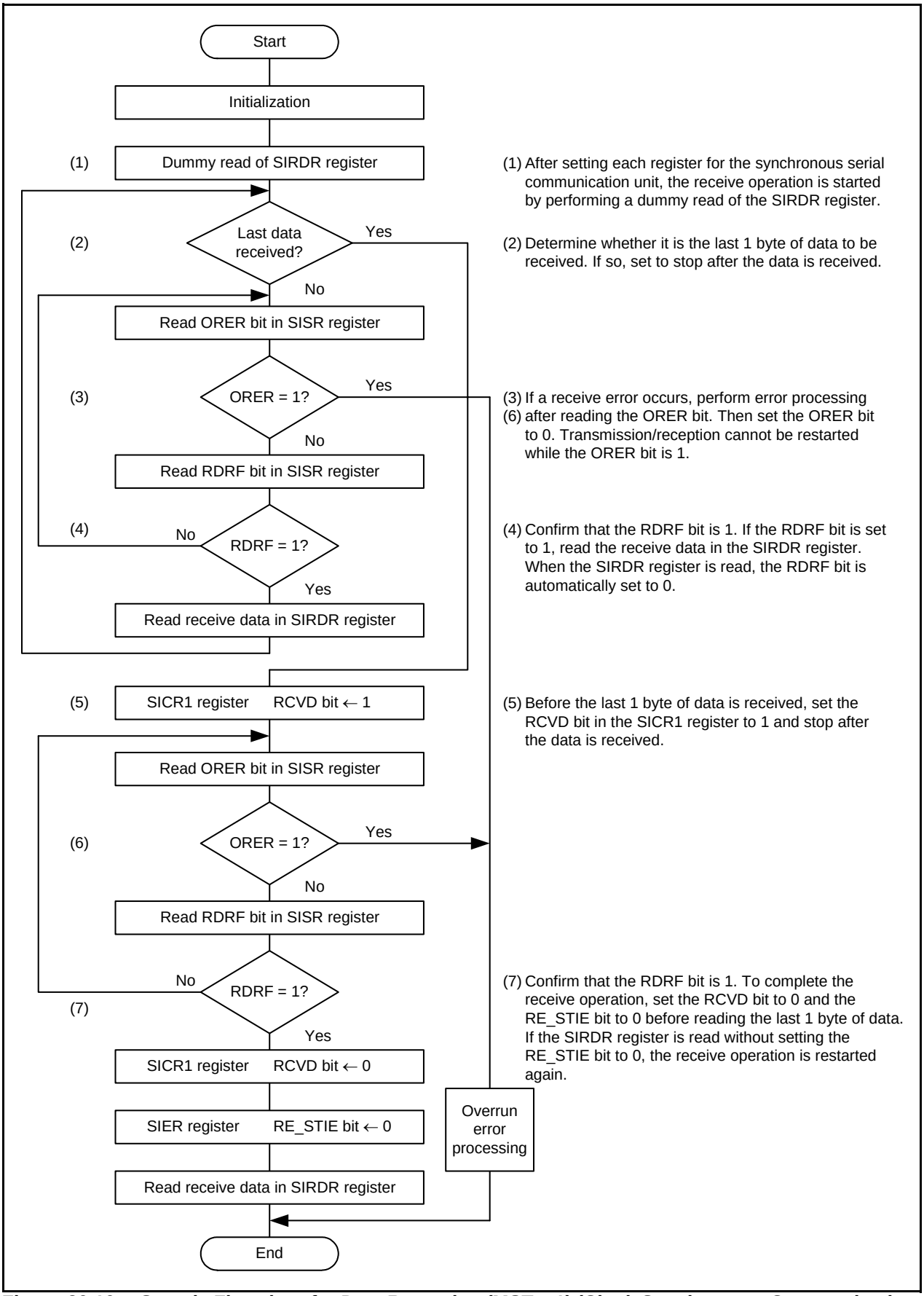


Figure 20.10 Sample Flowchart for Data Reception (MST = 1) (Clock Synchronous Communication Mode)

20.3.2.4 Data Transmission/Reception

Figure 20.11 shows an Operation Example during Data Transmission/Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length).

Data transmission/reception is an operation combining data transmission and reception which were described earlier.

Transmission/reception is started by writing data to the SITDR register. While the TDRE bit is 1 (data is transferred from registers SITDR to SISDR), if the last transfer clock (the data transfer length can be set from 8 to 16 bits using the SSBR register) rises or the ORER_AL bit is set to 1 (overrun error), the transmit/receive operation is stopped.

When switching from transmit mode (TE_NAKIE = 1) or receive mode (RE_STIE = 1) to transmit/receive mode (TE_NAKIE = RE_STIE = 1), set the TE_NAKIE bit to 0 and RE_STIE bit to 0 once before making the change. After confirming the TEND bit is 0 (the TDRE bit is 0 when the last bit of transmit data is transmitted), the RDRF bit is 0 (no data in the SIRDR register), and the ORER_AL bit is 0 (no overrun error), set bits TE_NAKIE and RE_STIE to 1.

Figure 20.12 shows a Sample Flowchart for Data Transmission/Reception (Clock Synchronous Communication Mode).

When cancelling transmit/receive mode after this mode is used (TE_NAKIE = RE_STIE = 1), a clock may be output if transmit/receive mode is cancelled after reading the SIRDR register. To avoid any clock outputs, use either of the following procedures:

- First set the RE_STIE bit to 0, and then set the TE_NAKIE bit to 0.
- Set bits TE_NAKIE and RE_STIE to 0 at the same time.

When switching to receive mode (TE_NAKIE = 0 and RE_STIE = 1) after that, write 1 to the SRES bit and then set this bit to 0 to initialize the SSU control block and the SISDR register before setting the RE_STIE bit to 1.

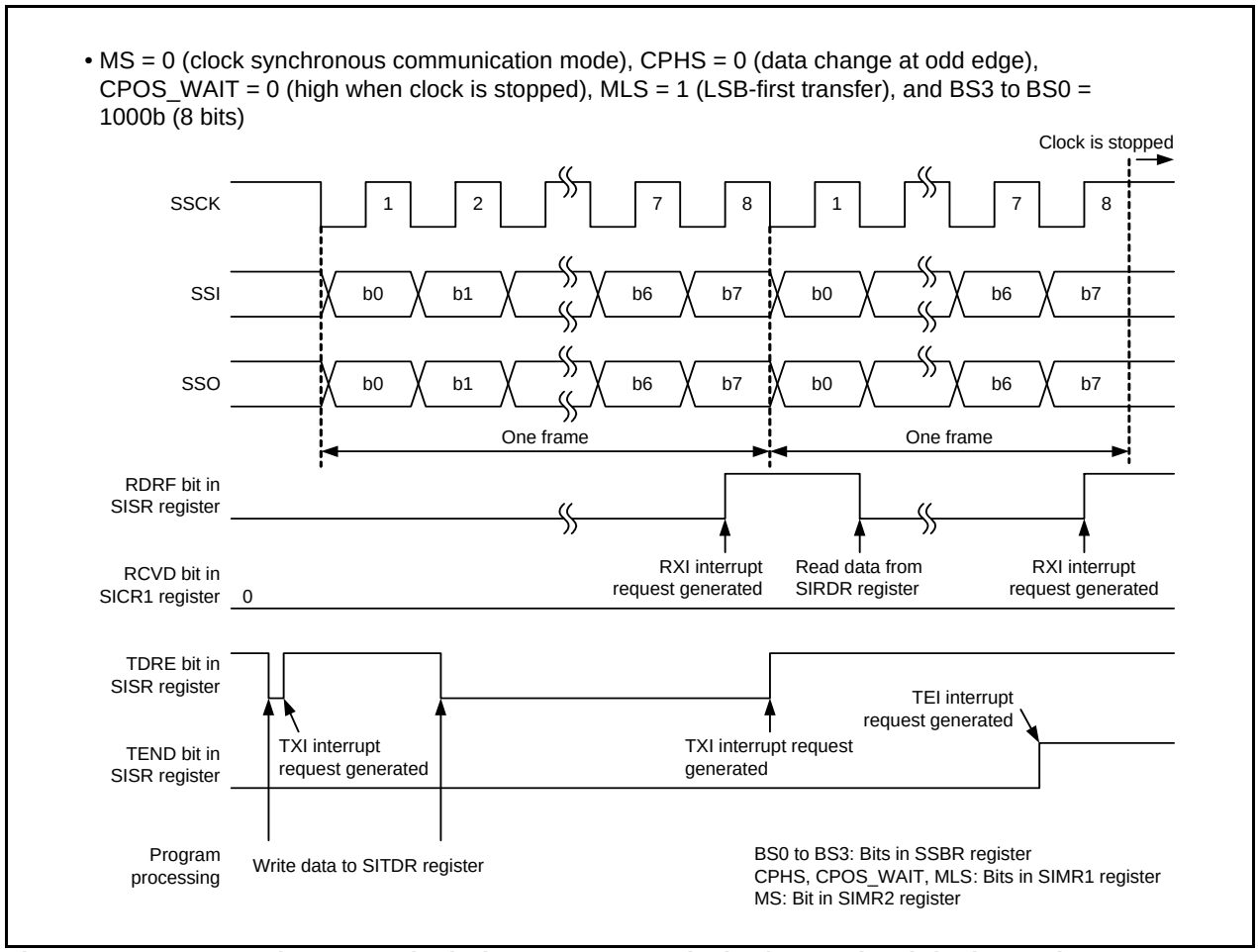
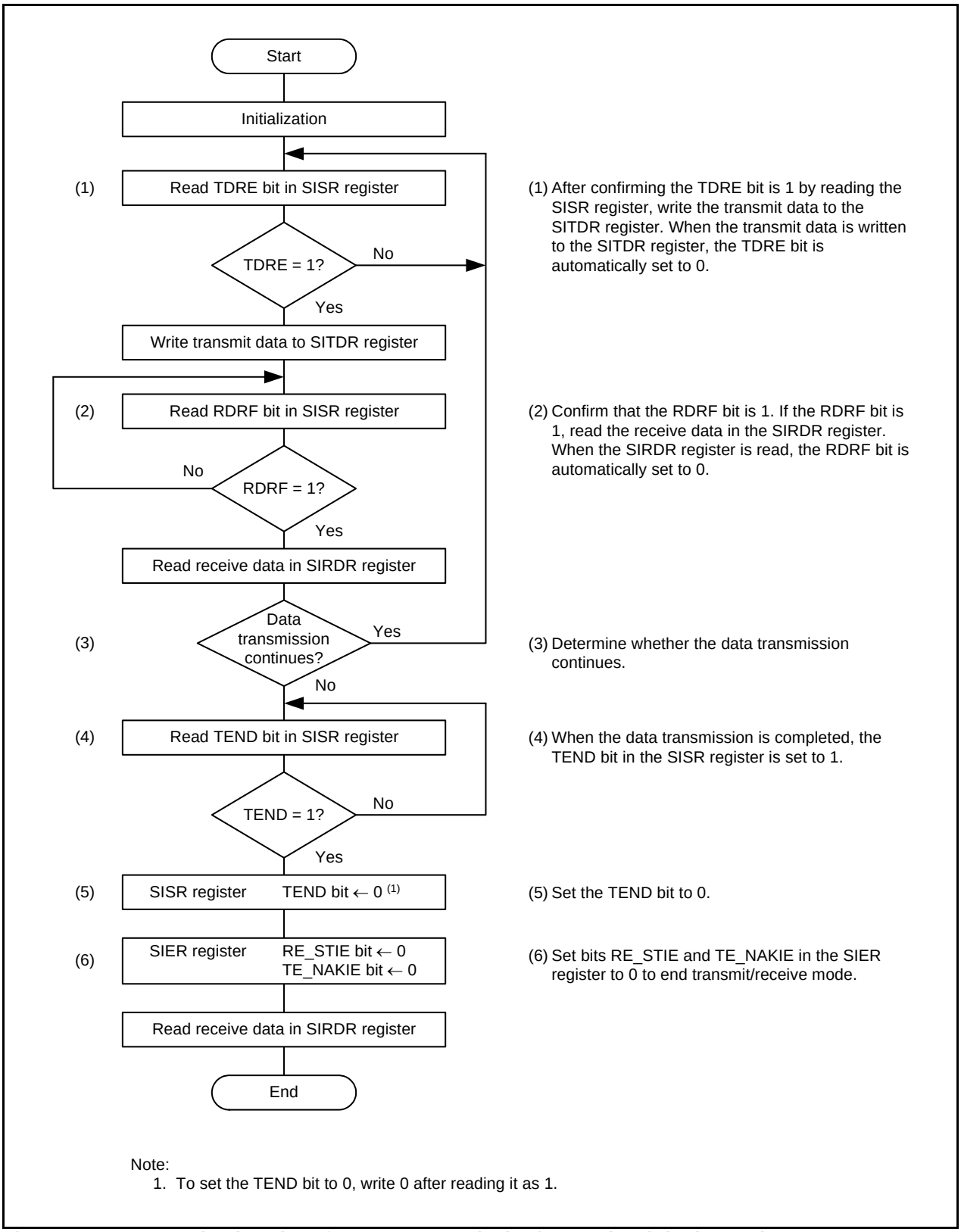


Figure 20.11 Operation Example during Data Transmission/Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)



Note:
1. To set the TEND bit to 0, write 0 after reading it as 1.

Figure 20.12 Sample Flowchart for Data Transmission/Reception (Clock Synchronous Communication Mode)

20.3.3 4-Wire Bus Communication Mode

In 4-wire bus communication mode, a 4-wire bus consisting of a clock line, a data input line, a data output line, and a chip select line is used for communication. This mode includes bidirectional mode in which the data input line and data output line function as a single pin.

The data input line and output line change according to the settings of the MST bit in the SICR1 register and the BIDE bit in the SIMR2 register. For details, see **20.3.1.3 Association between Data I/O Pins and SS Shift Register**. In this mode, the association between clock polarity, phase, and data are set using bits CPOS_WAIT and CPHS in the SIMR1 register. For details, see **20.3.1.2 Association between Transfer Clock Polarity, Phase, and Data**.

The chip select line controls output for the master device, and it controls input for the slave device. For the master device, the chip select line controls output of the $\overline{SCS}$ pin or controls output of an I/O port when the CSS1 bit in the SIMR2 register is set to 1. For the slave device, the chip select line sets the $\overline{SCS}$ pin to function as an input pin when bits CSS1 and CSS0 in the SIMR2 register are set to 01b.

In 4-wire bus communication mode, the MLS bit in the SIMR1 register is set to 0 and communication is performed with MSB first.

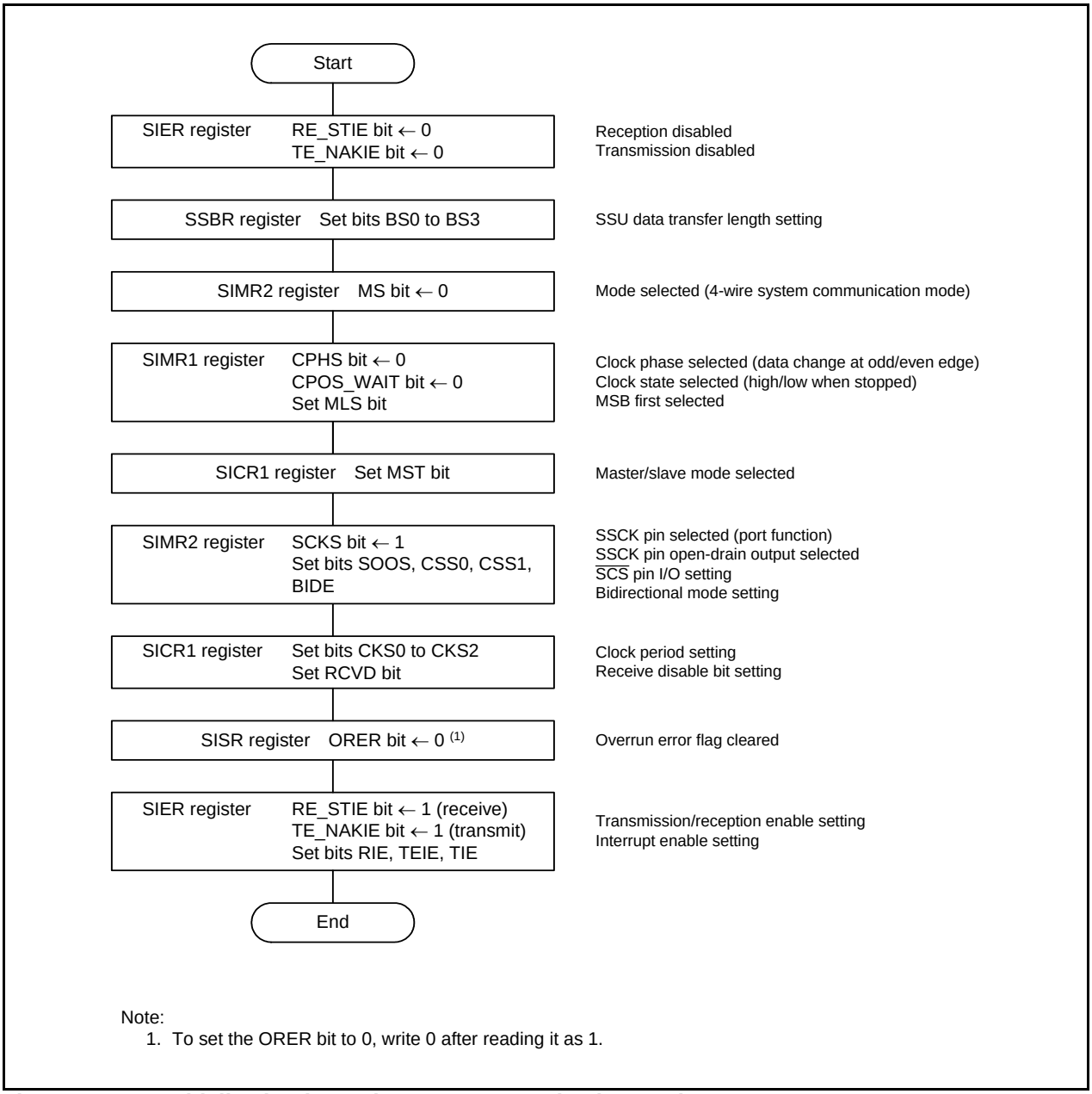
20.3.3.1 Initialization in 4-Wire Bus Communication Mode

Figure 20.13 shows the Initialization in 4-Wire Bus Communication Mode. Before data transmission/reception, set the TE_NAKIE bit in the SIER register to 0 (transmission disabled), the RE_STIE bit 0 (reception disabled) for initialization.

To change the communication mode or the communication format, set the TE_NAKIE bit to 0 and the RE_STIE bit to 0 before making the change.

Even if the RE_STIE bit is set to 0, the contents of flags RDRF and ORER_AL and the SIRDR register are retained.

After data is received in slave mode, when the mode is switched to master mode, the $\overline{SCS}$ pin may be set to low even if no transfer start condition is written.



Note:
1. To set the ORER bit to 0, write 0 after reading it as 1.

Figure 20.13 Initialization in 4-Wire Bus Communication Mode

20.3.3.2 Data Transmission

Figure 20.14 shows an Operation Example during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During data transmission, the synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)

When the MCU is set as the master device, it outputs a synchronous clock and data. When the MCU is set as a slave device, it outputs data synchronized with the input clock while the $\overline{SCS}$ pin input is held low.

When the transmit data is written to the SITDR register after setting the TE_NAKIE bit to 1 (transmission enabled), the TDRE bit is automatically set to 0 (data is not transferred from registers SITDR to SISDR) and the data is transferred from registers SITDR to SISDR. After that, the TDRE bit is set to 1 (data is transferred from registers SITDR to SISDR) and transmission is started. If the TIE bit in the SIER register is 1 at this time, the TXI interrupt request is generated.

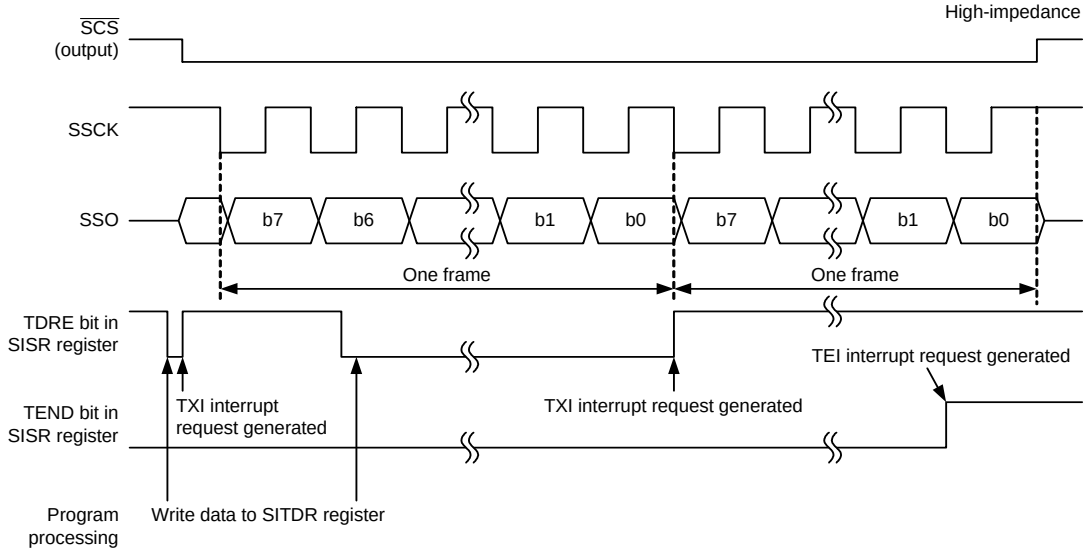
After one frame of data is transferred while the TDRE bit is 0, the data is transferred from registers SITDR to SISDR and the next frame transmission is started. If the 8th bit is transmitted while TDRE is 1, the TEND bit in the SISR register is set to 1 (the TDRE bit is 1 when the last bit of transmit data is transmitted) and the state is retained. If the TEIE bit in the SIER register is 1 (transmit end interrupt request enabled) at this time, the TEI interrupt request is generated. After transmission is completed, the SSCK pin is fixed at high and the $\overline{SCS}$ pin is set to high. To perform transmission continuously while the $\overline{SCS}$ pin is held low, write the next transmit data to the SITDR register before transmitting the 8th bit.

Transmission cannot be performed while the ORER_AL bit in the SISR register is 1 (overrun error). Confirm that the ORER_AL bit is 0 before transmission.

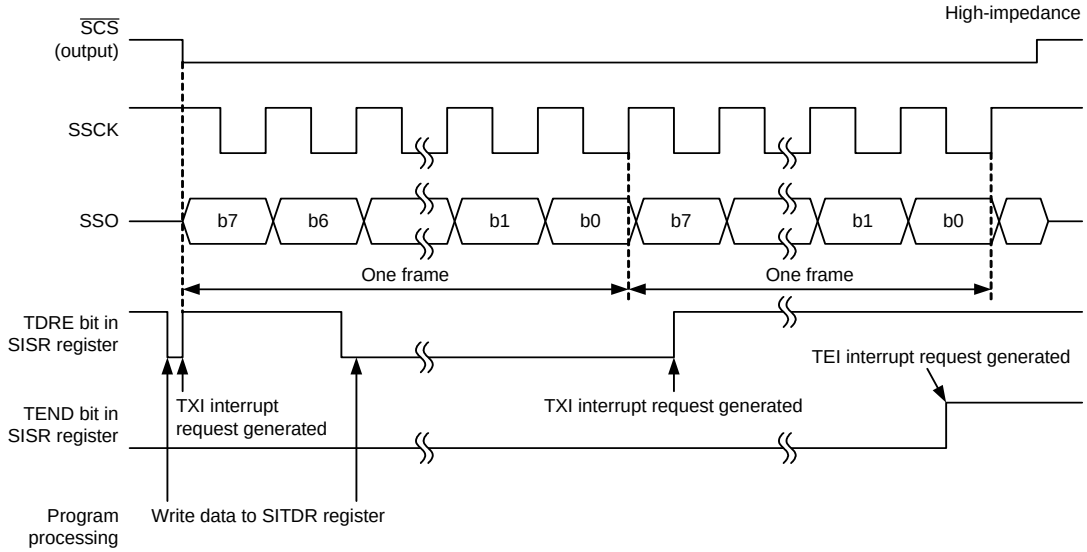
In contrast to the clock synchronous communication mode, the SSO pin becomes the high-impedance state while the $\overline{SCS}$ pin is in the high-impedance state in master device operation, and the SSI pin becomes the high-impedance state while the $\overline{SCS}$ pin input is held high in slave device operation.

The sample flowchart is the same as that for the clock synchronous communication mode (see **Figure 20.8 Sample Flowchart for Data Transmission (Clock Synchronous Communication Mode)**).

• CPHS = 0 (data change at odd edge), CPOS_WAIT = 0 (high when clock is stopped), MLS = 0 (MSB-first transfer), and BS3 to BS0 = 1000b (8 bits)



• CPHS = 1 (data change at even edge), CPOS_WAIT = 0 (high when clock is stopped), MLS = 0 (MSB-first transfer), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS, CPOS_WAIT, MLS: Bits in SIMR1 register

Figure 20.14 Operation Example during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

20.3.3.3 Data Reception

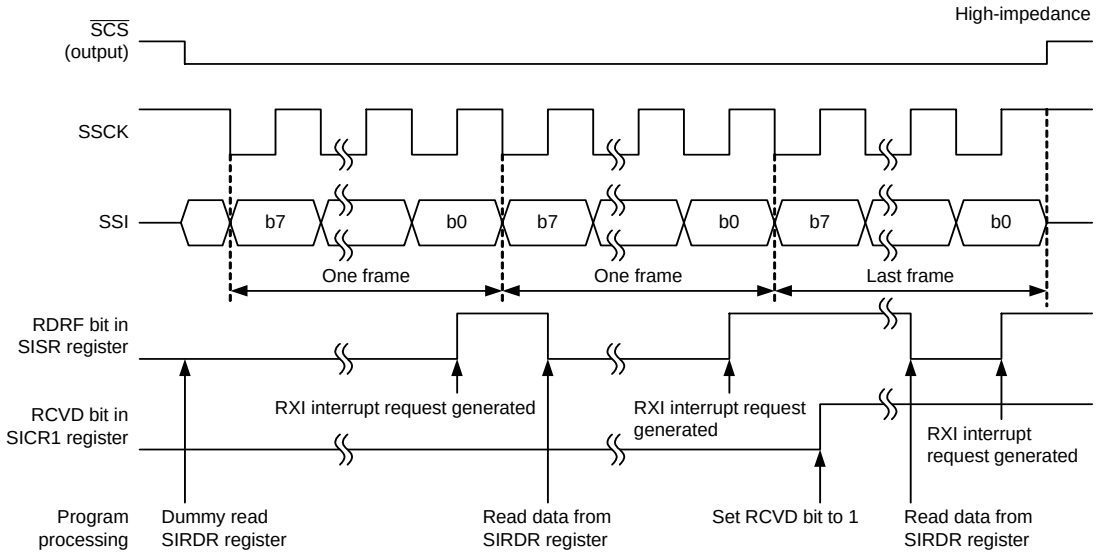
Figure 20.15 shows an Operation Example during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, the synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)
When the MCU is set as the master device, it outputs a synchronous clock and inputs data. When the MCU is set as a slave device, it outputs data synchronized with the input clock while the $\overline{SCS}$ pin input is held low.
When the MCU is set as the master device, it outputs a receive clock and reception is started by performing a dummy read of the SIRDR register.
After 8 bits of data are received, the RDRF bit in the SISR register is set to 1 (data present in the SIRDR register) and receive data is stored in the SIRDR register. If the RIE bit in the SIER register is 1 (RXI and OEI interrupt requests enabled) at this time, the RXI interrupt request is generated. When the SIRDR register is read, the RDRF bit is automatically set to 0 (no data in the SIRDR register).
When setting the MCU as the master device to complete reception, set the RCVD bit in the SICR1 register to 1 (receive operation is completed after 1-byte data is received) and then read the receive data. The synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE_STIE bit in the SIER register to 0 (reception disabled) and the RCVD bit to 0 (receive operation continues after 1-byte data is received), and then read the receive data. When the SIRDR register is read while the RE_STIE bit is set to 1 (receive enabled), a receive clock is output again.
When the 8th clock rises while the RDRF bit is 1, the ORER_AL bit in the SISR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER_AL bit is 1, reception cannot be performed. Confirm that the ORER_AL bit is 0 before restarting reception.
The timing with which bits RDRF and ORER_AL are set to 1 varies depending on the setting of the CPHS bit in the SIMR1 register. Figure 19.15 shows this timing. If the CPHS bit is set to 1 (data download at odd edge), care must be taken when reception is completed because these bits are set to 1 at some point during the frame.
The sample flowchart is the same as that for the clock synchronous communication mode (see **Figure 20.10 Sample Flowchart for Data Reception (MST = 1) (Clock Synchronous Communication Mode)**).

[Notes on when an overrun error occurs]
After an overrun error occurs, use the following procedure to cancel the overrun error:

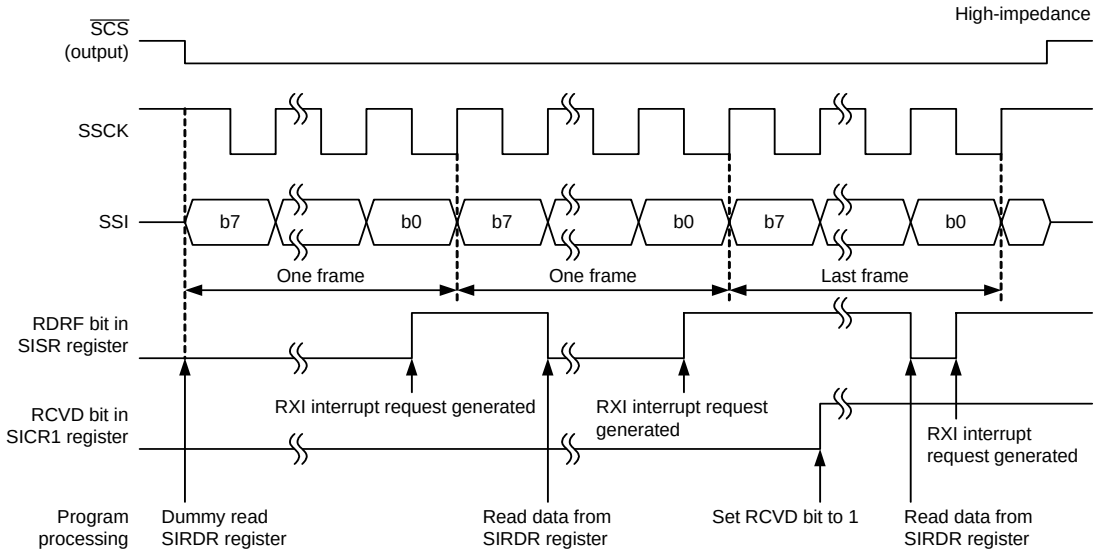
• In master mode
(1) Complete the transfer operation (confirm that the $\overline{SCS}$ pin becomes high impedance).
(2) Read the last received data (data before an overrun error occurs).
(3) Set the ORER_AL bit to 0.

• In slave mode
(1) Complete the transfer operation (confirm that a conflict error).
(2) Read the last received data (data before an overrun error occurs).
(3) Set bits CE_ADZ and ORER_AL to 0.

• CPHS = 0 (data download at even edge), CPOS_WAIT = 0 (high when clock is stopped), MLS = 0 (MSB-first transfer), and BS3 to BS0 = 1000b (8 bits)



• CPHS = 1 (data download at odd edge), CPOS_WAIT = 0 (high when clock is stopped), MLS = 0 (MSB-first transfer), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS, CPOS_WAIT, MLS: Bits in SIMR1 register

Figure 20.15 Operation Example during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

20.3.3.4 $\overline{\text{SCS}}$ Pin Control and Arbitration

When the MS bit in the SIMR2 register is set to 1 (4-wire bus communication mode) and the CSS1 bit is set to 1 (functions as the $\overline{\text{SCS}}$ output pin), set the MST bit in the SICR1 register to 1 (master mode) and check the arbitration of the $\overline{\text{SCS}}$ pin before starting serial transfer. If the synchronous serial communication unit detects that the synchronized internal $\overline{\text{SCS}}$ signal is held low in this period, the CE_ADZ bit in the SISR register is set to 1 (conflict error) and the MST bit is automatically set to 0 (slave mode).
Figure 20.16 shows the Arbitration Check Timing.

Future transmit operations are not performed while the CE_ADZ bit is 1. Set the CE_ADZ bit to 0 (no conflict error) before starting transmission.

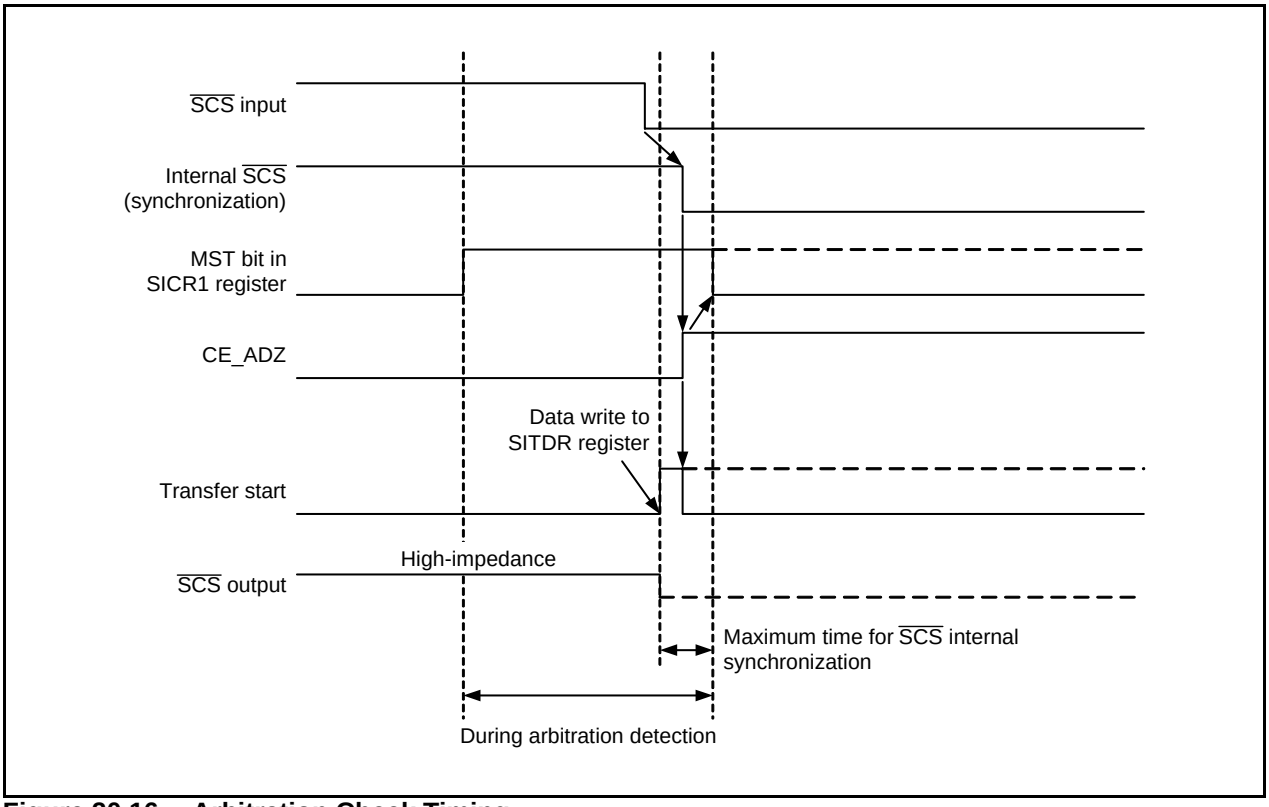


Figure 20.16 Arbitration Check Timing

20.4 I²C bus Interface Operation

20.4.1 Items Common to I²C bus Interface and Clock Synchronous Serial Mode

20.4.1.1 Transfer Clock

When the MST bit in the SICR1 register is 0, the transfer clock is the external clock input from the SCL pin. When the MST bit in the SICR1 register is 1, the transfer clock is the internal clock selected by bits CKS0 to CKS3 in the SICR1 register and bits IICTCTWI and IICTCHALF in the IICCR register, and the transfer clock is output from the SCL pin. Tables 20.9 and 20.10 list the Transfer Rate Examples.

Table 20.9 Transfer Rate Examples (1)

IICCR Register		SICR1 Register				Transfer Clock	Transfer Rate				
IICTCHALF	IICTCTWI	CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	0	0	0	0	0	f1/28	179 kHz	286 kHz	357 kHz	571 kHz	714 kHz
					1	f1/40	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
				1	0	f1/48	104 kHz	167 kHz	208 kHz	333 kHz	417 kHz
					1	f1/64	78.1 kHz	125 kHz	156 kHz	250 kHz	313 kHz
			1	0	0	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
					1	f1/100	50.0 kHz	80.0 kHz	100 kHz	160 kHz	200 kHz
				1	0	f1/112	44.6 kHz	71.4 kHz	89.3 kHz	143 kHz	179 kHz
					1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
		1	0	0	0	f1/56	89.3 kHz	143 kHz	179 kHz	286 kHz	357 kHz
					1	f1/80	62.5 kHz	100 kHz	125 kHz	200 kHz	250 kHz
				1	0	f1/96	52.1 kHz	83.3 kHz	104 kHz	167 kHz	208 kHz
					1	f1/128	39.1 kHz	62.5 kHz	78.1 kHz	125 kHz	156 kHz
			1	0	0	f1/160	31.3 kHz	50.0 kHz	62.5 kHz	100 kHz	125 kHz
					1	f1/200	25.0 kHz	40.0 kHz	50.0 kHz	80.0 kHz	100 kHz
				1	0	f1/224	22.3 kHz	35.7 kHz	44.6 kHz	71.4 kHz	89.3 kHz
					1	f1/256	19.5 kHz	31.3 kHz	39.1 kHz	62.5 kHz	78.1 kHz

Table 20.10 Transfer Rate Examples (2)

IICCR Register		SICR1 Register				Transfer Clock	Transfer Rate				
IICTCHALF	IICTCTWI	CKS3	CKS2	CKS1	CKS0		f1 = 5 MHz	f1 = 8 MHz	f1 = 10 MHz	f1 = 16 MHz	f1 = 20 MHz
0	1	0	0	0	0	f1/28	358 kHz	572 kHz	714 kHz	1142 kHz	1428 kHz
					1	f1/40	250 kHz	400 kHz	500 kHz	800 kHz	1000 kHz
				1	0	f1/48	208 kHz	334 kHz	416 kHz	666 kHz	834 kHz
					1	f1/64	156 kHz	250 kHz	312 kHz	500 kHz	626 kHz
			1	0	0	f1/80	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
					1	f1/100	100 kHz	160 kHz	200 kHz	320 kHz	400 kHz
				1	0	f1/112	89 kHz	143 kHz	179 kHz	286 kHz	358 kHz
					1	f1/128	78 kHz	125 kHz	156 kHz	250 kHz	312 kHz
		1	0	0	0	f1/56	179 kHz	286 kHz	358 kHz	572 kHz	714 kHz
					1	f1/80	125 kHz	200 kHz	250 kHz	400 kHz	500 kHz
				1	0	f1/96	104 kHz	167 kHz	208 kHz	334 kHz	416 kHz
					1	f1/128	78 kHz	125 kHz	156 kHz	250 kHz	312 kHz
			1	0	0	f1/160	63 kHz	100 kHz	125 kHz	200 kHz	250 kHz
					1	f1/200	50 kHz	80 kHz	100 kHz	160 kHz	200 kHz
				1	0	f1/224	45 kHz	71 kHz	89 kHz	143 kHz	179 kHz
					1	f1/256	39 kHz	63 kHz	78 kHz	125 kHz	156 kHz
1	0	0	0	0	0	f1/28	90 kHz	143 kHz	179 kHz	286 kHz	357 kHz
					1	f1/40	63 kHz	100 kHz	125 kHz	200 kHz	250 kHz
				1	0	f1/48	52 kHz	84 kHz	104 kHz	167 kHz	209 kHz
					1	f1/64	39 kHz	63 kHz	78 kHz	125 kHz	157 kHz
			1	0	0	f1/80	31 kHz	50 kHz	63 kHz	100 kHz	125 kHz
					1	f1/100	25 kHz	40 kHz	50 kHz	80 kHz	100 kHz
				1	0	f1/112	22 kHz	36 kHz	45 kHz	72 kHz	90 kHz
					1	f1/128	20 kHz	31 kHz	39 kHz	63 kHz	78 kHz
		1	0	0	0	f1/56	45 kHz	72 kHz	90 kHz	143 kHz	179 kHz
					1	f1/80	31 kHz	50 kHz	63 kHz	100 kHz	125 kHz
				1	0	f1/96	26 kHz	42 kHz	52 kHz	84 kHz	104 kHz
					1	f1/128	20 kHz	31 kHz	39 kHz	63 kHz	78 kHz
			1	0	0	f1/160	16 kHz	25 kHz	31 kHz	50 kHz	63 kHz
					1	f1/200	13 kHz	20 kHz	25 kHz	40 kHz	50 kHz
				1	0	f1/224	11 kHz	18 kHz	22 kHz	36 kHz	45 kHz
					1	f1/256	10 kHz	16 kHz	20 kHz	31 kHz	39 kHz

20.4.1.2 SDA Pin Digital Delay Selection

The digital delay value of the SDA pin can be selected by bits SDADLY0 and SDADLY1 in the IICCR register. Figure 20.17 shows the Operation Example of Digital Delay for SDA Pin.

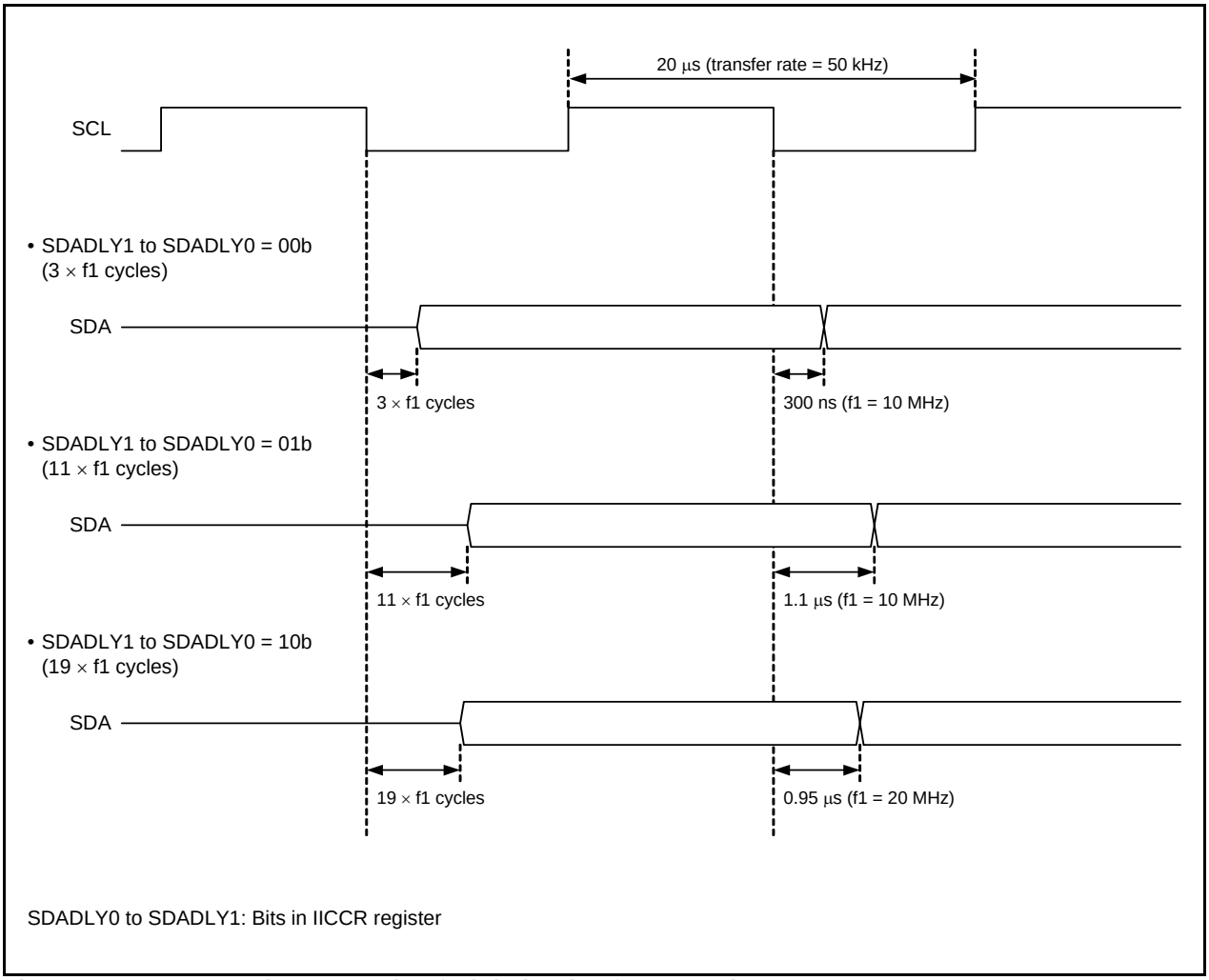


Figure 20.17 Operation Example of Digital Delay for SDA Pin

20.4.1.3 Interrupt Requests

The I2C bus interface has six interrupt requests in I2C bus interface mode and four interrupt requests in clock synchronous serial mode. Table 20.11 lists the Interrupt Requests of I2C bus Interface.

Because these interrupt requests are assigned to the I2C bus interface interrupt vector table, interrupt sources must be determined using bits.

Table 20.11 Interrupt Requests of I2C bus Interface

Interrupt Request		Generation Condition	Format	
			I2C bus	Clock synchronous serial
Transmit data empty	TXI	TIE = 1 and TDRE = 1	Enabled	Enabled
Transmit end	TEI	TEIE = 1 and TEND = 1	Enabled	Enabled
Receive data full	RXI	RIE = 1 and RDRF = 1	Enabled	Enabled
Stop condition detection	STPI	RE_STIE = 1 and STOP = 1	Enabled	Disabled
NACK detection	NAKI	TE_NAKIE = 1 and ORER_AL = 1 (or TE_NAKIE = 1 and NACKF = 1)	Enabled	Disabled
Arbitration lost			Enabled	Disabled
Overrun error			Disabled	Enabled

RE_STIE, TE_NAKIE, RIE, TEIE, TIE: Bits in SIER register
ORER_AL, STOP, NACKF, RDRF, TEND, TDRE: Bits in SISR register

When generation conditions listed in Table 20.11 are met, an I2C bus interface interrupt request is generated. Set the interrupt generation conditions to 0 by the I2C bus interface interrupt routine.

Note that bits TDRE and TEND are automatically set to 0 by writing transmit data to the SITDR register and the RDRF bit is automatically set to 0 by reading the SIRDR register. In particular, the TDRE bit is set to 0 when transmit data is written to the SITDR register and set to 1 when data is transferred from registers SITDR to SISDR. If the TDRE bit is further set to 0, additional 1 byte may be transmitted. Because the data is retained in the transmit buffer, the data is shifted to the shift register by a trigger (the TDRE bit in the SISR register is 0), and thus the same data is retransmitted.

Also, set the RE_STIE bit in the SIER register to 1 (stop condition detection interrupt request enabled) only when the STOP bit in the SISR register is 0.

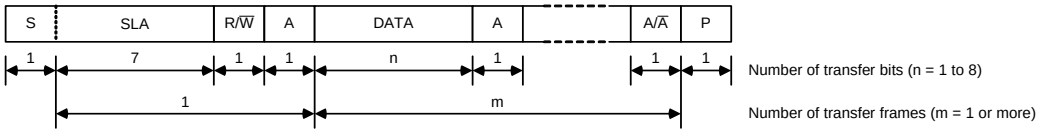
20.4.2 I²C bus Interface Mode

20.4.2.1 I²C bus Format

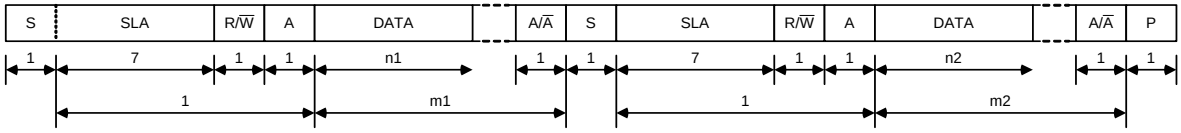
When the MS bit in the SIMR2 register is set to 0, I²C bus interface mode is used for communication.
Figure 20.18 shows the I²C bus Format and Bus Timing. The first frame following the start condition consists of 8 bits.

(1) I²C bus format

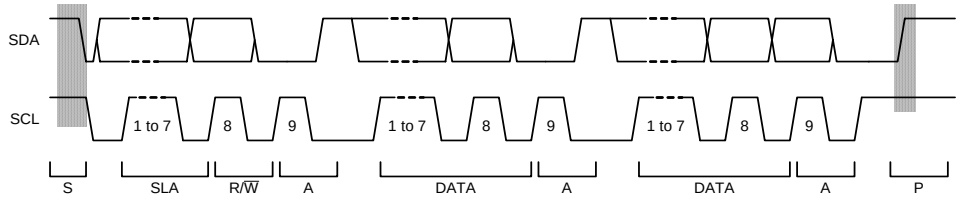
(a) I²C bus format (MS = 0)



(b) I²C bus format (When Start Condition is Retransmitted, MS = 0)



(2) I²C bus timing



Legend:
S : Start condition
The master device changes the SDA signal from high to low while the SCL signal is held high.
SLA : Slave address
R/W : Indicates the direction of data transmission/reception. Data is transmitted when:
R/W value is 1: From the slave device to the master device
R/W value is 0: From the master device to the slave device
A : Acknowledge
The receive device sets the SDA signal to low.
DATA : Transmit/receive data
P : Stop condition
The master device changes the SDA signal from low to high while the SCL signal is held high.

Figure 20.18 I²C bus Format and Bus Timing

20.4.2.2 I²C bus Slave Addressing

In the I²C bus format, the first 1 byte immediately after a start condition is specified as a slave address. When this module operates as a slave device, slave addresses can be programmed using bits SVA0 to SVA6 in the SIMR2 register. However, this does not apply to the “general call address” and the “start byte” defined in the I²C bus specification.

- General call address (0000_000_0)
  Since all the devices are addressed, an acknowledge signal is returned.
- Start byte (0000_000_1)
  All the devices cannot return any acknowledge signal.

20.4.2.3 Master Transmit Operation

In master transmit mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal. Figures 20.19 and 20.20 show the Operation Timing in Master Transmit Mode (I^2C bus Interface Mode).

The transmit procedure and operation in master transmit mode are shown below:

(1) Set the STOP bit in the SISR register to 0 for initialization. Set the ICE bit in the SICR1 register to 1 (transfer operation enabled). Then, set bits CPOS_WAIT and MLS in the SIMR1 register and bits CKS0 to CKS3 in the SICR1 register (initial setting).
(2) After confirming the bus is released by reading the BBSY bit in the SICR2 register, set bits TRS and MST in the SICR1 register to master transmit mode. Then, write 1 to the BBSY bit and 0 to the SCP bit with the MOV instruction (start condition generated). This will generate a start condition.
(3) After confirming the TDRE bit in the SISR register is 1, write transmit data to the SITDR register (data in which a slave address and R/$\overline{W}$ are indicated in the 1st byte). The TDRE bit is automatically set to 0 at this time and data is transferred from registers SITDR to SISDR, and then the TDRE bit is set to 1 again.
(4) When 1 byte of data transmission is completed while the TDRE bit is 1, the TEND bit in the SISR register is set to 1 at the rising edge of the 9th clock cycle of the transmit clock. After confirming the slave device is selected by reading the ACKBR bit in the SIER register, write the 2nd byte of data to the SITDR register. Since the slave device is not acknowledged when the ACKBR bit is 1, generate a stop condition. A stop condition is generated by writing 0 to the BBSY bit and 0 to the SCP bit with the MOV instruction. The SCL signal is fixed at low until data is ready or a stop condition is generated.
(5) Write the transmit data after the 2nd byte to the SITDR register every time the TDRE bit is set to 1.
(6) When the number of bytes to be transmitted is written to the SITDR register, wait until the TEND bit is set to 1 while the TDRE bit is 1. Or wait for NACK (NACKF bit in SISR register = 1) from the receive device while the ACKE bit in the SIER register is 1 (when the receive acknowledge bit is 1, transfer is halted). Then, generate a stop condition and set the TEND bit or the NACKF bit to 0.
(7) When the STOP bit in the SISR register is set to 1, return to slave receive mode.

To generate a restart condition after receiving NACK, use the following procedure:

(1) Confirm a NACK error.
(2) Generate a restart condition.
(3) Confirm the rising edge of the SCL signal.
(4) Set bits NACKF and TEND in the SISR register to 0.

- **Operation and Switching Flow When Start/Stop Condition is Detected during Master Transmit Operation**

(1) Detect arbitration is lost and enter to slave receive mode.
(2) Set bits ORER_AL and TDRE in the SISR register to 0.
(3) Confirm the BBSY bit in the SICR2 register.
→ If this bit is 1, receive a slave address.
→ If this bit is 0, master and slave operations are both possible.

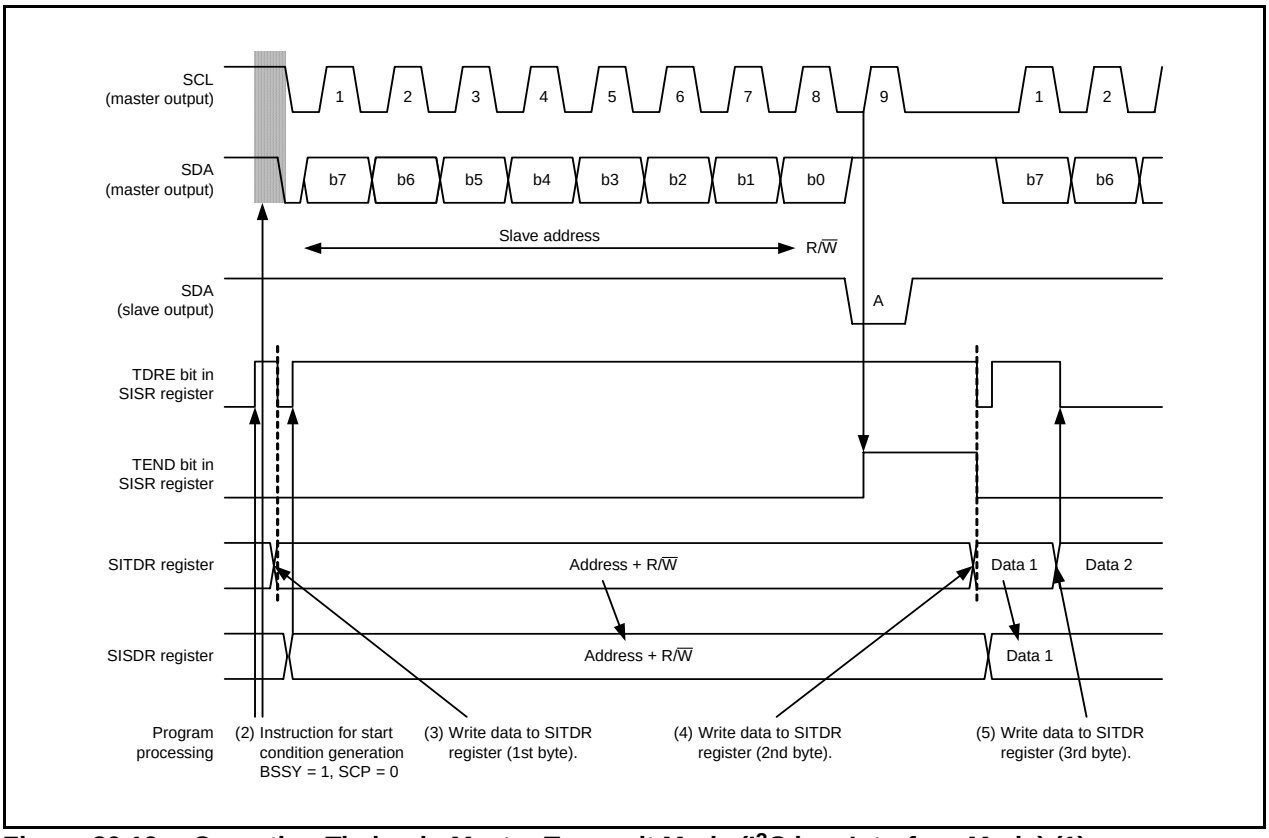


Figure 20.19 Operation Timing in Master Transmit Mode (I^2C bus Interface Mode) (1)

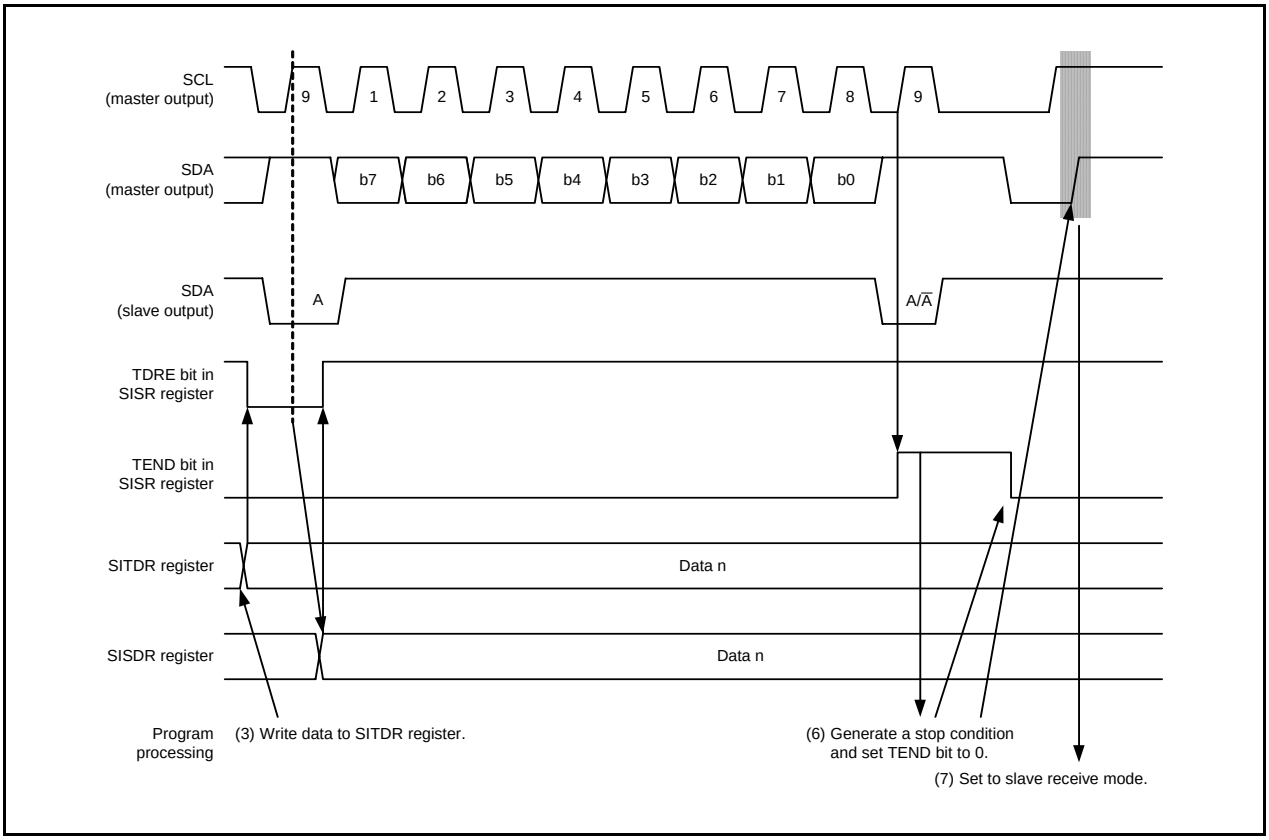


Figure 20.20 Operation Timing in Master Transmit Mode (I^2C bus Interface Mode) (2)

20.4.2.4 Master Receive Operation

In master receive mode, the master device outputs the receive clock, receives data from the slave device, and returns an acknowledge signal. Figures 20.21 and 20.22 show the Operation Timing in Master Receive Mode (I^2C bus Interface Mode).

The receive procedure and operation in master receive mode are as follows:

(1) After setting the TEND bit in the SISR register to 0, set the TRS bit in the SICR1 register to 0 to switch from master transmit mode to master receive mode. Then, set the TDRE bit in the SISR register to 0.
(2) Reception is started by performing a dummy read of the SIRDR register. The receive clock is output in synchronization with the internal clock and data is received. The master device outputs the level set by the CEIE_ACKBT bit in the SIER register to the SDA pin at the rising edge of the 9th clock cycle of the receive clock.
(3) When one frame of data reception is completed, the RDRF bit in the SISR register is set to 1 at the rising edge of the 9th clock cycle of the receive clock. If the SIRDR register is read at this time, the received data can be read and the RDRF bit is set to 0 at the same time.
(4) Reception can be performed continuously by reading the SIRDR register every time the RDRF bit is set to 1. If reading of the SIRDR register is delayed by another process and the 8th clock cycle falls while the RDRF bit is 1, the SCL signal is fixed at low until the SIRDR register is read. No stop condition or repeat start condition can be generated at this time.
(5) If the next frame is the last receive frame, set the RCVD bit in the SICR1 register to 1 (next receive operation disabled) and the CEIE_ACKBT bit to 1 before reading the SIRDR register. This enables returning NACK to the slave device and a stop condition can be generated after the next reception.
(6) When the RDRF bit is set to 1 at the rising edge of the 9th clock cycle of the receive clock, generate a stop condition.
(7) When the STOP bit in the SISR register is set to 1, read the SIRDR register. Then, set the RCVD bit to 0 (next receive operation continues).
(8) Return to slave receive mode.

- **Flow for Generating Repeat Start Condition during Master Receive Mode**

To generate a repeat start condition after transmitting NACK, use the following procedure:

(1) The same applies as the flow for generating a stop condition until step (5).
(2) After the RDRF bit is set to 1 at the rising edge of the 9th clock of the receive clock, generate a repeat start condition (write 1 to BBSY and 0 to SCP with the MOV instruction).
(3) Read the SIRDR register after setting to master transmit mode. Then set the RCVD bit to 0 (next receive operation continues).
(4) Write the data indicating a slave address and R/W to the SITDR.

Note 1: After a repeat start condition is generated (write 1 to BBSY and 0 to SCP with the MOV instruction), the SCL and SDA signals are held low after 2.5 cycles or more of the transfer clock. Be sure to set to master transmit mode before that.

- **Operation and Switching Flow When Stop Condition is Detected during Master Receive Operation**

(1) Detect a stop condition and enter to slave receive mode.
(2) Confirm the BBSY bit in the SICR2 register is 0.
(3) Set the STOP bit in the SISR register to 0.
(4) Reset the control block.

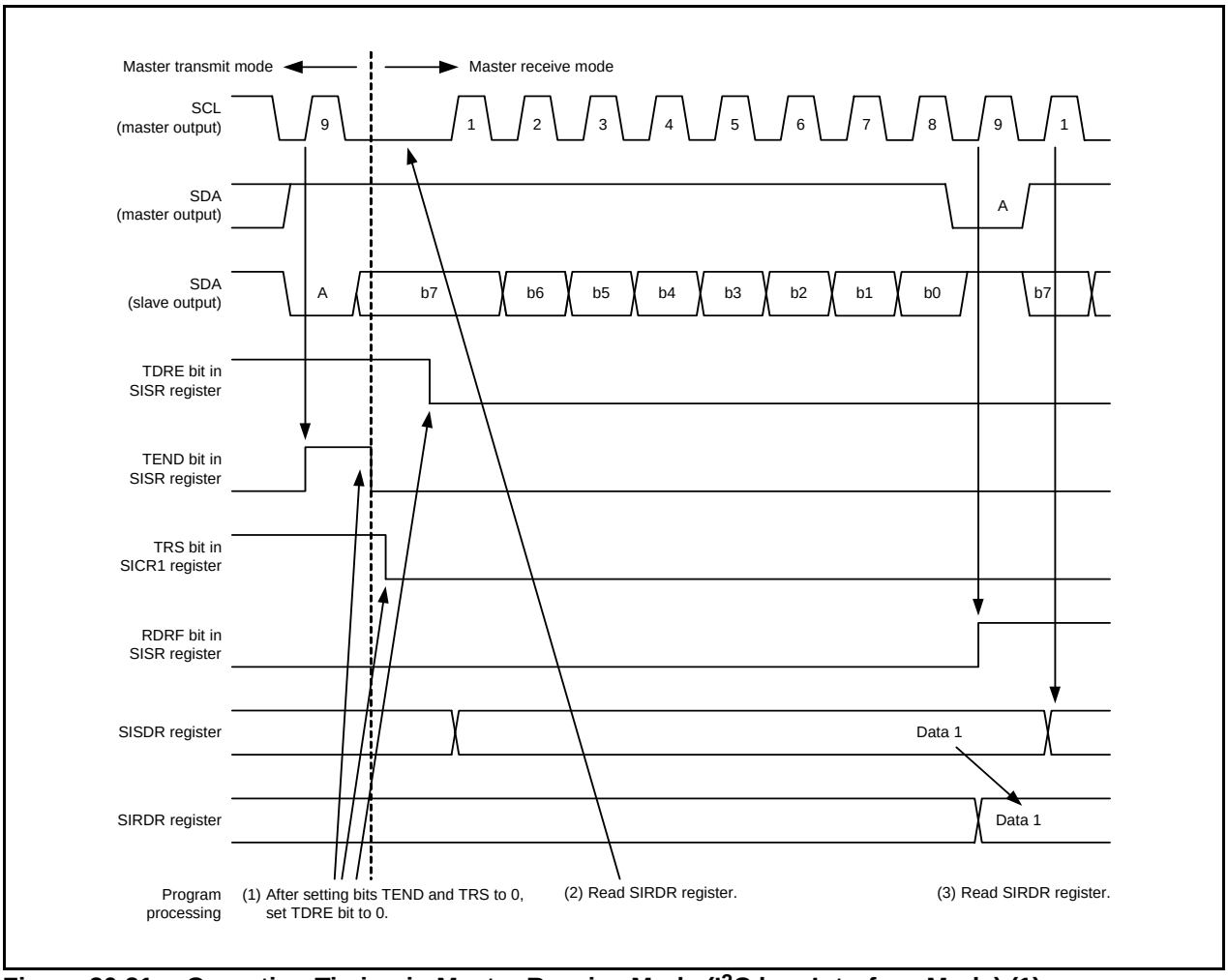


Figure 20.21 Operation Timing in Master Receive Mode (I^2C bus Interface Mode) (1)

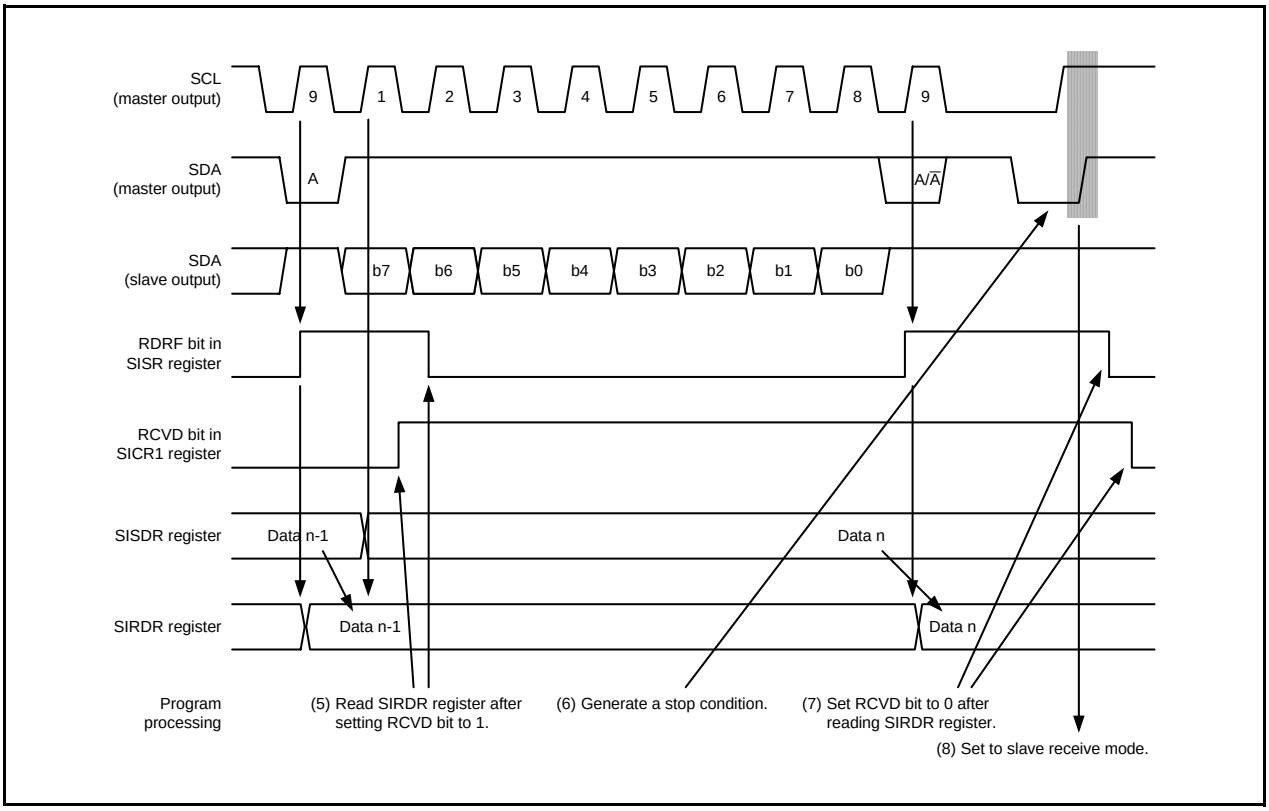


Figure 20.22 Operation Timing in Master Receive Mode (I^2C bus Interface Mode) (2)

20.4.2.5 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data while the master device outputs the receive clock and returns an acknowledge signal. Figures 20.23 and 20.24 show the Operation Timing in Slave Transmit Mode (I^2C bus Interface Mode).

The transmit procedure and operation in slave transmit mode are as follows:

(1) Set the ICE bit in the SICR1 register to 1 (transfer operation enabled). Then, set bits CPOS_WAIT and MLS in the SIMR1 register and bits CKS0 to CKS3 in the SICR1 register (initial setting). Next, set bits TRS and MST in the SICR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set by the CEIE_ACKBT bit in the SIER register to the SDA pin between the falling edge of the 8th clock cycle and the falling edge of the 9th clock cycle. If the 8th bit of data (R/$\overline{W}$) is 1, the TRS bit and the TDRE bit in the SISR register are set to 1, and the mode is switched to slave transmit mode automatically. Continuous transmission is enabled by writing transmit data to the SITDR register every time the TDRE bit is set to 1.

(3) When the TDRE bit is set to 1 after the last transmit data is written to the SITDR register, wait until the TEND bit is set to 1 while the TDRE bit is 1. After the TEND bit is set to 1, set the TEND bit to 0.

(4) Set the TRS bit to 0 and perform a dummy read of the SIRDR register to complete the process. This will release the SCL signal.

(5) Set the TDRE bit to 0.

- **Maintaining Data Setup Time during Slave Transmit Operation**

During data transfer, if the 9th clock cycle falls while the TDRE bit is 1 and the TEND bit is 1, the SCL signal is fixed at low until transmit data is written to the transmit register. After transmit data is written, maintain the data setup time set with the CKS3 bit after the transmit data is output to the SDA pin and release the SCL signal (rising) (See **Figure 20.25 Data Setup Time during Slave Transmit Operation**).

The CKS3 bit 0: 9, 10 Tcyc
1: 17 to 20 Tcyc (1 Tcyc = 1/f1 (s))

The setup time is doubled when the IICTCHALF bit in the IICCR register is set to 1, and halved when the IICTCTWI bit in the IICCR register is set to 1.

- **Operation and Switching Flow When Stop Condition is Detected during Slave Transmit Operation**

(1) Set to slave receive mode.

(2) Set the TDRE bit in the SISR register to 0.

When a start condition is detected during slave transmit operation, any address following that condition cannot be received. Reset the control block and input a start condition again.

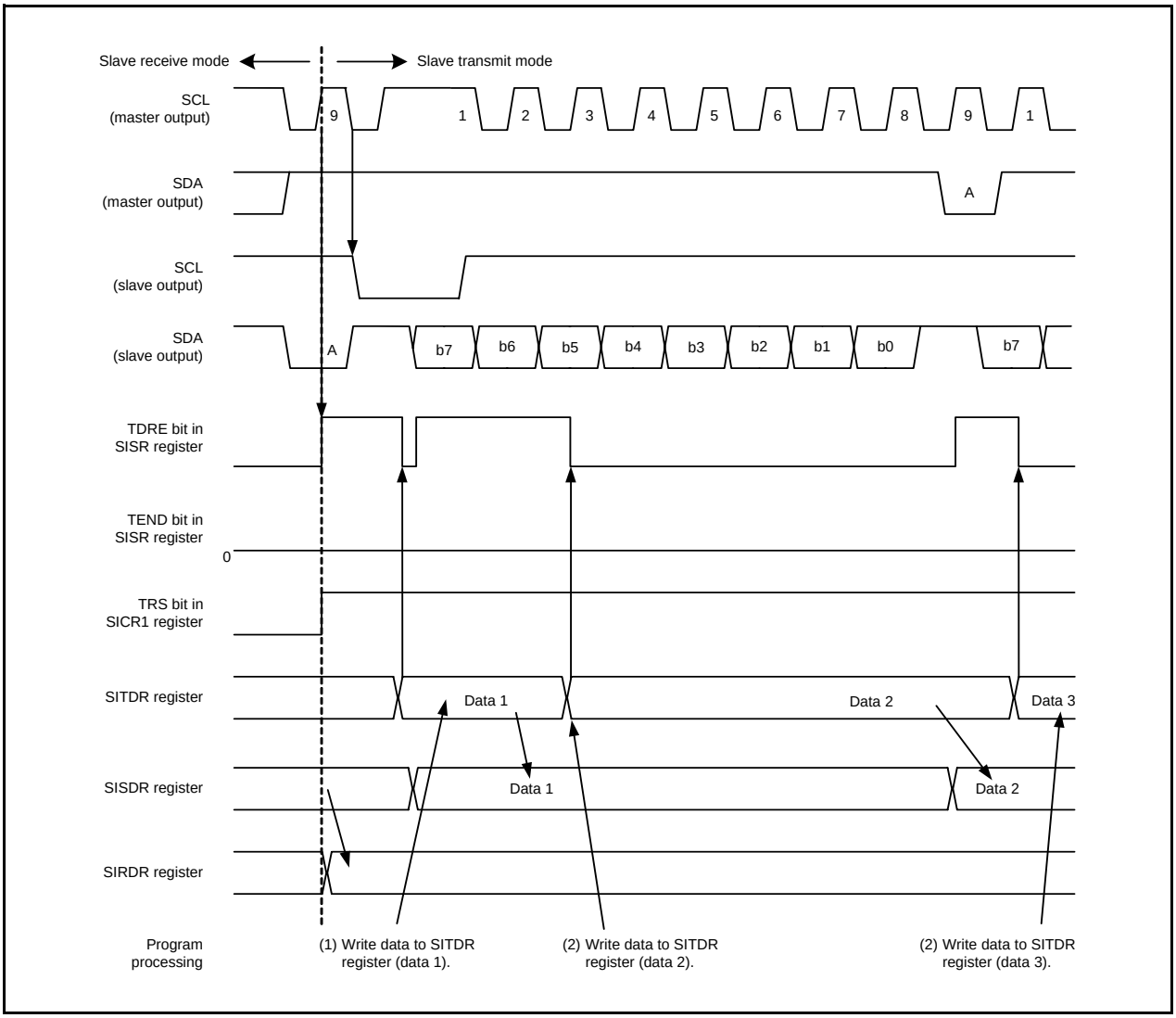


Figure 20.23 Operation Timing in Slave Transmit Mode (I^2C bus Interface Mode) (1)

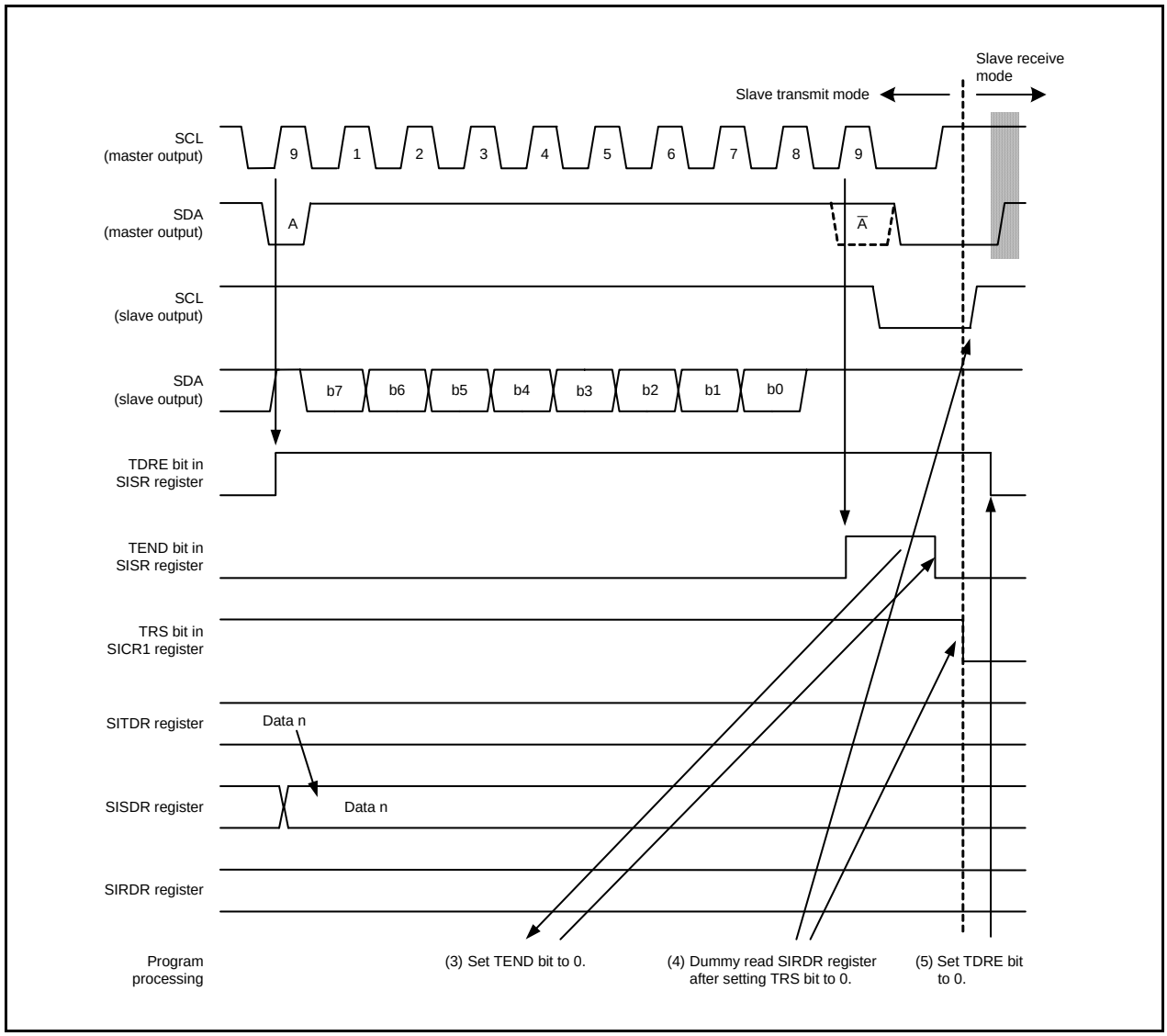


Figure 20.24 Operation Timing in Slave Transmit Mode (I^2C bus Interface Mode) (2)

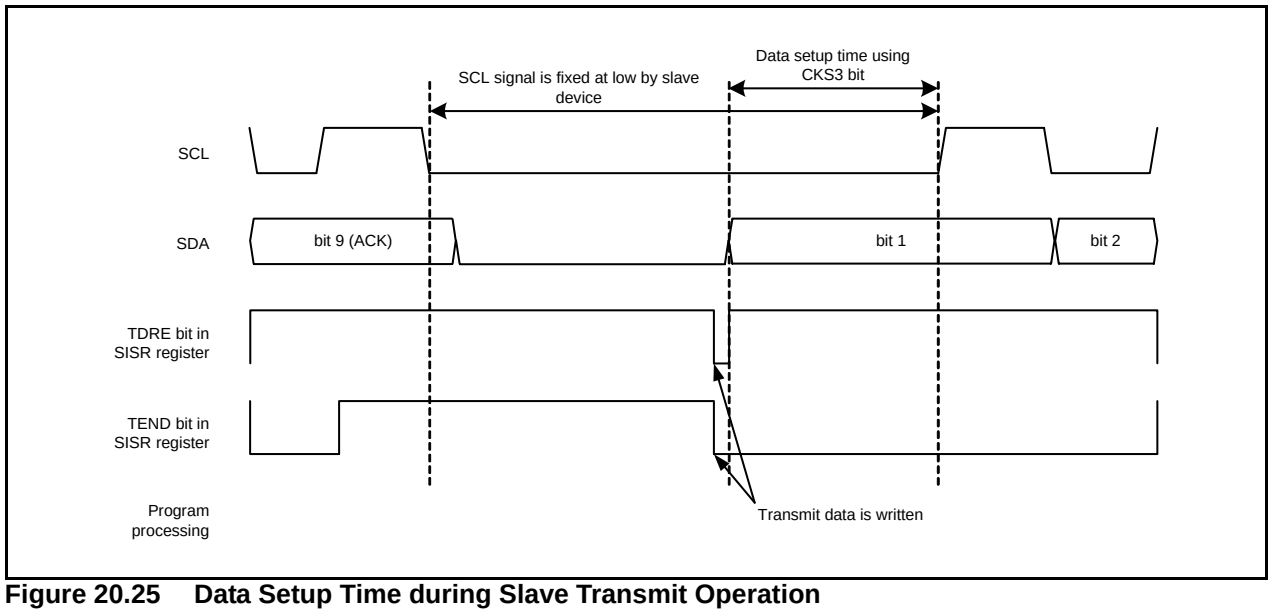


Figure 20.25 Data Setup Time during Slave Transmit Operation

20.4.2.6 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal. Figures 20.26 and 20.27 show the Operation Timing in Slave Receive Mode (I^2C bus Interface Mode).

The receive procedure and operation in slave receive mode are as follows:

(1) Set the ICE bit in the SICR1 register to 1 (transfer operation enabled). Then, set bits CPOS_WAIT and MLS in the SIMR1 register and bits CKS0 to CKS3 in the SICR1 register (initial setting). Next, set bits TRS and MST in the SICR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after the start condition is detected, the slave device outputs the level set in the CEIE_ACKBT bit in the SIER register to the SDA pin between the falling edge of the 8th clock cycle and the falling edge of the 9th clock cycle. Since the RDRF bit in the SISR register is set to 1 simultaneously, perform a dummy read of the SIRDR register (the read data is unnecessary because it indicates the slave address and R/$\overline{W}$).

(3) Read the SIRDR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is 1, the SCL signal is fixed at low until the SIRDR register is read. The setting change of the acknowledge signal returned to the master device before reading the SIRDR register takes effect from the following transfer frame.

(4) If the next frame is the last receive frame, set the CEIE_ACKBT bit in the SIER register to 1 before reading the SIRDR register. This enables returning NACK to the master device and a stop can be generated after the next reception.

(5) Reading the last byte is also performed by reading the SIRDR register.

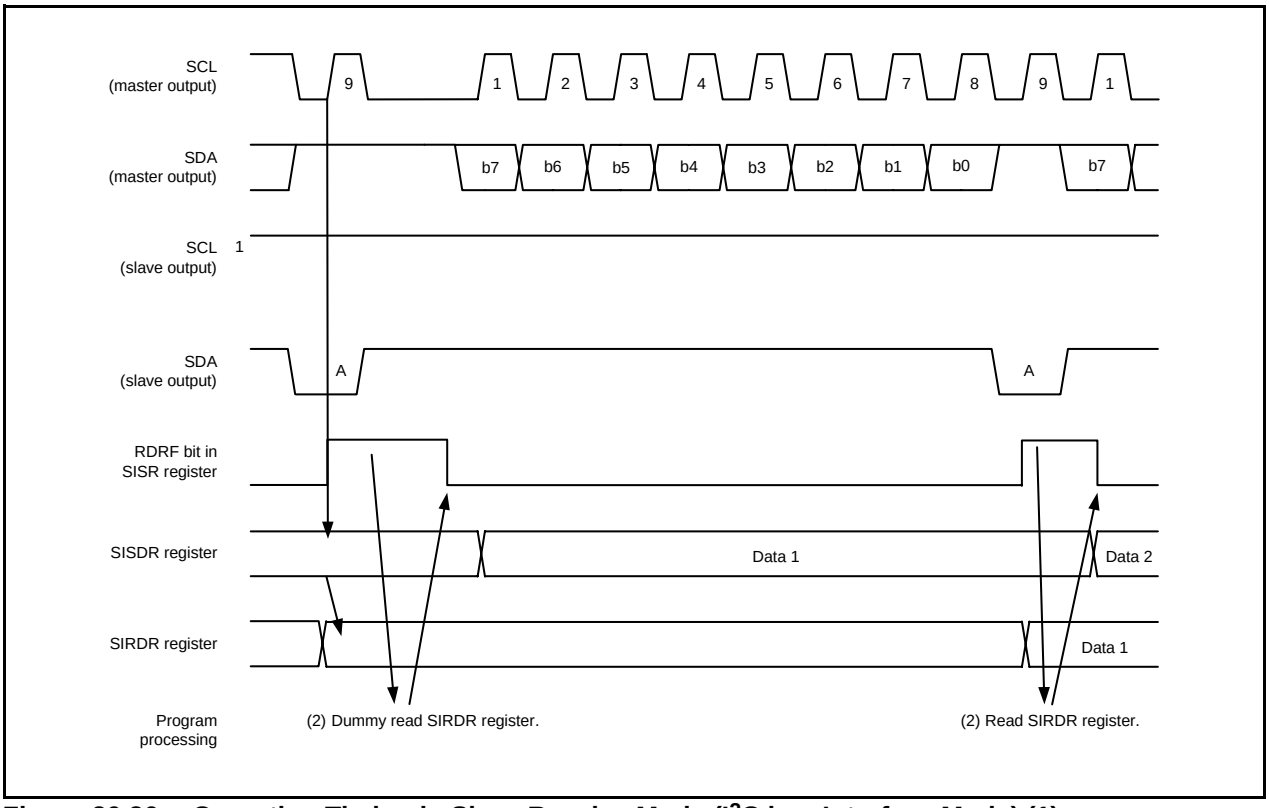


Figure 20.26 Operation Timing in Slave Receive Mode (I^2C bus Interface Mode) (1)

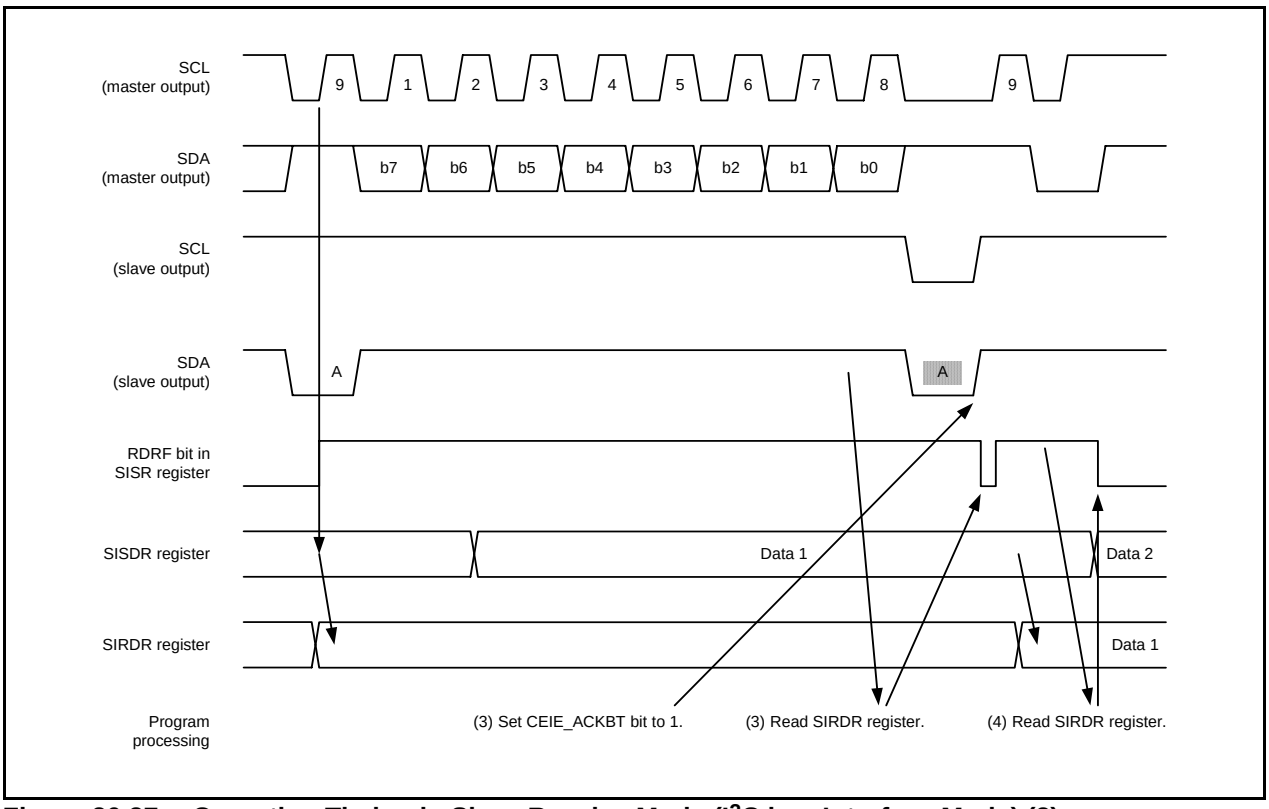


Figure 20.27 Operation Timing in Slave Receive Mode (I^2C bus Interface Mode) (2)

20.4.3 Clock Synchronous Serial Mode

20.4.3.1 Clock Synchronous Serial Format

When the MS bit in the SIMR2 register is set to 1, the clock synchronous serial format is used for communication.
Figure 20.28 shows the Transfer Format for Clock Synchronous Serial Mode.

When the MST bit in the SICR1 register is 1, the transfer clock is output from the SCL pin. When the MST bit is set to 0, the external clock is input.

The transfer data is output between successive falling edges of the SCL clock, and data is determined at the rising edge of the SCL clock. MSB first or LSB first can be selected as the order of the data transfer by setting the MLS bit in the SIMR1 register. The SDA output level can be changed by the SDAO bit in the SICR2 register during transfer standby.

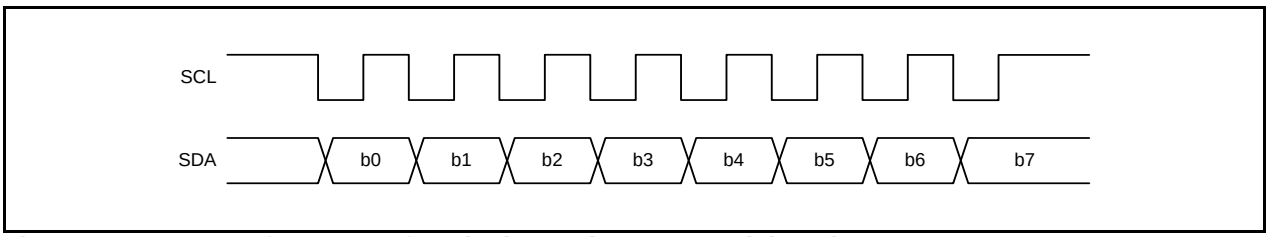


Figure 20.28 Transfer Format for Clock Synchronous Serial Mode

20.4.3.2 Transmit Operation

In transmit mode, transmit data is output from the SDA pin in synchronization with the falling edge of the transfer clock. The transfer clock is output when the MST bit in the SICR1 register is 1 and input when the MST bit is 0.
Figure 20.29 shows the Operation Timing in Transmit Mode (Clock Synchronous Serial Mode).

The transmit procedure and operation in transmit mode are as follows:

(1) Set the ICE bit in the SICR1 register to 1 (transfer operation enabled). Then, set bits CKS0 to CKS3 in the SICR1 register and the MST bit (initial setting).
(2) Set the TRS bit in the SICR1 register to 1 to select transmit mode. This will set the TDRE bit in the SISR register to 1.
(3) After confirming the TDRE bit is 1, write transmit data to the SITDR register. Data is transferred from registers SITDR to SISDR and the TDRE bit is automatically set to 1. Continuous transmission is enabled by writing data to the SITDR register every time the TDRE bit is set to 1. To switch from transmit to receive mode, set the TRS bit to 0 while the TDRE bit is 1.

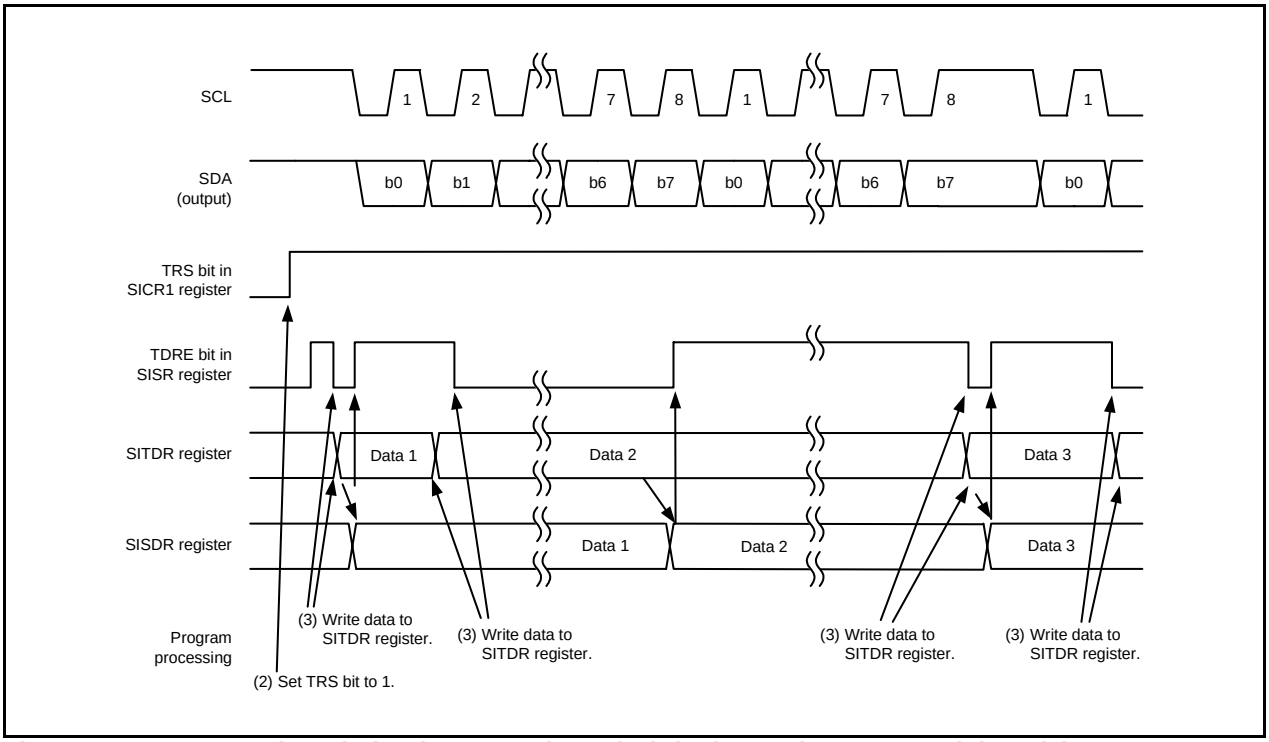


Figure 20.29 Operation Timing in Transmit Mode (Clock Synchronous Serial Mode)

20.4.3.3 Receive Operation

In receive mode, data is latched at the rising edge of the transfer clock. The transfer clock is output when the MST bit in the SICR1 register is 1 and input when the MST bit is 0.
Figure 20.30 shows the Operation Timing in Receive Mode (Clock Synchronous Serial Mode).

The receive procedure and operation in receive mode are as follows:

(1) Set the ICE bit in the SICR1 register to 1 (transfer operation enabled). Then, set bits CKS0 to CKS3 in the SICR1 register and the MST bit (initial setting).
(2) Set the MST bit to 1 while the transfer clock is being output. This will start the output of the receive clock.
(3) When the receive operation is completed, data is transferred from registers SISDR to SIRDR and the RDRF bit in the SISR register is set to 1. When the MST bit is set to 1, the clock is output continuously since the next byte of data is enabled for reception. Continuous reception is enabled by reading the SIRDR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is 1, an overrun is detected and the ORER_AL bit in the SISR register is set to 1. At this time, the last receive data is retained in the SIRDR register.
(4) When the MST bit is 1, set the RCVD bit in the SICR1 register to 1 (next receive operation disabled) before reading the SIRDR register. The SCL signal is fixed at high after the following byte of data reception is completed.

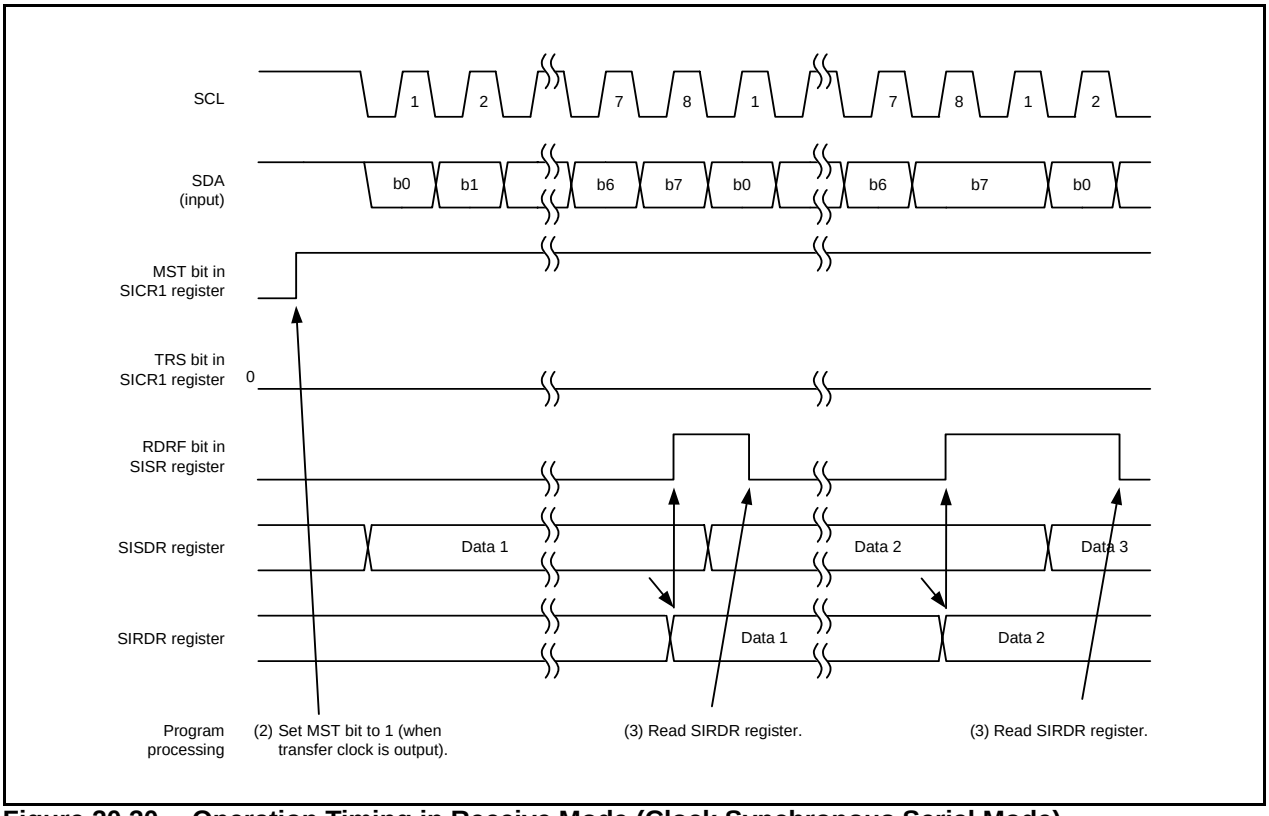


Figure 20.30 Operation Timing in Receive Mode (Clock Synchronous Serial Mode)

20.4.4 Register Setting Examples

Figures 20.31 to 20.34 show examples of register setting when the I²C bus interface is used.

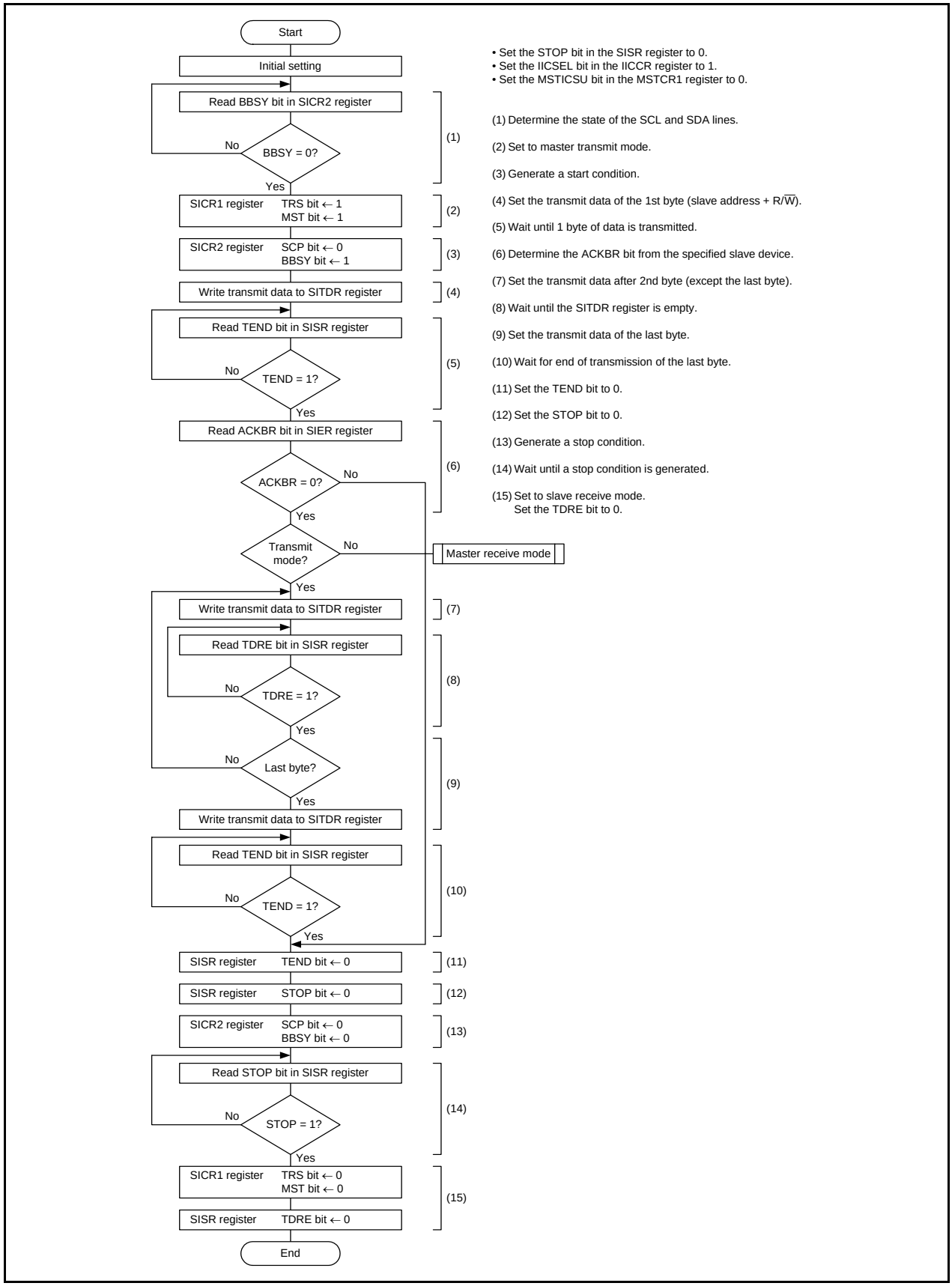
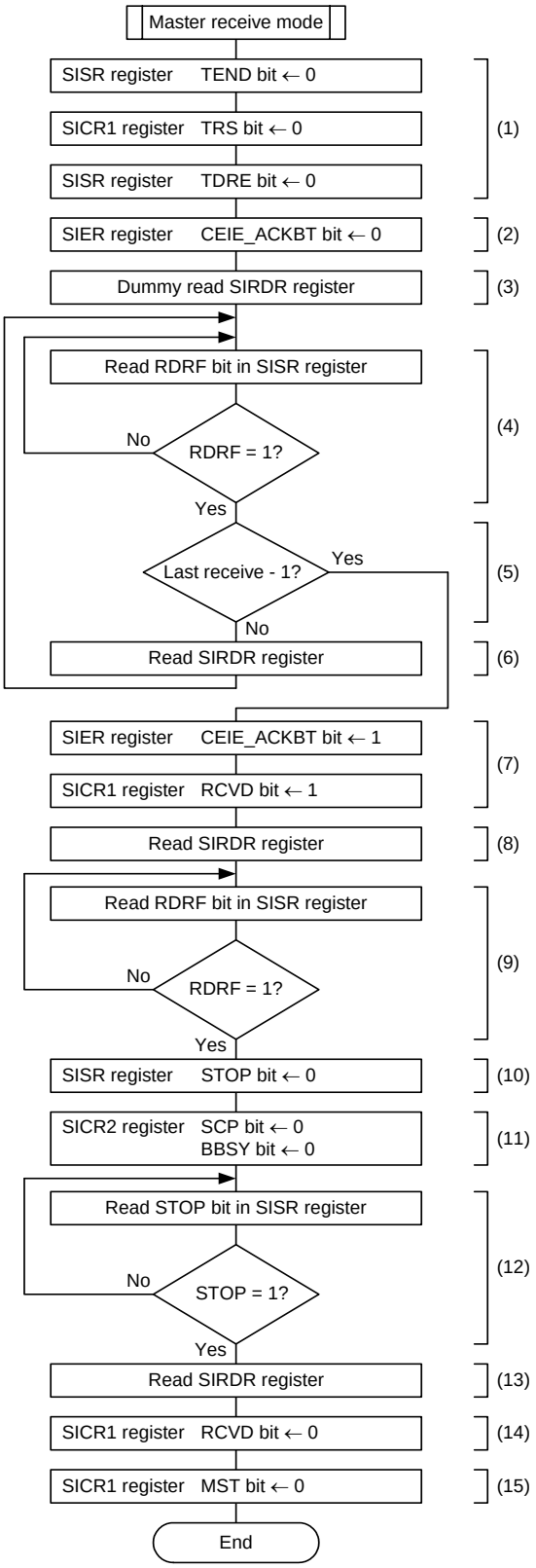


Figure 20.31 Register Setting Example in Master Transmit Mode (I²C bus Interface Mode)



(1) Set the TEND bit to 0 and set to master receive mode. Set the TDRE bit to 0. (1, 2)

(2) Set the ACKBT bit to the transmit device. (1)

(3) Dummy read the SIRDR register. (1)

(4) Wait until 1 byte is received.

(5) Determine (last receive - 1).

(6) Read the receive data.

(7) Set the ACKBT bit of the last byte and set continuous receive operation to disable (RCVD = 1). (2)

(8) Read the receive data of (last byte - 1).

(9) Wait until the last byte is received.

(10) Set the STOP bit to 0.

(11) Generate a stop condition.

(12) Wait until a stop condition is generated.

(13) Read the receive data of the last byte.

(14) Set the RCVD bit to 0.

(15) Set to slave receive mode.

Notes:
1. Do not generate interrupts during process steps (1) to (3).
2. For 1 byte of data reception, skip steps (2) to (6) after step (1) and jump to process step (7). Process step (8) is a dummy read from the SIRDR register.

Figure 20.32 Register Setting Example in Master Receive Mode (I^2C bus Interface Mode)

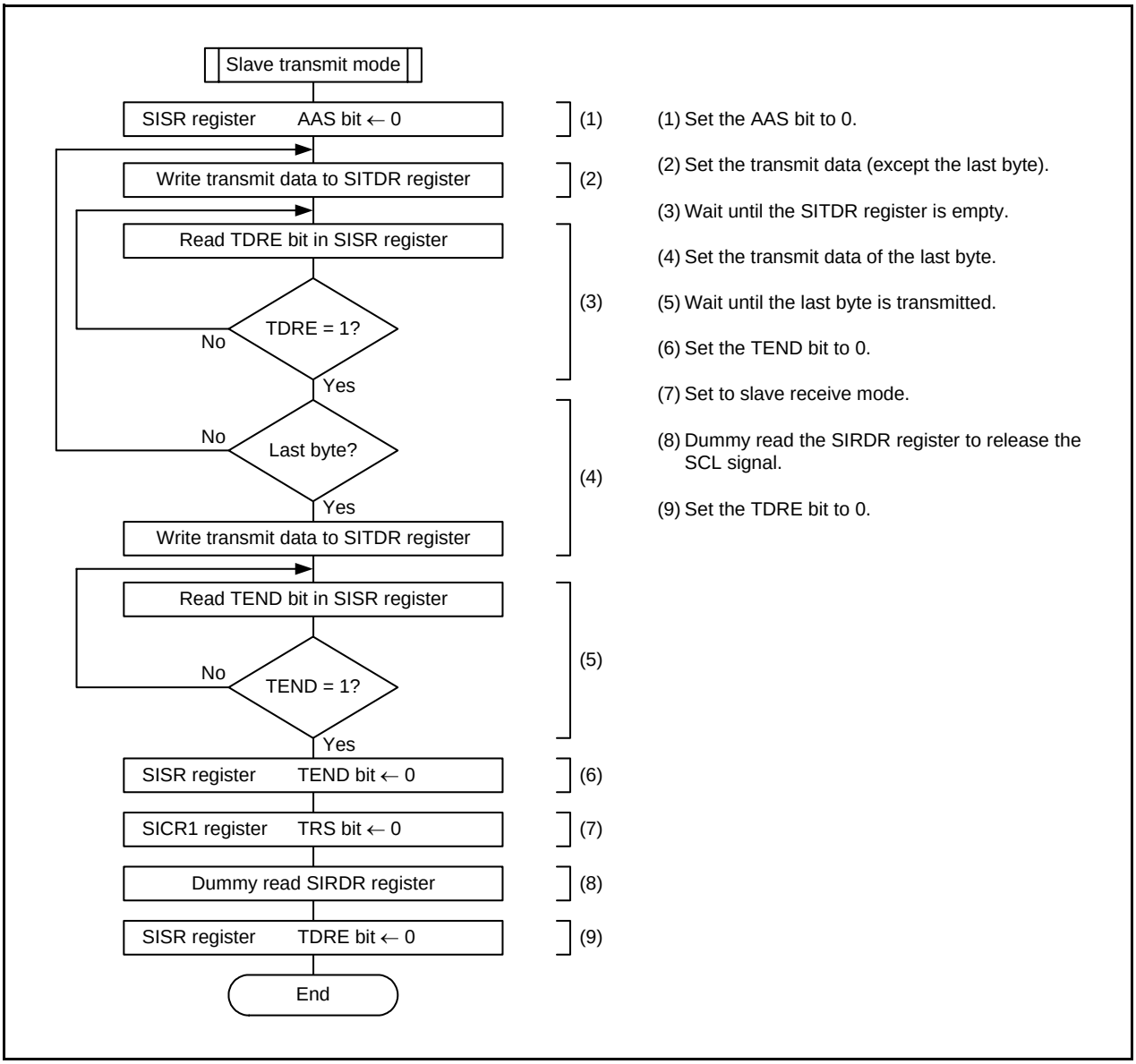
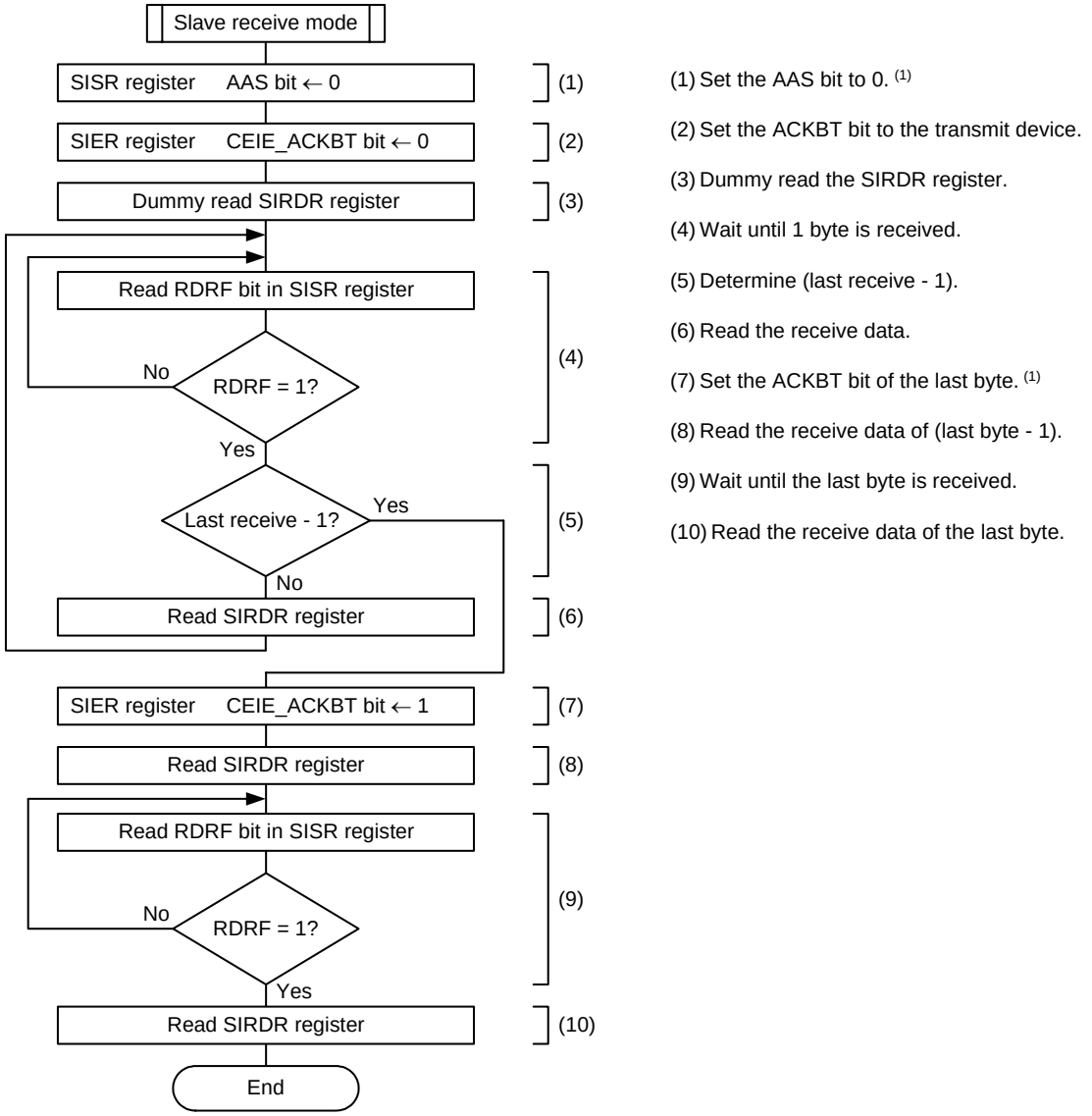


Figure 20.33 Register Setting Example in Slave Transmit Mode (I^2C bus Interface Mode)



Note:
1. For 1 byte of data reception, skip steps (2) to (6) after step (1) and jump to process step (7). Process step (8) is a dummy read from the SIRDR register.

Figure 20.34 Register Setting Example in Slave Receive Mode (I^2C bus Interface Mode)

20.4.5 Noise Canceller

The states of pins SCL and SDA are routed through the noise canceller before being latched internally. Figure 20.35 shows the Noise Canceller Block Diagram.

The noise canceller consists of two cascaded latch and match detection circuits. When the SCL pin input signal (or SDA pin input signal) is sampled on f1 and two latch outputs match, the level is passed forward to the next circuit. When they do not match, the former value is retained.

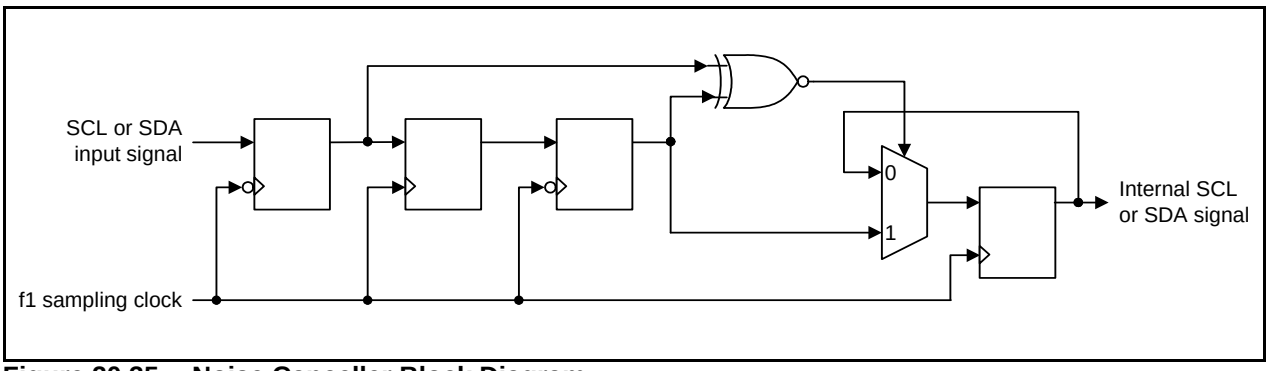


Figure 20.35 Noise Canceller Block Diagram

20.4.6 Bit Synchronization Circuit

When the I^2C bus interface is set to master mode, the high-level period may become shorter if:

- The SCL signal is held low by a slave device.
- The rise speed of the SCL signal is reduced by a load (load capacity or pull-up resistor) on the SCL line.

Therefore, the SCL signal is monitored and communication is synchronized bit by bit.

Figure 20.36 shows the Timing of Bit Synchronization Circuit. Table 20.12 lists the Time between Changing SCL Signal from Low-Level Output to High Impedance and Monitoring SCL Signal.

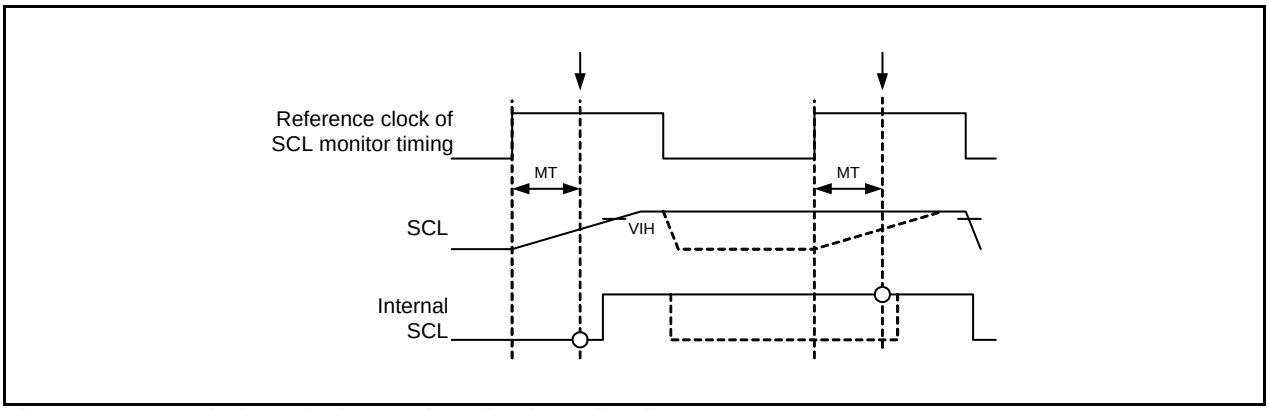


Figure 20.36 Timing of Bit Synchronization Circuit

Table 20.12 Time between Changing SCL Signal from Low-Level Output to High Impedance and Monitoring SCL Signal

SICR1 Register				SCL Monitoring Time (MT)
IICTCHALF	IICTCTW1	CKS3	CKS2	
0	0	0	0	7.5 Tcyc
			1	19.5 Tcyc
		1	0	17.5 Tcyc
			1	41.5 Tcyc
0	1	0	0	2.5 Tcyc
			1	8.5 Tcyc
		1	0	7.5 Tcyc
			1	19.5 Tcyc
1	0	0	0	17.5 Tcyc
			1	41.5 Tcyc
		1	0	37.5 Tcyc
			1	85.5 Tcyc

1 Tcyc = 1/f1 (s)

When SCK = 1000b, the bit synchronization circuit does not function even if the high-level period of the SCL signal is 600 ns or less (breach of the I^2C specification).

20.4.7 Procedure for Resetting Control Block in I²C bus Interface Mode

In I²C bus interface mode, writing 1 to the SIRST bit in the SICR2 register can reset some of the I²C bus function registers and the control block. Figure 20.37 shows the Procedure for Resetting Control Block in I²C bus Interface Mode.
When the control block is reset ((2) in Figure 20.37), the corresponding IR bit for the ICU may be set to 1 (interrupt requested). For the notes on clearing the IR bit, see **11. Interrupts**.

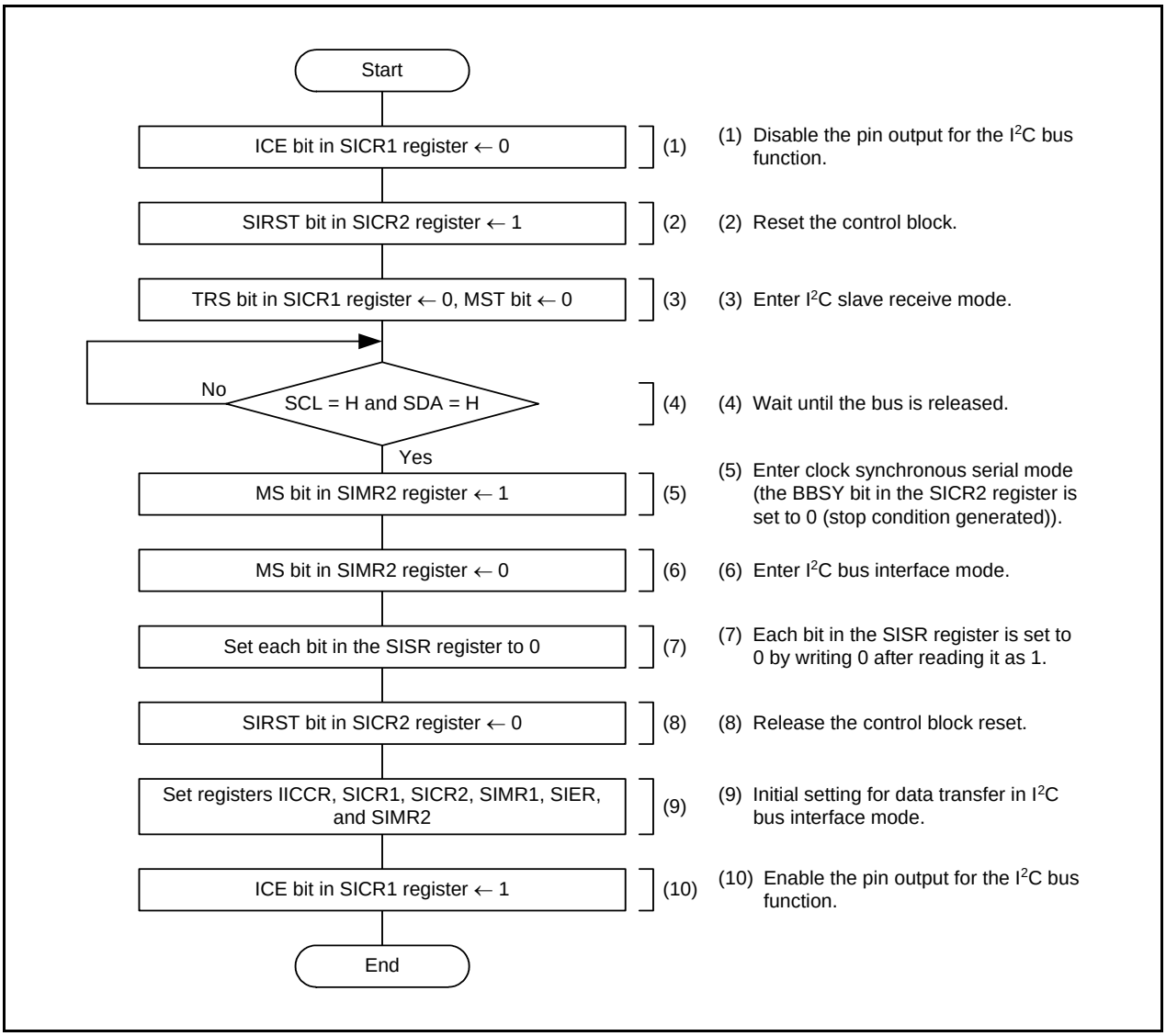


Figure 20.37 Procedure for Resetting Control Block in I²C bus Interface Mode

20.5 Notes on Clock Synchronous Serial Interface

20.5.1 Notes on Synchronous Serial Communication Unit

To use the synchronous serial communication unit, set the IICSEL bit in the IICCR register to 0 (SSU function).

20.5.2 Notes on I²C bus Interface

To use the I²C bus interface, set the IICSEL bit in the IICCR register to 1 (I²C bus function).

Notes regarding the I²C specification

Do not use the I²C interface with the settings that do not meet the I²C specification.

(1) In the I²C specification, the transfer rate is a maximum of 400 kHz and the low-level period of the SCL signal is a minimum of 1.3 µs in high-speed mode. Since the duty cycle for the I²C bus interface in this MCU is 50%, this minimum of 1.3 µs for the low-level period of the SCL signal cannot be met during operation at 400 kHz. To meet this minimum of 1.3 µs for the low-level period of the SCL signal, set the transfer rate to 384.6 kHz or below to use the I²C bus interface.

(2) There must be a delay of a minimum of 300 ns for the SDA pin to change at the rising edge of the SCL signal. For the I²C bus interface in this MCU, the delay value can be set by bits SDADLY0 to SDADLY1 in the IICCR register. The delay value must be determined for the system. When f1 is set to 11 MHz or above, set bits SDADLY1 to SDADLY0 in the IICCR register to 01b (digital delay of 11 × f1 cycles) or 10b (digital delay of 19 × f1 cycles).

(3) There is no compatibility with the CBUS.

(4) 10-bit addressing cannot be used.

(5) When a start condition is detected while data is transmitted in slave transmission, any address following that condition cannot be received and the operation is stopped. Follow the procedure for resetting the control block to reset the I²C bus interface.

(6) Do not set to 1111XXXb and 0000XXXb as slave addresses.

(7) When starting communication by the master after a stop condition is detected, set the STOP bit in the SISR register to 0.

20.5.3 ICE Bit in SICR1 Register and SIRST Bit in SICR2 Register

When writing 0 to the ICE bit or 1 to the SIRST bit during an I2C bus interface operation, the BBSY bit in the SICR2 register and the STOP bit in the SISR register may become undefined.

20.5.3.1 Conditions When Bits Become Undefined

- When this module occupies the I2C bus in master transmit mode (bits MST and TRS in the SICR1 register are 1).
- When this module occupies the I2C bus in master receive mode (the MST bit is 1 and the TRS bit is 0).
- When this module transmits data in slave transmit mode (the MST bit is 0 and the TRS bit is 1).
- When this module transmits an acknowledge in slave receive mode (bits MST and TRS are 0).

20.5.3.2 Countermeasures

- When the start condition (the SDA falling edge when SCL is high) is input, the BBSY bit becomes 1.
- When the stop condition (the SDA rising edge when SCL is high) is input, the BBSY bit becomes 0.
- When writing 1 to the BBSY bit, 0 to the SCP bit, and the start condition (the SDA falling edge when SCL is high) is output while SCL and SDA are high in master transmit mode, the BBSY bit becomes 1.
- When writing 0 to bits BBSY and SCP, the stop condition (the SDA rising edge when SCL is high) is output while SDA is low, and this is the only module that holds SCL low in master transmit mode or master receive mode, the BBSY bit becomes 0.
- When writing 1 to the FS bit in the SAR register, the BBSY bit becomes 0.

20.5.3.3 Additional Descriptions Regarding SIRST Bit

- When writing 1 to the SIRST bit, bits SDAO and SCLO in the SICR2 register become 1.
- When writing 1 to the SIRST bit in master transmit mode and slave transmit mode, the TDRE bit in the SISR register becomes 1.
- While the control block of the I2C bus interface is reset by setting the SIRST bit to 1, writing to bits BBSY, SCP, and SDAO is disabled. Write 0 to the SIRST bit before writing to the BBSY bit, SCP bit, or SDAO bit.
- Even when writing 1 to the SIRST bit, the BBSY bit does not become 0. However, the stop condition (the SDA rising edge when SCL is high) may be generated depending on the states of SCL and SDA and the BBSY bit may become 0.
  There may also be a similar effect on other bits.
- While the control block of the I2C bus interface is reset by setting the SIRST bit to 1, data transmission/reception is stopped. However, the function to detect the start condition, stop condition, or arbitration lost operates. The values in the SICR1 register, SICR2 register, or SISR register may be updated depending on the signals applied to pins SCL and SDA.

21. A/D Converter

This MCU features a 10-bit successive approximation A/D converter that can process analog inputs for up to eight channels.

21.1 Overview

Table 21.1 lists the A/D Converter Specifications. Figure 21.1 shows the A/D Converter Block Diagram.

Table 21.1 A/D Converter Specifications

Item	Specification
A/D conversion method	Successive approximation (with capacitive coupling amplifier)
Analog input voltage	0 V to AVCC
Input channels	8 channels (AN0 to AN7)
Resolution	10 bits
A/D conversion clock	f1, f2, f4, f8, or fAD
Conversion time	2.2 μs (A/D conversion clock = 20 MHz)
A/D operating modes	• One-shot mode: A/D conversion is performed on the specified single channel for a single round. • Repeat mode: A/D conversion is performed on the specified single channel repeatedly. • Single sweep mode: A/D conversion is performed on the specified two channels for a single round. • Repeat sweep mode: A/D conversion is performed on the specified two channels repeatedly.
A/D conversion data register (× 2)	16-bit data register corresponding to each channel group where the A/D conversion result is stored (valid data length: 10 bits).
A/D conversion start conditions	• Software trigger • Conversion start trigger from timer RC • External trigger
Interrupt source	An A/D conversion interrupt is generated when A/D conversion completes.
Others	The A/D converter is set to standby by the MSTAD bit in the MSTCR register.

Note:
1. The symbol of the conversion clock ϕAD shown in Electrical Characteristics indicates the A/D conversion clock. Make sure the measurement condition is ϕAD = the A/D conversion clock.

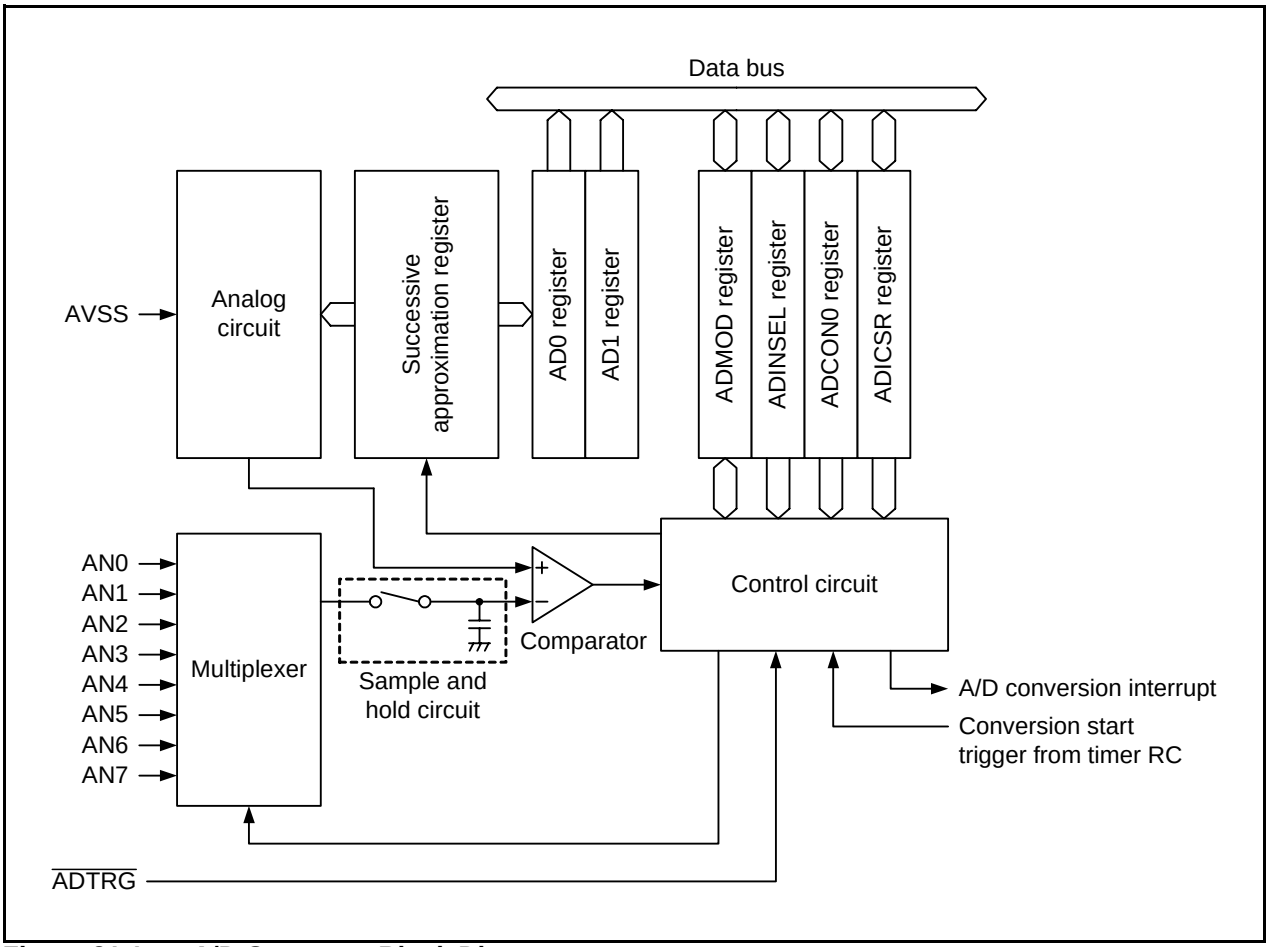


Figure 21.1 A/D Converter Block Diagram

Table 21.2 lists the A/D Converter Pin Configuration.
Pins AVCC and AVSS are used for the power supply to the analog block in the A/D converter.
The eight analog input pins are divided into four channel groups.

Table 21.2 A/D Converter Pin Configuration

Pin Name	Assigned Pin	I/O	Function
AVCC	VCC	I	Power supply input for the A/D converter
AVSS	VSS	I	
AN0	P1_0	I	Analog input for channel group 0
AN1	P1_1	I	
AN2	P1_2	I	Analog input for channel group 1
AN3	P1_3	I	
AN4	P1_4	I	Analog input for channel group 2
AN7	P1_7	I	
AN5	P1_5	I	Analog input for channel group 3
AN6	P1_6	I	
$\overline{\text{ADTRG}}$	P3_7, P4_5	I	External trigger input for starting A/D conversion

21.2 Registers

Table 21.3 lists the A/D Converter Register Configuration.

Table 21.3 A/D Converter Register Configuration

Register Name		Symbol	After Reset	Address	Access Size
A/D Register 0	Lower 8 bits	AD0L	XXh	00098h	8 or 16 (1)
	Higher 2 bits	AD0H	000000XXb	00099h	
A/D Register 1	Lower 8 bits	AD1L	XXh	0009Ah	8 or 16 (1)
	Higher 2 bits	AD1H	000000XXb	0009Bh	
A/D Mode Register		ADMOD	00h	0009Ch	8
A/D Input Select Register		ADINSEL	00h	0009Dh	8
A/D Control Register 0		ADCON0	00h	0009Eh	8
A/D Interrupt Control Status Register		ADICSR	00h	0009Fh	8

X: Undefined

Note:

1. For details on access, see the description of the individual registers.

21.2.1 A/D Register i (ADi) (i = 0 or 1)

Address 00098h (AD0L), 0009Ah (AD1L)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Address 00099h (AD0H), 0009Bh (AD1H)

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	X	X

Bit	Symbol	Function	R/W
b7 to b0	—	Lower 8 bits in the A/D conversion result	R
b8	—	Higher 2 bits in the A/D conversion result	R
b9	—		
b10	—	Nothing is assigned. The write value must be 0. The read value is 0.	—
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

ADi (i = 0 or 1) is a 16-bit read-only register that stores the A/D conversion results. It is divided into ADiL (lower) and ADiH (higher). Table 21.4 lists the Correspondence between Analog Input Channels and ADi Register.

When the higher 6 bits in the ADiH register are read, the value is 0. Access can be made in 8-bit or 16-bit units. To read the ADi register as 8-bit units, read the ADiL register first and then ADiH register. When the ADi register is read as 16-bit units, it is read twice in 8-bit units.

Table 21.4 Correspondence between Analog Input Channels and ADi Register

Analog Input Channel				A/D Data Register that Stores Conversion Result
Channel Group 0 (ADGSEL1 to ADGSEL0 = 00b)	Channel Group 1 (ADGSEL1 to ADGSEL0 = 01b)	Channel Group 2 (ADGSEL1 to ADGSEL0 = 10b)	Channel Group 3 (ADGSEL1 to ADGSEL0 = 11b)	
AN0	AN2	AN4	AN5	AD0 register
AN1	AN3	AN7	AN6	AD1 register

ADGSEL0 to ADGSEL1: Bits in ADINSEL register

21.2.2 A/D Mode Register (ADMOD)

Address 0009Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADCAP1	ADCAP0	—	MD1	MD0	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	A/D conversion clock select bits	b2 b1 b0 0 0 0: f8 0 0 1: f4 0 1 0: f2 0 1 1: f1 1 0 0: fAD Other than the above: Do not set.	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	MD0	A/D operating mode select bits	b4 b3 0 0: One-shot mode 0 1: Repeat mode 1 0: Single sweep mode 1 1: Repeat sweep mode	R/W
b4	MD1			R/W
b5	—	Reserved	Set to 0.	R/W
b6	ADCAP0	A/D conversion trigger select bits	b7 b6 0 0: A/D conversion start by external trigger is disabled 0 1: Do not set. 1 0: A/D conversion is started by conversion trigger from timer RC 1 1: A/D conversion is started by external trigger ($\overline{\text{ADTRG}}$)	R/W
b7	ADCAP1			R/W

The ADMOD register must be written only when A/D conversion is stopped.

Bits CKS0 to CKS2 (A/D conversion clock select bits)

These bits are used to select the clock for A/D conversion.

Bits ADCAP0 to ADCAP1 (A/D conversion trigger select bits)

These bits are used to select or disable the trigger for starting A/D conversion.
When using a software trigger, set bits ADCAP1 to ADCAP0 to a value other than 01b.

21.2.3 A/D Input Select Register (ADINSEL)

Address 0009Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADGSEL1	ADGSEL0	—	—	—	—	—	CH0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CH0	Channel select bit	See **Table 21.5 Channel Groups and A/D Converter Input Channels**.	R/W
b1	—	Reserved	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	—			
b6	ADGSEL0	A/D input group select bits	b7 b6 0 0: Channel group 0 (AN0, AN1) 0 1: Channel group 1 (AN2, AN3) 1 0: Channel group 2 (AN4, AN7) 1 1: Channel group 3 (AN5, AN6)	R/W
b7	ADGSEL1			R/W

The ADINSEL register must be written only when A/D conversion is stopped.

CH0 Bit (Channel select bit)

The input channel must be selected when the ADST bit in the ADCON0 register is 0 (A/D conversion stops).

Table 21.5 Channel Groups and A/D Converter Input Channels

	ADGSEL1 Bit	ADGSEL0 Bit	CH0 Bit	One-Shot Mode Repeat Mode	Single Sweep Mode Repeat Sweep Mode
Channel group 0	0	0	0	AN0	AN0, AN1
			1	AN1	
Channel group 1	0	1	0	AN2	AN2, AN3
			1	AN3	
Channel group 2	1	0	0	AN4	AN4, AN7
			1	AN7	
Channel group 3	1	1	0	AN5	AN5, AN6
			1	AN6	

21.2.4 A/D Control Register 0 (ADCON0)

Address 0009Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	ADST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADST	A/D conversion start bit	0: A/D conversion stops 1: A/D conversion starts	R/W
b1	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

The ADCON0 register is used to control A/D conversion operation.

ADST Bit (A/D conversion start bit)

[Conditions for setting to 0]
- When A/D conversion is completed in one-shot mode or single sweep mode.
- When 0 is written to this bit by software (A/D conversion stops).

[Conditions for setting to 1]
- When 1 is written to this bit by software (A/D conversion starts).
- When the A/D conversion start trigger enabled by the TRCADCR register is input.
- When an external trigger ($\overline{\text{ADTRG}}$) is input.

21.2.5 A/D Interrupt Control Status Register (ADICSR)

Address 0009Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ADF	ADIE	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	ADIE	A/D interrupt enable bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b7	ADF	A/D conversion complete flag	0: No interrupt requested 1: Interrupt requested	R/W (1)

Note:
1. Only 0 (no interrupt requested) can be written to the ADF bit.

ADF Bit (A/D conversion complete flag)

This bit indicates whether an A/D conversion interrupt is requested. It also indicates whether A/D conversion has completed.

[Conditions for setting to 0]
When 0 is written to this bit after reading it as 1.
[Conditions for setting to 1]
• When A/D conversion is completed in one-shot mode or single sweep mode.
• When A/D conversion is completed on all the selected channels in repeat mode or repeat sweep mode.

21.3 Operation

This A/D converter provides operating four modes: One-shot, repeat, single sweep, and repeat sweep modes. This converter is a successive approximation type with 10-bit resolution.
The operating mode, analog input channel, and A/D conversion clock should be switched while the ADST bit in the ADCON0 register is 0 (A/D conversion stops).

21.3.1 Items Common to Multiple Modes

21.3.1.1 Input Sampling and A/D Conversion Time

The A/D converter includes a sample and hold circuit. When the ADST bit in the ADCON0 register is set to 1 (A/D conversion is in progress), the A/D converter samples the input and starts conversion after the A/D conversion start delay time (tD) has elapsed.
Figure 21.2 shows the A/D Conversion Timing. Table 21.6 lists the A/D Conversion Time.
As shown in Figure 21.2, the A/D conversion time (tCONV) includes tD and the input sampling time (tSPL). Here, tD is determined by the timing for writing to the ADCON0 register and is not a fixed value. The conversion time, therefore, varies within the range shown in Table 21.6.
In one-shot mode and single sweep mode, the ADF bit in the ADICSR register is set to 1 during end processing time, and the last A/D conversion result is stored in the ADi register.

- In one-shot mode
  A/D conversion time (tCONV) + end processing time (tEND)
- When two channels are selected in single sweep mode
  A/D conversion time (tCONV) + A/D conversion time (tCONV with no start delay time (tD) included) + end processing time (tEND)

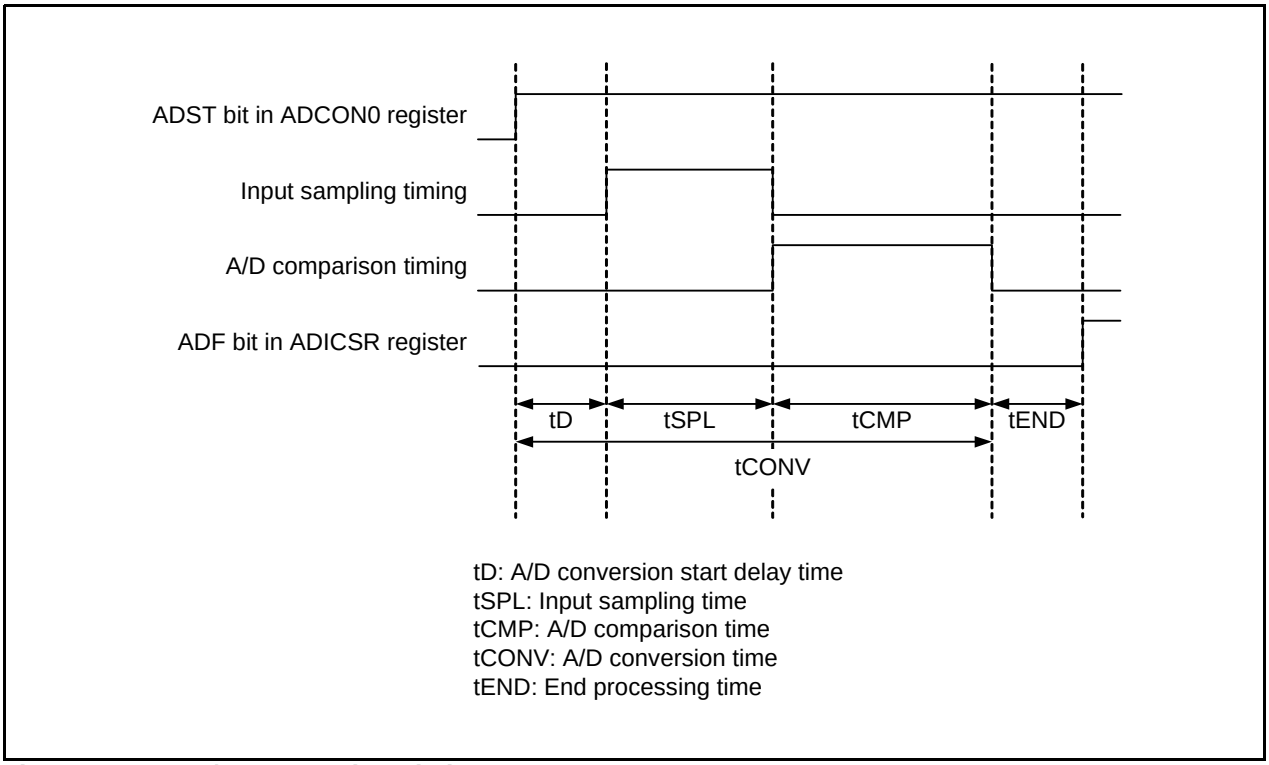


Figure 21.2 A/D Conversion Timing

Table 21.6 A/D Conversion Time

Item	Symbol	A/D Conversion Clock				
		f1	f2	f4	f8	fAD
		CKS0 = 1	CKS0 = 0	CKS0 = 1	CKS0 = 0	CKS0 = 0
		CKS1 = 1		CKS1 = 0		CKS1 = 0
		CKS2 = 0 (1)				CKS2 = 1 (2)
A/D conversion start delay time (3)	tD	3	3 to 4	3 to 6	3 to 10	3
Input sampling time	tSPL	16	31	61	121	16
A/D comparison time	tCMP	25	50	100	200	25
A/D conversion time	tCONV	44	84 to 85	164 to 167	324 to 331	44
End processing time	tEND	2 to 3 cycles of fAD				

CKS0, CKS1, CKS2: Bits in ADMOD register

Notes:
1. The numerical values in the table indicate the number of system clock (f) cycles.
2. The numerical values in the table indicate the number of fAD cycles.
3. In repeat mode, single sweep mode, and repeat sweep mode, there is no delay time during the A/D conversion time (tCONV) for the second and subsequent rounds.

21.3.1.2 External Trigger Input Timing

A/D conversion can also be started by an external trigger input. When bits ADCAP1 to ADCAP0 in the ADMOD register are 11b (A/D conversion is started by external trigger ($\overline{\text{ADTRG}}$)), an external trigger can be input to the $\overline{\text{ADTRG}}$ pin. The ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) on the rising edge of the $\overline{\text{ADTRG}}$ input pin and A/D conversion is started. Other operations are the same as when the ADST bit in the ADCON0 register set to 1 by software.

Figure 21.3 shows the External Trigger Input Timing.

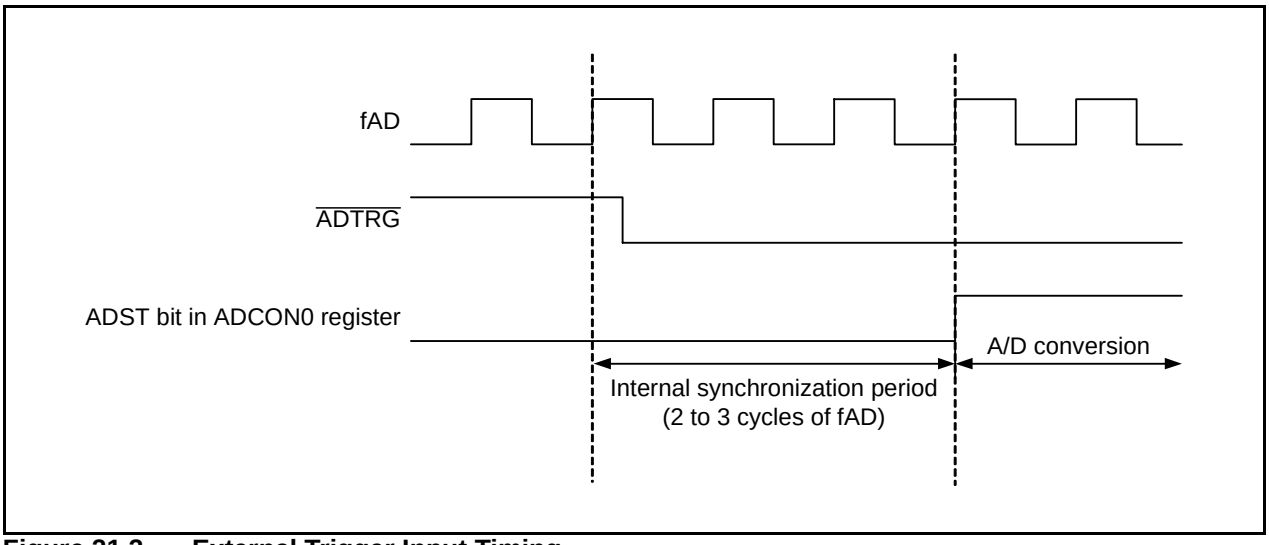


Figure 21.3 External Trigger Input Timing

21.3.2 One-Shot Mode

Figure 21.4 shows an Operation Example in One-Shot Mode When Channel 1 is Selected.
In one-shot mode, A/D conversion of an analog input is performed for the specified single channel a single time as follows:

(1) When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) by software trigger, timer RC trigger, or external trigger input, A/D conversion is started on the selected channel.
(2) When A/D conversion completes, the result is transferred to the ADi register (i = 0 or 1) corresponding to the channel.
(3) When A/D conversion completes, the ADF bit in the ADICSR register is set to 1 (interrupt requested). If the ADIE bit in the ADICSR register is 1 (A/D conversion interrupt enabled) at this time, an A/D conversion interrupt is generated.
Writing 0 after reading the value 1 sets the ADF bit to 0 (no interrupt requested).
(4) The ADST bit remains at 1 (A/D conversion starts) during A/D conversion. When conversion completes, the ADST bit is automatically set to 0 (A/D conversion stops) and the A/D converter enters the standby state. When the ADST bit is set to 0 during A/D conversion, A/D conversion is stopped and the A/D converter enters the standby state.

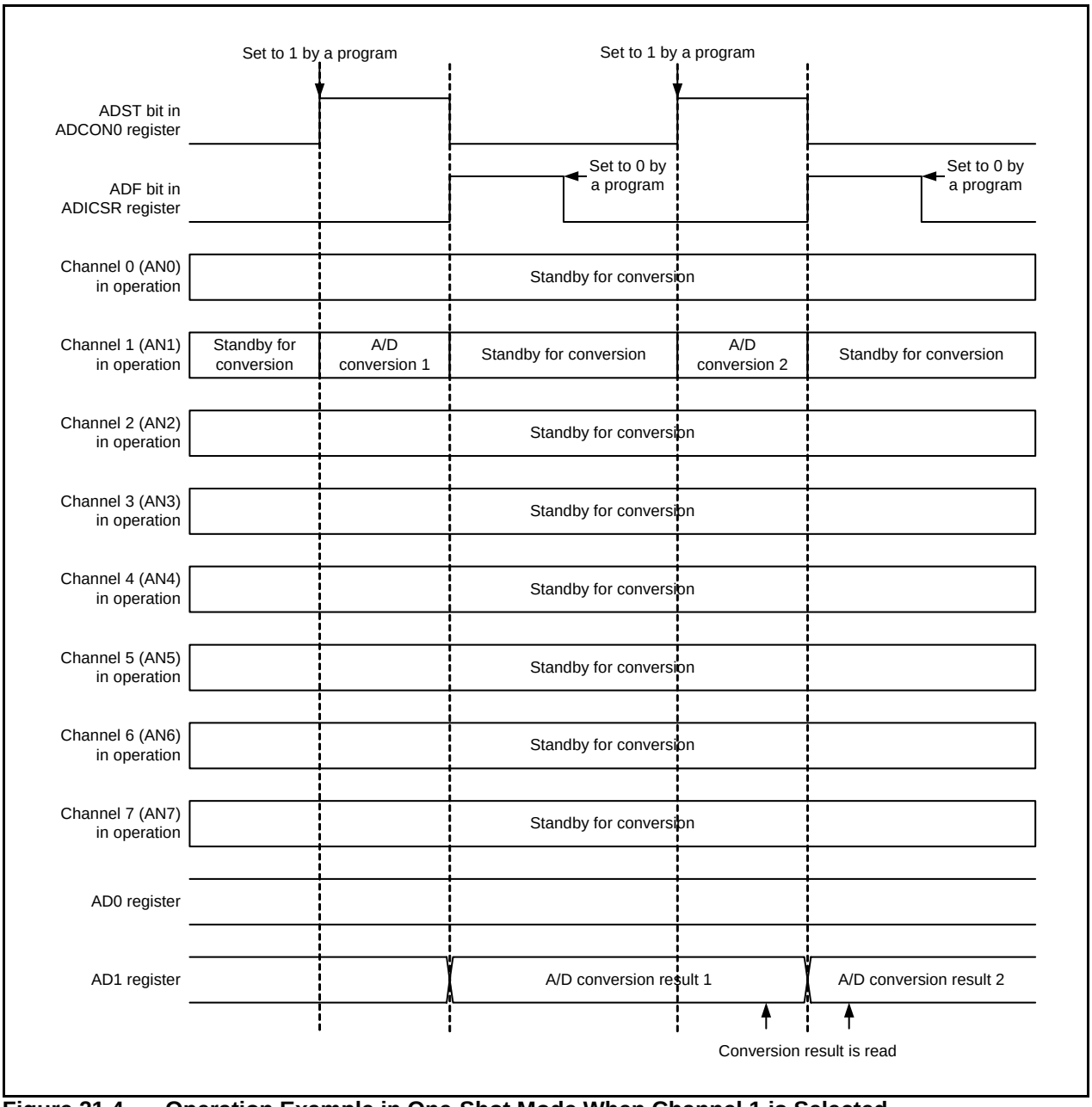
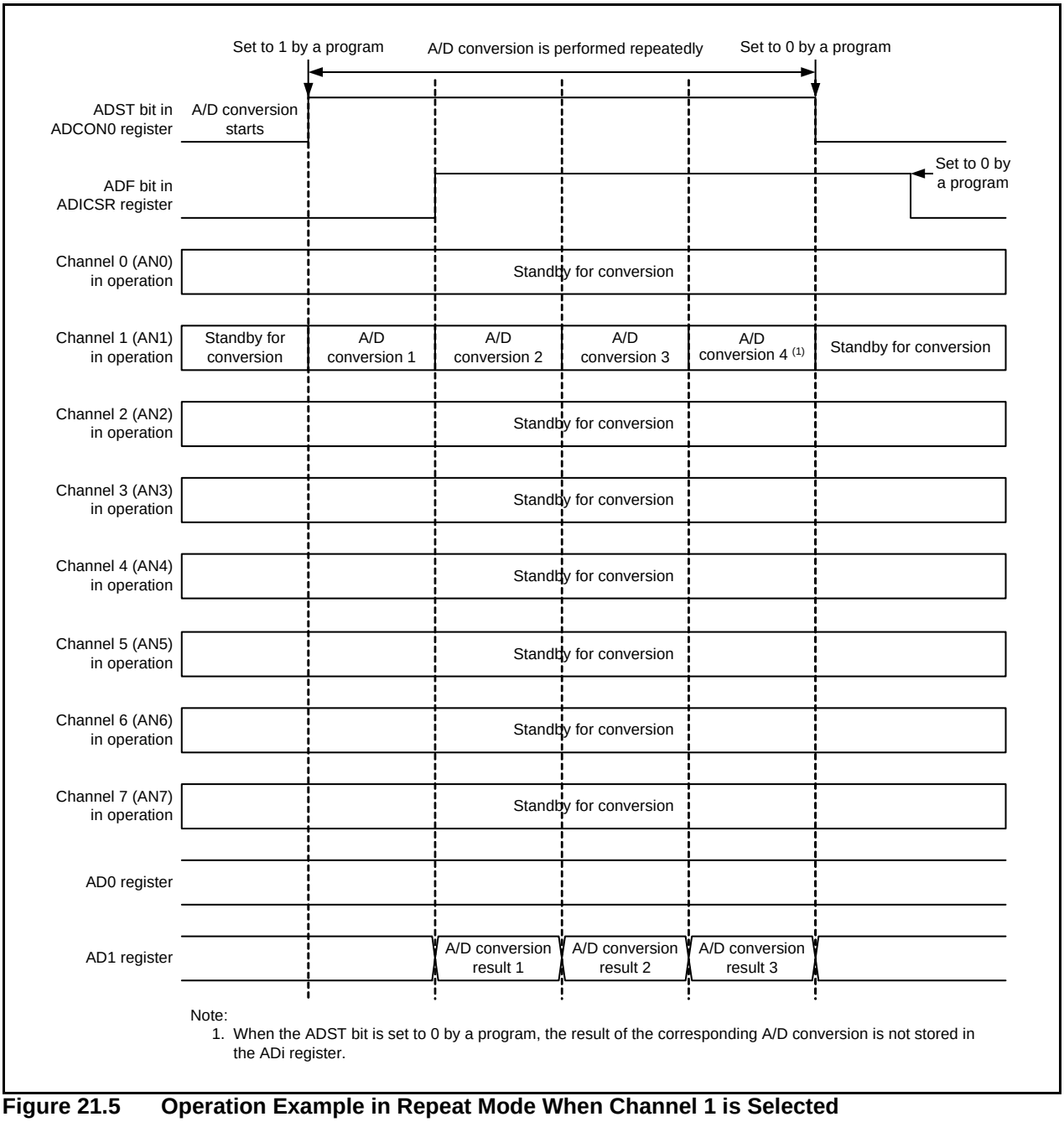


Figure 21.4 Operation Example in One-Shot Mode When Channel 1 is Selected

21.3.3 Repeat Mode

Figure 21.5 shows an Operation Example in Repeat Mode When Channel 1 is Selected.
In repeat mode, A/D conversions of an analog input are performed for the specified single channel repeatedly as follows:

(1) When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) by software trigger, timer RC trigger, or external trigger input, A/D conversion is started on the selected channel.
(2) When A/D conversion completes, the result is transferred to the ADi register (i = 0 or 1) corresponding to the channel.
(3) When A/D conversion completes, the ADF bit in the ADICSR register is set to 1 (interrupt requested). If the ADIE bit in the ADICSR register is 1 (A/D conversion interrupt enabled) at this time, an A/D conversion interrupt is generated.
Writing 0 after reading the value 1 sets the ADF bit to 0 (no interrupt requested).
(4) While the ADST bit is 1 (A/D conversion starts), steps between (2) and (3) are repeated. When the ADST bit is set to 0 (A/D conversion stops), A/D conversion is stopped and the A/D converter enters the standby state. Then, when the ADST bit is set to 1, A/D conversion is restarted on the selected channel.



Note:
1. When the ADST bit is set to 0 by a program, the result of the corresponding A/D conversion is not stored in the ADi register.

Figure 21.5 Operation Example in Repeat Mode When Channel 1 is Selected

21.3.4 Single Sweep Mode

Figure 21.6 shows an Operation Example in Single Sweep Mode When Channels 0 and 1 are Selected.
In single sweep mode, A/D conversions of the analog inputs are performed for the specified two channels a single time as follows:

(1) When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) by software trigger, timer RC trigger, or external trigger input, A/D conversion is started from AN0 when channel group 0 is selected, and AN2 when channel group 1 is selected. A/D conversion is started from AN0 when channel group 0 is selected, and AN2 when channel group 1 is selected. A/D conversion is started from AN4 when channel group 2 is selected, and AN5 when channel group 3 is selected.

(2) When A/D conversion has completed on each channel, the result is transferred to the corresponding ADi register (i = 0 or 1).

(3) When A/D conversion has completed on all the selected channels, the ADF bit in the ADICSR register is set to 1 (interrupt requested).
Writing 0 after reading the value 1 sets the ADF bit to 0 (no interrupt requested).

(4) The ADST bit remains at 1 (A/D conversion starts) during A/D conversion. When conversion has completed on all the selected channels, the ADST bit is automatically set to 0 (A/D conversion stops) and the A/D converter enters the standby state. When the ADST bit is set to 0 during A/D conversion, A/D conversion is stopped and the A/D converter enters the standby state.

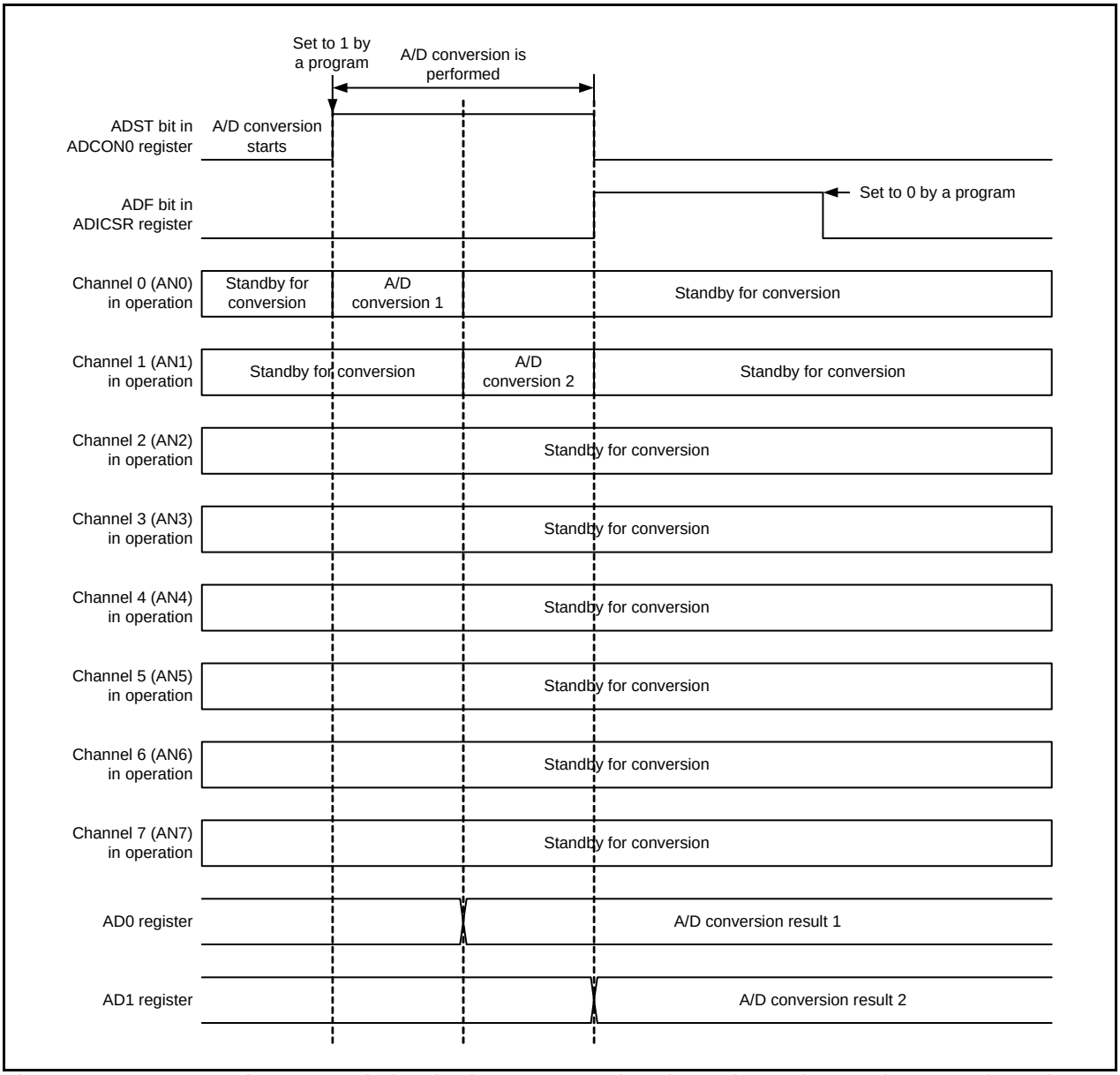


Figure 21.6 Operation Example in Single Sweep Mode When Channels 0 and 1 are Selected

21.3.5 Repeat Sweep Mode

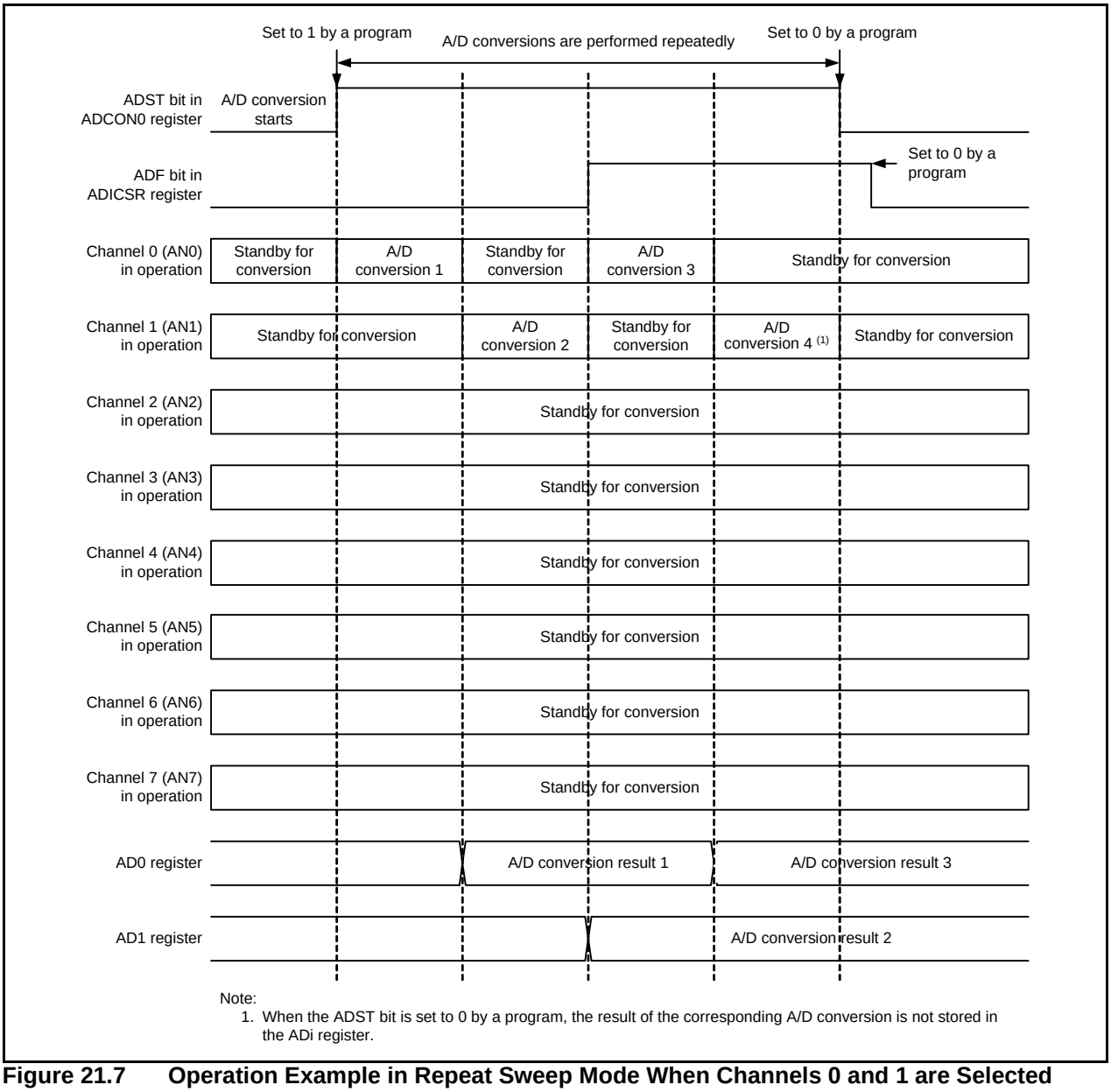
Figure 21.7 shows an Operation Example in Repeat Sweep Mode When Channels 0 and 1 are Selected.
In repeat sweep mode, A/D conversions of the analog inputs are performed for the specified two channels repeatedly as follows:

(1) When the ADST bit in the ADCON0 register is set to 1 (A/D conversion starts) by software trigger, timer RC trigger, or external trigger input, A/D conversion is started from AN0 when channel group 0 is selected, and AN2 when channel group 1 is selected. A/D conversion is started from AN4 when channel group 2 is selected, and AN5 when channel group 3 is selected.

(2) When A/D conversion has completed on each channel, the result is transferred to the corresponding ADi register (i = 0 or 1).

(3) When A/D conversion has completed on all the selected channels, the ADF bit in the ADICSR register is set to 1 (interrupt requested).
Writing 0 after reading the value 1 sets the ADF bit to 0 (no interrupt requested).

(4) While the ADST bit is 1 (A/D conversion starts), steps between (2) and (3) are repeated. When the ADST bit is set to 0 (A/D conversion stops), A/D conversion is stopped and the A/D converter enters the standby state. Then, when the ADST bit is set to 1, A/D conversion is restarted from AN0 when channel group 0 is selected, and AN2 when channel group 1 is selected. When channel group 2 is selected, A/D conversion is started from AN4.



Note:
1. When the ADST bit is set to 0 by a program, the result of the corresponding A/D conversion is not stored in the ADi register.

Figure 21.7 Operation Example in Repeat Sweep Mode When Channels 0 and 1 are Selected

21.4 A/D Converter Interrupt

Table 21.7 lists the A/D Converter Interrupt.
When A/D conversion completes, the ADF bit in the ADICSR register is set to 1 (interrupt requested). If the ADIE bit is 1 (interrupt enabled), an A/D conversion interrupt is generated.

Table 21.7 A/D Converter Interrupt

Interrupt Source	Interrupt Name	Interrupt Flag
Completion of A/D conversion	A/D conversion interrupt	The ADF bit in the ADICSR register

21.5 Notes on A/D Converter

21.5.1 A/D Converter Standby Setting

The A/D converter can be set to standby or active using the MSTAD bit in the MSTCR register.
Stop A/D conversion before setting to module standby. Register access is enabled by clearing the A/D converter standby state. For details, see **5. System Control**.

21.5.2 Sensor Output Impedance during A/D Conversion

To perform A/D conversion accurately, charging of the internal capacitor C shown in Figure 21.8 must be completed within the period of time specified as T (sampling time). Let the output impedance of the sensor equivalent circuit be R0, the internal resistance of the microcomputer be R, the accuracy (error) of the A/D converter be X, and the resolution of A/D converter be Y (Y is 1024 in 10-bit mode).

$$\text{VC is generally } VC = VIN\left\{1 - e^{-\frac{1}{C(R0+R)}t}\right\}$$

$$\text{And when } t = T,\ VC = VIN - \frac{X}{Y}VIN = VIN\left(1 - \frac{X}{Y}\right)$$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$$

$$\text{Hence, } R0 = -\frac{T}{C \bullet \ln\frac{X}{Y}} - R$$

Figure 21.8 shows the Analog Input Pin and External Sensor Equivalent Circuit. The user can obtain an impedance R0 that makes the pin-to-pin voltage VC increase from 0 to VIN – (0.1/1024) VIN within time T when the difference between VIN and VC becomes 0.1 LSB. The value, (0.1/1024) indicates a precondition for the calculation of R0 when the degradation due to insufficient capacitor charge is suppressed to 0.1 LSB during A/D conversion in 10-bit mode. The actual error, however, is the absolute accuracy plus 0.1 LSB.
A/D conversion clock = 20 MHz, T = 0.8 μs. Output impedance R0 through which an capacitor C is fully charged within T is obtained as follows:

T = 0.8 μs, R = 10 kΩ, C = 6.0 pF, X = 0.1, and Y = 1024. Hence,

$$R0 = -\frac{0.8 \times 10^{-6}}{6.0 \times 10^{-12} \bullet \ln\frac{0.1}{1024}} - 10 \times 10^{3} \approx 4.4 \times 10^{3}$$

Thus the maximum output impedance of a sensor circuit for an accuracy (error) of 0.1 LSB or less is 4.4 kΩ maximum.

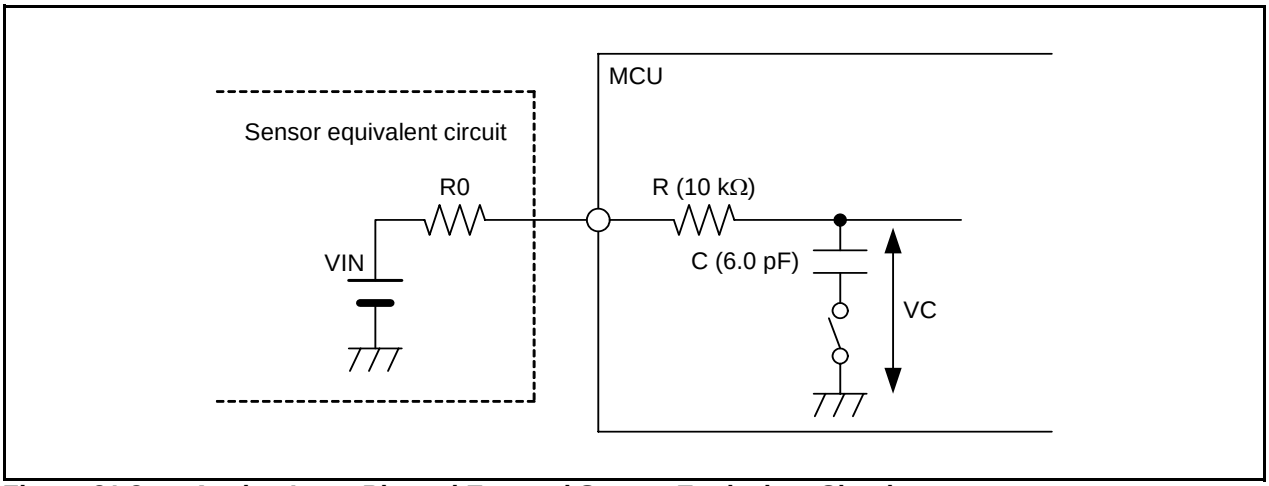


Figure 21.8 Analog Input Pin and External Sensor Equivalent Circuit

21.5.3 Register Setting

- Registers ADMOD and ADINSEL must be written only when A/D conversion is stopped.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion while the WCKSTP bit in the CKSTPR register is 1 (system clock is stopped in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory is stopped) or the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled) during A/D conversion.
- During A/D conversion, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion is stopped) by a program to forcibly terminate the conversion, the conversion result from the A/D converter will be undefined and no interrupt will be generated. The value of the ADi register (i = 0 or 1) which is not engaged in A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use any of the values of the ADi register.
- When using the A/D converter, it is recommended that the average of the conversion results be taken.

22. Comparator B

Comparator B consists of two independent comparators, B1 and B3, which compare an analog input voltage with a reference input voltage.

22.1 Overview

The comparison result between the reference input voltage and the analog input voltage can be read by software. Table 22.1 lists the Comparator B Specifications. Figure 22.1 shows the Comparator B Block Diagram. Table 22.2 lists the Comparator B Pin Configuration.

Table 22.1 Comparator B Specifications

Item	Specification	
Input voltage	Reference input	Input from the reference pin (IVREFi)
	Analog input	Input voltage from the analog pin (IVCMPi)
Comparison result	The result can be read from the WCBiOUT bit in the WCMPR register or monitored with the VCOUTi pin.	
Interrupt request generation timing	When the comparison result changes.	
Digital filter function	• The digital filter can be enabled or disabled. • The sampling frequency can be selected (f1, f8, or f32).	

i = 1 or 3

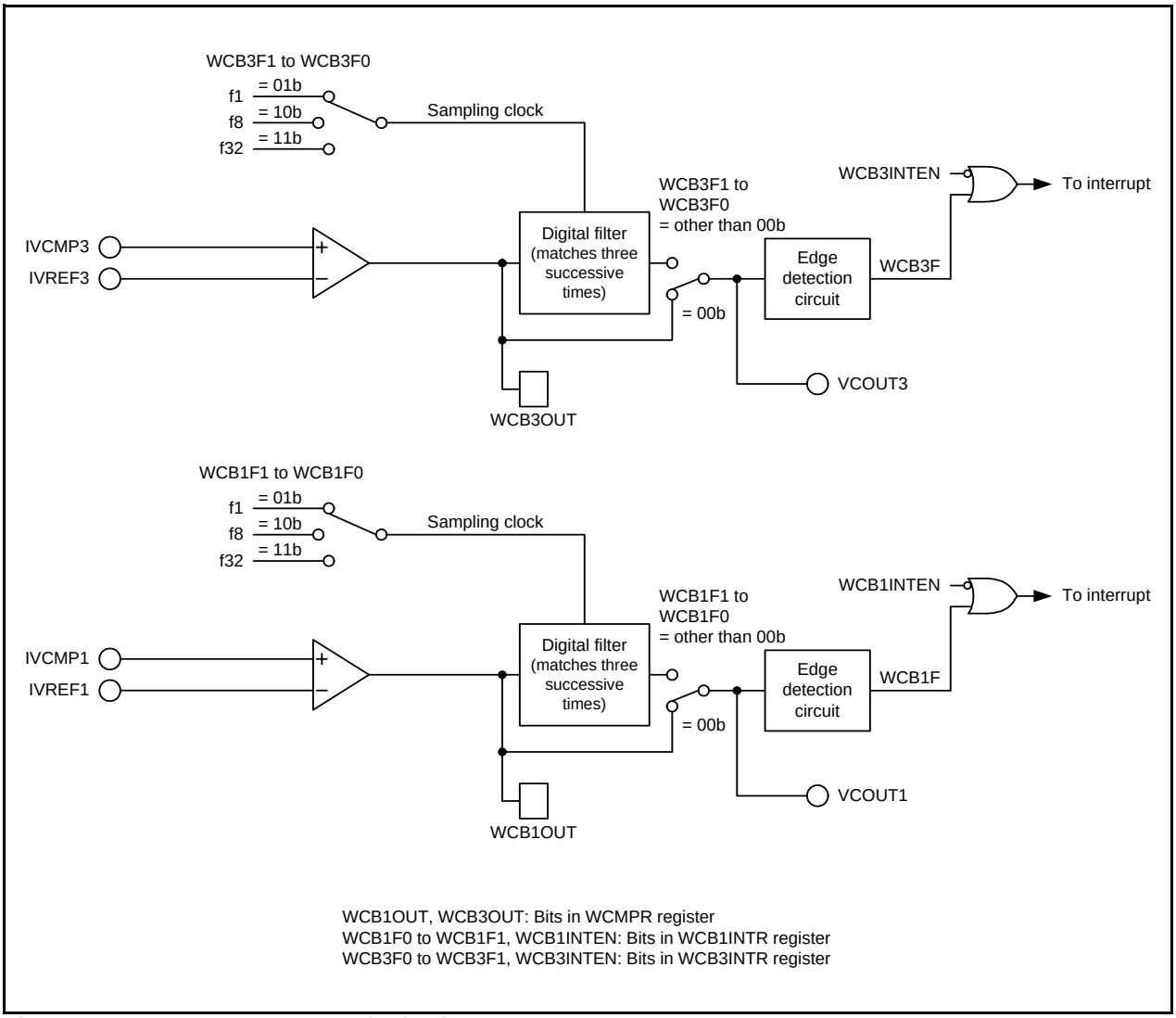


Figure 22.1 Comparator B Block Diagram

Table 22.2 Comparator B Pin Configuration

Pin Name	Assigned Pin	I/O	Function
IVCMP1	P1_7	I	Analog voltage input for comparator B1
IVREF1	P1_6	I	Reference voltage input for comparator B1
VCOUT1	P1_5	O	Comparison result output for comparator B1
IVCMP3	P3_3	I	Analog voltage input for comparator B3
IVREF3	P3_4	I	Reference voltage input for comparator B3
VCOUT3	P3_5	O	Comparison result output for comparator B3

Note:
1. When port P1_5 is set as the VCOUT1 pin while operation of comparator B1 is disabled (WCB1M0 = 0), the initial level of the pin is set to low. When port P3_5 is set as the VCOUT3 pin while operation of comparator B3 is disabled (WCB3M0 = 0), the initial level of the pin is set to low.

22.2 Registers

Table 22.3 lists the Comparator B Register Configuration.

Table 22.3 Comparator B Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Comparator B Control Register	WCMPR	00h	00180h	8
Comparator B1 Interrupt Control Register	WCB1INTR	00h	00181h	8
Comparator B3 Interrupt Control Register	WCB3INTR	00h	00182h	8

22.2.1 Comparator B Control Register (WCMPR)

Address 00180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WCB3OUT	—	—	WCB3M0	WCB1OUT	—	—	WCB1M0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	WCB1M0	Comparator B1 operation enable bit	0: Operation disabled 1: Operation enabled	R/W
b1	—	Reserved	Set to 0.	R/W
b2	—			
b3	WCB1OUT	Comparator B1 monitor flag	0: IVCMP1 < IVREF1 or comparator B1 disabled 1: IVCMP1 > IVREF1	R
b4	WCB3M0	Comparator B3 operation enable bit	0: Operation disabled 1: Operation enabled	R/W
b5	—	Reserved	Set to 0.	R/W
b6	—			
b7	WCB3OUT	Comparator B3 monitor flag	0: IVCMP3 < IVREF3 or comparator B3 disabled 1: IVCMP3 > IVREF3	R

22.2.2 Comparator B1 Interrupt Control Register (WCB1INTR)

Address 00181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WCB1F	WCB1INTEN	WCB1S1	WCB1S0	—	—	WCB1F1	WCB1F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	WCB1F0	Comparator B1 filter select bits	b1 b0 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b1	WCB1F1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	WCB1S0	Comparator B1 interrupt edge select bits	b5 b4 0 0: When the analog input voltage is lower than the reference input voltage 0 1: When the analog input voltage is higher than the reference input voltage 1 0: Do not set. 1 1: When the analog input voltage is lower or higher than the analog input voltage	R/W
b5	WCB1S1			R/W
b6	WCB1INTEN	Comparator B1 interrupt enable signal bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b7	WCB1F	Comparator B1 interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W

WCB1F Bit (Comparator B1 interrupt request flag)

[Condition for setting to 0]
• When 0 is written to this bit.
[Condition for setting to 1]
• When an interrupt request is generated.

22.2.3 Comparator B3 Interrupt Control Register (WCB3INTR)

Address 00182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WCB3F	WCB3INTEN	WCB3S1	WCB3S0	—	—	WCB3F1	WCB3F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	WCB3F0	Comparator B3 filter select bits	b1 b0 0 0: No filter 0 1: Filter sampled at f1 1 0: Filter sampled at f8 1 1: Filter sampled at f32	R/W
b1	WCB3F1			R/W
b2	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b3	—			
b4	WCB3S0	Comparator B3 interrupt edge select bits	b5 b4 0 0: When the analog input voltage is lower than the reference input voltage 0 1: When the analog input voltage is higher than the reference input voltage 1 0: Do not set. 1 1: When the analog input voltage is lower or higher than the analog input voltage	R/W
b5	WCB3S1			R/W
b6	WCB3INTEN	Comparator B3 interrupt enable signal bit	0: Interrupt disabled 1: Interrupt enabled	R/W
b7	WCB3F	Comparator B3 interrupt request flag	0: No interrupt requested 1: Interrupt requested	R/W

WCB3F Bit (Comparator B3 interrupt request flag)

[Condition for setting to 0]
• When 0 is written to this bit.
[Condition for setting to 1]
• When an interrupt request is generated.

22.3 Operation

Comparator B1 and comparator B3 compare an input voltage from the reference voltage input pin (IVREFi) and an input voltage from the analog input voltage pin (IVCMPi) (i = 1 or 3).

22.3.1 Comparator Bi Digital Filter (i = 1 or 3)

In comparator Bi, the digital filter can be used. The sampling clock can be selected by bits WCBiF0 to WCBiF1 in the WCBiINTR register. The WCBiOUT signal output from comparator Bi is sampled on every sampling clock. When the level matches three successive times, the WCBiF bit in the WCBiINTR register is set to 1 (interrupt requested).
Figure 22.2 shows an Example of Comparator Bi Digital Filter Operation.

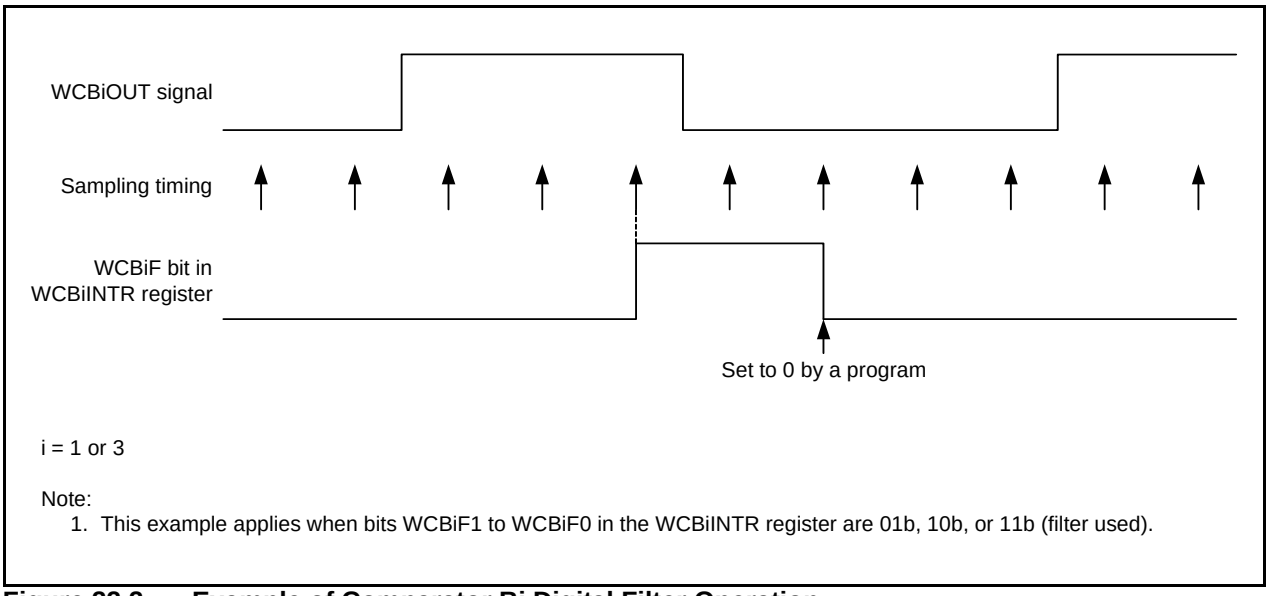


Figure 22.2 Example of Comparator Bi Digital Filter Operation

22.3.2 Comparator Bi (i = 1 or 3) Setting Procedure and Operation Example

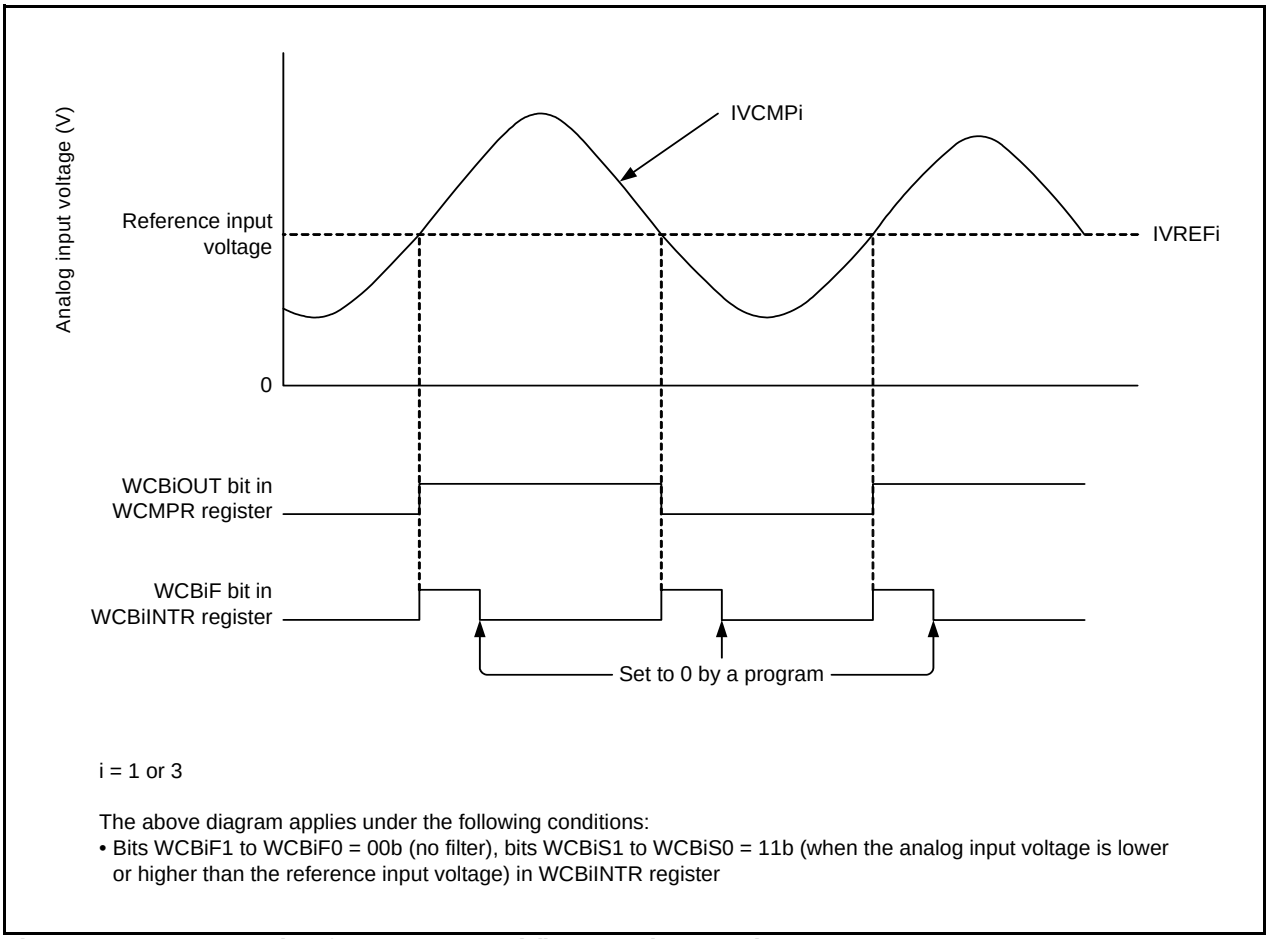
Comparator B1 and comparator B3 operate independently of each other.
Table 22.4 lists the Procedure for Setting Registers Associated with Comparator B.

Table 22.4 Procedure for Setting Registers Associated with Comparator B

Step	Register	Bit	Setting Value
1	Select the functions of pins IVCMPi and IVREFi. For the settings, see **12. I/O Ports**.		
2	WCBiINTR	WCBiF1 to WCBiF0	• Enable or disable the digital filter. • Select the sampling frequency.
3	WCMPR	WCB1M0	1 (operation enabled)
		WCB3M0	
4	Wait for the comparator stabilization time (100 μs max.).		
5	ILVL2	ILVL21 to ILVL20	When an interrupt is used: Select the interrupt priority level for comparator B1.
		ILVL25 to ILVL24	When an interrupt is used: Select the interrupt priority level for comparator B3.
6	WCBiINTR	WCBiS1 to WCBiS0	When an interrupt is used: Select the input polarity.
7	WCBiINTR	WCBiF	0 (no interrupt requested)
8	WCBiINTR	WCBiINTEN	When an interrupt is used: 1 (interrupt enabled)

i = 1 or 3

Figure 22.3 shows an Example of Comparator Bi (i = 1 or 3) Operation.
When the analog input voltage is higher than the reference input voltage, the WCBiOUT bit in the WCMPR register is set to 1. When the analog input voltage is lower than the reference input voltage, the WCBiOUT bit is set to 0.
When a comparator Bi interrupt (i = 1 or 3) is used, set the WCBiINTEN bit in the WCBiINTR register to 1 (interrupt enabled). If the comparison result changes at this time, a comparator Bi interrupt request is generated. For details on interrupts, see **11. Interrupts**.



i = 1 or 3

The above diagram applies under the following conditions:
- Bits WCBiF1 to WCBiF0 = 00b (no filter), bits WCBiS1 to WCBiS0 = 11b (when the analog input voltage is lower or higher than the reference input voltage) in WCBiINTR register

Figure 22.3 Example of Comparator Bi (i = 1 or 3) Operation

23. Flash Memory

The flash memory supports two rewrite modes: CPU rewrite mode and standard serial I/O mode.

23.1 Overview

Table 23.1 lists the Flash Memory Specifications (see **Tables 1.1** and **1.2 Specifications** for items not listed in Table 23.1). Table 23.2 outlines Flash Memory Rewrite Mode.

Table 23.1 Flash Memory Specifications

Item		Specification
Flash memory operating modes		2 modes (CPU rewrite and standard serial I/O modes)
Erase block division		See **Figure 23.1 Flash Memory Block Diagram**.
Programming method		Byte units
Erase method		Block erase
Program/erase control method (1)		Program/erase control by software commands
Rewrite control method	Blocks 1 to 3 (program ROM) (2)	Rewrite protect control in block units by lock bits
	Blocks A and B (data flash)	Individual rewrite control on blocks A and B by bits FMR16 to FMR17 in the FMR1 register
Number of commands		6 commands
Program/erase endurance (3)	Blocks 1 to 3 (program ROM) (2)	10,000 times
	Blocks A and B (data flash)	
ID code check function (4)		Standard serial I/O mode supported

Notes:
1. When programming/erasing the program ROM and the data flash, use a VCC supply voltage in the range of 1.8 V to 5.5 V.
2. The number of blocks and their division differ depending on products. For details, see **Figure 23.1 Flash Memory Block Diagram**.
3. Definition of program/erase endurance
   The number of program/erase cycles is defined on a per-block basis.
   If the number of cycles is 10,000, each block can be erased 10,000 times.
   For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. When rewrites are performed 100 or more times, the actual erase count can be reduced by executing program operations in such a way that all blank areas are used up before performing an erase operation. Avoid rewriting only particular blocks and average out the number of programming/erasure of the blocks. It is also advisable to retain data on the number of erasure of each block and limit the number to a certain extent.
4. For details on the ID code check function, see **23.3 ID Code Check Function**.

Table 23.2 Flash Memory Rewrite Mode

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode
Function	The user ROM area is rewritten by executing software commands from the CPU.	The user ROM area is rewritten using a dedicated serial programmer.
Rewritable area	User ROM	User ROM
Rewrite programs	User program	Standard boot program

23.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved).
Figure 23.1 shows the Flash Memory Block Diagram.
The user ROM area contains program ROM and data flash.
• Program ROM: Flash memory mainly used for storing programs
• Data flash: Flash memory mainly used for storing data to be rewritten
The user ROM area is divided into several blocks.
The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area when the MCU is shipped. The boot ROM area is allocated separately from the user ROM area.

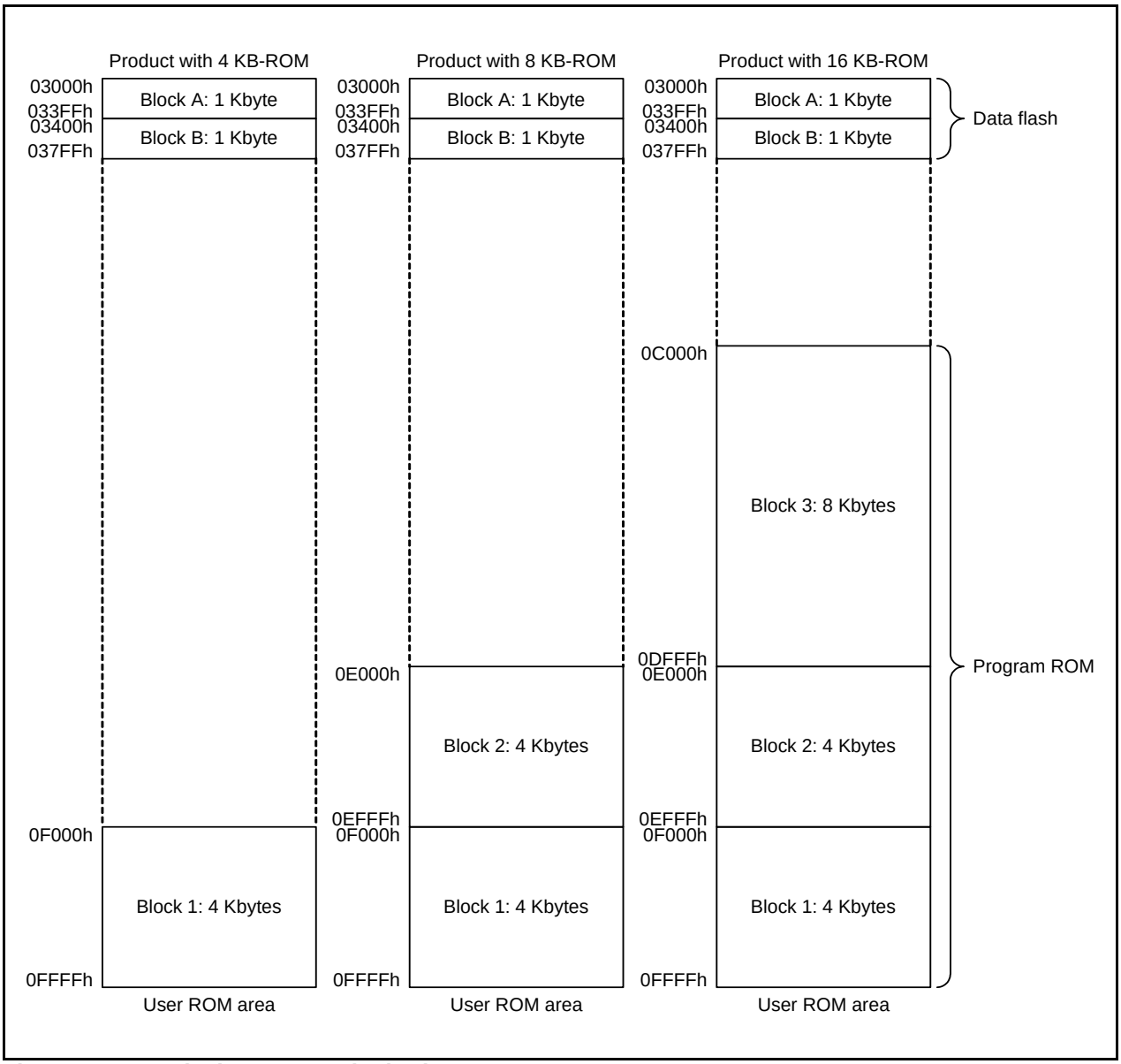


Figure 23.1 Flash Memory Block Diagram

23.3 ID Code Check Function

The ID code check function prevents the flash memory from being read, rewritten, or erased when standard serial I/O mode is used. This function is implemented by checking the ID codes written in the ID code area.
The ID code area is assigned to certain of the highest addresses for each vector in the fixed vector table, 0FFDFh, 0FFE3h, 0FFEBh, 0FFEFh, 0FFF3h, 0FFF7h, and 0FFFBh. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Figure 23.2 shows the ID Code Area.

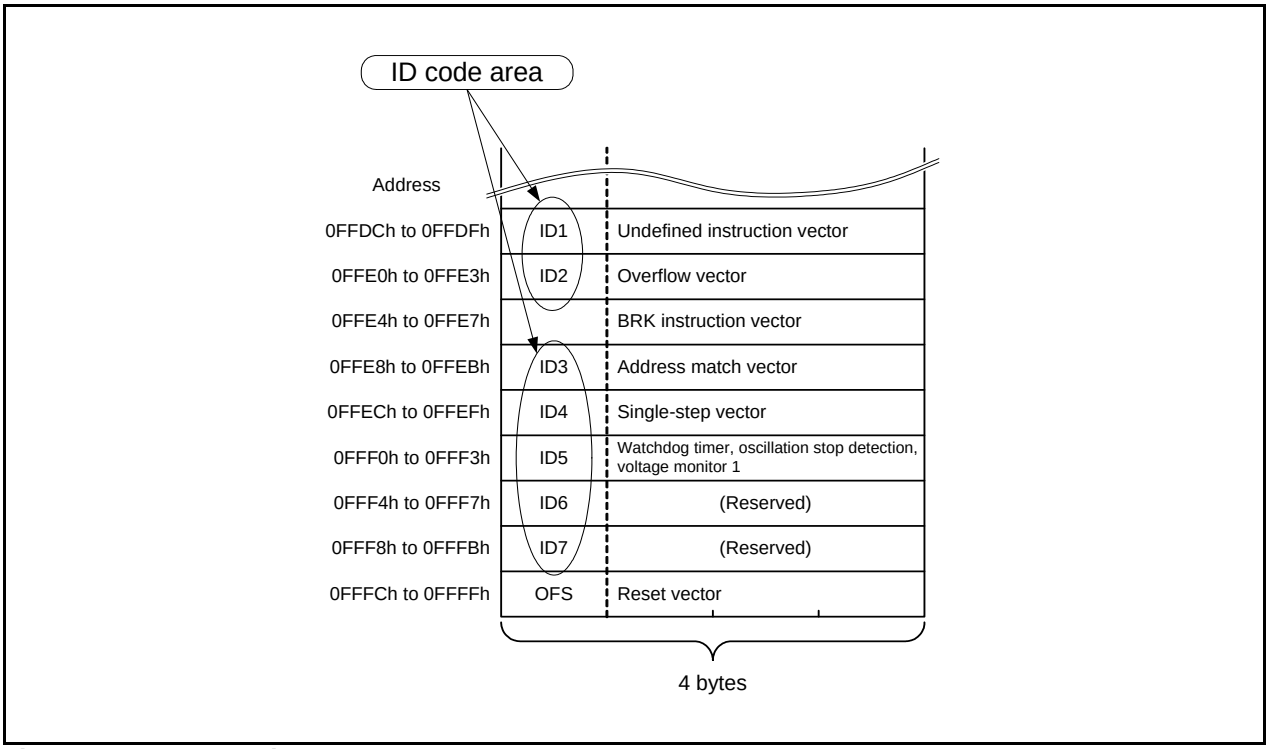


Figure 23.2 ID Code Area

23.3.1 Operation

The ID code check function is used in standard serial I/O mode. Its operation differs depending on whether the three bytes in the reset vector at addresses 0FFFCh to 0FFFEh are FFFFFFh or not.
If the value is FFFFFFh, the ID codes are not examined and all commands are accepted.
If the value is not FFFFFFh, the ID codes stored in the ID code area (stored ID code) and those sent from the serial programmer or the on-chip debugging emulator are examined to see whether they match. If they match, the commands are accepted. Otherwise, the commands are not accepted. To use the serial programmer or the on-chip debugging emulator, write predetermined ID codes, in advance, to the ID code area. In addition to the reserved word (see **23.3.2 Reserved Words**), any ID codes can be used.

The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

23.3.2 Reserved Words

The ID code with the character combination “ALeRASE” in ASCII is the reserved word for the forced erase function. The ID code “Protect” is the reserved word for the standard serial I/O mode disabled function. Table 23.3 lists the ID Code Reserved Words. When the combination of ID codes and addresses match those listed in Table 23.3, respectively, the ID codes forms the reserved word. When the forced erase function or standard serial I/O mode disabled function is not used, use another combination of ID codes.

Table 23.3 ID Code Reserved Words

ID Code Storage Address		Reserved Word of ID Code (ASCII) (1)	
		ALeRASE (forced erase function)	Protect (standard serial I/O mode disabled function)
0FFDFh	ID1	41h: A (upper-case)	50h: P (upper-case)
0FFE3h	ID2	4Ch: L (upper-case)	72h: r (lower-case)
0FFEBh	ID3	65h: e (lower-case)	6Fh: o (lower-case)
0FFEFh	ID4	52h: R (upper-case)	74h: t (lower-case)
0FFF3h	ID5	41h: A (upper-case)	65h: e (lower-case)
0FFF7h	ID6	53h: S (upper-case)	63h: c (lower-case)
0FFFBh	ID7	45h: E (upper-case)	74h: t (lower-case)

Note:
1. When the combination of ID codes and addresses match those listed in Table 23.3 respectively, the set of characters forms the corresponding reserved word.

23.3.2.1 Forced Erase Function

This function is used in standard serial I/O mode. When the sent ID codes are “ALeRASE” in ASCII and the stored ID codes are the same, the entire data in the user ROM area will be erased (forced erase). Even if the stored ID codes are other than “ALeRASE” (see **Table 23.3 ID Code Reserved Words**), the entire data in the user ROM area will be erased if bits ROMCP1 to ROMCR in the OFS register are any value other than 01b (ROM code protect disabled). If the stored ID codes are any value other than “ALeRASE” (see **Table 23.3 ID Code Reserved Words**) and when bits ROMCP1 to ROMCR in the OFS register are 01b (ROM code protect enabled), a forced erase is not performed and the ID codes are examined with the ID code check function.
Table 23.4 lists the Conditions and Operations of Forced Erase Function.

Also, when the stored ID codes are set to “ALeRASE” in ASCII, if the sent ID codes are “ALeRASE”, the data in the user ROM area will be erased. If the sent ID codes are any value other than “ALeRASE”, the ID codes do not match and no command is accepted, thus the user ROM area remains protected.

Table 23.4 Conditions and Operations of Forced Erase Function

Condition			Operation
ID Code from Serial Programmer or On-Chip Debugging Emulator	ID Code in ID Code Storage Address	Bits ROMCP1 to ROMCR in OFS Register	
ALeRASE	ALeRASE	—	Erasure of the whole user ROM area (forced erase function)
	Other than ALeRASE (1)	Other than 01b (ROM code protect disabled)	
		01b (ROM code protect enabled)	ID code examination (ID code check function)
Other than ALeRASE	ALeRASE	—	ID code examination (ID code check function. No ID code match.)
	Other than ALeRASE (1)	—	ID code examination (ID code check function)

Note:
1. See **23.3.2.2 Standard Serial I/O Mode Disabled Function** for the case where the ID codes are “Protect”.

23.3.2.2 Standard Serial I/O Mode Disabled Function

This function is used in standard serial I/O mode. When the stored ID codes are “Protect” in ASCII (see **Table 23.3 ID Code Reserved Words**), no communication with the serial programmer or the on-chip debugging emulator is performed. This prevents the flash memory from being read, written, or erased using the serial programmer or the on-chip debugging emulator.

If the stored ID codes are set to “Protect” in ASCII when bits ROMCP1 to ROMCR in the OFS register are 01b (ROM code protect enabled), ROM code protection cannot be disabled using the serial programmer or the on-chip debugging emulator. This prevents the flash memory from being read, written, or erased using the serial programmer or the on-chip debugging emulator.

23.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly with the MCU mounted on a board without using a ROM programmer. Software commands should be executed only for blocks in the user ROM area.
The MCU has a suspend function (program-suspend, erase-suspend) which halts erase or program operation temporarily in CPU rewrite mode. During suspend, the flash memory can be read and the read lock bit status command can be sent. For erase-suspend only, the flash memory can be programmed and the read lock bit status is enabled. For program-suspend only, the read lock bit status of the flash memory is enabled.
Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode.
Table 23.5 lists the Differences between EW0 Mode and EW1 Mode.

Table 23.5 Differences between EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	User mode	User mode
Area where rewrite control program can be allocated	User ROM	User ROM
Areas where rewrite control program can be executed	RAM (The rewrite control program must be transferred before being executed.)	User ROM or RAM
Rewritable area	User ROM	User ROM (Other than blocks which contain the rewrite control program.)
Software command restrictions	—	Program and block erase commands cannot be executed to any block which contains the rewrite control program.
Mode after programming or block erasure or after entering suspend	Read array mode	Read array mode
CPU state during programming/block erase	The CPU operates.	The CPU is put in the hold state. (I/O ports retain the states before the command is executed.)
Flash memory status detection	Read bits FST2 to FST7 in the FST register by a program.	Read bits FST2 to FST7 in the FST register by a program.
Conditions for entering erase/program-suspend	• Set bits FMR20 to FMR21 in the FMR2 register to 1 by a program. • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.	Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.
CPU clock	Max. 20 MHz	Max. 20 MHz

23.5 Registers (CPU Rewrite Mode)

Table 23.6 lists the Flash Memory Register Configuration.

Table 23.6 Flash Memory Register Configuration

Register Name	Symbol	After Reset	Address	Access Size
Flash Memory Status Register	FST	10000000b	001A9h	8
Flash Memory Control Register 0	FMR0	00h	001AAh	8
Flash Memory Control Register 1	FMR1	00h	001ABh	8
Flash Memory Control Register 2	FMR2	00h	001ACh	8
Flash Memory Refresh Control Register	FREFR	00h	001ADh	8

23.5.1 Flash Memory Status Register (FST)

Address 001A9h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FST7	FST6	FST5	FST4	FST3	FST2	BSYAEI	RDYSTI
After Reset	1	0	0	0	0	X	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RDYSTI	Flash ready status interrupt request flag (1, 4)	0: No flash ready status interrupt requested 1: Flash ready status interrupt requested	R/W
b1	BSYAEI	Flash access error interrupt request flag (2, 4)	0: No flash access error interrupt requested 1: Flash access error interrupt requested	R/W
b2	FST2	LBDATA monitor flag	0: Locked 1: Not locked	R
b3	FST3	Program-suspend status flag	0: Program not suspended 1: Program suspended	R
b4	FST4	Program error status flag (3)	0: No program error 1: Program error	R
b5	FST5	Erase error/blank check error status flag (3)	0: No erase error/blank check error 1: Erase error/blank check error	R
b6	FST6	Erase-suspend status flag	0: Erase not suspended 1: Erase suspended	R
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

Notes:
1. The RDYSTI bit cannot be set to 1 (flash ready status interrupt requested) by a program.
   Read this bit (dummy read) before writing 0 (no flash ready status interrupt requested) to the RDYSTI bit.
   To check this bit, set the RDYSTIE bit in the FMR0 register to 1 (flash ready status interrupt enabled).
2. The BSYAEI bit cannot be set to 1 (flash access error interrupt requested) by a program.
   Read this bit (dummy read) before writing 0 (no flash access error interrupt requested) to the BSYAEI bit.
   To check this bit, set the BSYAEIE bit in the FMR0 register to 1 (flash access error interrupt enabled) or set the CMDERIE bit in the FMR0 register to 1 (erase/write error interrupt enabled).
3. This bit is also set to 1 (error) when a command sequence error occurs.
4. When this bit is 1, do not set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).

RDYSTI Bit (Flash ready status interrupt request flag)

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled) and auto-programming or auto-erase completes, or suspend mode is entered, the RDYSTI bit is set to 1 (flash ready status interrupt requested).
During interrupt handling, set the RDYSTI bit to 0 (no flash ready status interrupt requested).

[Condition for setting to 0]
• When 0 is written to this bit after reading it as 1.
[Condition for setting to 1]
• If the flash memory status transits from busy to ready when the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt request enabled).

The status changes from busy to ready in the following states:
• Completion of programming/erasing the flash memory
• Suspend acknowledgement
• Completion of forced termination
• Completion of the lock bit program
• Completion of the read lock bit status
• Completion of the block blank check
• When the flash memory can be read after it has been activated from disabling flash memory stop.

BSYAEI Bit (Flash access error interrupt request flag)

The BSYAEI bit is set to 1 (flash access error interrupt requested) if the user ROM area is read or written while the flash memory is busy when the BSYAEIE bit in the FMR0 register is 1 (flash access error interrupt enabled). The BSYAEI bit is also set to 1 if a block erase error, program error, block blank check error, command sequence error, or lock bit program error occurs when the CMDERIE bit in the FMR0 register is 1 (interrupt enabled).
During interrupt handling, set the BSYAEI bit to 0 (no flash access error interrupt requested).

[Conditions for setting to 0]
(1) When 0 is written to this bit after reading it as 1.
(2) When the clear status register command is executed.
[Conditions for setting to 1]
(1) If the user ROM area is read or written while the flash memory is busy when the BSYAEIE bit in the FMR0 register is 1 (flash access error interrupt enabled).
(Note that the read value is undefined. Writing has no effect.)
(2) If a block erase error, program error, block blank check error, command sequence error, or lock bit program error occurs when the CMDERIE bit in the FMR0 register is 1 (interrupt enabled).

FST2 Bit (LBDATA monitor flag)

This is a read-only bit indicating the lock bit status. To confirm the lock bit status, execute the read lock bit status command and then read the FST2 bit after the FST7 bit is set to 1 (ready).
This bit is updated when the program, erase, and read lock bit status commands are generated. When the read lock bit status command is input, the FST7 bit is set to 0 (busy). When the FST7 bit is set to 1 (ready), the lock bit status is stored in the FST2 bit. The data in the FST2 bit is retained until the next command is input.

FST3 Bit (Program-suspend status flag)

This is a read-only bit indicating the suspend status. This bit is set to 1 when a program-suspend request is acknowledged and a program-suspend status is entered; otherwise it is set to 0.

FST4 Bit (Program error status flag)

This is a read-only bit indicating the auto-programming status. The bit is set to 1 if a program error occurs; otherwise it is set to 0. For details, see the description in **23.6.7 Full Status Check**.

FST5 Bit (Erase error/blank check error status flag)

This is a read-only bit indicating the status of auto-erase or block blank check command. The bit is set to 1 if an erase error or blank check error occurs; otherwise it is set to 0. For details, see the description in **23.6.7 Full Status Check**.

FST6 Bit (Erase-suspend status flag)

This is a read-only bit indicating the suspend status. This bit is set to 1 when an erase-suspend request is acknowledged and an erase-suspend status is entered; otherwise it is set to 0.

FST7 Bit (Ready/busy status flag)

When the FST7 bit is set to 0 (busy), the flash memory is in one of the following states:
- During programming
- During erasure
- During the lock bit program
- During the read lock bit status
- During the block blank check
- During forced stop operation
- The flash memory is being stopped
- The flash memory is being activated

Otherwise, the FST7 bit is set to 1 (ready).

23.5.2 Flash Memory Control Register 0 (FMR0)

Address 001AAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RDYSTIE	BSYAEIE	CMDERIE	CMDRST	FMSTP	FMR02	FMR01	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	FMR01	CPU rewrite mode select bit (1, 4)	0: CPU rewrite mode disabled 1: CPU rewrite mode enabled	R/W
b2	FMR02	EW1 mode select bit (1, 5)	0: EW0 mode 1: EW1 mode	R/W
b3	FMSTP	Flash memory stop bit (2)	0: Flash memory operates 1: Flash memory is stopped	R/W
b4	CMDRST	Erase/write sequence reset bit (3)	0: No erase/write sequence reset 1: Erase/write sequence reset	R/W
b5	CMDERIE	Erase/write error, blank check error, command sequence error interrupt enable bit	Erase/write error, blank check error, command sequence error 0: Interrupt disabled 1: Interrupt enabled	R/W
b6	BSYAEIE	Flash access error interrupt enable bit (5)	0: Flash access error interrupt disabled 1: Flash access error interrupt enabled	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit (5)	0: Flash ready status interrupt disabled 1: Flash ready status interrupt enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then write 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
2. Only write to the FMSTP bit by a program transferred to the RAM. The FMSTP bit is enabled when the FMR01 bit is 1 (CPU rewrite mode enabled). Set the FMSTP bit to 1 (flash memory is stopped) when the FST7 bit in the FST register is 1 (ready).
3. The CMDRST bit can be set when the FMR01 bit is 1 (CPU rewrite mode enabled) and the FST7 bit in the FST register is 0 (busy).
4. Set the FMR01 bit to 0 (CPU rewrite mode disabled) only when the RDYSTI bit in the FST register is 0 (no flash ready status interrupt requested) and the BSYAEI bit is 0 (no flash access error interrupt requested).
5. This bit is set to 0 when the FMR01 bit is 0 (CPU rewrite mode disabled).

FMR01 Bit (CPU rewrite mode select bit)

When the FMR01 bit is set to 1 (CPU rewrite mode enabled), the MCU is made ready to accept software commands.

FMR02 Bit (EW1 mode select bit)

When the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected.

FMSTP Bit (Flash memory stop bit)

This bit is used to initialize the control circuits and to reduce the amount of current consumed in the flash memory. When the FMSTP bit is set to 1 (flash memory is stopped), the flash memory cannot be accessed. Therefore, only write to the FMSTP bit by a program transferred to the RAM.

To reduce the power consumption further in low-speed clock mode (XIN clock is stopped), high-speed on-chip oscillator mode, and low-speed on-chip oscillator mode (XIN clock is stopped), set the FMSTP bit to 1 (flash memory is stopped). Do not set the FMSTP bit in the FMR0 register to 1 (flash memory is stopped) during A/D conversion.

Do not set the FMR27 bit to 1 while the FMSTP bit (flash memory stop bit) in the FMR0 register is 1 (flash memory is stopped).

For details on the setting of this bit, see **10.5.11 Stopping Flash Memory**.

CMDRST Bit (Erase/write sequence reset bit)

This bit is used to initialize the flash memory sequence and forcibly stop a program or block erase command.
If the program or block erase command is forcibly stopped using the CMDRST bit in the FMR0 register, execute the clear status register command after the FST7 bit in the FST register is changed to 1 (ready). To program the same address again, execute the block erase command again and ensure it has been completed normally before programming. If the addresses and blocks which the program or block erase command is forcibly stopped are allocated in the program area, set the FMR13 bit in the FMR1 register to 1 (lock bit disabled) before executing the block erase command again.
When the CMDRST bit is set to 1 (erasure/writing stopped) during erase-suspend, the suspend status is also initialized. Thus execute block erasure again to the block which the block erasure is being suspended.
When td(CMDRST-READY) has elapsed after the CMDRST bit is set to 1 (erasure/writing stopped), the executing command is forcibly terminated and reading from the flash memory is enabled.

CMDERIE Bit (Erase/write error, blank check error, command sequence error interrupt enable bit)

This bit enables a flash command error interrupt to be generated if the following errors occur:
• Program error
• Block erase error
• Command sequence error
• Block blank check error
• Lock bit program error
When the CMDERIE bit is set to 1 (interrupt enabled), an interrupt is generated if the above errors occur.
If a flash command error interrupt is generated, execute the clear status register command during interrupt handling.
To change the CMDERIE bit from 0 (interrupt disabled) to 1 (interrupt enabled), make the setting as follows:
(1) Execute the clear status register command.
(2) Set the CMDERIE bit to 1.

BSYAEIE Bit (Flash access error interrupt enable bit)

This bit enables flash access error interrupt generation if the flash memory being rewritten is accessed.
To change the BSYAEIE bit from 0 (flash access error interrupt disabled) to 1 (flash access error interrupt enabled), follow the steps below:
(1) Read the BSYAEI bit in the FST register (dummy read).
(2) Write 0 (no flash access error interrupt requested) to the BSYAEI bit.
(3) Set the BSYAEIE bit to 1 (flash access error interrupt enabled).

RDYSTIE Bit (Flash ready status interrupt enable bit)

This bit enables flash ready status interrupt generation when the status of the flash memory sequence changes from busy to ready.
To change the RDYSTIE bit from 0 (flash ready status interrupt disabled) to 1 (flash ready status interrupt enabled), follow the steps below:
(1) Read the RDYSTI bit in the FST register (dummy read).
(2) Write 0 (no flash ready status interrupt requested) to the RDYSTI bit.
(3) Set the RDYSTIE bit to 1 (flash ready status interrupt enabled).

23.5.3 Flash Memory Control Register 1 (FMR1)

Address 001ABh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR17	FMR16	—	—	FMR13	WTFMSTP	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved	Set to 0.	R/W
b1	—			
b2	WTFMSTP	Flash memory stop bit in wait mode	0: Flash memory operates in wait mode 1: Flash memory is stopped in wait mode	R/W
b3	FMR13	Lock bit disable select bit (1)	0: Lock bit enabled 1: Lock bit disabled	R/W
b4	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b5	—			
b6	FMR16	Data flash block A rewrite disable bit (2, 3)	0: Rewrite enabled (software commands acceptable) 1: Rewrite disabled (software commands not acceptable, no error occurred)	R/W
b7	FMR17	Data flash block B rewrite disable bit (2, 3)		R/W

Notes:
1. To set this bit to 1, first write 0 and then write 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
2. To set this bit to 0, first write 1 and then write 0 immediately. Interrupts must be disabled between writing 1 and then writing 0.
3. This bit is set to 0 when the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).

WTFMSTP Bit (Flash memory stop bit in wait mode)

When the WTFMSTP bit is 1 (flash memory is stopped in wait mode), the flash memory is stopped when wait mode is entered. To perform A/D conversion in wait mode, set the WTFMSTP bit to 0 (flash memory operates in wait mode).

FMR13 Bit (Lock bit disable select bit)

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit is disabled. When the FMR13 bit is set to 0, the lock bit is enabled. For details on the lock bit, see **23.6.5 Data Protect Function**.

The FMR13 bit is used to enable the lock bit function only and the lock bit data remains unchanged. However, when a block erase command is executed while the FMR13 bit is 1 (lock bit disabled), the lock bit data set to 0 (lock bit enabled) is changed to 1 (lock bit disabled) after erase completes.

[Conditions for setting to 0]
- When the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready) and the program/erase command completes.
- When the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready) and program-suspend/erase-suspend is entered.
- When a command sequence error occurs.
- When the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- When the FMSTP bit in the FMR0 register is set to 1 (flash memory is stopped).
- When the CMDRST bit in the FMR0 register is set to 1 (erase/write sequence reset).

[Condition for setting to 1]
- When 1 is written to this bit by a program.

FMR16 Bit (Data flash block A rewrite disable bit)

When the FMR16 bit is set to 0, data flash block A accepts program and block erase commands.

FMR17 Bit (Data flash block B rewrite disable bit)

When the FMR17 bit is set to 0, data flash block B accepts program and block erase commands.

23.5.4 Flash Memory Control Register 2 (FMR2)

Address 001ACh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	—	FMR22	FMR21	FMR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Suspend enable bit (1)	0: Suspend disabled 1: Suspend enabled	R/W
b1	FMR21	Suspend request bit (2)	0: Restart 1: Suspend request	R/W
b2	FMR22	Interrupt request suspend request enable bit (1)	0: Suspend request disabled by interrupt request 1: Suspend request enabled by interrupt request	R/W
b3	—	Reserved	Set to 0.	R/W
b4	—			
b5	—			
b6	—			
b7	FMR27	Low-current-consumption read mode enable bit (1, 3)	0: Low-current-consumption read mode disabled 1: Low-current-consumption read mode enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then write 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
2. The FMR21 bit can be set when the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled) and the FMR20 bit is 1 (suspend enabled).
3. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU write mode disabled). Set this bit to 0 to perform A/D conversion.

FMR20 Bit (Suspend enable bit)

When the FMR20 bit is set to 1 (enabled), the suspend function is enabled.

FMR21 Bit (Suspend request bit)

When the FMR21 bit is set to 1 (suspend request), program/erase-suspend mode is entered. When the FMR22 bit is 1 (suspend request enabled by interrupt request), if an interrupt request for the enabled interrupt is generated, the FMR21 bit is automatically set to 1 (suspend request) and suspend mode is entered. To restart auto-erase or auto-programming, set the FMR21 bit to 0 (restart).

[Condition for setting to 0]
- When 0 is written to this bit by a program.

[Conditions for setting to 1]
- When the FMR22 bit is 1 (suspend request enabled by interrupt request) at the time an interrupt request is generated.
- When 1 is written to this bit by a program while the flash memory is busy.

FMR22 Bit (Interrupt request suspend request enable bit)

When the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) at the time an interrupt request is generated during auto-erase or auto-programming. Set the FMR22 bit to 1 when erase-suspend is used while the user ROM area is rewritten in EW1 mode.

FMR27 Bit (Low-current-consumption read mode enable bit)

When the FMR27 bit is set to 1 (low-current-consumption read mode enabled) in low-speed clock mode (XIN clock stopped) or low-speed on-chip oscillator mode (XIN clock stopped), current consumption when reading the flash memory can be reduced. When setting the FMR27 bit to 1, set the CPU clock (fs) to a frequency in the range of 3 kHz to 50 kHz. The flash memory circuit needs to be refreshed periodically in low-current-consumption read mode. Setting the FREFR register allows the MCU to perform a refresh automatically. Set the FMR27 bit in the FMR2 register to 0 (low-current-consumption read mode disabled) and then set the FREFR register. After that, set the FMR27 bit to 1 (low-current-consumption read mode enabled). For details on the setting of the FREFR register, see **23.5.5 Flash Memory Refresh Control Register (FREFR)**.
For details on the lock bit, see **10.5.12 Low-Current-Consumption Read Mode**.

Low-current-consumption read mode can be used when the CPU clock is set to either of the following:
• The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
• The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.
However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below. After setting the division ratio of the CPU clock, set the FMR27 bit to 1.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).
When the FMR27 bit is set to 1 (low-current-consumption read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory is stopped) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-current-consumption read mode disabled).

23.5.5 Flash Memory Refresh Control Register (FREFR)

Address 001ADh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	REF5	REF4	REF3	REF2	REF1	REF0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	REF0	Periodic refresh interval control bits	Value in the FREFR register = fs/10^3 (the result value is expressed as an integer) If the clock source for the CPU clock (fs) is the low-speed on-chip oscillator, it is taken to be the minimum fLOCO value (60 kHz). Ex: Value set in the FREFR register when the CPU clock (fs) is set to 12.5 kHz: ($12.5 \times 10^3/10^3$) = 12 = 001100b	R/W
b1	REF1			R/W
b2	REF2			R/W
b3	REF3			R/W
b4	REF4			R/W
b5	REF5			R/W
b6	—	Nothing is assigned. The write value must be 0. The read value is 0.		—
b7	—			

The FREFR register is used to control the interval between refresh operations when the FMR27 bit in the FMR2 register is 1 (low-current-consumption read mode enabled). Set the FMR27 bit in the FMR2 register to 0 (low-current-consumption read mode disabled) and then set the value of this register. After that, set the FMR27 bit to 1 (low-current-consumption read mode enabled).

23.6 CPU Rewrite Mode

Each mode is described as below.

23.6.1 EW0 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), CPU rewrite mode is entered and software commands are accepted. Since the FMR02 bit in the FMR0 register is 0 at this time, EW0 mode is selected.

Software commands are used to control programming/erase. The FST register can be used to confirm the status when programming/erase is completed.

To enter suspend during auto-erase or auto-programming, set the FMR20 bit to 1 (suspend enabled) and the FMR21 bit to 1 (suspend request). Next, verify the FST7 bit in the FST register is set to 1 (ready), then verify the FST3 bit is set to 1 (during program-suspend) or the FST6 bit is set to 1 (during erase-suspend) before accessing the flash memory. When the FST3 bit is set to 0, programming completes. When the FST6 bit is set to 0, erasure completes.

When the FMR21 bit in the FMR2 register is set to 0 (restart), auto-erase or auto-programming is restarted. To confirm whether auto-programming or auto-erase has restarted, verify the FST7 bit in the FST register is set to 0, then verify the FST3 bit is set to 0 (other than program-suspend) or the FST6 bit is set to 0 (other than erase-suspend).

23.6.2 EW1 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled) and then the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected. The FST register can be used to confirm the status when programming/erase is completed.

To enable the suspend function during auto-erase or auto-programming, set the FMR20 bit in the FMR2 register to 1 (suspend enabled) and the FMR22 bit to 1 (suspend request enabled by interrupt request) and then execute the block program/erase command. The interrupt to enter suspend must be enabled beforehand.

When an interrupt request is generated, the FMR21 bit in the FMR2 register is automatically set to 1 (suspend request) and auto-erase or auto-programming is suspended after td(SR-SUS). Set the FMR21 bit to 0 (restart) to restart auto-erase or auto-programming after interrupt handling is completed.

23.6.3 Suspend Operation

The erase-suspend function temporarily halts the auto-erase during the operation.
The program suspend function temporarily halts the auto-programming during the operation.
When auto-erase or auto-programming is suspended, the following operation can be executed (see **Table 23.7 Executable Operation during Suspend**).

- When auto-erase of any block in the user ROM is suspended, auto-programming and reading of another block in the user ROM can be executed.
- When auto-programming of any block in the user ROM is suspended, reading of another block in the user ROM can be executed.

Table 23.7 Executable Operation during Suspend

		Operation during Suspend							
		Block where erase or program operation is executed before entering suspend				Block where erase or program operation is not yet executed before entering suspend			
		Erase	Program	Read lock bit status	Read	Erase	Program	Read lock bit status	Read
Command in execution	Erase	No	No	No	No	No	Yes	Yes	Yes
	Program	No	No	No	No	No	No	Yes	Yes

Note:
1. “Yes” indicates operation is possible by using the suspend function and “No” indicates operation is disabled.
2. The block erase command can be executed for erasure. The program and lock bit program commands can be executed for programming.
   The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).
   The block blank check operation is disabled during suspend.
3. The MCU enters read array mode immediately after entering suspend.

Figure 23.3 shows the Timing for Erase-Suspend Operation. Figure 23.4 shows the Timing for Program-Suspend Operation.

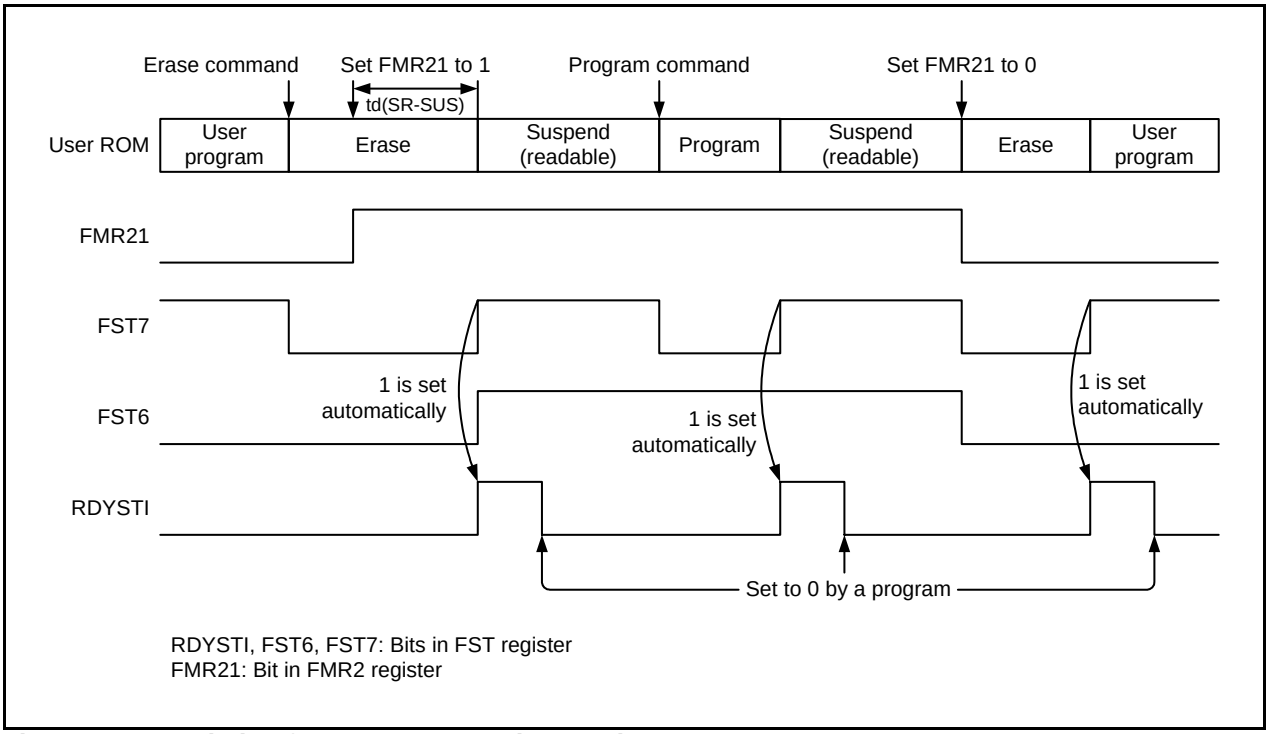


Figure 23.3 Timing for Erase-Suspend Operation

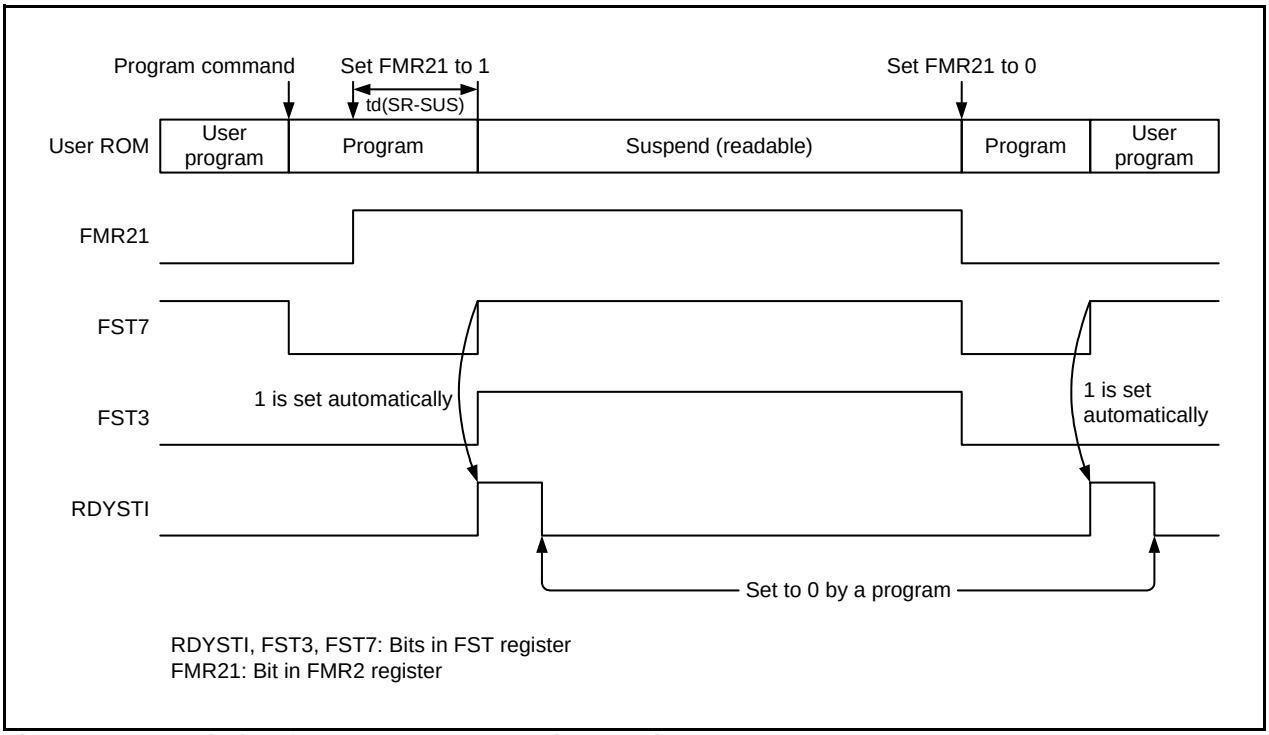
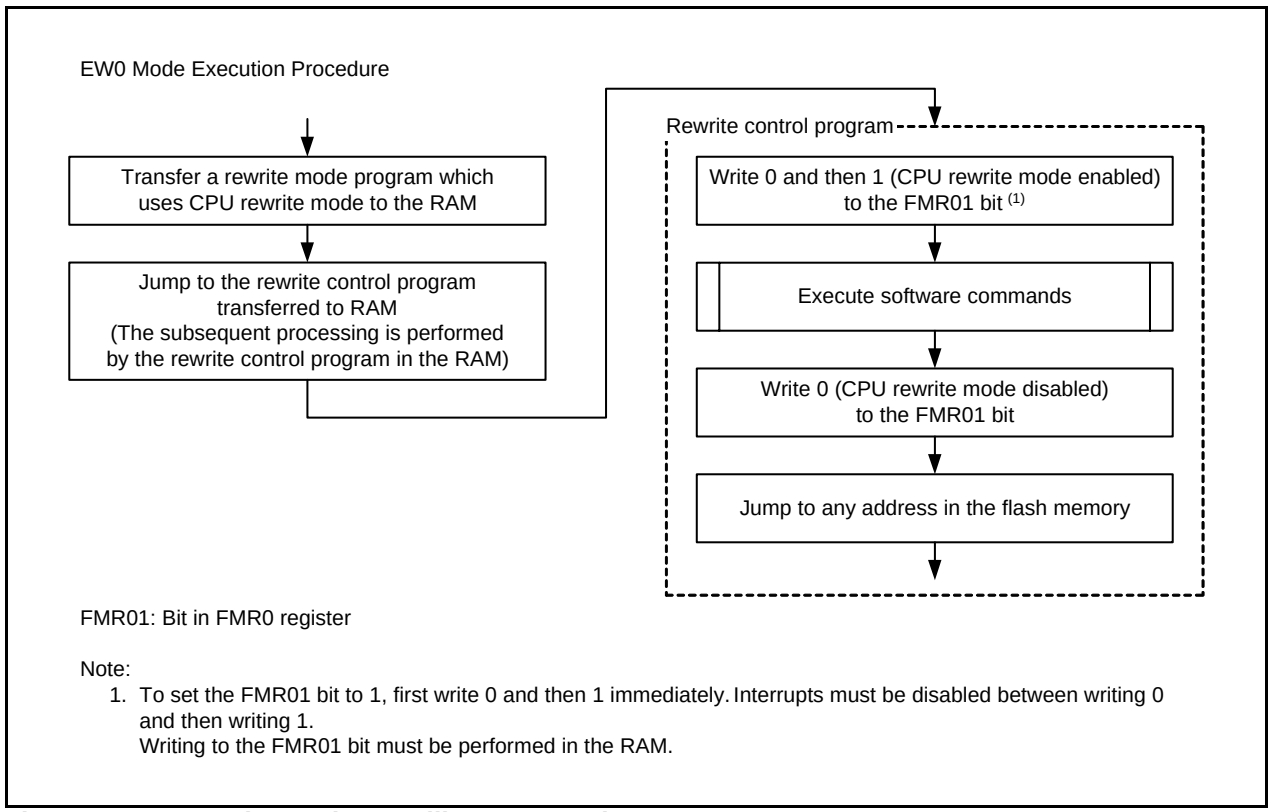


Figure 23.4 Timing for Program-Suspend Operation

23.6.4 Setting and Cancelling Each Mode

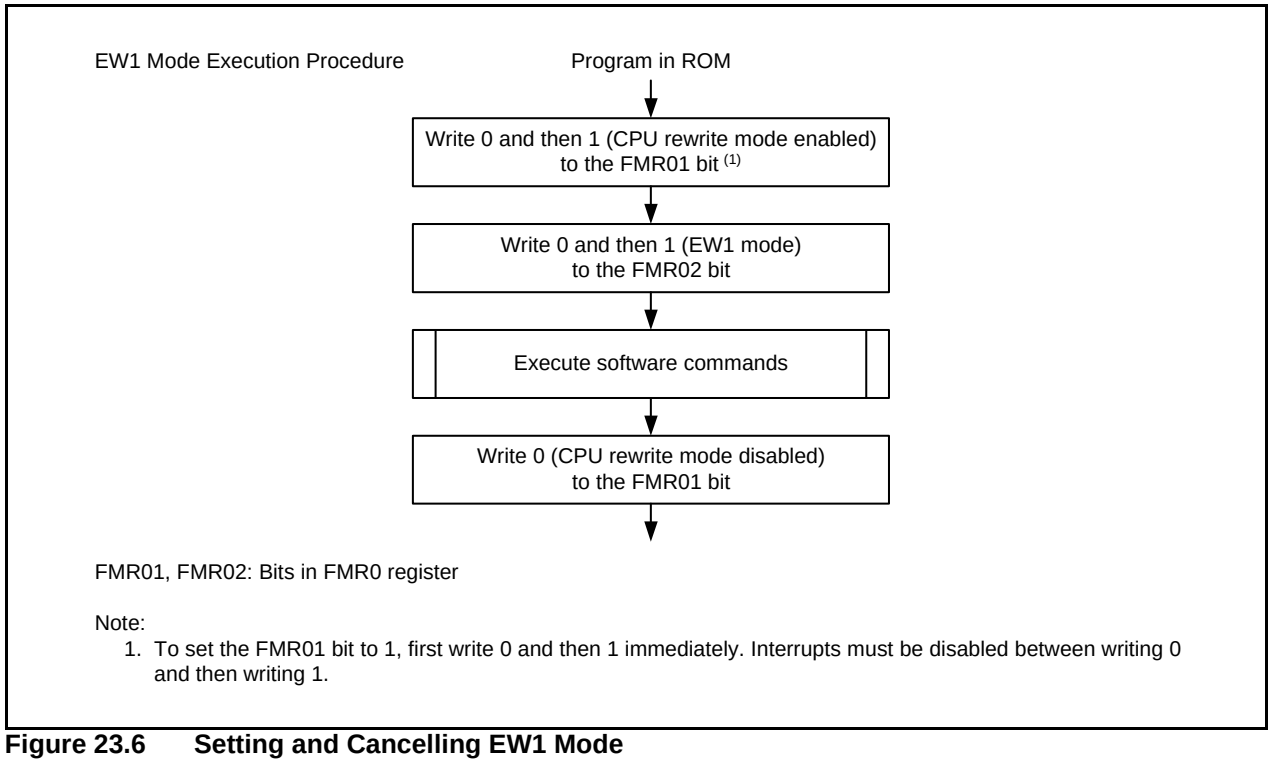
Figure 23.5 shows Setting and Cancelling EW0 Mode. Figure 23.6 shows Setting and Cancelling EW1 Mode.



FMR01: Bit in FMR0 register

Note:
1. To set the FMR01 bit to 1, first write 0 and then 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
   Writing to the FMR01 bit must be performed in the RAM.

Figure 23.5 Setting and Cancelling EW0 Mode



FMR01, FMR02: Bits in FMR0 register

Note:
1. To set the FMR01 bit to 1, first write 0 and then 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.

Figure 23.6 Setting and Cancelling EW1 Mode

23.6.5 Data Protect Function

Each block in the program ROM in the flash memory has a nonvolatile lock bit. The lock bit is enabled when the FMR13 bit in the FMR1 register is 0 (lock bit enabled). The lock bit can be used to disable (lock) programming/erasing each block. This prevents data from being written or erased inadvertently. The block status changes according to the lock bit as follows:

- When the lock bit data is 0: locked (the block cannot be programmed/erased)
- When the lock bit data is 1: not locked (the block can be programmed/erased)

The lock bit data is set to 0 (locked) when the lock bit program command is executed, and 1 (not locked) when the block is erased. There are no commands that can be used to set only the lock bit data to 1.
The lock bit data can be read using the read lock bit status command.

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit function is disabled and no blocks are locked. The lock bit data remains unchanged. When the FMR13 bit is set to 0 (lock bit enabled), the lock bit function is enabled. The lock bit data is retained.
When the block erase command is executed while the FMR13 bit is 1 (lock bit disabled), the target block is erased regardless of the lock bit status. The lock bit for the erase-target block is set to 1 after erase is completed. For details on individual commands, see **23.6.6 Software Commands**.
The FMR13 bit is set to 0 after auto-erase is completed. This bit is also set to 0 when one of the following conditions is met. To program/erase a block with a lock bit in a different state, set the FMR 13 bit to 1 (lock bit disabled) again and execute the program command or the block erase command.

- When the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready) and the program/erase command completes.
- When the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready) and program-suspend/erase-suspend is entered.
- When a command sequence error occurs.
- When the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- When the FMSTP bit in the FMR0 register is set to 1 (flash memory is stopped).
- When the CMDRST bit in the FMR0 register is set to 1 (erase/write sequence reset).

Figure 23.7 shows the Timing for FMR13 Bit Operation.

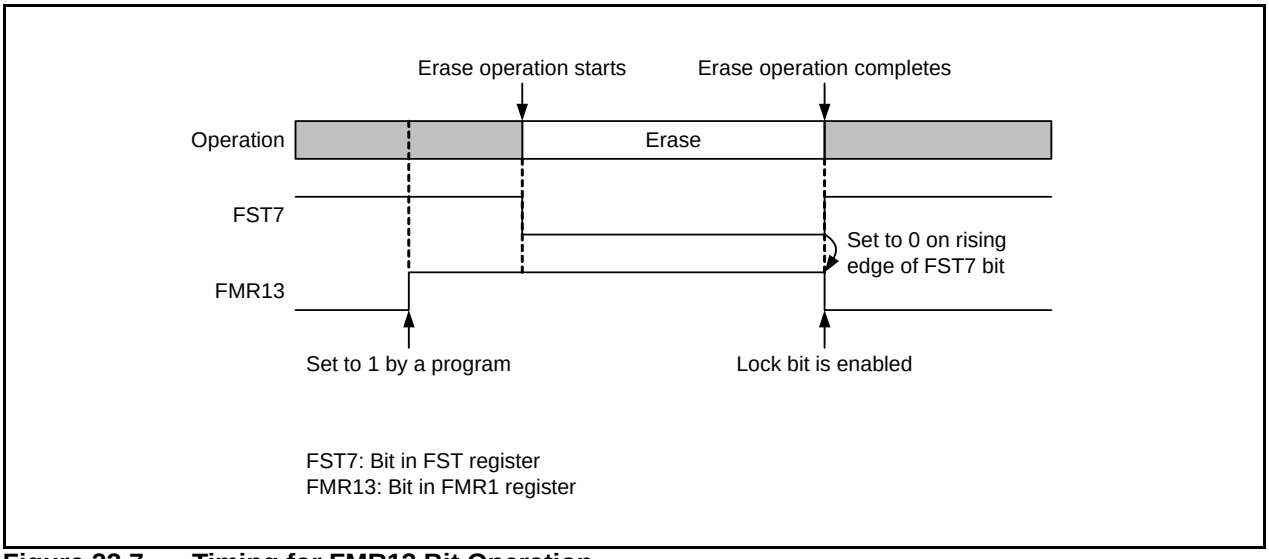


Figure 23.7 Timing for FMR13 Bit Operation

23.6.6 Software Commands

The software commands are described below. Commands must be read or written and data in 8-bit units. Do not input any command other than those listed in the table below.

Table 23.8 Software Commands

Command	First Command			Second Command (1)		
	Mode	Address	Data	Mode	Address	Data
Read array	Write	x	FFh			
Clear status register	Write	x	50h			
Program	Write	WA	40h	Write	WA	WD
Block erase	Write	x	20h	Write	BA	D0h
Lock bit program	Write	BT	77h	Write	BT	D0h
Read lock bit status	Write	x	71h	Write	BT	D0h
Block blank check	Write	x	25h	Write	BA	D0h

WA: Write address
WD: Write data
BA: Any address in the block
BT: Start address in the block
Block 3 → 0C000h
Block 2 → 0E000h
Block 1 → 0F000h
x: Any address in the user ROM area
Note:
1. For block erase, lock bit program, read lock bit status, and block blank check commands, if FFh is written as the second command, the command code written as the first command becomes invalid. A command sequence error does not occur.

The data flash does not have a lock bit, so the lock bit program and the read lock bit status commands are handled as illegal.

23.6.6.1 Read Array

This command is used to read the flash memory.
When FFh is written as the first command, the MCU enters read array mode. When the read address is input in the following cycles, the content of the specified address can be read in 8-bit units.
Since read array mode is retained until another command is written, the contents of multiple addresses can be read continuously.
In addition, after a reset, the MCU enters read array mode after a program, block erase, block blank check, read lock bit status, or clear status register command, or after entering suspend.

23.6.6.2 Clear Status Register

The clear status register command is used to set bits FST4 and FST5 in the FST register to 0.
When 50h is written as the first command, bits FST4 and FST5 in the FST register are set to 0.

23.6.6.3 Program

This command writes data to the flash memory in 1-byte units.
When 40h is written as the first command and data is written to the write address with the second command, auto-programming (a data program and verify operation) starts. The address value for the first command must be the same address as the write address specified with the second command.
The FST7 bit in the FST register can be used to confirm whether auto-programming has completed. The FST7 bit is set to 0 during auto-programming and is set to 1 when auto-programming completes.
After auto-programming has completed, the auto-program result can be confirmed by the FST4 bit in the FST register (see **23.6.7 Full Status Check**).
Do not write additions to the already programmed addresses.
For each block in the program ROM, the program command can be disabled using the lock bit.
When the FMR16 bit in the FMR1 register is 1 (rewrite disabled), the program command for block A of data flash is not accepted. When the FMR17 bit is 1 (rewrite disabled), the program command for block B is not accepted.
Figure 23.8 shows the Program Flowchart (Flash Ready Status Interrupt Disabled and Suspend Disabled). Figure 23.9 shows the Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled). Figure 23.10 shows the Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled). Figure 23.11 shows the Program Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

In EW1 mode, do not execute this command for any address where the rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt enabled), a flash ready status interrupt is generated when auto-programming is completed.
When the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt enabled) and the FMR20 bit in the FMR2 register is 1 (suspend enabled), a flash ready status interrupt is generated when the FMR21 bit is set to 1 (suspend request) and auto-programming is suspended. The result can be confirmed by reading the FST register in the interrupt routine.

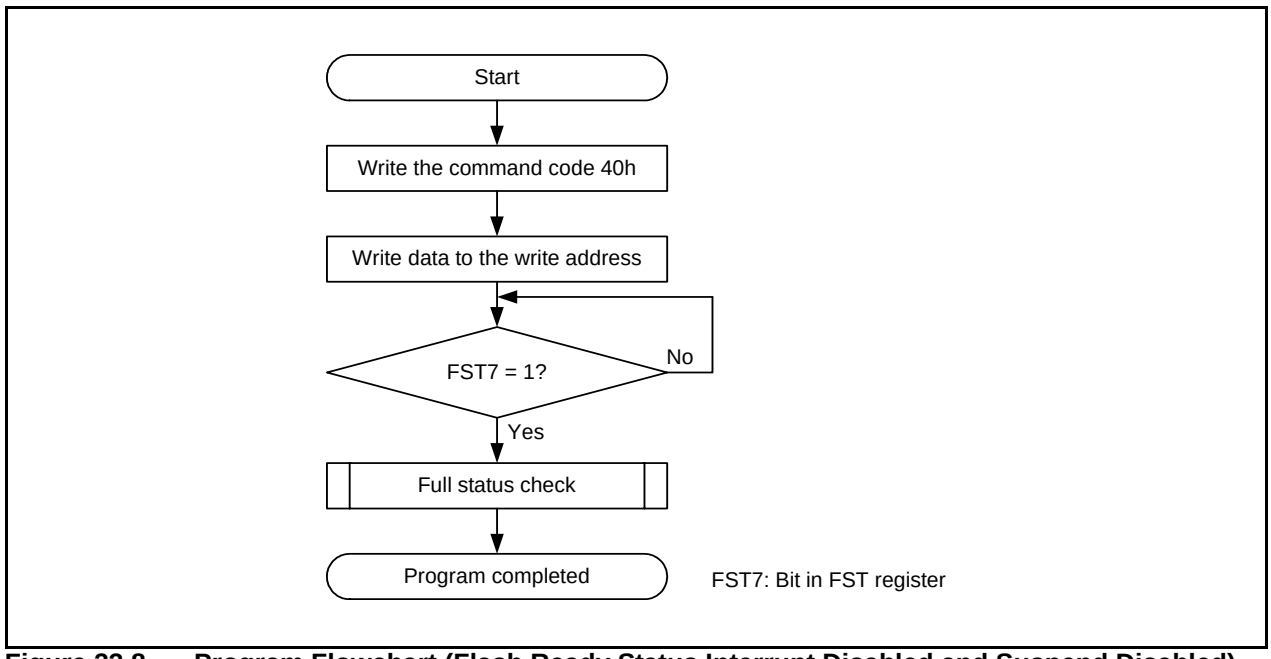
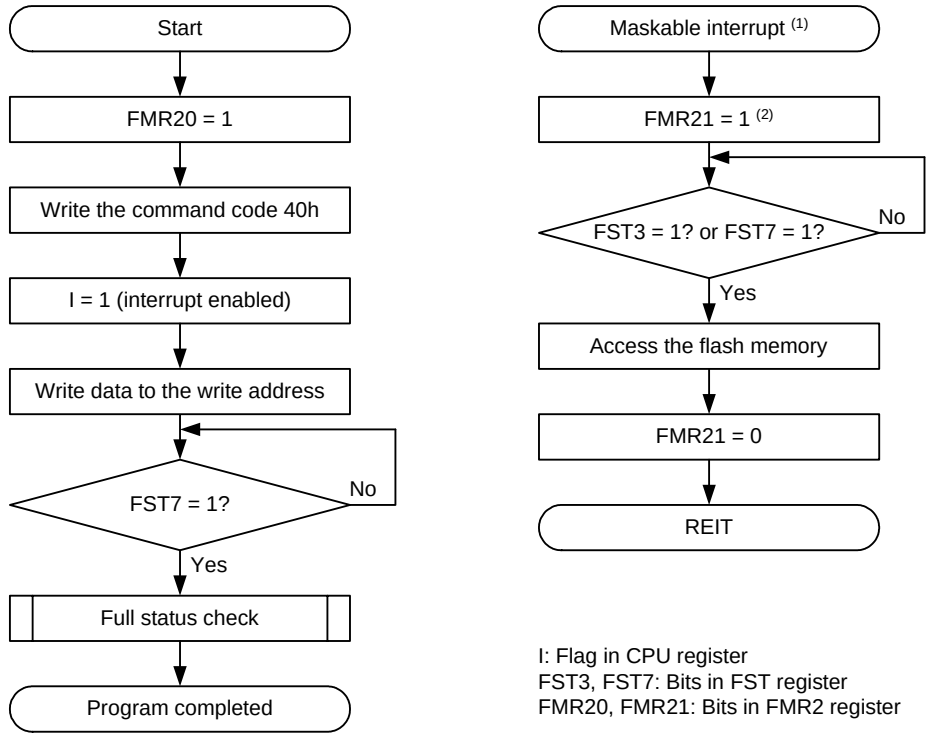
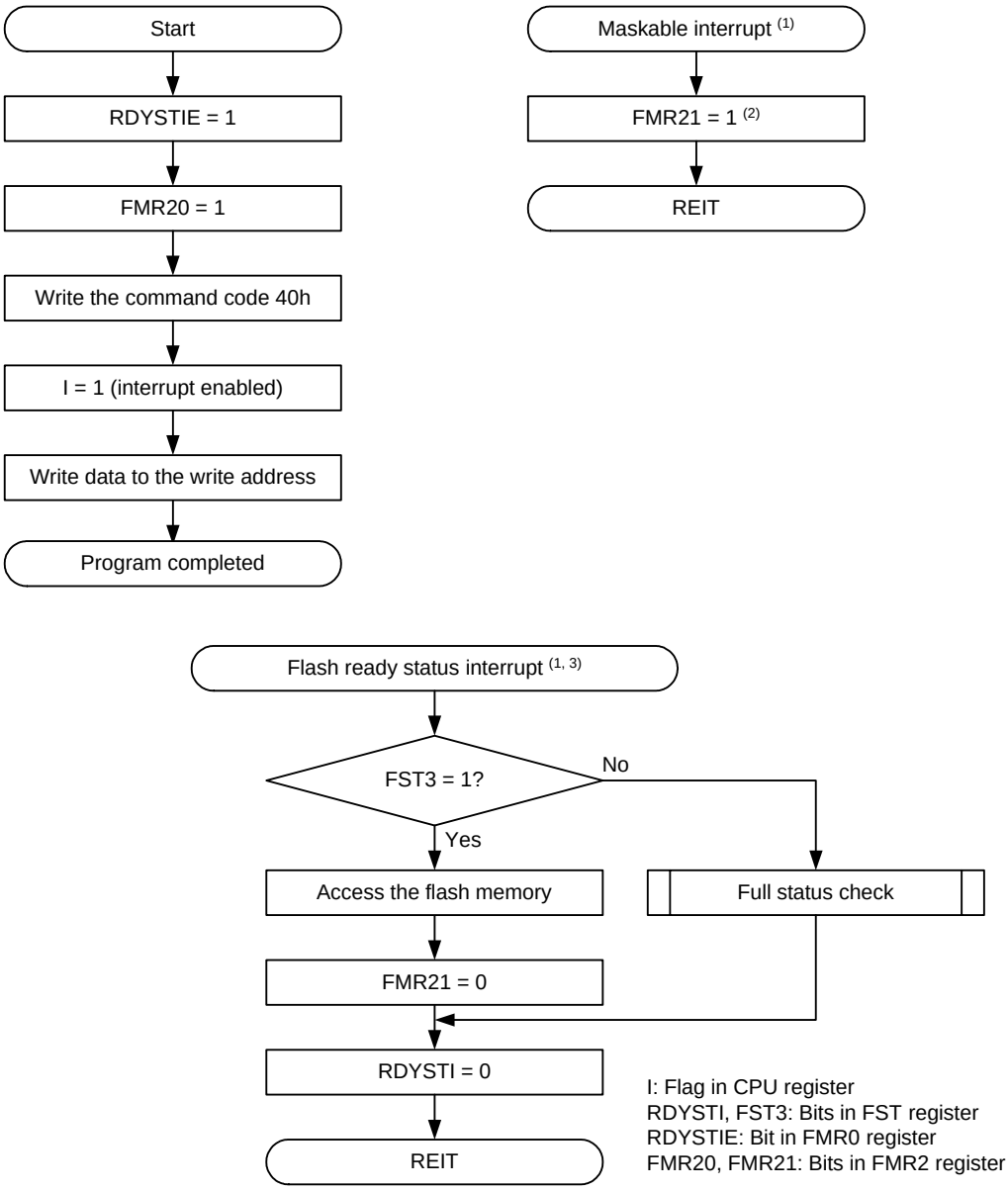


Figure 23.8 Program Flowchart (Flash Ready Status Interrupt Disabled and Suspend Disabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt to enter the suspend state must be enabled beforehand.

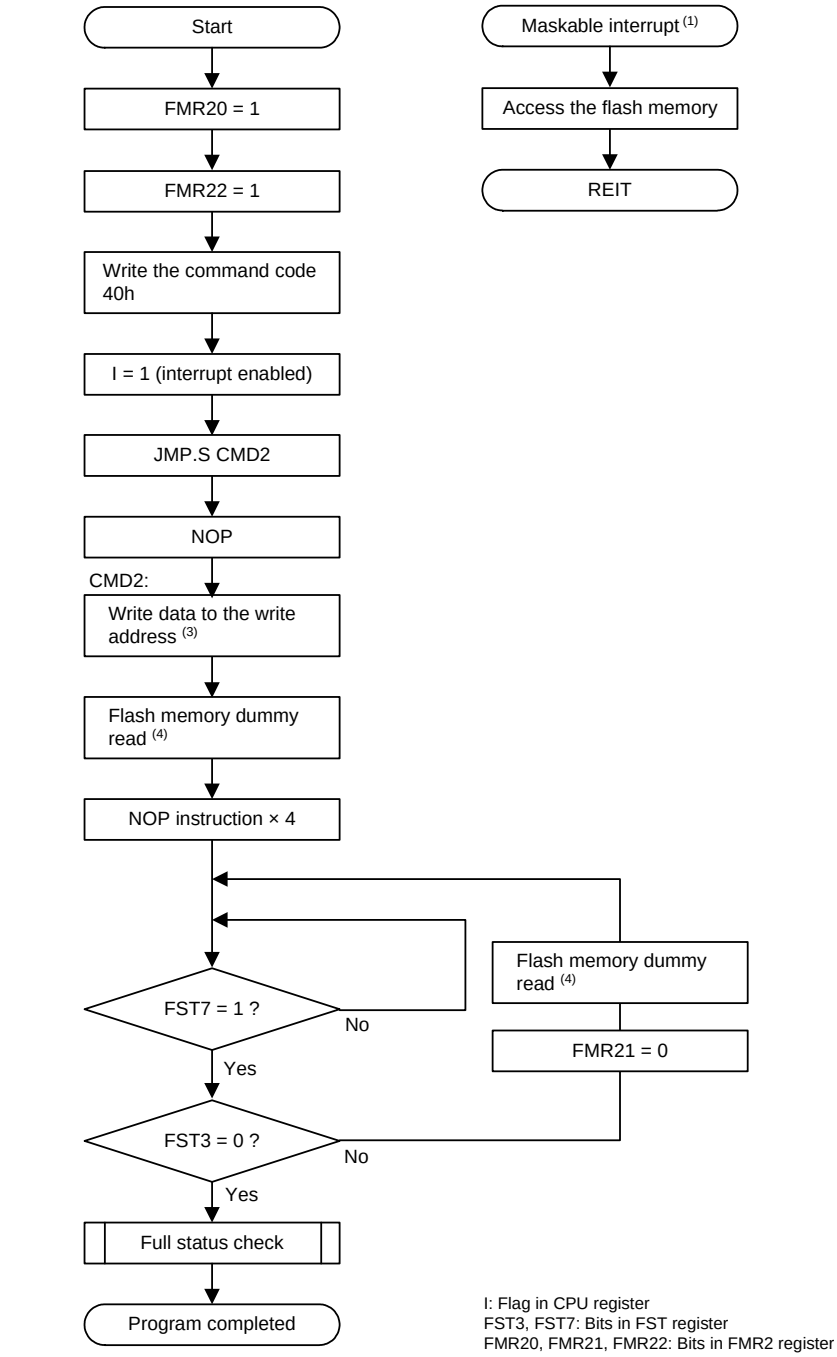
Figure 23.9 Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt to enter the suspend state must be enabled beforehand.
3. A flash ready status interrupt is generated when auto-programming is suspended.

Figure 23.10 Program Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled)

When the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is generated during auto-programming. Set the FMR22 bit to 1 when suspend is used while the user ROM area is rewritten in EW1 mode.



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the maskable interrupt is generated until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.
3. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
4. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn

Figure 23.11 Program Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

23.6.6.4 Block Erase

When 20h is written as the first command and then D0h is written to any address in the block with the second command, an auto-erase (erase and erase-verify operation) is started in the specified block.
The FST7 bit in the FST register can be used to confirm whether auto-erase is completed. The FST7 bit is set to 0 during auto-erase and changed to 1 when auto-erase is completed. After auto-erase completes, all data in the block is set to FFh.
After auto-erase is completed, the result can be confirmed by the FST5 bit in the FST register (see **23.6.7 Full Status Check**).
For each block in the program ROM, the program erase command can be disabled using the lock bit.
When the FMR16 bit in the FMR1 register is 1 (rewrite disabled), the block erase command for block A of data flash is not accepted. When the FMR17 bit is 1 (rewrite disabled), the block erase command for block B is not accepted.
Figure 23.12 shows the Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Disabled). Figure 23.13 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled). Figure 23.14 shows the Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled). Figure 23.15 shows the Block Erase Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled).

In EW1 mode, do not execute this command for the block where the rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt enabled), a flash ready status interrupt is generated when auto-erase is completed. When the RDYSTIE bit in the FMR0 register is 1 (flash ready status interrupt enabled) and the FMR20 bit in the FMR2 register is 1 (suspend enabled), a flash ready status interrupt is generated when the FMR21 bit is set to 1 (suspend request) and auto-erase is suspended. The result can be confirmed by reading the FST register in the interrupt routine.

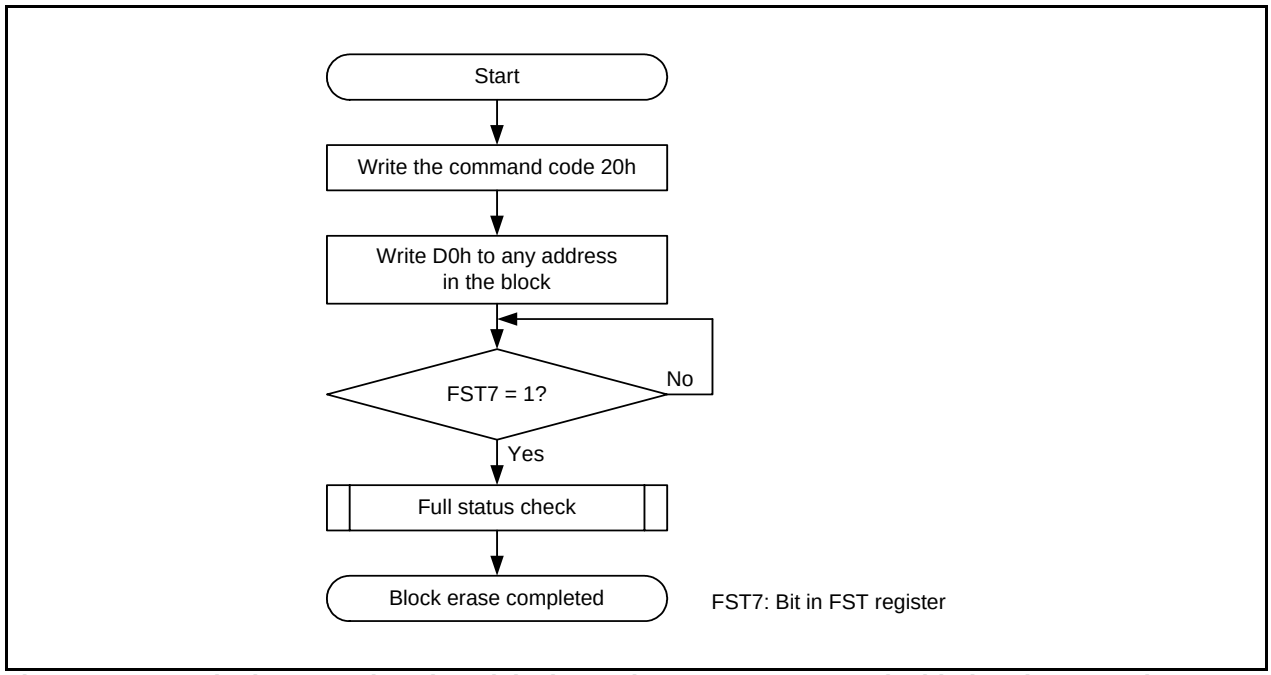
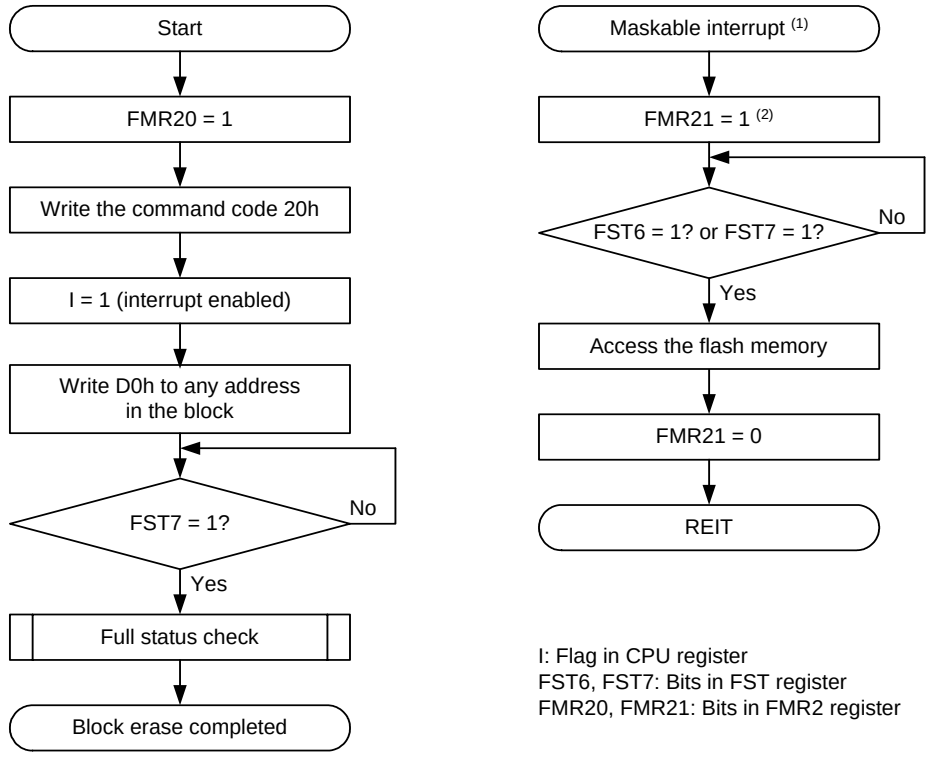
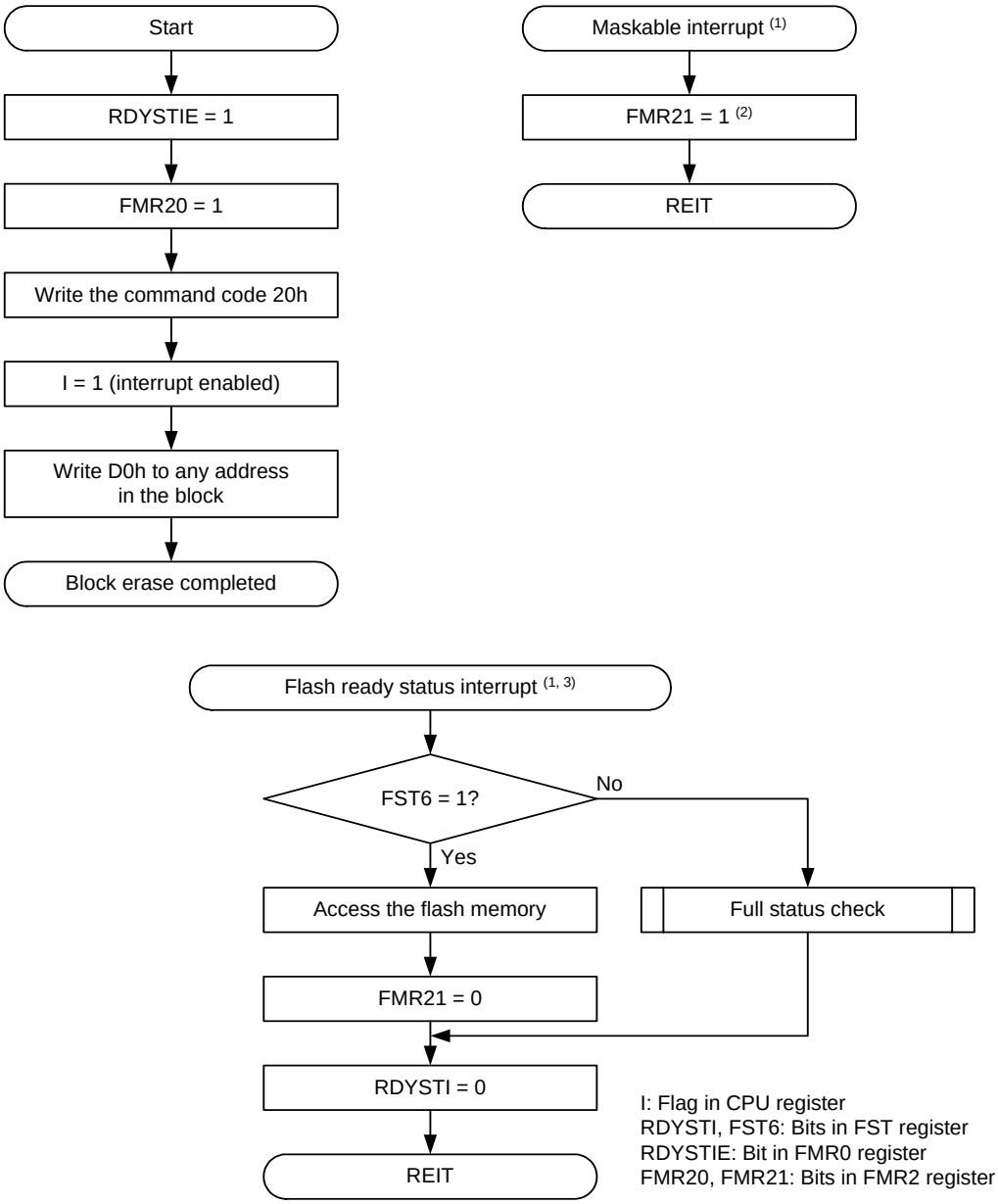


Figure 23.12 Block Erase Flowchart (Flash Ready Status Interrupt Disabled and Suspend Disabled)



Notes:
1. The interrupt vector table and interrupt routine to be used must be allocated to an area other than the erase-target area.
2. td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.

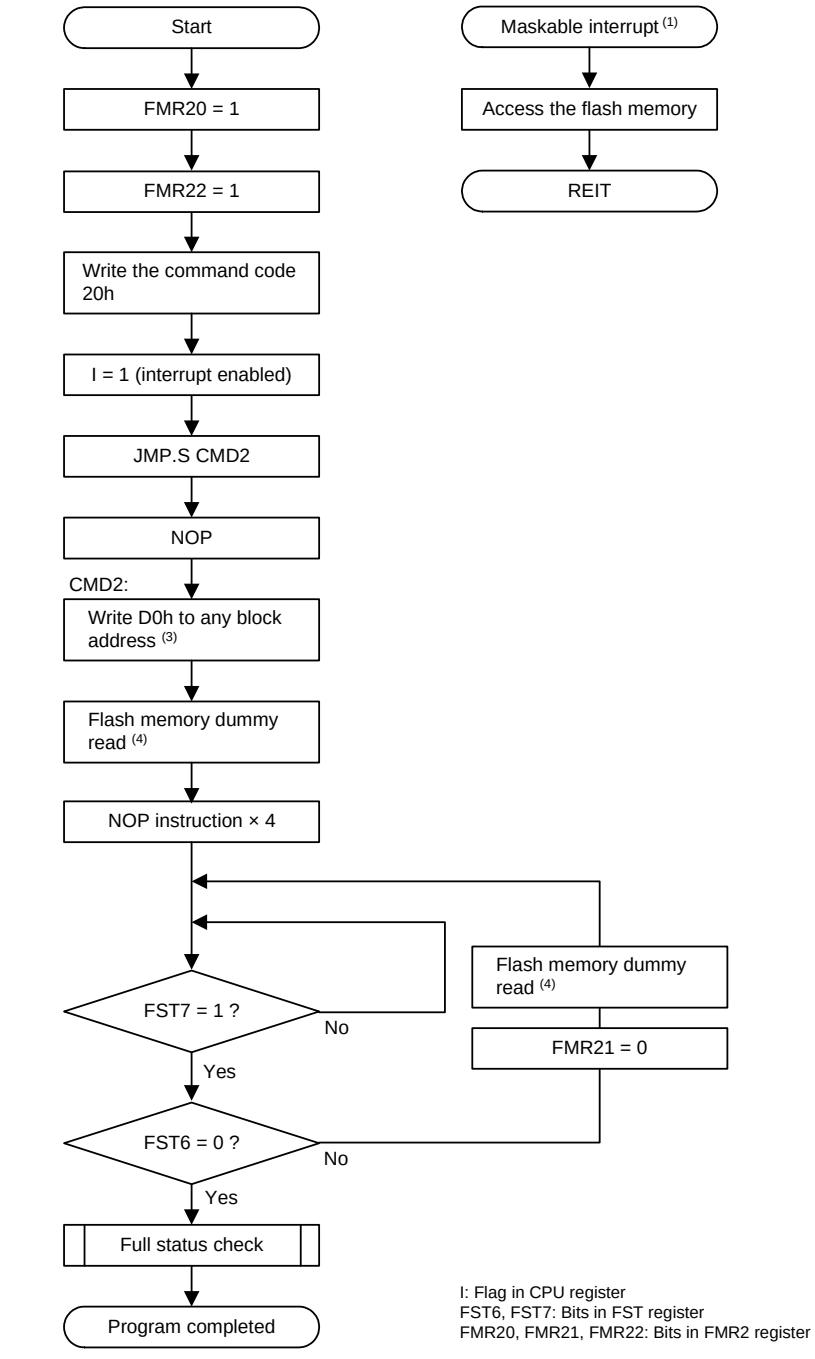
Figure 23.13 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)



Notes:
1. The interrupt vector table and interrupt routine to be used must be allocated to an area other than the erase-target area.
2. td(SR-SUS) is required from when the FMR21 bit is set to 1 until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.
3. A flash ready status interrupt is generated when auto-erase is suspended.

Figure 23.14 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled)

When the FMR22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is generated during auto-erase. Set the FMR22 bit to 1 when suspend is used while the user ROM area is rewritten in EW1 mode.



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the maskable interrupt is generated until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.
3. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
4. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn

Figure 23.15 Block Erase Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

23.6.6.5 Lock Bit Program

This command is used to set the lock bit for any block in the program ROM area to 0 (locked).
When 77h is written as the first command and D0h is written to the start address in the block with the second command, 0 is written to the lock bit in the specified block. The address for the first command must be the same as that for the second which specifies the start address in the block.
Figure 23.16 shows the Lock Bit Program Flowchart.
The lock bit status (lock bit data) can be read using the read lock bit status command.
The FST7 bit in the FST register can be used to confirm whether writing to the lock bit is completed.
For details on the lock bit function and how to set the lock bit to 1 (not locked), see **23.6.5 Data Protect Function**.

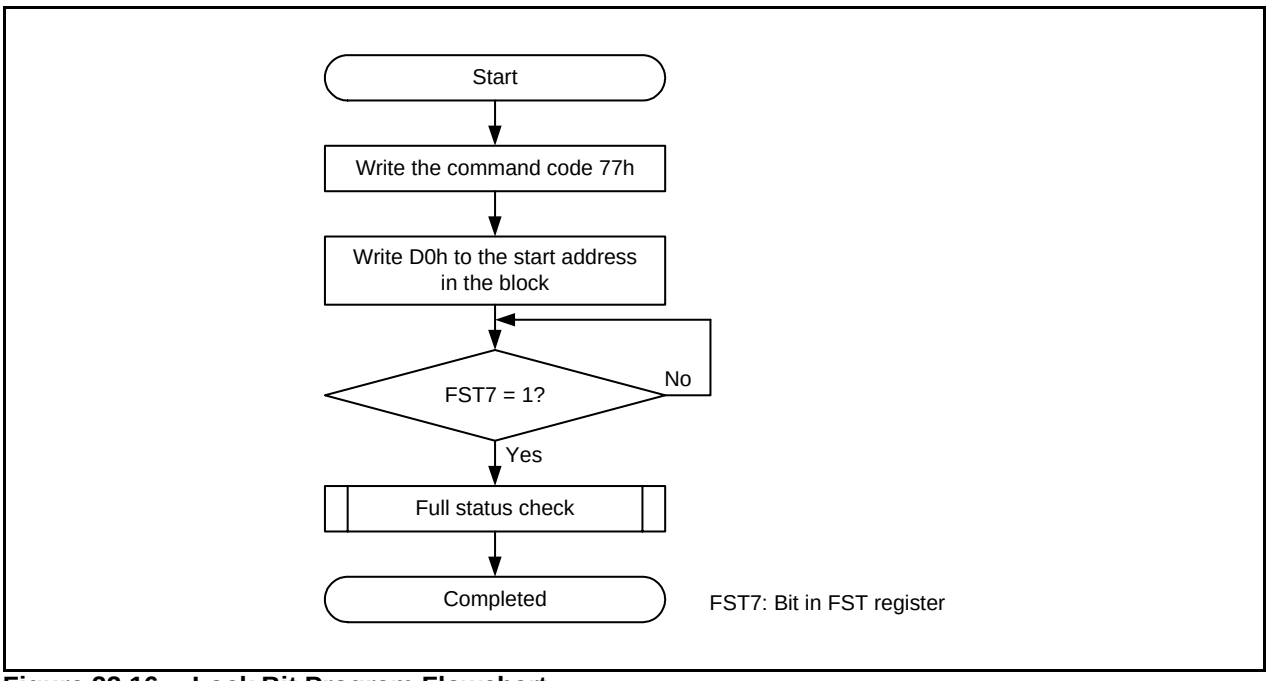


Figure 23.16 Lock Bit Program Flowchart

23.6.6.6 Read Lock Bit Status Command

This command is used to read the lock bit status for any block in the program ROM area.
When 71h is written as the first command and D0h is written to the start address in the block with the second command, the lock bit status in the specified block is stored in the FST2 bit in the FST register. Read the FST2 bit after the FST7 bit in the FST register has changed to 1 (ready).
Figure 23.17 shows the Read Lock Bit Status Flowchart.

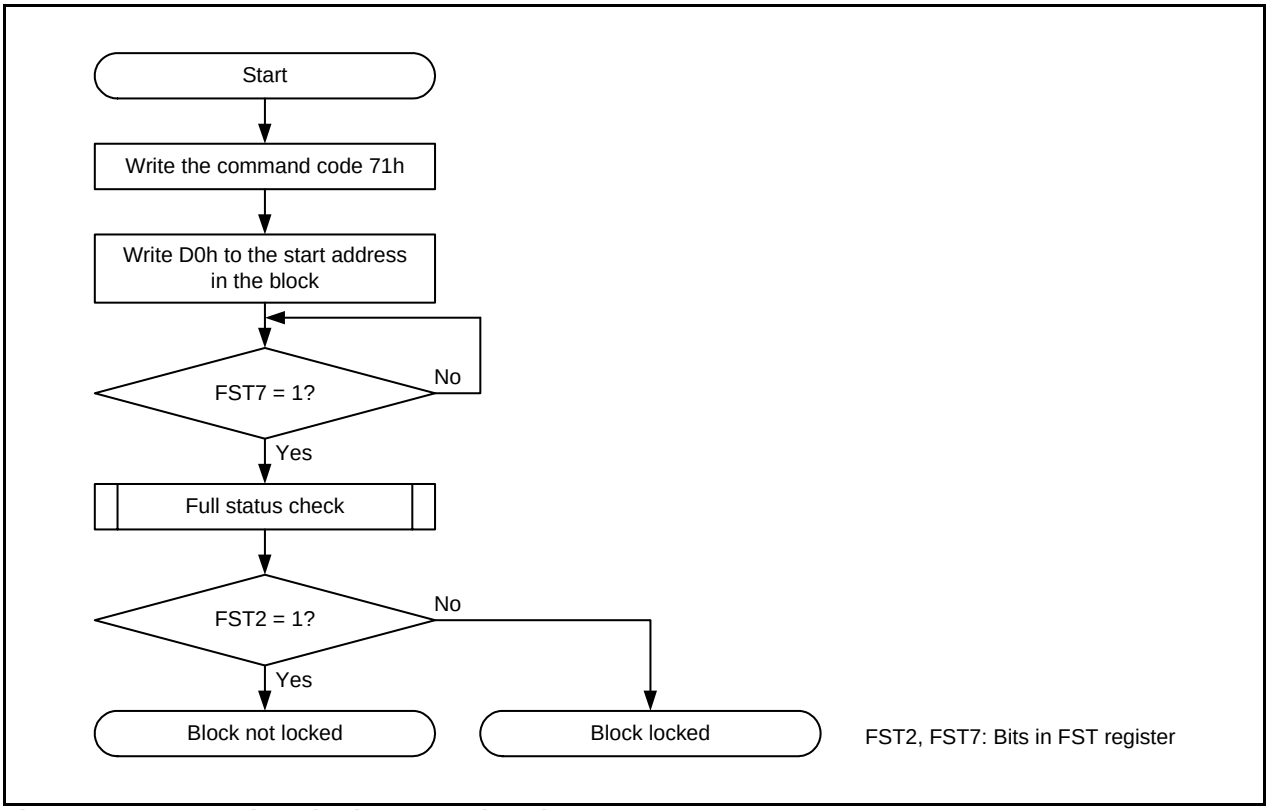


Figure 23.17 Read Lock Bit Status Flowchart

23.6.6.7 Block Blank Check

This command is used to confirm that all addresses in any block are blank data, FFh.
When 25h is written as the first command and D0h is written to any address in the block with the second command, a blank check is started for the specified block. The FST7 bit in the FST register can be used to confirm whether blank check is completed. The FST7 bit is set to 0 during the blank-check period and changed to 1 when the blank check has completed.
After the blank check has completed, the result can be determined by reading the FST5 bit in the FST register (see **23.6.7 Full Status Check**). This command is also used to verify the target block has not been written. To confirm whether erase has completed normally, execute the full status check.

Do not execute the block blank check command when the FST6 bit in the FST register is 1 (erase suspended) or the FST3 bit is 1 (program suspended).
Figure 23.18 shows the Block Blank Check Flowchart.

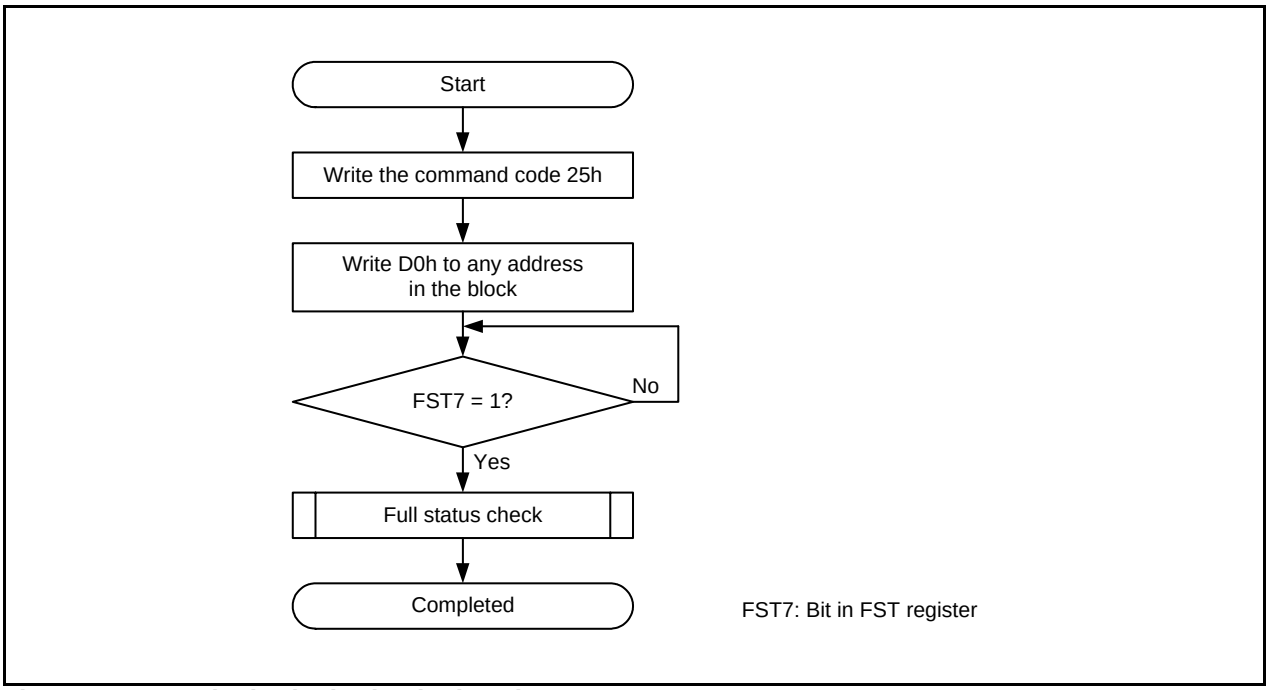


Figure 23.18 Block Blank Check Flowchart

This command is intended for programmer manufacturers, not for general users.

23.6.7 Full Status Check

If an error occurs, bits FST4 to FST5 in the FST register are set to 1, indicating the occurrence of the error. The execution result can be confirmed by checking these status bits (full status check).
Table 23.9 lists the Errors and FST Register States. Figure 23.19 shows the Full Status Check and Handling Procedures for Individual Errors.

Table 23.9 Errors and FST Register States

FST Register States		Error	Error Occurrence Condition
FST5 Bit	FST4 Bit		
1	1	Command sequence error	• When a command is not written correctly. • When data other than valid data (i.e., D0h or FFh) is written as the second command of the block erase, lock bit program, read lock bit status, or block blank check command (1). • The erase command is executed during erase-suspend or the block blank check command is executed. • The program, lock bit program, erase, or block blank check command is executed during program-suspend. • The program, lock bit program, erase, or block blank check command is executed to the block during suspend. • The lock bit program or read lock bit status commands are executed to the data flash.
1	0	Erase error	When the block erase command is executed and auto-erase does not complete normally.
		Blank check error	When the block blank check command is executed and data other than the blank data, FFh, is read.
0	1	Program error	When the program command is executed and auto-programming does not complete normally.
		Lock bit program error	When the lock bit command is executed, but the lock bit is not set to 0 (locked).

Note:
1. When FFh is written as the second command of these commands, the MCU enters read array mode. At the same time, the command code written as the first command becomes invalid.

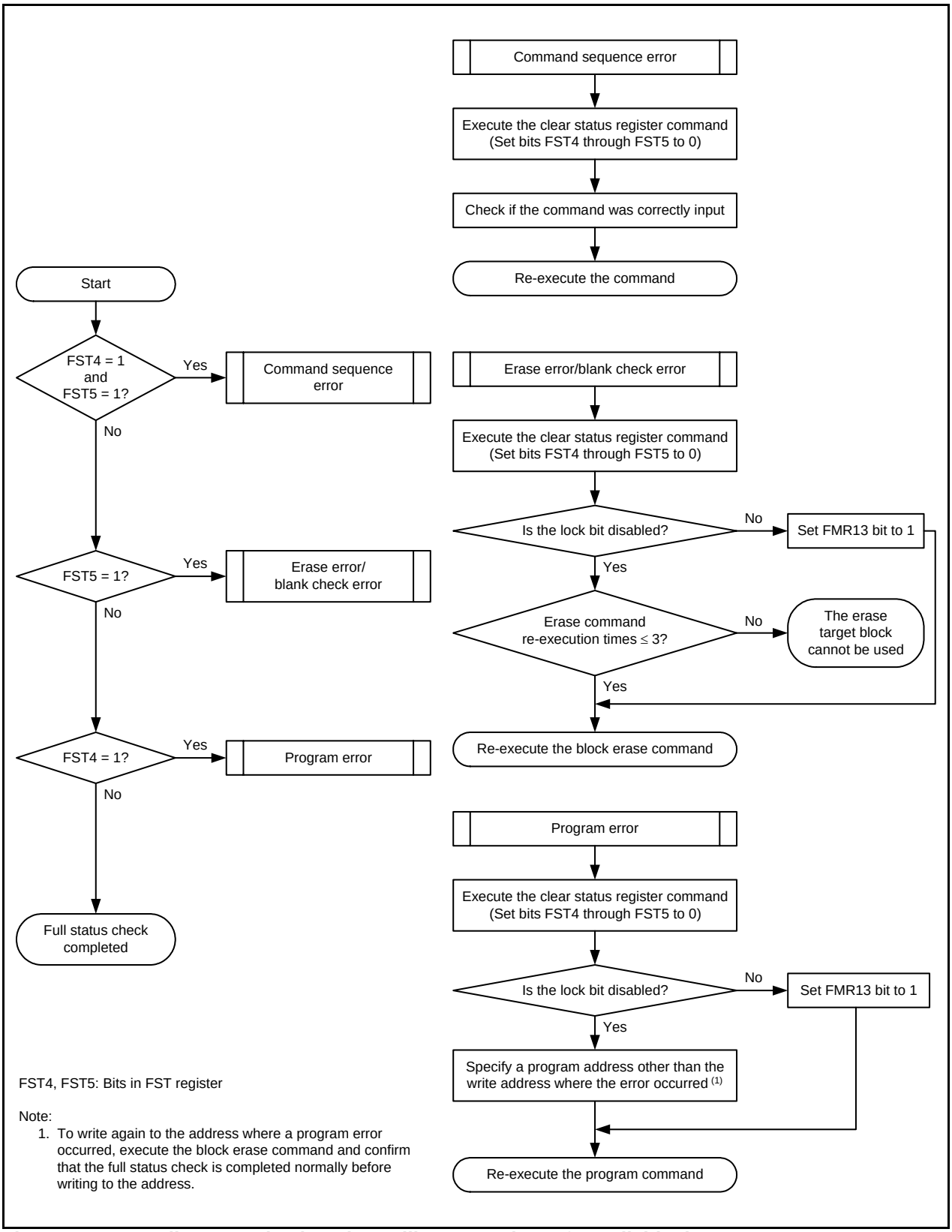


Figure 23.19 Full Status Check and Handling Procedures for Individual Errors

23.7 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer that supports the MCU can be used to rewrite the user ROM area with the MCU mounted on-board.
There are three standard serial I/O modes:
• Standard serial I/O mode 1: Connection to a serial programmer via clock synchronous serial I/O
• Standard serial I/O mode 2: Connection to a serial programmer via clock asynchronous serial I/O
• Standard serial I/O mode 3: Connection to a serial programmer via special clock asynchronous serial I/O

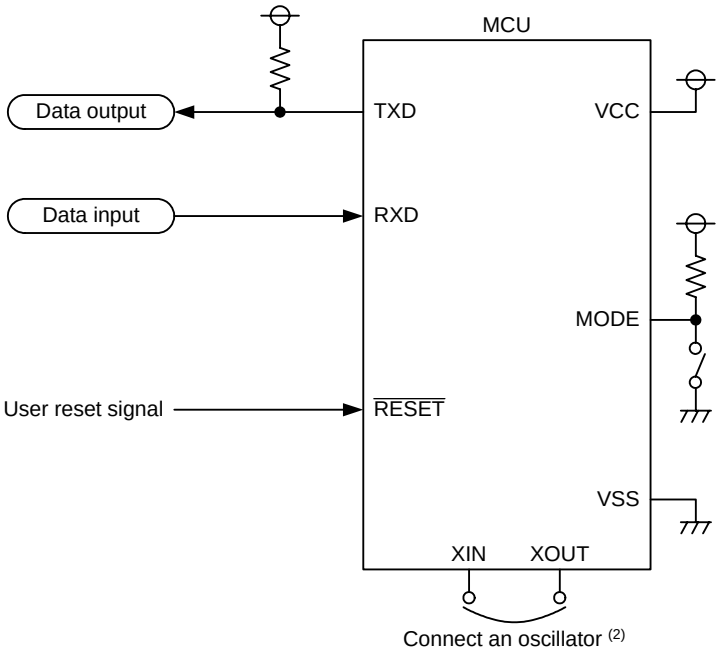
Standard serial I/O modes 2 and 3 can be used with the MCU.

See **Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator** for examples of connecting a serial programmer. Contact the manufacturer for more information on the serial programmer. Also, see the user's manual for how to use the serial programmer.

Table 23.10 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2). Figure 23.20 shows a Pin Handling Example in Standard Serial I/O Mode 2. Table 23.11 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3). Figure 23.21 shows a Pin Handling Example in Standard Serial I/O Mode 3.
When a program in the flash memory is run in user mode after the pins are handled as shown in Table 23.11 and the flash memory is rewritten with the programmer, input a high level to the MODE pin and reset the hardware.
For details on the ID code check function, see **23.3 ID Code Check Function**.

Table 23.10 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin Name	Name	I/O	Description
VCC, VSS	Power supply input	—	Apply the guaranteed program/erase voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input.
P3_1/XIN	P3_1 input/clock input	I	When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Operation is not affected even if an external oscillator is connected in the user system.
P4_5/XOUT	P4_5 input/clock output	I/O	
MODE	MODE	I/O	Input a low level.
P1_4	TXD output	O	Serial data output.
P1_6	RXD input	I	Serial data input.
Other pins			Input a low level or a high level, or leave the pin open.

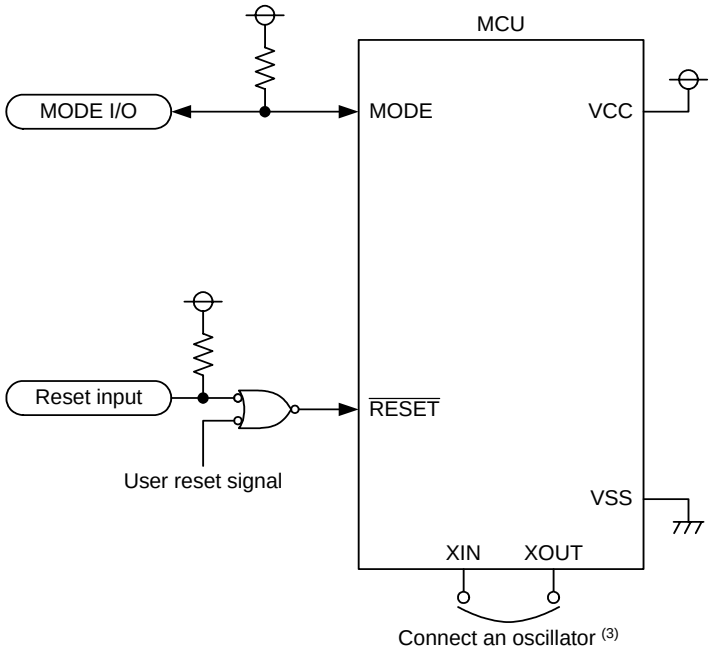


Notes:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.
2. When operating on the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. See **Appendix Figure 2.1 MF Ten Nine Cable (M3A-0652CBL) Connection Examples**.

Figure 23.20 Pin Handling Example in Standard Serial I/O Mode 2

Table 23.11 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin Name	Name	I/O	Description
VCC, VSS	Power supply input	—	Apply the guaranteed program/erase voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input.
P3_1/XIN	P3_1 input/clock input	I	When operating with the on-chip oscillator clock, it is not necessary to connect an oscillation circuit. Operation is not affected even if an external oscillator is connected in the user system.
P4_5/XOUT	P4_5 input/clock output	I/O	
MODE	MODE	I/O	Serial data I/O. Connect this pin to a flash programmer.
Other pins			Input a low level or a high level, or leave the pin open.



Notes:
1. Controlled pins and external circuits vary depending on the programmer. For details, see the programmer manual.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.
3. When operating on the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Figure 23.21 Pin Handling Example in Standard Serial I/O Mode 3

23.8 Notes on Flash Memory

23.8.1 ID Code Area Setting Example

The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

• To set 55h in all of the ID code area

```
  .org 00FFDCH
  .lword dummy | (55000000h)      ; UND
  .lword dummy | (55000000h)      ; INTO
  .lword dummy                    ; BREAK
  .lword dummy | (55000000h)      ; ADDRESS MATCH
  .lword dummy | (55000000h)      ; SET SINGLE STEP
  .lword dummy | (55000000h)      ; WDT
  .lword dummy | (55000000h)      ; RESERVE
  .lword dummy | (55000000h)      ; RESERVE
```

Programming formats vary depending on the compiler. Check the compiler manual.

23.8.2 CPU Rewrite Mode

23.8.2.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory:
UND, INTO, and BRK

23.8.2.2 Interrupts

Tables 23.12 and 23.13 list the Interrupt Handling during CPU Rewrite Operation.

Table 23.12 Interrupt Handling during CPU Rewrite Operation (EW0 Mode)

Interrupt Type	Data Flash/Program ROM	
	Suspend Enabled (FMR20 = 1)	Suspend Disabled (FMR20 = 0)
Maskable interrupt	When an interrupt request is acknowledged, interrupt handling is executed. (The interrupt vector is allocated in the RAM) The suspend state can be entered by either of the following: (1) When the FMR22 bit is 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request). The flash memory suspends auto-erase or auto-programming after td(SR-SUS). (2) When the FMR22 bit is 0 (suspend request disabled by interrupt request) and suspend is required, set the FMR21 bit to 1 (suspend request) in the interrupt handling. The flash memory suspends auto-erase or auto-programming after td(SR-SUS). While auto-erase is suspended, auto-programming and reading can be executed for any block other than the blocks being auto-erased. While auto-programming is suspended, any block other than the blocks being auto-programmed can be read. Auto-erase can be restarted by setting the FMR21 bit to 0 (restart).	Interrupt handling is executed with auto-erase or auto-programming executed (The interrupt vector is allocated in the RAM)
Address match	Do not use during auto-erasing or auto-programming.	
UND, INTO, and BRK instructions		
Single-step		
Watchdog timer	When an interrupt request is acknowledged, auto-erase or auto-programming is forcibly stopped immediately and the flash memory is reset. After the specified period, the flash memory is restarted before interrupt handling is started. Since auto-erase or auto-programming is forcibly stopped, the correct values may not be read from the block being auto-erased or the address being auto-programmed. After the flash memory is restarted, execute auto-erase again and verify it complete normally. The watchdog timer does not stop while the command is executing, so interrupt requests may be generated. Initialize the watchdog timer periodically using the erase-suspend function. Since the flash memory control registers are initialized in this case, these registers must be set again. (1)	
Oscillation stop detection		
Voltage monitor 1		

FMR20, FMR21, FMR22: Bits in FMR2 register
Note:
1. Registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated while the flash memory is busy.
When the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled) and the FMSTP bit is 1 (flash memory is stopped), registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated.

Table 23.13 Interrupt Handling during CPU Rewrite Operation (EW1 Mode)

Interrupt Type	Data Flash/Program ROM	
	Suspend Enabled (FMR20 = 1)	Suspend Disabled (FMR20 = 0)
Maskable interrupt	When an interrupt request is acknowledged, the FMR21 bit is automatically set to 1 (suspend request) if the FMR22 bit is 1 (suspend request enabled by interrupt request). The flash memory suspends auto-erase or auto-programming after td(SR-SUS) and interrupt handling is executed. When auto-erase is being suspended, auto-programming and reading can be executed for any block other than the blocks being auto-erased. When auto-programming is being suspended, any block other than the blocks being auto-programmed can be read. After interrupt handling completes, auto-erase or auto-programming can be restarted by setting the FMR21 bit is set to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.	Auto-erase or auto-programming has priority. Interrupt handling is executed after auto-erase or auto-programming.
Address match	Do not use during auto-erasing or auto-programming.	
UND, INTO, and BRK instructions		
Single-step		
Watchdog timer	When an interrupt request is acknowledged, auto-erase or auto-programming is forcibly stopped immediately and the flash memory is reset. After the specified period, the flash memory is restarted before interrupt handling is started. Since auto-erase or auto-programming is forcibly stopped, the correct values may not be read from the block being auto-erased or the address being auto-programmed. After the flash memory is restarted, execute auto-erase again and verify it complete normally. The watchdog timer does not stop while the command is executing, so interrupt requests may be generated. Initialize the watchdog timer periodically using the erase-suspend function. Since the flash memory control registers are initialized in this case, these registers must be set again. (1)	
Oscillation stop detection		
Voltage monitor 1		

FMR20, FMR21, FMR22: Bits in FMR2 register

Note:

1. Registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated while the flash memory is busy.
   When the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled) and the FMSTP bit is 1 (flash memory is stopped), registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated.

23.8.2.3 Access Methods

To set one of the following bits to 1, first write 0 and then 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
- The FMR01 or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20, FMR22, or FMR27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Interrupts must be disabled between writing 1 and then writing 0.
The FMR16 or FMR17 bit in the FMR1 register

23.8.2.4 Rewriting User ROM Area

When EW0 mode is used and the supply voltage falls while rewriting a block where a rewrite control program is stored, the rewrite control program is not be rewritten correctly. As a result, it may not be possible to rewrite the flash memory afterwards. Use standard serial I/O mode to rewrite this block.

23.8.2.5 Programming

Do not perform even a single additional write to an already programmed address.

23.8.2.6 Entering Wait Mode or Stop Mode

Do not enter wait mode or stop mode during suspend.
When the FST7 bit in the FST register is 0 (busy) while programming or erasing the flash memory, do not enter wait mode or stop mode.
Do not set the FMR27 bit to 1 while the FMSTP bit (flash memory stop bit) in the FMR0 register is 1 (flash memory is stopped).

23.8.2.7 Flash Memory Programming and Erase Voltages

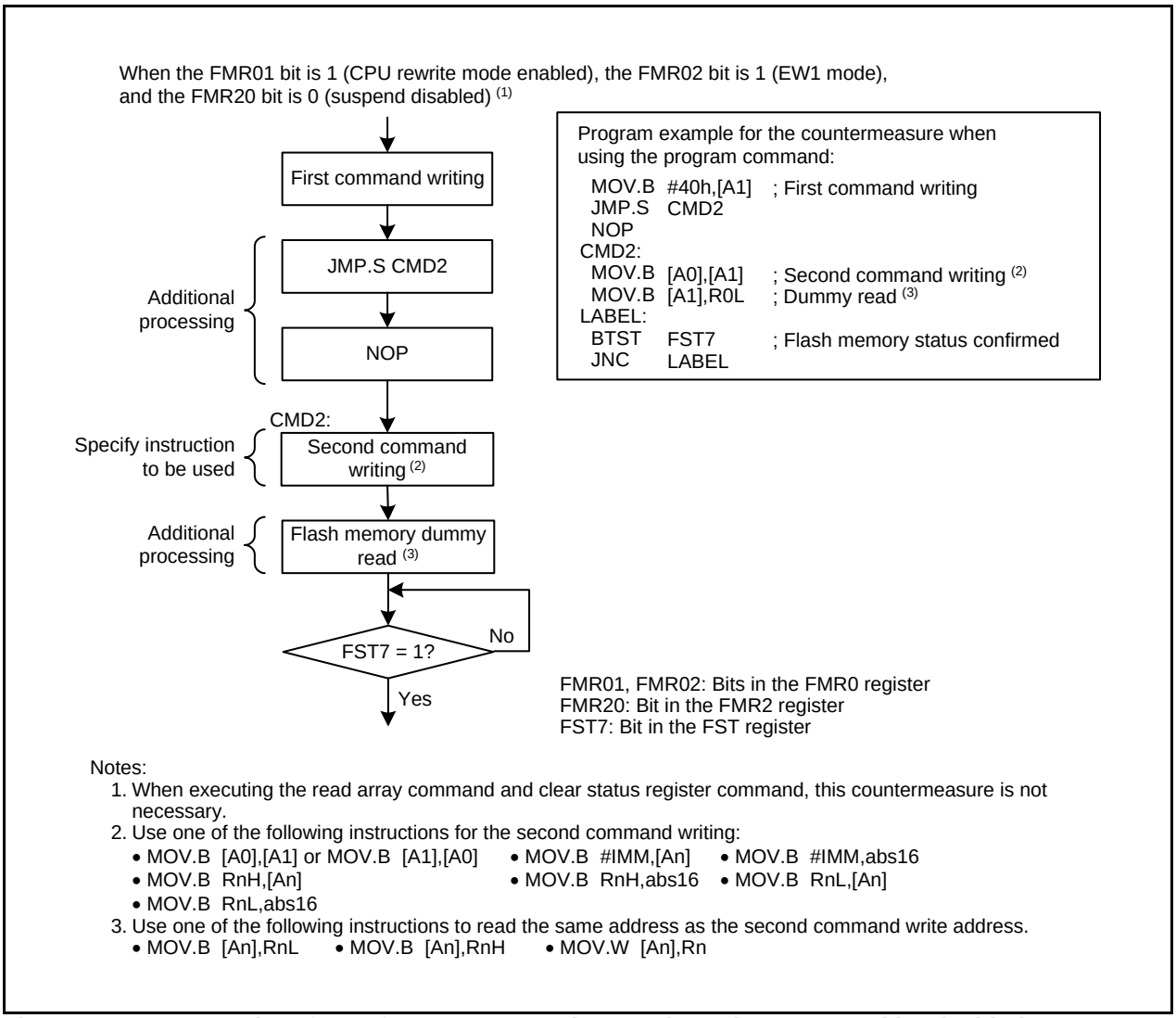
When performing a program/erase operation, use a VCC supply voltage in the range of 1.8 V to 5.5 V. Do not perform a program/erase operation at less than 1.8 V.

23.8.2.8 Block Blank Check

Do not execute a block blank check command during erase-suspend.

23.8.2.9 EW1 Mode

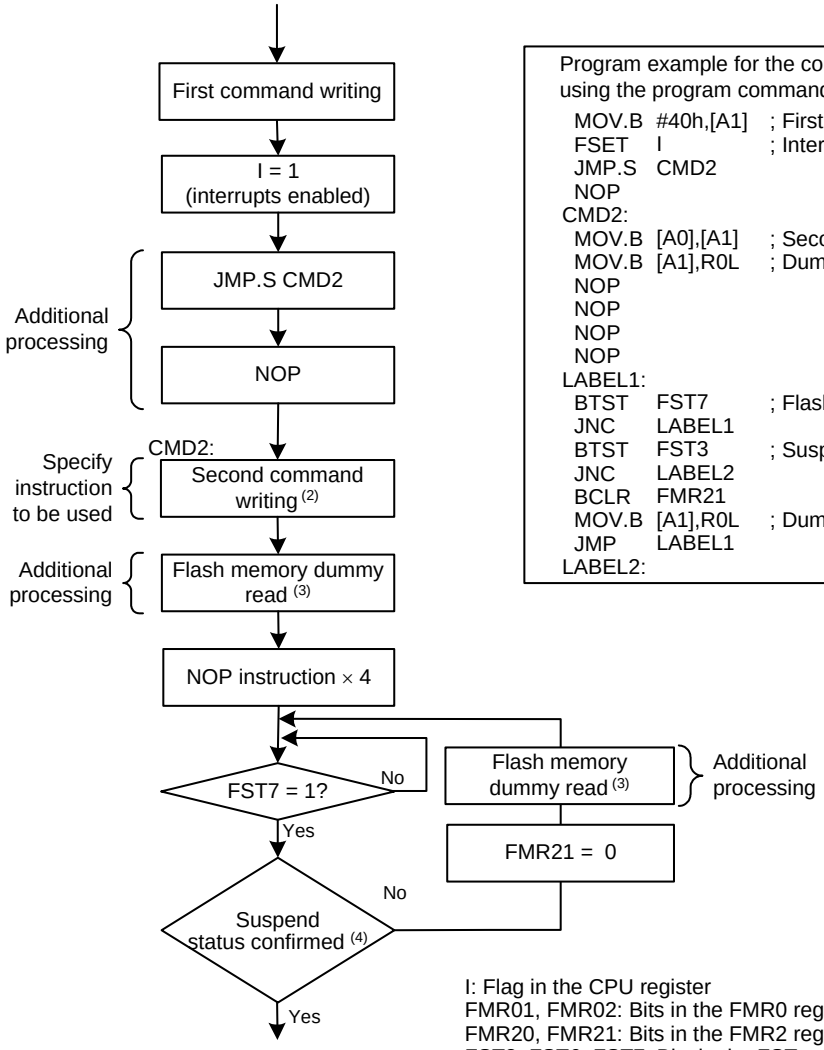
When setting the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled) and the FMR02 bit to 1 (EW1 mode) to execute CPU rewrite mode, follow the procedure below in EW1 mode. Figure 23.22 shows the Procedure for Software Command Execution When Suspend is Disabled. Figure 23.23 shows the Procedure for Software Command Execution When Suspend is Enabled.



Notes:
1. When executing the read array command and clear status register command, this countermeasure is not necessary.
2. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
3. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn

Figure 23.22 Procedure for Software Command Execution When Suspend is Disabled

When the FMR01 bit is 1 (CPU rewrite mode enabled), the FMR02 bit is 1 (EW1 mode), and the FMR20 bit is 1 (suspend enabled) (1)




```
Program example for the countermeasure when
using the program command:
  MOV.B  #40h,[A1]   ; First command writing
  FSET   I           ; Interrupts enabled
  JMP.S  CMD2
  NOP
CMD2:
  MOV.B  [A0],[A1]   ; Second command writing (2)
  MOV.B  [A1],R0L    ; Dummy read (3)
  NOP
  NOP
  NOP
  NOP
LABEL1:
  BTST   FST7        ; Flash memory status confirmed
  JNC    LABEL1
  BTST   FST3        ; Suspend status confirmed (4)
  JNC    LABEL2
  BCLR   FMR21
  MOV.B  [A1],R0L    ; Dummy read (3)
  JMP    LABEL1
LABEL2:
```

I: Flag in the CPU register
FMR01, FMR02: Bits in the FMR0 register
FMR20, FMR21: Bits in the FMR2 register
FST3, FST6, FST7: Bits in the FST register

Notes:
1. When executing the read array command and clear status register command, this countermeasure is not necessary.
2. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
3. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn
4. Confirm the suspend status using the FST3 bit for the program command, and the FST6 bit for the block erase command.

Figure 23.23 Procedure for Software Command Execution When Suspend is Enabled

23.8.3 Notes on Flash Memory Stop and Operation Transition

(1) Do not enter stop mode while the FMSTP bit is 1 (the flash memory is stopped).
(2) Do not enter wait mode while the FMSTP bit is 1 (the flash memory is stopped) and the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
(3) Do not enter flash memory stop state for 42 μs after entering from flash memory stop state to flash memory operation state. And do not rewrite the LOCODIS bit in the OCOCR register for 42 μs.

Conditions when entering flash memory operation state from flash memory stop state.
• Set the FMSTP bit to 0 (the flash memory operates).
• Return from wait mode while the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
• Return from stop mode.

Conditions when entering flash memory stop state from flash memory operation state.
• Set the FMSTP bit to 1 (the flash memory is stopped).
• Enter wait mode while the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
• Enter stop mode.

24. Electrical Characteristics

Table 24.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Power supply voltage			-0.3 to 6.5	V
V_I	Input voltage	XIN	XIN-XOUT oscillation on (oscillation circuit used) (1)	-0.3 to 1.9	V
			XIN-XOUT oscillation off (oscillation circuit not used) (1)	-0.3 to Vcc + 0.3	V
		Other pins		-0.3 to Vcc + 0.3	V
V_O	Output voltage	XOUT	XIN-XOUT oscillation on (oscillation circuit used) (1)	-0.3 to 1.9	V
			XIN-XOUT oscillation off (oscillation circuit not used) (1)	-0.3 to Vcc + 0.3	V
		Other pins		-0.3 to Vcc + 0.3	V
P_d	Power consumption		-40 °C ≤ Topr ≤ 85 °C	500	mW
T_{opr}	Operating ambient temperature			-20 to 85 (N version)/ -40 to 85 (D version)	°C
T_{stg}	Storage temperature			-60 to 150	°C

Note:
1. When the oscillation circuit is used: bits CKPT1 to CKPT0 in the EXCKCR register are set to 11b
   When the oscillation circuit is not used: bits CKPT1 to CKPT0 in the EXCKCR register are set to any value other than 11b

Table 24.2 Recommended Operating Conditions

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Power supply voltage			1.8	—	5.5	V
V_{SS}/AV_{SS}	Power supply voltage			—	0	—	V
V_{IH}	Input high voltage	Other than CMOS input		0.8 Vcc	—	Vcc	V
		CMOS input	4.0 V ≤ Vcc ≤ 5.5 V	0.65 Vcc	—	Vcc	V
			2.7 V ≤ Vcc < 4.0 V	0.7 Vcc	—	Vcc	V
			1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
V_{IL}	Input low voltage	Other than CMOS input		0	—	0.2 Vcc	V
		CMOS input	4.0 V ≤ Vcc ≤ 5.5 V	0	—	0.4 Vcc	V
			2.7 V ≤ Vcc < 4.0 V	0	—	0.3 Vcc	V
			1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
$I_{OH(sum)}$	Peak sum output high current	Sum of all pins $I_{OH(peak)}$		—	—	-160	mA
$I_{OH(sum)}$	Average sum output high current	Sum of all pins $I_{OH(avg)}$		—	—	-80	mA
$I_{OH(peak)}$	Peak output high current		When drive capacity is low	—	—	-10	mA
			When drive capacity is high (5)	—	—	-40	mA
$I_{OH(avg)}$	Average output high current		When drive capacity is low	—	—	-5	mA
			When drive capacity is high (5)	—	—	-20	mA
$I_{OL(sum)}$	Peak sum output low current	Sum of all pins $I_{OL(peak)}$		—	—	160	mA
$I_{OL(sum)}$	Average sum output low current	Sum of all pins $I_{OL(avg)}$		—	—	80	mA
$I_{OL(peak)}$	Peak output low current		When drive capacity is low	—	—	10	mA
			When drive capacity is high (5)	—	—	40	mA
$I_{OL(avg)}$	Average output low current		When drive capacity is low	—	—	5	mA
			When drive capacity is high (5)	—	—	20	mA
$f_{(XIN)}$	XIN oscillation frequency		2.7 V ≤ Vcc ≤ 5.5 V	2	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	2	—	5	MHz
	XIN clock input oscillation frequency		2.7 V ≤ Vcc ≤ 5.5 V	0	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	0	—	5	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency		1.8 V ≤ Vcc ≤ 5.5 V	—	32.768	—	kHz
fHOCO	High-speed on-chip oscillator oscillation frequency (3)		1.8 V ≤ Vcc ≤ 5.5 V	—	20	—	MHz
fLOCO	Low-speed on-chip oscillator oscillation frequency (4)		1.8 V ≤ Vcc ≤ 5.5 V	—	125	—	kHz
—	System clock frequency		2.7 V ≤ Vcc ≤ 5.5 V	—	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	—	—	5	MHz
f_S	CPU clock frequency		2.7 V ≤ Vcc ≤ 5.5 V	0	—	20	MHz
			1.8 V ≤ Vcc < 2.7 V	0	—	5	MHz

Notes:
1. Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. For details, see **Table 24.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
4. For details, see **Table 24.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics**.
5. The pins with high drive capacity are P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, and P3_7.

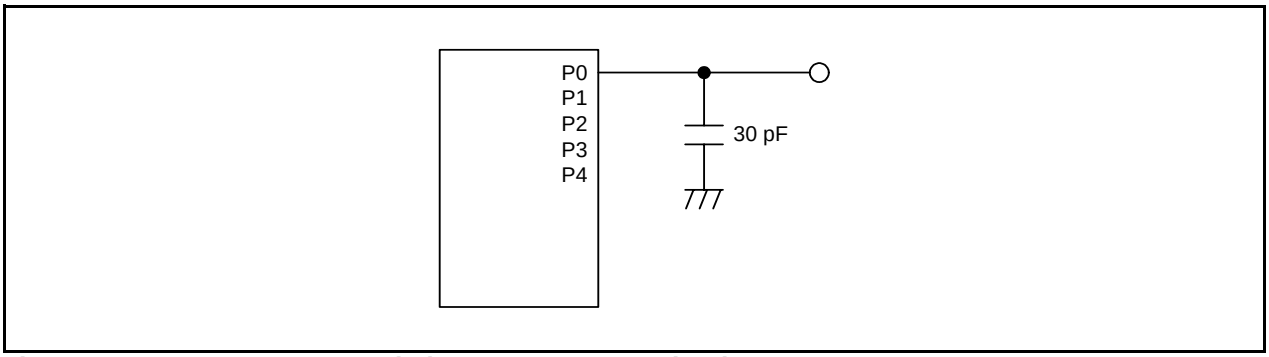


Figure 24.1 Ports P0 to P4 Timing Measurement Circuit

Table 24.3 A/D Converter Characteristics

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
—	Resolution			—	—	10	Bit
—	Absolute accuracy	AVcc = 5.0 V	AN0 to AN7 input	—	—	±3	LSB
		AVcc = 3.0 V	AN0 to AN7 input	—	—	±5	LSB
		AVcc = 1.8 V	AN0 to AN7 input	—	—	±5	LSB
—	A/D conversion clock	4.0 V ≤ AVcc ≤ 5.5 V (2)		2	—	20	MHz
		3.2 V ≤ AVcc ≤ 5.5 V (2)		2	—	16	MHz
		2.7 V ≤ AVcc ≤ 5.5 V (2)		2	—	10	MHz
		1.8 V ≤ AVcc ≤ 5.5 V (2)		2	—	5	MHz
—	Permissible signal source impedance				3		kΩ
t_{CONV}	Conversion time	AVcc = 5.0 V, ϕAD = 20 MHz		2.20	—	—	µs
t_{SAMP}	Sampling time	ϕAD = 20 MHz		0.80	—	—	µs
V_{IA}	Analog input voltage			0	—	AVcc	V

Notes:
1. Vcc/AVcc = 1.8 V to 5.5 V and Vss = 0 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in stop mode, or when the flash memory is in low-current-consumption read mode or stopped. Do not perform A/D conversion in these states. Do not enter these states during A/D conversion.

Table 24.4 Comparator B Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	Vcc - 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		-0.3	—	Vcc + 0.3	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (2)	V_I = Vref ± 100 mV	—	0.1	—	µs
I_{CMP}	Comparator operating current	Vcc = 5.0 V	—	17.5	—	µA

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. When the digital filter is disabled.

Table 24.5 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte programming time (program/erase endurance ≤ 1,000 times)		—	80	—	µs
—	Byte programming time (program/erase endurance > 1,000 times)		—	160	—	µs
—	Block erase time		—	0.12	—	s
$t_{d(SR-SUS)}$	Transition time to suspend		—	—	0.25 + CPU clock × 3 cycles	ms
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST READY)}$	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program/erase voltage		1.8	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program/erase temperature		0	—	60	°C
—	Data hold time (7)	Ambient temperature = 85 °C	10	—	—	years

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = 0 °C to 60 °C, unless otherwise specified.
2. Definition of program/erase endurance
   The number of program/erase cycles is defined on a per-block basis.
   If the number of cycles is 10,000, each block can be erased 10,000 times.
   For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. Note, however, that the same address must not be programmed more than once before completion of an erase (overwriting prohibited).
3. This indicates the number of times up to which all electrical characteristics can be guaranteed after the last programming/erase operation. Operation is guaranteed for any number of operations in the range of 1 to the specified minimum (Min).
4. In a system that executes multiple programming operations, the actual erase count can be reduced by shifting the write addresses in sequence and programming so that as much of the flash memory as possible is used before performing an erase operation. For example, when programming in 16-byte units, the effective number of rewrites can be minimized by programming up to 128 units before erasing them all in one operation. It is also advisable to retain data on the number of erase operations for each block and establish a limit for the number of erase operations performed.
5. If an error occurs during a block erase, execute a clear status register command and then a block erase command at least three times until the erase error does not occur.
6. For information on the program/erase failure rate, contact a Renesas technical support representative.
7. The data hold time includes the time that the power supply is off and the time the clock is not supplied.

Table 24.6 Flash Memory (Blocks A and B of Data Flash) Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte programming time		—	150	—	µs
—	Block erase time		—	0.05	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	0.25 + CPU clock × 3 cycles	ms
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program/erase voltage		1.8	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program/erase temperature		-20 (N version)	—	85	°C
			-40 (D version)	—	85	°C
—	Data hold time (7)	Ambient temperature = 85 °C	10	—	—	years

Notes:
1. Vcc = 2.7 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. Definition of program/erase endurance
   The number of program/erase cycles is defined on a per-block basis.
   If the number of cycles is 10,000, each block can be erased 10,000 times.
   For example, if 1,024 cycles of 1-byte-write are performed to different addresses in 1 Kbyte of block A, and then the block is erased, the number of cycles is counted as one. Note, however, that the same address must not be programmed more than once before completion of an erase (overwriting prohibited).
3. This indicates the number of times up to which all electrical characteristics can be guaranteed after the last programming/erase operation. Operation is guaranteed for any number of operations in the range of 1 to the specified minimum (Min).
4. In a system that executes multiple program operations, the actual erase count can be reduced by shifting the write addresses in sequence and programming so that as much of the flash memory as possible is used before performing an erase operation. For example, when programming in 16-byte units, the effective number of rewrites can be minimized by programming up to 128 units before erasing them all in one operation. It is also advisable to retain data on the number of erase operations for each block and establish a limit for the number of erase operations performed.
5. If an error occurs during a block erase, execute a clear status register command and then a block erase command at least three times until the erase error does not occur.
6. For information on the program/erase failure rate, contact a Renesas technical support representative.
7. The data hold time includes the time that the power supply is off and the time the clock is not supplied.

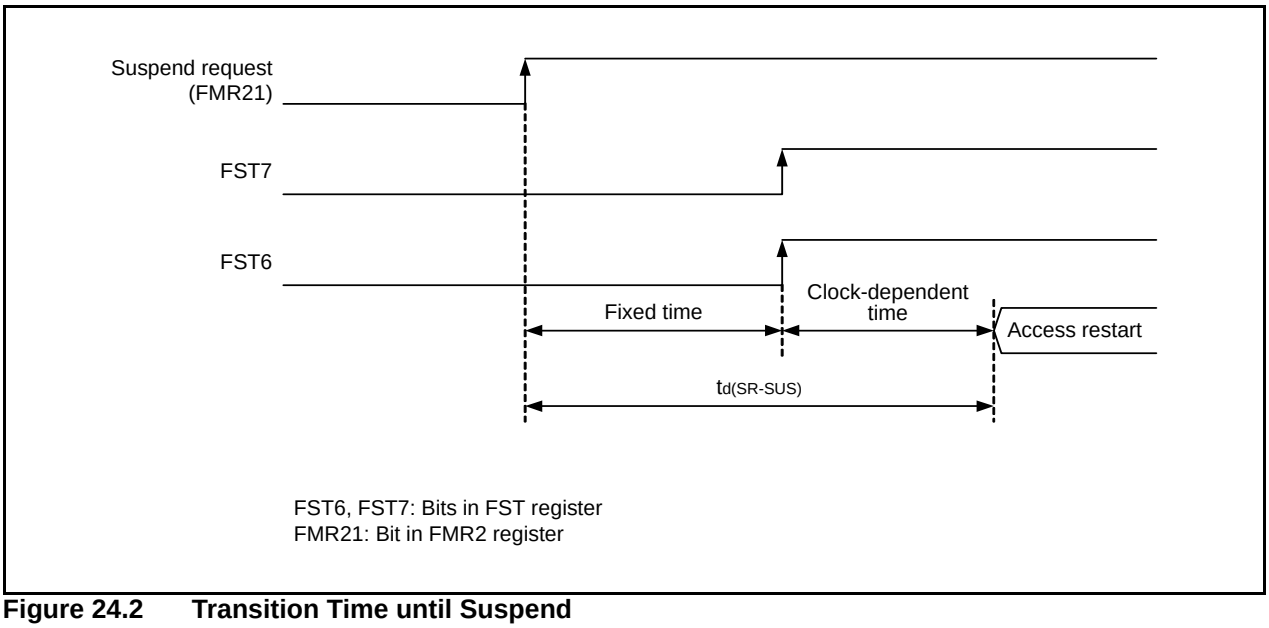


Figure 24.2 Transition Time until Suspend

Table 24.7 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (3)	When Vcc decreases from 5 V to (Vdet0_0 - 0.1) V	—	30	—	µs
—	Self power consumption in voltage detection circuit	VC0E = 1, Vcc = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Wait time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. The response time is from when the voltage passes Vdet0 until the voltage monitor 0 reset is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC0E bit in the VCA2 register is set to 0 and then 1.

Table 24.8 Voltage Detection 1 Circuit Electrical Characteristics

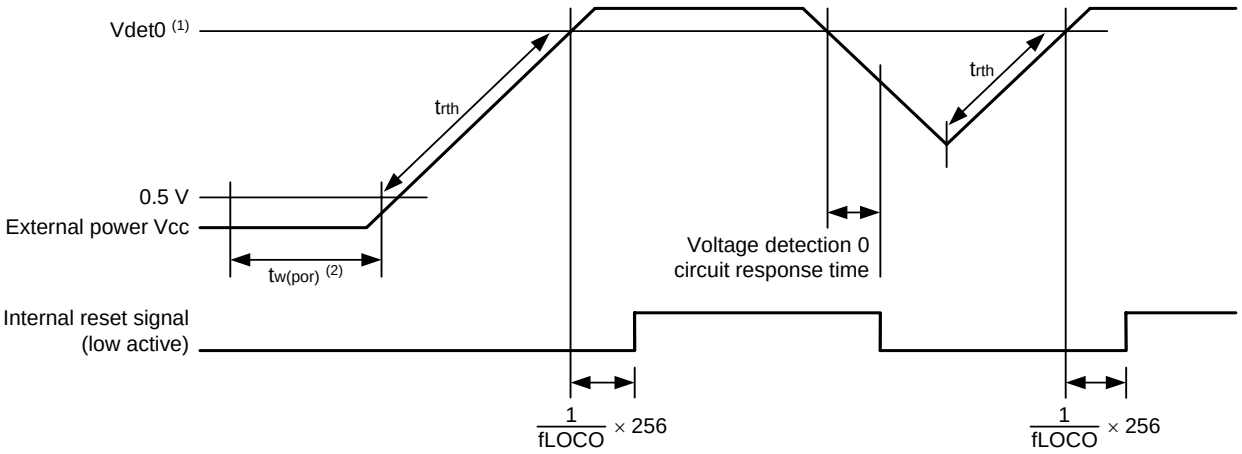
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_1 (2)	When Vcc decreases	2.15	2.35	2.55	V
	Voltage detection level Vdet1_3 (2)	When Vcc decreases	2.45	2.65	2.85	V
	Voltage detection level Vdet1_5 (2)	When Vcc decreases	2.75	2.95	3.15	V
	Voltage detection level Vdet1_7 (2)	When Vcc decreases	3.00	3.25	3.55	V
	Voltage detection level Vdet1_9 (2)	When Vcc decreases	3.30	3.55	3.85	V
	Voltage detection level Vdet1_B (2)	When Vcc decreases	3.60	3.85	4.15	V
	Voltage detection level Vdet1_D (2)	When Vcc decreases	3.90	4.15	4.45	V
	Voltage detection level Vdet1_F (2)	When Vcc decreases	4.20	4.45	4.75	V
—	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_1 to Vdet1_5 selected	—	0.07	—	V
		Vdet1_7 to Vdet1_F selected	—	0.10	—	V
—	Voltage detection 1 circuit response time (3)	When Vcc decreases from 5 V to (Vdet1_0 - 0.1) V	—	60	150	µs
—	Self power consumption in voltage detection circuit	VC1E = 1, Vcc = 5.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Wait time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version).
2. Select the voltage detection level with bits VD1S1 to VD1S3 in the VD1LS register.
3. The response time is from when the voltage passes Vdet1 until the voltage monitor 1 interrupt request is generated.
4. The wait time is necessary for the voltage detection circuit to operate when the VC1E bit in the VCA2 register is set to 0 and then 1.

Table 24.9 Power-On Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power Vcc rise gradient		0	—	50,000	mV/msec

Notes:
1. The measurement condition is Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. To use the power-on reset function, enable the voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. For details, see **7. Voltage Detection Circuit**.
2. $t_{w(por)}$ is required for a power-on reset to be enabled with the external power Vcc held below the valid voltage (0.5 V) to enable a power-on reset. When Vcc decreases with voltage monitor 0 reset disabled and then turns on, maintain $t_{w(por)}$ for 1 ms or more.

Figure 24.3 Power-On Reset Circuit Electrical Characteristics

Table 24.10 High-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset is cleared	Vcc = 1.8 V to 5.5 V, -20 °C ≤ Topr ≤ 85 °C	19.2	20.0	20.8	MHz
		Vcc = 1.8 V to 5.5 V, -40 °C ≤ Topr ≤ 85 °C	19.0	20.0	21.0	MHz
	High-speed on-chip oscillator frequency when the FR18S0 register adjustment value is written into the FRV1 register and the FR18S1 register adjustment value into the FRV2 register (2)	Vcc = 1.8 V to 5.5 V, -20 °C ≤ Topr ≤ 85 °C	17.694	18.432	19.169	MHz
		Vcc = 1.8 V to 5.5 V, -40 °C ≤ Topr ≤ 85 °C	17.510	18.432	19.353	MHz
—	Oscillation stabilization time		—	—	30	µs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25 °C	—	530	—	µA

Notes:
1. Vcc = 1.8 V to 5.5 V, Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

Table 24.11 Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fLOCO	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stabilization time		—	—	35	µs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25 °C	—	2	—	µA

Note:
1. Vcc = 1.8 V to 5.5 V, Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.

Table 24.12 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2,000	µs

Notes:
1. The measurement condition is Vcc = 1.8 V to 5.5 V and Topr = 25 °C.
2. Wait time until the internal power supply generation circuit stabilizes during power-on.

Table 24.13 Timing Requirements of Synchronous Serial Communication Unit (SSU)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	—	—	t_{CYC} (2)
t_{HI}	SSCK clock high width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK clock low width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{FALL}	SSCK clock falling time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{SU}	SSO, SSI data input setup time			100	—	—	ns
t_H	SSO, SSI data input hold time			1	—	—	t_{CYC} (2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1 t_{CYC} + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1 t_{CYC} + 50	—	—	ns
t_{OD}	SSO, SSI data output delay time			—	—	1	t_{CYC} (2)
t_{SA}	SSI slave access time		2.7 V ≤ Vcc ≤ 5.5 V	—	—	1.5 t_{CYC} + 100	ns
			1.8 V ≤ Vcc < 2.7 V	—	—	1.5 t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ Vcc ≤ 5.5 V	—	—	1.5 t_{CYC} + 100	ns
			1.8 V ≤ Vcc < 2.7 V	—	—	1.5 t_{CYC} + 200	ns

Notes:
1. Vcc = 1.8 V to 5.5 V, Vss = 0 V, and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. 1 t_{CYC} = 1/f1 (s)

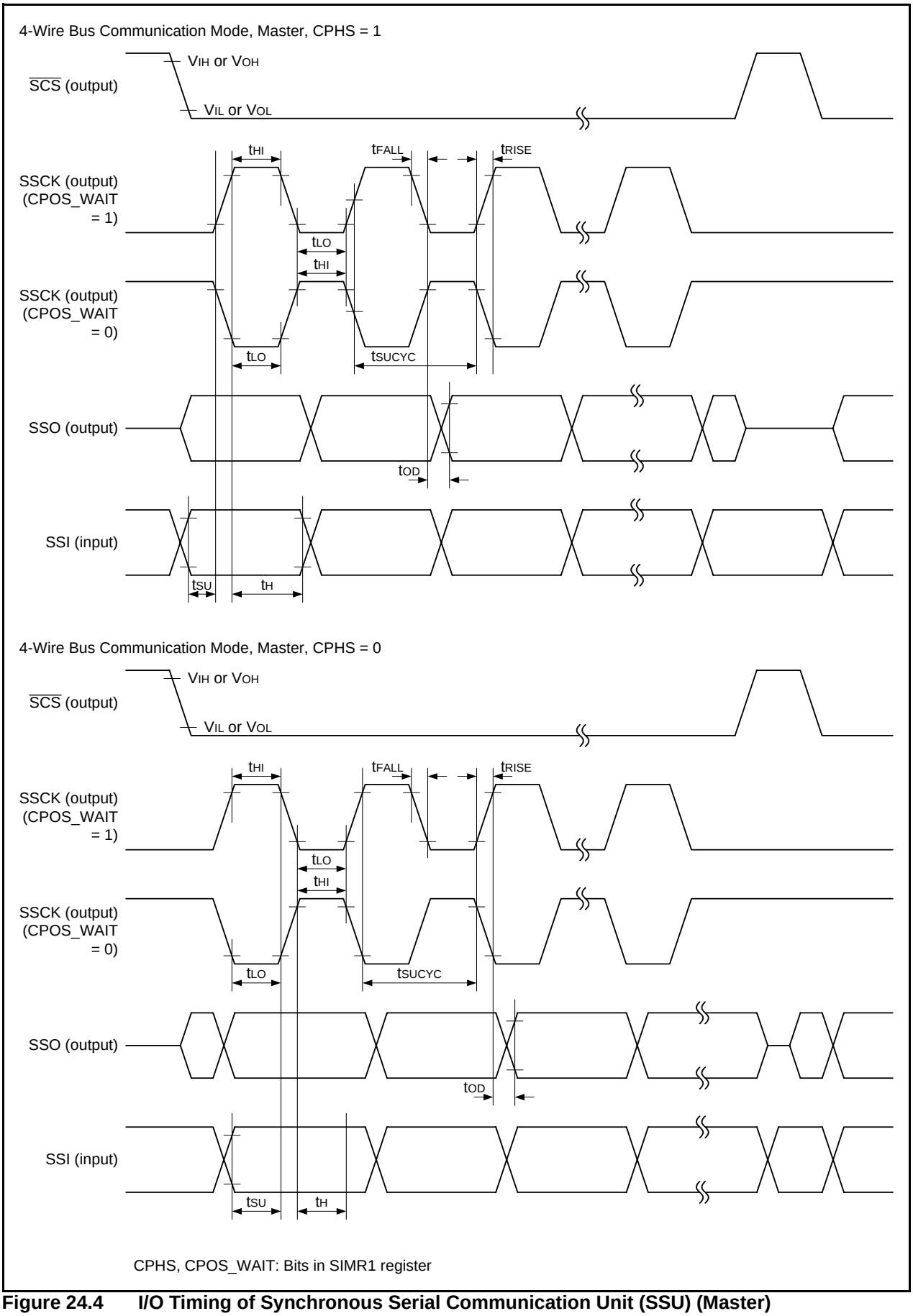


Figure 24.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

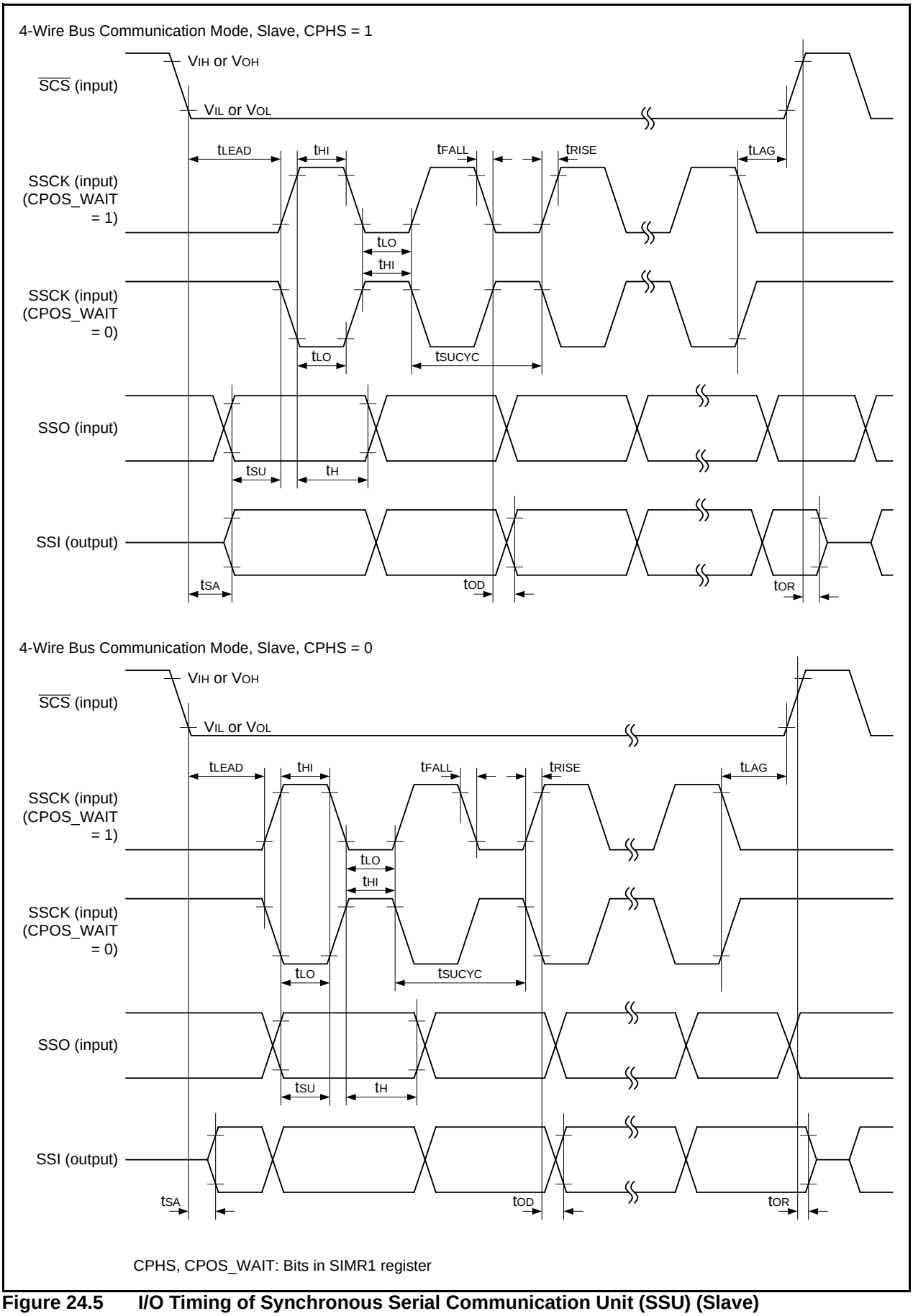


Figure 24.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

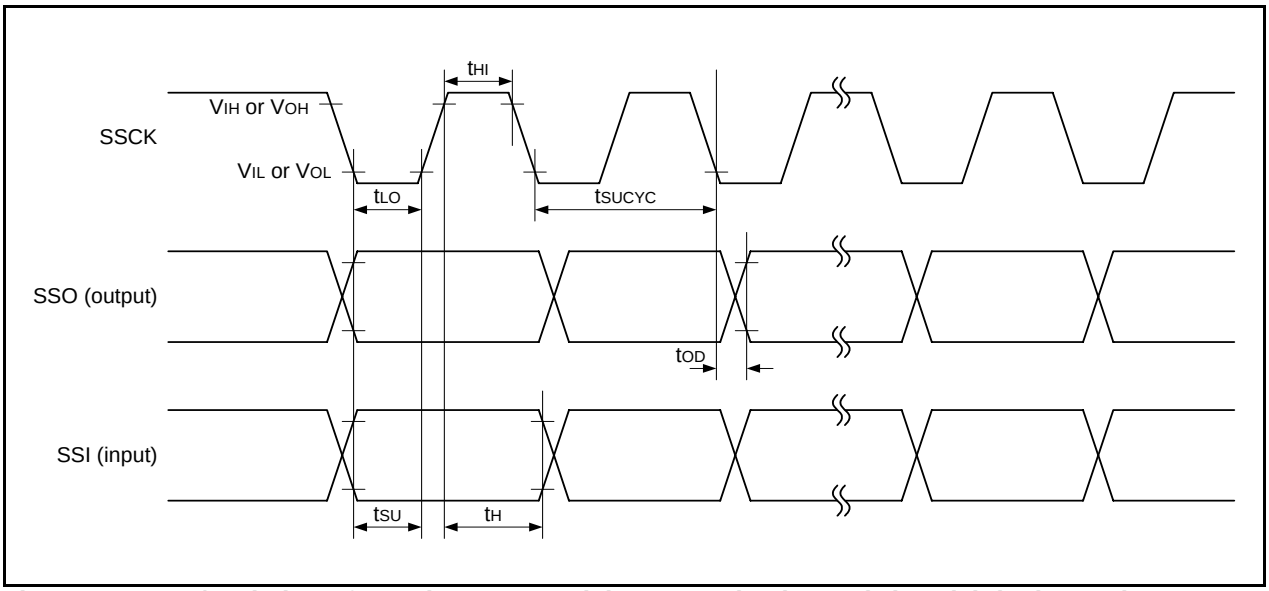
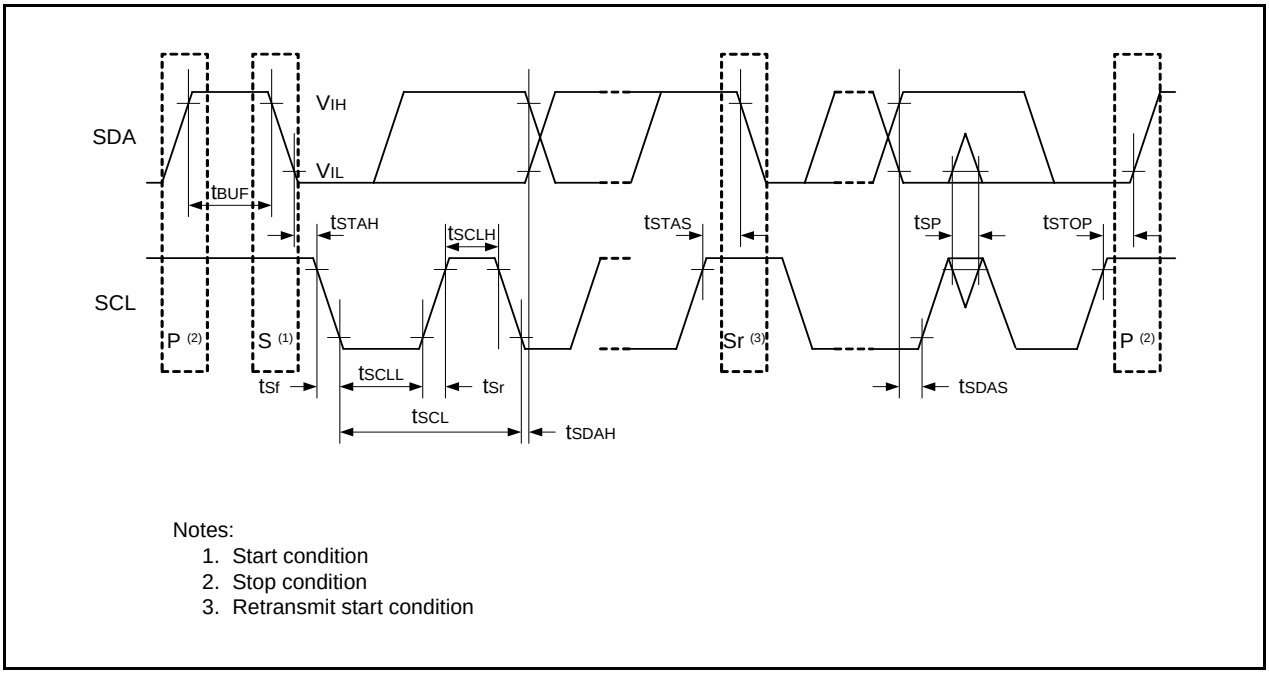


Figure 24.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 24.14 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		12 t_{CYC} + 600 (2)	—	—	ns
t_{SCLH}	SCL input high width		3 t_{CYC} + 300 (2)	—	—	ns
t_{SCLL}	SCL input low width		5 t_{CYC} + 500 (2)	—	—	ns
t_{sf}	SCL, SDA input fall time		—	—	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		—	—	1 t_{CYC} (2)	ns
t_{BUF}	SDA input bus-free time		5 t_{CYC} (2)	—	—	ns
t_{STAH}	Start condition input hold time		3 t_{CYC} (2)	—	—	ns
t_{STAS}	Retransmit start condition input setup time		3 t_{CYC} (2)	—	—	ns
t_{STOP}	Stop condition input setup time		3 t_{CYC} (2)	—	—	ns
t_{SDAS}	Data input setup time		1 t_{CYC} + 40 (2)	—	—	ns
t_{SDAH}	Data input hold time		10	—	—	ns

Notes:
1. Vcc = 1.8 V to 5.5 V, Vss = 0 V, and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified.
2. 1 t_{CYC} = 1/f1 (s)



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 24.7 I/O Timing of I²C bus Interface

Table 24.15 DC Characteristics (1) [4.0 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -20 mA	Vcc - 2.0	—	Vcc	V
			When drive capacity is low	I_{OH} = -5 mA	Vcc - 2.0	—	Vcc	V
		P0_0, P0_1, P0_2, P0_3, P0_4, P0_5, P0_6, P0_7, P1_0, P1_1, P1_6, P1_7, P2_0, P2_1, P2_2, P3_1, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -5 mA	Vcc - 2.0	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 20 mA	—	—	2.0	V
			When drive capacity is low	I_{OL} = 5 mA	—	—	2.0	V
		P0_0, P0_1, P0_2, P0_3, P0_4, P0_5, P0_6, P0_7, P1_0, P1_1, P1_6, P1_7, P2_0, P2_1, P2_2, P3_1, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 5 mA	—	—	2.0	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, KI0, KI1, KI2, KI3, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 5 V		0.1	1.2	—	V
		$\overline{RESET}$	Vcc = 5 V		0.1	1.2	—	V
I_{IH}	Input high current		V_I = 5 V, Vcc = 5.0 V		—	—	5.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 5.0 V		—	—	-5.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	14	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 4.0 V ≤ Vcc ≤ 5.5 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 20 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Table 24.16 DC Characteristics (2) [4.0 V ≤ Vcc ≤ 5.5 V] (Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other				
			XIN (2)	XCIN	High-Speed	Low-Speed				Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—		—	3.5	7.0	mA
			16 MHz	Off	Off	125 kHz	No division	—		—	2.8	6.0	mA
			10 MHz	Off	Off	125 kHz	No division	—		—	1.8	—	mA
			20 MHz	Off	Off	125 kHz	Division by 8	—		—	2.0	—	mA
			16 MHz	Off	Off	125 kHz	Division by 8	—		—	1.7	—	mA
			10 MHz	Off	Off	125 kHz	Division by 8	—		—	1.1	—	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division			—	4.0	7.5	mA
			Off	Off	20 MHz	125 kHz	Division by 8			—	2.5	—	mA
			Off	Off	4 MHz (4)	125 kHz	Division by 16	MSTTRC = 1		—	1.0	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Division by 8	FMR27 = 1 LPE = 0		—	70	270	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	—	FMR27 = 1 LPE = 0		—	65	270	µA
			Off	32 kHz	Off	Off	—	FMSTP = 1 LPE = 0	Flash memory stopped during program operation in RAM	—	45	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1	Peripheral clock supplied during WAIT instruction execution	—	15	100	µA
			Off	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	5.0	90	µA
			Off	32 kHz	Off	Off	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 25 °C Peripheral clock stopped	—	1.0	4.0	µA
			Off	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 85 °C Peripheral clock stopped	—	1.9	—	µA

Notes:
1. Vcc = 4.0 V to 5.5 V, single-chip mode, output pins are open, and other pins are connected to Vss.
2. When the XIN input is a square wave.
3. Vcc = 5.0 V
4. Set the system clock to 4 MHz with the PHISEL register.

Timing Requirements (Vcc = 5 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified) [Vcc = 5 V]

Table 24.17 External Clock Input (XIN, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns
$t_{c(XCIN)}$	XCIN input cycle time	20	—	µs
$t_{WH(XCIN)}$	XCIN input high width	10	—	µs
$t_{WL(XCIN)}$	XCIN input low width	10	—	µs

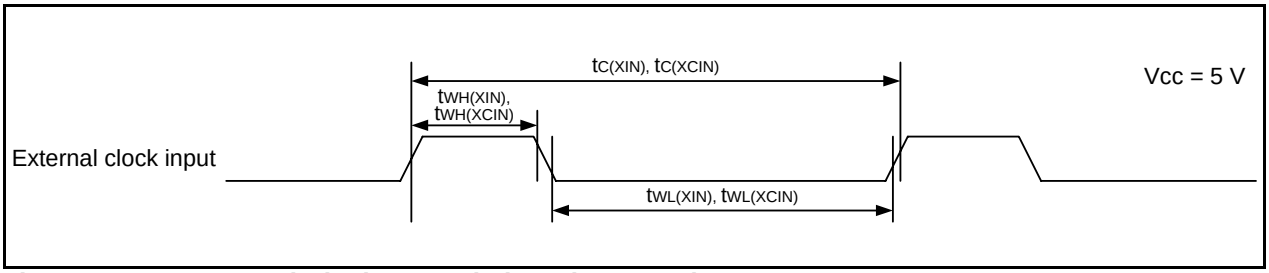


Figure 24.8 External Clock Input Timing Diagram When Vcc = 5 V

Table 24.18 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	100	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	40	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	40	—	ns

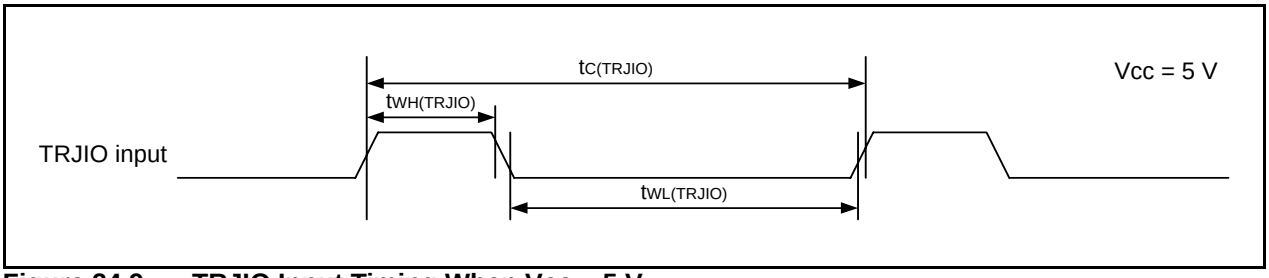


Figure 24.9 TRJIO Input Timing When Vcc = 5 V

Table 24.19 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	—	ns
$t_{W(CKH)}$	CLKi input high width	100	—	ns
$t_{W(CKL)}$	CLKi input low width	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	50	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 1

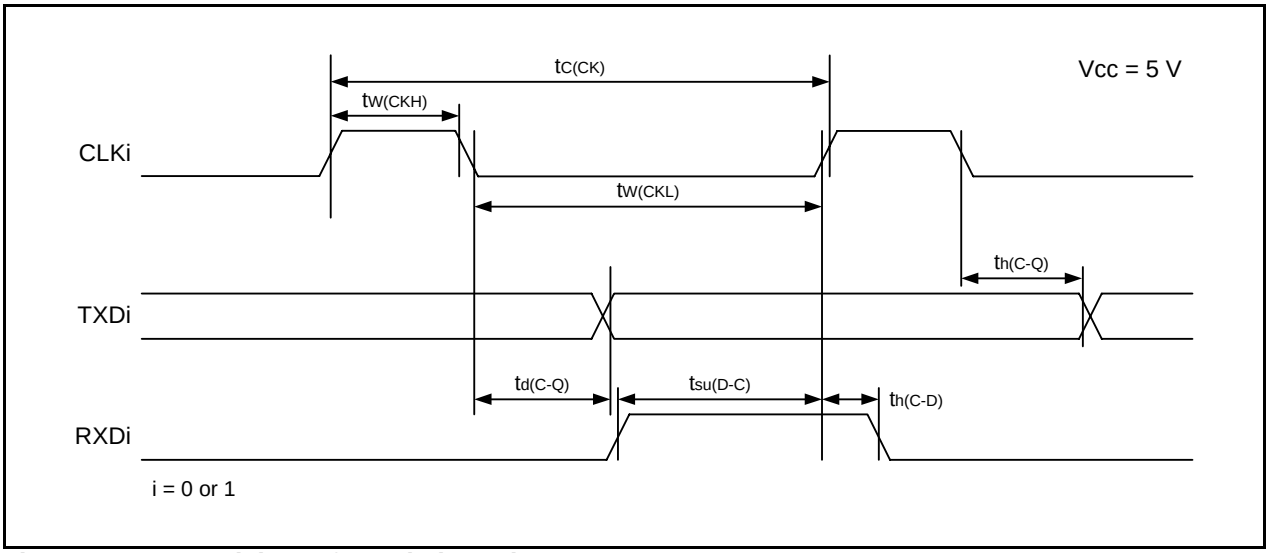


Figure 24.10 Serial Interface Timing When Vcc = 5 V

Table 24.20 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	250 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

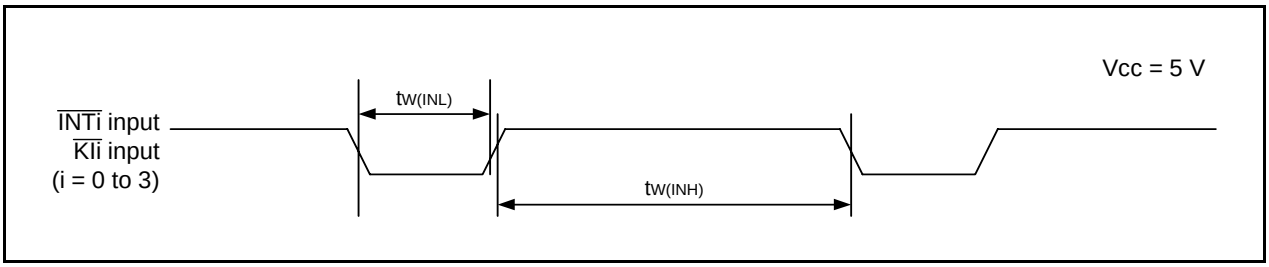


Figure 24.11 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 5 V

Table 24.21 DC Characteristics (3) [2.7 V ≤ Vcc < 4.0 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -5 mA	Vcc - 0.5	—	Vcc	V
			When drive capacity is low	I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
		P0_0, P0_1, P0_2, P0_3, P0_4, P0_5, P0_6, P0_7, P1_0, P1_1, P1_6, P1_7, P2_0, P2_1, P2_2, P3_1, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 5 mA	—	—	0.5	V
			When drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		P0_0, P0_1, P0_2, P0_3, P0_4, P0_5, P0_6, P0_7, P1_0, P1_1, P1_6, P1_7, P2_0, P2_1, P2_2, P3_1, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, KI0, KI1, KI2, KI3, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 3 V		0.1	0.4	—	V
		$\overline{RESET}$	Vcc = 3 V		0.1	0.5	—	V
I_{IH}	Input high current		V_I = 3 V, Vcc = 3.0 V		—	—	4.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 3.0 V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	14	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 2.7 V ≤ Vcc < 4.0 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 10 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Table 24.22 DC Characteristics (4) [2.7 V ≤ Vcc < 4.0 V] (Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

Symbol	Parameter	Condition										Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Standard			
			XIN (2)	XCIN	High-Speed	Low-Speed				Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—		—	3.5	7.0	mA
			16 MHz	Off	Off	125 kHz	No division	—		—	2.7	6.0	mA
			10 MHz	Off	Off	125 kHz	No division	—		—	1.7	5.0	mA
			20 MHz	Off	Off	125 kHz	Division by 8	—		—	1.9	—	mA
			16 MHz	Off	Off	125 kHz	Division by 8	—		—	1.6	—	mA
			10 MHz	Off	Off	125 kHz	Division by 8	—		—	1.0	4.5	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz	125 kHz	No division			—	3.9	7.5	mA
			Off	Off	20 MHz	125 kHz	Division by 8			—	2.5	—	mA
			Off	Off	10 MHz (4)	125 kHz	No division			—	2.4	—	mA
			Off	Off	10 MHz (4)	125 kHz	Division by 8			—	1.6	—	mA
			Off	Off	4 MHz (4)	125 kHz	Division by 16	MSTTRC = 1		—	1.0	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Division by 8	FMR27 = 1 LPE = 0		—	60	260	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	—	FMR27 = 1 LPE = 0		—	60	260	µA
			Off	32 kHz	Off	Off	—	FMSTP = 1 LPE = 0	Flash memory stopped during program operation in RAM	—	40	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1	Peripheral clock supplied during WAIT instruction execution	—	15	90	µA
			Off	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	5.0	80	µA
			Off	32 kHz	Off	Off	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	3.2	—	µA
		Stop mode	Off	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 25 °C Peripheral clock stopped	—	1.0	4.0	µA
			Off	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 85 °C Peripheral clock stopped	—	1.7	—	µA

Notes:
1. Vcc = 2.7 V to 4.0 V, single-chip mode, output pins are open, and other pins are connected to Vss.
2. When the XIN input is a square wave.
3. Vcc = 3.0 V
4. Set the system clock to 10 MHz or 4 MHz with the PHISEL register.

Timing Requirements (Vcc = 3 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified) [Vcc = 3 V]

Table 24.23 External Clock Input (XIN, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	—	ns
$t_{WH(XIN)}$	XIN input high width	24	—	ns
$t_{WL(XIN)}$	XIN input low width	24	—	ns
$t_{c(XCIN)}$	XCIN input cycle time	20	—	µs
$t_{WH(XCIN)}$	XCIN input high width	10	—	µs
$t_{WL(XCIN)}$	XCIN input low width	10	—	µs

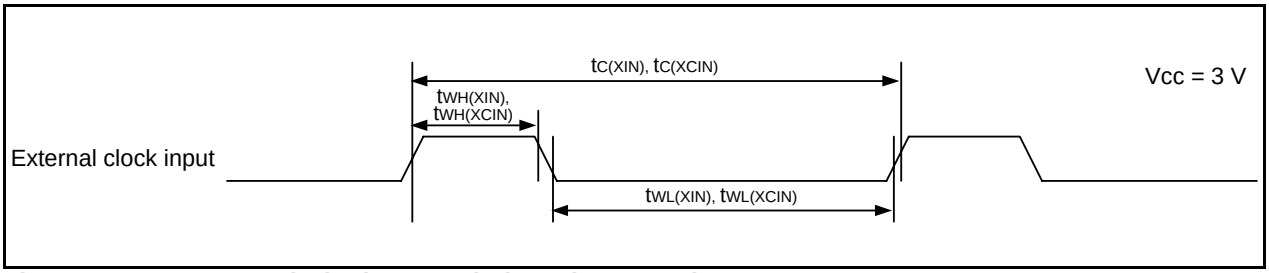


Figure 24.12 External Clock Input Timing Diagram When Vcc = 3 V

Table 24.24 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	300	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	120	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	120	—	ns

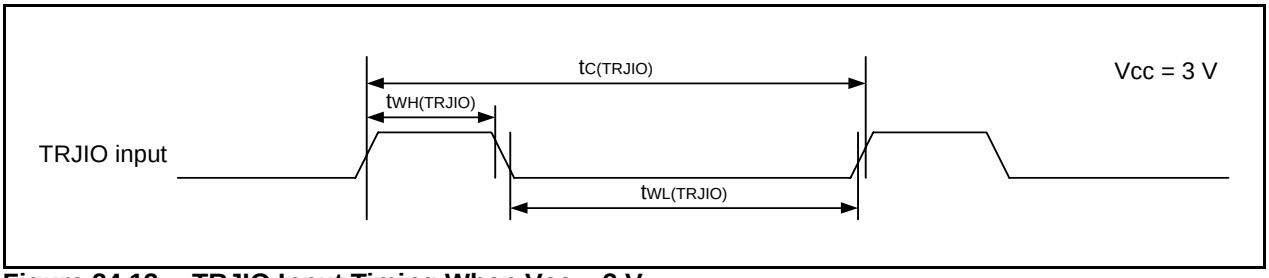


Figure 24.13 TRJIO Input Timing When Vcc = 3 V

Table 24.25 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{W(CKH)}$	CLKi input high width	150	—	ns
$t_{W(CKL)}$	CLKi input low width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 1

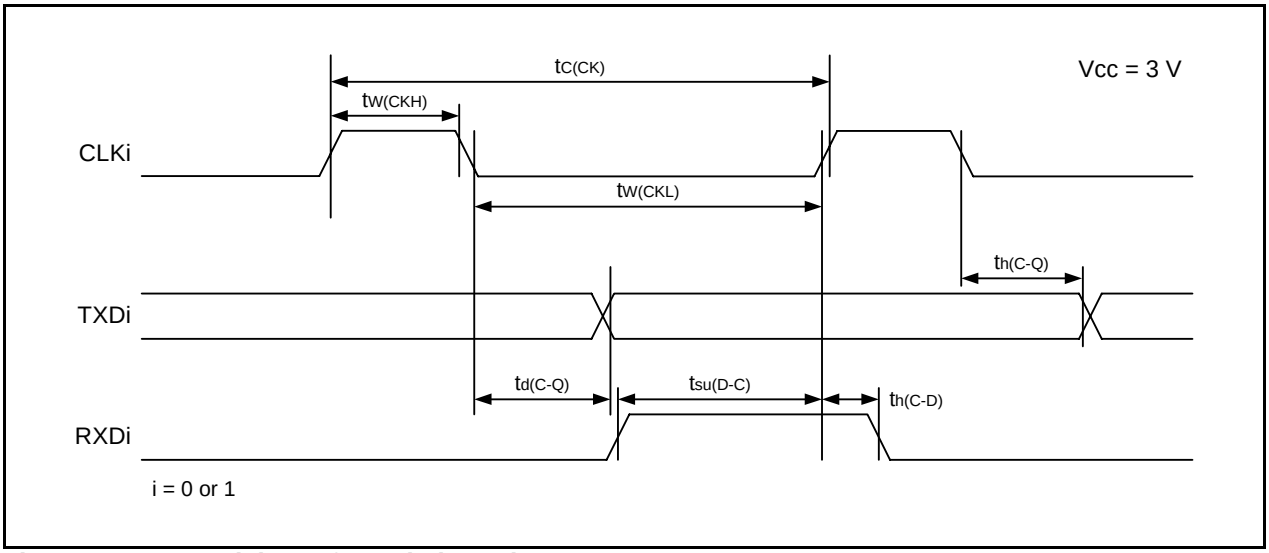


Figure 24.14 Serial Interface Timing When Vcc = 3 V

Table 24.26 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	380 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

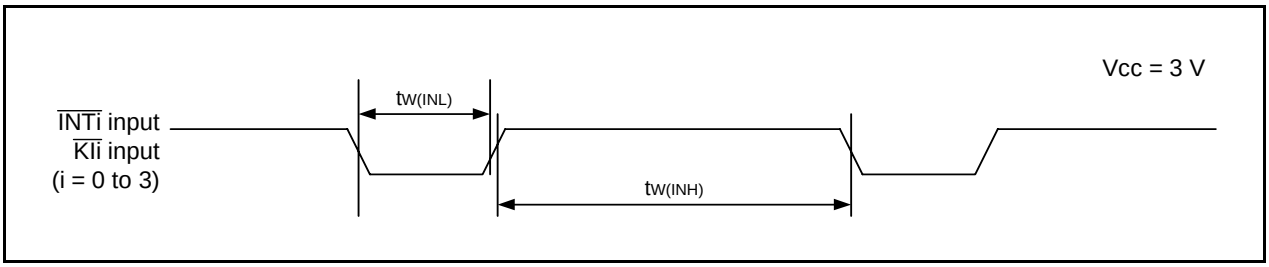


Figure 24.15 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 3 V

Table 24.27 DC Characteristics (5) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OH} = -2 mA	Vcc - 0.5	—	Vcc	V
			When drive capacity is low	I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
		P0_0, P0_1, P0_2, P0_3, P0_4, P0_5, P0_6, P0_7, P1_0, P1_1, P1_6, P1_7, P2_0, P2_1, P2_2, P3_1, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OH} = -1 mA	Vcc - 0.5	—	Vcc	V
V_{OL}	Output low voltage	P1_2, P1_3, P1_4, P1_5, P3_3, P3_4, P3_5, P3_7 (2)	When drive capacity is high	I_{OL} = 2 mA	—	—	0.5	V
			When drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		P0_0, P0_1, P0_2, P0_3, P0_4, P0_5, P0_6, P0_7, P1_0, P1_1, P1_6, P1_7, P2_0, P2_1, P2_2, P3_1, P4_2, P4_5, P4_6, P4_7, PA_0		I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, KI0, KI1, KI2, KI3, TRJIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, RXD0, CLK0	Vcc = 2.2 V		0.05	0.20	—	V
		$\overline{RESET}$	Vcc = 2.2 V		0.05	0.20	—	V
I_{IH}	Input high current		V_I = 2.2 V, Vcc = 2.2 V		—	—	4.0	µA
I_{IL}	Input low current		V_I = 0 V, Vcc = 2.2 V		—	—	-4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, Vcc = 2.2 V		70	140	300	kΩ
R_{fXIN}	Feedback resistance	XIN			—	2.2	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	14	—	MΩ
V_{RAM}	RAM hold voltage		In stop mode		1.8	—	—	V

Notes:
1. 1.8 V ≤ Vcc < 2.7 V and Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), f(XIN) = 5 MHz, unless otherwise specified.
2. High drive capacity can also be used while the peripheral output function is used.

Table 24.28 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V] (Topr = -20 °C to 85 °C (N version)/-40 °C to 85 °C (D version), unless otherwise specified)

Symbol	Parameter	Condition								Standard			Unit
			Oscillation Circuit		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other				
			XIN (2)	XCIN	High-Speed	Low-Speed				Min.	Typ. (3)	Max.	
Icc	Power supply current (1)	High-speed clock mode	5 MHz	Off	Off	125 kHz	No division	—		—	1.1	—	mA
			5 MHz	Off	Off	125 kHz	Division by 8	—		—	0.8	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz (4)	125 kHz	No division			—	1.8	6.5	mA
			Off	Off	5 MHz (4)	125 kHz	Division by 8			—	1.6	—	mA
			Off	Off	4 MHz (4)	125 kHz	Division by 16	MSTTRC = 1		—	1.3	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Division by 8	FMR27 = 1 LPE = 0		—	60	200	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	—	FMR27 = 1 LPE = 0		—	55	200	µA
			Off	32 kHz	Off	Off	—	FMSTP = 1 LPE = 0	Flash memory stopped during program operation in RAM	—	30	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1	Peripheral clock supplied during WAIT instruction execution	—	15	90	µA
			Off	Off	Off	125 kHz	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	4.5	80	µA
			Off	32 kHz	Off	Off	—	VC1E = 0 VC0E = 0 LPE = 1 WCKSTP = 1	Peripheral clock stopped during WAIT instruction execution	—	3	—	µA
		Stop mode	Off	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 25 °C Peripheral clock stopped	—	1	4.0	µA
			Off	Off	Off	Off	—	VC1E = 0 VC0E = 0 STPM = 1	Topr = 85 °C Peripheral clock stopped	—	1.6	—	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single-chip mode, output pins are open, and other pins are connected to Vss.
2. When the XIN input is a square wave.
3. Vcc = 2.2 V
4. Set the system clock to 5 MHz or 4 MHz with the PHISEL register.

Timing Requirements (Vcc = 2.2 V, Vss = 0 V at Topr = 25 °C, unless otherwise specified) [Vcc = 2.2 V]

Table 24.29 External Clock Input (XIN, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	200	—	ns
$t_{WH(XIN)}$	XIN input high width	90	—	ns
$t_{WL(XIN)}$	XIN input low width	90	—	ns
$t_{c(XCIN)}$	XCIN input cycle time	20	—	µs
$t_{WH(XCIN)}$	XCIN input high width	10	—	µs
$t_{WL(XCIN)}$	XCIN input low width	10	—	µs

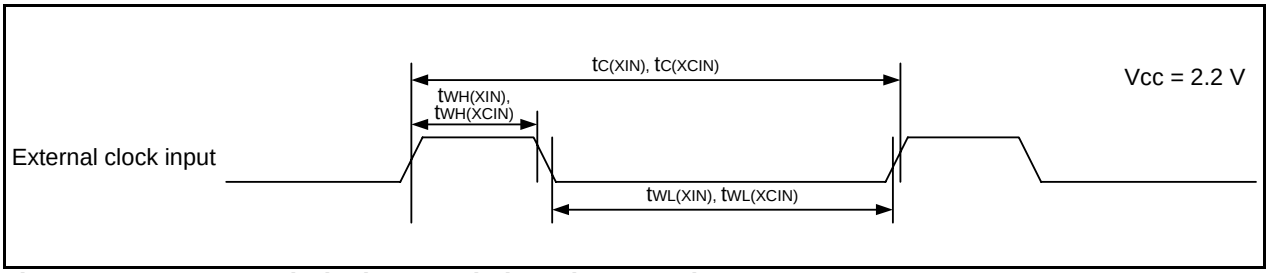


Figure 24.16 External Clock Input Timing Diagram When Vcc = 2.2 V

Table 24.30 TRJIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRJIO)}$	TRJIO input cycle time	500	—	ns
$t_{WH(TRJIO)}$	TRJIO input high width	200	—	ns
$t_{WL(TRJIO)}$	TRJIO input low width	200	—	ns

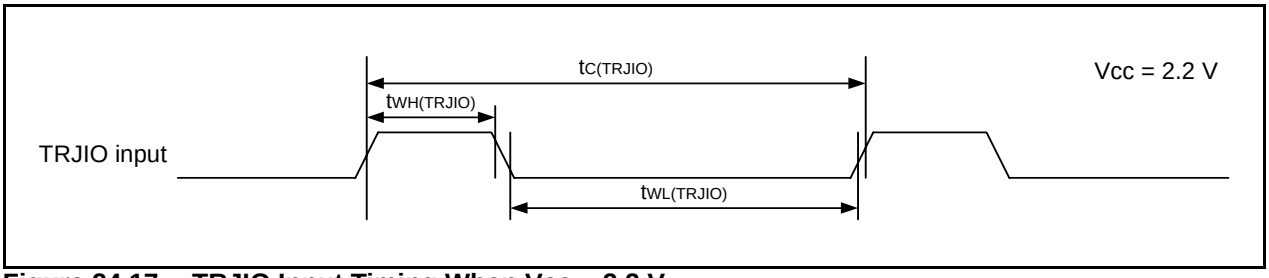


Figure 24.17 TRJIO Input Timing When Vcc = 2.2 V

Table 24.31 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	ns
$t_{W(CKH)}$	CLKi input high width	400	—	ns
$t_{W(CKL)}$	CLKi input low width	400	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

i = 0 or 1

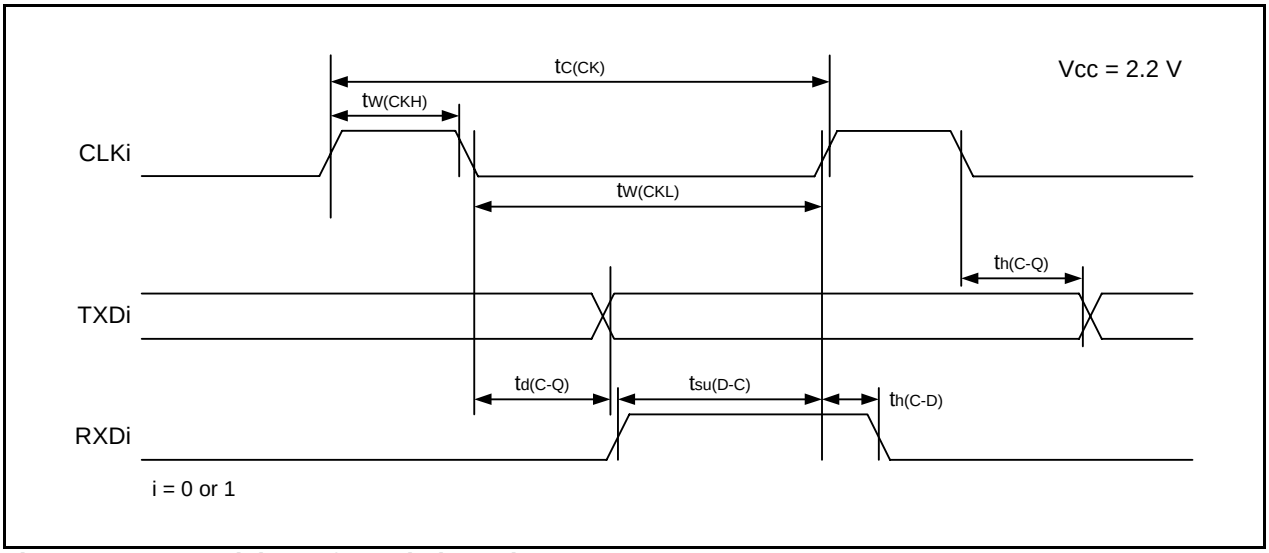


Figure 24.18 Serial Interface Timing When Vcc = 2.2 V

Table 24.32 External Interrupt $\overline{INTi}$ Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIi}$ input high width	1,000 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIi}$ input low width	1,000 (2)	—	ns

Notes:
1. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input high width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.
2. When the digital filter is enabled by the $\overline{INTi}$ input filter select bit, the $\overline{INTi}$ input low width is (1/digital filter clock frequency × 3) or the minimum value of the standard, whichever is greater.

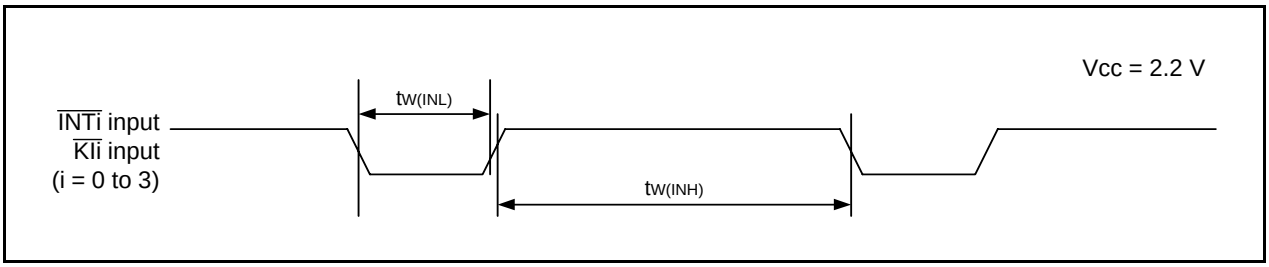


Figure 24.19 Timing for External Interrupt $\overline{INTi}$ Input and Key Input Interrupt $\overline{KIi}$ When Vcc = 2.2 V

25. Usage Notes

25.1 Notes on System Control

25.1.1 Option Function Select Area Setting Example

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

• To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

Programming formats vary depending on the compiler. Check the compiler manual.

• To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)          ; RESET
```

Programming formats vary depending on the compiler. Check the compiler manual.

25.2 Notes on Watchdog Timer

- Do not switch the count sources during watchdog timer operation.
- There is a delay of two cycles of the count source from a write to the WDTR register until the initialization of the watchdog timer.
- Allow at least three cycles of the count source between the previous and the next initialization of the watchdog timer.

25.3 Notes on Clock Generation Circuit

25.3.1 Oscillation Stop Detection Function

The oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz, so set bits CKSWIE to XINBAKE in the BAKCR register to 00b (interrupt request disabled, oscillation stop detection function disabled).

25.3.2 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

25.4 Notes on Power Control

25.4.1 Program Restrictions When Entering Wait Mode

To enter wait mode by setting the WAITM bit to 1, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the WAITM bit to 1.
To enter wait mode with the WAIT instruction, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before executing the WAIT instruction. The 4 bytes of instruction data following the instruction that sets the WAITM bit to 1 (wait mode is entered) or the WAIT instruction are prefetched from the instruction queue and then the program stops. Insert at least four NOP instructions after the instruction that sets the WAITM bit to 1 (wait mode is entered) or after the WAIT instruction.

• Program example to execute the WAIT instruction

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        FSET    I               ; Interrupt enabled
        WAIT                    ; Wait mode
        NOP
        NOP
        NOP
        NOP
```

• Program example to set the WAITM bit to 1

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        BSET    0, PRCR         ; Writing to SCKCR register enabled
        FCLR    I               ; Interrupt disabled
        BSET    5, SCKCR        ; Wait mode
        NOP
        NOP
        NOP
        NOP
        BCLR    0, PRCR         ; Writing to the SCKCR register disabled
        FSET    I               ; Interrupt enabled
```

25.4.2 Program Restrictions When Entering Stop Mode

When entering stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) before setting the STPM bit in the CKSTPR register to 1 (all clocks are stopped (stop mode)). The four bytes of instruction data following the instruction that sets the STPM bit to 1 are prefetched from the instruction queue and then the program stops.
Insert at least four NOP instructions following the JMP.B instruction immediately after the instruction that sets the STPM bit to 1.

• Program example to enter stop mode

```
        BCLR    1, FMR0         ; CPU rewrite mode disabled
        BCLR    7, FMR2         ; Low-current-consumption read mode disabled
        BSET    0, PRCR         ; Writing to CKSTPR register enabled
        FSET    I               ; Interrupt enabled
        BSET    0, CKSTPR       ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

25.5 Notes on Interrupts

25.5.1 Reading Address 00000h

Do not read address 00000h by a program. When an external interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from address 00000h in the interrupt sequence. At this time, the corresponding bit in the IRR3 register for the acknowledged interrupt is set to 0.
If a program is used to read address 00000h, the corresponding bit in the IRR3 register for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

25.5.2 SP Setting

Set a value in the SP before any interrupt is acknowledged. The SP is 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

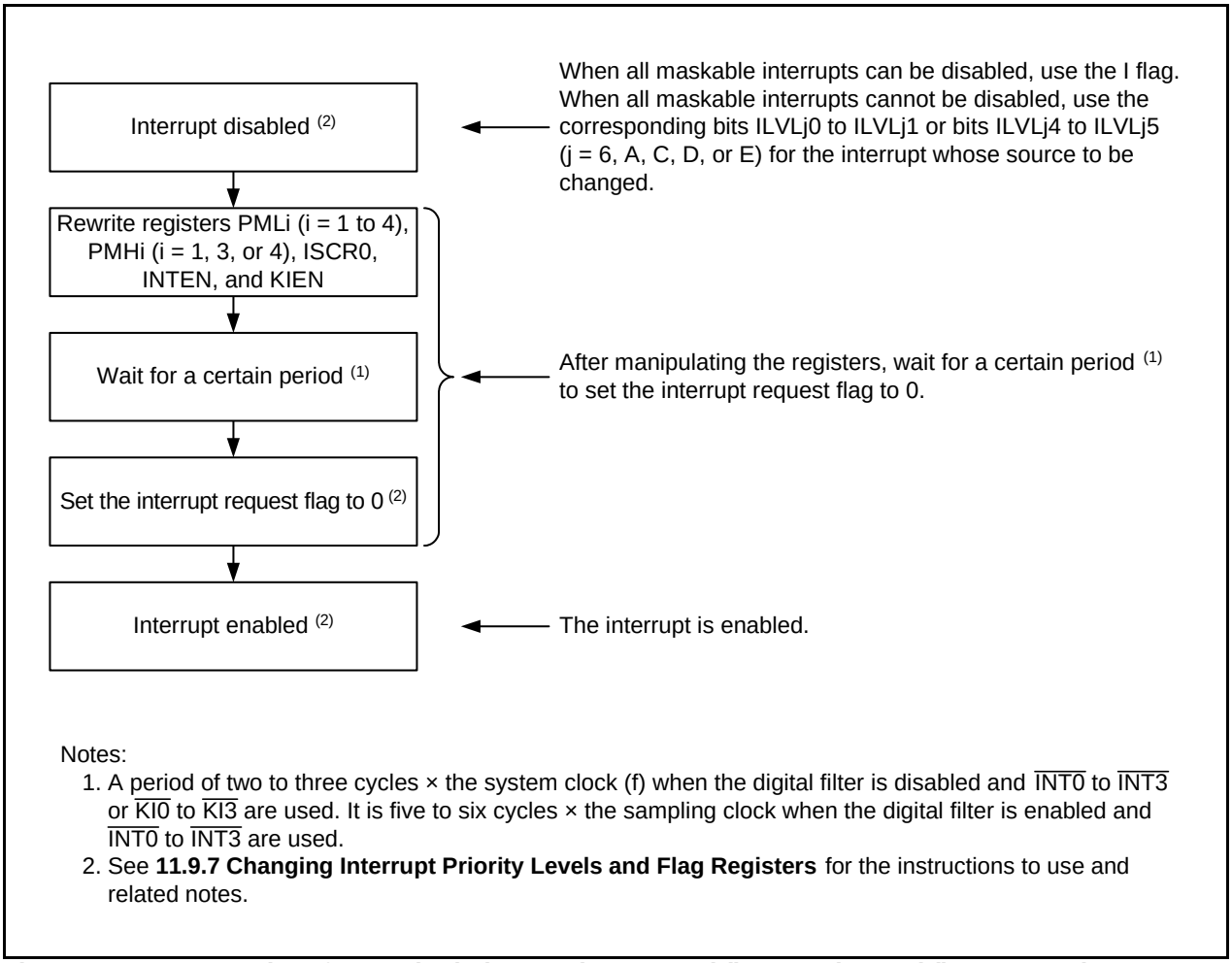
25.5.3 External Interrupt and Key Input Interrupt

Signal input to pins $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ must meet either the low-level width or the high-level width requirements shown in External Interrupt $\overline{\text{INTi}}$ Input (i = 0 to 3) in the Electrical Characteristics, regardless of the CPU operating clock. For details, see **Table 24.20** (Vcc = 5 V), **Table 24.26** (Vcc = 3 V), and **Table 24.32** (Vcc = 2.2 V) **External Interrupt $\overline{\text{INTi}}$ Input, Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 3)**.

25.5.4 Rewriting Registers PMLi (i = 1 to 4), PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN

When changing the functions of the $\overline{INT0}$ to $\overline{INT3}$ and $\overline{KI0}$ to $\overline{KI3}$ interrupts, an interrupt request flag may be set to 1 by rewriting registers PMLi (i = 1 to 4), PMHi (i = 1, 3, or 4), ISCR0, and KIEN. When an interrupt function is switched, rewrite these registers with interrupt requests disabled, and wait for a certain period (1) before setting the interrupt request flag to 0.
Figure 25.1 shows the Procedure for Manipulating Registers PMLi (i = 1 to 4), PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN, and Setting Interrupt Request Flag to 0.

Note:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{INT0}$ to $\overline{INT3}$ or $\overline{KI0}$ to $\overline{KI3}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{INT0}$ to $\overline{INT3}$ are used.



Notes:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{INT0}$ to $\overline{INT3}$ or $\overline{KI0}$ to $\overline{KI3}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{INT0}$ to $\overline{INT3}$ are used.
2. See **11.9.7 Changing Interrupt Priority Levels and Flag Registers** for the instructions to use and related notes.

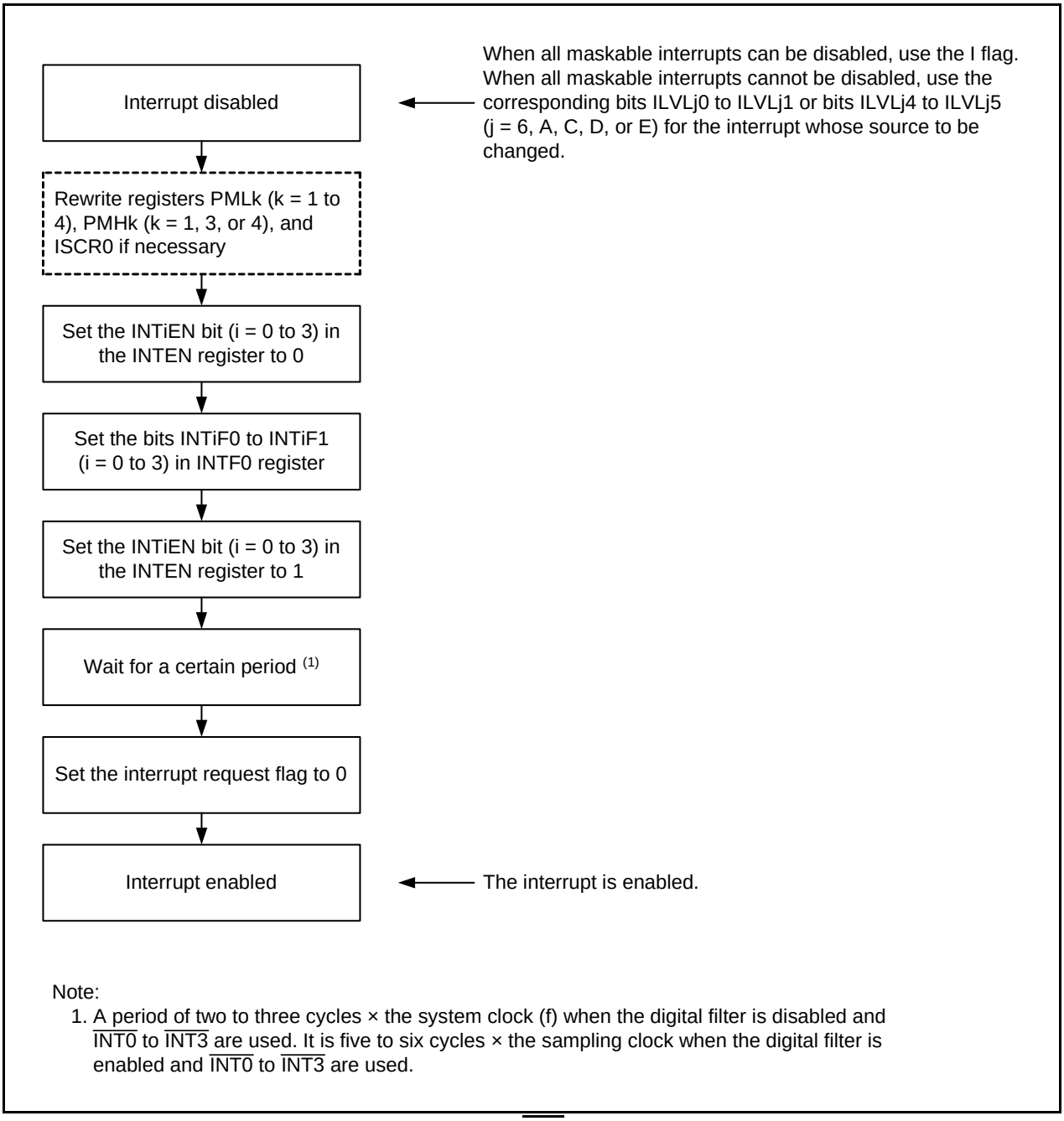
Figure 25.1 Procedure for Manipulating Registers PMLi (i = 1 to 4), PMHi (i = 1, 3, or 4), ISCR0, INTEN, and KIEN, and Setting Interrupt Request Flag to 0

25.5.5 $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) When Returning from Wait Mode or Stop Mode to Standard Operating Mode

When a transition is made to wait mode or stop mode with the WCKSTP bit in the CKSTPR register set to 1 (system clock stopped in wait mode) while in use of the $\overline{\text{INTi}}$ filter, the $\overline{\text{INTi}}$ interrupt cannot be used to return to standard mode.

When the $\overline{\text{INTi}}$ interrupt is used to return, set the WCKSTP bit to 1 and bits INTiF1 to INTiF0 in the INTF0 register to 00b (no filter) before a transition is made to wait mode or stop mode. When the filter is used again, select the sampling clock with bits INTiF0 to INTiF1 to enable the INTiEN bit in the INTEN register.

Figure 25.2 shows the Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) is Used.

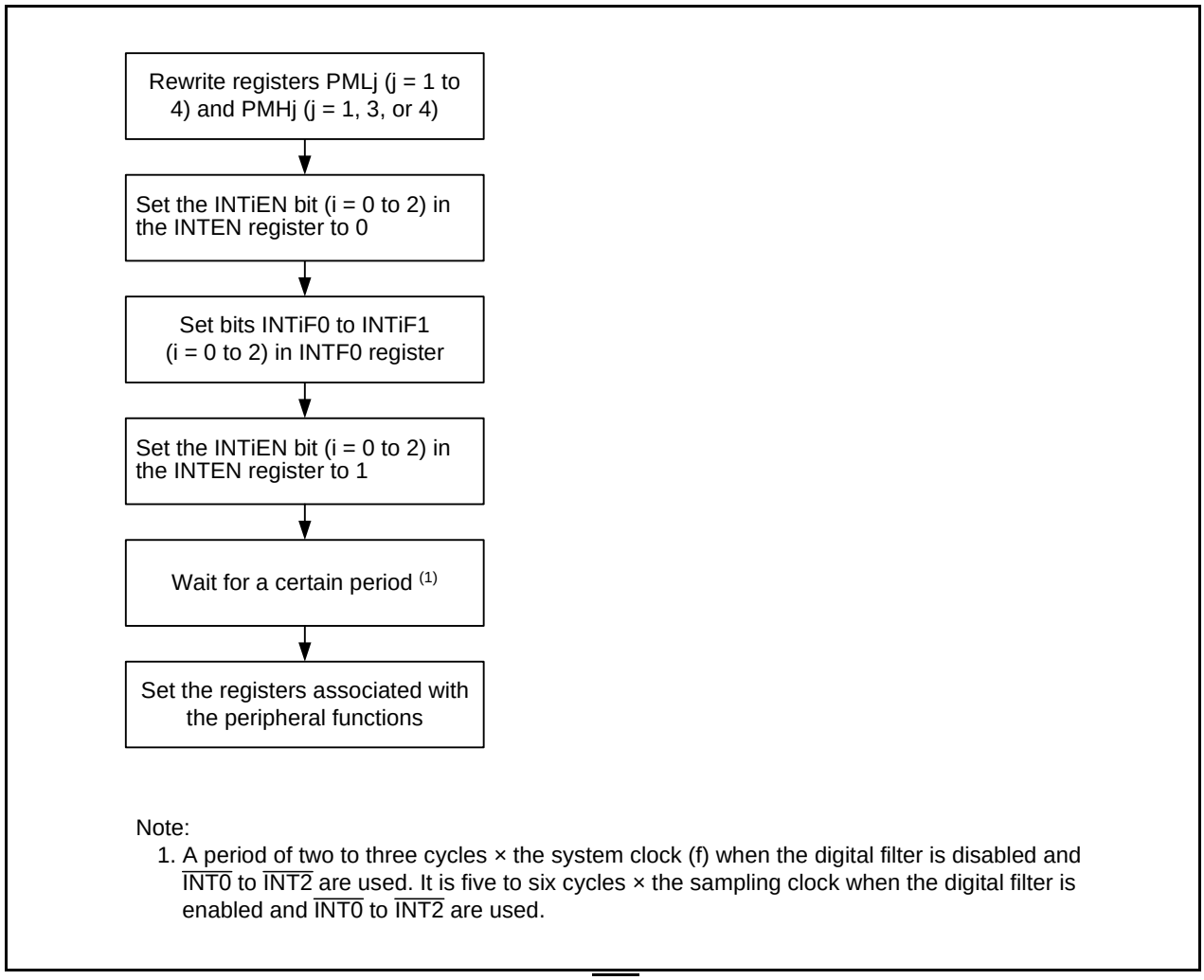


Note:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ are used.

Figure 25.2 Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 3) is Used

25.5.6 Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions

Figure 25.3 shows the Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions (Timer RJ2, Timer RB2, and Timer RC).



Note:
1. A period of two to three cycles × the system clock (f) when the digital filter is disabled and $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ are used. It is five to six cycles × the sampling clock when the digital filter is enabled and $\overline{\text{INT0}}$ to $\overline{\text{INT2}}$ are used.

Figure 25.3 Register Setting Procedure When $\overline{\text{INTi}}$ Input Filter (i = 0 to 2) is Used for Peripheral Functions (Timer RJ2, Timer RB2, and Timer RC)

25.5.7 Changing Interrupt Priority Levels and Flag Registers

(a) The interrupt priority level and the flag register must be changed only while no interrupt requests are generated. If an interrupt may be generated, using the I flag to disable the interrupt before changing the interrupt priority level and the flag register.

(b) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below.

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupts enabled) before the interrupt priority level and the flag register are changed due to effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause the program until the interrupt priority level register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #CFH, ILVLE     ; Set INT0 interrupt priority level 0
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #CFH, ILVLE     ; Set INT0 interrupt priority level 0
    MOV.W   MEM, R0         ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #CFH, ILVLE     ; Set INT0 interrupt priority level 0
    POPC     FLG            ; Enable interrupts
```

25.6 Notes on I/O Ports

25.6.1 Notes on $\overline{\text{RESET}}$/PA_0 Pin

The $\overline{\text{RESET}}$/PA_0 pin is multiplexed with the hardware reset function ($\overline{\text{RESET}}$), and this pin functions as the $\overline{\text{RESET}}$ pin when a reset is cleared. After the reset is cleared, the $\overline{\text{RESET}}$/PA_0 pin functions as the I/O port (PA_0) when the HWRSTE bit in the PAMCR register is set to 0. In this case, an external pull-up resistor must be connected.
This pin can also be used as CMOS output when it is set as an output port, but be sure not to conflict with an external reset input signal.
Refer to the following program example to use this pin as N-channel open-drain output as necessary.

• Program example to set PA_0 as an N-channel open-drain output port

```
FCLR    I
BCLR    0, HRPR
BSET    0, HRPR          ; Writing to the PAMCR register enabled
FSET    I
BSET    0, PAMCR         ; Port PA_0 function selected, N-channel open-drain output
                           selected
BSET    0, PDA           ; Output mode setting
```

25.6.2 I/O Pins for Peripheral Functions

In this MCU, the pin assignment of the peripheral functions can be changed using the port function mapping register. However, multiple pins must not be assigned to the same peripheral function input at the same time. Otherwise, no signal can be input correctly.

25.7 Notes on Timer RJ2

(1) Timer RJ2 stops counting after a reset. Start the count only after setting the value in the timer.

(2) After 1 (count is started) is written to the TSTART bit in the TRJCR register while the count is stopped, the TCSTF bit in the TRJCR register remains 0 (count is stopped) for two to three cycles of the count source. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 1 (count is in progress). The count is started from the first active edge of the count source after the TCSTF bit is set to 1. After 0 (count is stopped) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for two to three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RJ2 (1) other than the TCSTF bit until this bit is set to 0.
Note:
1. Registers associated with timer RJ2: TRJ, TRJCR, TRJIOC, and TRJMR

(3) In event counter mode, set the TSTART bit in the TRJCR register to 1 (count is started) and then input an external pulse.

(4) In pulse width/pulse period measurement modes, bits TEDGF and TUNDF in the TRJCR register used are set to 0 by writing 0 by a program but remain unchanged even if 1 is written to these bits. If a read-modify-write instruction is used to set the TRJCR register, bits TEDGF and TUNDF may be erroneously set to 0 depending on the timing, even when the TEDGF bit is set to 1 (active edge received) and the TUNDF bit is set to 1 (underflow) during execution of the instruction.
In this case, write 1 using the MOV instruction to the TEDGF or TUNDF bit which is not supposed to be set to 0.

(5) Insert NOP instructions between writing to and reading from registers associated with the TRJ counter while the counter is stopped.

(6) When the TSTART bit in the TRJCR register is 1 (count is started) or the TCSTF bit is 1 (count is in progress), allow at least three cycles of the count source clock for each write interval when writing to the TRJ register successively.

(7) When the mode is changed to pulse width measurement mode or pulse period measurement mode from another mode, the values of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before starting the timer RJ2 count.

(8) The TEDGF bit may be set to 1 by the first count source signal after the count is started.

(9) When using pulse period measurement mode, allow at least two periods of the count source for timer RJ2 immediately after the count is started and set the TEDGF bit to 0 before use.

(10) If the count is forcibly stopped by writing 1 to the TSTOP bit in the TRJCR register during count operation, the TRJIF bit in the TRJIR register may be set to 1 (interrupt requested). Set the TRJIF bit to 0 (no interrupt requested) before restarting the count.

(11) In pulse width measurement mode or pulse period measurement mode, set associated registers and set the TSTART bit in the TRJCR register to 1 (count is started) before inputting an external event.

(12) Do not set the TRJ register to 0000h in pulse width measurement mode and pulse period measurement mode.

(13) Note the following when writing 0 to the TEDGF bit in the TRJCR register in pulse width measurement mode or pulse period measurement mode.
Set the TRJIF bit in the TRJIR register to 0 before setting the TEDGF bit to 0.
When reading the TEDGF bit immediately after setting it to 0, it is read as 0. However the internal signal of the TEDGF bit remains 1 for one to two cycles of the count source. If an active edge is input during this period, the internal signal of the TEDGF bit does not become 0 and the TEDGF bit is read as 1.
Since the TRJIF bit becomes 1 when the internal signal of the TEDGF bit changes from 0 to 1, the TRJIF bit does not become 1 and no interrupt is generated.
After setting the TEDGF bit to 0, confirm that 0 can be read after waiting for three or more count source cycles in order to accept the next interrupt request.

25.8 Notes on Timer RB2

- Timer RB2 stops counting after a reset. Start the count after setting the value in the timer and prescaler.
- In the 8-bit timer with 8-bit prescaler, even if the prescaler and timer are read in 16-bit units, they are actually read sequentially byte by byte in the MCU. This may cause the value in the timer to be updated during reading of these two registers.
  In the 16-bit timer, access the TRBPRE register first and then the TRBPR register. Read the TRBPRE register first to read the count value in the lower byte. The count value in the higher byte will be retained. Next, read the TRBPR register to read the retained value in the higher byte. The timer value is not updated during reading of these two registers.
- In programmable one-shot and programmable wait one-shot generation modes, when the TOSSP bit in the TRBOCR register is set to 1 and the one-shot is stopped, the timer reloads the reload register value and is stopped. The timer count value must be read before the timer is stopped.
- After 1 (count is started) is written to the TSTART bit in the TRBCR register while the count is stopped, the TCSTF bit in the TRBCR register remains 0 (count is stopped) for two to three cycles of the count source. Do not access the registers associated with timer RB2 (1) other than the TCSTF bit until this bit is set to 1 (count is in progress). The count is started on the first active edge of the counter source after the TCSTF bit is set to 1.
  After 0 (count is stopped) is written to the TSTART bit during count operation, the TCSTF bit remains 1 for two to three cycles of the count source. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with timer RB2 (1) other than the TCSTF bit until this bit is set to 0.
  Note:
  1. Registers associated with timer RB2:
     TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBPR, and TRBSC
- In timer mode, do not set both the TRBPRE and TRBPR registers to 00h at the same time.
- When the TSTART bit in the TRBCR register is 0 (count is stopped), change the values of registers TRBPRE, TRBPR, and TRBSC, then wait for at least two cycles of the system clock (f) before setting the TSTART bit in the TRBCR register to 1 (count is started).
- When the TSTART bit in the TRBCR register is 1 (count is started) or the TCSTF bit is 1 (count is in progress), do not change the values in registers TRBIOC and TRBMR, and the TRBIE bit in the TRBIR register.
- Make sure the TCSTF bit in the TRBCR register is 1 (count is in progress) before writing 1 (one-shot count is started) to the TOSST bit in the TRBOCR register. When the TCSTF bit is 0 (count is stopped), writing 1 (one-shot count is started) to the TOSST bit is invalid.
- When writing to registers TRBPRE, TRBPR, and TRBSC during count operation (the TSTART bit is 1 or the TCSTF bit is 1), note the following points:
  - When writing to the TRBPRE register successively, allow at least three cycles of the count source for each write interval.
  - When writing to the TRBPR register successively, allow at least three cycles of the count source for each write interval.
  - When writing to the TRBSC register successively, allow at least three cycles of the count source for each write interval.
- When the TRBPR register is rewritten in programmable waveform generation mode, do not write to the TRBPRE, TRBPR, or TRBSC register during the secondary output period as described below after rewriting.
  - 8-bit timer with 8-bit prescaler:
    Two cycles of the prescaler underflow before the secondary output period ends.
  - 16-bit timer:
    Two cycles of the count source clock before the secondary output period ends.
- When the underflow signal from timer RJ2 is used as the count source for timer RB2, set timer RJ2 to timer mode, pulse output mode, or event counter mode.
- When 1 is written to the TOSST bit or the TOSSP bit in the TRBOCR register, the TOSSTF bit is changed after two to three cycles of the count source. If 1 is written to the TOSSP bit from when 1 is written to the TOSST bit until the TOSSTF bit is set to 1, the TOSSTF bit may be set to 0 or 1 depending on the internal state. Likewise, if 1 is written to the TOSST bit from when 1 is written to the TOSSP bit until the TOSSTF bit is set to 0, the TOSSTF may be set to 0 or 1 depending on the internal state.

- In programmable waveform generation mode and programmable wait one-shot mode, write to the TRBSC register before writing to the TRBPR register. At the underflow during the secondary period after the TRBPR register is written, the value written to the TRBPR register is transferred to the counter. If registers TRBPR and TRBSC are written two or more times after the TRBPR register is written until the underflow during the secondary period, the last written value is transferred to the counter at the underflow.
- When 1 is written to the TSTOP bit in the TRBCR register during count operation, timer RB2 is immediately stopped.
- If the count is forcibly stopped by writing 1 to the TSTOP bit during count operation, the TRBIF bit in the TRBIR register may be set to 1 (interrupt requested). Set the TRBIF bit to 0 (no interrupt requested) before restarting the count.
- When the TSTART bit in the TRBCR register is 0 (count is stopped), wait for at least two cycles of the system clock (f) after writing the values of registers TRBPRE and TRBPR before reading them.

25.9 Notes on Timer RC

25.9.1 TRCCNT Register

The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (TRCCNT counter is cleared by input capture/compare match A).

- When writing a value to the TRCCNT register by a program while the CTS bit in the TRCMR register is set to 1 (count is started), ensure that the write timing does not coincide with when the TRCCNT register is set to 0000h.
- If the timing when the TRCCNT register is set to 0000h and is written coincide with each other, the value is not be written and the TRCCNT register is set to 0000h.

If the TRCCNT register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.W   #XXXXh, TRCCNT      ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.W   TRCCNT, DATA        ; Read
```

25.9.2 TRCCR1 Register

To set bits CKS2 to CKS0 in the TRCCR1 register to 110b (fHOCO), set fHOCO to the clock frequency higher than the system clock frequency.

25.9.3 TRCSR Register

If the TRCSR register is written and read, the value before this register is written may be read. In this case, execute the JMP.B instruction between the write and read instructions.

- Program Example

```
        MOV.B   #XXh, TRCSR         ; Write
        JMP.B   L1                  ; JMP.B instruction
L1:     MOV.B   TRCSR, DATA         ; Read
```

25.9.4 Count Source Switching

When switching the count sources, stop the count before switching. After switching the count sources, wait for at least two cycles of the system clock before writing to the registers (at addresses 000E8h to 000FCh) associated with timer RC.

- Switching procedure

(1) Set the CTS bit in the TRCMR register to 0 (count is stopped).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of the system clock.
(4) Write to the registers (at addresses 000E8h to 000FCh) associated with timer RC.

When changing the count source from fHOCO to another source and stopping fHOCO, wait for at least two cycles of the system clock after changing the clock setting before stopping fHOCO.

- Switching procedure

(1) Set the CTS bit in the TRCMR register to 0 (count is stopped).
(2) Change bits CKS0 to CKS2 in the TRCCR1 register.
(3) Wait for at least two cycles of the system clock.
(4) Set the HOCOE bit in the OCOCR register to 0 (high-speed on-chip oscillator off).

25.9.5 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 15.1 Timer RC Specifications**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 15.19 Digital Filter Circuit Block Diagram**)

- The value of the TRCCNT register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

25.9.6 TRCMR Register in PWM2 Mode

When the CSTP bit in the TRCCR2 register is 1 (increment is stopped), do not set the TRCMR register when a compare match occurs between registers TRCCNT and TRCGRA.

25.9.7 MSTCR Register

After stopping the timer RC count, set the MSTTRC bit in the MSTCR register to 1 (standby).

25.9.8 Mode Switching

- When switching the modes during operation, set the CTS bit in the TRCMR register to 0 (count is stopped) before switching.
- After switching the modes, set each flag in the TRCSR register to 0 before operation is started.

25.9.9 Procedure for Setting Registers Associated with Timer RC

Set the registers associated with timer RC following the procedure below:
(1) Set timer RC operating mode (bits PWMB, PWMC, PWMD, and PWM2 in the TRCMR register).
(2) Set the registers other than that set in (1).
(3) Set the port output to be enabled (bits EA to ED in the TRCOER register).

25.10 Notes on Timer RK

- After writing 0 (count is stopped) to the TSTART bit in the TMKCR register during count operation, do not access the registers associated with timer RK (1) for two to three cycles of the count source.
  Note:
  1. Registers associated with timer RK: TMKM, TMKCR, TMKLD, and TMKIR
- When writing to and reading from the TMKLD register continuously while the count is stopped, insert one NOP instruction between the instructions used for writing and reading.

25.11 Notes on Timer RE2

- When 0 (count is stopped) is written to the RUN bit in the TRECR register, the count is stopped after three cycles of the count source.
- When switching to module standby, set the RUN bit to 0 (count is stopped) and allow three or more cycles of the count source to elapse before setting the MSTTRE bit in the MSTCR register to 1 (standby).
- Switching registers TREIFR and TREIER must be performed as follows:
  [Real-time clock mode]
  - Switch the TREIER register while the RTCF bit in the TREIFR register is 0 (no interrupt requested).
  - Switch the ALIE bit in the TREIFR register while the ALIF bit in the TREIFR register is 0 (no interrupt requested).

  [Compare match timer mode]
  - Switch the CMIE bit in the TREIER register while the CMIF bit in the TREIFR register is 0 (interrupt requested).
  - Switch the OVIE bit in the TREIER register while the OVIF bit in the TREIFR register is 0 (no interrupt requested).
- When changing the CS3 bit in the TRECSR register, all of the following conditions must be met:
  - The RUN bit is 0 (count is stopped).
  - When changing the CS3 bit from 0 to 1, the CMIF bit is 0 (no interrupt requested) and the OVIF bit is 0 (no interrupt requested).
  - When changing the CS3 bit from 1 to 0, the ALIF bit is 0 (no interrupt requested) and the RTCF bit is 0 (no interrupt requested).

25.12 Notes on Serial Interface (UARTi (i = 0 or 1))

Regardless of clock synchronous I/O mode or clock asynchronous I/O mode, read the UiRB register (i = 0 or 1) in 16-bit units.
When the UiRBH register is read, bits FER and PER in the UiRB register are set to 0 (no framing error, no parity error). Also, the RI bit in the UiC1 register is set to 0 (the UiRB register empty).
To check receive errors, use the data read from the UiRB register.

• Program example to read the receive buffer register

```
MOV.W    0086H, R0        ; Read the U0RB register
```

When the transfer data is 9 bits long in clock asynchronous I/O mode, write to the UiTB register in the order UiTBH first and then UiTBL in 8-bit units.

• Program example to write to the transmit buffer register

```
MOV.B    #XXH, 0083H      ; Write to the U0TBH register
MOV.B    #XXH, 0082H      ; Write to the U0TBL register
```

Do not set the MSTUART0 bit in the MSTCR register or the MSTUART1 bit in the MSTCR1 register to 1 (standby) during communication. When setting the module to the standby state, confirm whether communication has completed. After communication has completed, set bits TE and RE in the UiC1 register to 0 (communication disabled) before setting the module to the standby state. After the module standby state is cleared, the initial settings for communication must be set again.

25.13 Notes on Clock Synchronous Serial Interface

25.13.1 Notes on Synchronous Serial Communication Unit

To use the synchronous serial communication unit, set the IICSEL bit in the IICCR register to 0 (SSU function).

25.13.2 Notes on I²C bus Interface

To use the I²C bus interface, set the IICSEL bit in the IICCR register to 1 (I²C bus function).

Notes regarding the I²C specification

Do not use the I²C interface with the settings that do not meet the I²C specification.

(1) In the I²C specification, the transfer rate is a maximum of 400 kHz and the low-level period of the SCL signal is a minimum of 1.3 µs in high-speed mode. Since the duty cycle for the I²C bus interface in this MCU is 50%, this minimum of 1.3 µs for the low-level period of the SCL signal cannot be met during operation at 400 kHz. To meet this minimum of 1.3 µs for the low-level period of the SCL signal, set the transfer rate to 384.6 kHz or below to use the I²C bus interface.

(2) There must be a delay of a minimum of 300 ns for the SDA pin to change at the rising edge of the SCL signal. For the I²C bus interface in this MCU, the delay value can be set by bits SDADLY0 to SDADLY1 in the IICCR register. The delay value must be determined for the system. When f1 is set to 11 MHz or above, set bits SDADLY1 to SDADLY0 in the IICCR register to 01b (digital delay of 11 × f1 cycles) or 10b (digital delay of 19 × f1 cycles).

(3) There is no compatibility with the CBUS.

(4) 10-bit addressing cannot be used.

(5) When a start condition is detected while data is transmitted in slave transmission, any address following that condition cannot be received and the operation is stopped. Follow the procedure for resetting the control block to reset the I²C bus interface.

(6) Do not set to 1111XXXb and 0000XXXb as slave addresses.

(7) When starting communication by the master after a stop condition is detected, set the STOP bit in the SISR register to 0.

25.13.3 ICE Bit in SICR1 Register and SIRST Bit in SICR2 Register

When writing 0 to the ICE bit or 1 to the SIRST bit during an I2C bus interface operation, the BBSY bit in the SICR2 register and the STOP bit in the SISR register may become undefined.

25.13.3.1 Conditions When Bits Become Undefined

- When this module occupies the I2C bus in master transmit mode (bits MST and TRS in the SICR1 register are 1).
- When this module occupies the I2C bus in master receive mode (the MST bit is 1 and the TRS bit is 0).
- When this module transmits data in slave transmit mode (the MST bit is 0 and the TRS bit is 1).
- When this module transmits an acknowledge in slave receive mode (bits MST and TRS are 0).

25.13.3.2 Countermeasures

- When the start condition (the SDA falling edge when SCL is high) is input, the BBSY bit becomes 1.
- When the stop condition (the SDA rising edge when SCL is high) is input, the BBSY bit becomes 0.
- When writing 1 to the BBSY bit, 0 to the SCP bit, and the start condition (the SDA falling edge when SCL is high) is output while SCL and SDA are high in master transmit mode, the BBSY bit becomes 1.
- When writing 0 to bits BBSY and SCP, the stop condition (the SDA rising edge when SCL is high) is output while SDA is low, and this is the only module that holds SCL low in master transmit mode or master receive mode, the BBSY bit becomes 0.
- When writing 1 to the FS bit in the SAR register, the BBSY bit becomes 0.

25.13.3.3 Additional Descriptions Regarding SIRST Bit

- When writing 1 to the SIRST bit, bits SDAO and SCLO in the SICR2 register become 1.
- When writing 1 to the SIRST bit in master transmit mode and slave transmit mode, the TDRE bit in the SISR register becomes 1.
- While the control block of the I2C bus interface is reset by setting the SIRST bit to 1, writing to bits BBSY, SCP, and SDAO is disabled. Write 0 to the SIRST bit before writing to the BBSY bit, SCP bit, or SDAO bit.
- Even when writing 1 to the SIRST bit, the BBSY bit does not become 0. However, the stop condition (the SDA rising edge when SCL is high) may be generated depending on the states of SCL and SDA and the BBSY bit may become 0.
  There may also be a similar effect on other bits.
- While the control block of the I2C bus interface is reset by setting the SIRST bit to 1, data transmission/reception is stopped. However, the function to detect the start condition, stop condition, or arbitration lost operates. The values in the SICR1 register, SICR2 register, or SISR register may be updated depending on the signals applied to pins SCL and SDA.

25.14 Notes on A/D Converter

25.14.1 A/D Converter Standby Setting

The A/D converter can be set to standby or active using the MSTAD bit in the MSTCR register.
Stop A/D conversion before setting to module standby. Register access is enabled by clearing the A/D converter standby state. For details, see **5. System Control**.

25.14.2 Sensor Output Impedance during A/D Conversion

To perform A/D conversion accurately, charging of the internal capacitor C shown in Figure 25.4 must be completed within the period of time specified as T (sampling time). Let the output impedance of the sensor equivalent circuit be R0, the internal resistance of the microcomputer be R, the accuracy (error) of the A/D converter be X, and the resolution of A/D converter be Y (Y is 1024 in 10-bit mode).

$$\text{VC is generally } VC = VIN\left\{1 - e^{-\frac{1}{C(R0+R)}t}\right\}$$

$$\text{And when } t = T,\ VC = VIN - \frac{X}{Y}VIN = VIN\left(1 - \frac{X}{Y}\right)$$

$$e^{-\frac{1}{C(R0+R)}T} = \frac{X}{Y}$$

$$-\frac{1}{C(R0+R)}T = \ln\frac{X}{Y}$$

$$\text{Hence, } R0 = -\frac{T}{C \bullet \ln\frac{X}{Y}} - R$$

Figure 25.4 shows the Analog Input Pin and External Sensor Equivalent Circuit. The user can obtain an impedance R0 that makes the pin-to-pin voltage VC increase from 0 to VIN – (0.1/1024) VIN within time T when the difference between VIN and VC becomes 0.1 LSB. The value, (0.1/1024) indicates a precondition for the calculation of R0 when the degradation due to insufficient capacitor charge is suppressed to 0.1 LSB during A/D conversion in 10-bit mode. The actual error, however, is the absolute accuracy plus 0.1 LSB.
A/D conversion clock = 20 MHz, T = 0.8 μs. Output impedance R0 through which an capacitor C is fully charged within T is obtained as follows:

T = 0.8 μs, R = 10 kΩ, C = 6.0 pF, X = 0.1, and Y = 1024. Hence,

$$R0 = -\frac{0.8 \times 10^{-6}}{6.0 \times 10^{-12} \bullet \ln\frac{0.1}{1024}} - 10 \times 10^{3} \approx 4.4 \times 10^{3}$$

Thus the maximum output impedance of a sensor circuit for an accuracy (error) of 0.1 LSB or less is 4.4 kΩ maximum.

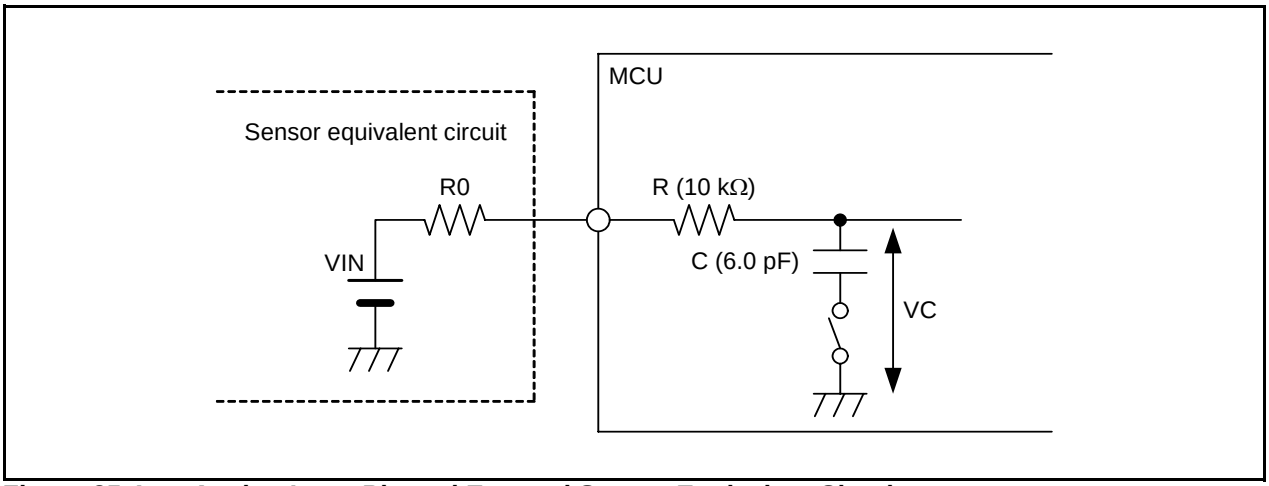


Figure 25.4 Analog Input Pin and External Sensor Equivalent Circuit

25.14.3 Register Setting

- Registers ADMOD and ADINSEL must be written only when A/D conversion is stopped.
- Do not enter stop mode during A/D conversion.
- Do not enter wait mode during A/D conversion while the WCKSTP bit in the CKSTPR register is 1 (system clock is stopped in wait mode).
- Do not set the FMSTP bit in the FMR0 register to 1 (flash memory is stopped) or the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled) during A/D conversion.
- During A/D conversion, if the ADST bit in the ADCON0 register is set to 0 (A/D conversion is stopped) by a program to forcibly terminate the conversion, the conversion result from the A/D converter will be undefined and no interrupt will be generated. The value of the ADi register (i = 0 or 1) which is not engaged in A/D conversion may also be undefined.
  If the ADST bit is set to 0 by a program, do not use any of the values of the ADi register.
- When using the A/D converter, it is recommended that the average of the conversion results be taken.

25.15 Notes on Flash Memory

25.15.1 ID Code Area Setting Example

The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

• To set 55h in all of the ID code area

```
  .org 00FFDCH
  .lword dummy | (55000000h)      ; UND
  .lword dummy | (55000000h)      ; INTO
  .lword dummy                    ; BREAK
  .lword dummy | (55000000h)      ; ADDRESS MATCH
  .lword dummy | (55000000h)      ; SET SINGLE STEP
  .lword dummy | (55000000h)      ; WDT
  .lword dummy | (55000000h)      ; RESERVE
  .lword dummy | (55000000h)      ; RESERVE
```

Programming formats vary depending on the compiler. Check the compiler manual.

25.15.2 CPU Rewrite Mode

25.15.2.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory:
UND, INTO, and BRK

25.15.2.2 Interrupts

Tables 25.1 and 25.2 list the Interrupt Handling during CPU Rewrite Operation.

Table 25.1 Interrupt Handling during CPU Rewrite Operation (EW0 Mode)

Interrupt Type	Data Flash/Program ROM	
	Suspend Enabled (FMR20 = 1)	Suspend Disabled (FMR20 = 0)
Maskable interrupt	When an interrupt request is acknowledged, interrupt handling is executed. (The interrupt vector is allocated in the RAM) The suspend state can be entered by either of the following: (1) When the FMR22 bit is 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request). The flash memory suspends auto-erase or auto-programming after td(SR-SUS). (2) When the FMR22 bit is 0 (suspend request disabled by interrupt request) and suspend is required, set the FMR21 bit to 1 (suspend request) in the interrupt handling. The flash memory suspends auto-erase or auto-programming after td(SR-SUS). While auto-erase is suspended, auto-programming and reading can be executed for any block other than the blocks being auto-erased. While auto-programming is suspended, any block other than the blocks being auto-programmed can be read. Auto-erase can be restarted by setting the FMR21 bit to 0 (restart).	Interrupt handling is executed with auto-erase or auto-programming executed (The interrupt vector is allocated in the RAM)
Address match	Do not use during auto-erasing or auto-programming.	
UND, INTO, and BRK instructions		
Single-step		
Watchdog timer	When an interrupt request is acknowledged, auto-erase or auto-programming is forcibly stopped immediately and the flash memory is reset. After the specified period, the flash memory is restarted before interrupt handling is started. Since auto-erase or auto-programming is forcibly stopped, the correct values may not be read from the block being auto-erased or the address being auto-programmed. After the flash memory is restarted, execute auto-erase again and verify it complete normally. The watchdog timer does not stop while the command is executing, so interrupt requests may be generated. Initialize the watchdog timer periodically using the erase-suspend function. Since the flash memory control registers are initialized in this case, these registers must be set again. (1)	
Oscillation stop detection		
Voltage monitor 1		

FMR20, FMR21, FMR22: Bits in FMR2 register
Note:
1. Registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated while the flash memory is busy.
When the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled) and the FMSTP bit is 1 (flash memory is stopped), registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated.

Table 25.2 Interrupt Handling during CPU Rewrite Operation (EW1 Mode)

Interrupt Type	Data Flash/Program ROM	
	Suspend Enabled (FMR20 = 1)	Suspend Disabled (FMR20 = 0)
Maskable interrupt	When an interrupt request is acknowledged, the FMR21 bit is automatically set to 1 (suspend request) if the FMR22 bit is 1 (suspend request enabled by interrupt request). The flash memory suspends auto-erase or auto-programming after td(SR-SUS) and interrupt handling is executed. When auto-erase is being suspended, auto-programming and reading can be executed for any block other than the blocks being auto-erased. When auto-programming is being suspended, any block other than the blocks being auto-programmed can be read. After interrupt handling completes, auto-erase or auto-programming can be restarted by setting the FMR21 bit is set to 0 (restart). If the FMR22 bit is set to 0 (suspend request disabled by interrupt request), auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.	Auto-erase or auto-programming has priority. Interrupt handling is executed after auto-erase or auto-programming.
Address match	Do not use during auto-erasing or auto-programming.	
UND, INTO, and BRK instructions		
Single-step		
Watchdog timer	When an interrupt request is acknowledged, auto-erase or auto-programming is forcibly stopped immediately and the flash memory is reset. After the specified period, the flash memory is restarted before interrupt handling is started. Since auto-erase or auto-programming is forcibly stopped, the correct values may not be read from the block being auto-erased or the address being auto-programmed. After the flash memory is restarted, execute auto-erase again and verify it complete normally. The watchdog timer does not stop while the command is executing, so interrupt requests may be generated. Initialize the watchdog timer periodically using the erase-suspend function. Since the flash memory control registers are initialized in this case, these registers must be set again. (1)	
Oscillation stop detection		
Voltage monitor 1		

FMR20, FMR21, FMR22: Bits in FMR2 register

Note:

1. Registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated while the flash memory is busy.
   When the FMR01 bit in the FMR0 register is 1 (CPU rewrite mode enabled) and the FMSTP bit is 1 (flash memory is stopped), registers FMR0, FMR1, and FMR2 are initialized if a watchdog timer, oscillation stop detection, or voltage monitor 1 interrupt is generated.

25.15.2.3 Access Methods

To set one of the following bits to 1, first write 0 and then 1 immediately. Interrupts must be disabled between writing 0 and then writing 1.
• The FMR01 or FMR02 bit in the FMR0 register
• The FMR13 bit in the FMR1 register
• The FMR20, FMR22, or FMR27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Interrupts must be disabled between writing 1 and then writing 0.
The FMR16 or FMR17 bit in the FMR1 register

25.15.2.4 Rewriting User ROM Area

When EW0 mode is used and the supply voltage falls while rewriting a block where a rewrite control program is stored, the rewrite control program is not be rewritten correctly. As a result, it may not be possible to rewrite the flash memory afterwards. Use standard serial I/O mode to rewrite this block.

25.15.2.5 Programming

Do not perform even a single additional write to an already programmed address.

25.15.2.6 Entering Wait Mode or Stop Mode

Do not enter wait mode or stop mode during suspend.
When the FST7 bit in the FST register is 0 (busy) while programming or erasing the flash memory, do not enter wait mode or stop mode.
Do not set the FMR27 bit to 1 while the FMSTP bit (flash memory stop bit) in the FMR0 register is 1 (flash memory is stopped).

25.15.2.7 Flash Memory Programming and Erase Voltages

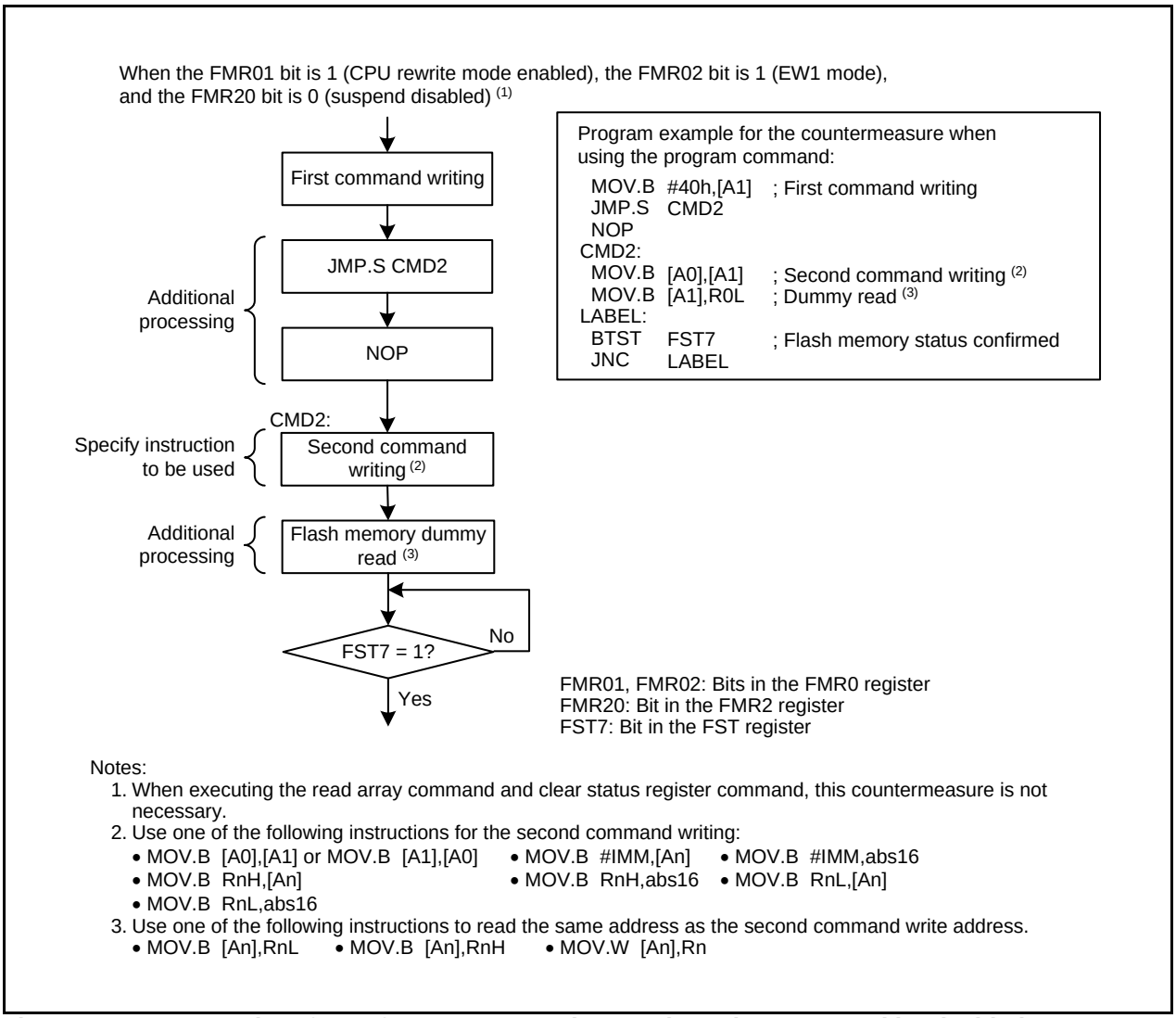
When performing a program/erase operation, use a VCC supply voltage in the range of 1.8 V to 5.5 V. Do not perform a program/erase operation at less than 1.8 V.

25.15.2.8 Block Blank Check

Do not execute a block blank check command during erase-suspend.

25.15.2.9 EW1 Mode

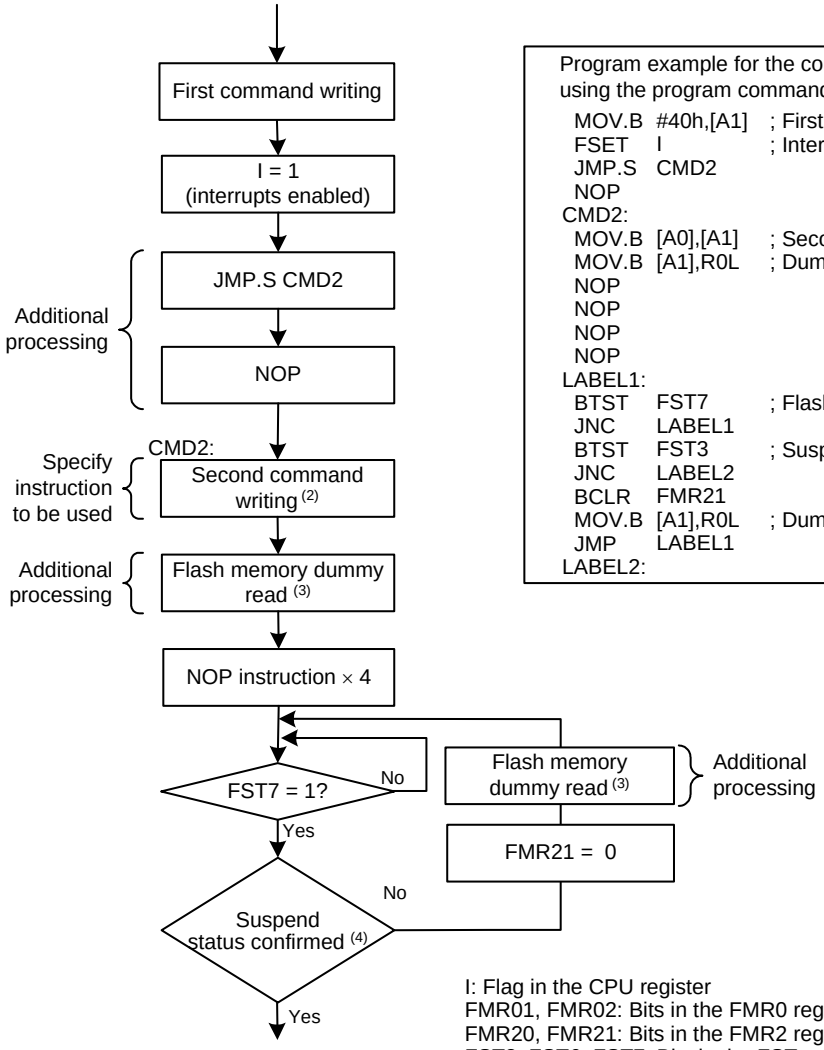
When setting the FMR01 bit in the FMR0 register to 1 (CPU rewrite mode enabled) and the FMR02 bit to 1 (EW1 mode) to execute CPU rewrite mode, follow the procedure below in EW1 mode. Figure 25.5 shows the Procedure for Software Command Execution When Suspend is Disabled. Figure 25.6 shows the Procedure for Software Command Execution When Suspend is Enabled.



Notes:
1. When executing the read array command and clear status register command, this countermeasure is not necessary.
2. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
3. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn

Figure 25.5 Procedure for Software Command Execution When Suspend is Disabled

When the FMR01 bit is 1 (CPU rewrite mode enabled), the FMR02 bit is 1 (EW1 mode), and the FMR20 bit is 1 (suspend enabled) (1)




```
Program example for the countermeasure when
using the program command:
  MOV.B  #40h,[A1]   ; First command writing
  FSET   I           ; Interrupts enabled
  JMP.S  CMD2
  NOP
CMD2:
  MOV.B  [A0],[A1]   ; Second command writing (2)
  MOV.B  [A1],R0L    ; Dummy read (3)
  NOP
  NOP
  NOP
  NOP
LABEL1:
  BTST   FST7        ; Flash memory status confirmed
  JNC    LABEL1
  BTST   FST3        ; Suspend status confirmed (4)
  JNC    LABEL2
  BCLR   FMR21
  MOV.B  [A1],R0L    ; Dummy read (3)
  JMP    LABEL1
LABEL2:
```

I: Flag in the CPU register
FMR01, FMR02: Bits in the FMR0 register
FMR20, FMR21: Bits in the FMR2 register
FST3, FST6, FST7: Bits in the FST register

Notes:
1. When executing the read array command and clear status register command, this countermeasure is not necessary.
2. Use one of the following instructions for the second command writing:
   - MOV.B [A0],[A1] or MOV.B [A1],[A0]
   - MOV.B #IMM,[An]
   - MOV.B #IMM,abs16
   - MOV.B RnH,[An]
   - MOV.B RnH,abs16
   - MOV.B RnL,[An]
   - MOV.B RnL,abs16
3. Use one of the following instructions to read the same address as the second command write address.
   - MOV.B [An],RnL
   - MOV.B [An],RnH
   - MOV.W [An],Rn
4. Confirm the suspend status using the FST3 bit for the program command, and the FST6 bit for the block erase command.

Figure 25.6 Procedure for Software Command Execution When Suspend is Enabled

25.15.3 Notes on Flash Memory Stop and Operation Transition

(1) Do not enter stop mode while the FMSTP bit is 1 (the flash memory is stopped).
(2) Do not enter wait mode while the FMSTP bit is 1 (the flash memory is stopped) and the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
(3) Do not enter flash memory stop state for 42 μs after entering from flash memory stop state to flash memory operation state. And do not rewrite the LOCODIS bit in the OCOCR register for 42 μs.

Conditions when entering flash memory operation state from flash memory stop state.
• Set the FMSTP bit to 0 (the flash memory operates).
• Return from wait mode while the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
• Return from stop mode.

Conditions when entering flash memory stop state from flash memory operation state.
• Set the FMSTP bit to 1 (the flash memory is stopped).
• Enter wait mode while the WTFMSTP bit is 1 (the flash memory is stopped in wait mode).
• Enter stop mode.

25.16 Notes on Noise

25.16.1 Inserting a Bypass Capacitor between Pins VCC and VSS as a Countermeasure against Noise and Latch-up

Connect a bypass capacitor (approximately 0.1 μF) across pins VCC and VSS using the shortest and thickest possible wiring.

25.16.2 Countermeasures against Noise Error in Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU's internal noise control circuitry. In such cases the contents of the port related registers may be changed.

As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may occur between the reset routine and interrupt routines.

25.17 Note on Power Supply Voltage Fluctuation

After a reset is cleared, the supply voltage applied to the VCC pin must meet either or both of the allowable ripple voltage Vr(vcc) and the ripple voltage falling gradient dVr(vcc)/dt shown in Figure 25.7.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
Vr(vcc)	Allowable ripple voltage			0.1 VCC	V
dVr(vcc)/dt	Ripple voltage falling gradient			10	V/ms

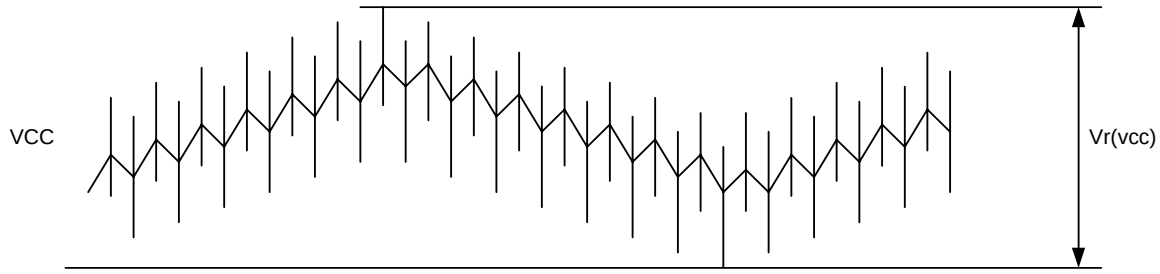


Figure 25.7 Ripple Voltage Definition

26. Notes on On-Chip Debugger

When using the on-chip debugger to develop and debug programs for the R8C/M13B Group, attention must be paid to the following restrictions:

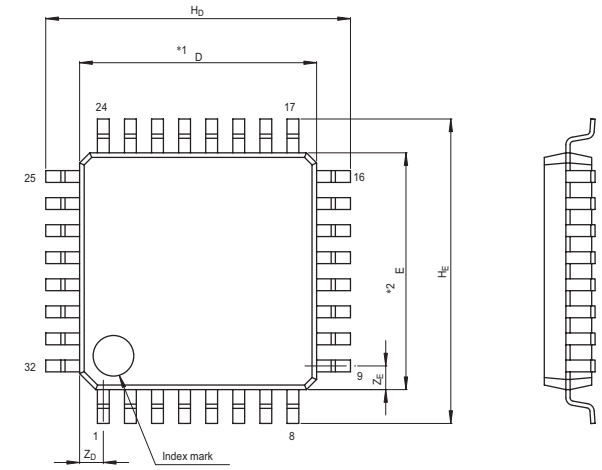
(1) Some of the user flash memory and RAM areas are used by the on-chip debugger. These areas cannot be accessed by the user.
See the on-chip debugger manual for which areas are used.
(2) Do not set the address match interrupt (registers AIENi and AIADRi (i = 0 or 1) and fixed vector table) in a user system.
(3) Do not use the BRK instruction in a user system.
(4) The debugging is possible with VCC in the range of 1.8 V to 5.5 V. Set the supply voltage to 2.7 V or above for rewriting the flash memory.

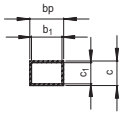
There are some special restrictions on connecting and using the on-chip debugger. For details, see the on-chip debugger manual.

Appendix 1. Package Dimensions

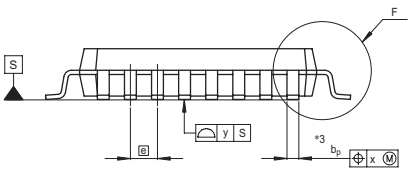
Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

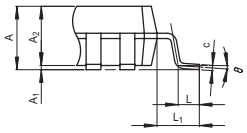
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP32-7x7-0.80	PLQP0032GB-A	32P6U-A	0.2g





Terminal cross section





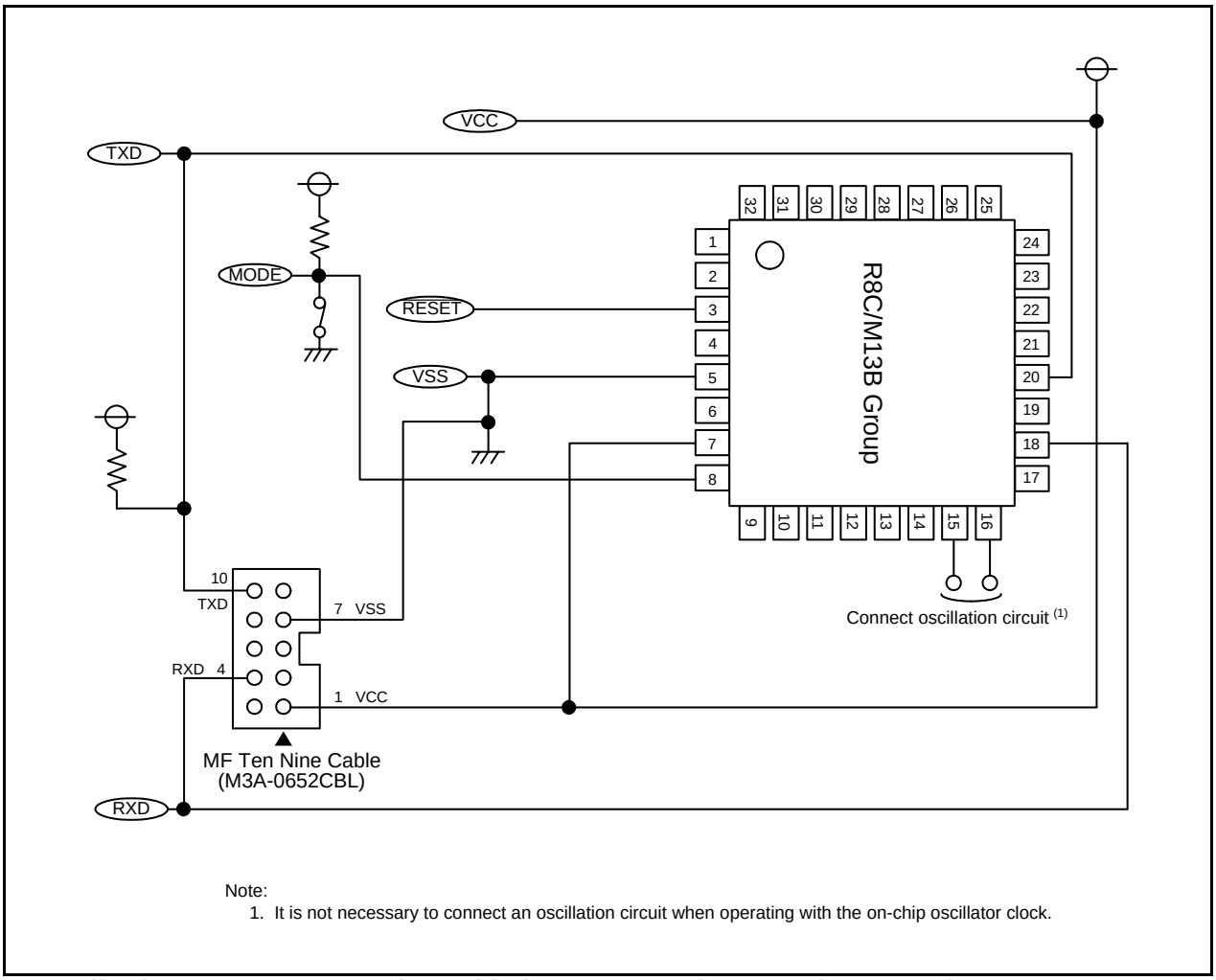
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.32	0.37	0.42
b_1	—	0.35	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.8	—
x	—	—	0.20
y	—	—	0.10
Z_D	—	0.7	—
Z_E	—	0.7	—
L	0.3	0.5	0.7
L_1	—	1.0	—

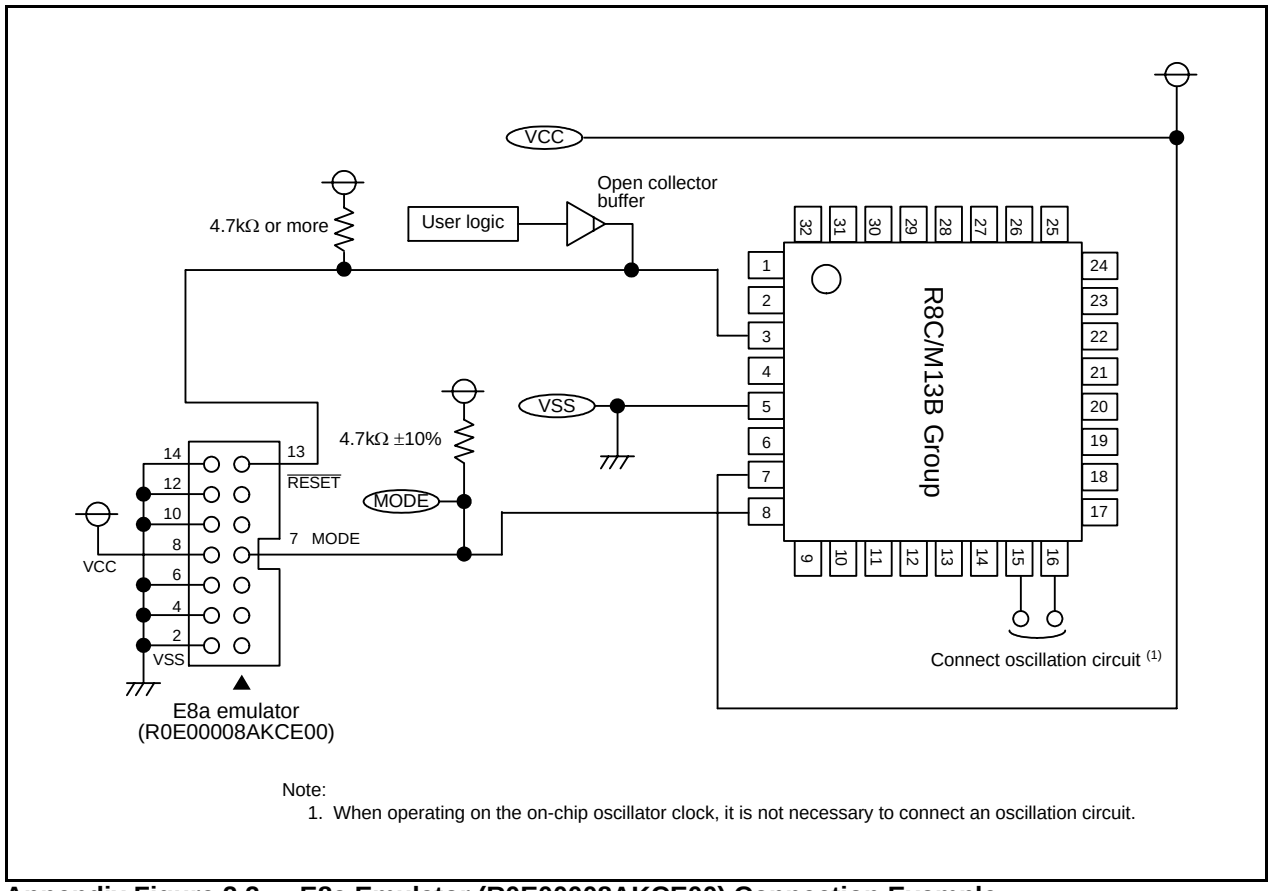
Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator

Appendix Figure 2.1 shows a MF Ten Nine Cable (M3A-0652CBL) Connection Example. Appendix Figure 2.2 shows a E8a Emulator (R0E00008AKCE00) Connection Example.



Note:
1. It is not necessary to connect an oscillation circuit when operating with the on-chip oscillator clock.

Appendix Figure 2.1 MF Ten Nine Cable (M3A-0652CBL) Connection Example

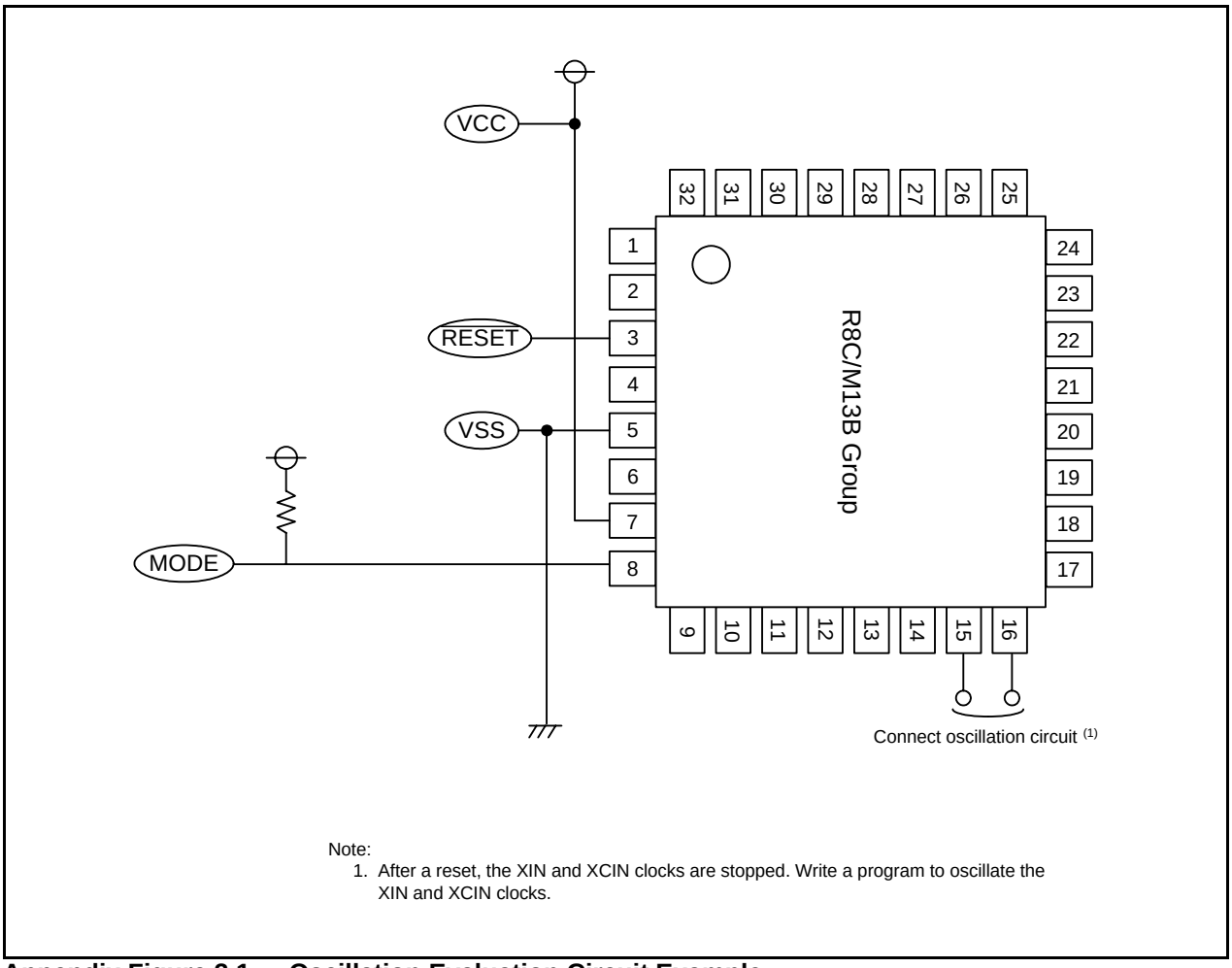


Note:
1. When operating on the on-chip oscillator clock, it is not necessary to connect an oscillation circuit.

Appendix Figure 2.2 E8a Emulator (R0E00008AKCE00) Connection Example

Appendix 3. Oscillation Evaluation Circuit Example

Appendix Figure 3.1 shows an Oscillation Evaluation Circuit Example.



Note:
1. After a reset, the XIN and XCIN clocks are stopped. Write a program to oscillate the XIN and XCIN clocks.

Appendix Figure 3.1 Oscillation Evaluation Circuit Example

Appendix 4. Comparison between R8C/M12A Group and R8C/M13B Group

Appendix Table 4.1 lists Specification Comparison between R8C/M12A Group and R8C/M13B Group.
For details on the R8C/M12A Group specifications, refer to the R8C/M11A Group, R8C/M12A Group User's Manual: Hardware.

Appendix Table 4.1 Specification Comparison between R8C/M12A Group and R8C/M13B Group

Item	Function	R8C/M12AGroup	R8C/M13B Group
Memory	ROM	2 KB, 4 KB, 8 KB	4 KB, 8 KB, 16 KB
	RAM	256 bytes, 384 bytes, 512 bytes	384 bytes, 512 bytes, 1K bytes
Clock generation circuit	XCIN clock generation circuit	Not available	Available
I/O port	Number of pins	20	32 Added ports: P2_2/TRCIOD/TRKI/SSO/SDA P2_1/TRCIOC/TRKO/SSCK/SCL P2_0/TRCIOB/TRKO/INT1 P3_1/XIN/TRBO P0_7/TRCIOC/TRKO P0_6/TRCIOD P0_5/TRCIOB P0_4/TRCIOB/TREO P0_3/TRCIOB/CLK1 P0_2/TRCIOA/TRCTRG/RXD1/IrRXD P0_1/TRCIOA/TRCTRG/TXD1/IrTXD P0_0/TRCIOA/TRCTRG
	Number of CMOS I/O ports	17	29 Added ports: P2_2, P2_1, P2_0, P3_1, P0_7, P0_6, P0_5, P0_4, P0_3, P0_2, P0_1, P0_0
Timer	Timer RE2	Not available	Available
	Timer RK	Not available	Available
Serial interface	UART1	Not available	Available
Clock synchronous serial interface	IIC/SSU	Not available	Available
IrDA interface		Not available	Available
A/D converter	Number of A/D channels	6 channels	8 channels Added channels: AN5, AN6
Package		20-pin LSSOP 20-pin DIP	32-pin LQFP

Appendix Tables 4.2 and 4.3 list the Register Comparison between R8C/M12A Group and R8C/M13B Group.
For details on the R8C/M12A Group registers, refer to the R8C/M11A Group, R8C/M12A Group User's Manual: Hardware.

Appendix Table 4.2 Register Comparison between R8C/M12A Group and R8C/M13B Group (1)

Related Function	Register	Address	Bit	Remarks
System Control	MSTCR	00012h	MSTTRE	Functions added
	MSTCR1	00017h	MSTUART1, MSTTRK, MSTICSU, MSTIRDA	Register added
Clock	EXCKCR	00020h	CKPT1, CKPT0	Functions changed
			XCRCUT, XCINNC1, XCINNC0, CKPT3, CKPT2	Functions added
	SCKCR	00022h	LSCKSEL	Functions added
Interrupt	ILVL1	00041h	ILVL11, ILVL10	Register added
	ILVL5	00045h	ILVL51, ILVL50	Functions added
	ILVL7	00047h	ILVL75, ILVL74	Functions added
	ILVL9	00049h	ILVL95, ILVL94	Functions added
	ILVLA	0004Ah	ILVLA1, ILALA0	Functions added
	IRR0	00050h	IRS1R, IRS1T, IRTE	Functions added
	IRR1	00051h	IRTK, IRIS	Functions added
P0	PD0	000A8h		Register added
	P0	000AEh		Register added
	PUR0	000B4h		Register added
	POD0	000C0h		Register added
	PML0	000C6h		Register added
	PMH0	000C7h		Register added
P1_0, P1_2, P1_4, P1_5, P1_6	PML1	000C8h	P12SEL1, P12SEL0, P10SEL1, P10SEL0	Functions changed
	PMH1	000C9h	P16SEL1, P16SEL0, P15SEL1, P15SEL0, P14SEL1, P14SEL0	Functions changed
P2_0, P2_1, P2_2	PD2	000AAh	PD2_2, PD2_1, PD2_0	Register added
	P2	000B0h	P2_2, P2_1, P2_0	Register added
	PUR2	000B6h	PU2_2, PU2_1, PU2_0	Register added
	POD2	000C2h	POD2_2, POD2_1, POD2_0	Register added
	PML2	000CAh	P22SEL1, P22SEL0, P21SEL1, P21SEL0, P20SEL1, P20SEL0	Register added
P3_1, P3_3, P3_4	PD3	000ABh	PD3_1	Functions added
	P3	000B1h	P3_1	Functions added
	PUR3	000B7h	PU3_1	Functions added
	POD3	000C3h	POD3_1	Functions added
	PML3	000CCh	P33SEL1, P33SEL0	Functions changed
			P31SEL1, P31SEL0	Functions added
	PMH3	000CDh	P34SEL1, P34SEL0	Functions changed
P4_2, P4_5, P4_6, P4_7	PML4	000CEh	P42SEL1, P42SEL0	Functions changed
	PMH4	000CFh	P47SEL1, P47SEL0, P46SEL1, P46SEL0, P45SEL1, P45SEL0	Functions changed
AN5, AN6	ADINSEL	0009Dh	ADGSEL1, ADGSEL0	Functions changed

Appendix Table 4.3 Register Comparison between R8C/M12A Group and R8C/M13B Group (2)

Related Function	Register	Address	Bit	Remarks
Timer RK	TMKM	00188h		Registers added
	TMKCR	00189h		
	TMKLD	0018Ah		
	TMKCMP	0018Bh		
	TMKIR	0018Ch		
Timer RE2	TRESEC (TRECNT)	00130h		Registers added
	TREMIN	00131h		
	TREHR	00132h		
	TREWK	00133h		
	TREDY	00134h		
	TREMON	00135h		
	TREYR	00136h		
	TRECR	00137h		
	TRECSR	00138h		
	TREADJ	00139h		
	TREIFR	0013Ah		
	TREIER	0013Bh		
	TREAMN	0013Ch		
	TREAHR	0013Dh		
	TREAWK	0013Eh		
	TREPRC	0013Fh		
UART1	U1MR	00190h		Registers added
	U1BRG	00191h		
	U1TBL	00192h		
	U1TBH	00193h		
	U1C0	00194h		
	U1C1	00195h		
	U1RBL	00196h		
	U1RBH	00197h		
	U1IR	00198h		
IrDA	IRCR	0019Ch		Register added
IIC/SSU	IICCR	00160h		Registers added
	SSBR	00161h		
	SITDR	00162h		
	SIRDR	00164h		
	SICR1	00166h		
	SICR2	00167h		
	SIMR1	00168h		
	SIER	00169h		
	SISR	0016Ah		
	SIMR2	0016Bh		

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		Page	Summary
0.01	Aug 24, 2010	—	First Edition issued
1.00	Mar 11, 2011	All pages	"Preliminary" and "Under development" deleted
		B-1	00021h, 00028h, 00030h, 00035h, 000DEh and 000E7h revised
		1	1.1 "Power consumption is low, ... with countermeasure circuits." → "Power consumption is low, ... EMI/EMS performance."
		2	Table 1.1 Watchdog timer: revised
		7	Table 1.4 "Voltage Detection Circuit" deleted
		8	Table 1.5: Description revised
		13	3.1 "02FFFh" → "02FFh"
		14	Table 3.1 00021h, 00028h, 00030h to 00033h, 00035h revised
		17	Table 3.4 000DEh and 000E7h revised
		18	Table 3.5 00167h revised
		22	Table 3.9 Notes 1 and 2 revised
		23	4. revised
		24	Table 5.2 Notes 3 and 4 revised
		25	5.2.1 "For details, see 6. Resets." added
		26	5.2.2 After Reset: "MSTINT" → "MSTINI", Note 4 revised "When changing ...I function beforehand." added
		27	5.2.3 b3 revised, 5.2.4 Note 1 added
		28	5.2.5 b2: "Set to 0." → "Set to 1.", "When changing ...I function beforehand." added
		31, 32	5.2.7 and 5.2.8 Note 1 revised
		33	Table 5.2 "PRC3" revised, 5.4 "Table 5.3 lists ... Register (HRPR)." and Table 5.3 added
		37	Table 6.2 Notes 2 and 3 revised, 6.2.1 "For details, see 6. Resets." added
		40, 41	6.2.3 and 6.2.4 Note 1 revised
		42	Figure 6.2 Note 1 revised
		43	6.3.2 "Figure 6.3 shows ... " deleted
		44	Figure 6.3 deleted
		62	"7.6 Digital Filter for Voltage Detection Circuits 0 and 1" and Figure 7.6 added
		63	Table 8.1 revised, Note 1 deleted
		64	Figure 8.1 revised
		65	Table 8.2 and 8.2.1 title revised, Note 1 "Do not write ... set to 1." deleted
		66	8.2.2 revised, 8.2.3 After Reset revised
		67	8.2.6 title, b6 bit name, and "[Condition for setting to 1]" revised, Note 1 added
		68	8.3.1.1 "In addition, ... set to 1." added, Figure 8.2 revised
		69	Table 8.3 Specification revised, Note 2 deleted
		70	Table 8.4 Specification revised, Notes 1 to 3 deleted
		71	Table 8.5 revised, Note 1 added, Figure 8.3 "and ... period: 25 %)" added
		72	8.4 revised
		73	Table 9.1: "Clock frequency", "Others" revised, Notes 2 and 4 deleted
		74	Figure 9.1 revised
		76	Table 9.3 Register Name revised, "XCIN Clock Control Register" added

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1.00	Mar 11, 2011	77, 78	9.2.1 b0 to b3: Function revised, "Bits CKPT0 to CKPT1", "Bits CKPT2 to CKPT3", "XRCUT Bit", and "XCRCUT Bit" revised
		79	9.2.2 "HOCOE Bit" and "LOCODIS Bit", Table 9.5 revised
		80	9.2.3 b0 to b2: Bit Name and Function revised, b6 and b7 Function revised, "LSCKSEL Bit" deleted
		81	9.2.4 revised
		82	9.2.5 b0 Function and "SCKSEL Bit", "WCKSTP Bit" revised
		83, 84	9.2.6 b5: Bit Name revised, b6 and b7: Bit Name and Function revised, Note 1 added, "Bits CKST0 to CKST3" and Table 9.7 revised, "WAITRS Bit" and "STOPRS Bit" deleted
		85	9.2.7 b2: Bit Name, b1 and b2: Function, Note 1 and "[Condition for setting to 1]" revised, 9.2.8 added
		87 to 89	9.3.1 to 9.3.4 revised
		90 to 93	9.4.1 to 9.4.5 revised, 9.4.6, 9.4.6.1 and 9.4.6.2 added
		94	9.5 "The XINHALT bit in the BAKCR register = 1" → "The XINHALT bit in the BAKCR register = 0", 9.5.1 "See 11.8 ... interrupt sources." added
		95, 535	9.6.2 and 25.3.2 "When the MCU is ... to the chip." deleted
		97	Figure 10.1 revised
		99	10.2.1 and 10.2.2 "fHOCO can be ... 1 (high-speed on-chip oscillator on)" deleted
		100	10.3 and 10.3.1 "that use these clocks" → "that use the system clock and ... by the prescaler"
		101 to 104	10.3.4 revised, Table 10.3 "Watchdog timer interrupt" deleted, Figure 10.3 added
		105	10.4.2 revised
		106	10.4.3 revised
		107 to 110	10.5, 10.5.1 to 10.5.12 added
		111, 536	10.6.1 and 25.4.1 revised
		112	Table 11.1 "Enable or" deleted
		115	11.2.1 Note 1 added
		117	Note 1 "KIiPL bit" → "bits KIiPL or KIiEN"
		119	11.2.6 and 11.2.7 "See 11.4.2.1 ... peripheral function interrupts." added
		120	11.2.8 b0 and b1 "Set to 0." → "The read value is 0.", "The IRR2 register is ... peripheral function interrupts." added
		122	11.2.10 and 11.2.11 "This register remains ... or software reset." added
		123	Table 11.5 BRK instruction: "0FFE7h" → "0FFE6h"
		125	11.4.2 revised, 11.4.2.1
		126	Table 11.7 and 11.4.2.2 added
		127	11.4.3 "Each flag ... IRR3 = 1" → "The interrupt request ... flag (IRR3) = 1"
		128	11.4.4 (1) revised
		130	11.4.7 revised, Note 1 added
		133	Figure 11.8 Note 1 deleted
		134	11.5.1 "Several input ... to $\overline{\text{INT0}}$". → "The input ... can be selected."
		135	11.5.2 "The $\overline{\text{INTi}}$ input ... in the INTF0 register" deleted
		136	Figure 11.11 revised
		138	Figure 11.12 revised

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1.00	Mar 11, 2011	140 to 142, 538 to 540	11.9.4, 11.9.5, 25.5.4 and 25.5.5 revised, 11.9.6 and 25.5.6 added
		145	Table 12.3 Port PA Mode Control Register: "00010001b" → "00010011b"
		146	12.2.1 b7 Bit Name revised, "[When the IOINSEL ... register is 0]" and "[When the IOINSEL ... register is 1]" added
		148, 154, 163, 168, 175, 180	12.3.2, 12.4.2, 12.5.2, 12.6.2, 12.7.2 and "[When the IOINSEL ... register is 0]" and "[When the IOINSEL ... register is 1]" deleted
		155, 169	12.4.4, 12.6.4 Note 1 added
		161	Table 12.19 revised
		183	Table 12.37 revised
		184, 186 to 189	Figures 12.8, 12.9, 12.11 to 12.15 revised
		185	Figure 12.10 added
		194	Figure 12.21 revised
		196, 541	12.13.1, 25.6.1 revised, 12.13.2 and 25.6.2 added
		197	13. revised, Table 13.1 Operating modes and Count source revised
		198	Figure 13.1 revised
		199	Table 13.2 Function revised, Note 1 added
		200	Table 13.3 Register Name revised, 13.3.1 Note 2 revised
		201	13.3.2 Note 3 deleted, "Use the MOV instruction ...write 1 to these bits." added
		203	Table 13.6 "I/O port" → "Not used"
		205	13.3.6 title revised
		208, 209	13.4.3 and 13.4.4 revised
		213, 542	13.5 and 25.7 (3): "external event" → "external pulse", (13) added
		215	14.2 "Do not use ... INT0 pin enabled)." deleted
		216	Table 14.3 Register name revised
		217	14.3.1 Notes 2 and 3 deleted
		224	14.3.8 title revised
		237	Table 14.7 Programmable wait one-shot generation mode: "(3)" deleted
		250	15.2.1 "Do not ....in 16-bit units." → "TRCCNT register ... in 8-bit units."
		251	15.2.2 "TRCCRD" → "TRCGRD", "Do not .... are FFFFh." → "When these registers ... are FFFFh."
		253	15.2.4 b5 and b6: Function revised
		272	Table 15.12: Note 1 revised
		279	Figure 15.19 revised
		282	15.4.1 "TRCIOD" → "TRCIOB"
		283 to 285	Figures 15.23 to 15.26 "TRCOAE_XN" → "TRCOBE_XN"
		286	Figure 15.27 revised
		291, 545	15.6.2, 15.6.4, 25.9.2 and 25.9.4 "CPU clock" → "system clock", 15.6.7, 25.9.7 "MSTR Register" → "MSTCR Register"
		355	Figure 18.2 revised
		360	18.2.6 revised
		371	Table 18.8: Note 1 revised

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1.00	Mar 11, 2011	379	19.4 (1), (7), (9) added
		386	Table 20.6 revised
		389	20.2.3 Note 1, 20.2.4 Note 2 revised
		427	20.4.2.4 (4) revised, "• Flow for Generating Repeat Start Condition during Master Receive Mode" added
		430, 433	20.4.2.5, 20.4.2.6 (2) revised
		446	Table 21.1 revised, Note 1 added
		447	Figure 21.1 and Table 21.2: Function revised
		449	21.2.1 "If any of ... will be undefined." → "When the ADi ... 8-bit units."
		450	21.2.2 revised
		451	21.2.3 "If the content ... will be undefined." → "The ADINSEL ... is stopped"
		452, 453	21.2.4 and 21.2.5 revised
		454	21.3, 21.3.1.1, Figure 21.2 revised
		455	Table 21.6 and Figure 21.3 revised, Note 3 added, Table 21.7 deleted
		456	21.3.2 (1) and Figure 21.4 revised
		457	21.3.3 (2), (3) and Figure 21.5 revised
		458	21.3.4, Figure 21.6 revised
		459	21.3.5, Figure 21.7 revised
		460	21.4 revised, 21.5 deleted
		461, 462, 552, 553	21.5.1 to 21.5.3, and 25.14.1 to 25.14.3 revised, 21.5.2, Figure 21.10, 25.14.2, Figure 25.4 deleted
		464	Table 22.2: Note 1 added
		469	Table 22.4 step 4: "(TBD μs max.)" → "(100 μs max.)"
		479	23.5.2 Note 2 revised, Note 5 added
		482	23.5.4 Note 2 added, "FMR27 Bit" revised
		483	23.5.5 revised, Function: "TBD kHz" → "60 kHz",
		485	Table 23.7: Note 3 added
		487	Figures 23.5 and 23.6 revised
		489	Table 23.8 revised, 23.6.6.1 added
		490, 494	Figure 23.8 and 23.12 to 23.14 title revised
		491, 492	Figures 23.9 and 23.10 title, Note 1 revised
		493	"When the FMR22 bit is ... rewritten in EW1 mode.", Figure 23.11 added
		497	"When the FMR22 bit is ... rewritten in EW1 mode.", Figure 23.15 added
		501	Table 23.9: Note 1 revised
		504	Figure 23.20 revised
		509, 555	23.8.2.9, 23.8.2.10, 25.15.2.9, and 25.15.2.10 deleted
		517	Table 24.11 revised
		519	Tables 24.10 and 24.11 revised, Note 3 deleted
		522	Table 24.14 revised
		523, 527, 531	Tables 24.15, 24.21, 24.27 "R_{fXCIN}" added
		524, 528, 532	Tables 24.16, 24.22, 24.28 revised

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1.00	Mar 11, 2011	525, 529, 533	Tables 24.17, 24.23, and 24.29 revised Figures 24.8, 24.12, 24.16 revised
		526, 530, 534	Tables 24.19, 24.25, 24.31 revised Figures 24.10, 24.14, 24.18 revised
		559, 561	Appendix Figures 2.1, 2.2, 3.1 revised
2.00	Mar 07, 2012	B-1, 14, 76, 85	"XCIN Clock Control Register" deleted
		4	"Under development" deleted
		54, 105, 106, 108, 111, 546	7.2.2 Note 1, 10.4.1, 10.4.3, Figure 10.5 Note 5, 10.6.2, and 25.4.2 "clocks are stopped" → "all clocks are stopped"
		81	9.2.4 b7 to b0: Bit Name revised
		83	9.2.6 Note 2 added
		84	9.2.6 Bits CKST0 to CKST3: Description revised
		87	9.3.1 Description, Figure 9.3 revised
		88	9.3.2 Description, Figure 9.4 revised
		90	9.4.4 Table 9.8 revised
		91	9.4.5 Description revised
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		97	Figure 10.1 revised
		100	10.3 Description revised
		102	10.3.4 Description revised, Figure 10.2 title revised
		105	10.4 and 10.4.2 Description revised
		107	10.5.5 Description revised
		109	Figure 10.6 revised
		111, 546	10.6.1, 10.6.2, 25.4.1, and 25.4.2 revised
		118, 121	11.2.5 and 11.2.9 Description revised
		119	11.2.7 b0 and b1: Function revised
		122	11.2.10 and 11.2.11 Description revised
		134	11.5.1 Description revised
		135	Figure 11.10 revised
		140, 548	Figure 11.13 and 25.1 Note 2 added
		143, 551	"11.9.7 Changing Interrupt Priority Levels and Flag Registers" and "25.5.7 Changing Interrupt Priority Levels and Flag Registers" added
		199	Figure 13.1 revised
		201	13.3.1 Note 3 added
		203	13.3.3 b6 and b7: Function revised
		204	13.3.3 Bits TIOGT0 to TIOGT1: Description added
		205	13.3.4 Note 1 deleted, description added
		207	13.4.1 and Figure 13.2 revised
		208	Figure 13.3 revised
		209	Figure 13.4 revised
		212	Figure 13.7 revised

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2.00	Mar 07, 2012	214, 553	13.5 and 25.7 (3) revised, (5) deleted, (13) added
		218	14.3.1 Note 1 revised
		219	14.3.2 b0 and b1: Function revised, description added
		220	Table 14.4 "Timer mode" revised
		221	14.3.4 Note 2 revised
		223	14.3.6 Note 1 added
		224	14.3.7 Description revised
		226	14.4.1 Description revised
		228	14.4.2 Description revised
		231	14.4.3 Description revised
		234	14.4.4 Description revised
		239	14.5.2 Description revised
		240 to 243	Figures 14.10 to 14.13 revised
		246, 247, 554, 555	14.8 and 25.8 revised
		248	Table 15.1 "Operating clock" added
		251	15.2.1 Description revised
		252, 253	15.2.2 Description deleted, Tables 15.5 to 15.8 added
		254	15.2.3 Notes 1 and 2 revised
		255	15.2.4 b7: Function revised, Note 3 added
		257	15.2.6 Note 1 added, Table 15.9 Note 2 added
		258	15.2.7 b0, b1, b4, b5 : Function revised, Note 1 revised
		259, 260	15.2.8 b0, b1, b4, and b5: Function revised, Note 8 added
		260	15.2.9 b5 : Function revised, Notes 1 to 3 added, CSTP Bit and Bits TCEG0 to TCEG1: Description deleted
		261	15.2.10 Description deleted, b0 to b4: Function revised, Notes 1 and 2 added.
		262	15.2.11 Note 3 added
		265	Table 15.10 revised
		266	15.3.1 Description revised
		270	15.3.2 Description revised
		272	Figure 15.10 and title revised
		281	Figure 15.19 revised
		283	15.4.3 Description revised
		285	15.4.4 Description revised
		286	Figure 15.24 revised
		290	Figure 15.31 revised
		292	15.5.8 revised
		293	"15.6 Timer RC Interrupt" added
		294, 295, 556, 557	15.7.4, 15.7.5, 25.9.4, and 25.9.5 revised
		298	16.2.2 Note 2 added
		299	16.2.3.2 Description revised

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		320	Table 17.5 "TREIFR" revised
		322	17.2.11 b4: Function revised, Note 2 added
		323	17.2.12 Note 1 to 3 added
		327	"ALIE Bit" description deleted
		329	17.2.17 Description revised
		337	Figure 17.5 revised
		338	17.3.3.1 Description revised, Figure 17.6 deleted
		339	17.3.3.2 Description revised
		340	17.3.4.1 Description revised
		341	Figures 17.8 and 17.9 titles revised
		344, 345	Figures 17.12 to 17.14 revised
		347	17.3.5 Notes 1 and 2 added
		348	Figure 17.15 revised
		352	Figure 17.19 revised
		353	Figure 17.20 revised
		356	18.1 Description revised
		359	18.2.1 Notes 1 to 3 added
		363	18.2.6 Note 1 revised, Note 2 added
		370	Table 18.6 Note 2 added
		376	18.4 Description revised
		379	19.2.1 Bits IRCKS0 to IRCKS2: Description revised
		382	19.4 revised
		393	20.2.5.1 b4 and b7: Function revised
		394	20.2.5.2 Note 8 added
		395	20.2.6.1 b1 and b3: Function revised, Note 1 added
		396	20.2.6.2 b2 and b5 revised, Note 8 added
		398	20.2.7.2 Note 1 added
		400	20.2.8.2 b5: Function revised, Note 3 added
		402	20.2.9.2 Note 7 added
		432	Figure 20.22 revised
		435	Figure 20.24 revised
		437	Figure 20.26 revised
		439	Figure 20.29 revised
		449, 561	"20.5.3 ICE Bit in SICR1 Register and SIRST Bit in SICR2 Register" and "25.13.3 ICE Bit in SICR1 Register and SIRST Bit in SICR2 Register" added
		450	Table 21.1 "Conversion time" revised
		456	21.2.4 ADST bit: Description revised
		459	Table 21.6 and Notes 1 and 2 revised
		460 to 463	Figures 21.4 to 21.7 revised
		465, 562	21.5.2 and 25.14.2 revised

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2.00	Mar 07, 2012	479	23.3.2.1 and 23.3.2.2: Description revised
		480	23.4 Description revised
		481	23.5.1 "After Reset" revised, Notes 1 to 4 added
		482	23.5.1 RDYSTI and BSYAEI: Description revised
		483	23.5.1 Bits FST2 to FST6: Description revised, FST7 bit: Description added
		484	23.5.2 Notes 2 to 4, FMSTP bit description revised, FMR01 and FMR02 bit description added
		485	23.5.2 CMDRST, CMDERIE, BSYAEIE, and RDYSTIE bit description revised
		486	23.5.3 FMR13 bit description revised
		487	23.5.3 FMR16 and FMR17 bit description added
		488	23.5.4 Note 2 and FMR22 bit revised, FMR20 bit description added
		489	23.5.4 FMR27 bit description revised
		491	23.6.1 Description revised
		492, 493	Figures 23.3 and 23.4 revised
		495	23.6.5 Description revised
		496	23.6.6 and 23.6.6.1: Description revised
		497	23.6.6.2 and 23.6.6.3: Description revised
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		507	Figure 23.18 revised
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		511	Tables 23.10 revised
		512	Tables 23.11 revised
		514, 515, 565, 566	Tables 23.12, 23.13, 25.1, and 25.2 revised
		516, 567	23.8.2.6 and 25.15.2.6 revised
		517, 518, 568, 569	"23.8.2.9 EW1 Mode" and "25.15.2.9 EW1 Mode" added
		519, 570	"23.8.3 Notes on flash memory stop and operation transition" and "25.15.3 Notes on flash memory stop and operation transition" added
		522	Table 24.3 revised
		574	Appendix Figure 2.1 Note 1 revised
		577 to 579	"Appendix 4. Comparison between R8C/M12A Group and R8C/M13B Group" added

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